*Application Note*

# *AM62x Schematic Review Checklist*

*EP Processors Sitara MPU*


**ABSTRACT**

This application report shows examples and documents that specifically reference AM62x devices. Links for additional AM62x product pages and reference documents are added as they become available.


## Table of Contents



## Trademarks

# 1 Introduction

This document applies to the following devices:

- AM62x Schematic Checklist:
  - AM6254
  - AM6252
  - AM6251
  - AM6234
  - AM6232
  - AM6231

Refer sections on *Tools and Software* and *Documentation Support* sections in the *AM62x Sitara Processors Data Sheet* for links to other documents on hardware and software.

# 2 Recommendations Specific to AM62x

## 2.1 EVM versus Data Sheet

In case of any discrepancy between the TI EVMs and the device-specific data sheet, always follow the data sheet. Despite the designer's best efforts, the EVMs may contain errors that may still function but are not completely aligned with the data sheet specification. Thus, the EVM designs should not be considered as reference designs to be blindly reused.

## 2.2 Power

- **Have you used the output of the power model and estimates from the rest of your design to determine the power solution needed?**

  The power needed for each rail of the AM62x SoC varies based on the interfaces used and the environment in which it is operating. Power requirements must be determined using the power model.
- **Have you checked that the correct voltages are applied to the correct power pins on the device?**

  The SoC includes a number of power rails which must be powered with the specified voltage for proper operation.
- **Have you checked that all signals connected to each of the power domains are operating at the same voltage level?**

  The AM62x SoC includes nine dual-voltage I/O domains, where each domain provides power to a fixed set of I/Os. Each I/O power domain can be configured for 3.3 V or 1.8 V, which determines a common operating voltage for the entire set of I/Os powered by the respective I/O power domain. All signals connected to these domains must operate from the same power source that is being used to power the respective VDDSHVx supply rail. The AM62x I/O buffers are not failsafe. The voltage for the VDDSHVx rail must be present before any voltage is applied to the associated I/Os.
- **Do you have the required capacitor value connected to each output of the internal LDOs?**

  The AM62x SoC includes nine internal LDOs with the output of each connected to a pin on the device. The LDOs require an output capacitor connected between each of these pins. Each CAP_VDDS_x pins requires a 1uF capacitor on each. Low inductance capacitors and low loop inductance connectivity is required for these capacitors.
- **Does your design meet the power sequencing requirement recommended in the data sheet?**

  Proper power supply sequencing in proper correlation with resets and clocks is required. For the recommended power sequencing requirements, see the device-specific data sheet.
- **Has the PDN analysis been performed and are the proper values and number of bypass capacitors included in your design?**

  Use low ESL capacitors and mount them with short traces to keep the mounting inductance very low. This is required to meet the specified PDN impedance. For more information, see *Sitara Processor Power Distribution Networks: Implementation and Analysis*.
- **How are you connecting VDD_CANUART?**

For more information, see the *Recommended Operating Conditions* table in the *AM62x Sitara Processors Data Sheet*.

- **What features are you trying to implement in the power delivery network for your design?**

  Ensure that your power source follows the *Power Sequencing* defined in the *AM62x Sitara Processors Data Sheet*.
- **If dynamic adjustment of VDD_CORE is not required, can this be tied to VDDR_CORE?**

  Dynamic voltage change on VDD_CORE is not supported on AM62x. For more information, see the *Recommended Operating Conditions* table and *Power Sequencing* section of the *AM62x Sitara Processors Data Sheet*.
- **If MCU subsystem is not used, how do VDDS_OSC0, VDDA_MCU and CAP_VDDS_MCU need to be terminated**

  Not powering the above power rails is not an option on AM62x. CAP_VDDS_MCU requires the recommended capacitor (1 µF) connected to it.
- **If eFuse ROM programming is not done, how does VPP need to be terminated?**

  This is covered in the *VPP Specifications for One-Time Programmable (OTP) eFuses* section of the *AM62x Sitara Processors Data Sheet*. Further, during normal operation, when the eFuse array is not being actively programmed, the VPP source needs to beterminated to 0V. One option to implement this is to use an LDO providing an active discharge function for their output when disabled. The other option is to use a pull-down to hold the LDO output to 0 V when it is disabled. The **pull-down** resistor value needs to be to selected such that it doesn't allow any leakage path through the LDO to source a potential greater than 0 V when disabled.
- **If the voltage monitor is not used for 1.8 V/3.3 V functions, how do the VMON_1P8_SOC and VMON_3P3_SOC pins need to be terminated?**

  Not connecting these pins to the appropriate power rails is not an option. Refer *System Power Supply Monitor Design Guidelines* in the *AM62x Sitara Processors Datasheet* for more information.

## 2.3 Unused Signals

Signals on unused interfaces can typically be left as no connect, unless otherwise stated. Many of the IOs have a Pad Configuration Register which provides control over the input capabilities of the IO (RXENABLE field in each conf_<module>_<pin> register). For more details, see the *Control Module* chapter of the *AM62x Sitara Processors Technical Reference Manual*. Software should disable the IO receive buffers (that is, RXENABLE=0) that are not connected in the design as soon as possible during initialization. Software needs to ensure that it does not accidentally enable the receiver of an IO (by setting the RXENABLE bit) when the associated pin is floating.

**Note**

For specific guidance on certain unused pins, see the *Pin Connectivity requirements* section in the *AM62x Sitara Processors Data Sheet*

**Note**

For specific guidance configuring IOs, see the *Pad Configuration Registers* chapter in the *AM62x Sitara Processors Technical Reference Manual*.

## 2.4 Reset

- **Do you have a reset circuit that generates the proper reset signals into MCU_PORz, MCU_RESETz and RESET_REQz?**

  The reset signal MCU_PORz must meet the requirements for pulse length and must be held low during power sequencing. For more information, see the *System Timing* section in the *AM62x Sitara Processors Data Sheet*

  For guidance on MCU_RESETz and RESET_REQz, see the *Pin Connectivity requirements* section in the *AM62x Sitara Processors Data Sheet*
- **Does your system contain any inputs which need to be held to valid logic levels during initialization?**

The inputs that are used to configure the AM62x device (BOOTMODExx inputs) and must be held in the desired known state to select the appropriate bootmode as defined in the *AM62x Sitara Processors Data Sheet* and *AM62x Sitara Processors Technical Reference Manual*, until after the rising edge of the MCU_PORz. The system might contain other devices that require bootstrap configurations, that is, Ethernet PHYs. External pull resistors might need to be used for all such pins, depending on whether the associated device does not have internal pull capability.

## 2.5 Boot Modes

- **Do all BOOTMODE inputs require external pulling resistors or a circuit to drive these inputs to a valid state that defines the desired boot mode.**

  BOOTMODE inputs do not have internal pull-up or pull-down resistors that are active during power up and reset. External pulling resistors must be used to set the boot mode. Alternatively, a buffer that is only driven when reset is active can be used to present the boot mode. MCU_RESETSTATz can be used to enable this buffer when it is low.
- **Is the expected boot configuration present on the BOOTMODE pins when PORz_OUT is active (low)?**

  PORz_OUT should be used as an enable signal for any bootmode buffers on signals that are also used for I/O. If the I/O pins associated with boot mode inputs are redefined for another signal function during operation, they must be released and set back to the proper levels to select the boot mode whenever the SoC enters the cold reset state. This problem may occur when an external device may attempt to drive the bootmode signals.
- **Are you using Ethernet Boot and RGMII?**

  You must implement a PHY that enables RGMII_ID mode on the PHY RX data path and disables RGMII_ID mode on the TX data path by default (the SoC implements RGMII_ID on the TX channel). The SoC ROM is PHY agnostic and will not programatically enable/disable RGMII_ID mode on attached PHYs. Typically, this is accomplished via pin strapping on the PHY.

## 2.6 Clocking

- **Do you have a clock source for MCU_OSC0_XI?**

  A clock source for MCU_OSC0_XI is required for proper operation of SoC.
- **Is the frequency for MCU_OSC0_XI 25 MHz?**

  24, 25 and 26 MHz are the supported input clock frequencies.
- **Did you implement passive components around the crystal?**

  For more details, see the *MCU_OSC0 Internal Oscillator Clock Source* section in the device *AM62x Sitara Processors Data Sheet*
- **Are you using WKUP_LFOSC?**

  If WKUP_LFOSC0_XI/XO is not being used
  – • XI needs to be connected directly to VSS
  – • XO needs to be left unconnected

  This is covered in the *WKUP_LFOSC0 Not Used* section of the *AM62x Sitara Processors Data Sheet*

## 2.7 System Issues

**Pull-up Resistors**:

- **Are all pullups connected to the AM62x device pulled up to the correct I/O voltage?**

  Pulling a signal to the wrong I/O voltage can cause leakage between the I/O rails of the device. Each terminal has an associated supply voltage used to power its I/O cell. This can be found in the *Ball Characteristics* table in the *AM62x Sitara Processors Data Sheet*.

**Peripheral clock outputs:**

- **Do you have series termination resistors on the clock outputs?**

  Put 22-Ω series resistors (close to processor) on the output clocks of the SPI module.

**General Debug:**

- **Have you added visibility for the internal clocks MCU_SYSCLKOUT0, SYSCLKOUT0 and CLKOUT0?**

  Output clocks MCU_SYSCLKOUT0, SYSCLKOUT0 and CLKOUT0 are available on pins. You should consider attaching short signal traces with test points to allow monitoring of internal clocks to enable hardware and software debug if the pins/signals are not muxed to other signal functions in your design.
- **Have you added the ability to probe the MCU_RESETSTATz, RESETSTATz and PORz_OUT signals?**

  Accessible test points for MCU_RESETSTATz, RESETSTATz and PORz_OUT are useful for debug.

## 2.8 DDR

Ensure that you have implemented all recommendations found in *AM62x DDR Board Design and Layout Guidelines* for your specific DDR interface type.

## 2.9 MMC

**Under Revision**

## 2.10 OSPI and QSPI

- **Is the OSPI0_LBCLKO signal connected correctly for the device you have selected?**

  The OSPI0_LBCLKO signal is used differently depending on what type of device you are using and whether internal pad loopback is used. For more information, see the *AM62x Sitara Processors Technical Reference Manual*.
- **Are the OSPI/QSPI data bits connected in the proper order?**

  D0 and D1 of the OSPI peripheral must be connected to D0 and D1 of the QSPI/OSPI memory to support legacy x1 commands. Data swapping is not allowed.

## 2.11 GPMC NAND

- **Does your design use the NAND R/B# signal**

  Typically, the active high ready / active low busy (R/B#) output from the NAND is open drain and connected to the GPMC0_WAIT0 signal. A 4.7K pullup must be connected between this signal and the respective I/O power source if the R/B# output is open-drain.
- **Do you have pullup resistors on GPMC0_CSn?**

  It is recommended to have an external pull-up resistor on GPMC0_CSn to hold the signal high when AM62x SoC is held in reset, or after reset, before software has configured padconfig registers to enable the Tx buffer.

## 2.12 I2C

- **Do you have the I2C pull-ups connected to the correct voltage?**

  I2C interfaces require a pull-up resistor on both the data and the clock lines. 4.7K-Ω pull-up resistors must be attached on both I2C signals (x_SDA and x_SCL). Ensure the pull-up resistors connect to the correct I/O voltage rail. For more information, see the note on the *Pull-up Resistors* bullet in Section 2.7.
- **Do you need a fully compliant I2C buffer?**

  The WKUP_I2C0 and MCU_I2C0 use true open-drain buffers that are fully compliant to the I2C specifications. These support 100-kHz and 400-kHz operation. The remaining I2C interfaces, I2C0-I2C2, use LVCMOS to emulate an open-drain buffer. These can support 3.4-Mbps I2C operations; however, these ports are not fully compliant with the I2C specification, in particular falling edges are too fast (< 2 ns). Any devices connected to these ports must be able to function properly with the faster fall time.

## 2.13 CPSW Ethernet

- **Have you correctly configured the initial configuration for your PHY?**

  Most PHYs configure their outputs as inputs during reset, and captures configuration information on theses I/Os when the device is released from reset. Therefore, it may be necessary to apply appropriate pull-up/pull-down resistors on these I/Os which also connect to AM62x I/Os. The TI PHYs used on the GP EVM use a combination of pull-up and pull-down resistors to generate a mid-level voltage, allowing multiple configuration

bits to be encoded on each pin. By default, the AM62x input buffers and internal pull-up/pull-down resistors are disabled, which eliminates any concern with a mid-supply potential being applied to the AM62x input buffer when required by the PHY. The PHYs should be removed from reset before enabling any of the associated AM62x input buffers to ensure the PHY is driving a valid logic state before enabling the AM62x input buffers.

- **Have you terminated your RGMII signals correctly?**

  A 22-Ω series termination resistor is recommended (but optional) to be placed on each of the 12 RGMII interface signals as close as possible to the sourcing pin.

## 2.14 PRUSS-M

**Have you selected the correct pins for your industrial application?**

PRUSS-M pins allow muxing at the PRUSS IP level and at the SoC level using the PADCONFx registers. Carefully check that you have connected your schematic correctly for your application.

## 2.15 USB2 - High Speed

- **Have you planned for the routing of the USB interface?**

  For detailed recommendations on proper USB signal connection and routing, see the *High-Speed Interface Layout Guidelines*. Add appropriate constraints or routing requirements to your schematic. This will vary from tool to tool.
- **Have you included the correct VBUS decoupling for your configuration?**

  USB device operation requires decoupling capacitance of less than 10 µF connected to the USB VBUS. USB host operation requires decoupling capacitance of greater than 120 µF connected to the USB VBUS. VBUS decoupling capacitance should be connected close to the USB connector.
- **Have you connected the USB_DP and USB_DM signals directly to the connector?**

  USB_DP and USB_DM should never have any series resistors or capacitors on these signals. These signals should be routed with traces that do not include stubs or test points. These traces should be connected directly between the SoC and the connector, unless EMI control is needed.
- **If you are including a USB hub, have you connected the USB signals correctly?**

  USB_DP and USB_DM should be connected directly to the USB hub upstream port. The hub then distributes these signals to the downstream ports as needed. The connector ID should be grounded to enable host mode. As each hub has different implementation requirements, the customer should seek implementation advice from the hub manufacturer.
- **Do you need components for EMI and ESD protection?**

  Common-mode chokes may be needed for EMI/EMC control. These may reduce the signal amplitude and degrade performance. In addition, ESD suppression may also be required. If necessary, these components should be included in the design.
- **How are you connecting the USBn_VBUS signal?**

  This should be connected in accordance with the *USB Design Guidelines* section in the *AM62x Sitara Processors Data Sheet*. The voltage divider/clamp circuit must be implemented for proper operation. The Zener diode can only be potentially removed if one is absolutely sure that the product will never experience a VBUS signal potential greater than 6 V. The voltage range for the VBUS pin are defined in the *Absolute Maximum Ratings* table. If the system is designed to operate AM62x in USB host mode only, the relevant USBn_VBUS pin(s) should be left unconnected.

## 2.16 JTAG and EMU

To ensure a proper implementation of the JTAG interface, see the *Emulation and Trace Headers Technical Reference Manual* and the *XDS Target Connection Guide*.

- **Have you included a JTAG connection?**

  If the JTAG and EMU interface is not used, all pins except TRSTn, TCK, and TMS can be left floating. TRSTn must be pulled low to ground through a 4.7k-Ω resistor. TCK and TMS must be pulled separately to VDDSHV_MCU through a 4.7k-Ω resistor. However, TI strongly recommends that all board designs contain

at least a minimal JTAG port connection to test points or a header footprint to support early prototype debugging. The minimum connections are TCK, TMS, TDI, TDO, and TRSTn. JTAG routes and component footprints (except the PD on TRSTn and the PU on TMS and TCK) can be deleted in the production version of the board, if desired.

- **Have you provided the proper buffering for robust JTAG operation?**

  For more details, see the *Emulation and Trace Headers Technical Reference Manual* and the *XDS Target Connection Guide*
- **Are you connecting the TRC_x signals for trace operation?**

  If trace operation is needed, the TRC_x signals must be connected to the emulation connector. All TRC_x signals are pin-muxed with other signals. If the trace connections are needed, the connections for GPMC interface may not be used. Routes for TRC_x signals used for trace must be short and skew matched. Trace signals are on a separate power domain, VDDSHV3, and can be at a different voltage from the other JTAG signals. For more recommendations on TRC/EMU routing, see the *Emulation and Trace Headers Technical Reference Manual*. A similar summary of this information is available at *XDS Target Connection Guide*.
- **Do you require boundary scan on your design?**

  If boundary scan is required, the EMU0/1 pins must be directly connected to the JTAG connector

## 2.17 OLDI

**If OLDI is not used in the system**

The OLDI IO power rail VDDA_1P8_OLDI0 must remain powered by a valid 1.8V source when OLDI0 is not used. Refer to the *Recommended Operating Conditions* section of the *AM62x Sitara Processors Datasheet.*

The pins associated with the LVDS IOs can be left unconnected. Refer *Pin Connection Requirements* section in the *AM62x Sitara Processors Datasheet*

**If OLDI is used in the system**

*High-speed interface layout guidelines* should be followed for this interface due to higher data rates on serial data lanes.

This needs to be implemented as a point-to-point interface going from the AM62x SoC to a connector. No stubs should be present in the design

The differential impedance for the OLDI signal traces **must** be within the tolerance of 100 +/- 10 ohms. Source termination resistors are not required.

The board-level implementation should comply with the physical layer definition of *IEEE1596.3* standard and *ANSI/TIA/EIA644-A standard (Electrical Characteristics of Low Voltage Differential Signaling (LVDS) interface Circuits)*.

## 2.18 CSI

**If CSI is not used in the system**

Refer *Pin Connection Requirements* section in the *AM62x Sitara Processors Datasheet*

**If CSI is used in the system**

*High-speed interface layout guidelines* should be followed for this interface due to higher data rate.

VDDA_1P8_CSIRX0, VDDA_CORE_CSIRX0 must be connected to the appropriate power sources. CSI0_RXRCALIB needs to be connected via an appropriately chosen resistor to GND.

# 3 References

- *AM62x Sitara Processors Data Sheet*
- *AM62x DDR Board Design and Layout Guidelines*
- *AM62x Sitara Processors Technical Reference Manual*
- *High-Speed Interface Layout Guidelines*
- *Emulation and Trace Headers Technical Reference Manual*
- *XDS Target Connection Guide*
- *IEEE1596.3*
- *ANSI/TIA/EIA644-A standard (Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265