Application Report
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Hardware Design Guide for AM65x/DRA80xM Devices

ABSTRACT

This document describes hardware system design considerations for the AM65x/DRA80xM family of processors. This design guide is intended to be used as an aid during the development of application hardware. Other aids including, but not limited to, device data sheets, TRMs, and explicit collateral should also be used.

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Trademarks

1 Introduction

The Hardware Design Guide for AM65x/DRA80xM Devices Application Report provides a starting point for the engineer designing with one of the AM65x/DRA80xM processors. It shows a road map for the design effort and highlights areas of significant importance that must be addressed. This document does not contain all the information needed to complete the design. In many cases, it refers to the device-specific data manual or to various user guides as sources for specific information.

The guide is organized in a sequential manner. It moves from decisions that must be made in the initial planning stages of the design, through the selection of support components, to the mechanical, electrical, and thermal requirements. For the greatest success, each of the issues discussed in a section should be resolved before moving to the next section.

NOTE: This guide may not cover every aspect of your system design.

NOTE: The AM65x/DRA80xM device has capabilities to help system designers address safety requirements. This guide is focused on non-safety applications.

1.1 Before Getting Started

The AM65x/DRA80xM processors provide a wide variety of capabilities, not all of which will be used in every design. Consequently, the requirements for different designs using the same device can vary widely depending on how that part is used. You must understand your requirements before determining the details of the design. In addition, your design may require additional circuitry to operate correctly in the target environment. Review the data sheet for your device and determine the following:

- Which peripherals will be used to move data in and out of the processor
- What is the speed and organization of the DDR memory interface that will be used
- How much processing will each of the cores in your device be performing
- How you will boot the processor
- What are the expected environmental conditions for your device

1.2 Design Documentation

Throughout this guide, TI periodically recommends generating a design document based on your requirements. Generating and storing this information provides you with the foundation for your documentation package, and this design document will be needed if you are seeking support from TI. Examples of many of these can be found in the schematic package provided with the EVM boards for your device.

2 System Block Diagram

2.1 Creating the System Block Diagram

The first step in designing the hardware platform is to create a detailed block diagram. The block diagram should contain all major system ICs and illustrate which I/O ports are used for device interconnection.

The following is a collection of resources to aid in the block diagram creation process:

- The TMDX654GPEVM and TMDX654IDKEVM are a good source from which to start building a reference design for these devices.
- The links at the TI website below provide block diagrams, application notes, tools, software, design considerations, and other related information for various applications.
  - AM65x Product Folder
  - DRA8xM Product Folder

2.2 Selecting the Boot Mode

The block diagram should indicate which interface is used for booting this device.

The AM65x device contains multiple interfaces that support boot loading. Examples include: I2C, SPI, QSPI, OSPI, PCIe, NOR, Ethernet, USB, MMC/SD, and UART. The AM65x device supports a primary boot mode option and an optional backup boot mode option. If the primary boot source fails to boot, the ROM moves on to the backup mode.

The boot mode pins provide vital information to ROM code for boot. These pins are sampled at power-on-reset, and must be properly set up before reset rising. The BOOTMODE[06:00] pins are used to select the primary and backup interfaces used for booting. Additionally, each boot mode has different configuration options, controlled by the other boot mode pins (BOOTMODE[18:07] and MCU_BOOTMODE[09:00]).

Key boot considerations:

- TI recommends including population options for other boot modes to aid in development, such as UART boot of NOBOOT mode for JTAG debug.
- Boot pins have other functions after reset. Ensure your board design takes this into account when choosing pullup/pulldown resistors for the boot pins. If these pins are driven by another device, they must return to the proper boot configuration levels whenever the device is reset to enable it to boot properly each time. This is indicated by the PORz_OUT pin.
- The functionality of some boot mode pins are reserved, but these pins must be pulled a certain way. For details regarding reserved boot mode pins, see the *Boot Mode Pins* section of the *Initialization* chapter of the device TRM. For details regarding pull requirements for these pins, see the *Signal Descriptions* section of the *Terminal Configuration and Functions* chapter of the device data sheet.

For details regarding boot modes, see the *Initialization* chapter of the device TRM.

2.3 Confirming Pin Multiplexing Compatibility

The processor contains many peripheral interfaces. To reduce package costs while maintaining maximum functionality, many of the device terminals can multiplex up to eight signal functions. Thus, not all peripheral interface instances can be used simultaneously.

Texas Instruments has developed a Pin Mux Tool that helps a system designer select the appropriate pin-multiplexing configuration for their AM65x/DRA80xM based product design.

NOTE: The Pin Mux Tool's pin mux configuration for your design should be saved with your design documentation.

2.4 Selecting Peripherals Across Functional Domains

The processor is partitioned into three functional domains, each containing specific processing cores and peripherals:

- Wake-up (WKUP) domain
- Microcontroller (MCU) domain
- MAIN domain

For most use cases, peripherals from any domain can be used. All peripherals, regardless of their domain, are memory mapped, and the Arm® Cortex®-A53 cores can see and access all peripherals in the MCU and WKUP domains.

3 Power Supplies

After constructing a block diagram, the next requirement for a successful design is to determine the power needs for your processor.

3.1 Determining Your Power Requirements

The maximum and minimum current requirements for each of these voltage rails are not found in the device data sheet. These requirements are highly application-dependent and must be calculated for your specific product. For information on the device power consumption, see the Power Estimation SpreadSheet provided in the product folder for each AM65x/DRA80xM device.

3.2 Power Rails

For the full list of processor power rails and associated voltage range, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device data sheet. The following sections provide additional details about select power rails.

3.2.1 Internal LDOs

The processor includes seventeen internal LDOs, with the output of each connected to a pin (named "CAP_VDD*") on the device. The LDOs require an output capacitor connected to each of these pins. For guidance on the capacitor selection and connection, see the *Power Supply* section in the *Signal Descriptions* chapter of the device data sheet.

3.2.2 Dual-Voltage LVCMOS I/Os

VDDSHV[0:8] and VDDSHV[0:2]_WKUP are the dual-voltage LVCMOS I/O supplies, and can be configured as 1.8 V or 3.3 V. Each of these supplies has a corresponding I/O bias supply (VDDS[0:8] and VDDS[0:2]_WKUP). If any of the VDDSHV[0:8] or VDDSHV[0:2]_WKUP are configured for 3.3-V operation, the corresponding VDDS[0:8] or VDDSHV[0:2]_WKUP should be sourced from the internal I/O Bias LDO (CAP_VDDA_1P8_IOLDO[0:1] and CAP_VDDA_1P8_IOLDO_WKUP). When any of the VDDSHV[0:8] or VDDSHV[0:2]_WKUP are configured for 1.8-V operation, both VDDS[0:8] and VDDSHV[0:8] or VDDS[0:2]_WKUP and VDDSHV[0:2]_WKUP should be supplied from the same source.

For more information, see the *External Capacitors* section in the *Applications, Implementation, and Layout* chapter of the device data sheet.

3.2.3 Dual-Voltage Switching SDIO I/Os

The processor includes one integrated 1.8-V SDIO LDO to support SD card I/O voltage switching from card initialization to high-speed data modes. Only one MMCSD port (selectable through the MCU_BOOTMODE09 pin) can be connected to the SDIO LDO in a given system.

For information about how to connect and configure the SDIO LDO, see:

- The *External Capacitors* section in the *Applications, Implementation, and Layout* chapter of the device data sheet.
- The *Power Supply* section in the *Signal Descriptions* chapter of the device data sheet.

3.3 Power Supply Filters

The processor contains multiple analog power pins that provide power to sensitive analog circuitry such as PLLs, DLLs, and SERDES buffers and terminations. These must be attached to filtered power sources.

3.4 Power Supply Decoupling and Bulk Capacitors

To properly decouple the supply planes from system noise, decoupling and bulk capacitors are required. For general information about decoupling capacitors, see the device data sheet.

For guidance for optimizing the selection and placement of the decoupling and bulk capacitors, see the *Sitara Processor Power Distribution Networks: Implementation and Analysis*.

3.5 Power Supply Sequencing

A detailed representation of the power supply sequencing for the processor can be found in the device-specific datasheet. This power sequencing can be achieved using discrete components.

4 Clocking

The next requirement for your design is proper clocking, and providing appropriate clocks to all ICs in the system. These clocks can be created by pairing crystals with internal oscillators within the system ICs, or they can be created by a separate clock generator. This section describes the clocks found in the processor and the requirements for these clocks.

4.1 System Clock Inputs

The processor input clocks and recommended oscillator connections are summarized in the *Clock Specifications* section in the *Specifications* chapter of the device data sheet. WKUP_OSC0 is a required clock for proper operation of the device. OSC1 and WKUP_LFOSC are optional, depending on your system requirements.

4.2 Unused Clock Inputs

For guidance on the recommended connections for unused clock inputs, see the *Connections for Unused Pins* section in the *Terminal Configuration and Functions* chapter of the device data sheet.

4.3 Single-ended Clock Sources

The WKUP_OSC0 and OSC1 internal oscillators can be sourced from a crystal or an LVCMOS square-wave digital clock source. The WKUP_LFOSC0 internal oscillator can only be sourced from a crystal. For more details, see the *Input Clocks / Oscillators* section in the *Specifications* chapter of the device data sheet.

5 JTAG

The JTAG interface on the processor is used to communicate with test and emulation systems. Although JTAG is not required for operation, TI strongly recommends that a JTAG connection be included in all designs.

5.1 JTAG / Emulation

Relevant documentation for the JTAG/Emulation:

- *Emulation and Trace Headers Technical Reference Manual*
- *Boundary Scan Test Specification (IEEE-1149.1)*
- *AC Coupled Net Test Specification (IEEE-1149.6)*

5.1.1 Configuration of JTAG / Emulation

The IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) interface can be used for boundary scan and emulation. The boundary scan implementation is compliant with both IEEE-1149.1 and 1149.6. Boundary scan can be used regardless of the device configuration.

As an emulation interface, the JTAG port can be used in various modes:

- Standard emulation: requires only five standard JTAG signals
- HS-RTDX emulation: requires five standard JTAG signals plus EMU0 and/or EMU1. EMU0 and/or EMU1 are bidirectional in this mode.
- Trace port: The trace port allows real-time dumping of certain internal data. The trace port uses the EMU pins to output the trace data.

Emulation can be used regardless of the device configuration.

For supported JTAG clocking rates (TCLK), see the device-specific data manual.

5.1.2 System Implementation of JTAG / Emulation

The JTAG/Emulation pins on this processor are split across different power domains. The TDI, TDO, and TMS I/Os are powered by the VDDSHV0 domain. The TCK, TRSTz, EMU0, and EMU1 I/Os are powered by the VDDSHV0_WKUP domain. For proper operation of most emulators, these signals must be operating at the same voltage level. If this is a requirement for your emulator, ensure that the power domains associated with any JTAG/Emulation pins used by your system (such as VDDSHV0 and VDDSHV0_WKUP) are all configured for either 1.8 V or 3.3 V.

For most other system-level implementation details, see the *Emulation and Trace Headers Technical Reference Manual*.

5.1.3 Unused Emulation Pin Requirement

See the *Connections for Unused Pins* section in the *Terminal Configuration and Functions* chapter of the device data sheet.

6 Device Configurations and Initialization

When the voltage rails and the required clocks are present, the processor may be released from reset and initialized.

6.1 Device Reset

The processor can be reset in several ways. The methods are defined and described in greater detail in the device data sheet and TRM.

The device incorporates four external reset pins (MCU_PORz, MCU_RESETz, PORz, and RESETz) and four reset status pins (MCU_PORz_OUT, MCU_RESETSTATz, PORz_OUT, and RESETSTATz). Additional reset modes are available through internal registers and emulation.

The device integrates an on-chip Power-on-Reset (POR) generator. Additionally, this device supports an external POR generation through a PORz and MCU_PORz input pin. The MCU_BYPASS_POR pin selects the POR source. When the MCU_BYPASS_POR pin is set high at power-up, on-chip POR generation will be completely bypassed and the external POR used. When it is low, the POR is generated internally. However, the four external reset inputs must all be pulled high to enable this internal POR generation.

6.2 Boot Modes

For more details about the processor boot mode options, see Section 2.2.

Boot modes and certain device configuration selections are latched at the rising edge of MCU_PORz and PORz using specific pins. The configuration and boot mode inputs are multiplexed with general-purpose I/O (GPIO) pins or other pins. When the level on these pins is latched into the configuration registers, these pins are released to be used for their primary function. If internal POR is being used, the PORZ_OUT pin must be monitored to know when this latching occurs.

6.3 Device Configuration

The processor boot mode pins include several device configuration options, including system clock frequency and SDIO LDO configuration. For more details, see the *Boot Mode Pins* section of the *Initialization* chapter of the device TRM.

7 Peripherals

This section covers the device peripherals and modules, and is intended to be used in addition to the information provided in the device data sheet, TRM, and relevant application reports. The four types of documents should be used as follows:

- Data Sheet: AC Timings, Used pin guidance
- TRM: Functional Description, Programming Guide, Register offsets
- Application Reports: System-level issues
- This Chapter: System-level issues not covered in a separate application report

8 I/O Buffers and Termination

A key step in the hardware design, before beginning schematic capture, is to confirm both DC and AC electrical compatibility between this device and the other ICs connected to it.

- The device data sheet has important information with regards to timing and electrical characteristics.
- For high-speed interfaces, run IBIS simulations using IBIS models provided for the processor to confirm signal integrity.
  - Package IBIS

9 Power Consumption and Thermal Solutions

9.1 Power Consumption

For information on the device power consumption, see the Power Estimation SpreadSheet provided in AM654x, AM652x Power Consumption Model or DRA80x Power Consumption Model.

9.2 Power Savings Modes

The device supports multiple power modes. For more details, see the *Device Power States* section in the *Device Configuration* chapter of the device TRM.

9.3 Thermal Solution Guidance

The *Thermal Design Guide for DSP and Arm Application Processors Application Report* provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application report.

10 Schematic Recommendations

At this point in the design, start capturing the schematics. See the below collection of information to aid you in creating the schematics.

10.1 Floorplanning the PCB

Before beginning schematic capture, TI recommends to floorplan the system PCB to determine the interconnect distances between the various system ICs.

10.2 Creating your Schematics

During and after schematic capture, check your design against the *AM65x/DRA08xM Schematic Checklist*.

Plan to have an internal schematic review to go through the schematic checklist and inspect other key areas of the schematic to look for inaccuracies, missing net connections, and so forth.

11 Layout and Routing Guidelines

After completing schematic capture and reviews, the next step is to laying out the PCB. See the below collection of information to aid in creating the layout.

11.1 Escape Routing Guidelines

The *AM654x/DRA80xM PDB Escape Routing Application Report* provides a sample PCB escape routing for the AM654x SoC.

11.2 High-Speed Differential Signal Routing Guidance

The *High-Speed Interface Layout Guidelines Application Report* provides guidance for successful routing of the high-speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length, and spacing limits. TI supports only designs that follow the board design guidelines contained in the application report.

11.3 DDR Board Design and Layout Guidelines

The goal of the *DDR3L, DDR4, and LPDDR4 Board Design and Layout Guidelines Application Report* is to make the DDR3L, DDR4, and LPDDR4 system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using DDR3L, DDR4, and LPDDR4 memories that follow the guidelines in this document.

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