AMC23C12 Fast Response, Reinforced Isolated Window Comparator With Adjustable Threshold and Latch Function

1 Features

- Wide high-side supply range: 3 V to 27 V
- Low-side supply range: 2.7 V to 5.5 V
- Adjustable threshold:
  - Window-comparator mode: ±20 mV to ±300 mV
  - Positive-comparator mode: 600 mV to 2.7 V
- Reference for threshold adjustment: 100 µA, ±2%
- Trip threshold error: ±1% (max) at 250 mV
- Open-drain output with optional latch mode
- Propagation delay: 280 ns (typ)
- High CMTI: 55 V/ns (min)
- Safety-related certifications:
  - 7000-V_{PK} reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 5000-V_{RMS} isolation for 1 minute per UL1577
- Fully specified over the extended industrial temperature range: –40°C to +125°C

2 Applications

- Overcurrent or overvoltage detection in:
  - Motor drives
  - Frequency inverters
  - Solar inverters
  - DC/DC converters

3 Description

The AMC23C12 is an isolated window comparator with a short response time. The open-drain output is separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5 kV_{RMS} according to VDE 0884-17 and UL1577, and supports a working voltage of up to 1 kV_{PK}.

The comparison window is centered around 0 V, meaning that the comparator trips if the absolute value of the input voltage exceeds the trip threshold value. The trip threshold is adjustable from 20 mV to 300 mV through a single external resistor and, therefore, the comparison window ranges from ±20 mV to ±300 mV. When the voltage on the REF pin is greater than 550 mV, the negative comparator is disabled and only the positive comparator is functional. The reference voltage in this mode can be as high as 2.7 V. This mode is particularly useful for monitoring voltage supplies.

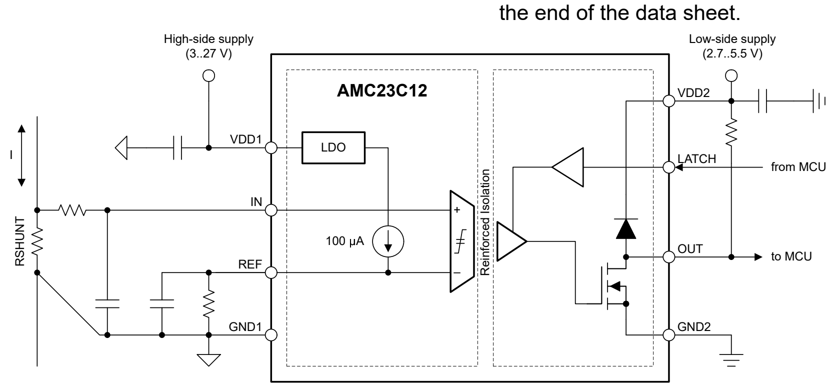
The open-drain output on the device supports transparent mode (LATCH input tied to GND2) where the output follows the input state, or latch mode, where the output is cleared on the falling edge of the latch input signal.

The AMC23C12 is available in a 8-pin, wide-body SOIC package and is specified over the extended industrial temperature range of –40°C to +125°C.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC23C12	SOIC (8)	5.85 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2022) to Revision A (July 2022) — **Page**

- Changed document status from *advance information* to *production data* ... 1

5 Pin Configuration and Functions

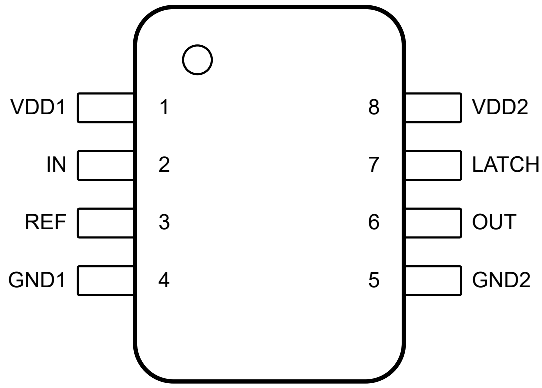


Figure 5-1. DWV Package, 8-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply.[(1)]
2	IN	Analog input	Analog input pin to the window comparator.
3	REF	Analog input	Reference pin that defines the trip threshold. The voltage on this pin also affects the hysteresis of comparator Cmp0, as explained in the *Reference Input* section. This pin is internally connected to a 100-μA current source. Connect a resistor from REF to GND1 to define the trip threshold, and a capacitor from REF to GND1 to filter the reference voltage. For best transient noise immunity, place the capacitor as closely to the pin as possible. This pin can also be driven by an external voltage source.
4	GND1	High-side ground	High-side ground.
5	GND2	Low-side ground	Low-side ground.
6	OUT	Digital output	Open-drain output of the window comparator. Connect to an external pullup resistor.
7	LATCH	Digital input	Digital input to select latch mode (high) or transparent mode (low) of the open-drain output. Do not leave the input pin unconnected (floating). Connect to GND2 when not used.
8	VDD2	Low-side power	Low-side power supply.[(1)]

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

see[(1)]

		MIN	MAX	UNIT
Power-supply voltage	VDD1 to GND1	–0.3	30	V
	VDD2 to GND2	–0.3	6.5	
Analog input voltage	REF to GND1	–0.5	6.5	V
	IN to GND1	–6	5.5	
Digital input voltage	LATCH to GND1	–0.5	VDD2 + 0.5	V
Digital output voltage	OUT to GND2	–0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
V_{VDD1}	High-side power-supply voltage	VDD1 to GND1	3.0	5	27	V
V_{VDD2}	Low-side power supply voltage	VDD2 to GND2	2.7	3.3	5.5	V
ANALOG INPUT						
V_{IN}	Input voltage	IN to GND1, VDD1 ≤ 4.3 V	–0.4		VDD1 – 0.3	V
		IN to GND1, VDD1 > 4.3 V	–0.4		4	
V_{REF}	Reference voltage, window comparator mode	REF to GND1	20		300	mV
	Reference voltage, positive-comparator mode	Low hysteresis mode	20		450	
		High hysteresis mode (Cmp0 only)	600		2700[(1)]	
	Reference voltage headroom	VDD1 – V_{REF}	1.4			V
	Filter capacitance on REF pin		20	100		nF
DIGITAL I/O						
	Digital input voltage	LATCH pin	GND2		VDD2	V
	Digital output voltage	OUT to GND2	GND2		VDD2	V
	Sink current	OUT	0		4	mA
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40	25	125	°C

(1) Reference voltages (V_{REF}) >1.6 V require V_{VDD1} > $V_{VDD1,MIN}$ to maintain minimum headroom (V_{VDD1} – V_{REF}) of 1.4 V.

6.4 Thermal Information

THERMAL METRIC[(1)]		DWV (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = 25 V, VDD2 = 5.5 V	102	mW
		VDD1 = VDD2 = 5.5 V	32	
		VDD1 = VDD2 = 3.6 V	21	
P_{D1}	Maximum power dissipation (high-side)	VDD1 = 25 V	90	mW
		VDD1 = 5.5 V	20	
		VDD1 = 3.6 V	13	
P_{D2}	Maximum power dissipation (low-side)	VDD2 = 5.5 V	12	mW
		VDD2 = 3.6 V	8	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance[(1)]	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage[(1)]	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-III	
		Rated mains voltage ≤ 1000 V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17)[(2)]				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	1060	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	750	V_{RMS}
		At DC voltage	1060	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification test)	7070	V_{PK}
		V_{TEST} = 1.2 × V_{IOTM}, t = 1 s (100% production test)	8500	
V_{IMP}	Maximum impulse voltage[(3)]	Tested in air, 1.2/50-µs waveform per IEC 62368-1	8300	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[(4)]	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge[(5)]	Method a, after input/output safety test subgroups 2 and 3, V_{ini} = V_{IOTM}, t_{ini} = 60 s, $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s, $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), V_{ini} = V_{IOTM}, t_{ini} = 1 s, $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output[(6)]	V_{IO} = 0.5 V_{PP} at 1 MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output[(6)]	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 5700 V_{RMS}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO} = 6840 V_{RMS}, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition
Reinforced insulation	Single protection
Certificate number: pending	File number: E181974

6.8 Safety Limiting Values

Safety limiting[(1)] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 102.8°C/W, VDD1 = VDD2 = 5.5 V, T_J = 150°C, T_A = 25°C			220	mA
		$R_{\theta JA}$ = 102.8°C/W, VDD1 = VDD2 = 3.6 V, T_J = 150°C, T_A = 25°C			340	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 102.8°C/W, T_J = 150°C, T_A = 25°C			1220	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times AVDD_{max} + I_S \times DVDD_{max}$, where $AVDD_{max}$ is the maximum high-side voltage and $DVDD_{max}$ is the maximum controller-side supply voltage.

6.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to 125°C, VDD1 = 3.0 V to 27 V, VDD2 = 2.7 V to 5.5 V, V_{REF} = 20 mV to 2.7 V(1), and V_{IN} = –400 mV to 4 V(3); typical specifications are at T_A = 25°C, VDD1 = 5 V, VDD2 = 3.3 V, and V_{REF} = 250 mV (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
R_{IN}	Input resistance	IN pin, 0 ≤ V_{IN} ≤ 4 V		1		GΩ
I_{BIAS}	Input bias current	IN pin, 0 ≤ V_{IN} ≤ 4 V(4)		0.1	25	nA
		IN pin, –400 mV ≤ V_{IN} ≤ 0 V(5)	–310	–0.5		
C_{IN}	Input capacitance	IN pin		4		pF
REFERENCE PIN						
I_{REF}	Reference current	REF to GND1, 20 mV < V_{REF} ≤ 2.7 V	99	100	101	µA
V_{MSEL}	Mode selection threshold(2)	V_{REF} rising	500	550	600	mV
		V_{REF} falling	450	500	550	
	Mode selection threshold hysteresis			50		mV
COMPARATORS						
V_{IT+}	Positive-going trip threshold	Cmp0		V_{REF} + V_{HYS}		mV
E_{IT+}	Positive-going trip threshold error	Cmp0, (V_{IT+} – V_{REF} – V_{HYS}), V_{REF} = 20 mV, V_{HYS} = 4 mV	–2		2	mV
		Cmp0, (V_{IT+} – V_{REF} – V_{HYS}), V_{REF} = 250 mV, V_{HYS} = 4 mV	–2		2	
		Cmp0, (V_{IT+} – V_{REF} – V_{HYS}), V_{REF} = 2 V, V_{HYS} = 25 mV	–5		5	
V_{IT-}	Negative-going trip threshold	Cmp0		V_{REF}		mV
E_{IT-}	Negative-going trip threshold error	Cmp0, (V_{IT-} – V_{REF}), V_{REF} = 20 mV	–2.5		2.5	mV
		Cmp0, (V_{IT-} – V_{REF}), V_{REF} = 250 mV	–2.5		2.5	
		Cmp0, (V_{IT-} – V_{REF}), V_{REF} = 2 V	–5		5	
V_{IT-}	Negative-going trip threshold	Cmp1		–V_{REF} – V_{HYS}		mV
E_{IT-}	Negative-going trip threshold error	Cmp1, (V_{IT-} + V_{REF} + V_{HYS}), V_{REF} = 20 mV, V_{HYS} = 4 mV	–3		3	mV
		Cmp1, (V_{IT-} + V_{REF} + V_{HYS}), V_{REF} = 250 mV, V_{HYS} = 4 mV	–3		3	
V_{IT+}	Positive-going trip threshold	Cmp1		–V_{REF}		mV
E_{IT+}	Positive-going trip threshold error	Cmp1, (V_{IT+} + V_{REF}), V_{REF} = 20 mV	–3.5		3.5	mV
		Cmp1, (V_{IT+} + V_{REF}), V_{REF} = 250 mV	–3.5		3.5	
V_{HYS}	Trip threshold hysteresis	Cmp0 and Cmp1, (V_{IT+} – V_{IT-}), V_{REF} ≤ 450 mV		4		mV
		Cmp0 only, (V_{IT+} – V_{IT-}), V_{REF} ≥ 600 mV		25		
DIGITAL I/O						
V_{IH}	High-level input voltage	LATCH pin	0.7 x VDD2		VDD2 + 0.3	V
V_{IL}	Low-level input voltage	LATCH pin	–0.3		0.3 x VDD2	V
C_{IN}	Input capacitance	LATCH pin		4		pF
V_{OL}	Low-level output voltage	I_{SINK} = 4 mA		80	250	mV
I_{LKG}	Open-drain output leakage current	VDD2 = 5 V, V_{OUT} = 5 V		5	100	nA
CMTI	Common-mode transient immunity	|V_{IN} – V_{REF}| ≥ 4 mV, R_{PULLUP} = 10 kΩ	55	110		V/ns

6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to 125°C, VDD1 = 3.0 V to 27 V, VDD2 = 2.7 V to 5.5 V, V_{REF} = 20 mV to 2.7 V(1), and V_{IN} = –400 mV to 4 V(3); typical specifications are at T_A = 25°C, VDD1 = 5 V, VDD2 = 3.3 V, and V_{REF} = 250 mV (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
$VDD1_{UV}$	VDD1 undervoltage detection threshold	VDD1 rising			3	V
		VDD1 falling			2.9	
$VDD1_{POR}$	VDD1 power-on reset threshold	VDD1 falling			2.3	V
$VDD2_{UV}$	VDD2 undervoltage detection threshold	VDD2 rising			2.7	V
		VDD2 falling			2.1	
I_{DD1}	High-side supply current			3.2	4.3	mA
I_{DD2}	Low-side supply current			1.8	2.2	mA

(1) Reference voltages >1.6 V require VDD1 > $VDD1_{MIN}$. See the *Recommended Operating Conditions* table for details.
(2) The voltage level V_{REF} determines if the device operates as window-comparator with positive and negative thresholds or as simple comparator with positive thresholds only. See the *Reference Input* section for more details.
(3) But not exceeding the maximum input voltage specified in the *Recommended Operating Conditions* table.
(4) The typical value is measured at V_{IN} = 0.4 V.
(5) The typical value is measured at V_{IN} = –400 mV.

6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LATCH INPUT						
	Deglitch time	Falling edge	1.8		3.2	µs
OPEN-DRAIN OUTPUT						
t_{pH}	Propagation delay time, $\|V_{IN}\|$ rising	VDD2 = 3.3 V, V_{REF} = 250 mV, $V_{OVERDRIVE}$ = 10 mV, C_L = 15 pF		280	410	ns
		VDD2 = 3.3 V, V_{REF} = 2 V, $V_{OVERDRIVE}$ = 50 mV, C_L = 15 pF		240	370	
t_{pL}	Propagation delay time, $\|V_{IN}\|$ falling	VDD2 = 3.3 V, V_{REF} = 250 mV, $V_{OVERDRIVE}$ = 10 mV, C_L = 15 pF		280	410	ns
		VDD2 = 3.3 V, V_{REF} = 2 V, $V_{OVERDRIVE}$ = 50 mV, C_L = 15 pF		240	370	
t_f	Output signal fall time	R_{PULLUP} = 4.7 kΩ, C_L = 15 pF		2		ns
MODE SELECTION						
t_{HSEL}	Comparator hysteresis selection deglitch time	Cmp0, V_{REF} rising or falling		10		µs
t_{DIS13}	Comparator disable deglitch time	Cmp1, V_{REF} rising		10		µs
t_{EN13}	Comparator enable deglitch time	Cmp1, V_{REF} falling		100		µs
START-UP TIMING						
$t_{LS,STA}$	Low-side start-up time	VDD2 step to 2.7 V, VDD1 ≥ 3.0 V		40		µs
$t_{HS,STA}$	High-side start-up time	VDD1 step to 3.0 V, VDD2 ≥ 2.7 V		45		µs
$t_{HS,BLK}$	High-side blanking time			200		µs
$t_{HS,FLT}$	High-side-fault detection delay time			100		µs

6.11 Timing Diagrams

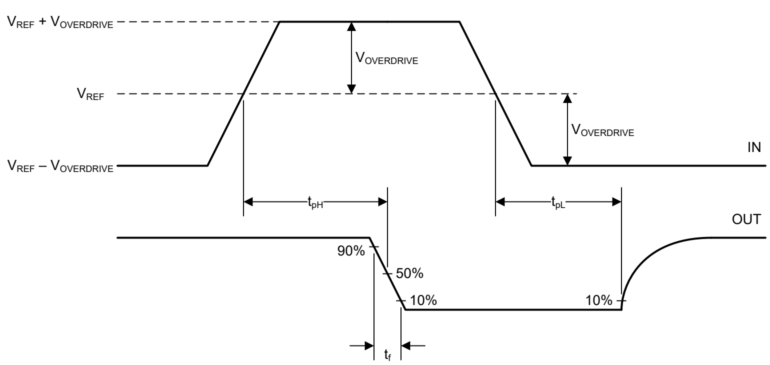


Figure 6-1. Rise, Fall, and Delay Time Definition (LATCH = Low)

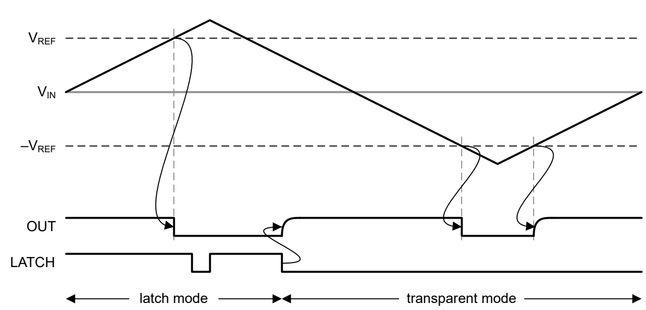


Figure 6-2. Functional Timing Diagram

6.12 Insulation Characteristics Curves

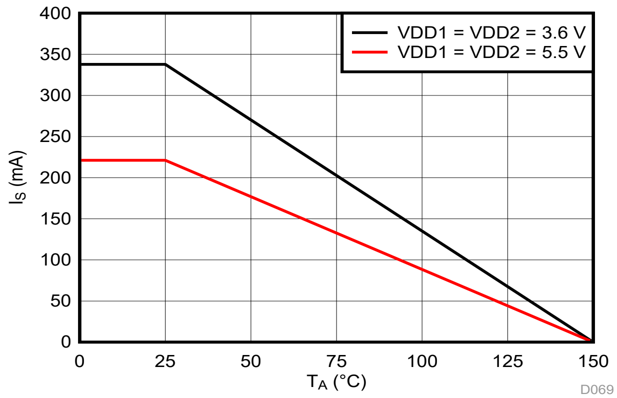


Figure 6-3. Thermal Derating Curve for Safety-Limiting Current per VDE

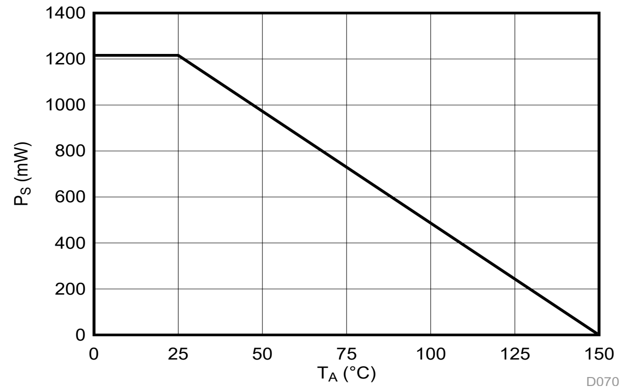
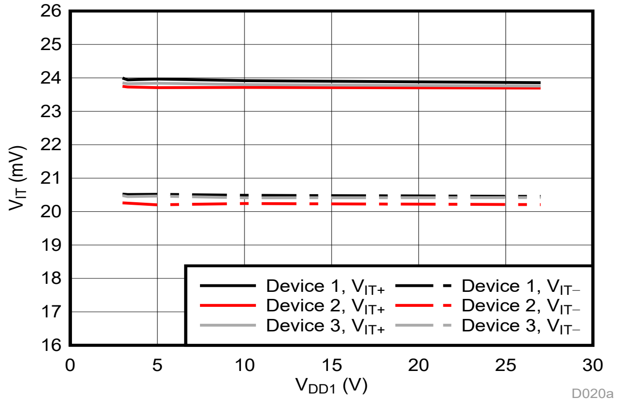


Figure 6-4. Thermal Derating Curve for Safety-Limiting Power per VDE

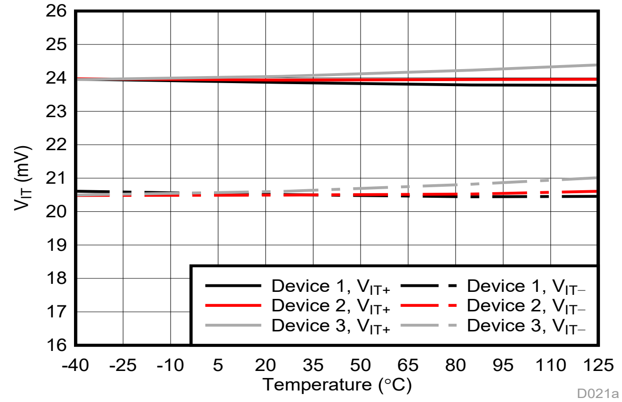
6.13 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V (unless otherwise noted)



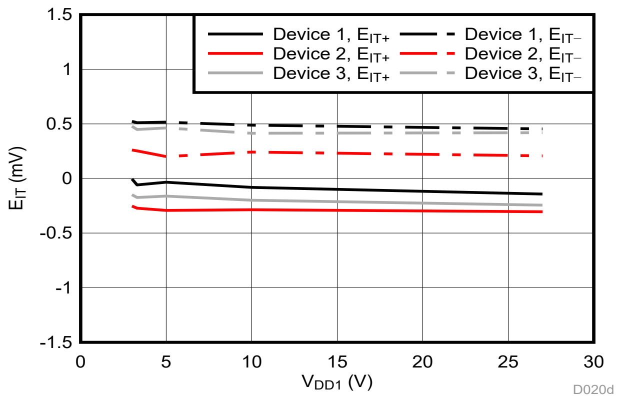
V_{REF} = 20 mV

Figure 6-5. Cmp0 Trip Threshold vs Supply Voltage



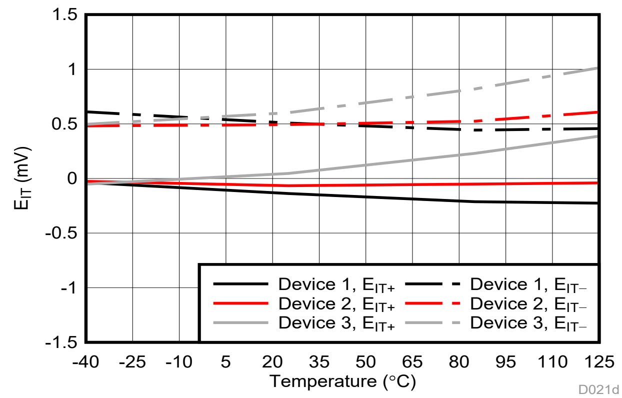
V_{REF} = 20 mV

Figure 6-6. Cmp0 Trip Threshold vs Temperature



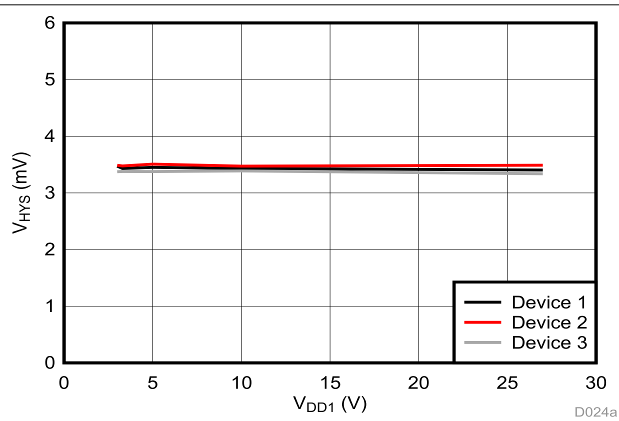
V_{REF} = 20 mV

Figure 6-7. Cmp0 Trip Threshold Error vs Supply Voltage



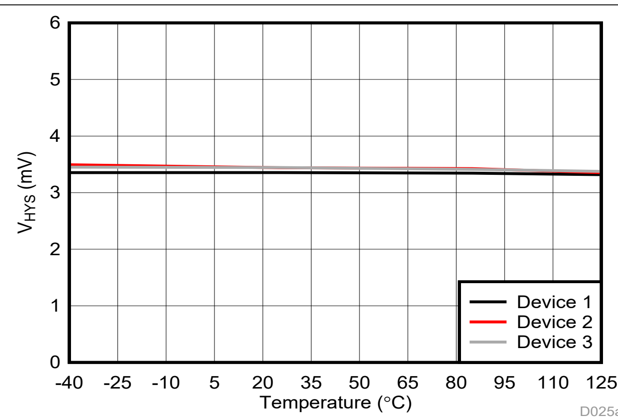
V_{REF} = 20 mV

Figure 6-8. Cmp0 Trip Threshold Error vs Temperature



V_{REF} = 20 mV

Figure 6-9. Cmp0 Trip Threshold Hysteresis vs Supply Voltage

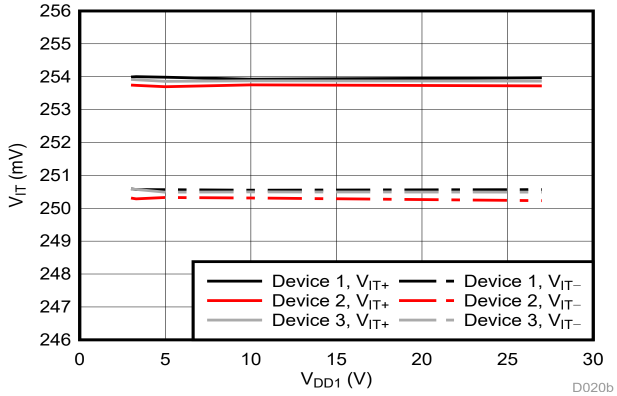


V_{REF} = 20 mV

Figure 6-10. Cmp0 Trip Threshold Hysteresis vs Temperature

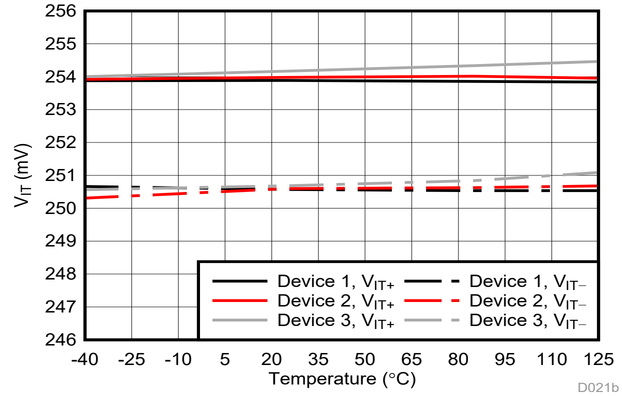
6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V (unless otherwise noted)



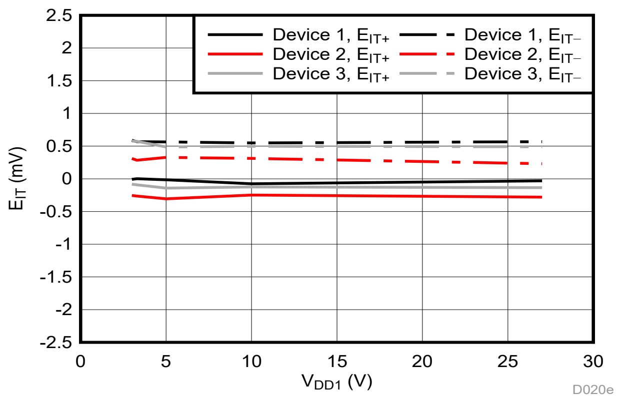
V_{REF} = 250 mV

Figure 6-11. Cmp0 Trip Threshold vs Supply Voltage



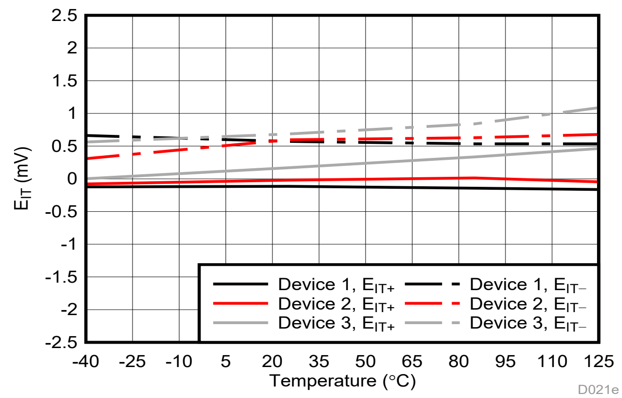
V_{REF} = 250 mV

Figure 6-12. Cmp0 Trip Threshold vs Temperature



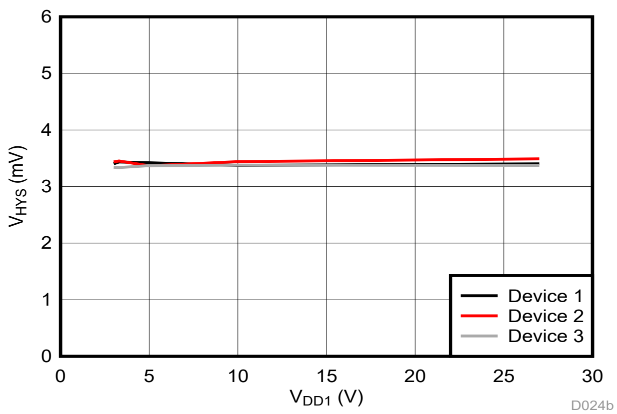
V_{REF} = 250 mV

Figure 6-13. Cmp0 Trip Threshold Error vs Supply Voltage



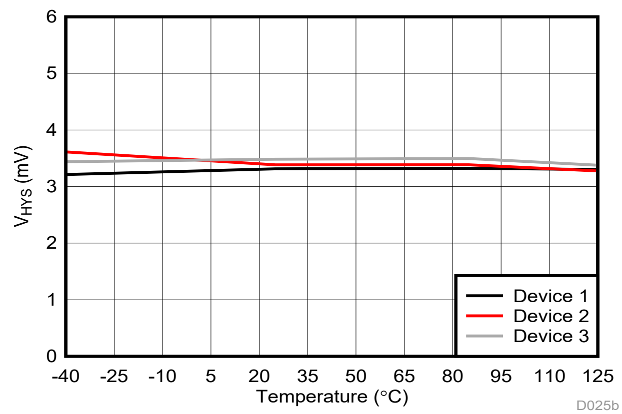
V_{REF} = 250 mV

Figure 6-14. Cmp0 Trip Threshold Error vs Temperature



V_{REF} = 250 mV

Figure 6-15. Cmp0 Trip Threshold Hysteresis vs Supply Voltage

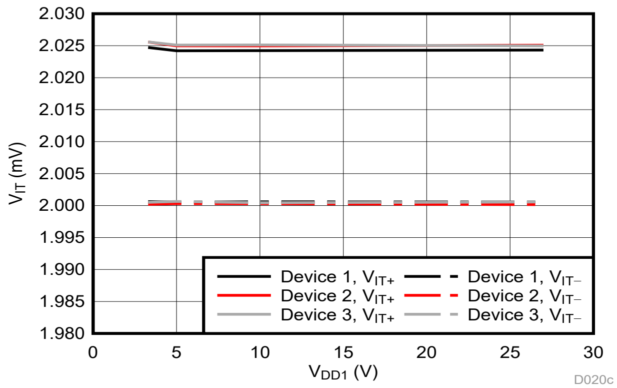


V_{REF} = 250 mV

Figure 6-16. Cmp0 Trip Threshold Hysteresis vs Temperature

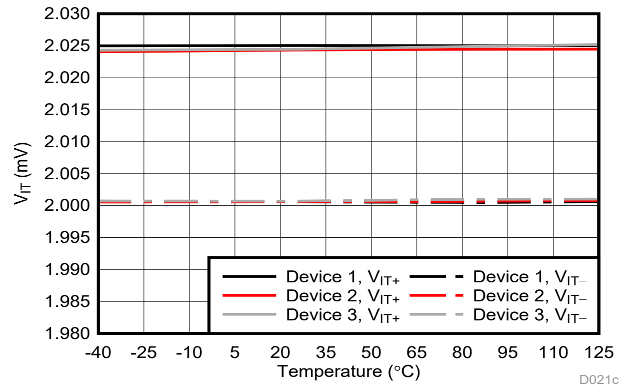
6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V (unless otherwise noted)



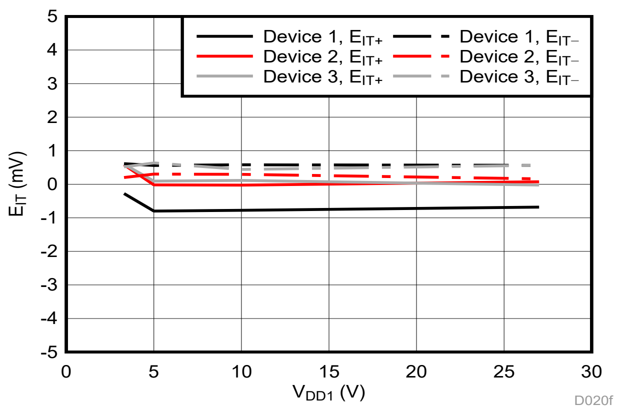
V_{REF} = 2 V

Figure 6-17. Cmp0 Trip Threshold vs Supply Voltage



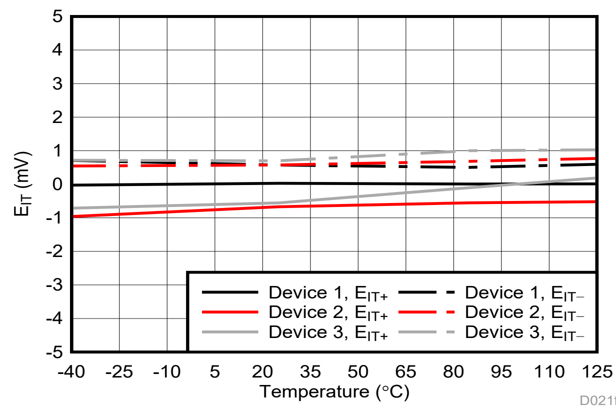
V_{REF} = 2 V

Figure 6-18. Cmp0 Trip Threshold vs Temperature



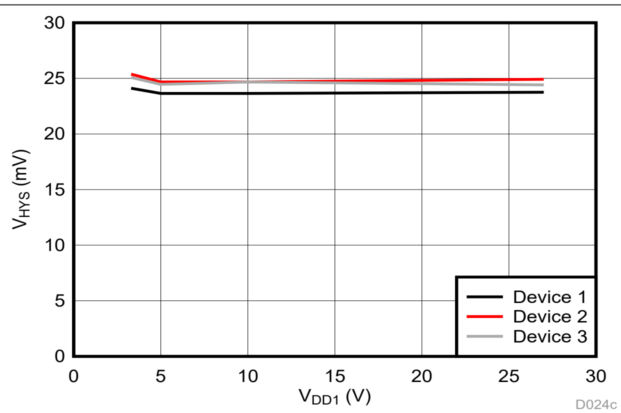
V_{REF} = 2 V

Figure 6-19. Cmp0 Trip Threshold Error vs Supply Voltage



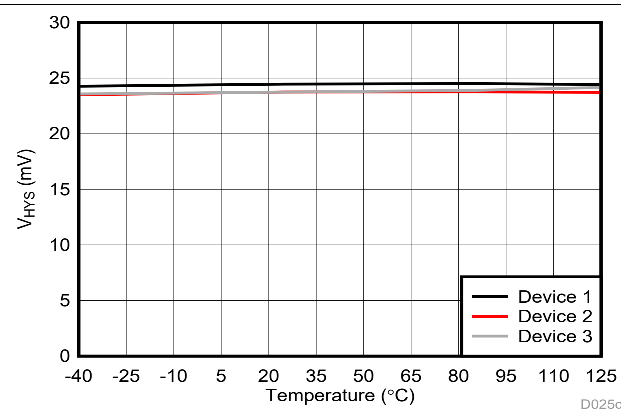
V_{REF} = 2 V

Figure 6-20. Cmp0 Trip Threshold Error vs Temperature



V_{REF} = 2 V

Figure 6-21. Cmp0 Trip Threshold Hysteresis vs Supply Voltage

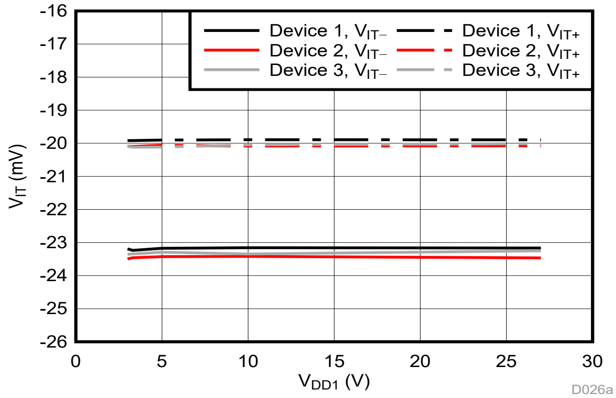


V_{REF} = 2 V

Figure 6-22. Cmp0 Trip Threshold Hysteresis vs Temperature

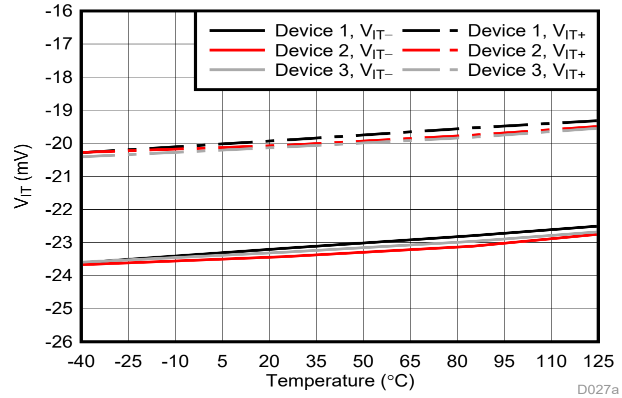
6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V (unless otherwise noted)



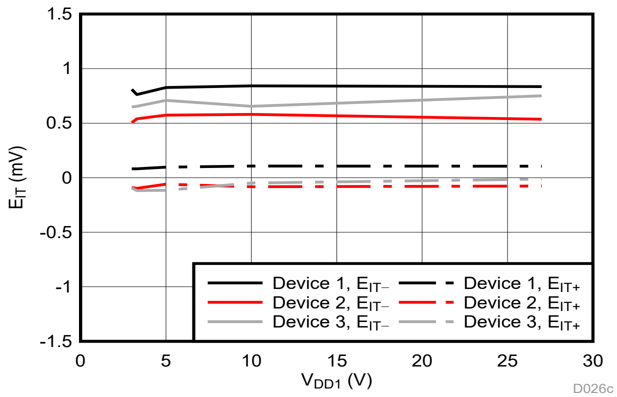
V_{REF} = 20 mV

Figure 6-23. Cmp1 Trip Threshold vs Supply Voltage



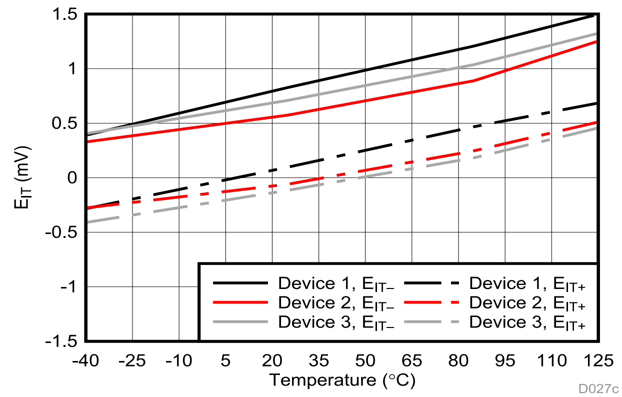
V_{REF} = 20 mV

Figure 6-24. Cmp1 Trip Threshold vs Temperature



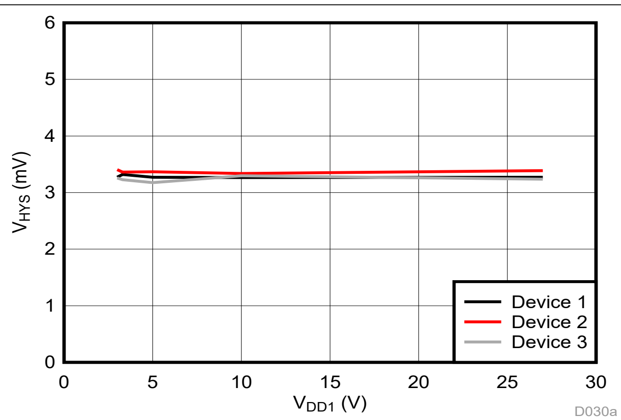
V_{REF} = 20 mV

Figure 6-25. Cmp1 Trip Threshold Error vs Supply Voltage



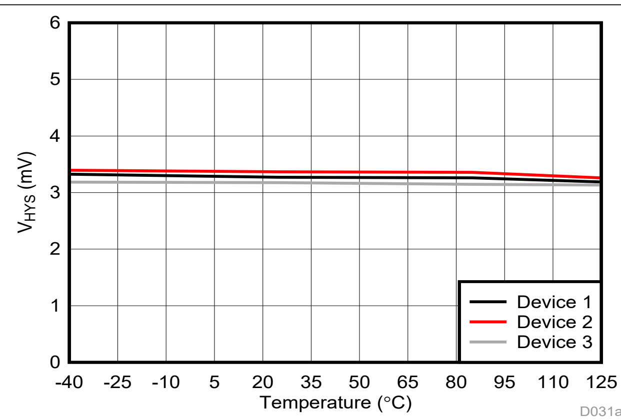
V_{REF} = 20 mV

Figure 6-26. Cmp1 Trip Threshold Error vs Temperature



V_{REF} = 20 mV

Figure 6-27. Cmp1 Trip Threshold Hysteresis vs Supply Voltage

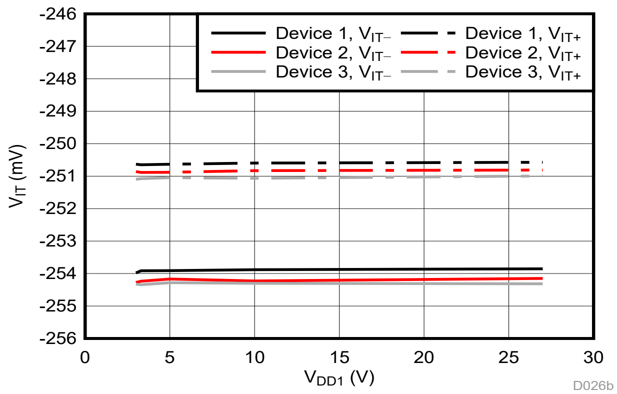


V_{REF} = 20 mV

Figure 6-28. Cmp1 Trip Threshold Hysteresis vs Temperature

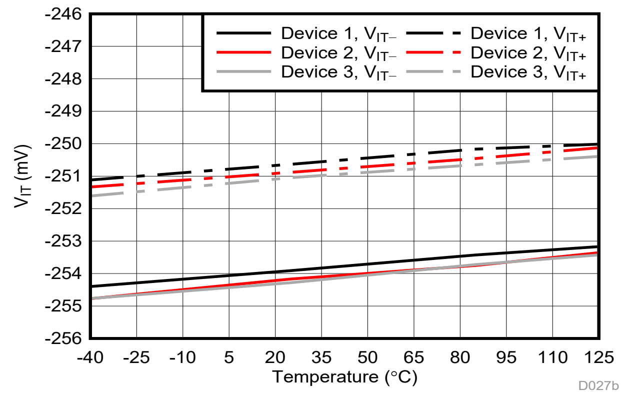
6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V (unless otherwise noted)



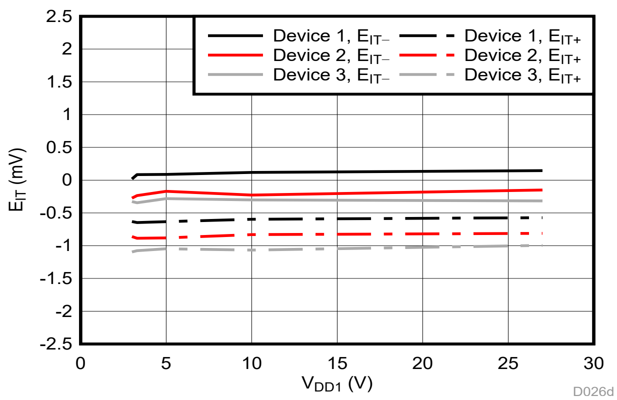
V_{REF} = 250 mV

Figure 6-29. Cmp1 Trip Threshold vs Supply Voltage



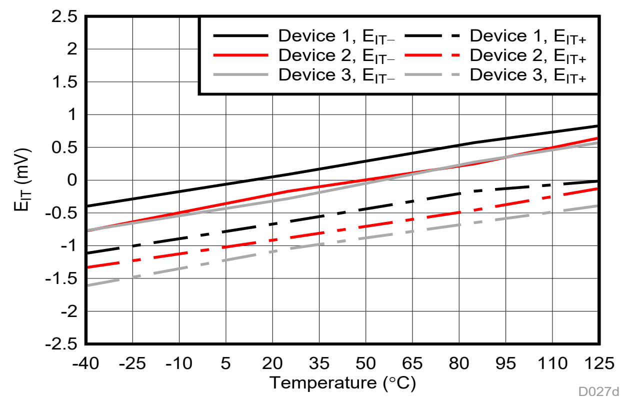
V_{REF} = 250 mV

Figure 6-30. Cmp1 Trip Threshold vs Temperature



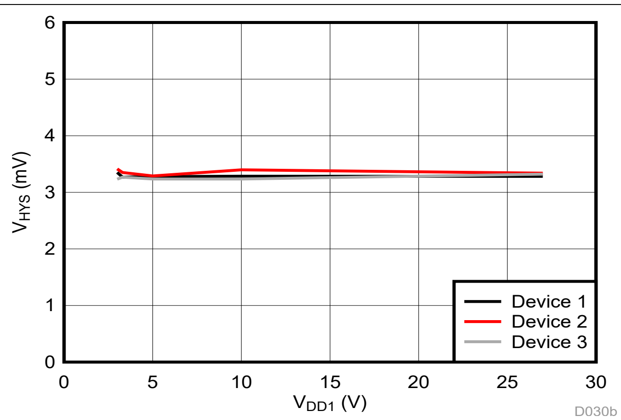
V_{REF} = 250 mV

Figure 6-31. Cmp1 Trip Threshold Error vs Supply Voltage



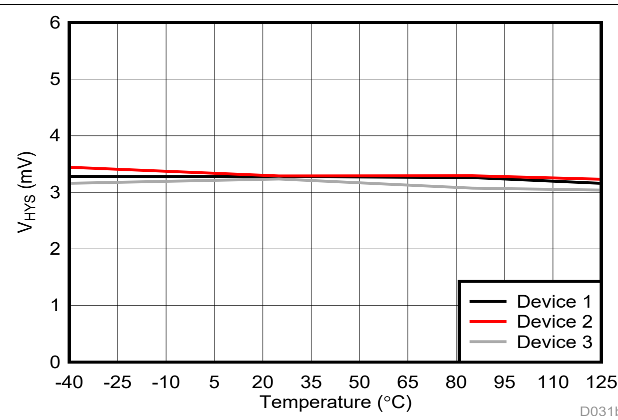
V_{REF} = 250 mV

Figure 6-32. Cmp1 Trip Threshold Error vs Temperature



V_{REF} = 250 mV

Figure 6-33. Cmp1 Trip Threshold Hysteresis vs Supply Voltage



V_{REF} = 250 mV

Figure 6-34. Cmp1 Trip Threshold Hysteresis vs Temperature

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V (unless otherwise noted)

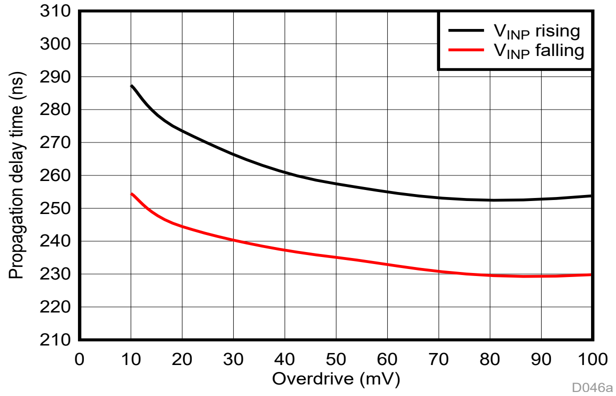


Figure 6-35. Cmp0 Propagation Delay vs Overdrive

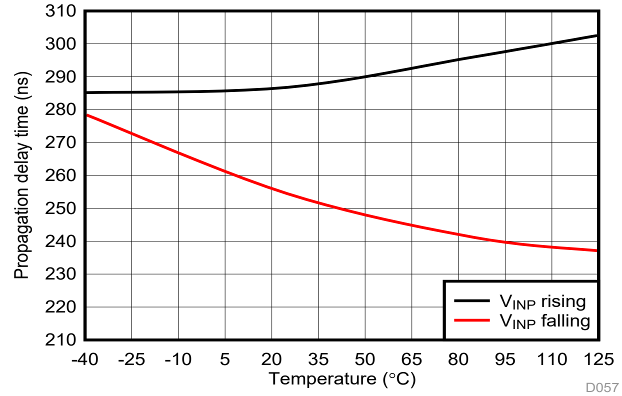


Figure 6-36. Cmp0 Propagation Delay vs Temperature

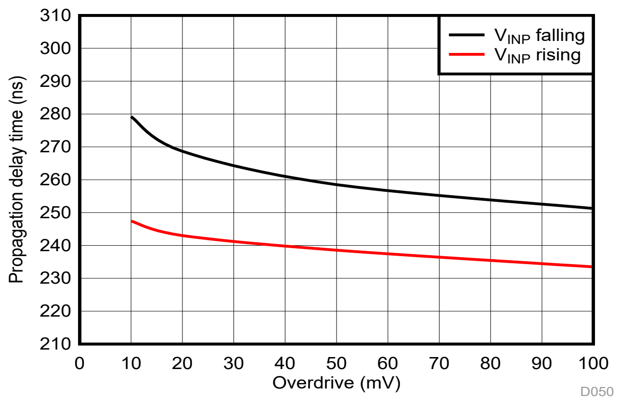


Figure 6-37. Cmp1 Propagation Delay vs Overdrive

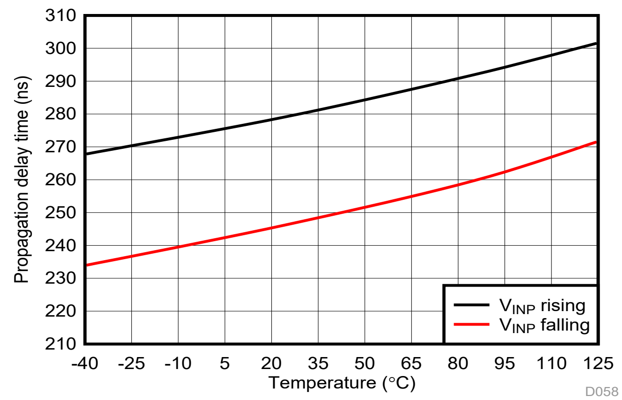


Figure 6-38. Cmp1 Propagation Delay vs Temperature

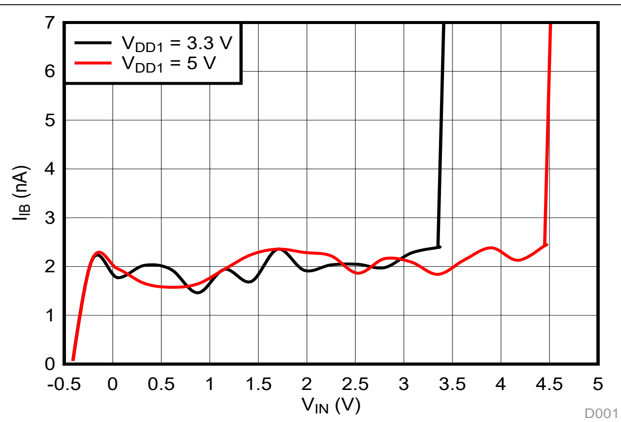
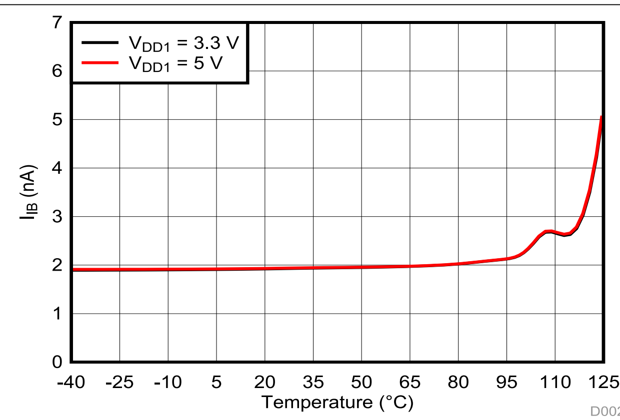


Figure 6-39. Input Bias Current vs Input Voltage



V_{IN} = 2 V

Figure 6-40. Input Bias Current vs Temperature

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V (unless otherwise noted)

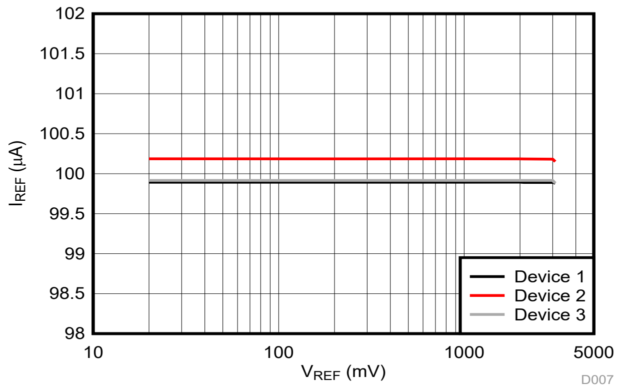


Figure 6-41. Reference Current vs Reference Voltage

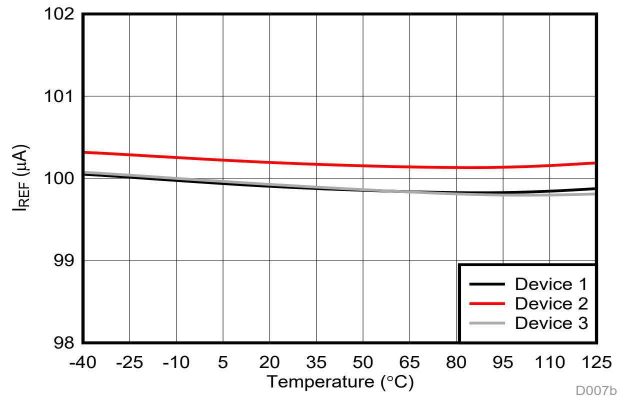


Figure 6-42. Reference Current vs Temperature

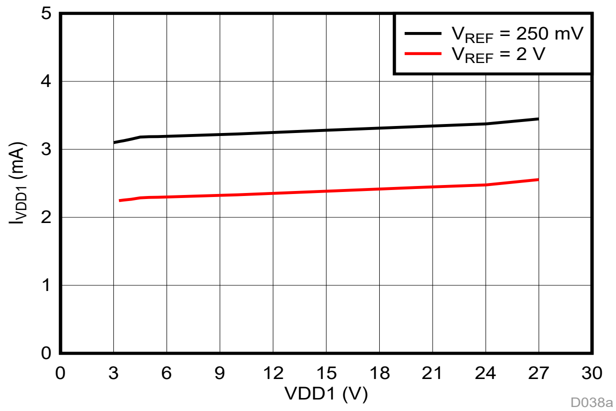


Figure 6-43. High-Side Supply Current vs Supply Voltage

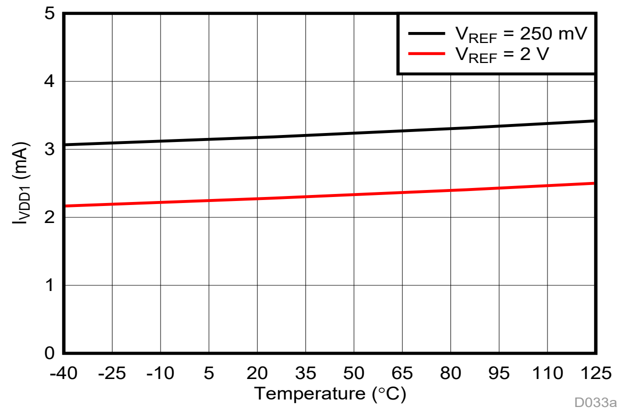


Figure 6-44. High-Side Supply Current vs Temperature

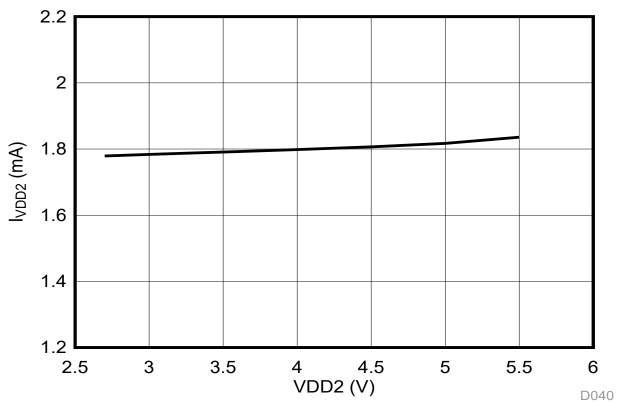


Figure 6-45. Low-Side Supply Current vs Supply Voltage

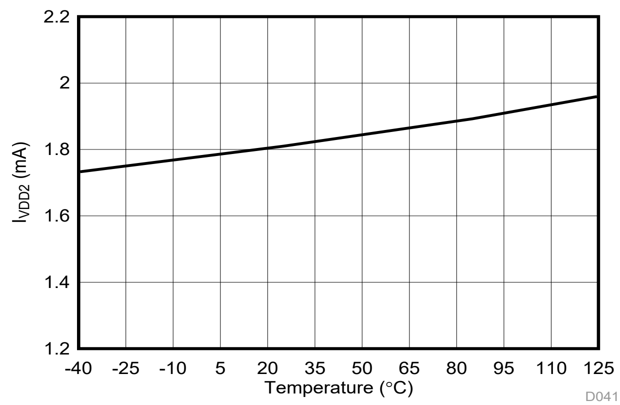


Figure 6-46. Low-Side Supply Current vs Temperature

7 Detailed Description

7.1 Overview

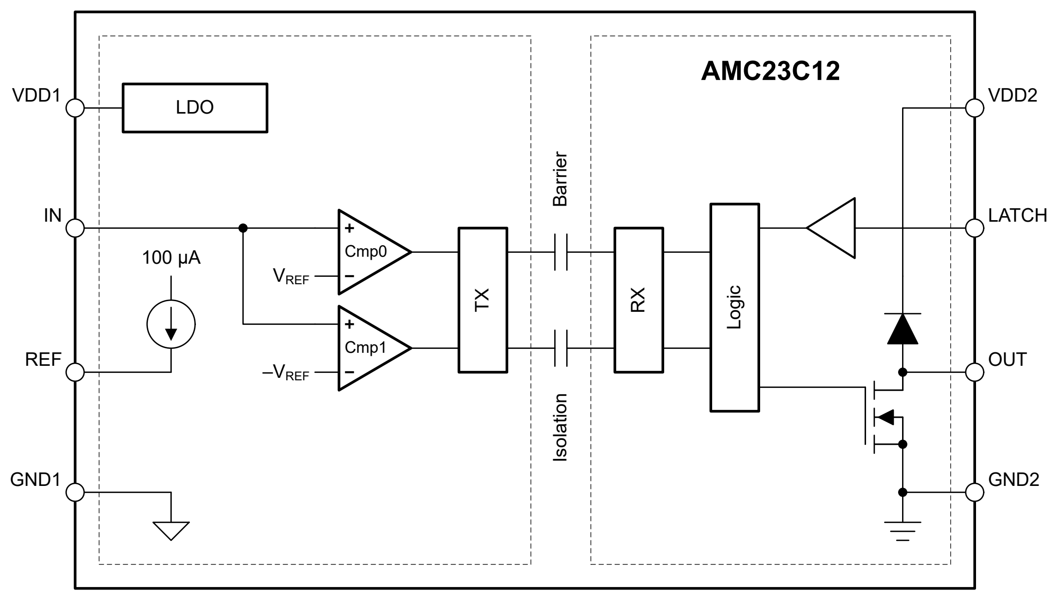
The AMC23C12 is an isolated window comparator with an open-drain output and optional latch function. The window comparator is comprised of comparator Cmp0 and Cmp1. Cmp0 compares the input voltage (V_{IN}) against the positive threshold (V_{IT+}) and Cmp1 compares the input voltage (V_{IN}) against the negative threshold ($V_{IT–}$). V_{IT+} and $V_{IT–}$ are of equal magnitude but opposite signs, therefore the comparison window is centered around 0 V. The comparison threshold is adjustable from ±20 mV to ±300 mV through an internally generated 100-µA reference current and a single external resistor.

The open-drain output is actively pulled low when the input voltage (V_{IN}) is outside the comparison window. The behavior when V_{IN} drops back inside the window is determined by the LATCH pin, as described in the *Open-Drain Digital Output* section.

When the voltage on the REF pin is greater than V_{MSEL}, the device operates in positive-comparator mode. This mode is particularly useful for monitoring positive voltages. The negative comparator (Cmp1) is disabled and only the positive comparator (Cmp0) is functional. The reference voltage in this mode can be as high as 2.7 V.

Galvanic isolation between the high- and low-voltage side of the device is achieved by transmitting the comparator states across a SiO_2-based, reinforced capacitive isolation barrier. This isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report. The digital modulation scheme used in the AMC23C12 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and common-mode transient immunity.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The positive comparator trips when the input voltage (V_{IN}) rises above the V_{IT+} threshold that is defined as the reference value plus the internal hysteresis voltage. The positive comparator releases when V_{IN} drops below the $V_{IT–}$ threshold that equals the reference value. The negative comparator trips when V_{IN} drops below its $V_{IT–}$ threshold that is defined as the negative reference value minus the internal hysteresis voltage. The negative comparator releases when V_{IN} rises above its V_{IT+} threshold that equals the negative reference value.

The difference between V_{IT+} and $V_{IT–}$ is referred to as the *comparator hysteresis* and is 4 mV for reference voltages below 450 mV. The integrated hysteresis makes the AMC23C12 less sensitive to input noise and provides stable operation in noisy environments without having to add external positive feedback to create hysteresis. The hysteresis of Cmp0 increases to 25 mV for reference values (V_{REF}) greater than 600 mV. See the *Reference Input* description for more details.

Figure 7-1 shows a timing diagram of the relationship between hysteresis and switching thresholds.

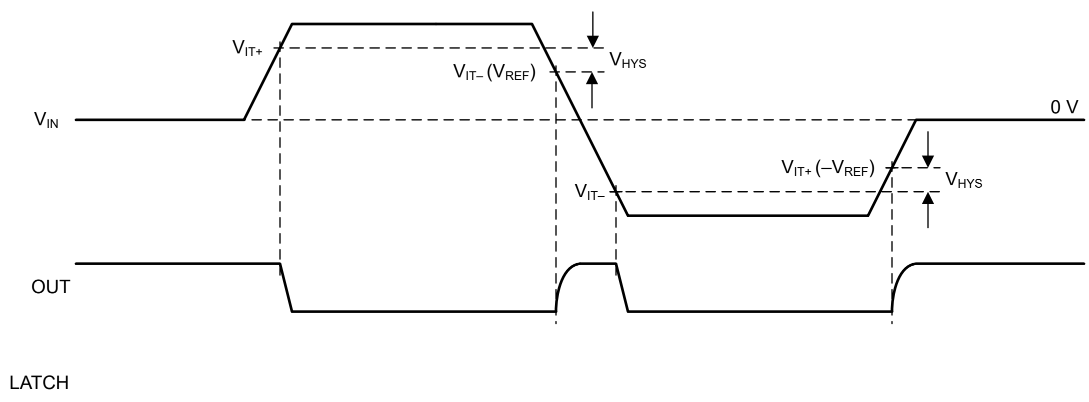


Figure 7-1. Switching Thresholds and Hysteresis

7.3.2 Reference Input

The voltage on the REF pin determines the trip threshold of the window comparator. The internal precision current source forces a 100-µA current through an external resistor connected from the REF pin to GND1. The resulting voltage across the resistor (V_{REF}) equals the magnitude of the positive and negative trip thresholds, see Figure 7-1. Place a 100-nF capacitor parallel to the resistor to filter the reference voltage. This capacitor must be charged by the 100-µA current source during power-up and the charging time may exceed the high-side blanking time ($t_{HS,BLK}$). In this case, as shown in Figure 7-2, the comparator may output an incorrect state after the high-side blanking time has expired until V_{REF} reaches its final value. See the *Power-Up and Power-Down Behavior* section for more details on power-up behavior.

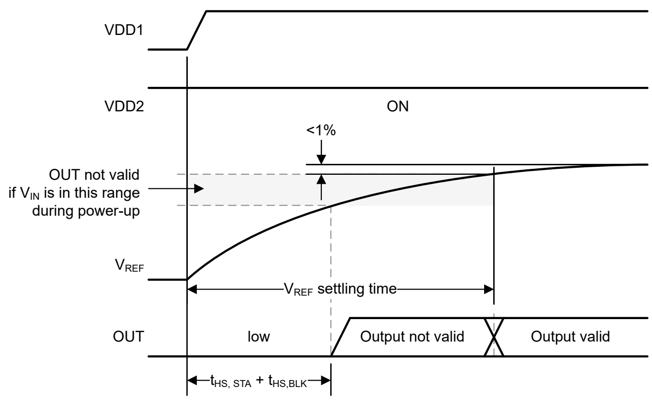


Figure 7-2. Output Behavior for Long Settling Times of the Reference Voltage

The voltage on the REF pin also determines the functionality of the negative comparator (Cmp1) and the hysteresis of the positive comparator (Cmp0) shown in the *Functional Block Diagram*. If V_{REF} exceeds the V_{MSEL} threshold defined in the *Electrical Characteristics* table, Cmp1 is disabled and the hysteresis of Cmp0 is increased from 4 mV (typical) to 25 mV. Positive-comparator mode is intended for voltage-monitoring applications that require higher input voltages and higher noise immunity.

The reference pin can be driven by an external voltage source to change the comparator thresholds during operation. However, do not drive V_{REF} dynamically across the V_{MSEL} threshold during normal operation because doing so changes the hysteresis of the Cmp0 comparator and can lead to unintentional switching of the output.

Figure 7-3 shows a mode selection timing diagram.

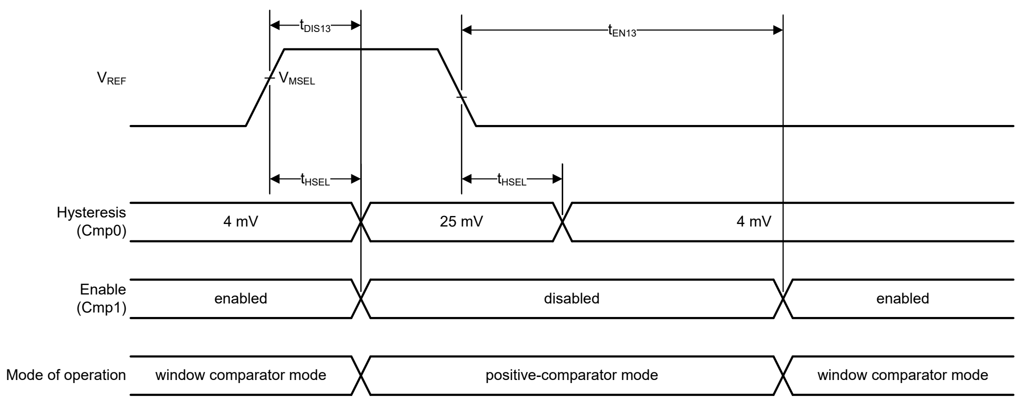


Figure 7-3. Mode Selection

7.3.3 Isolation Channel Signal Transmission

The AMC23C12 uses an on-off keying (OOK) modulation scheme, as shown in Figure 7-4, to transmit the comparator output states across the SiO_2-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the data for the logic that drives the open-drain output buffer. The AMC23C12 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

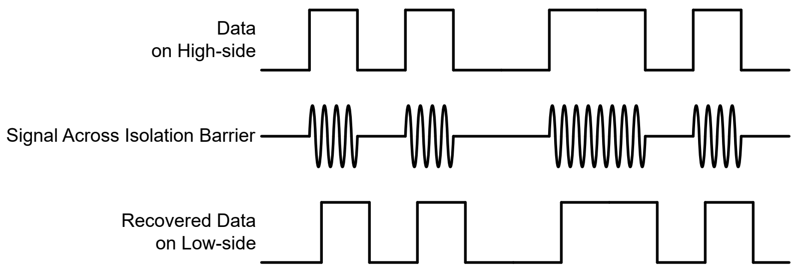


Figure 7-4. OOK-Based Modulation Scheme

7.3.4 Open-Drain Digital Output

The AMC23C12 provides an open-drain output with optional latching function. The output is actively pulled low when $|V_{IN}|$ exceeds the threshold value defined by the voltage on the REF pin, see Figure 7-1.

The open-drain output is diode-connected to the VDD2 supply (see the *Functional Block Diagram*), meaning that the output cannot be pulled more than 500 mV above the VDD2 supply before significant current begins to flow into the OUT pin. In particular, the open-drain output is clamped to one diode voltage above ground if VDD2 is at the GND2 level. This behavior is indicated by the gray shadings in Figure 7-5 through Figure 7-10.

On a system level, the CMTI performance of an open-drain signal line depends on the value of the pullup resistor. During a common-mode transient event with a high slew rate (high dV/dt), the open-drain signal line may be pulled low due to parasitic capacitive coupling between the high-side and the low-side of the printed circuit board (PCB). The effect of the parasitic coupling on the signal level is a function of the pullup strength and a lower value pullup resistor results in better CMTI performance. The AMC23C12 has been characterized with a relatively weak pullup resistor value of 10 kΩ to ensure that the specified CMTI performance is met in a typical application with a 4.7 kΩ or lower pullup resistor.

7.3.4.1 Transparent Output Mode

The device is set to transparent mode when the LATCH pin is pulled low, thus allowing the output state to change and follow the input signal with respect to the programmed trip threshold. For example, when the input signal rises above the trip threshold, the OUT pin is pulled low. When the input signal drops below the trip threshold, the output returns to the default high output state. A common implementation using the device in transparent mode is to connect the OUT pin to a hardware interrupt input on a controller. As soon as an out-of-range condition is detected by the device and the OUT pin is pulled low, the controller interrupt terminal detects the output state change and can begin making changes to the system operation needed to address the out-of-range condition.

7.3.4.2 Latch Output Mode

Some applications do not have the functionality available to continuously monitor the state of the OUT pin to detect an overcurrent condition. A typical example of this application is a system that is only able to poll the OUT terminal state periodically to determine if the system is functioning correctly. If the device is set to transparent mode in this type of application, a change in the state of the OUT pin can be missed if the out-of-range condition does not appear during one of these periodic polling events.

Latch mode is specifically intended to accommodate these applications. The device is placed in latch mode by setting the voltage on the LATCH terminal to a logic high level. The difference between latch mode and transparent mode is how the output responds when an out-of-range event ends. In transparent mode, when the input signal drops below the trip threshold, the output state returns to the default high setting to indicate that the out-of-range event has ended.

In latch mode, when an out-of-range condition is detected and the OUT pin is pulled low, the OUT pin does not return to the default high level when the input signal drops below the trip threshold level. To clear the event, the LATCH terminal must be pulled low for at least 4 µs. Pulling the LATCH pin low allows the OUT pin to return to the default high level, provided that the input signal has dropped below the trip threshold. If the input signal is still above the threshold when the LATCH pin is pulled low, the OUT terminal remains low. When the out-of-range event is detected by the system controller, the LATCH pin can be set back to high in order to place the device back into latch mode.

7.3.5 Power-Up and Power-Down Behavior

The open-drain output powers up in a high-impedance (Hi-Z) state when the low-side supply (VDD2) turns on. After power-up, if the high-side is not functional yet, the output is actively pulled low. This condition happens after the low-side start-up time plus the high-side fault detection delay time ($t_{LS,STA}$ + $t_{HS,FLT}$), as shown in Figure 7-5. Similarly, if the high-side supply drops below its undervoltage threshold ($VDD1_{UV}$) for more than the high-side fault detection delay time during normal operation, the open-drain output is pulled low, as shown in Figure 7-8. This delay allows the system to shut down reliably when the high-side supply is missing.

Communication starts between the high-side and low-side of the comparator is delayed by the high-side blanking time ($t_{HS,BLK}$, a time constant implemented on the high-voltage side) to allow the internal 300-mV reference and the voltage on the REF pin to settle, and to avoid unintentional switching of the comparator output during power-up.

Figure 7-5 through Figure 7-10 depict typical power-up and power-down scenarios.

In Figure 7-5, the low-side supply (VDD2) turns on but the high-side supply (VDD1) remains off. The output powers up in a Hi-Z state. After $t_{HS,\ FLT}$, OUT is pulled low indicating a no-power fault on the high-side.

In Figure 7-6, the high-side supply (VDD1) turns on long after the low-side supply (VDD2) turns on. The output is initially in an active-low state, see case (1). After the high-side supply is enabled, there is a duration of $t_{HS,\ STA}$ + $t_{HS,\ BLK}$ before the device assumes normal operation and the output reflects the current state of the comparator.

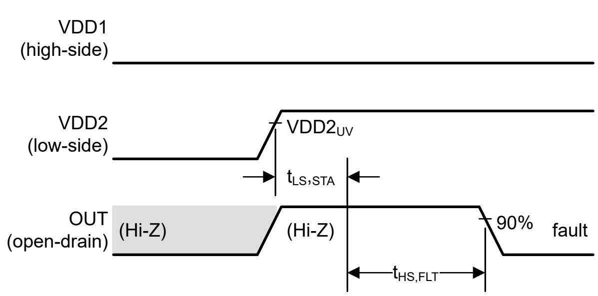


Figure 7-5. VDD2 Turns On, VDD1 Stays Off

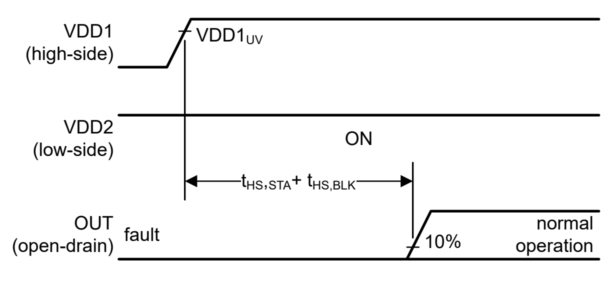


Figure 7-6. VDD2 is On; VDD1 Turns On (Long Delay)

In Figure 7-7, the low-side supply (VDD2) turns on, followed by the high-side supply (VDD1) with only a short delay. The output is initially in a Hi-Z state. The high-side fault detection delay ($t_{HS,FLT}$) is shorter than the high-side blanking time ($t_{HS,BLK}$), and therefore the output is pulled low after $t_{HS,FLT}$, indicating that the high-side is not operational yet. After the high-side blanking time ($t_{HS,BLK}$) elapses, the device assumes normal operation and the output reflects the current state of the comparator.

In Figure 7-8, the high-side supply (VDD1) turns off, followed by the low-side supply (VDD2). After the high-side fault detection delay time ($t_{HS,FLT}$), the output is actively pulled low. As soon as VDD2 drops below the $VDD2_{UV}$ threshold, the output enters a Hi-Z state.

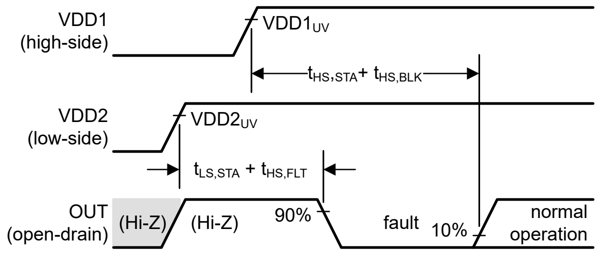


Figure 7-7. VDD2 Turns On, Followed by VDD1 (Short Delay)

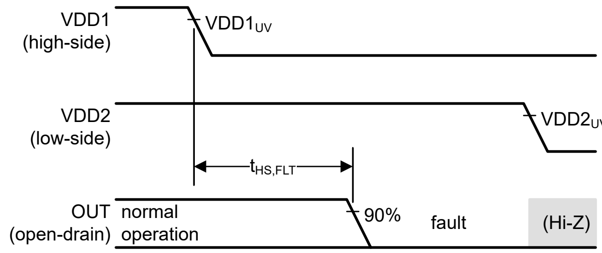


Figure 7-8. VDD1 Turns Off, Followed by VDD2

In Figure 7-9, the low-side supply (VDD2) turns on after the high-side is fully powered up (the delay between VDD1 and VDD2 is greater than ($t_{HS,STA}$ + $t_{HS,BLK}$)). The output starts in a Hi-Z state. After the low-side start-up time ($t_{LS,STA}$), the device enters normal operation.

In Figure 7-10, the low-side supply (VDD2) turns off, followed by the high-side supply (VDD1). As soon as VDD2 drops below the $VDD2_{UV}$ threshold, the output enters a Hi-Z state.

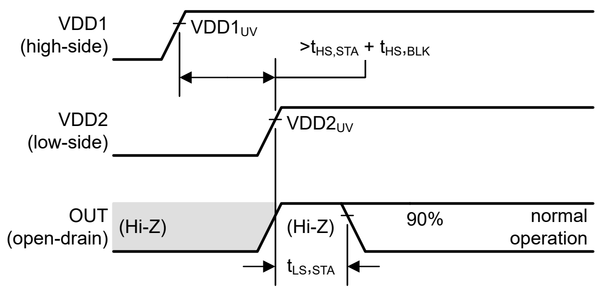


Figure 7-9. VDD1 Turns On, Followed by VDD2 (Long Delay)

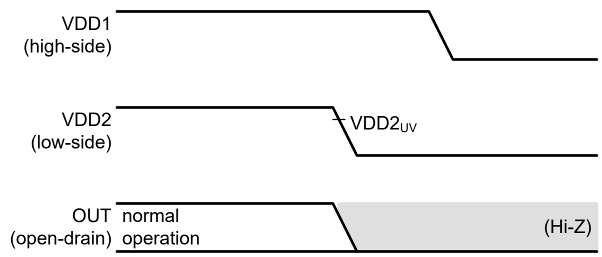


Figure 7-10. VDD2 Turns Off, Followed by VDD1

7.3.6 VDD1 Brownout and Power-Loss Behavior

Brownout is a condition where the VDD1 supply droops below the specified operating voltage range but the device remains functional. Power-loss is a condition where the VDD1 supply drops below a level where the device stops being functional. Depending on the duration and the voltage level, a brownout condition may or may not be noticeable at the output of the device. A power-loss condition is always signaled on the output of the isolated comparator.

Figure 7-11 through Figure 7-13 show typical brownout and power-loss scenarios.

In Figure 7-11, VDD1 droops below the undervoltage detection threshold ($VDD1_{UV}$) but recovers before the high-side-fault detection delay time ($t_{HS,FLT}$) expires. The brownout event has no effect on the comparator output.

In Figure 7-12, VDD1 droops below the undervoltage detection threshold ($VDD1_{UV}$) for more than the high-side-fault detection delay time ($t_{HS,FLT}$). The brownout condition is detected as a fault and the output is pulled low after a delay equal to $t_{HS,FLT}$. The device resumes normal operation as soon as VDD1 recovers above the $VDD1_{UV}$ threshold.

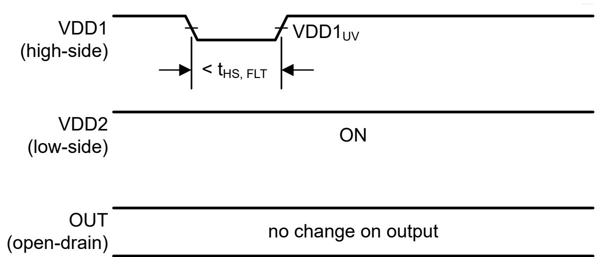


Figure 7-11. Output Response to a Short Brownout Event on VDD1

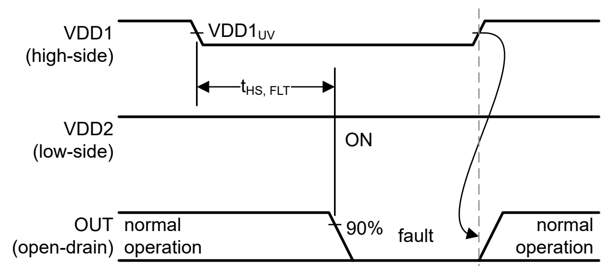


Figure 7-12. Output Response to a Long Brownout Event on VDD1

In Figure 7-13, VDD1 droops below the power-on-reset (POR) threshold ($VDD1_{POR}$). The power-loss condition is detected as a fault and the output is pulled low after a delay equal to $t_{HS,FLT}$. The device resumes normal operation after a delay equal to $t_{HS,STA}$ + $t_{HS,BLK}$ after VDD1 recovers above the $VDD1_{UV}$ threshold.

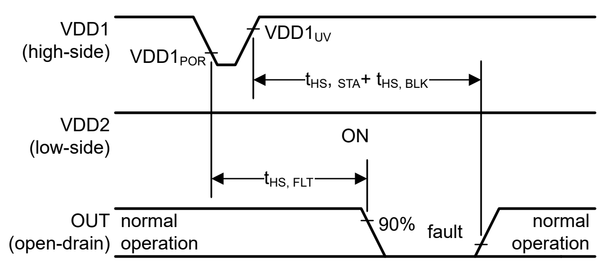


Figure 7-13. Output Response to a Power-Loss Event on VDD1

7.4 Device Functional Modes

The AMC23C12 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the *Recommended Operating Conditions* table.

Both comparators on the high-side function together as one window comparator when the voltage on the REF pin is below the V_{MSEL} threshold. If the voltage on the REF pin exceeds the V_{MSEL} threshold, the negative comparator (Cmp0) is disabled and Cmp1 functions as a single positive comparator with increased hysteresis, as described in the *Reference Input* section.

The device has two output operating modes that are selected based on the LATCH input pin setting: transparent mode and latch mode. These modes affect how the OUT pin responds to the changing input signal conditions. See the *Open-Drain Digital Output* section for details.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

With its low response time, high common-mode transient immunity (CMTI) and reinforced isolation barrier, the AMC23C12 is designed to provide fast and reliable overcurrent and overvoltage detection for high-voltage applications in harsh and noisy environments.

8.2 Typical Applications

8.2.1 Overcurrent Detection

Fast overcurrent detection is a common requirement in DC/DC converter and motor-control applications, and can be implemented with an AMC23C12 isolated window comparator as shown in Figure 8-1.

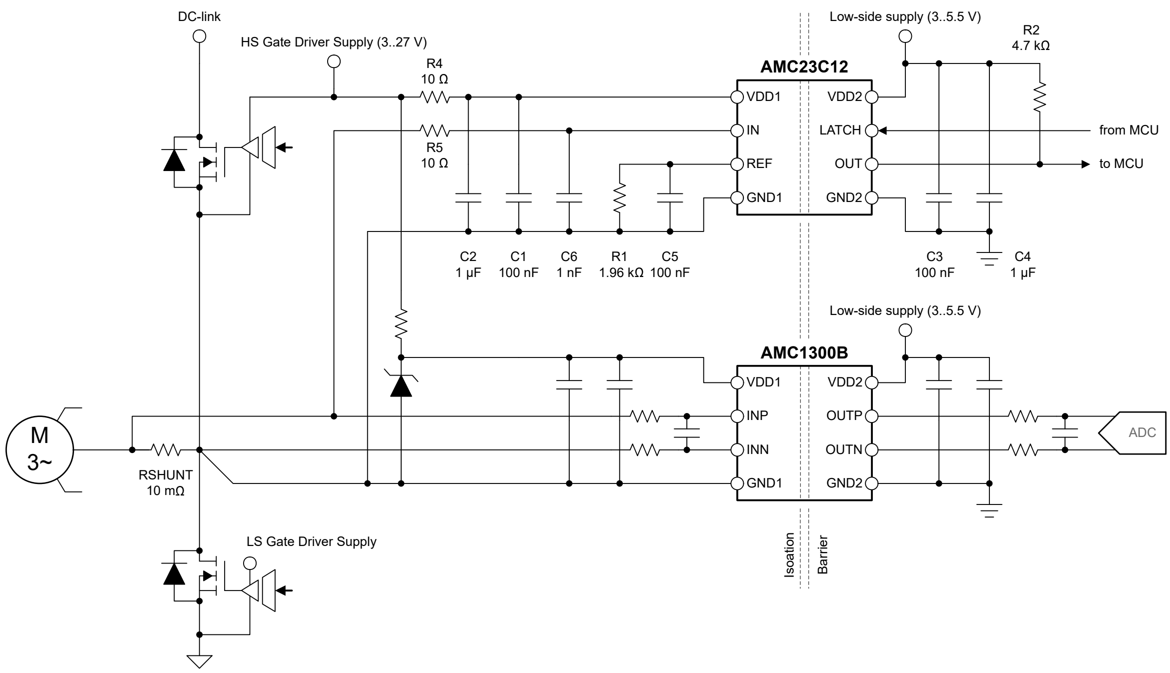


Figure 8-1. Using the AMC23C12 for Overcurrent Detection

The load current flowing through an external shunt resistor RSHUNT produces a voltage drop that is sensed by the AMC1300B for control purposes. The same voltage is monitored by the AMC23C12 that is connected in parallel to the current-sensing amplifier and provides a fast sensing path for positive and negative fault-current detection. The overcurrent detection threshold is set by the external resistor R1 and the overcurrent event is signaled on the open-drain output OUT.

As depicted in Figure 8-1, the integrated low-dropout (LDO) regulator on the high-side allows direct connection of the VDD1 input to a commonly used floating gate-driver supply. Alternatively, the AMC23C12 can share a regulated supply with the AMC1300B. In that case, the VDD1 pin of the AMC23C12 connects directly to the VDD1 pin of the AMC1300B and R4 is not needed. The fast response time and high common-mode transient immunity (CMTI) of the AMC23C12 ensure reliable and accurate operation even in high-noise environments.

8.2.1.1 Design Requirements

Table 8-1 lists the parameters for the application example in Figure 8-1.

Table 8-1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3 V to 27 V
Low-side supply voltage	2.7 V to 5.5 V
Shunt-resistor value	10 mΩ
Linear input voltage range of the AMC1300B	±250 mV
Maximum peak motor current	±25 A
Overcurrent detection threshold	±20 A

8.2.1.2 Detailed Design Procedure

The value of the shunt resistor in this example is 10 mΩ, determined by the linear input voltage range of the AMC1300B current-sensing amplifier (±250 mV) and the full-scale current of ±25 A.

At the desired 20-A overcurrent detection level, the voltage drop across the shunt resistor is 10 mΩ × 20 A = 200 mV. The positive-going trip threshold of the window comparator is V_{REF} + V_{HYS}, where V_{HYS} is 4 mV as specified in the *Electrical Characteristics* table and V_{REF} is the voltage across R1 that is connected between the REF and GND1 pins. R1 is calculated as (V_{TRIP} – V_{HYS}) / I_{REF} = (200 mV – 4 mV) / 100 µA = 1.96 kΩ and matches a value from the E96 series (1% accuracy).

A 10-Ω, 1-nF RC filter (R5, C6) is placed at the input of the comparator to filter the input signal and reduce noise sensitivity. This filter adds 10 Ω × 1 nF = 10 ns of propagation delay that must be considered when calculating the overall response time of the protection circuit. Larger filter constants are preferable to increase noise immunity if the system can tolerate the additional delay.

Table 8-2 summarizes the key parameters of the design.

Table 8-2. Overcurrent Detection Design Example

PARAMETER	VALUE
Reference resistor value (R1)	1.96 kΩ
Reference capacitor value (C5)	100 nF
Reference voltage	196 mV
Reference voltage settling time (to 90% of final value)	470 µs
Overcurrent trip threshold (rising)	200 mV / 20.0 A
Overcurrent trip threshold (falling)	196 mV / 19.6 A

8.2.2 Overvoltage Detection

Industrial motor drive systems commonly deploy an active or passive rectifier stage to generate a high-voltage, DC link potential from a single- or three-phase AC line input. The DC link voltage is sensed by an isolated amplifier such as the AMC1311B for control purposes. Power stages connected to the DC link rail may be sensitive to overvoltage conditions that can occur (for example, during a braking operation). The isolated amplifier may not be able to alert the system controller fast enough to take appropriate action to reduce the DC link voltage (for example, by turning on the break resistor) in case of an overvoltage condition. Therefore, a fast, isolated comparator is required to detect overvoltage conditions.

Figure 8-2 shows an active rectifier stage where the DC link voltage is sensed by an AMC1311B isolated amplifier. The AMC23C12 is connected parallel to the AMC1311B and monitors the voltage across RSNS for overvoltage conditions. The overvoltage trip-threshold is set by the R1 resistor connected to the REF pin of the AMC23C12. The open-drain OUT pin of the AMC23C12 is connected to a GPIO or interrupt pin of the MCU and is actively pulled low whenever the input voltage (V_{IN}) exceeds the reference voltage (V_{REF}).

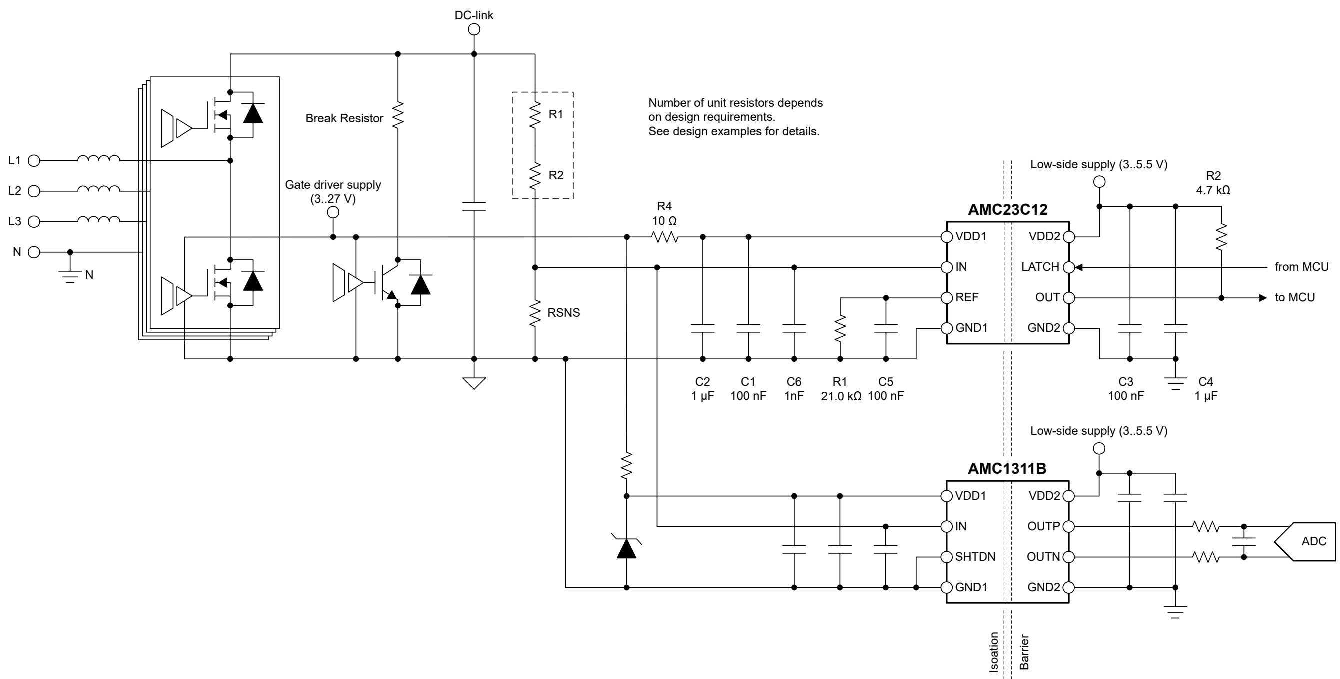


Figure 8-2. Using the AMC23C12 for Overvoltage Detection

8.2.2.1 Design Requirements

Table 8-3 lists the parameters for the application example in Figure 8-2.

Table 8-3. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3 V to 27 V
Low-side supply voltage	3 V to 5.5 V
Nominal DC link voltage	400 V
Linear full-scale input voltage of the AMC1311B	2 V
DC link voltage range for linear sensing	0 V to 450 V
DC link overvoltage detection threshold	480 V

8.2.2.2 Detailed Design Procedure

The voltage divider consisting of R1, R2, and RSNS is sized such that the voltage drop across RSNS equals the linear full-scale input voltage (2 V) of the AMC1311B at the maximum DC-link voltage that is of interest for linear sensing (450 V). Therefore, the voltage drop across RSNS at the overvoltage condition is 480 V / 450 V × 2 V = 2.133 V. This value is the target value for the reference voltage (V_{REF}) of the AMC23C12.

V_{REF} is determined by the external resistor R1 and the internal 100-µA current source of the AMC23C12. R1 is calculated as (V_{TRIP} – V_{HYS}) / I_{REF} = (2133 mV – 25 mV) / 100 µA = 21.08 kΩ. The closest value in the E192 series is 21.0 kΩ. The comparator hysteresis voltage (V_{HYS}) is subtracted from V_{TRIP} because the comparator trips at V_{REF} + V_{HYS}, see Figure 7-1. The hysteresis value is 25 mV because the reference voltage is greater than 550 mV, as explained in the *Reference Input* section.

Table 8-4 summarizes the key parameters of the design.

Table 8-4. Overvoltage and Undervoltage Detection Design Example

PARAMETER	VALUE
Reference resistor value (R1)	21.0 kΩ
Reference capacitor value (C5)	100 nF
Reference voltage	2100 mV
Reference voltage settling time (to 90% of final value)	4.85 ms
Overvoltage trip threshold (rising)	478 V
Overvoltage trip threshold (falling)	472 V

8.2.3 Application Curves

Figure 8-3 shows the typical response of the AMC23C12 to a bipolar, triangular input waveform with an amplitude of 720 mV_{PP}. The output (OUT) switches when VIN crosses the ±250-mV level determined by the REF pin voltage that is biased to 250 mV in this example.

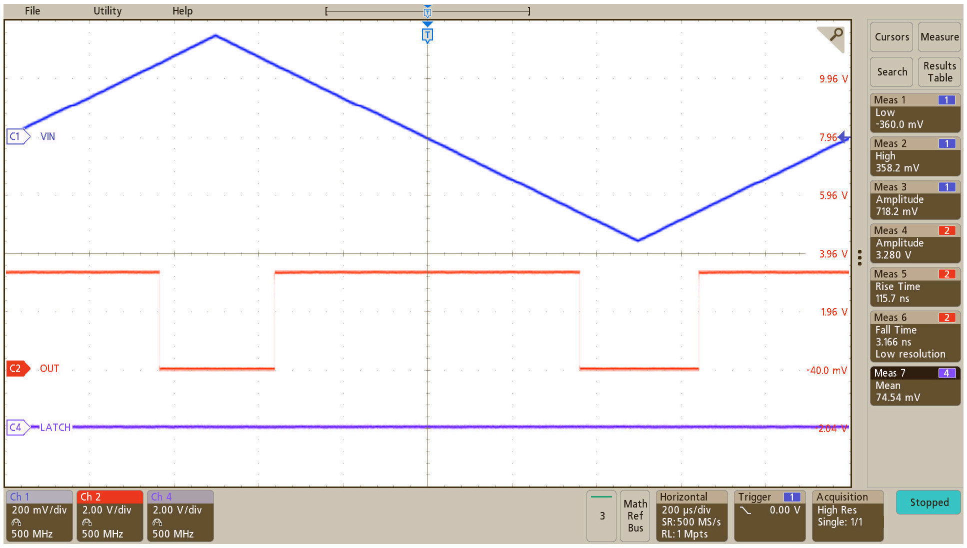


Figure 8-3. Output Response of the AMC23C12 to a Triangular Input Waveform

The integrated LDO of the AMC23C12 greatly relaxes the power-supply requirements on the high-voltage side and allows powering the device from non-regulated transformer, charge pump, and bootstrap supplies. As shown in Figure 8-4 and Figure 8-4, the internal LDO provides a stable operating voltage to the internal circuitry, allowing the trip thresholds to remain mostly undisturbed even at ripple voltages of 2 V_{PP} and higher.

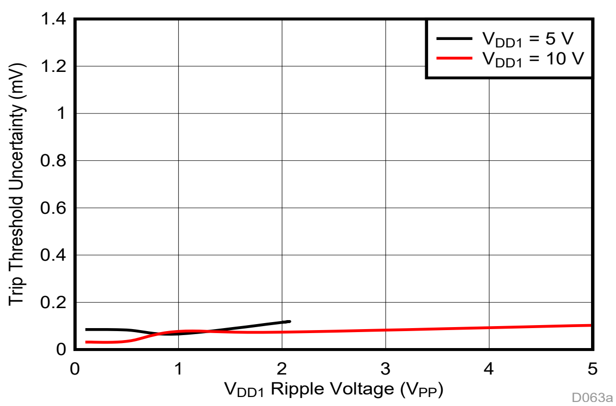


Figure 8-4. Trip Threshold Sensitivity to VDD1 Ripple Voltage (Cmp0, f_{RIPPLE} = 10 kHz)

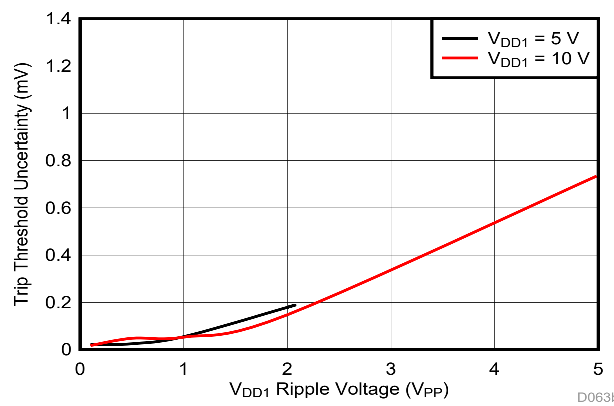


Figure 8-5. Trip Threshold Sensitivity to VDD1 Ripple Voltage (Cmp1, f_{RIPPLE} = 10 kHz)

8.3 Best Design Practices

Keep the connection between the low-side of the sense resistor and the GND1 pin of the AMC23C12 short and low impedance. Any voltage drop in the ground line adds error to the voltage sensed at the input of the comparator and leads to inaccuracies in the trip thresholds.

For best common-mode transient immunity, place the filter capacitor C5 as closely to the REF pin as possible as illustrated in Figure 8-7. Use a low value pullup resistor (<10 kΩ) on the open-drain output, as explained in the *Open-Drain Digital Output* section, to minimize the effect of capacitive coupling on the open-drain signal line during a common-mode transient event.

Do not exceed the 300-mV V_{REF} limit specified in the *Recommended Operating Conditions* table for bidirectional current-sensing applications. Do not operate the device with the REF pin biased close to the V_{MSEL} threshold (450-mV to 600-mV range) to avoid dynamic switching of the Cmp0 hysteresis as explained in the *Reference Input* section.

The AMC23C12 provides a limited 200-µs blanking time ($t_{HS,BLK}$) to allow the reference voltage (V_{REF}) to settle during start up. For many applications, the reference voltage takes longer to settle than the 200-µs blanking time and the output of the comparator can possibly glitch during system start up as described in Figure 7-2. Consider the reference voltage settling time in the overall system start-up design.

8.4 Power Supply Recommendations

The AMC23C12 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100-nF capacitor (C1) parallel to a low-ESR, 1-µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100-nF capacitor (C3) parallel to a low-ESR, 1-µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. Figure 8-6 shows a decoupling schematic for the AMC23C12.

For high VDD1 supply voltages (>5.5 V) place a 10-Ω resistor (R4) is series with the VDD1 power supply for additional filtering.

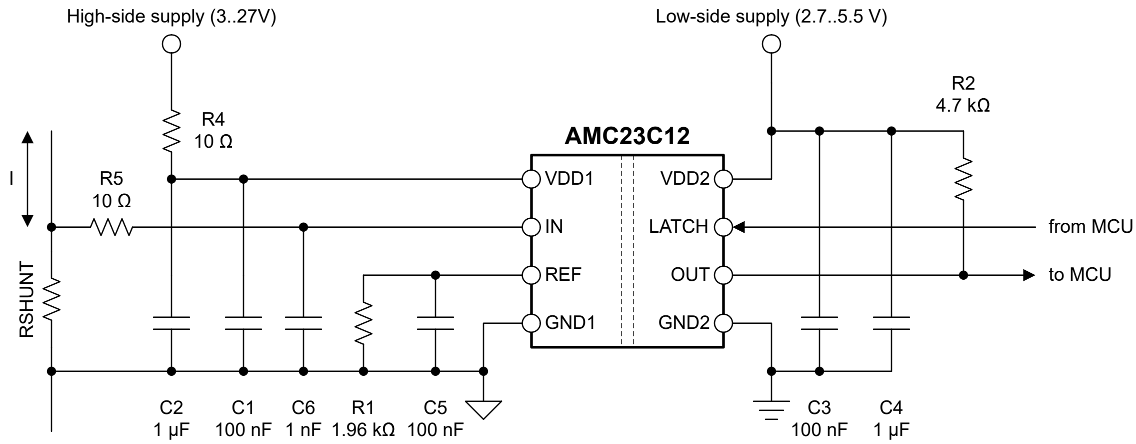


Figure 8-6. Decoupling of the AMC23C12

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCCs) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

8.5 Layout

8.5.1 Layout Guidelines

Figure 8-7 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC23C12 supply pins) and placement of the other components required by the device.

8.5.2 Layout Example

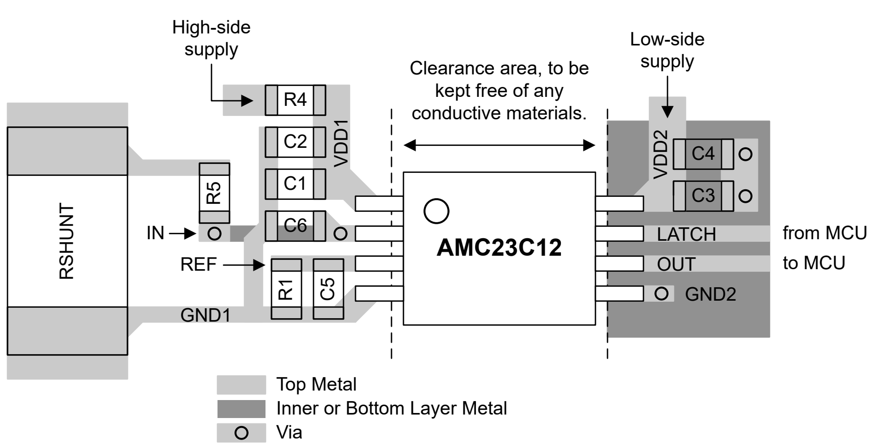


Figure 8-7. Recommended Layout of the AMC23C12

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *AMC1300 Precision, ±250-mV Input, Reinforced Isolated Amplifier* data sheet
- Texas Instruments, *AMC1311x High-Impedance, 2-V Input, Reinforced Isolated Amplifiers* data sheet
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PAMC23C12DWVR	ACTIVE	SOIC	DWV	8	1000	TBD	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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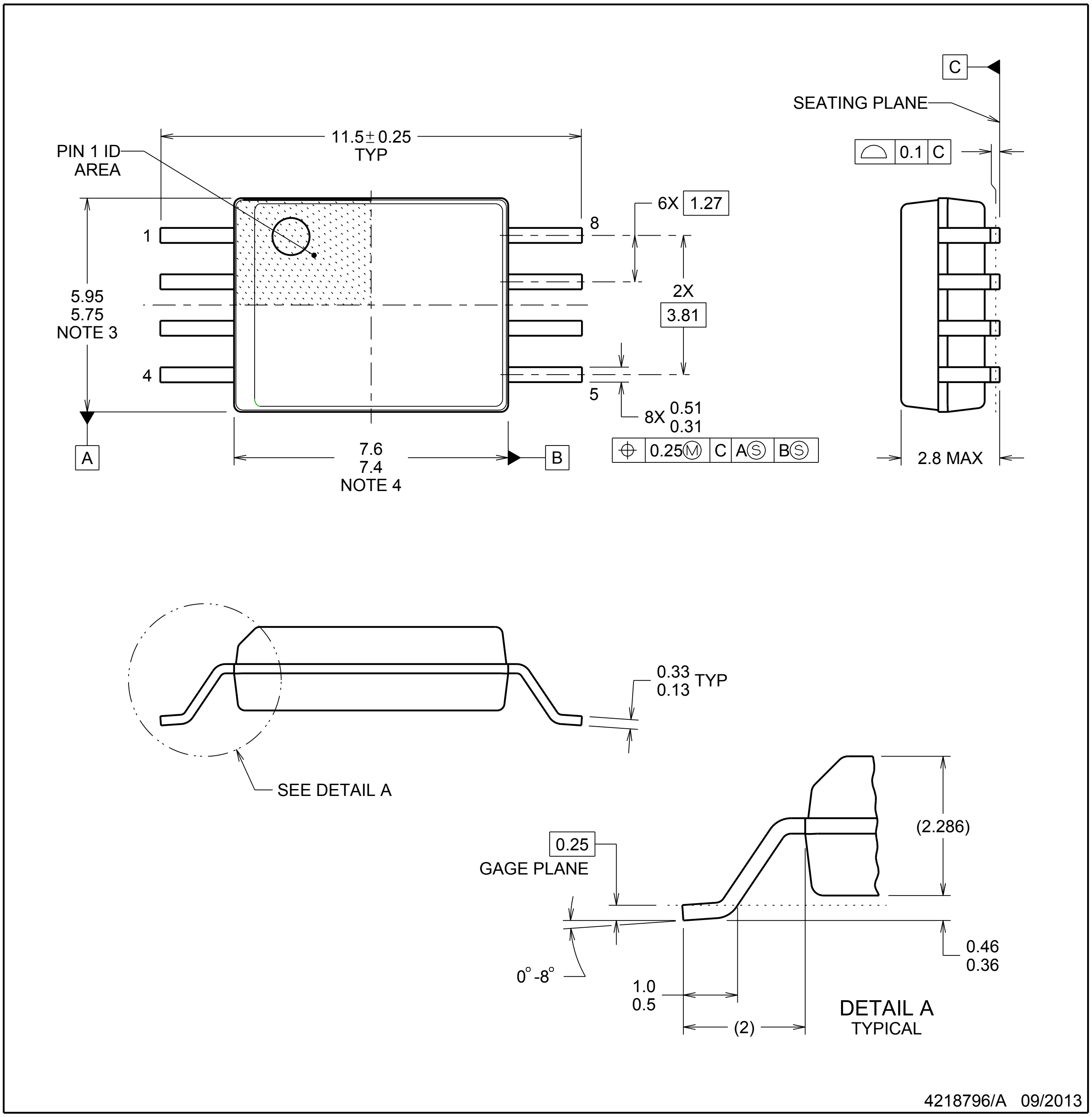
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AMC23C12 :

- Automotive : AMC23C12-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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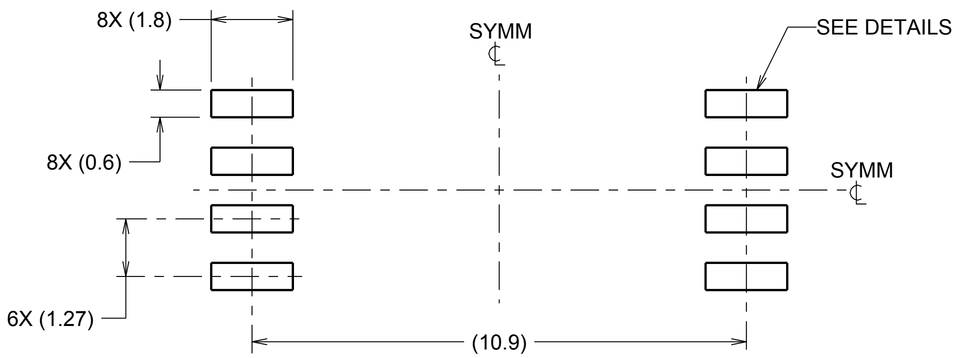
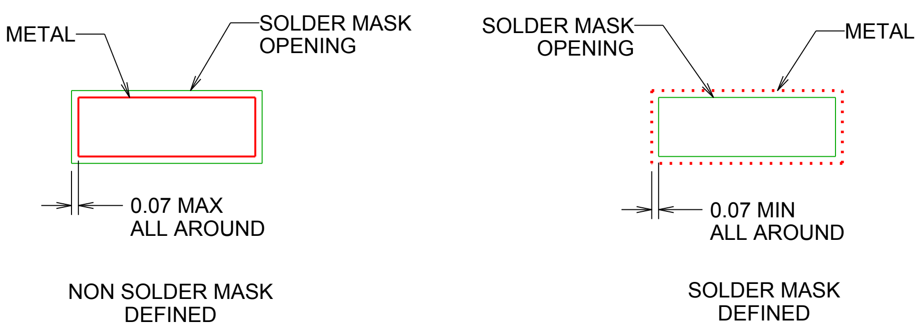
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

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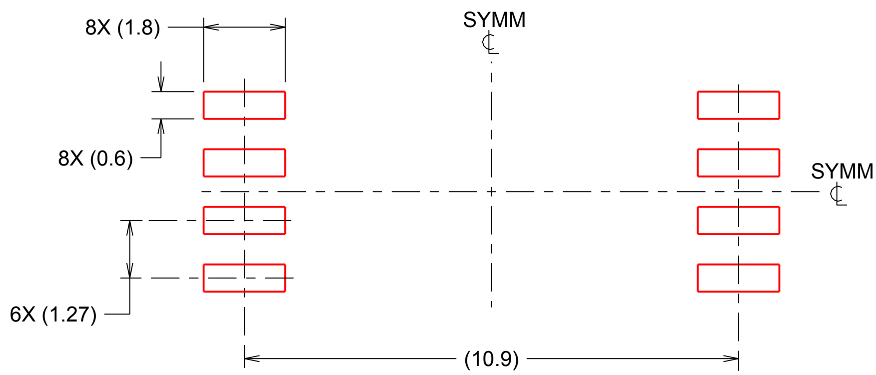
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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