Benchmarq Products from Texas Instruments

bq2050H

Low-Cost Lithium Ion Power Gauge™ IC

Features

- Accurate measurement of available capacity in Lithium Ion batteries
- Provides a low-cost battery management solution for pack integration
  - Complete circuit can fit in as little as ½ square inch of PCB
  - Low operating current (120µA typical)
  - Less than 100nA of data retention current
- High-speed (5kb) single-wire communication interface (HDQ bus) for critical battery parameters
- Monitors and controls charge FET in Li-Ion pack protection circuit
- Direct drive of remaining capacity LEDs
- Measurements automatically compensated for rate and temperature
- 16-pin narrow SOIC

General Description

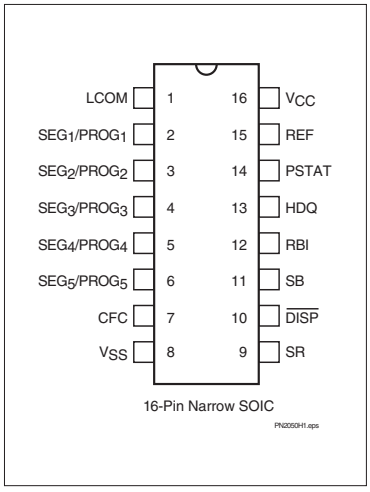
The bq2050H Lithium Ion Power Gauge™ IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery capacity. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. Compensations for battery temperature, self discharge, and rate of discharge are applied to the charge counter to provide available capacity information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

Nominal available capacity may be directly indicated using a five-segment LED display. These segments are used to graphically indicate available capacity. The bq2050H also supports a simple single-line bidirectional serial link to an external processor (common ground). The 5kb HDQ bus interface reduces communications overhead in the external microcontroller.

Internal registers include available capacity, temperature, scaled available energy, battery ID, battery status, and Li-Ion charge FET status. The external processor may also overwrite some of the bq2050H power gauge data registers.

The bq2050H can operate from the batteries in the pack. The REF output and an external transistor allow a simple, inexpensive voltage regulator to supply power to the circuit from the cells.

Pin Connections



16-Pin Narrow SOIC

Pin Names

LCOM	LED common output
$SEG_1/PROG_1$	LED segment 1/ program 1 input
$SEG_2/PROG_2$	LED segment 2/ program 2 input
$SEG_3/PROG_3$	LED segment 3/ program 3 input
$SEG_4/PROG_4$	LED segment 4/ program 4 input
$SEG_5/PROG_5$	LED segment 5/ program 5 input
CFC	Charge FET control output
V_{SS}	System ground
SR	Sense resistor input
$\overline{DISP}$	Display control input
SB	Battery sense input
RBI	Register backup input
HDQ	Serial communications input/output
PSTAT	Protector status input
REF	Voltage reference output
V_{CC}	Supply voltage

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Pin Descriptions

LCOM **LED common output**

This open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_5 **LED display segment outputs (dual function with $PROG_1$–$PROG_5$)**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ **Programmed full count selection inputs (dual function with SEG_1–SEG_2)**

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ **Power gauge scale selection inputs (dual function with SEG_3–SEG_4)**

These three-level input pins define the scale factor described in Table 2.

$PROG_5$ **Self-discharge rate selection (dual function with SEG_5)**

This three-level input pin defines the self-discharge and battery compensation factors as shown in Table 1.

CFC **Charge FET control output**

This pin can be used as an additional control to the charge FET of the Li-Ion pack protection circuitry.

V_{SS} **Ground**

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied between the negative terminal of the battery and the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2050H is $V_{SR} + V_{OS}$.

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during charge. $\overline{DISP}$ low activates the display. See Table 1.

SB **Secondary battery input**

This input monitors the battery cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds and battery-removed detection.

RBI **Register backup input**

This pin is used to provide backup potential to the bq2050H registers during periods when $V_{CC} \leq 3V$. A storage capacitor or a battery can be connected to RBI.

HDQ **Serial communication input/output**

This is the open-drain bidirectional communications port.

PSTAT **Protector status input**

This input provides overvoltage status from the Li-Ion protector circuit. It should connect to V_{SS} when not used.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

Functional Description

General Operation

The bq2050H determines battery capacity by monitoring the amount of current input to or removed from a rechargeable battery. The bq2050H measures discharge and charge currents, measures battery voltage, estimates self-discharge, monitors the battery for low battery-voltage thresholds, and compensates for temperature and discharge rate. Current measurement is measured by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. Scaled available energy is estimated using the remaining average battery voltage during the discharge cycle and the remaining nominal available capacity. The scaled available energy measurement is corrected for environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2050H using the LED display capability as a charge-state indicator. The bq2050H is configured to display capacity in relative display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. A push-button display feature is available for momentarily enabling the LED display.

The bq2050H monitors the charge and discharge currents as a voltage across a sense resistor. (See R_S in Figure 1.) A filter between the negative battery terminal and the SR pin is required.

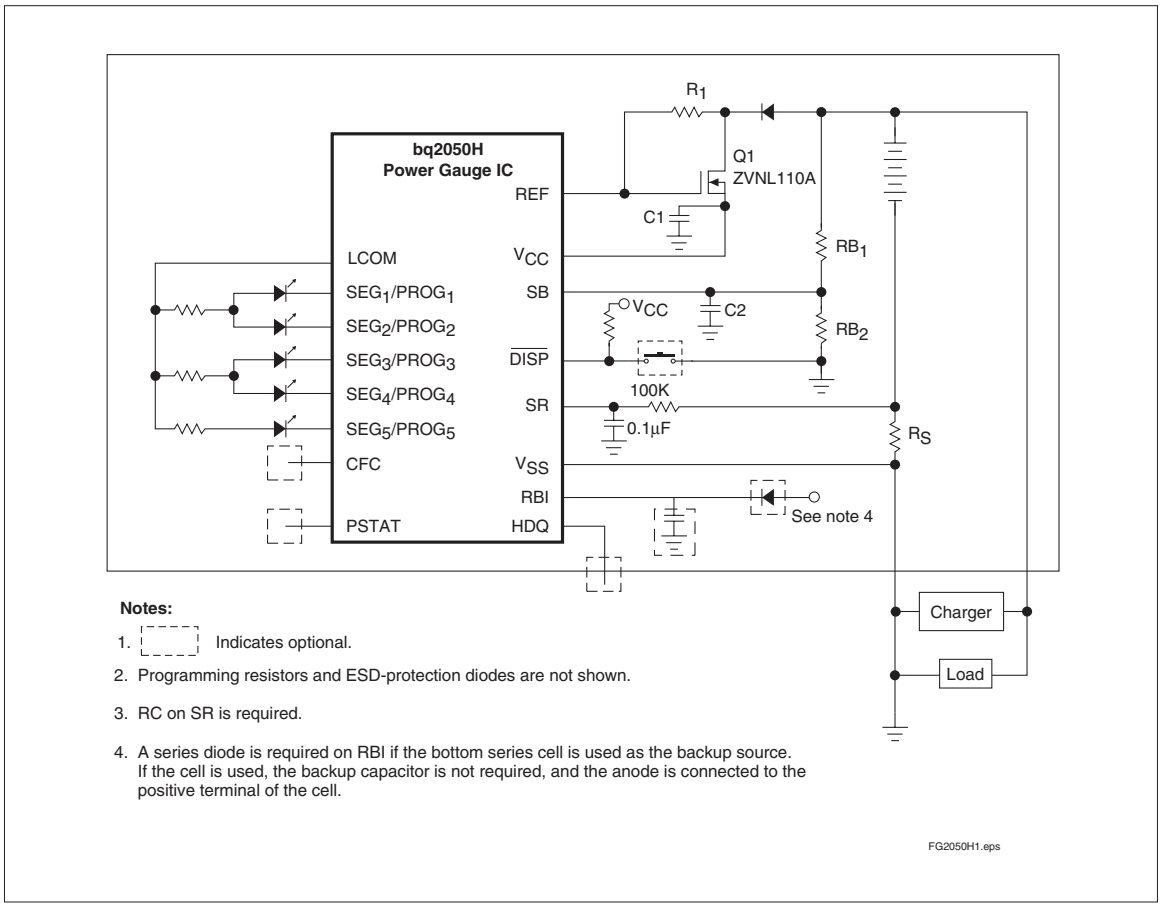


Figure 1. Battery Pack Application Diagram—LED Display

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2050H monitors the battery potential through the SB pin. The voltage is determined through a resistor-divider network per the following equation:

$$\frac{RB1}{RB2} = 4N - 1$$

where N is the number of cells, RB1 is connected to the positive battery terminal, and RB2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) thresholds. The EDV threshold levels are used to determine when the battery has reached an "empty" state.

The EDV thresholds for the bq2050H are programmable with the default values fixed at:

EDV1 (first) = 0.76V

EDVF (final) = EDV1-0.025V = 0.735V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge. The V_{SB} value is also available over the serial port.

During discharge and charge, the bq2050H monitors V_{SR} for various thresholds used to compensate the charge counter. EDV monitoring is disabled if the discharge rate is greater than 2C (OVLD Flag = 1) and resumes ½ second after the rate falls below 2C.

RBI Input

The RBI input pin is intended to be used with a storage capacitor or external supply to provide backup potential to the internal bq2050H registers when V_{CC} drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V. If using an external supply (such as the bottom series cell) as the backup source, an external diode is required for isolation.

Reset

The bq2050H can be reset by removing V_{CC} and grounding the RBI pin for 15 seconds or by commands over the serial port. The serial port reset command sequence requires writing 00h to register PPFC (address = 1Eh) and then writing 00h to register LMD (address = 05h).

Temperature

The bq2050H internally determines the temperature in 10°C steps centered from approximately -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown in the following table:

TMP (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2050H measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (C1 and C2) should be placed as close as possible to the V_{CC} and SB pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µF is recommended for V_{CC}.
- The sense-resistor capacitor should be placed as close as possible to the SR pin.
- The sense resistor (R_S) should be as close as possible to the bq2050H.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2050H. The bq2050H accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. The accumulated charge and discharge currents are adjusted for temperature and rate to provide the indication of compensated available capacity to the host system or user.

The main counter, Nominal Available Capacity (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2050H adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity equals the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

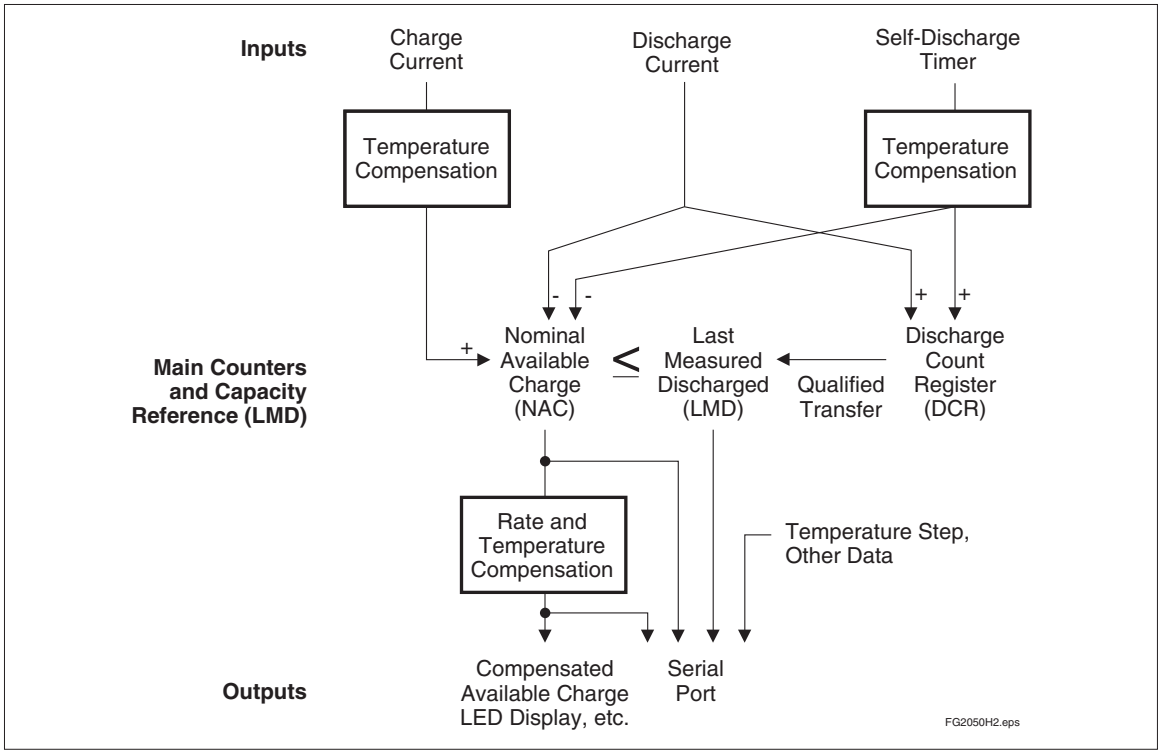


Figure 2. Operational Overview

2. Programmed Full Count (PFC) or initial battery capacity:

The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The bq2050H is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) ∗ sense resistor (Ω) =

PFC (mVh)

Selecting a PFC slightly less than the rated capacity provides a conservative capacity reference until the bq2050H "learns" a new capacity reference.

Example: Selecting a PFC Value

Given:

Sense resistor = 0.05Ω
Number of cells = 2
Capacity = 1000mAh, Li-Ion battery, coke-anode
Current range = 50mA to 1A
Relative display mode
Self-discharge = $^{NAC}/_{512}$ per day @ 25°C
Voltage drop over sense resistor = 2.5mV to 50mV
Nominal discharge voltage = 3.6V

Therefore:

1000mAh ∗ 0.05Ω = 50mVh

Table 1. Self-Discharge and Capacity Compensation

Pin Connection	$PROG_5$ Compensation/Self-Discharge (See Tables 3 and 4)	$\overline{DISP}$ Display State
H	Coke anode/disabled	LEDs disabled
Z	Coke anode/ $^{NAC}/_{512}$	LEDs on when charging
L	Graphite anode/ $^{NAC}/_{512}$	LEDs on for 4 s

Table 2. bq2050H Programmed Full Count mVh, V_{SR} Gain Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z or H			Units
1	2		$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	
-	-	-	SCALE = 1/80	SCALE = 1/160	SCALE = 1/320	SCALE = 1/640	SCALE = 1/1280	SCALE = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
V_{SR} equivalent to 2 counts/s (nom.)			90	45	22.5	11.25	5.6	2.8	mV

Select:

PFC = 30720 counts or 48mVh
$PROG_1$ = float
$PROG_2$ = low
$PROG_3$ = high
$PROG_4$ = float
$PROG_5$ = float

The initial full battery capacity is 48mVh (960mAh) until the bq2050H "learns" a new capacity with a qualified discharge from full to EDV1.

3. Nominal Available Capacity (NAC):

NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV1. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

4. Discharge Count Register (DCR):

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFh.

The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if all the following conditions are met:

- No valid charge initiations (charges greater than 2 NAC updates where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC = LMD and EDV1.
- The self-discharge is less than 6% of NAC.
- The temperature is ≥ 0°C when the EDV1 level is reached during discharge.
- VDQ is set

The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update. If the DCR update value is less than 0.94 * LMD, LMD will only be modified by 0.94 * LMD. This prevents invalid DCR values from corrupting LMD.

5. Scaled Available Energy (SAE):

SAE is useful in determining the available energy within the battery, and may provide a more useful capacity reference in battery chemistries with sloped voltage profiles during discharge. SAE may be converted to an mWh value using the following formula:

$$E(mWh) = (SAEH * 256 + SAEL) * \frac{1.2 * SCALE * (R_{B1} + R_{B2})}{R_S * R_{B2}}$$

where R_{B1}, R_{B2}, and R_S are resistor values in ohms, as shown in Figure 1. SCALE is the selected scale from Table 2.

6. Compensated Available Capacity (CACT)

CACT counts similarly to NAC, but contains the available capacity compensated for discharge rate and temperature.

Charge Counting

Charge activity is detected based on a positive voltage on the SR input. If charge activity is detected, the bq2050H increments NAC at a rate proportional to V_{SR} and, if enabled, activates an LED display.

The bq2050H counts charge activity when the voltage at the SR input (V_{SRO}) exceeds the minimum charge threshold (V_{SRQ}). A valid charge is detected when NAC has been updated twice without discharging or reaching the digital magnitude filter time-out. Once a valid charge is detected, charge counting continues until V_{SR}, including offset, falls below V_{SRQ}.

Discharge Counting

Discharge activity is detected based on a negative voltage on the SR input. All discharge counts where V_{SRO} is less than the minimum discharge threshold (V_{SRD}) cause the NAC register to decrement and the DCR to increment.

Self-Discharge Counting

The bq2050H continuously decrements NAC and increments DCR for self-discharge based on time and temperature.

Charge/Discharge Current

The bq2050H current-scale registers, VSRH and VSRL, can be used to determine the battery charge or discharge current. See the Current Scale Register description for details.

Count Compensations

Compensated Available Capacity

Compensated Available Capacity compensation is based on the rate of discharge, temperature, and negative electrode type. Tables 3A and 3B outline the correction factor typically used for graphite-anode Li-Ion batteries, and Tables 4A and 4B outline the factors typically used for coke-anode Li-Ion batteries. The compensation factor is applied to NAC to derive the CACD and CACT values.

Table 3A. Graphite Anode

Approximate Discharge Rate	Available Capacity Reduction
< 0.5C	0
≥ 0.5C	0.05 * LMD

Table 3B. Graphite Anode

Temperature	Available Capacity Reduction
≥ 10°C	0
0°C to 10°C	0.05 * LMD
-20°C to 0°C	0.15 * LMD
≤ -20°C	0.37 * LMD

Table 4A. Coke Anode

Approximate Discharge Rate	Available Capacity Reduction
<0.5C	0
≥ 0.5C	0.10 * LMD

Table 4B. Coke Anode

Temperature	Available Capacity Reduction
≥ 10°C	0
0°C to 10°C	0.10 * LMD
-20°C to 0°C	0.30 * LMD
≤ -20°C	0.60 * LMD

The CACD value is the available charge compensated for the rate of discharge. At high discharge rates, CACD is reduced. The reduction is maintained until a valid charge is detected. The CACT value is the available charge compensated for the rate of discharge and temperature. The CACT value is used to drive the LED display.

Charge Compensation

The bq2050H also monitors temperature during charge. If the temperature is <0°C, NAC will only increment up to 0.94 * LMD, inhibiting VDQ from being set. This keeps a "learn" cycle from occurring when the battery is charged at very low temperatures. If the temperature rises above 0°C, NAC will be allowed to count up to NAC = LMD.

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $1/512$ * NAC per day. This is the rate that NAC is reduced for a battery within the 20–30°C temperature range. This rate varies across 8 ranges from <10°C to >70°C, as shown in Table 5.

Table 5. Self-Discharge Compensation

Temperature Range	Typical Rate $PROG_5$ = Z or L
< 10°C	$NAC/2048$
10–20°C	$NAC/1024$
20–30°C	$NAC/512$
30–40°C	$NAC/256$
40–50°C	$NAC/128$
50–60°C	$NAC/64$
60–70°C	$NAC/32$
> 70°C	$NAC/16$

Self-discharge may be disabled by connecting $PROG_5$ = H.

Digital Magnitude Filter

The bq2050H has a digital filter to eliminate charge and discharge counting below a set threshold. The minimum charge (V_{SRQ}) and discharge (V_{SRD}) threshold for the bq2050H is 250µV.

Pack Protection Supervision

The bq2050H can monitor the charge FET in a Li-Ion pack protector circuit as shown in Figure 3. If the battery voltage is too high or the temperature is out of the 0—60°C range, the bq2050H disables the charge FET with the CFC output, which turns off the charge to the pack.

The PSTAT input is used to monitor the protector state. If PSTAT is above 2.5V, bit 5 of FLGS1 is set to 1. If PSTAT is below 0.5V, bit 5 of FLGS1 is cleared to zero. Using this input, the system can monitor the state of the charge con-

Table 6. bq2050H Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

trol FET signal and can quickly determine if the protector circuit is operating properly during charge.

Register 15h, NMCV, is used to set the maximum battery voltage for the battery stack. If V_{SB} > NMCV or the battery temperature is < 0°C or > 60°C, then CFC is driven low.

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description). It is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 6 shows the non-linearity and non-repeatability errors associated with the bq2050H current sensing.

Table 7 illustrates the current-sensing error as a function of V_{OS}. A digital filter prevents charge and discharge counts to the NAC register when V_{SRO} is between V_{SRQ} and V_{SRD}.

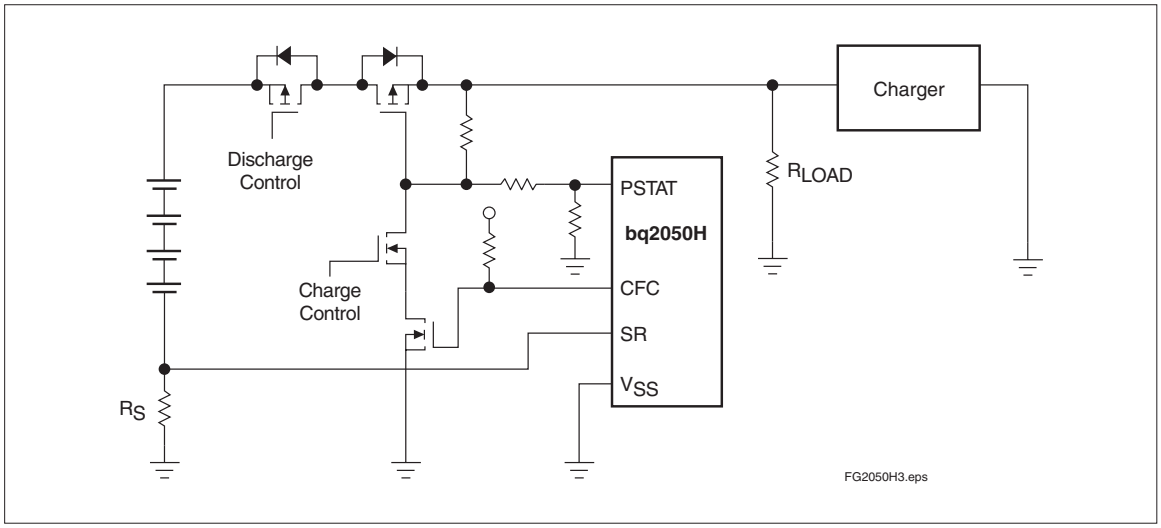


Figure 3. bq2050H Pack Supervision

Table 7. V_{OS}-Related Current Sense Error (Current = 1A)

V_{OS} (μV)	Sense Resistor			
	20	50	100	mΩ
50	0.25	0.10	0.05	%
100	0.50	0.20	0.10	%
150	0.75	0.30	0.15	%
180	0.90	0.36	0.18	%

Communicating With the bq2050H

The bq2050H includes a simple single-pin (HDQ plus return) serial data interface. A host processor uses the interface to access various bq2050H registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain HDQ pin on the bq2050H should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2050H. The command directs the bq2050H to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte. (See Figure 4.)

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5K bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2050H may be sampled using the pulse--width capture timers available on some microcontrollers.

If a communication error occurs (e.g., $t_{CYCB} > 250\mu s$), the bq2050H should be sent a BREAK to reinitiate the serial interface. A BREAK is detected when the HDQ pin is driven to a logic-low state for a time, t_B or greater. The HDQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2050H is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2050H taking the HDQ pin to a logic-low state for a period, $t_{STRH;B}$. The next section is the actual data transmission, where the data should be valid by a period, $t_{DSU;B}$, after the negative edge used to start communication. The data should be held for a period, $t_{DH;DV}$, to allow the host or bq2050H to sample the data bit.

The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a period, $t_{SSU;B}$, after the negative edge used to start communication. The final logic-high state should be until a period $t_{CYCH;B}$, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2050H is always performed with the least-significant bit being transmitted first. Figure 5 shows an example of a communication sequence to read the bq2050H NACH register.

bq2050H Command Code and Registers

The bq2050H status registers are listed in Table 8 and described below. All registers are Read/Write in the bq2050H. **Caution: When writing to bq2050H registers ensure that proper data is written. A write-verify read is recommended.**

Command Code

The bq2050H latches the command code when eight valid command bits have been received by the bq2050H. The command code contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command code is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

Command Code Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2050H outputs the requested register contents specified by the address portion of command code.

1 The following eight bits should be written to the register specified by the address portion of command code.

The lower seven-bit field of the command code contains the address portion of the register to be accessed.

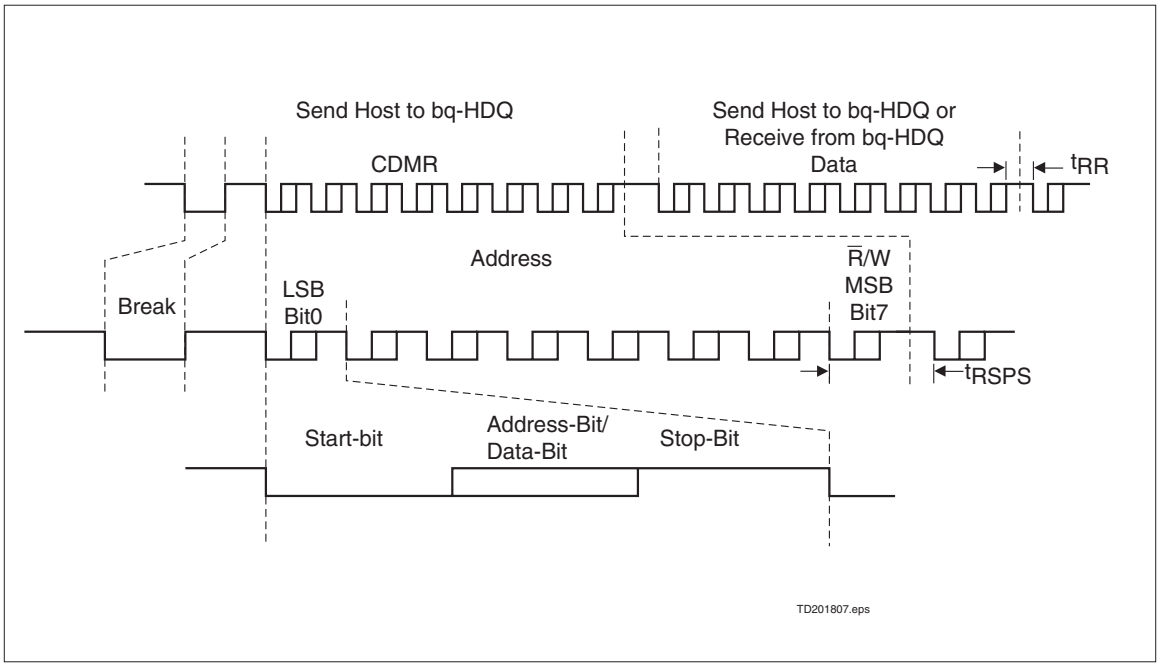


Figure 4. bq2050H Communication Example

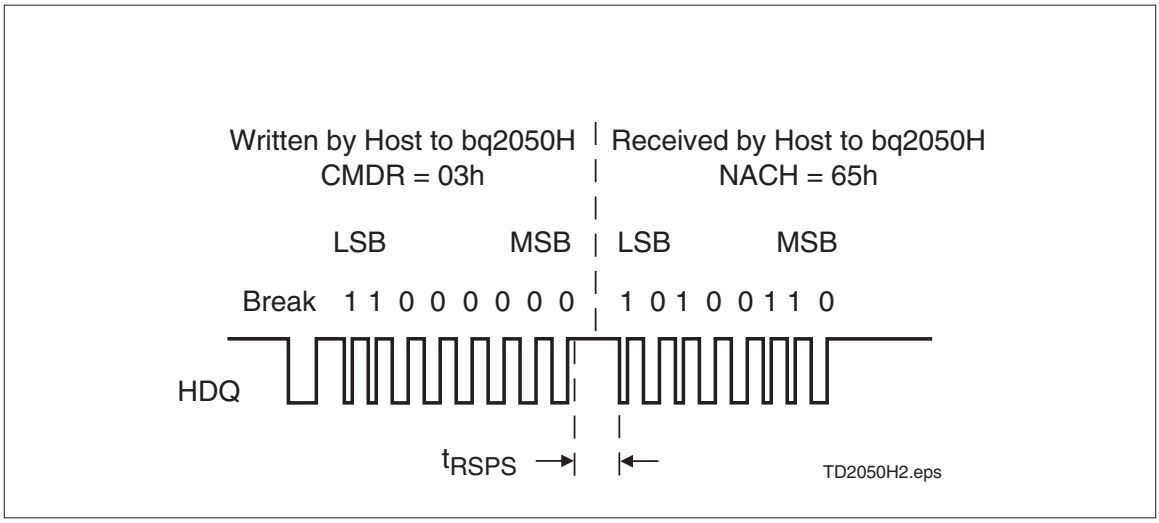


Figure 5. Typical Communication With the bq2050H

Table 8. bq2050H Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
FLGS1	Primary status flags register	01h	R	CHGS	BRP	PSTAT	CI	VDQ	1	EDV1	EDVF
TMP	Temperature register	02h	R	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available capacity high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available capacity low byte register	17h	R/W	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	R	RSVD	DR2	DR1	DR0	ENINT	VQ	RSVD	OVLD
PPD	Program pin pull-down register	07h	R	RSVD	RSVD	RSVD	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	R	RSVD	RSVD	RSVD	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	R/W	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
VSB	Battery voltage register	0bh	R	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	End-of-discharge threshold select register	0ch	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
CACT	Temperature and Discharge Rate compensated available capacity	0dh	R/W	CACT7	CACT6	CACT5	CACT4	CACT3	CACT2	CACT1	CACT0
CACD	Discharge Rate compensated available capacity	0eh	R/W	CACD7	CACD6	CACD5	CACD4	CACD3	CACD2	CACD1	CACD0
SAEH	Scaled available energy high byte register	0fh	R	SAEH7	SAEH6	SAEH5	SAEH4	SAEH3	SAEH2	SAEH1	SAEH0
SAEL	Scaled available energy low byte register	10h	R	SAEL7	SAEL6	SAEL5	SAEL4	SAEL3	SAEL2	SAEL1	SAEL0
RCAC	Relative CAC	11h	R	-	RCAC6	RCAC5	RCAC4	RCAC3	RCAC2	RCAC1	RCAC0
VSRH	Current scale high	12h	R	VSRH7	VSRH6	VSRH5	VSRH4	VSRH3	VSRH2	VSRH1	VSRH0
VSRL	Current scale low	13h	R	VSRL7	VSRL6	VSRL5	VSRL4	VSRL3	VSRL2	VSRL1	VSRL0
NMCV	Maximum cell voltage	15h	R/W	NMCV7	NMCV6	NMCV5	NMCV4	NMCV3	NMCV2	NMCV1	NMCV0
DCR	Discharge register	18h	R/W	DCR7	DCR6	DCR5	DCR4	DCR3	DCR2	DCR1	DCR0
PPFC	Program pin data	1eh	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
INTSS	V_{OS} Interrupt	38h	R	RSVD	RSVD	RSVD	RSVD	DCHGI	RSVD	RSVD	CHGI
RST	Reset register	39h	R/W	RST	0	0	0	0	0	0	0
HEXFF	Check register	3fh	R/W	1	1	1	1	1	1	1	1

Notes: RSVD = reserved.

All other registers not documented are reserved.

Command Code Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The FLGS1 register (address = 01h) contains the primary bq2050H flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} \leq V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The ***battery replaced*** flag (BRP) is asserted whenever the bq2050H is reset either by application of V_{CC} or by a serial port command. BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 bq2050H is reset

The *protector status* flag (PSTAT) provides information on the state of the overvoltage protector within the Li-Ion battery pack. The PSTAT flag is asserted whenever this input is high and is cleared when the input is low.

The PSTAT values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	PSTAT	-	-	-	-	-

Where PSTAT is:

0 PSTAT input is low (PSTAT < 0.5V)

1 PSTAT input is high (PSTAT > 2.5V)

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2050H is reset. The flag is cleared after an LMD update.

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or the bq2050H is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2050H is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- When NAC has been reduced by more than 6% because of self-discharge since VDQ was set.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 2 NAC updates.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 Self-discharge of 6% of NAC, valid charge action detected, EDV1 asserted with the temperature less than 0°C, or reset

1 On first discharge after NAC = LMD

The ***first end-of-discharge warning*** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected. The EDV1 threshold is externally controlled via the VTS register (see Voltage Threshold Register).

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq V_{TS}$

1 $V_{SB} < V_{TS}$ providing that the discharge rate is < 2C

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EDVF threshold is set 25mV below the EDV1 threshold.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq (V_{TS} - 25mV)$

1 $V_{SB} < (V_{TS} - 25mV)$ providing the discharge rate is < 2C

Temperature Register (TMP)

The TMP register (address=02h) contains the battery temperature.

The bq2050H contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown in Table 9.

TMP Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	-

The bq2050H calculates the gas gauge bits, GG3-GG0 as a function of CACT and LMD. The results of the calculation give available capacity in $1/16$ increments from 0 to $15/16$.

TMP Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

Table 9. Temperature Register

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

Nominal Available Capacity Registers (NACH/NACL)

The NACH high-byte register (address=03h) and the NACL low-byte register (address=17h) are the main gas gauging registers for the bq2050H. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. NACH and NACL are set to 0 during a bq2050H reset.

Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2050H gas gauge operation. Do not write the NAC registers to a value greater than LMD.

Battery Identification Register (BATID)

The BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{RBI} is greater than 2V. The contents of BATID have no effect on the operation of the bq2050H. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is the register (address=05h) that the bq2050H uses as a measured full reference. The bq2050H adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2050H updates the capacity of the battery. LMD is set to PFC during a bq2050H reset.

LMD is set to DCR upon the first valid charge after EDV is set if VDQ is set.

If DCR < 0.94 LMD, then LMD is set to 0.94 * LMD.

Secondary Status Flags Register (FLGS2)

The FLGS2 register (address=06h) contains the secondary bq2050H flags.

Bit 7 and bit 1 of FLGS2 are reserved. Do not write to these bits.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current discharge regime as follows:

DR2	DR1	DR0	Discharge Rate
0	0	0	DRATE < 0.5C
0	0	1	0.5C ≤ DRATE < 2C
0	1	0	2C < DRATE

The ***enable interrupt*** flag (ENINT) is a test bit used to determine V_{SR} activity sensed by the bq2050H. The state of this bit will vary and should be ignored by the system.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	ENINT	-	-	

The ***valid charge*** flag (VQ), bit 2 of FLGS2, is used to indicate whether the bq2050H recognizes a valid charge condition. This bit is reset on the first discharge after NAC = LMD.

The VQ values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	VQ	-	

Where VQ is:

0 Valid charge action not detected between a discharge from NAC = LMD and EDV1

1 Valid charge action detected

The ***overload*** flag (OVLD) is asserted when a discharge rate in excess of 2C is detected. OVLD remains asserted as long as the condition persists and is cleared 0.5 seconds after the rate drops below 2C. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

Program Pin Pull-Down Register (PPD)

The PPD register (address=07h) contains some of the programming pin information for the bq2050H. The segment drivers, $SEG_{1–5}$, have a corresponding PPD register location, $PPD_{1–5}$. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xxx01001.

Program Pin Pull-Up Register (PPU)

The PPU register (address=08h) contains the rest of the programming pin information for the bq2050H. The segment drivers, $SEG_{1–5}$, have a corresponding PPU register location, $PPU_{1–5}$. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and SEG_5 have pull-up resistors, the contents of PPU are xxx10100.

PPD/PPU Bits							
7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
RSVD	RSVD	RSVD	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2050H adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and there has been no more than a 6% self-discharge reduction.

The CPI register is incremented every time a valid charge is detected. When NAC > 0.94 * LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 * LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Battery Voltage Register (VSB)

The battery voltage register is used to read the single-cell battery voltage on the SB pin. The VSB register (address = 0Bh) is updated approximately once per second with the present value of the battery voltage.
V_{SB} = 1.2V * (VSB/256).

VSB Register Bits							
7	6	5	4	3	2	1	0
VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0

Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register (address = 0Ch). The VTS register sets the EDV1 trip point. EDVF is set 25mV below EDV1. The default value in the VTS register is A2h, representing EDV1 = 0.76V and EDVF = 0.735V. EDV1 = 1.2V * (VTS/256).

VTS Register Bits							
7	6	5	4	3	2	1	0
VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0

Compensated Available Charge Registers (CACT/CACD)

The CACD register (address = 0Eh) contains the NAC value compensated for discharge rate. This is a monotonicly decreasing value during discharge. If the discharge rate is > 0.5C then this value is lower than NAC. CACD is updated only when the discharge rate compensated NAC value is a lower value than CACD during discharge. During charge, CACD is continuously updated with the NAC value.

The CACT register (address = 0Dh) contains the CACD value compensated for temperature. CACT will contain a value lower than CACD when the battery temperature is below 10°C. The CACT value is also used in calculating the LED display pattern.

Scaled Available Energy Registers (SAEH/SAEL)

The SAEH high-byte register (address = 0Fh) and the SAEL low-byte register (address = 10h) are used to scale battery voltage and CACT to a value that can be translated to watt-hours remaining under the present conditions.

Relative CAC Register (RCAC)

The RCAC register (address = 11h) provides the relative battery state-of-charge by dividing CACT by LMD. RCAC varies from 0 to 64h representing relative state-of-charge from 0 to 100%.

Current Scale Register (VSRH/VSRL)

The VSRH register (address = 12h) and the VSRL register (address = 13h) report the average signal across the SR and V_{SS} pins. The bq2050H updates this register pair every 22.5s. V_{SRH} (high-byte) and V_{SRL} (low-byte) form a 16-bit signed integer value representing the average current during this time. The battery pack current can be calculated from:

$$I(mA) = (V_{SRH} * 256 + V_{SRL})/(8 * R_S)$$

where:

R_S = sense resistor value in Ω.
V_{SRH} = high-byte value of battery current
V_{SRL} = low-byte value of battery current

The bq2050H indicates an average discharge current with a “1” in the MSB position of the VSRH register. To calculate discharge current, use the 2’s complement if the concatenated register contents in the above equation.

Maximum Cell Voltage Register (NMCV)

The NMCV register (address 15h) is used to set the maximum battery pack voltage for control of the CFC pin. If desired, the system can write a value to NMCV to enable CFC to go low if V_{SB} exceeds this value. This may be useful as a secondary protection of the Li-Ion battery pack. NMCV should be set to the following equation:

$$\text{NMCV} = \text{2s complement of}\left(\frac{256 * \text{MCV} * \text{RB2}}{1.2 * (\text{RB1} + \text{RB2})}\right)$$

Where:

MCV = maximum desired battery stack voltage.

NMCV = set to 00h on power up or reset and should be programmed to the desired value by the host system.

Discharge Count Register (DCR)

The DCR register (address = 18h) stores the high-byte of the discharge count. DCR is reset to zero at the start of a valid discharge cycle and can count to a maximum of FFh. DCR will not increment if EDV1 = 1 and will not roll over from FFh.

Program Pin Full Count (PPFC)

The PPFC register contains information concerning the program pin configuration. This information is used to determine the data integrity of the bq2050H. **The only approved user application for this register is to write a zero to this register as part of a reset request.**

Voltage Offset (V_{OS}) Interrupt (INTSS)

The INTSS register (address = 38h) is useful during intial characterization of bq2050H designs. When the bq2050H counts a charge pulse, CHGI (bit 0) will be set to 1. When the bq2050H counts a discharge pulse, DCHGI (bit 3) will be set to 1. All other locations in the INTSS register are reserved.

Reset Register (RST)

The reset register (address = 39h) provides an alternate means of initializing the bq2050H via software. Since this register contains device test bits, it is recommended to use the PPFC and LMD registers to reset the bq2050H. **Setting any bits in the reset register is not allowed and will result in improper bq2050H operation.** The recommended reset method for the bq2050H is :

- Write PPFC to zero
- Write LMD to zero

After these operations, a software reset will occur.

Resetting the bq2050H sets the following:

- LMD = PFC
- CPI, VDQ, RCAC, NACH/L, CACH/L, SAEH/L, NMCV = 0
- CI and BRP = 1

Check Register (HEXFF)

The HEXFF register (address = 3F) is useful in determing if the device is a bq2050H or a bq2050. This register is always set to FFh for the bq2050H. The bq2050 returns data other than FFh.

Display

The bq2050H can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2050H displays the battery charge state in relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

The capacity display is also adjusted for the present battery temperature and discharge rate. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the CACT and CACD register descriptions.

When $\overline{\text{DISP}}$ is tied to V_{CC}, the $SEG_{1–5}$ outputs are inactive. When $\overline{\text{DISP}}$ is left floating, the display becomes active whenever the bq2050H detects a charge in progress $V_{SRO} > V_{SRQ}$. When pulled low, the segment outputs become active for a period of four seconds, ± 0.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

A micropower source for the bq2050H can be inexpensively built using a FET and an external resistor. (See Figure 1.)

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	Vcc+0.7	V	100kΩ series resistor should be used to protect SR in case of a shorted battery.
T_{OPR}	Operating temperature	0	+70	°C	Commercial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV1}	First empty warning	0.73	0.76	0.79	V	SB, default
V_{EDVF}	Final empty warning	V_{EDV1} - 0.035	V_{EDV1} - 0.025	V_{EDV1} - 0.015	V	SB, default
V_{SRO}	SR sense range	-300	-	+500	mV	SR, V_{SR} + V_{OS}
V_{SRQ}	Valid charge	250	-	-	µV	V_{SR} + V_{OS} (see note)
V_{SRD}	Valid discharge	-	-	-250	µV	V_{SR} + V_{OS} (see note)
V_{MCV}	Maximum SB voltage	1.10	1.12	1.15	V	SB pin

Note: V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See “Layout Considerations.”

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{OS}	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP}$ = VCC
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, HDQ = 0
		-	120	180	µA	V_{CC} = 4.25V, HDQ = 0
		-	170	250	µA	V_{CC} = 6.5V, HDQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
I_{RBI}	RBI data retention current	-	-	100	nA	V_{RBI} > V_{CC} < 3V
R_{HDQ}	Internal pulldown	500	-	-	KΩ	
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IHPFC}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_{1–5}$
V_{ILPFC}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_{1–5}$
V_{IZPFC}	Logic input Z	float	-	float	V	$PROG_{1–5}$
V_{OLSL}	SEG output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_5, CFC
V_{OLSH}	SEG output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_5, CFC
V_{OHML}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHMH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} > 3.5V, I_{OHLCOM} = -33.0mA
I_{OLS}	SEG sink current	11.0	-	-	mA	At V_{OLSH} = 0.4V, V_{CC} = 6.5V
I_{OL}	Open-drain sink current	5.0	-	-	mA	At V_{OL} = V_{SS} + 0.3V, HDQ
V_{OL}	Open-drain output low	-	-	0.3	V	I_{OL} ≤ 5mA, HDQ
V_{IHDQ}	HDQ input high	2.5	-	-	V	HDQ
V_{ILDQ}	HDQ input low	-	-	0.8	V	HDQ
V_{IH}	Logic input high	2.5	-	-	V	PSTAT
V_{IL}	Logic input low	-	-	0.5	V	PSTAT
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_{1–5}$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_{1–5}$

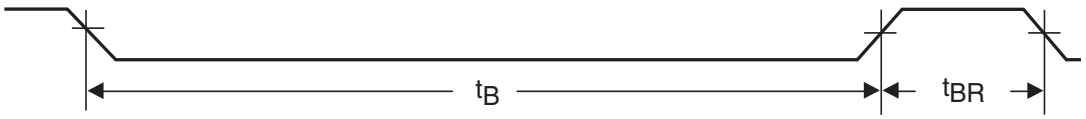
Note: All voltages relative to V_{SS}.

High-Speed Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2050H (write)	190	-	-	µs	See note
t_{CYCB}	Cycle time, bq2050H to host (read)	190	205	250	µs	
t_{STRH}	Start hold, host to bq2050H (write)	5	-	-	ns	
t_{STRB}	Start hold, bq2050H to host (read)	32	-	-	µs	
t_{DSU}	Data setup	-	-	50	µs	
t_{DSUB}	Data setup	-	-	50	µs	
t_{DH}	Data hold	90	-	-	µs	
t_{DV}	Data valid	-	-	80	µs	
t_{SSU}	Stop setup	-	-	145	µs	
t_{SSUB}	Stop setup	-	-	145	µs	
t_{RSPS}	Response time, bq2050H to host	190	-	320	µs	
t_B	Break	190	-	-	µs	
t_{BR}	Break recovery	40	-	-	µs	

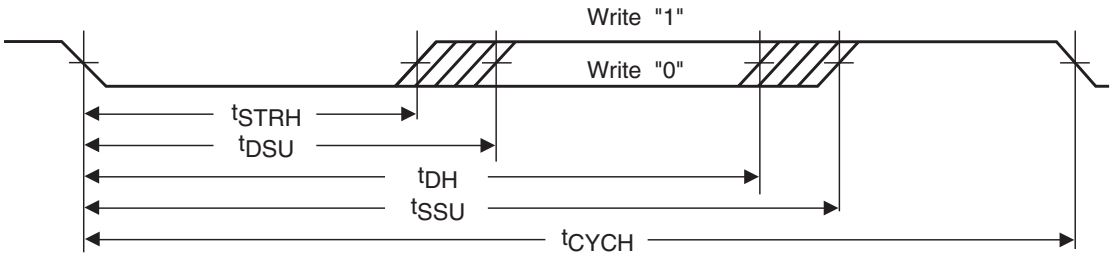
Note: The open-drain HDQ pin should be pulled to at least V_{CC} by the host system for proper HDQ operation. HDQ may be left floating if the serial interface is not used.

Break Timing

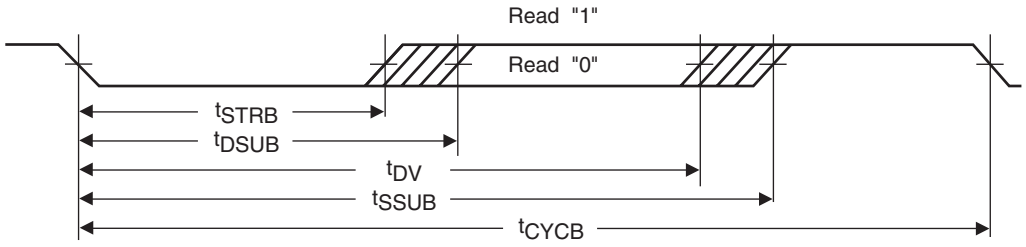


TD201803.eps

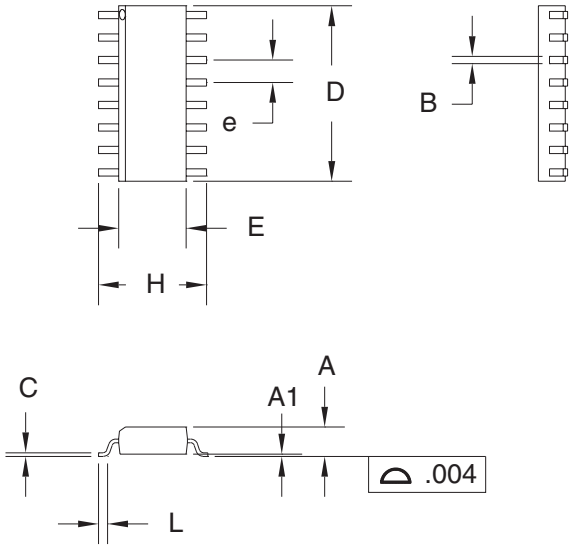
Host to bq2050H



bq2050H to Host



16-Pin SOIC Narrow (SN)



16-Pin SN (0.150" SOIC)

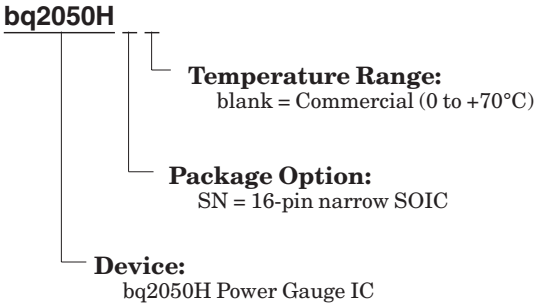
Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.385	0.400	9.78	10.16
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

Data Sheet Revision History

ChangeNo.	Page No.	Description of Change
1	All	"Final" changes from "Preliminary" version
2	8	Digital magnitude filter changed from 200µV to 250µV.
2	18	VSRQ changed from 200µV(min) to 250µV(min).
2	18	VSRD changed from -200µV(max) to -250µV(max).
3	3	Updated application diagram
3	12	Changed designation on appropriate locations from "R/W" to "R"
3	16	Clarified current scale register description
3	18	Changed V_{SRO} max. from +2000mV to +500mV
3	19	Changed V_{OL} max. from 0.5V to 0.3V
3	20	Changed t_{SSUB} max. from 95µs to 145µs

Notes: Change 1 = Aug. 1997 B changes from June 1996 "Preliminary."
Change 2 = June 1998 C changes from Aug. 1997 B.
Change 3 = May 1999 D changes from June 1998 C.

Ordering Information



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ2050HSN-A508	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2050H A508	Samples
BQ2050HSN-A508G4	ACTIVE	SOIC	D	16	40	TBD	Call TI	Call TI	0 to 70		Samples
BQ2050HSN-A508TR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2050H A508	Samples
BQ2050HSN-A508TRG4	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

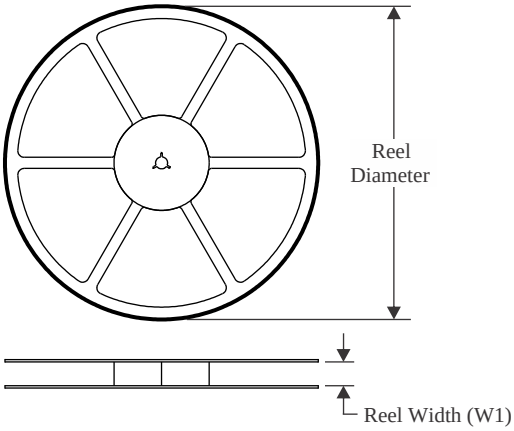
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

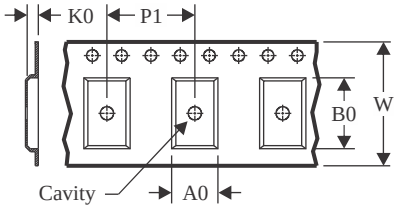
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

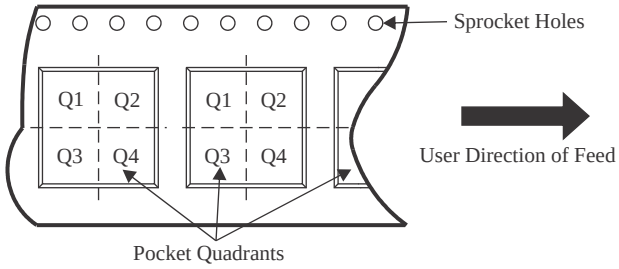


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

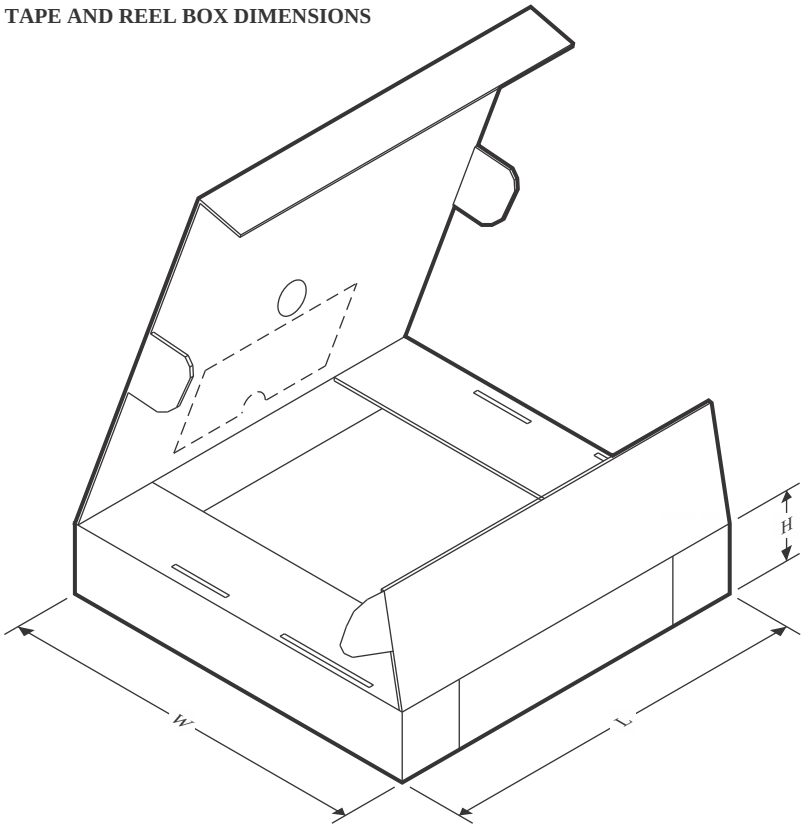
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2050HSN-A508TR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

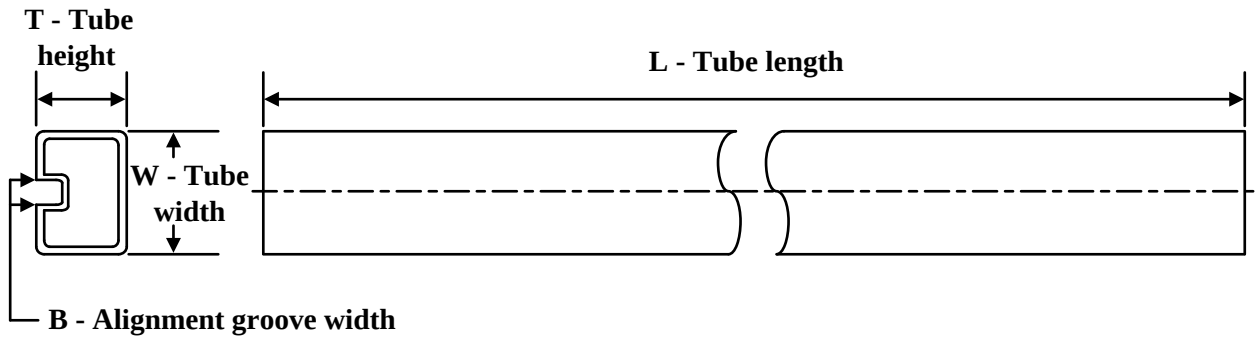
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2050HSN-A508TR	SOIC	D	16	2500	356.0	356.0	35.0

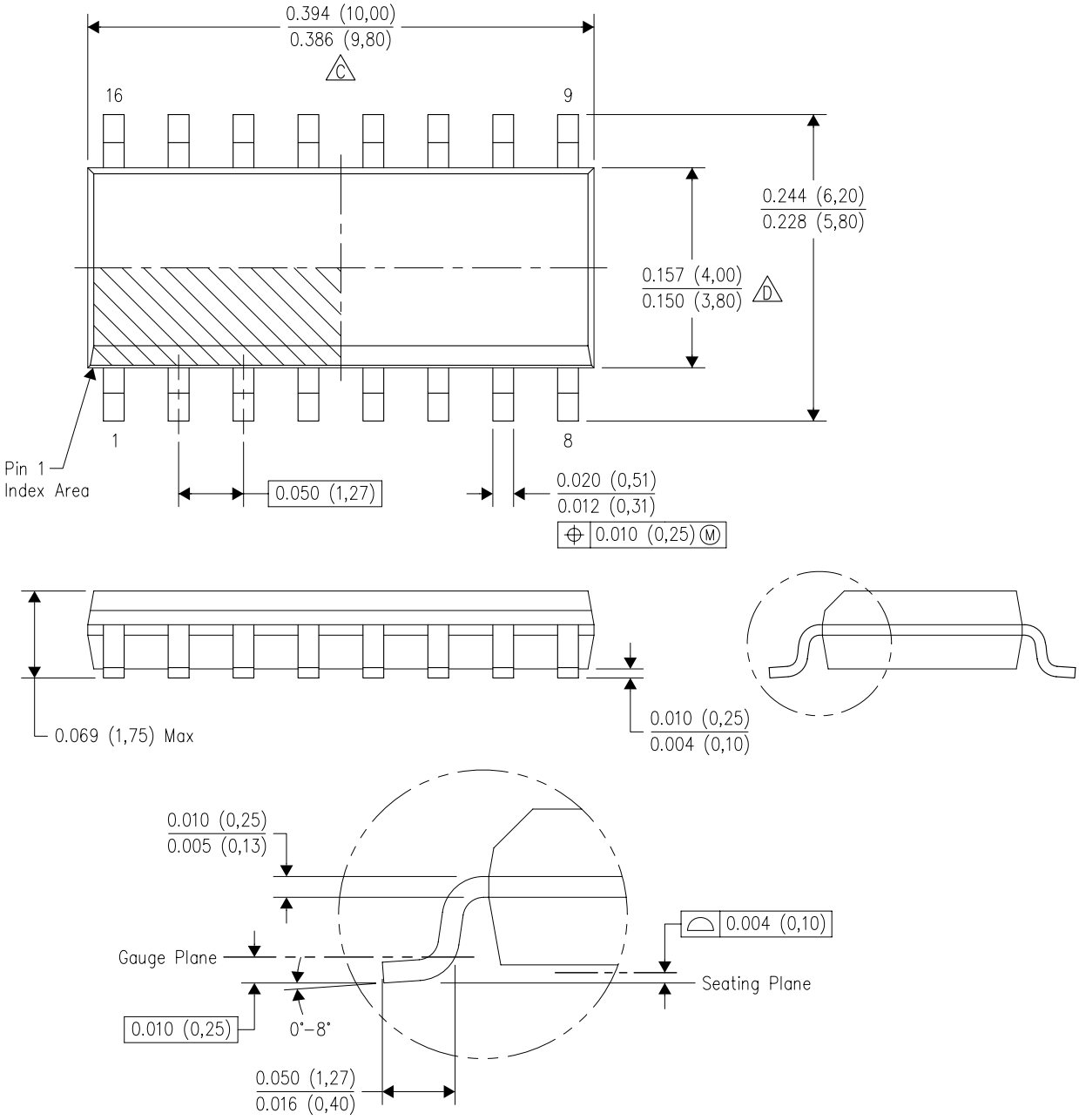
TUBE



*All dimensions are nominal

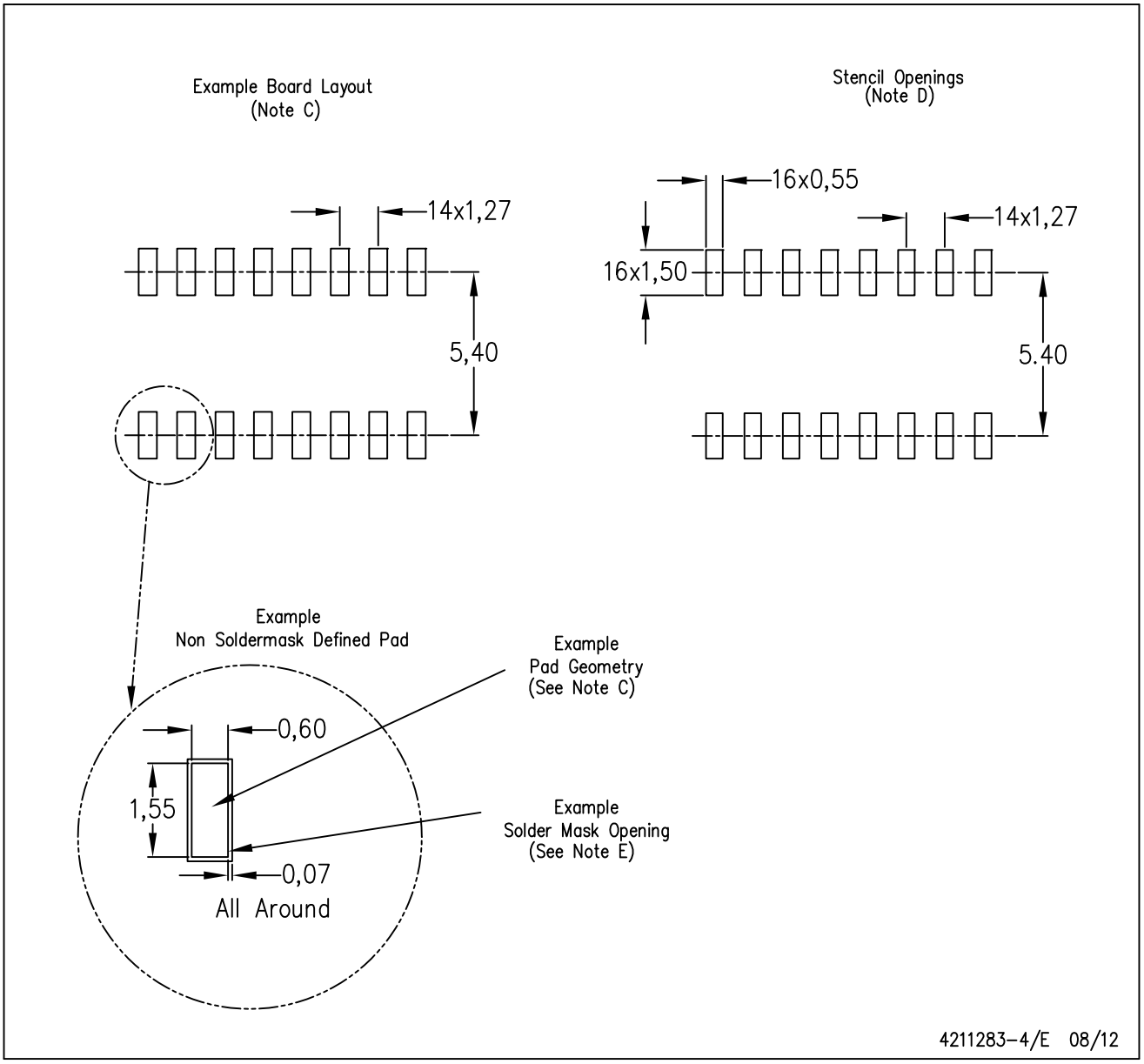
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ2050HSN-A508	D	SOIC	16	40	506.6	8	3940	4.32
BQ2050HSN-A508G4	D	SOIC	16	40	506.6	8	3940	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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