Application Report
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bq20z40/45/60/65 Printed-Circuit Board Layout Guide

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ABSTRACT

Attention to layout is critical to the success of any battery management circuit board. The mixture of high-current paths with an ultralow-current microcontroller creates the potential for design issues that can be challenging to solve. This application report presents guidelines to ensure a stable and well-performing project.

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1 Introduction

Attention to layout is critical to the success of any battery management circuit board. The mixture of high-current paths with an ultralow-current microcontroller creates the potential for design issues that are not always trivial to solve. Careful placement and routing with regard to the principles described in the following text can ensure success.

2 IC Orientation

The design of the pinouts has been improved to simplify the printed-circuit board layout. The recommended orientation of the two ICs is shown in Figure 1. With this technique, a board that required four layers with previous chipsets of bq20z80/bq29312 or bq208x/bq29312 can often be designed on only two layers.

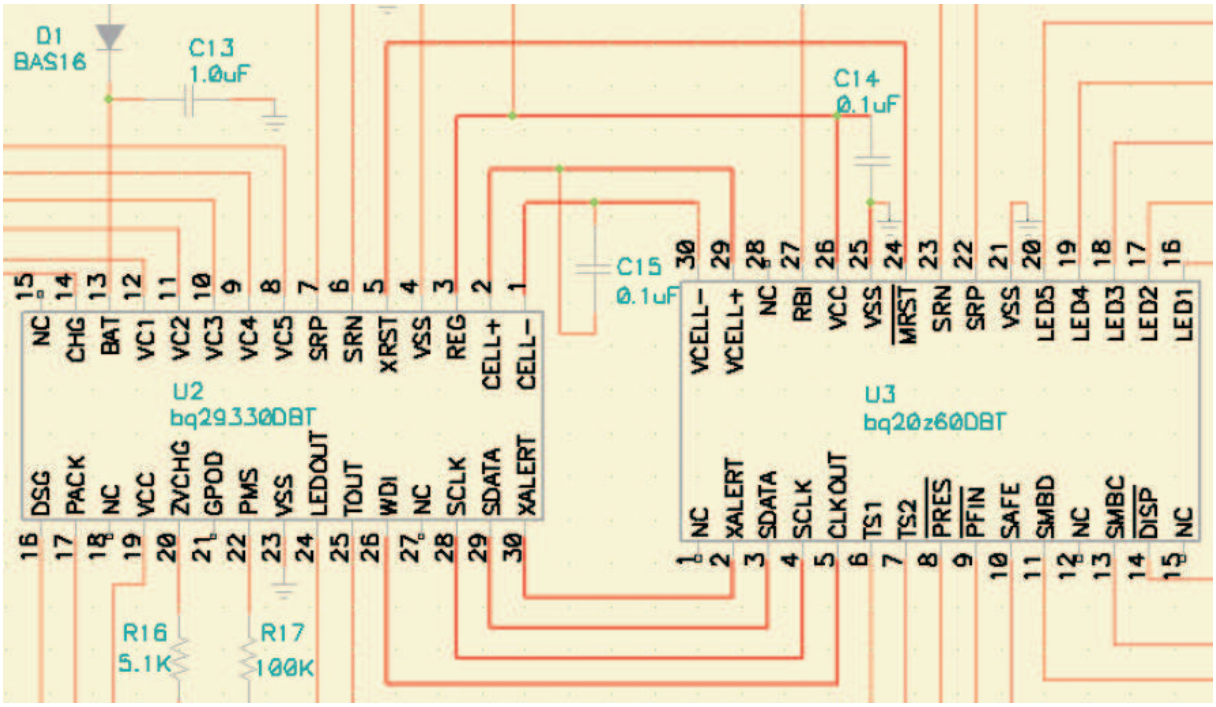

Figure 1. Orient the Chipset to Take Advantage of Easy Interconnection

3 bq20z40/45/60/65 Power Supply Decoupling Capacitor

Power supply decoupling from V_{CC} to ground is important for optimal operation of the bq20z40/45/60/65 advanced gas gauge. To keep the loop area small, place this capacitor next to the IC and use the shortest possible traces. A large-loop area renders the capacitor useless and forms a small-loop antenna for noise pickup.

Ideally, the traces on each side of the capacitor must be the same length and run in the same direction to avoid differential noise during ESD. If possible, place a via near the VSS pin to a ground plane layer.

Placement of the RBI capacitor is not as critical. It can be placed further away from the IC as shown in Figure 2.

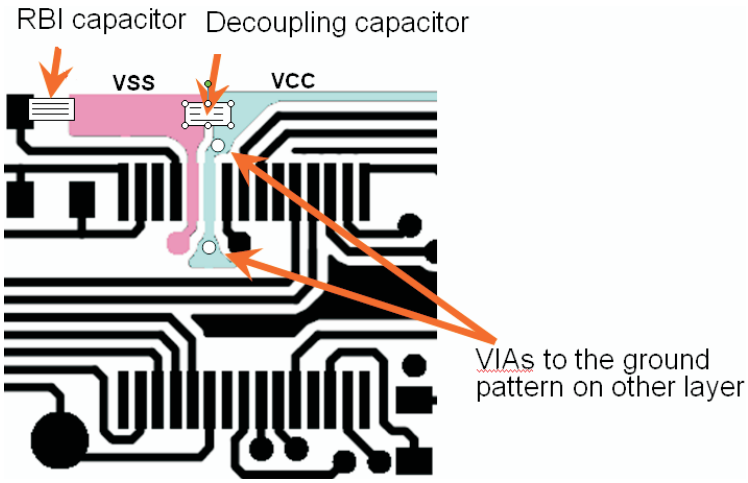

Figure 2. Recommended Placement of Decoupling and RBI Capacitors

4 bq29330 AFE Capacitors

Power supply decoupling for the bq29330 requires a pair of 1-µF ceramic capacitors from pin 13 (BAT) and pin 19 (VCC). These must be placed reasonably close to the IC, without using long traces back to VSS on pin 23.

The 3.3-V LED output requires a 4.7-µF ceramic capacitor when LEDs are used, but still requires 2.2-µF for loop stability when LEDs are not used, as with the bq20z40/45. This capacitor also must be placed as close as is practical to the IC.

The LDO voltage regulator within the bq29330 requires a 1-µF ceramic capacitor to be placed fairly close to the REG pin. This capacitor is for amplifier loop stabilization as well as an energy well for the 2.5-V supply.

Unwanted ESD hits to the AFE can have undesirable effects. Although the bq20z40/45/60/65 firmware has built-in routines to repair unwanted alteration of the internal registers, it is not easy to protect against an unwanted LDO shutdown, which would require application of the charger to restart the gas gauge. It has been experimentally determined that the placement of the capacitor on the REG pin can be helpful in diverting ESD current away from the AFE. The idea is to place the ground of the REG capacitor between the device ground and PACK(–) as shown in Figure 3. With this method, the capacitor absorbs an ESD hit to PACK plus, preventing unwanted LDO turnoff. The layout of Figure 4 is not recommended.

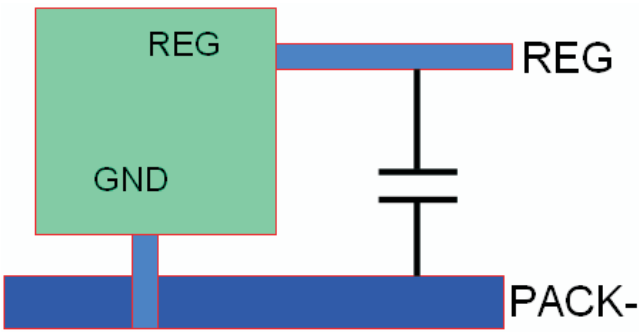

Figure 3. Preferred Method. Capacitor Absorbs Incoming ESD From PACK(–)

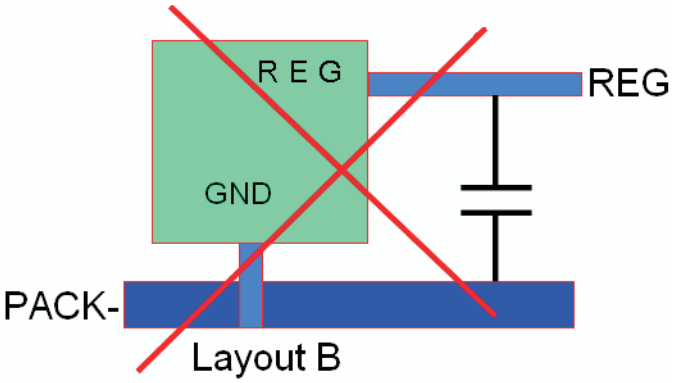

Figure 4. ESD From PACK– Can More Easily Affect Internal Registers

5 MRST Connection

The XRST (AFE) and MRST (GG) pins are connected to allow the AFE to control the gas gauge reset state. The connection between these pins must be as short as possible in order to avoid any incoming noise. With the recommended orientation of the two ICs, direct interconnection does not cause a problem. If unwanted resets are found, one or more of the following solutions may be effective:

- Add a 0.1-µF capacitor between MRST and ground.
- Provide a 1-kΩ pullup resistor to 2.5 V at MRST.
- Surround the entire circuit with a ground pattern.

Again, these steps are not normally required if the ICs are located close together. If a test pin is added at MRST, it must be provided with a 10-kΩ series resistor.

6 Communication Line Protection Components

The 5.6-V Zener diodes, used to protect the communication pins of the bq20z40/45/60/65 from ESD, must be located as close as possible to the pack connector. The grounded end of these Zener diodes must be returned to the PACK(–) node, rather than to the low-current digital ground system. This way, ESD is diverted away from the sensitive electronics as much as possible.

7 Protector FET Bypass and Pack Terminal Bypass Capacitors

The general principle is to use wide copper traces to lower the inductance of the bypass capacitor circuit. In Figure 5, an example layout demonstrates this technique.

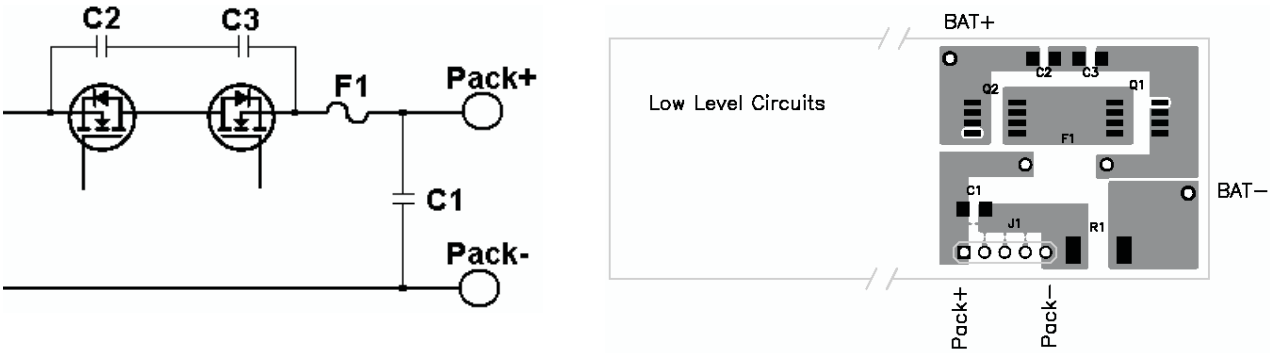

Figure 5. Use Wide Copper Traces to Lower the Inductance of Bypass Capacitors C1, C2, and C3

8 Ground System

The bq20z40/45/60/65 and bq29330 require a low-current ground system separate from the high-current PACK(-) path. ESD ground is defined along the high-current path from the PACK(–) terminal to the sense resistor. See the ground symbols in the bq20z40/45/60/65 reference design, and provide the separate low-current ground system accordingly. It is important that the low-current ground systems only connect to PACK(–) at the sense resistor Kelvin pick-off point as shown in Figure 6. The use of an optional inner layer ground plane is recommended for the low-current ground system.

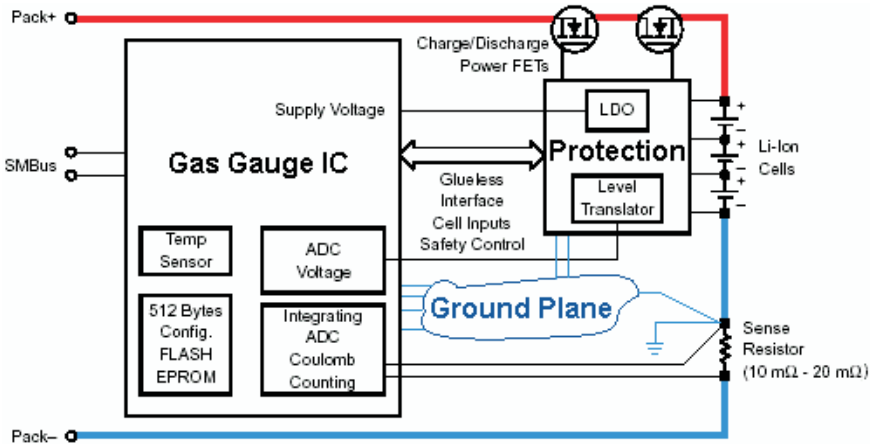

Figure 6. ICs Use a Low-Current Ground System. Ground Plane Is Optional.

9 Kelvin Connections

Kelvin voltage sensing is extremely important in order to accurately measure current and top and bottom cell voltages. Figure 7 and Figure 8 below demonstrate *correct* and *incorrect* techniques.

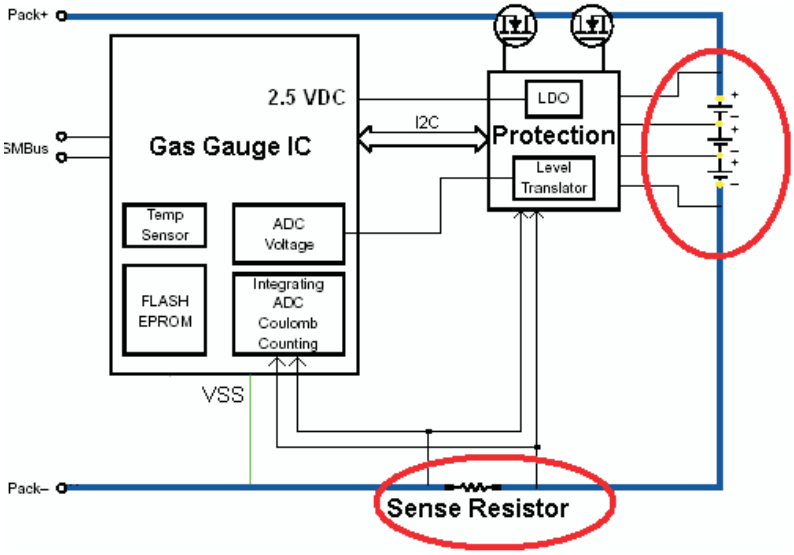

Figure 7. Incorrect: Sensing Through High-Current Copper Traces Produces Measurement Errors

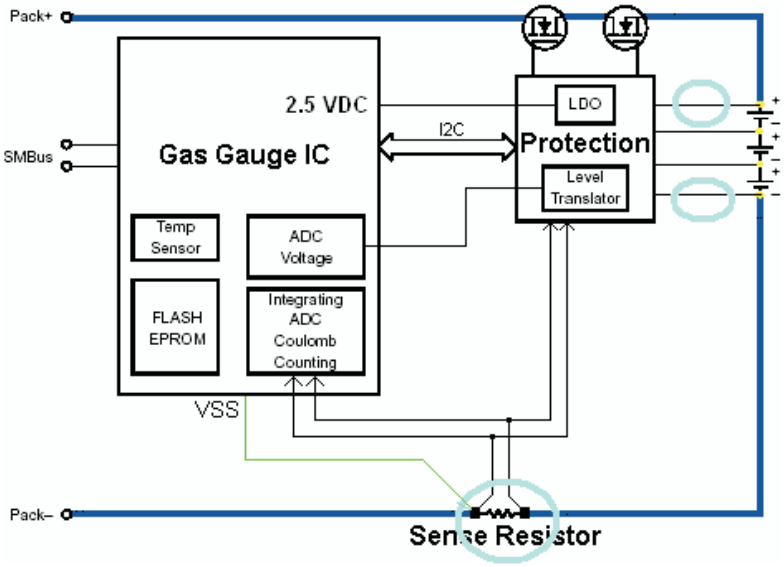

Figure 8. Correct: In Some Cases, Top and Bottom Cell Voltage Sensing May Be Extended Out to Cells

10 Board Offset Considerations

Although the most important component for board offset reduction is the decoupling capacitor for Vcc, additional benefit is possible by using this recommended pattern for the Coulomb Counter differential low-pass filter network. Maintain the symmetrical placement pattern shown for optimum current offset performance. Use symmetrical shielded differential traces, if possible, from the sense resistor to the 100-Ω resistors as shown in Figure 9.

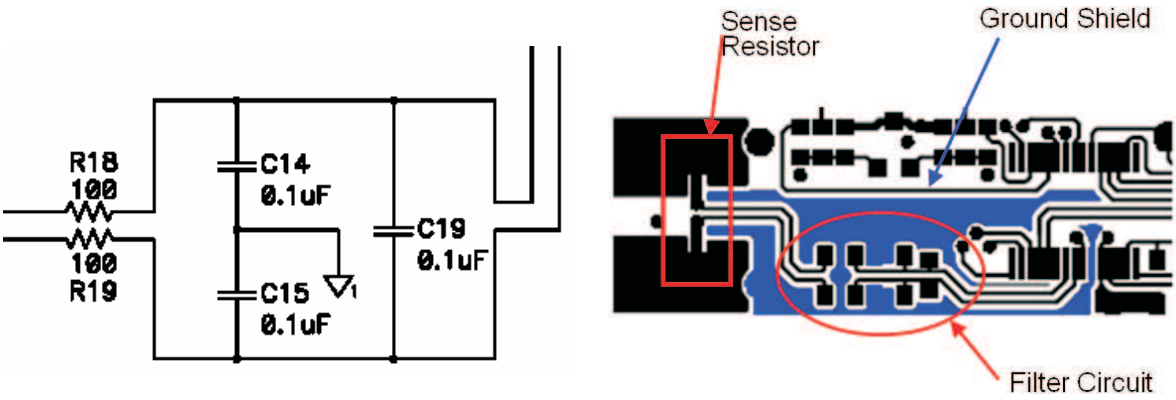

Figure 9. Differential Filter Components With Symmetrical Layout

11 ESD Spark Gap

Protect SMBus Clock, Data, and other communication lines from ESD with a spark gap at the connector. The following pattern is recommended, with 0,2-mm spacing between the points.

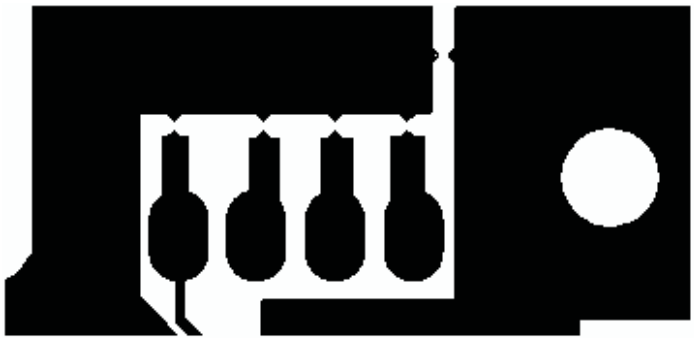

Figure 10. Recommended Spark-Gap Pattern Helps Protect Communication Lines From ESD.

12 Radio Frequency Interference

Normally, strong RF signals have no effect on gas gauge performance. However, understand that any silicon structure can rectify RF signals, producing unwanted voltages and currents at critical nodes. The most vulnerable node on the bq20z40/45/60/65 reference design is the SAFE output, which feeds into a signal diode, followed by an FET gate and shunt capacitor. This type of network demodulates an RF signal and can produce enough DC on the gate of the fuse ignition FET to actually blow the fuse. The solution is to keep the trace from the SAFE output to the diode as short as possible to reduce its effectiveness as an antenna. Alternately, both sides of the trace can be guarded with grounded copper.

13 Unwanted Magnetic Coupling

A battery fuel gauge circuit board is a challenging environment due to the fundamental incompatibility of high-current traces and ultralow-current semiconductor devices. The best way to protect against unwanted trace-to-trace coupling is with a component placement such as that shown in Figure 11, where the high-current section is on the opposite side of the board from the electronic devices. Clearly, this is not possible in many situations due to mechanical constraints. Still, every attempt must be made to route high-current traces away from signal traces, which enter the bq20z40/45/60/65 directly.

IC references and registers can be disturbed and in rare cases damaged due to magnetic and capacitive coupling from the high-current path. Note that during surge current and ESD events, the high-current traces appear inductive and can couple unwanted noise into sensitive nodes of the gas gauge electronics, as illustrated in Figure 12.

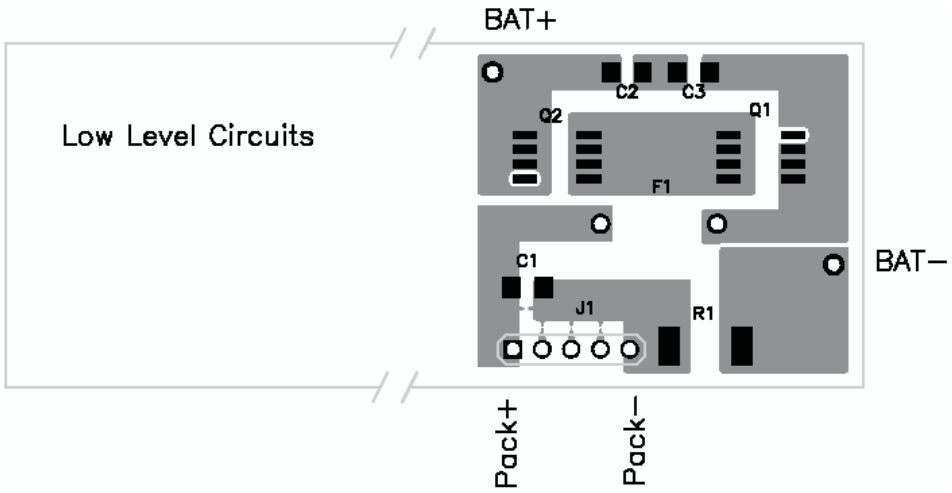

Figure 11. Separating High- and Low-Current Sections Provides an Advantage in Noise Immunity

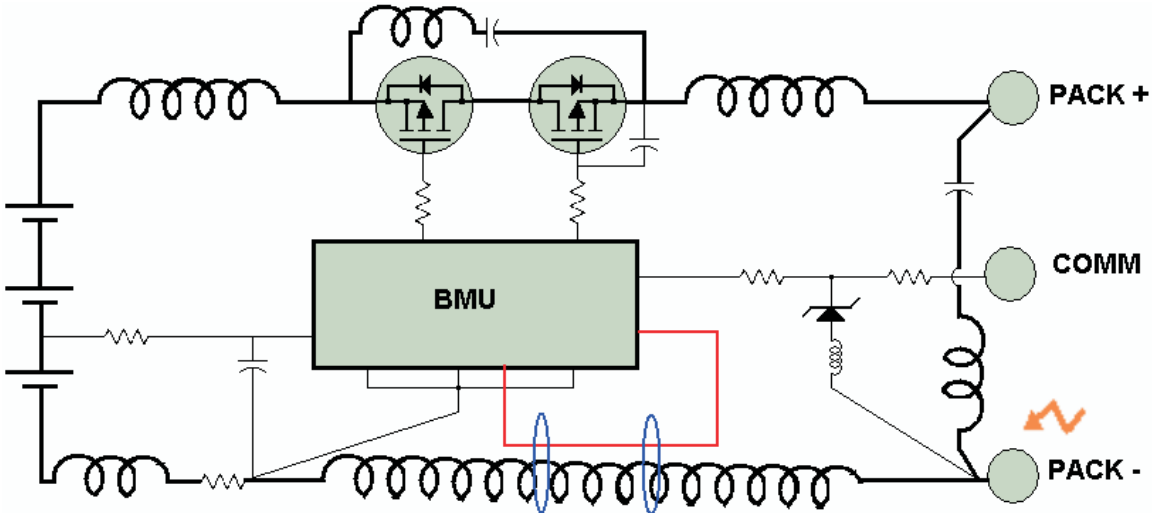

Figure 12. Avoid Close Spacing Between High-Current and Low-Level Signal Lines

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