

Configuring the bq20z80 Data Flash

Battery Management

ABSTRACT

The bq20z80 has numerous data flash constants that can be used to configure the device with a variety of different options for most features. The data flash of the bq20z80 is split into sections which are described in detail within this document.

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1 Glossary

ASOC: Absolute State of Charge

Bit: This word has a different meaning than Flag. This word is used to refer to a configuration setting bit. It is primarily used in data flash settings.

Blink, Flash and Delay: There are 3 different display modes for the LEDs in this document that need clarification.

- **Blinking:** When the display is said to be blinking, then the word “blinking” is used to refer to the LED located closest to the LED used to indicate 100% that is illuminated and “blinking” when the LED display is activated and displaying SOC (state of charge). Only this “topmost” activated LED in the display blinks. All other LEDs that are activated is steady state when activated. (see *LED Blink Rate*)
- **Flashing:** When the display is said to be flashing, then the word “flashing” means all LEDs that are activated to indicate the SOC will flash with a period of $(2 \times \text{LED Flash Rate})$.
- **Delay:** When the display is activate, all LEDs that are required to indicate the SOC may not illuminate at the same time. Starting from the LED that represents the lowest SOC, there can be a delay (*LED Delay*) between each LED illuminating from the LED that represents the lowest possible SOC up to the LED that represents the present SOC.

Cell Voltage(Max): This represents the maximum value among all the SBS cell voltage registers. (**Cell Voltage 1** through **Cell Voltage 4**)

Cell Voltage(Min): This represents the minimum value among all the SBS cell voltage registers. (**Cell Voltage 1** through **Cell Voltage 4**)

Cell Voltage(Any): This represents any of the possible SBS cell voltage registers. (**Cell Voltage 1** through **Cell Voltage 4**)

[DSG] in Battery Status: SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. This can be confused in many descriptions in this document because different functions require different methods for determining charging or discharging. The SBS description sometimes does not give enough resolution for correct part function so these functions require other data flash registers as described in their respective definitions. SBS states that if the battery is charging then [DSG] is 0, and any other time (Current less than or equal to 0), the [DSG] flag is set. The actual formula that the bq20z80 uses for setting or clearing the [DSG] flag are as follows:

[DSG] clear: [DSG]=0 if **Current** $\geq$ Chg Current Threshold

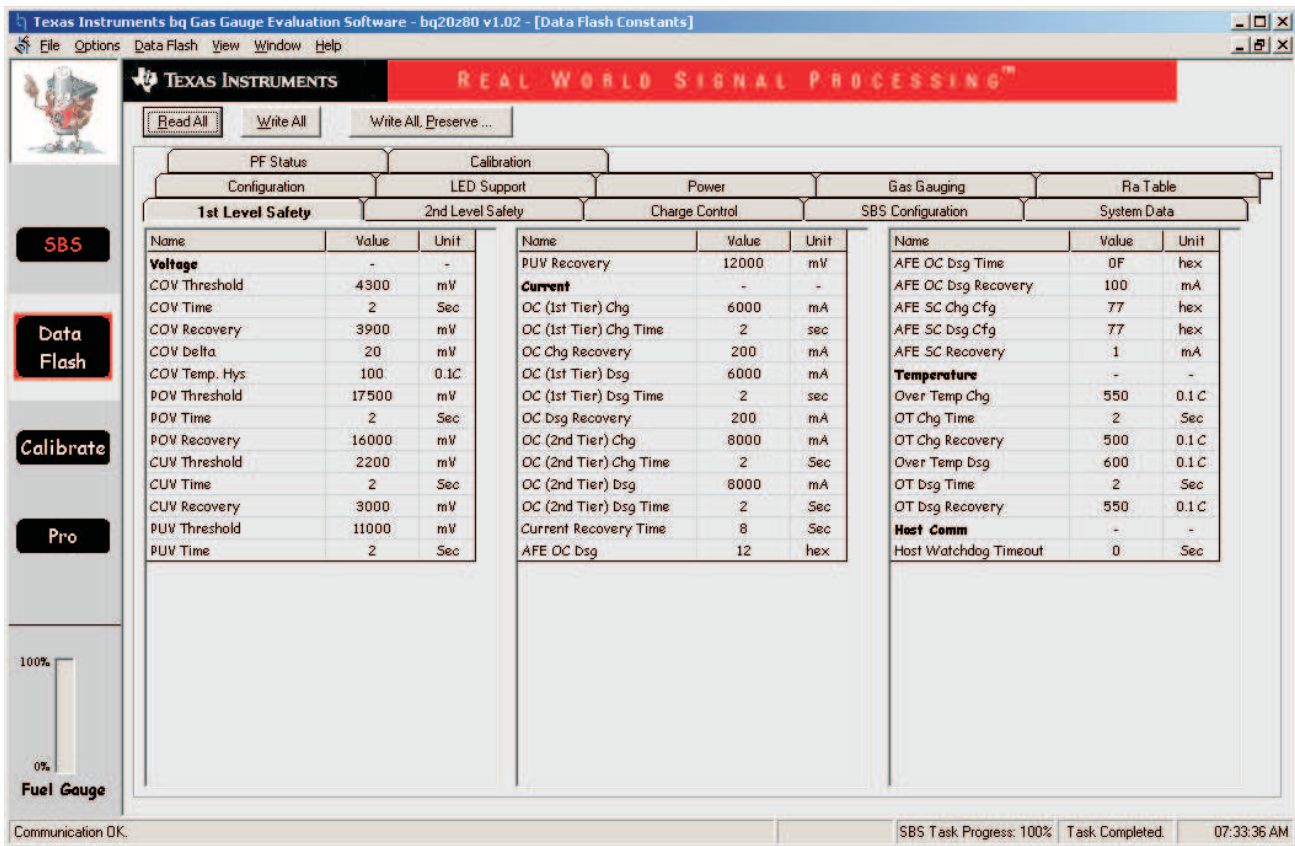
[DSG] set: [DSG]=1 if

1. Current $\leq$ Dsg Current Threshold or
2. Relaxation Mode which is defined by one of the following statements:
 - A) **Current** transitioning from below $(-)\text{Quit Current}$ to (above $(-)\text{Quit Current}$ and below *Quit Current*) for *Dsg Relax Time*
 - B) **Current** transitioning from above *Quit Current* to (below *Quit Current* and above $(-)\text{Quit Current}$) for *Chg Relax Time*

- FCC:** Full Charge Capacity
- FET opened/Closed:** It is common to say FET opened or FET closed. This is used throughout this document to mean the FET is turned off or the FET is turned on respectively.
- Flag:** This word is usually used to represent a read only status bit that indicates some action has occurred or is occurring. This bit usually cannot be modified by the user.
- Precharge/ZVCHG:** The words Precharge and ZVCHG are interchangeable throughout the document
- RCA:** Remaining Capacity Alarm
- RM:** Remaining Capacity
- RSOC:** Relative state of Charge
- RTA:** Remaining Time Alarm
- SAFE and SAFE:** These words are used throughout this document to represent 2 output pins on the bq20z80. SAFE is pin 7 on the bq20z80 and SAFE is pin 12. When this document discusses permanent failures, it normally includes a discussion of these two pins. When a permanent failure happens and its control bit is enabled, then these 2 pins are activated to either blow a fuse or to activate some hardware protection. The reason there are 2 outputs is for backwards compatibility with bq20z8X parts and to give options for an application. Both outputs are activated at the same time when enabled, but the SAFE pin is active low so it is driven low when activated while the SAFE pin is active high and is driven high when activated.
- SOC:** This is used as a generic meaning of State-of-Charge. It can mean RSOC, ASOC, or percentage of actual chemical capacity.
- System:** The word system is sometimes used in this document. It always means a host system that is consuming current from the battery pack that includes the bq20z80.
- Italics:*** All words in this document that are in italics represent names of data flash locations exactly as they are shown in the EV software.
- Bold Italics:***** All words that are bold italic represent SBS compliant registers exactly as they are shown in the EV software.
- [brackets]:** All words or letters in brackets represent bit/flag names exactly as they are shown in the SBS and Data Flash in the EV software.
- (-):** This is commonly used in this document to represent a minus sign. It is written this way to ensure that the sign is not lost in the translation of formulas in the text of this document.

2 1st Level Safety

All 1st Level Safety functions are temporary. There should be no permanent failures or damage to the battery if any of the 1st Level Safety functions are triggered.



2.1 Voltage

COV Threshold

When any cell voltage measured by **Cell Voltage (Any)** rises to this threshold, then the Cell Over Voltage (COV) protection process is triggered, initiating a [COV] in **Safety Alert** for **COV Time**. If the COV condition clears prior to the expiration of the **COV Time** timer, then [COV] in **Safety Alert** is cleared and no [COV] flag is set in **Safety Status**. If the COV condition does not clear, then [COV] is set in **Safety Status** and the Charge FET is opened. This fault condition causes [TCA] in **Battery Status** to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0. Setting **COV Time** to 0 completely disables this function.

Normal Setting: Default is 4300 mV. This cell is chemistry dependent, but 4200-4300 is the most common settings.

COV Time

See **COV Threshold**. This is a buffer time allotted for a COV condition. The timer starts after [COV] is set in **Safety Alert**. When it expires, then the bq20z80 forces [COV] set in **Safety Status** and opens the Charge FET. If the condition clears prior to the expiration of the **COV Time** timer, then the [COV] is cleared in **Safety Alert** and the **COV Time** timer resets without setting [COV] in **Safety Status**. Setting **COV Time** to 0 completely disables **COV Threshold**.

Normal Setting: This is normally set to 2 seconds, but depends on the application.

COV Recovery

When a [COV] is set in **Safety Status**, it is only cleared when **ALL** cell voltages as measured by **Cell Voltage(All)** fall below this threshold.

Normal Setting: This defaults to 3900 mV. It must be set low enough that the hysteresis between *COV Threshold* fault and this recovery prevents oscillation of the Charge FET.

COV Delta

The actual trigger value for the *COV Threshold* is adjusted down by this amount if **Temperature** rises above (*Over Temperature Threshold – COV Temp Hys*). The actual Data Flash location for *COV Threshold* is not modified, just the trigger value. It returns to normal if the temperature falls below (*Over Temperature Threshold – COV Temp Hys*). If this time is set to 0, then the *COV Threshold* trigger value is not modified based on the temperature.

Normal Setting: This value is normally set to 20 mV. This is application and cell chemistry dependent.

COV Temp Hys

See *COV Delta*. This is the delta temperature below the *Over Temperature Threshold* where the *COV Threshold* is modified by *COV Delta*.

Normal Setting: This value is normally set to 100 in 0.1°C. This is application and cell chemistry dependent.

POV Threshold

When the pack voltage measured by **Voltage** rises to this threshold, then the Pack Over Voltage (POV) protection process is triggered. This process starts by setting [POV] in **Safety Alert** for POV Time. If the POV condition clears prior to the expiration of the *POV Time* timer, then the [POV] is cleared in **Safety Alert** with no [POV] being set in **Safety Status**. If the POV condition does not clear, then [POV] is set in **Safety Status** and the Charge FET is opened. This fault condition causes [TCA] in **Battery Status** to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0. Setting *POV Time* to 0 completely disables this function.

Normal Setting: This register defaults to 17500 which is for a 4-cell pack. This is high, but it depends on the cell chemistry and the number of cells in series for an application. It is normally set to the (number of cells × 4300 mV). (i.e., 8600 mV for 2-cell applications, 12900 mV for 3-cell, and 17200 mV for 4-cell applications)

POV Time

See *POV Threshold*. This is a buffer time allotted for a POV condition. The timer starts after the [POV] is set in **Safety Alert**. When it expires, then the bq20z80 forces [POV] set in **Safety Status** and opens the Charge FET. If the condition clears prior to the expiration of the *POV Time* timer, then [POV] is cleared in **Safety Alert** and the *POV Time* timer resets. Setting *POV Time* to 0 completely disables *POV Threshold*.

Normal Setting: This is normally set to 2 seconds, but depends on the application.

POV Recovery

When [POV] is set in **Safety Status**, it is only cleared when the pack voltage measured by **Voltage** falls below this threshold.

Normal Setting: This defaults to 16000 mV. It must be set low enough that the hysteresis between *POV Threshold* fault and this recovery prevents oscillation of the Charge FET.

CUV Threshold

When any cell voltage measured by **Cell Voltage(Any)** falls below this threshold, then the Cell Under Voltage (CUV) protection process is triggered, initiating a [CUV] flag getting set in **Safety Alert** for *CUV Time*. If the CUV condition clears prior to the expiration of the *CUV Time* timer, then [CUV] is cleared in **Safety Alert** and no [CUV] is set in **Safety Status**. If the CUV condition does not clear, then a [CUV] is set in **Safety Status** and the Discharge FET is opened. This fault condition causes [TDA] and [FD] in **Battery Status** to be set. It also causes [XDSG] in **Operation Status**. Setting *CUV Time* to 0 completely disables this function.

Normal Setting: Default is 2200 mV. This is cell chemistry dependent but 2200 mV–2300 mV is the most common setting.

CUV Time

See *CUV Threshold*. This is a buffer time allotted for a CUV condition. The timer starts after [CUV] is set in **Safety Alert**. When it expires, then the bq20z80 forces [CUV] set in **Safety Status** and opens the Charge FET. If the condition clears prior to the expiration of the *CUV Time* timer, then [CUV] is cleared in **Safety Alert** and the *CUV Time* timer resets. Setting *CUV Time* to 0 completely disables *CUV Threshold*.

Normal Setting: This is normally set to 2 seconds but depends on the application.

CUV Recovery

When [CUV] is set in **Safety Status**, it is only cleared when **ALL** cell voltages as measured by **Cell Voltage(All)** rise above this threshold.

Normal Setting: The default for this register is 3000 mV. It must be set high enough that the hysteresis between *CUV Threshold* fault and this recovery prevents oscillation of the Discharge FET.

PUV Threshold

When the pack voltage measured by **Voltage** falls below this threshold, then the Pack Under Voltage (PUV) protection process is triggered, initiating a [PUVt] in **Safety Alert** for *PUV Time*. If the PUV condition clears prior to the expiration of the *PUV Time* timer, then [PUV] is cleared in **Safety Alert** and [PUV] are not set in **Safety Status**. If the PUV condition does not clear, then a [PUV] is set in **Safety Status** and the Discharge FET is opened. This fault condition causes [TDA] and [FD] in **Battery Status** to be set. It also causes [XDSG] in **Operation Status**. Setting *PUV Time* to 0 completely disables this function.

Normal Setting: This register defaults to 11000 which is for a 4-cell pack. This is very application and cell chemistry dependent. It also depends on the number of cells in series for an application. A very common setting is the (number of cells × 2750 mV). i.e., 5500 mV for 2-cell applications, 8250 mV for 3-cell, and 11000 mV for 4-cell applications)

PUV Time

See *PUV Threshold*. This is a buffer time allotted for a PUV condition. The timer starts after [PUV] is set in **Safety Alert**. When it expires, then the bq20z80 forces [PUV] set in **Safety Status** and opens the Discharge FET. If the condition clears prior to the expiration of the *PUV Time* timer, then [PUV] is cleared in **Safety Alert** and the *PUV Time* timer resets. Setting *PUV Time* to 0 completely disables *PUV Threshold*.

Normal Setting: This is normally set to 2 seconds but depends on the application.

PUV Recovery

When [POV] is set in **Safety Status**, it is only cleared when the pack voltage measured by **Voltage** falls below this threshold.

Normal Setting: The default for this register is 12000 mV. Set high enough that the hysteresis between *PUV Threshold* fault and this recovery prevents oscillation of the Discharge FET.

2.2 Current

There are 3 levels or tiers of current protection in the bq20z80. The first 2 levels, 1st Tier and 2nd Tier are slow responding (>1 second). The third level is a very quick responding current protection controlled directly by the bq29312A.

NOTE: IT is important that the bq29312A makes the triggering decision for any of the AFE fault conditions. This is to ensure quick response to dangerous faults. It is also designed in such a way that the AFE can act completely autonomously in the event of damage to the bq20z80 in the triggering of any AFE fault. The bq29312A cannot, however, clear the fault condition. It is cleared only by the bq20z80. The AFE data is transferred to the bq29312A on reset and (if enabled in the **AFE Verification** subclass) is continually monitored by the bq20z80 to ensure no corruption has occurred at any time. If corruption has occurred, the bq20z80 attempts to make corrections. If after repeated attempts (as set in the **AFE Verification** subclass), it cannot correct the condition, then it sets a permanent failure. If enabled in *Permanent Fail Cfg*, then the SAFE pin is driven high and **SAFE** pin is driven low on the bq20z80. (See *Permanent Fail Cfg*)

OC (1st Tier) Chg

When current measured by **Current** reaches up to or above this threshold during charging, then the 1st Tier Over Current in the Charge [OCC] protection process is triggered, initiating an [OCC] in **Safety Alert** for OC (1st Tier) Chg Time in seconds. If the 1st Tier OCC condition clears prior to the expiration of the OC (1st Tier) Chg Time timer, then [OCC] in **Safety Alert** is cleared and no [OCC] is set in **Safety Status**. If the 1st Tier OCC condition does not clear, then a [OCC] is set in **Safety Status** and the Charge FET is opened. This fault condition causes [TCA] in **Battery Status** to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0. Setting the OC (1st Tier) Chg Time to 0 completely disables this function.

Normal Setting: This register is application dependent. It should be set above the absolute maximum expected discharge current. It should be set high enough that unexpected mild charge spikes or inaccuracies do not create a false over current trigger, but low enough to force the Charge FET to open before damage occurs to the pack.

OC (1st Tier) Chg Time

See OC(1st Tier) Chg. This is a buffer time allotted for a 1st tier Over Current condition. The timer starts every time the [OCC] in **Safety Alert** is initially set. When the timer expires, then the bq20z80 forces an [OCC] in **Safety Status** and opens the Charge FET. If [OCC] in **Safety Alert** clears prior to the expiration of the OC (1st Tier) Chg Time timer, then [OCC] in **Safety Alert** is cleared and the OC (1st Tier) Chg Time timer resets. Setting the OC (1st Tier) Chg Time to 0 disables OC (1st Tier) Chg .

Normal Setting: This is normally set to 2 seconds, but depends on the application. It must be set long enough to prevent false triggering of the [OCC] in **Safety Status**, but short enough to prevent damage to the battery pack.

OC Chg Recovery

OC Chg Recovery is one of several recovery methods used for both 1st and 2nd level Over Current in the charge direction faults. This value is used for either nonremovable packs ([NR] in *Operation Cfg B* =1) or for removable packs configured ([OCC] in *Non-Removable Cfg*). With either of these settings, **Average Current** must fall below this value for *Current Recovery Timer* in seconds to clear the [OCC] or the [OCC2] in **Safety Status** if either is set.

Normal Setting: This register is application dependent, but is normally set low enough that it prevents quick oscillation in the Charge FET. **Average Current** is used for this recovery function and falls every second that it is recomputed with **Current** at or near 0. If this recovery is set too high, then the Charge FET can oscillate with a frequency that is fast enough to cause damage to the battery pack because the **Average Current** falls below this value quickly.

OC (1st Tier) Dsg

When current measured by **Current** falls down to or below this threshold during discharging then the 1st Tier Over Current in discharge (OCD) protection process is triggered, initiating an [OCD] in **Safety Alert** for OC (1st Tier) Dsg Time in seconds. If the 1st Tier OCD condition clears prior to the expiration of the OC (1st Tier) Dsg Time timer, then the [OCD] is cleared and no [OCD] is set. If the 1st Tier OCD condition does not clear, then a [OCD] is set in **Safety Status** and the Discharge FET is opened. This fault condition causes [XD SG] and [XD SG I] in **Operation Status** to be set. It also causes **Charging Current** to be set to 0.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent. It should be set **below** the absolute maximum expected discharge current. It must be set low enough that unexpected mild discharge spikes or inaccuracies do not create a false over current trigger, but high enough to force the Discharge FET open before damage occurs to the pack.

OC (1st Tier) Time Dsg

See OC(1st Tier) Dsg. This is a buffer time allotted for a 1st tier Over Current in the discharge direction condition. The timer starts every time [OCD] in **Safety Alert** is initially set. When the timer expires, the bq20z80 forces an [OCD] Alarm in **Safety Status** and opens the Discharge FET. If [OCD] in **Safety Alert** clears prior to the expiration of the OC (1st Tier) Time Dsg timer, then the [OCD] in **Safety Alert** is cleared and the OC (1st Tier) Time Dsg timer resets. Setting the OC (1st Tier) Time Dsg to 0 disables OC (1st Tier) Dsg.

Normal Setting: This is normally set to 2 seconds, but depends on the application. It should be set long enough to prevent false triggering of the [OCD] in *Safety Status*, but short enough to prevent damage to the battery pack.

OC Dsg Recovery

OC Dsg Recovery is one of several recovery methods used for both 1st and 2nd level Over Current in the discharge direction Faults. This value is used for either nonremovable packs ([NR] in *Operation Cfg B = 1*) or for removable packs configured ([OCD] in *Non-Removable Cfg*). With either of these settings, **Average Current** must rise **above** this value for *Current Recovery Timer* in seconds to clear the [OCD] or the [OCD2] in *Safety Status* if either is set.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent but is normally set **high** enough that it prevents quick oscillation in the Discharge FET. **Average Current** is used for this recovery function and moves closer to 0 every second that it is recomputed with *Current* at or near 0. If this recovery is set too *low*, then the Discharge FET can oscillate with a frequency that is fast enough to cause damage to the battery pack because the **Average Current** moves **above** this value quickly.

OC (2nd Tier) Chg

When current measured by **Current** reaches up to or above this threshold during charging then the 2nd Tier Over Current in Charge [OCC2] protection process is triggered, initiating an [OCC2] in *Safety Alert* for OC (2nd Tier) Chg Time in seconds. If the 2nd Tier Over Current condition clears prior to the expiration of the OC (2nd Tier) Chg Time timer, then [OCC2] in *Safety Alert* is cleared and no [OCC2] is set in *Safety Status*. If the 2nd Tier Over Current condition does not clear, then a [OCC2] is set in *Safety Status* and the Charge FET is opened. This fault condition causes [TCA] in *Battery Status* to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0. **Normal Setting:** This register is application dependent. It should be set above the OC (1st Tier) Chg threshold and should be set high enough that unexpected mild charge spikes or inaccuracies do not create a false over current trigger, but low enough to force the Charge FET to open before damage occurs to the pack.

Normal Setting: This register is application dependent. It should be set above the OC (1st Tier) Chg threshold and should be set high enough that unexpected mild charge spikes or inaccuracies do not create a false over current trigger, but low enough to force the Charge FET to open before damage occurs to the pack.

OC (2nd Tier) Time Chg

See OC(2nd Tier) Chg. This is a buffer time allotted for a 2nd Tier Over Current condition. The timer starts every time the [OCC2] in *Safety Alert* is initially set. When the timer expires then, the bq20z80 forces an [OCC2] in *Safety Status* and opens the Charge FET. If [OCC2] in *Safety Alert* clears prior to the expiration of the OC (2nd Tier) Chg Time timer, then [OCC2] in *Safety Alert* is cleared and the OC (2nd Tier) Chg Time timer resets. Setting the OC (2nd Tier) Chg Time to 0 disables OC (2nd Tier) Chg.

Normal Setting: This is normally set to 2 seconds, but depends on the application. It must be set long enough to prevent false triggering of the [OCC2] in *Safety Status*, but short enough to prevent damage to the battery pack. It is common for the second level over current threshold to be disabled.

OC (2nd Tier) Dsg

When current measured by **Current** falls down to or below this threshold during discharging, then the 2nd Tier Over Current in discharge (OCD2) protection process is triggered, initiating an [OCD2] in **Safety Alert** for OC (2nd Tier) Dsg Time in seconds. If the 2nd Tier OCD2 condition clears prior to the expiration of the OC (2nd Tier) Dsg Time timer, then the [OCD2] is cleared in **Safety Alert** and no [OCD2] alarm is set in **Safety Status**. If the 2nd Tier OCD condition does not clear, then a [OCD2] is set in **Safety Status** and the Discharge FET is opened. This fault condition causes [XDSG] and [XDSGI] in **Operation Status** to be set. It also causes **Charging Current** to be set to 0.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent. It should be set **below** the OC (1st Tier) Dsg threshold and must be set **below** the absolute maximum expected discharge current. It must be set **low** enough that unexpected mild discharge spikes or inaccuracies do not create a false over current trigger, but **high** enough to force the Discharge FET open before damage occurs to the pack.

OC (2nd Tier) Time Dsg

See OC (2nd Tier) Dsg. This is a buffer time allotted for a 2nd Tier Over Current in the discharge direction condition. The timer starts every time [OCD2] in **Safety Alert** is initially set. When the timer expires, then the bq20z80 forces an [OCD2] alarm in **Safety Status** and opens the Discharge FET. If [OCD2] in **Safety Alert** clears prior to the expiration of the OC (2nd Tier) Time Dsg timer, then the [OCD] in **Safety Alert** is cleared and the OC (2nd Tier) Time Dsg timer resets. Setting the OC (2nd Tier) Time Dsg to 0 disables OC (2nd Tier) Dsg.

Normal Setting: This is normally set to 2 seconds but depends on the application. It must be set long enough to prevent false triggering of the [OCD2] in **Safety Status** but short enough to prevent damage to the battery pack.

Current Recovery Timer

The **Current Recovery Timer** is used in the recovery process of any of the over current fault conditions. After a fault condition exists, depending on if enabled, the fault condition is cleared only after **Current Recovery Timer** time in seconds with **AverageCurrent** falling below the corresponding recovery threshold in the charge direction or rising above the corresponding recovery threshold in the discharge direction. The corresponding recovery does not happen immediately after the recovery condition exists. As soon as the recovery condition exists then the **Current Recovery Timer** starts and the condition clears and the corresponding FET is enabled after the **Current Recovery Timer** expires. This timer is associated with the following Fault Conditions as described in this section:

1. OC (1st Tier) Dsg
2. OC (1st Tier) Chg
3. OC (2nd Tier) Dsg
4. OC (2nd Tier) Chg
5. AFE OC Dsg
6. AFE SC Dsg
7. AFE SC Chg

This Recovery method is enabled if [NR] is set in **Operation Cfg B**, or if ([NR] is cleared and the corresponding bits are set in the **Non-Removable Cfg** register:

- | | |
|----------------------------------|--------|
| 1. OC (1 st Tier) Dsg | [OCD] |
| 2. OC (1 st Tier) Chg | [OCC] |
| 3. OC (2 nd Tier) Dsg | [OCD2] |
| 4. OC (2 nd Tier) Chg | [OCC2] |
| 5. AFE OC Dsg | [AOCD] |
| 6. AFE SC Dsg | [SCD] |
| 7. AFE SC Chg | [SCC] |

Normal Setting: The default for this register is 8 seconds. This is a recommended number to prevent heating up in the corresponding FET.

AFE OC Dsg

See the important note about all AFE fault conditions at the beginning of the **Current** section.

This is the third level Over Current protection in the discharge direction. This is a last effort protection function before using the Permanent Fail Functions in the Second Level Safety Class. This register displays in HEX using the EV Software. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If the *AFE OC Dsg* condition exists for *AFE OC Dsg Time* in milliseconds, then the discharge FET opens as controlled by the bq29312A. This fault condition causes [AOCD] to be set in **Safety Status** and [XDSG], [XDSGI] is set in *Operation Status*, and [TDA] is set in **Battery Status**. It also causes **Charging Current** to be set to 0. See [Table 1](#) for settings for this register.

Table 1. AFE OC Dsg Configuration

0x00	0.050 V	0x08	0.090 V	0x10	0.130 V	0x18	0.170 V
0x01	0.055 V	0x09	0.095 V	0x11	0.135 V	0x19	0.175 V
0x02	0.060 V	0x0a	0.100 V	0x12	0.140 V	0x1a	0.180 V
0x03	0.065 V	0x0b	0.105 V	0x13	0.145 V	0x1b	0.185 V
0x04	0.070 V	0x0c	0.110 V	0x14	0.150 V	0x1c	0.190 V
0x05	0.075 V	0x0d	0.115 V	0x15	0.155 V	0x1d	0.195 V
0x06	0.080 V	0x0e	0.120 V	0x16	0.160 V	0x1e	0.200 V
0x07	0.085 V	0x0f	0.125 V	0x17	0.165 V	0x1f	0.205 V

Normal Setting: Note that the maximum value for this register is 0x1F. Values above 0x1F cause unpredictable results. This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required in determining the proper setting for this register. Be sure that this value is **below** the OC (2nd Tier) Dsg.

AFE OC Dsg Time

This is the time after detection of an *AFE OC Dsg* fault before the Discharge FET attempts to open. This trigger function is completely controlled by the bq29312A. The setting of this register is in HEX, and it is in milliseconds (See *AFE OC Dsg*). See [Table 2](#) for setting for this register.

Table 2. AFE OC Dsg Time Configuration

0x00	1 ms	0x04	9 ms	0x08	17 ms	0x0c	25 ms
0x01	3 ms	0x05	11 ms	0x09	19 ms	0x0d	27 ms
0x02	5 ms	0x06	13 ms	0x0a	21 ms	0x0e	29 ms
0x03	7 ms	0x07	15 ms	0x0b	23 ms	0x0f	31 ms

Normal Setting: Note that the maximum value for this register is 0x0F. Values above 0x0F cause unpredictable results. This register is completely application specific. It should be set long enough to prevent false triggering of the [AOCD] in **Safety Status**, but short enough to prevent damage to the battery pack.

AFE OC Dsg Recovery

See the important note about all AFE fault conditions at the beginning of the **Current** section.

AFE OC Dsg Recovery is one of several recovery methods used for *AFE OC Dsg Fault*. This value is used for either nonremovable packs ([NR] in *Operation Cfg B* =1) or for removable packs configured ([AOCD] in *Non-Removable Cfg*). With either of these settings, **AverageCurrent** must rise **above** this value for *Current Recovery Timer* in seconds to clear the [AOCD] in **Safety Status** if it is set.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent, but is normally set **high** enough that it prevents quick oscillation in the Discharge FET. If set to **low**, then the Discharge FET can oscillate with a frequency that is fast enough to still cause damage to the battery pack because the **AverageCurrent** moves **above** this value quickly.

AFE SC Chg Cfg

See the **NOTE** at the beginning of the Current section for an important note about all AFE fault conditions.

This register includes 2 settings. We will refer to these as *AFE SC Chg* and *AFE SC Chg Time*. This register displays in HEX using the EV Software. The most significant nibble (bits 4-7) sets the time for the AFE short circuit in the Charge direction fault detection time (*AFE SC Chg Time*). The least significant nibble (bits 0-3) set the threshold at which the bq29312A detects a AFE short circuit fault (*AFE SC Chg*). This is an extreme condition with settings for very large voltages and very short setting times for violent faults far above any of the other fault conditions because its intended purpose is to detect a short circuit condition before damage to the battery pack can occur. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If an AFE short circuit in the Charge direction fault exists for AFE short circuit in the Charge direction fault detection time in microseconds, then the Charge FET opens as controlled by the bq29312A. This fault condition causes [SCC] to be set in **Safety Status**, and [TCA] to be set in **Battery Status**. It also causes **Charging Current** and **Charging Voltage** to be set to 0. See [Table 4](#) for settings for this register.

Table 3. AFE SC Chg Cfg Bit Description

7	6	5	4	3	2	1	0
SCCT3	SCCT2	SCCT1	SCCT0	SCCV3	SCCV2	SCCV1	SCCV0
<i>AFE SC Chg Time</i>				<i>AFE SC Chg</i>			

Table 4. AFE SC Chg Cfg Least Significant Nibble (SCCV3-SCCV0)

0x00	0.100 V	0x04	0.200 V	0x08	0.300 V	0x0c	0.400 V
0x01	0.125 V	0x05	0.225 V	0x09	0.325 V	0x0d	0.425 V
0x02	0.150 V	0x06	0.250 V	0x0a	0.350 V	0x0e	0.450 V
0x03	0.175 V	0x07	0.275 V	0x0b	0.375 V	0x0f	0.475 V

Table 5. AFE SC Chg Cfg Most Significant Nibble (SCCT3-SCCT0)

0x00	0 μ s	0x04	244 μ s	0x08	488 μ s	0x0c	732 μ s
0x01	61 μ s	0x05	305 μ s	0x09	549 μ s	0x0d	793 μ s
0x02	122 μ s	0x06	366 μ s	0x0a	610 μ s	0x0e	854 μ s
0x03	183 μ s	0x07	427 μ s	0x0b	671 μ s	0x0f	915 μ s

Normal Setting: This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required in determining the proper setting for this register. Be sure that this value is sufficiently above OC (2nd Tier) Chg.

AFE SC Dsg Config

See the important note about all AFE fault conditions at the beginning of the **Current** section.

This register includes 2 settings. Refer to these as *AFE SC Dsg* and *AFE SC Dsg Time*. This register displays in HEX using the EV Software. The most significant nibble (bits 4–7) sets the time for the AFE short circuit in the discharge direction fault detection time (*AFE SC Dsg Time*). The least significant nibble (bits 0–3) sets the threshold at which the bq29312A detects an AFE short circuit fault in the discharge direction (*AFE SC Dsg*). This is an extreme condition with settings for large voltages and short setting times for violent faults far above any of the other fault conditions because its intended purpose is to detect a short circuit condition before damage to the battery pack can occur. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If an AFE short circuit in the Charge direction fault exists for AFE short circuit in the Charge direction fault detection time in microseconds, then the Discharge FET opens as controlled by the bq29312A. This fault condition causes [SCD] to be set in **Safety Status**, [XD SG] and [XD SG I] to be set in **Operation Status**, and [TDA] to be set in **Battery Status**. See [Table 7](#) and [Table 8](#) for settings for this register.

Table 6. AFE SC Dsg Cfg Bit Description

7	6	5	4	3	2	1	0
SCDT3	SCDT2	SCDT1	SCDT0	SCDV3	SCDV2	SCDV1	SCDV0
AFE SC Dsg Time				AFE SC Dsg			

Table 7. AFE SC Dsg Cfg Least Significant Nibble (SCDV3-SCDV0)

0x00	0.10 V	0x04	0.20 V	0x08	0.30 V	0x0c	0.40 V
0x01	0.125 V	0x05	0.225 V	0x09	0.325 V	0x0d	0.425 V
0x02	0.150 V	0x06	0.250 V	0x0a	0.350 V	0x0e	0.450 V
0x03	0.175 V	0x07	0.275 V	0x0b	0.375 V	0x0f	0.475 V

Table 8. AFE SC Dsg Cfg Most Significant Nibble (SCDT3-SCDT0)

0x00	0 μs	0x04	244 μs	0x08	488 μs	0x0c	732 μs
0x01	61 μs	0x05	305 μs	0x09	549 μs	0x0d	793 μs
0x02	122 μs	0x06	366 μs	0x0a	610 μs	0x0e	854 μs
0x03	183 μs	0x07	427 μs	0x0b	671 μs	0x0f	915 μs

Normal Setting: This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required to determine the proper setting for this register. Be sure that this value is **below** AFE OC Dsg.

AFE SC Recovery

See the important note about all AFE fault conditions at the beginning of the **Current** section.

AFE SC Recovery is one of several recovery methods used for either a charge or discharge AFE short circuit fault. This value is used for either nonremovable packs ([NR] in *Operation Cfg B = 1*) or for removable packs that this function is configured ([SCD] for discharge or [SCC] in charge in *Non-Removable Cfg*). With either of these settings, *AverageCurrent* must rise **above** this value (for discharge fault) or **below** this value (for charge fault) for *Current Recovery Timer* in seconds to clear the [SCD] or [SCC] in *Safety Status* if either is set.

Normal Setting: Care must be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent, but is normally set close to 0 mA to prevent quick oscillation in the Charge/Discharge FET. If it is set to far from 0 mA, then the Charge/Discharge FET oscillates with a frequency that is fast enough to cause damage to the battery pack because the *AverageCurrent* is within this threshold value too quickly.

2.3 Temperature

Over Temp Chg

When the pack temperature measured by **Temperature** rises to or above this threshold while charging (**Current** > *Chg Current Threshold*), then the Over Temperature in charge direction (OTC) protection process is triggered and [OTC] is set in **Safety Alert** for *OT Chg Time*. If the OTC condition clears prior to the expiration of the *OT Chg Time* timer, then the [OTC] is cleared in **Safety Alert** and no [OTC] is set in **Safety Status**. If the condition does not clear, then [OTC] is set in **Safety Status** and if [OTFET] is set in *Operation Cfg B* the Charge FET is opened. If [OTFET] is not set in *Operation Cfg B*, then the Charge FET is not opened by this fault. This fault condition causes [TCA] and [OTA] in **Battery Status** to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0.

Normal Setting: This setting depends on the environment temperature and the battery specification. Verify the battery specification allows temperatures up to this setting while charging and verify these setting are sufficient for the application temperature. The default is 55°C which should be sufficient for most Li-Ion applications.

OT Chg Time

See *Over Temp Chg*. This is a buffer time allotted for Over Temperature in the charge direction condition. The timer starts every time the [OTC] in **Safety Alert** is initially set. When the timer expires, the bq20z80 forces an [OTC] in **Safety Status** and opens the Charge FET if enabled with [OTFET] in *Operation Cfg B*. If [OTC] in **Safety Alert** clears (fault condition clears) prior to the expiration of the *OT Chg Time* timer, then [OTC] in **Safety Alert** is cleared and the *OT Chg Time* timer resets. Setting the *OT Chg Time* to 0 disables this function.

Normal Setting: This is normally set to 2 seconds which should be sufficient for most applications. Temperature is normally a slow acting condition that does not need high speed triggering. It must be set long enough to prevent false triggering of the [OTC] in **Safety Status**, but short enough to prevent damage to the battery pack.

OT Chg Recovery

OT Chg Recovery is the temperature at which the battery recovers from an *OT Temp Chg* fault. This is the only recovery method for an *OT Temp Chg* fault.

Normal Setting: This register is application dependent, but is normally set low enough below the fault condition temperature to prevent quick oscillation in the Charge FET if it was opened with the fault. The default is 50°C which is a 5 degree difference which is sufficient to protect against oscillation during the transition between conditions.

Over Temp Dsg

When the pack temperature measured by **Temperature** rises to or above this threshold while discharging (**Current** < (-) (*Dsg Current Threshold*)), then the Over Temperature in discharge direction (OTD) protection process is triggered and [OTD] is set in **Safety Alert** for *OT Dsg Time*. If the OTD condition clears prior to the expiration of the *OT Dsg Time* timer, then the [OTD] is cleared in **Safety Alert** and no [OTD] is set in **Safety Status**. If the condition does not clear, then [OTD] is set in **Safety Status** and if [OTFET] is set in *Operation Cfg B* the Discharge FET is opened. If [OTFET] is not set in *Operation Cfg B* then the Discharge FET is not opened by this fault. This fault condition causes [TDA] and [OTA] in **Battery Status** to be set. It also causes **Charging Current** to be set to 0.

Normal Setting: This setting depends on the environment temperature and the battery specification. Verify the battery specification allows temperatures up to this setting while charging and verify these setting are sufficient for the application temperature. The default is 60°C which is sufficient for most Li-Ion applications. The default *Over Temp Dsg* setting is higher than the default *Over Temp Chg* because Li-Ion can handle a higher temperature in the discharge direction than in the charge direction.

OT Dsg Time

See *Over Temp Dsg*. This is a buffer time allotted for Over Temperature in the discharge direction condition. The timer starts every time the [OTD] in **Safety Alert** is initially set. When the timer expires, then the bq20z80 forces an [OTD] in **Safety Status** and opens the Discharge FET if enabled with [OTFET] in *Operation Cfg B*. If [OTD] in **Safety Alert** clears (fault condition clears) prior to the expiration of the *OT Dsg Time* timer, then [OTD] in **Safety Alert** is cleared and the *OT Dsg Time* timer resets. Setting the *OT Chg Time* to 0 disables this function.

Normal Setting: This is normally set to 2 seconds which is sufficient for most applications. Temperature is normally a slow acting condition that does not need high speed triggering. It should be set long enough to prevent false triggering of the [OTD] in **Safety Status**, but short enough to prevent damage to the battery pack.

OT Dsg Recovery

OT Dsg Recovery is the temperature at which the battery recovers from an *OT Temp Dsg* fault. This is the only recovery method for an *OT Temp Dsg* fault.

Normal Setting: This register is application dependent, but is normally set low enough below the fault condition temperature to prevent quick oscillation in the Discharge FET if it was opened with the fault. The default is 55°C which is a 5 degrees difference which is sufficient to protect against this oscillation during the transition between conditions.

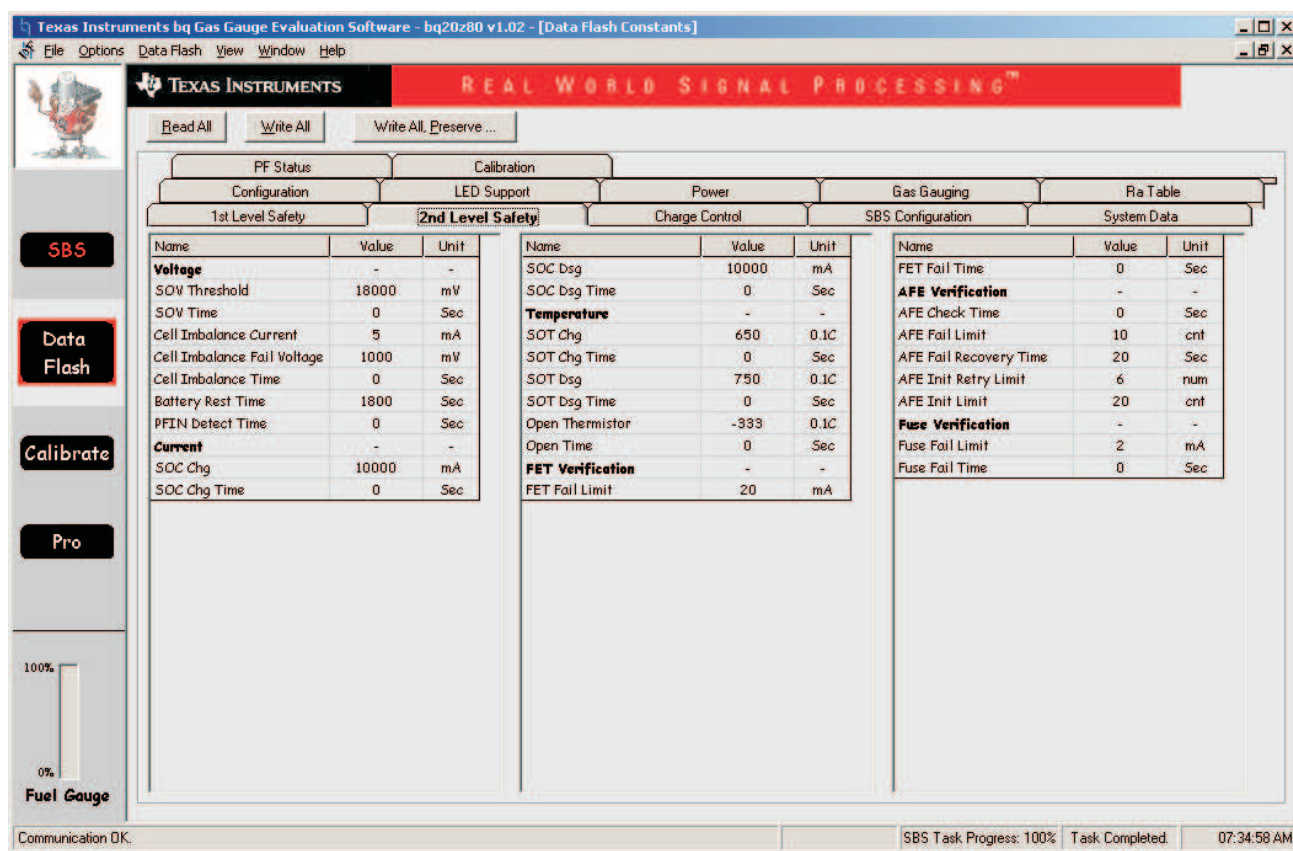
2.4 Host Comm

Host Watchdog Timeout

This function is only active when the bq20z80 is in Normal Power Mode (not asleep or in shutdown mode). It is also disabled if set to 0. If there is no communication to the bq20z80 via the SMBus for *Host Watchdog Timeout* time in seconds, then the bq20z80 reports [HWDG] set in **Safety Status** and opens the Charge, Discharge, and Pre-Charge FETs if enabled. This fault causes [TCA] and [TDA] in **Battery Status** to be set., and [XDSG] in **Operation Status** to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0. It is difficult to monitor this function because any SMBus communication clears the fault condition. To monitor the function using SMBus, then the SMBus command that is used to clear the fault condition must be an SMBus read of **Safety Status**. The [HWDG] flag is set on this read. Then on the next read (if its within the *Host Watchdog Timeout* window) the [HWDG] flag is cleared. The [HWDG] flag in **Safety Alert** as displayed in the EV Software is not used in this algorithm, and serves no purpose.

Normal Setting: This is not a common function and its default setting is 0. This provides another method for turning off the FETs, and preventing charge or discharge because the corresponding FETs are turned off when the fault occurs. It is also important to note that if the *Host Watchdog Timeout* is less than the *Bus Low Time*, then the fault condition occurs prior to the *Bus Low Timeout* which normally occurs prior to going to sleep. This function is disabled when in sleep mode, and the bq20z80 detects going to sleep mode as soon as the *Bus Low Timeout* expires. So, if the *Host Watchdog Timeout* timer expires prior to detecting bus low, then it triggers this fault.

3 2nd Level Safety



3.1 Voltage

SOV Threshold

This is a final level of protection. It is permanent. When the pack voltage measured by **Voltage** rises to this threshold, then the Safety Over Voltage (SOV) protection process is triggered. This process starts by setting [SOV] in **PF Alert** for **SOV Time**. If the SOV condition clears prior to the expiration of the **SOV Time** timer, then the [SOV] is cleared in **PF Alert**, and no [SOV] is set in **PF Status**. If the SOV condition does not clear, then [SOV] is set in **PF Status**. This triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in **Battery Status** is set
3. **Charging Current** and **Charging Voltage** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOV] in *Permanent Fail Cfg*, then
 - 0x3672 is programmed to the *Fuse Flag*.
 - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a voltage above the POV Threshold. This is meant to be a permanent condition, and it is recommended that [XSOV] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOV Time

See *SOV Threshold*. This is a buffer time allotted for an SOV condition. The timer starts after [SOV] is set in **PF Alert**. When it expires, then the bq20z80 forces an [SOV] in **PF Status** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOV Time* timer, then [SOV] is cleared in **PF Alert**, and the *SOV Time* timer resets without setting [SOV] in **PF Status**. If *SOV Time* is 0, then the *SOV Threshold* function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function must not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

Cell Imbalance Current

This is part of the safety cell imbalance detection algorithm. There are 4 registers that go together to make up this algorithm. *Cell Imbalance Current* is the value that **Current** must be below for the entire *Battery Rest Time* before Cell Imbalance detection is enabled. The bq20z80 does not start detecting a cell imbalance for this safety algorithm until the battery **Current** has been below this **Cell Imbalance Current** for at least the *Battery Rest Time*.

Normal Setting: This register should be set low to ensure the battery is completely relaxed when this algorithm is enabled. This Safety algorithm if triggered is permanent, and renders the battery useless. It is imperative that all data is valid prior to activation. The default setting is 5 mA which is sufficient for most applications.

Cell Imbalance Fail Voltage

This is part of the safety cell imbalance detection algorithm. For the purpose of this description:

Cell Voltage H = the highest SBS cell voltage

Cell Voltage L = the lowest SBS cell voltage

Delta Cell Voltage = **Cell Voltage H** - **Cell Voltage L**

There are 4 registers that go together to make up this algorithm. After the *Battery Rest Time* portion of the Cell Imbalance algorithm has passed the test criteria (see *Battery Rest Time* and *Cell Imbalance Current*), then if **Delta Cell Voltage** is greater than the *Cell Imbalance Fail Voltage* in millivolts, then the *Cell Imbalance Fail Voltage* protection process is triggered. This process starts by setting [CIM] in **PF Alert** for *Cell Imbalance Time*. If the cell imbalance condition clears prior to the expiration of the *Cell Imbalance Time* timer, then the [CIM] is cleared in **PF Alert** with no [CIM] being set in **PF Status**. If the cell imbalance condition does not clear, then [CIM] is set in **PF Status**. This triggers many permanent protection features as listed here:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in **Battery Status** is set
3. **Charging Current** and **Charging Voltage** is set to 0.
4. Data Flash Writes is disabled
5. if [XCIM] in *Permanent Fail Cfg* then
 - 0x3672 is programmed to the *Fuse Flag*.
 - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a voltage high enough to prevent any possibility of false triggering because this application is irreversible. This is meant to be a permanent condition and it is recommended that [XCIM] be set in Permanent Fail Cfg with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

Cell Imbalance Time

See *Cell Imbalance Fail Voltage*. This is a buffer time allotted for a cell imbalance safety condition. The timer starts after the *Battery Rest Time* has expired with current below the *Cell Imbalance Current* and **Delta Cell Voltage** (see *Cell Imbalance Fail Voltage*) is above the *Cell Imbalance Fail Voltage*. When the *Cell Imbalance Time* timer starts [CIM] is set in **PF Alert**. When the timer expires, then the bq20z80 forces a [CIM] in **PF Status** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *Cell Imbalance Time* timer, then [CIM] is cleared in **PF Alert**, and the *Cell Imbalance Time* timer resets without setting [CIM] in **PF Status**. The *Cell Imbalance Fail Voltage* function is disabled with *Cell Imbalance Time* equal to 0 or *Battery Rest Time* set to 0.

Normal Setting: This register defaults to 0. This disables the function. It is recommended that this function be enabled and the [XCIM] be enabled in *Permanent Failure Cfg* to protect against a potentially dangerous condition. *Battery Rest Time* helps prevent false triggering of this condition, so a good setting for Cell imbalance Time is 5 seconds. This gives several readings to ensure that the condition does exist.

Battery Rest Time

See *Cell Imbalance Current*. *Battery Rest Time* is the time in seconds that the battery **Current** must be below the *Cell Imbalance Current* for before Cell Imbalance detection is enabled. The bq20z80 does not start detecting a cell imbalance for this safety algorithm until the battery **Current** has been below *Cell Imbalance Current* for at least the *Battery Rest Time*. The *Cell Imbalance Fail Voltage* function is disabled with *Cell Imbalance Time* equal to 0 or *Battery Rest Time* set to 0.

Normal Setting: This register should be set for a relatively long time period to ensure the battery is completely relaxed when this algorithm is enabled. This safety algorithm, if triggered, is permanent and renders the battery useless. It is imperative that all data is valid prior to activation. The default setting is 1800 seconds which is sufficient for most applications.

PFIN Detect Time

This is a buffer time allotted for an $\overline{\text{PFIN}}$ safety condition. The timer *PFIN Detect Time* timer starts after the $\overline{\text{PFIN}}$ input pin has been set logic low by some external device (normally an external protector) which forces the [PFIN] is set in **PF Alert**. When it expires, then the bq20z80 forces an [PFIN] in **PF Status** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *PFIN Detect Time* timer, then [PFIN] is cleared in **PF Alert**, and the *PFIN Detect Time* timer resets without setting [PFIN] in **PF Status**. If *PFIN Detect Time* is 0, then this function is disabled. This fault condition triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in **Battery Status** is set
3. **Charging Current** and **Charging Voltage** is set to 0.
4. Data Flash Writes is disabled
5. if [XPFIN] in *Permanent Fail Cfg* then
 - 0x3672 is programmed to the *Fuse Flag*.
 - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: If this fault condition occurs then it is because an external device has already triggered a fault that should be nonrecoverable. This is meant to be a permanent condition, and it is recommended that [XPFIN] be set in *Permanent Fail Cfg*. If a fault occurs, and the external device sets the $\overline{\text{PFIN}}$ input low, the fuse will blow. If the fuse does not blow, then the bq20z80 attempts to blow the fuse (SAFE pin is set high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80). There is a clear function for this condition, but it is only intended to be used during the development process. The default for this function is 0. If the $\overline{\text{PFIN}}$ input is not used, then this function should be disabled. It is recommended that this function be used, and that [XPFIN] be set to ensure safe operation

3.2 Current

SOC Chg

SOC Chg is a final level of current protection from the bq20z80. This is not related to the 3rd level (AFE) protection which is a fast acting protection. It is also intended to be permanent. When the charge current as measured by **Current** rises to or above this threshold, then the Safety Over Current in the Charge direction (SOCC) protection process is triggered. This process starts by setting [SOCC] in **PF Alert** for SOC Chg Time. If the SOCC condition clears prior to the expiration of the SOC Chg Time timer, then the [SOCC] is cleared in **PF Alert** and with no [SOCC] being set in **PF Status**. If the SOC condition does not clear, then [SOCC] is set in **PF Status**. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET were all opened.
2. [TCA] and [TDA] in **Battery Status** is set
3. **Charging Current** and **Charging Voltage** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOCC] in *Permanent Fail Cfg* then
 - 0x3672 is programmed to the *Fuse Flag*.
 - The Safety Output pins is activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and should be set to a current above OC(2ndTier) Chg. It is not necessarily required to set above AFE OC Chg which is a fast acting fault condition meant for high current spike detection. This function is meant to be a permanent condition, and it is recommended that [XSOCC] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOC Chg Time

See SOC Chg. This is a buffer time allotted for an SOCC condition. The timer starts after [SOCC] is set in **PF Alert**. When it expires, then the bq20z80 forces an [SOCC] in **PF Status**, and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the SOC Chg Time timer, then [SOCC] is cleared in **PF Alert**, and the SOC Chg Time timer resets without setting [SOCC] in **PF Status**. If SOC Chg Time is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2-5 seconds.

SOC Dsg

SOC Dsg is a final level of current protection from the bq20z80. This is not related to the 3rd level (AFE) protection which is a fast acting protection. It is also intended to be permanent. When the discharge current as measured by **Current** falls down to or below a negative of this threshold (– (SOC Dsg)), then the Safety Over Current in the discharge direction (SOCD) protection process is triggered. This process starts by setting [SOCD] in **PF Alert** for SOC Dsg Time. If the SOCC condition clears prior to the expiration of the SOC Dsg Time timer, then the [SOCD] is cleared in **PF Alert** with no [SOCC] being set in **PF Status**. If the SOC condition does not clear, then [SOCD] is set in **PF Status**. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in **Battery Status** is set
3. **Charging Current** and **Charging Voltage** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOCD] in *Permanent Fail Cfg* then
 - 0x3672 is programmed to the *Fuse Flag*.
 - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: Care must be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This is the last level of protection and must be set to a current below *OC(2ndTier) Dsg*. It is not required to set above *AFE OC Dsg* which is a fast acting fault condition meant for high current spike detection. This is meant to be a permanent condition and it is recommended that [XSOCD] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOC Dsg Time

See *SOC Dsg*. This is a buffer time allotted for an SOCD condition. The timer starts after [SOCD] is set in **PF Alert**. When it expires, then the bq20z80 forces an [SOCD] in **PF Status** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOC Dsg Time* timer, then [SOCD] is cleared in **PF Alert**, and the *SOC Dsg Time* timer resets without setting [SOCD] in **PF Status**. If *SOC Dsg Time* is 0, then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function must not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

3.3 Temperature

SOT Chg

SOT Chg is a final level of temperature protection from the bq20z80. This fault condition is intended to be permanent. When the temperature as measured by **Temperature** rises to or above this threshold while charging ([DSG] cleared in **Battery Status**), then the Safety Over Temperature in the Charge direction (SOTC) protection process is triggered. This process starts by setting [SOTC] in **PF Alert** for *SOT Chg Time*. If the SOTC condition clears prior to the expiration of the *SOT Chg Time* timer, then the [SOTC] is cleared in **PF Alert** and with no [SOTC] being set in **PF Status**. If the SOT condition does not clear, then [SOTC] is set in **PF Status**. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET were all opened.
2. [TCA] and [TDA] in **Battery Status** is set
3. **Charging Current** and **Charging Voltage** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOTC] in *Permanent Fail Cfg* then
 - 0x3672 is programmed to the *Fuse Flag*.
 - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a temperature above *Over Temp Chg*. This is meant to be a permanent condition and it is recommended that [XSOTC] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOT Chg Time

See *SOT Chg*. This is a buffer time allotted for a Safety Over Temperature Condition. The timer starts after [SOTC] is set in **PF Alert**. When it expires, then the bq20z80 forces an [SOTC] in **PF Status** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOT Chg Time* timer, then [SOTC] is cleared in **PF Alert**, and the *SOT Chg Time* timer resets without setting [SOTC] in **PF Status**. If *SOT Chg Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

SOT Dsg

SOT Dsg is a final level of temperature protection from the bq20z80. This fault condition is intended to be permanent. When the temperature as measured by **Temperature** rises to or above this threshold while discharging ([DSG] set in **Battery Status**), then the Safety Over Temperature in the discharge direction (SOTD) protection process is triggered. This process starts by setting [SOTD] in **PF Alert** for SOT Dsg Time. If the SOTD condition clears prior to the expiration of the **SOT Dsg Time** timer, then the [SOTD] is cleared in **PF Alert** and with no [SOTD] being set in **PF Status**. If the SOT condition does not clear then [SOTD] is set in **PF Status**. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all be opened.
2. [TCA] and [TDA] in **Battery Status** is set
3. **Charging Current** and **Charging Voltage** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOTD] in *Permanent Fail Cfg* then
 - 0x3672 is programmed to the *Fuse Flag*.
 - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a temperature above *Over Temp Chg*. This is meant to be a permanent condition, and it is recommended that [XSOTC] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOT Dsg Time

See **SOT Dsg**. This is a buffer time allotted for a Safety Over Temperature Condition. The timer starts after [SOTD] is set in **PF Alert**. When it expires, then the bq20z80 forces an [SOTD] in **PF Status** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the **SOT Dsg Time** timer, then [SOTD] is cleared in **PF Alert**, and the **SOT Dsg Time** timer resets without setting [SOTD] in **PF Status**. If **SOT Dsg Time** is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function must not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

Open Thermistor

Setting *Open Thermistor Time* to 0 disables this function. The *Open Thermistor* register is part of a thermistor circuit fault protection algorithm in the bq20z80 that detects an open circuit in the thermistor circuit because **Temperature** reaches impossible values due to open circuit ADC readings. This fault condition is intended to be permanent. When the temperature as measured by **Temperature** falls to or below this threshold, then the Open Thermistor protection process is triggered. This process starts by setting [OTS] in **PF Alert** for *Open Thermistor Time*. If the OTS condition clears prior to the expiration of the Open Thermistor Time timer, then the [OTS] is cleared in **PF Alert** and with no [SOTS] being set in **PF Status**. If the OTS condition does not clear, then [OTS] is set in **PF Status**. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in **Battery Status** is set
3. **Charging Current** and **Charging Voltage** is set to 0.
4. Data Flash Writes is disabled
5. if [XOTS] in *Permanent Fail Cfg* then
 - 0x3672 is programmed to the *Fuse Flag*.
 - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This function is a good safety feature that is particularly useful in detecting thermistors that have come loose from the Gas Gauge PCB during the assembly process or if the wire of a thermistor comes loose from vibration. The value in this register does not need to be changed. This is meant to be a permanent condition, and it is recommended that [XOTS] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

Open Thermistor Time

See *Open Thermistor*. This is a buffer time allotted for an Open Thermistor Condition. The timer starts after [OTS] is set in **PF Alert**. When it expires, then the bq20z80 forces [OTS] set in **PF Status** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *Open Thermistor Time* timer, then [OTS] is cleared in **PF Alert**, and the *Open Thermistor Time* timer resets without setting [OTS] in **PF Status**. If *Open Thermistor Time* is 0 then the *Open Thermistor* function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

3.4 FET Verification

FET Fail Limit

FET Fail Limit register is part of a FET circuit fault protection algorithm in the bq20z80 that detects potentially hazardous FET circuit damage. This fault condition is intended to be permanent, and has two possible trigger functions to help prevent confusion. The functions are listed separately.

- (A) If the Charge and Pre-Charge FET (if enabled) have been commanded to be off for any reason by either the bq20z80 or the bq29312A (any AFE fault condition) and charge current as measured by **Current** still exists which is greater than *FET Fail Limit* in milliamps, then the *FET Fail Limit* protection process is triggered. This process starts by setting [CFETF] in **PF Alert** for *FET Fail Time*. If the [CFETF] condition clears prior to the expiration of the *FET Fail Time* timer, then the [CFETF] is cleared in **PF Alert** and no [CFETF] is set in **PF Status**. If the [CFETF] condition does not clear, then [CFETF] is set in **PF Status**. This triggers many permanent protection features as listed below:
- (B) If the discharge FET has been commanded to be off for any reason by either the bq20z80 or the bq29312A (any AFE fault condition) and discharge current as measured by **Current** still exists which is less than or equal to (–) *FET Fail Limit* in milliamps, then the *FET Fail Limit* protection process is triggered. This process starts by setting [DFETF] in **PF Alert** for *FET Fail Time*. If the [DFETF] condition clears prior to the expiration of the *FET Fail Time* timer, then the [DFETF] is cleared in **PF Alert** and no [DFETF] is set in **PF Status**. If the [DFETF] condition does not clear, then [DFETF] is set in **PF Status**. This triggers many permanent protection features as listed below:

Each of the above triggers (A. and B.) cause the following permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in **Battery Status** is set
3. **Charging Current** and **Charging Voltage** is set to 0.
4. Data Flash Writes is disabled
5. if A and [XCFETF] or B and [XDFETF] in *Permanent Fail Cfg* then
 - 0x3672 is programmed to the *Fuse Flag*.
 - The Safety Output pins is activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: The Charge and Discharge FETs arguably have more stress than any other component on the gas gauge PCB. This function is an excellent safety feature to help protect against the possibility of a shorted FET that is potentially hazardous. The default value in this register must be sufficient for most applications. This is meant to be a permanent condition, and it is recommended that [XCFETF] and [XDFETF] both be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

FET Fail Time

See *FET Fail Limit*. This is a buffer time allotted for the *FET Fail Limit* condition. The timer starts after either [CFETF] or [DFETF] set in **PF Alert**. When the timer expires, then the bq20z80 forces the associated flag (either [CFETF] or [DFETF]) in **PF Status** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *FET Fail Time* timer, then the associated flag (either [CFETF] or [DFETF]) is cleared in **PF Alert**, and the *FET Fail Time* timer resets without setting the associated flag (either [CFETF] or [DFETF]) in **PF Status**. If *FET Fail Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

3.5 AFE Verification

AFE Check Time

Every *AFE Check Time* in seconds, the bq20z80 reads all the bq29312A registers through the I²C port that is shared between the 2 parts and compares the static register read results to the AFE data in the bq20z80's Data Flash. If they do not match, then the bq20z80 attempts to repair the corruption. Then increment an internal counter (referred to in this document as AFE_P Fail Counter) which triggers the periodic AFE_P Fail protection process. This process starts by setting [AFE_P] in **PF Alert**. As long as the AFE_P Fail Counter stays below the *AFE Fail Limit* and above 0, [AFE_P] stays set in **PF Alert**. See *AFE Recovery Time* for a recovery description. If *AFE Check Time* is set to 0, then the periodic AFE verification (AFE_P) is completely disabled.

Normal Setting: Setting *AFE Check Time* to 0 only disables the AFE_P verification function. It does not disable the AFE_C verification function as described in *AFE Fail Limit*. *AFE Check Time* set to 0 is acceptable because there is still the AFE_C verification process. If, however, *AFE Check Time* is used, set it above 20 seconds since the periodic test does not need to be done often to ensure the correct function.

AFE Fail Limit

There are 2 AFE safety features that use this register. They are separated here to help prevent confusion.

- (A) The first safety feature is a continuation of *AFE Check Time*. If the AFE_P Fail Counter (as described above) reaches the *AFE Fail Limit* then [AFE_P] is cleared in **PF Alert**, and then set in **PF Status**. Setting *AFE Fail Limit* to 0 does not disable the periodic AFE verification (AFE_P). (See *AFE Check Time*)
- (B) The second safety feature is not associated with *AFE Check Time*. Anytime a communication with the bq29312A is performed over the I²C bus that is not part of the periodic check described in *AFE Check Time*, then a different internal counter (referred to in this document as AFE_C Fail Counter) increments. When the AFE_C Fail Counter increments, the AFE_C Fail protection process is triggered. This process starts by setting [AFE_C] in **PF Alert**. As long as the AFE_C Fail Counter stays below the *AFE Fail Limit* and above 0, then [AFE_C] stays set in **PF Alert**. See *AFE Recovery Time* for a recovery description. If the AFE_C Fail Counter reaches the *AFE Fail Limit*, then [AFE_C] is cleared in **PF Alert**, and then set in **PF Status**. Setting *AFE Fail Limit* to 0 disables the AFE_C Fail protection process.

Each of the above triggers (A. and B.) cause the following permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in **Battery Status** is set
3. **Charging Current** and **Charging Voltage** is set to 0.
4. Data Flash Writes is disabled

5. if A. [XAFE_P] set or if B and [XAFE_C] set in *Permanent Fail Cfg* then
 - 0x3672 is programmed to the *Fuse Flag*.
 - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the PF Status class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: *AFE Fail Limit* defaults to 10. It is very important to note that setting *AFE Fail Limit* to 0 only disables the AFE_C functions. AFE_P functions are not disabled with the *AFE Fail Limit* set to 0. This results in [AFE_P] flag getting set in **PF Status** on the first failure which is not recommended. The default of 10 is appropriate for most applications. This gives sufficient buffer for ESD, resets and other unknown failures that should be recoverable.

AFE Fail Recovery Time

See *AFE Check Time* and *AFE Fail Limit*. *AFE Fail Recovery Time* function works independently with each of the AFE counters described above (AFE_C Fail Counter and AFE_P Fail Counter). While [AFE_C] or [AFE_P] is set in **PF_Alert**, every *AFE Fail Recover Time* period in seconds AFE_C Fail Counter and/or AFE_P Fail Counter is decremented by 1 until each reaches 0. As soon as they are decremented back to 0, their associated flags ([AFE_C] or [AFE_P]) are cleared in **PF_Alert**, and the fault process is reversed.

Normal Setting: It is recommended that this register be set less than *AFE Check Time*, so that at least one recovery process can occur between periodic checks. *AFE Init Retry Limit*

This description is for reference only. The bq20z80 uses its internal ADC to measure initial AFE (bq29312A) offsets and gain values on every reset. The quality of these readings are critical to the accuracy of the voltage as displayed by **Voltage** and **Cell Voltage(All)**. Poor initial offset and gain readings can alter the voltage displayed, and it can take several minutes to reacquire accurate readings due to an internal slow responding digital filter in the bq20z80 firmware. With the importance of the quality of these initial readings, the bq20z80 takes 2 successive readings of these offsets and gain values, and compare them. If the comparison fails to meet the criteria as set by *AFE Init Limit* (see below), then the bq20z80 retries this procedure *AFE Init Retry Limit* times before it forces an AFE_C permanent failure. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in **Battery Status** is set
3. **Charging Current** and **Charging Voltage** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOV] in *Permanent Fail Cfg* then
 - 0x3672 is programmed to the *Fuse Flag*.
 - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: Modifying this register is not recommended; however, if unexplained AFE_C failures occur after resets, then this might be the function that caused the failure. Increasing this value can help, but the problem is normally a noisy environment due to switching from radio frequencies or PCB layout.

AFE Init Limit

This description is only for reference. This data flash location should never be modified. The bq20z80 uses its internal ADC to measure initial AFE (bq29312A) offsets and gain values on every reset. The quality of these readings are critical to the accuracy of the voltage as displayed by **Voltage** and **Cell Voltage(All)**. Poor initial offset and gain readings can alter the voltage displayed, and it can take several minutes to reacquire accurate readings due to an internal slow responding digital filter in the bq20z80 firmware. With the importance of the quality of these initial readings, the bq20z80 takes multiple readings (see *AFE Init Retry Limit* above) of these offsets and gain values, and compare them. The *AFE Init Limit* is the maximum difference in successive respective offset and gain value comparisons allowed for the values to be declared accurate. (Gain reading 2–Gain reading 1) must be below *AFE Init Limit*, (Offset reading 2–Offset reading 1) must be below *AFE Init Limit* etc.

Normal Setting: This register is in a reserved unit format; therefore, it is recommended that this value not be modified. It should be acceptable for most applications except for poor PCB layouts and noisy environments which affect voltage measurements. If this occurs, contact Texas Instruments for the value to put in this register.

3.6 Fuse Verification

Fuse Fail Limit

Fuse Fail Limit register is part of a Fuse circuit fault protection algorithm in the bq20z80 that detects potentially hazardous conditions. The *Fuse Fail Limit* is used in both the charge and the discharge direction. If the *Fuse Flag* has been set to 0x3672 (SAFE pin is set high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80) and the current as measured by **Current** still exists which is greater than *Fuse Fail Limit* in milliamps, or less than a (-) *Fuse Fail Limit* then the *Fuse Fail Limit* protection process is triggered. This process starts by setting [FBF] in **PF Alert** for *Fuse Fail Time*. If the [FBF] condition clears prior to the expiration of the *Fuse Fail Time* timer, then the [FBF] is cleared in **PF Alert** and no [FBF] is set in **PF Status**. If the [FBF] condition does not clear, then [FBF] is set in **PF Status**. This causes the normal Permanent Failure conditions except that with this function they are already set. This function only works with an existing permanent failure.

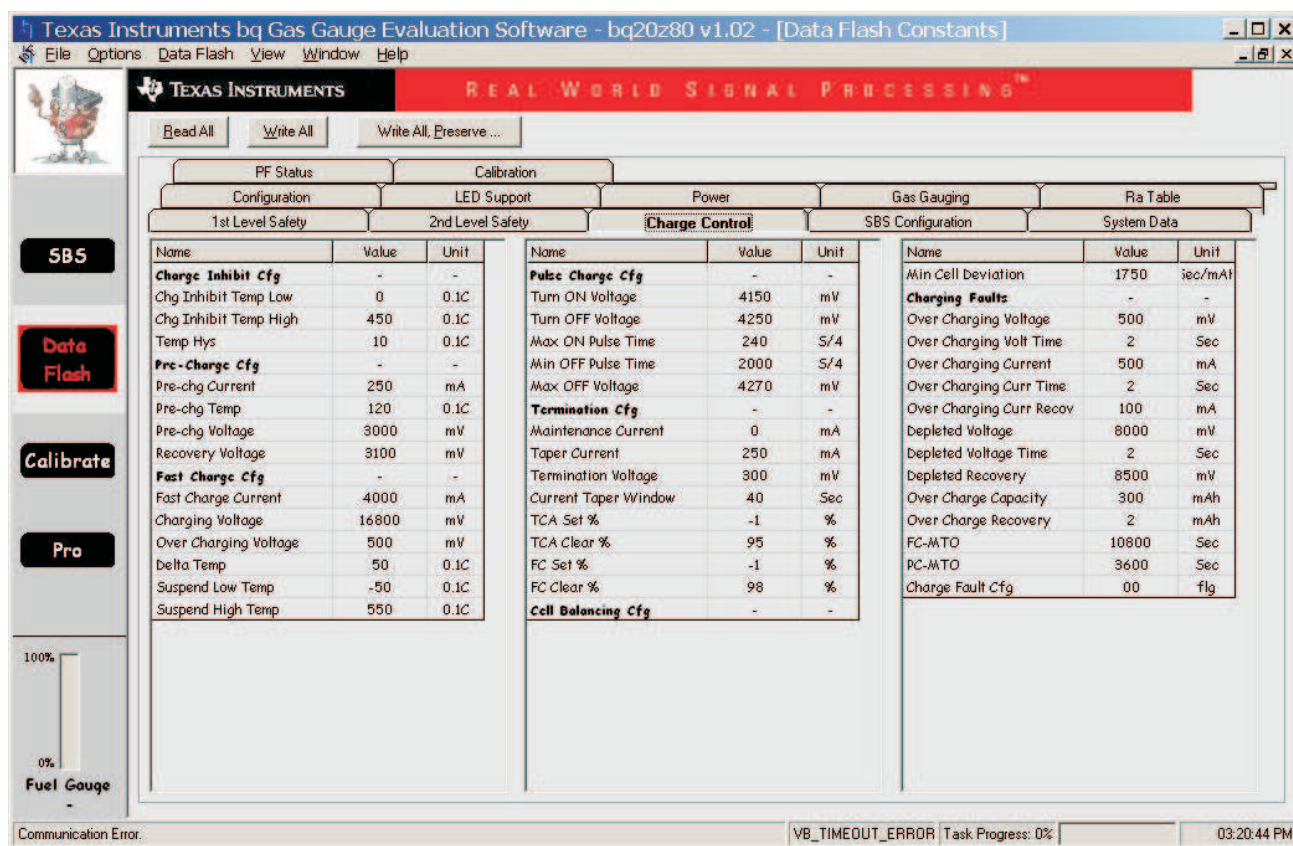
Normal Setting: The purpose of this function is for reporting and retaining the fact that the fuse was supposed to blow but did not. The fact that it causes an [FBF] flag being set in **PF Status** serves no purpose except for this fact being recorded for future data retrieval since the fuse was already supposed to be blown. The hope is that the bq20z80 will survive this potentially violent failure enough to be sent to the factory so that the Data Flash that this information was stored in can be read and analyzed to determine the cause of the failure. If the bq20z80 does not survive then this information is useless.

Fuse Fail Time

See *Fuse Fail Limit*. This is a buffer time allotted for the *Fuse Fail Limit* condition. The timer starts after [FBF] is set in **PF Alert**. When the timer expires, then the bq20z80 forces [FBF] in **PF Status**. If the condition clears prior to the expiration of the *Fuse Fail Time* timer, then [FBF] is cleared in **PF Alert** and the *Fuse Fail Time* timer resets without setting [FBF] in **PF Status**. If *Fuse Fail Time* is 0, then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. The only purpose of this function is to report that a fuse was instructed to blow and did not. The bq20z80 may not survive to report this information but it is possible. It is an uncommon event unless the fuse blow circuit design is faulty. The most common values for this register are between 2–5 seconds.

4 Charge Control



4.1 Charge Inhibit Config

Chg Inhibit Temp Low

When the pack temperature measured by **Temperature** falls to or below this threshold while discharging ([DSG] flag set in **Battery Status**), the Charge Inhibit Mode is triggered. This causes **Charging Current** and **Charging Voltage** to be set to 0, [XCHG] is set in **Charging Status**, and if [CHGIN] set in **Operation Cfg B**, then Charge FET is turned off and/or the Pre-Charge FET is turned off. There are two primary possible recoveries to this mode.

1. The primary recovery is if **Temperature** rises above (**Charge Inhibit Temp Low** + **Temp Hys**).
2. The condition is also cleared with pack removal and reinsertion (**PRE $\overline{S}$** transition) if [NR] is cleared in **Operation Cfg B**. If the condition still exists, then the inhibit mode is reactivated with [DSG] flag set in **Battery Status**.

With either of these recoveries, [XCHG] is cleared in **Charging Status**. This enables the charging process to initiate.

Normal Setting: The purpose of this low inhibit temperature is not to suspend charging, but to prevent it from starting when the conditions are not acceptable. This prevents damage to the pack. The default for this is 0 degrees, and can be modified to fit the application.

Chg Inhibit Temp High

When the pack temperature measured by **Temperature** rises to or above this threshold while discharging ([DSG] flag set in **Battery Status**) the Charge Inhibit Mode is triggered. This causes **Charging Current** and **Charging Voltage** to be set to 0, [XCHG] is set in **Charging Status**, and if [CHGIN] set in **Operation Cfg B** then Charge FET is turned off and/or the Pre-Charge FET is turned off. There are two primary possible recoveries to this mode.

1. The primary recovery is if **Temperature** falls below (**Charge Inhibit Temp Low** – **Temp Hys**).

2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists then, the inhibit mode is reactivated with [DSG] flag set in **Battery Status**.

With either of these recoveries, [XCHG] is cleared in **Charging Status**. This enables the charging process to initiate.

Normal Setting: The purpose of this high inhibit temperature is not to suspend charging but to prevent it from starting when the conditions are not acceptable. This prevents damage to the pack. The default for this is 45°. Notice that this is less than the default charge suspend mode (see *Suspend High Temp*).

Temp Hys

This register works with both *Chg Inhibit High* and *Chg Inhibit Low* in the recovery process.

1. With charge inhibited resulting from a high temperature and if **Temperature** falls below (*Charge Inhibit Temp High – Temp Hys*), then the [XCHG] is cleared in **Charging Status**. This enables the charging process to initiate.
2. With charge inhibited resulting from low temperature and if **Temperature** rises above (*Charge Inhibit Temp Low + Temp Hys*), then the [XCHG] is cleared in **Charging Status**. This enables the charging process to initiate.

Normal Setting: this register defaults to 1°C. For most applications, this is considered low for a hysteresis value. This register should be set to at least 2°C to 3°C to prevent oscillation of this condition.

4.2 Pre-Charge Config

Pre-Charge Current

This is the current that the bq20z80 reports in the **Charging Current** register when the bq20z80 is in Pre-Charge mode (see *Pre-Chg Temperature* and *Pre-Chg Voltage*). This current is broadcast to a smart charger when bq20z80 master mode broadcasts are enabled ([BCAST] set in *Operation Cfg B*). When in Pre-Charge Mode (**Charging Current** = *Pre-Charge Current*), [PCHG] is set in **Charging Status**, then the appropriate charging FET is enabled as set with [ZVCHG1] and [ZVCHG0] in *Operation Cfg A*.

ZVCHG1	ZVCHG0	FET Used
0	0	ZVCHG
0	1	CHG
1	0	OD
1	1	No Action

There are three primary recoveries from Pre-Charge mode:

1. Independent of the method (*Pre-Chg Voltage* or *Pre-Chg Temperature*) that caused the Pre-Charge Mode:
 - (a) **Cell Voltage (All)** must be above *Recovery Voltage*
 - (b) **Temperature** must be above (*Pre Chg Temperature + Temp Hys*)
 Either of these conditions cause the bq20z80 to enter Fast Charge Mode (See *Fast Charge Current*)
2. Pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the inhibit mode is reactivated with any of the Pre-Charge criteria.
3. This is considered a recovery, but it is really a transition from one mode to another. A charge suspend condition (see *Suspend High Temp* and *Suspend Low Temp*) which forces the bq20z80 to transition from Pre-Charge Mode to Charge Suspend Mode.

Normal Setting: This register is application dependent. If a Pre-Charge FET and a current limiting resistor is used to control the current allowed into the battery during Pre-Charge Mode ([ZVCHG1] and [ZVCHG1] both equal 0), then this register accuracy is not as important as if it were used for a smart charger which initiate a current equal to the requested Pre-Charge current. It is important to note that use of the OD pin is not recommended because it does not have limiting circuitry to ensure "hard" on control for a Zero Volt charging condition. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is always recommended.

Pre-Chg Temperature

See *Pre-Charge Current*. With either the *Pre-Chg Voltage* or the *Pre-Chg Temperature* criteria being met, then the bq20z80 triggers Pre-Charge Mode. With **Temperature** falling to or below *Pre-Chg Temperature*, but above Charge Inhibit Temp Low, then the bq20z80 enters the Pre-Charge Mode (see *Pre-Charge Current*).

Normal Setting: Ensure that this register is above the *Charge Inhibit Temp Low*. This ensures that *Pre-Chg Temperature* is above the charge suspend temperature because the charge suspend is below the charge inhibit. (See *Charge Inhibit Temp Low* and *Charge Suspend Temp Low*). At cold temperatures, lower currents are better for the battery cells. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is recommended.

Pre-Chg Voltage

See *Pre-Charge Current*. With either the *Pre-Chg Voltage* or the *Pre-Chg Temperature* criteria being met, then the bq20z80 triggers Pre-Charge Mode. With **Cell Voltage (Any)** falling to or below *Pre-Chg Voltage*, then the bq20z80 enters Pre-Charge Mode (see *Pre-Charge Current*).

Normal Setting: Ensure that this voltage is set per the battery cell specifications. Setting this value too high is not harmful (except for slower charging from empty), but setting this value too low can damage cells. This register gives the cells a chance for a Pre-Charge voltage which brings them up to a normal charging voltage before hitting them with a fast current. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is recommended.

Recovery Voltage

If the battery pack is in Pre-Charge mode due to **Cell Voltage (Any)** falling to or below *Pre-Chg Voltage*, then it exits the Pre-Charge mode and enter the Fast Charge Mode (see *Fast Charge Current*) when **Cell Voltage (All)** rises above *Recovery Voltage*. This is one of three primary recovery methods for a battery pack in Pre-Charge mode.

Normal Setting: This is battery cell dependent. Ensure that it is set per the battery cell specifications. Setting this value too high is not harmful (except for slower charging from empty), but setting this value too low can damage cells. This register gives the cells a chance for a Pre-Charge voltage which brings them up to normal charging voltage before hitting them with a fast current. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is recommended.

4.3 Fast Charge Config

Fast Charge Current

This is the current that the bq20z80 reports in the **Charging Current** register when the bq20z80 is in Fast Charge mode (see *Pre-Chg Temperature*, *Pre-Chg Voltage*, and *Pre-Chg Current*). This current is also broadcast to a smart charger when bq20z80 master mode broadcasts are enabled ([BCAST] set in *Operation Cfg B*). When in Fast Charge Mode (**Charging Current** = Fast Charge Current), [FCHG] is set in **Charging Status** and the Charge FET is enabled. There are three primary criteria that must be met to be in Fast Charge Mode:

1. Assuming all temperature faults are configured correctly (*Pre-Chg Temperature* configured in Data Flash as the highest low temperature mode), **Temperature** is above *Pre-Chg Temperature* with [PCHG] clear in **Charging Status**
2. **Temperature** is below *Suspend High Temp* and no [CHGSUSP] in **Charging Status**
3. **Voltage** must be above *Pre-Chg Voltage* with [PCHG] clear in **Charging Status**
4. **Voltage** must be below **Charging Voltage** + *Over Charging Voltage*

While in Fast Charge Mode, there is an option called Charge Throttling that is enabled/disabled by *Delta Temperature* as described below (See *Delta Temperature*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

Charging Voltage

When in any charging mode without a fault condition present, the *Charging Voltage* is the voltage that is put in **Charging Voltage**. With most fault conditions **Charging Voltage** is set to 0. This is also used in bq20z80 charge qualification and termination algorithms.

Normal Setting: This register is normally set based on the charger specifications. Charger tolerances are considered when setting this register.

Over Charging Voltage

THIS REGISTER IS NOT USED BY THE bq20z80. IT IS REMOVED FROM FUTURE VERSIONS. It is not used because there is an *Over Charging Voltage* register in the **Charging Faults** subclass as described in that section.

Delta Temp

Delta Temp is used in a “throttling” algorithm for maximizing the charging algorithm. This description starts in Fast Charge Mode with Temperature in the normal range and **Charging Current** = *Fast Charge Current*. The value that is in **Charging Current** is broadcast to smart chargers if master mode broadcasts are enabled ([BCAST] set in *Operation Cfg B*)

- (A) When the **Temperature** rises to (*Suspend High Temp* – (*Delta Temp* × 2)) then the bq20z80 initiates stage 2 throttling. In this mode, the **Charging Current** register is changed from *Fast Charge Current* to (*Fast Charge Current* – *Pre-Chg Current*) / 2. Also, [TCHG2] is set in **Charging Status**. The purpose of this stage is to request a slower **Charging Current** to prevent overheating of the battery. If Temperature continues to climb then see step B).
- (B) If the **Temperature** continues to rise even though the **Charging Current** was decreased, then when the **Temperature** rises to (*Suspend High Temp* – *Delta Temp*), the bq20z80 initiates stage 1 throttling. In this mode, the **Charging Current** register is changed from [(*Fast Charge Current* – *Pre-Chg Current*) / 2] to *Pre-Chg Current*. Also [TCHG1] is set in **Charging Status** and [TCHG2] is cleared.
- (C) If the **Temperature** continues to climb, then it reaches the *Suspend High Temp* which halts charging completely. (see *Suspend High Temp*).

The battery returns to Fast Charge Mode when the temperature falls back below (*Suspend High Temp* – (*Delta Temp* × 2)) which clears [TCHG1] and [TCHG2] in **Charging Status**. If *Delta Temp* is set to 0, then this function is disabled.

Normal Setting: Ensure that this value is large enough to keep the battery from switching modes rapidly; however, setting it to high increases the charging time and reduces the algorithms effectiveness. This register is only required in either high temperature environments, or with extreme charge currents.

Suspend Low Temp

When the pack temperature measured by **Temperature** falls to or below *Suspend Low Temp* while charging ([DSG] flag clear in **Battery Status**), then the Charge Suspend Mode is triggered. This causes **Charging Current** to be set to 0, [CHGSUSP] is set in **Charging Status**, and if [CHGSUSP] set in *Operation Cfg B*, then the Charge FET and Pre-Charge FET are both opened regardless of their prior open/close state. There are two primary possible recoveries to this mode

1. The primary recovery is if **Temperature** rises above (*Suspend Low Temp* + *Temp Hys*).
2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the suspend mode is reactivated with [DSG] flag cleared in **Battery Status**.

With either of these recoveries, [CHGSUSP] is cleared in **Charging Status**. This enables the charging process to resume.

Normal Setting: Notice that default *Suspend Low Temp* is lower than *Chg Inhibit Low Temp*. This value is application and battery cell dependent.

Suspend High Temp

When the pack temperature measured by **Temperature** rises to or above *Suspend High Temp* while charging the ([DSG] flag in **Battery Status**), then the Charge Suspend Mode is triggered. This causes **Charging Current** to be set to 0, [CHGSUSP] is set in **Charging Status**, and if [CHGSUSP] set in *Operation Cfg B*, then the Charge FET and Pre-Charge FET are both opened regardless of their prior open/close state. There are two primary possible recoveries to this mode.

1. The primary recovery is if **Temperature** falls below (*Suspend High Temp* – *Temp Hys*).
2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the suspend mode is reactivated with [DSG] flag cleared in **Battery Status**.

With either of these recoveries, [CHGSUSP] is cleared in **Charging Status**. This enables the charging process to resume.

Normal Setting: Notice that default *Suspend High Temp* is higher than *Chg Inhibit High Temp*. This value is application and battery cell dependent.

4.4 Pulse Charge Config

Pulse Charge Config is one of the most confusing setups in the bq20z80. In application, however, it is a relatively simple function. When charging, these settings can be used to turn ON and OFF the Charge FET to provide a pulse charging function. Figure 1 shows an example of a pulse charging voltage vs time wave form with all the Pulse Charge Config registers explained graphically.

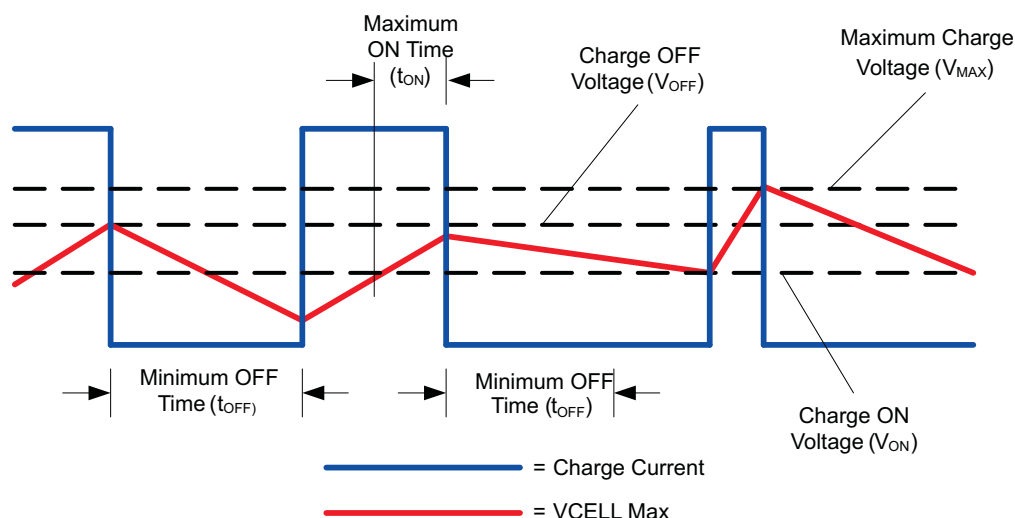


Figure 1. Pulse Charging Voltage vs Time

Turn Off Voltage

While charging ([DSG] clear in **Battery Status**) and in Fast Charge Mode ([FCHG] set in **Charging Status**), when **Cell Voltage (MAX)** rises to or above *Turn Off Voltage*, then the *Max On Pulse Time* timer initiates (see *Max On Pulse Time* for the rest of this process). If *Max On Pulse Time* is set to 0, then the process acts as if the *Max On Pulse Time* timer expired immediately (see *Max On Pulse Time* for the rest of this process).

Normal Setting: This is application dependent, if Pulse Charging is required, then *Turn Off Voltage* should be set below *Max Off Voltage* so that *Max On Pulse Time* is given time to expire throughout most of each charge cycle. This maximizes charge efficiency.

This explanation is continued from *Min Off Pulse Time* (see *Min Off Pulse Time*). While charging ([DSG] clear in **Battery Status**) and in Fast Charge Mode ([FCHG] set in **Charging Status**), the *Min Off Pulse Time* timer is initiated as soon as the Charge FET opens. Regardless of whether or not the **Cell Voltage (MAX)** falls below the *Turn On Voltage*, the *Min Off Pulse Time* timer must expire before the bq20z80 allows the Charge FET to be closed, and allows charge current to flow. If *Min Off Pulse Time* timer expires prior to **Cell Voltage (MAX)** falling below *Turn On Voltage*, the Charge FET is not closed until **Cell Voltage (MAX)** reaches *Turn On Voltage*. When the Charge FET is closed, then [PLSOFF] is cleared in **Charging Status**.

Normal Setting: This is battery cell specification specific. See the Cell manufacturer data sheet for maximum voltage allowed. Note that the cell voltage readings for this algorithm are updated every 250 ms when in pulse charging mode instead of 1 second updates with **Cell Voltage (ALL)**.

Max On Pulse Time

This explanation is continued from *Turn Off Voltage* above (see *Turn Off Voltage*). While charging ([DSG] clear in **Battery Status**) and in Fast Charge Mode ([FCHG] set in **Charging Status**), when **Cell Voltage (MAX)** rises to or above *Turn Off Voltage*, then the *Max On Pulse Time* timer initiates. If *Max On Pulse Time* is set to 0, then the process acts as if the *Max On Pulse Time* timer expired immediately. The expiration of the *Max On Pulse Time* timer forces the Charge FET to open, [PLSOFF] and [PULSE] to be set in **Charging Status**, and the *Min Off Pulse Time* timer to be initiated (See *Min Off Pulse Time*). If *Max On Pulse Time* timer does not expire prior to **Cell Voltage (MAX)** reaching *Max Off Voltage*, then *Max Off Voltage* forces the Charge FET to open (See *Max Off Voltage*).

Normal Setting:

This register should be set to such a time that the Charge FET will shut off by this timer most of the time and not by the *Max Off Voltage*. It is not uncommon for this register to be 0 which would only use the *Max Off Voltage* for turning off the Charge FET. Care should be taken when setting it to 0 to ensure that the voltage does not overrun enough to produce a COV condition. The default for this register is 240 ms. This register is in units of Seconds/4 or 250 ms which is one minute.

Min Off Pulse Time

This explanation is continued from one of the following condition descriptions.

1. *Max On Pulse Time*
2. *Max Off Voltage*
3. *Turn Off Voltage*

While charging ([DSG] clear in **Battery Status**) and in Fast Charge Mode ([FCHG] set in **Charging Status**), the *Min Off Pulse Time* timer is initiated as soon the Charge FET opens from one of these listed conditions (1–3 above). Regardless of whether or not the **Cell Voltage (MAX)** falls below the *Turn On Voltage*, the *Min Off Pulse Time* timer must expire before the bq20z80 allows the Charge FET to be closed, and allows charge current to flow. If *Min Off Pulse Time* timer expires prior to **Cell Voltage (MAX)** falling below *Turn On Voltage*, the Charge FET is not closed until **Cell Voltage (MAX)** reaches *Turn On Voltage* (see *Turn On Voltage*).

Normal Setting: This register defaults to 0. This is a buffer to prevent fast oscillation of the Charge FET.

Max Off Voltage

This explanation is continued from *Max On Pulse Time* above (see *Max On Pulse Time*). While charging ([DSG] clear in **Battery Status**) and in Fast Charge Mode, when **Cell Voltage (MAX)** rises to or above *Turn Off Voltage*, then the *Max On Pulse Time* timer initiates. If *Max On Pulse Time* timer does not expire prior to **Cell Voltage (MAX)** reaching *Max Off Voltage* then *Max Off Voltage* forces the Charge FET to open, [PLSOFF] and [PULSE] to be set in **Charging Status**, and the *Min Off Pulse Time* timer to be initiated (See *Min Off Pulse Time*).

Normal Setting: This is battery cell specification specific. See the Cell manufacturer data sheet for maximum voltage allowed. Note that the cell voltage readings of this algorithm are updated every 250 ms when in pulse charging mode instead of 1 second updates with **Cell Voltage (ALL)**.

4.5 Termination Config

Maintenance Current

Maintenance Current is only put into the **Charging Current** register when [TCA] is set in **Battery Status** by a primary charge termination (See **Taper Current**), or **TCA Set%** condition (see **TCA Set%**), or many of the fault conditions from the **1st Level Safety** and **2nd Level Safety** classes. Even with [TCA] set, if configured for Charge FET to be turned off ([CHGFET] set in **Operation Cfg B**) then **Charging Current** is set to 0, and [MCHG] is cleared in **Charging Status**.

Normal Setting: This register should be 0 for most if not all Li-Ion chemistries.

Taper Current

Taper Current is used in the Primary Charge Termination algorithm. **Current** is integrated over each of the two **Current Taper Window** periods separately, and then they are averaged separately to give two averages. Both of these averages must be below the **Taper Current** to qualify for a Primary Charge Termination. In total, a primary charge termination has the following requirements:

1. **Voltage** must be above (**Charging Voltage** – **Termination Voltage**) for the bq20z80 to start trying to qualify a termination. It must be above this voltage before bq20z80 starts trying to detect a primary charge termination.
2. An average of all **Current** measurements must be below **Taper Current** for two consecutive periods of **Current Taper Window** from beginning to end of each window.
3. An average of all **Current** measurements during each of two consecutive periods of **Current Taper Window** from beginning to end of each window must be above 0.25 mAh as integrated, and averaged over the two **Current Taper Windows**.

When these conditions are met, the primary charge termination has occurred and the following happens:

1. 1. if **TCA Set %** = –1 (disabled) then [TCA] is set in **Battery Status** and either of the following happens:
 - (a) if [CHGFET] set in **Operation Cfg B** then and **Charging Current** is set to 0, and the Charge FET is opened.
 - (b) if [CHGFET] is cleared in **Operation Cfg B** then and **Charging Current** is set to **Maintenance Current**.
2. If **FC_Set %** = –1 (disabled), then [FC] is set in **Battery Status**
3. If [CSYNC] is set in **Operation Cfg B**, then **Remaining Capacity** is written to **Full Charge Capacity**.

The primary charge termination mode has two clearing methods:

1. It is cleared when **RSOC** falls below **FC Clear %**
2. if [CHGTERM] in **Operation Cfg B** set, and **Current** is less than **Chg Current Threshold** for two consecutive periods of **Current Taper Window**.

Normal Settings: This register is dependent on battery cell characteristics and charger specifications, but typical values are C/10 to C/20. **Average Current** is not used for this qualification because its time constant is not the same as the **Current Taper Window**. The reason for making two **Current Taper** qualifications is to prevent false current taper qualifications. False primary terminations happens with pulse charging and with random starting and stopping of the charge current. This is particularly critical at the beginning or end of the qualification period. It is important to note that as the **Current Taper Window** value is increased, the current range in the 3rd requirement for primary charge termination is lowered. If you increase the **Current Taper Window**, then the current used to integrate to the 0.25 mAh is decreased, so this threshold becomes more sensitive. Therefore, care should be taken when modifying the **Current Taper Window**.

Termination Voltage

During Primary Charge Termination detection, one of the 3 requirements is that **Voltage** must be above (**Charging Voltage** – **Termination Voltage**) for the bq20z80 to start trying to qualify a termination. It must be above this voltage before bq20z80 starts trying to detect a primary charge termination.

Normal Setting: This value is dependent on charger characteristics. It needs to be set so that ripple voltage, noise, and charger tolerances are taken into account. A low value selected can cause early termination. If the value selected is too high, then it can cause no or late termination detection. An example value is 200 mV (see *Taper Current*).

Current Taper Window

During Primary Charge Termination detection, all three requirements as described in *Maintenance Current* must be valid for two periods of this *Current Taper Window* for the bq20z80 to detect a primary charge termination (see *Taper Current*).

Normal Setting: This register does not need to be modified for most applications. It is important to note that as the *Current Taper Window* value is increased, the current range in the 3rd requirement for primary charge termination is lowered. If the user increases the *Current Taper Window*, then the current used to integrate to the 0.25 mAh is decreased, so this threshold becomes more sensitive. Therefore, care should be taken when modifying the *Current Taper Window*.

TCA Set %

This is an alternative method to setting [TCA] in **Battery Status**. If this is set to anything but (-)1, then this is the only normal (nonfault condition) function that sets [TCA]. This means that a Primary Charge Termination is not set [TCA] with *TCA Set %* set between 0 and 100%. If set to (-)1, then the Primary Charge Termination algorithm is the only normal mode algorithms used to set [TCA]. If set between and including 0 and 100%, then whenever charging ([DSG] not set in **Battery Status**) and **RSOC** rises above this value then [TCA] is set in **Battery Status**. Regardless of this setting or any Primary Charge Termination setting, any fault condition that has [TCA] as part of its fault process works completely independent of these functions.

Normal Setting: This is a user preference. *TCA Set %* may be used if it is mandatory that [TCA] be set during the Charge process. It is a good process to use if the Primary Charge Termination is not assured every charge cycle (see *Maintenance Charge*). If the [CSYNC] bit is set in *Operation Cfg B*, then a Primary Charge Termination writes **Remaining Capacity** up to **Full Charge Capacity** and writes **RSOC** to 100% so [TCA] is set with this method even if *TCA Set %* is set between 0 and 100%

TCA Clear %

If during discharge ([DSG] set in **Battery Status**), **RSOC** falls below this value then [TCA] is cleared.

Normal Setting: Must be set below *TCA Set %* if used.

FC Set %

This is an alternative method to setting [FC] in **Battery Status**. If this is set to anything but (-)1, then this is the only normal function that sets [FC]. If set to (-)1, then the Primary Charge Termination algorithm is used to set [FC]. If set between and including 0 and 100%, then whenever charging ([DSG] not set in **Battery Status**) and **RSOC** rises above this value, then [FC] is set in **Battery Status**. Regardless of this setting, any fault condition that has [FC] as part of its fault process works completely independent of this function.

Normal Setting: This is user preference. *FC Set %* may be used if it is mandatory that [FC] be set during the Charge process. It is a good process to use if the Primary Charge Termination is NOT assured ever charge period (see *Taper Current*).

FC Clear %

If during discharge ([DSG] set in **Battery Status**), **RSOC** falls below this value, then [FC] is cleared.

Normal Setting: Must be set below *FC Set %* if used.

4.6 Cell Balancing Config

Min Cell Deviation

The cell balancing algorithm will be active only during charging ([DSG] cleared in **Battery Status**). The function is disabled completely if *Min Cell Deviation* is set to 0. With impedance track, the bq20z80 knows the Full Charge Capacity for each cell independently. Each cell input in the bq29312A has an internal FET that shorts the cell filtering resistors, and an internal 500-Ω resistor across the cells that need reduced charging to help balance the cells. The bq20z80 uses impedance track information along with the value for *Min Cell Deviation* to know how long to turn on the shorting FET. The algorithm works based on the formula:

$$\text{Min Cell Deviation} = dQ \times R / (V \times \text{duty cycle})$$

Where:

dQ = correction factor = 3600 seconds/hour

V = nominal cell voltage = 3600 mV

duty cycle = 40% = 0.4

R = Total resistance from cell top to cell bottom (2 filter resistors and internal 500-Ω resistor), so for the bq20z80 EVM, the filter resistors are 100 Ω; therefore, $R = 100 \times 2 + 500 = 700 \Omega$

So for 700 Ω in resistance Min Cell Deviation = 1750 sec/mAh

Normal Setting: The bq20z80 default value for this register is 1750 s/mAH. The only values that is needed to be changed in the formula are R (Resistance), and V (nominal cell voltage). (See [SLUA340](#) for more information)

4.7 Charging Faults

Over Charging Voltage

When the pack voltage measured by **Voltage** rises to or above (**Charging Voltage** + **Over Charging Voltage**), then Over Charging Voltage fault process is triggered which initiates the **Over Charging Volt Time** timer. If **Voltage** falls below (**Charging Voltage** + **Over Charging Voltage**) prior to the expiration of the **Over Charging Volt Time** timer, then the Over Charging Voltage fault process halts and the **Over Charging Volt Time** timer resets. If the **Voltage** continues to be above (**Charging Voltage** + **Over Charging Voltage**) until the **Over Charging Volt Time** timer expires, then the bq20z80 sets the [OCHGV] in **Charging Status** and if [OCHGV] is set in **Charge Fault Cfg**, then the Charge FET and Pre-Charge FET are both opened regardless of their status prior to the fault. This fault condition causes [TCA] in **Battery Status** to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0. The bq20z80 clears the Over Voltage fault condition when **Voltage** falls to or below **Charging**.

Voltage.Normal Setting: This value should be high enough that ripple on the charger voltage does not cause a false Over Charging Voltage fault, but low enough to allow for a normal fault condition.

Over Charge Voltage Time

When the **Over Charging Voltage** criteria are met then Over Charging Voltage fault process is triggered which initiates the **Over Charging Volt Time** timer. If the **Over Charging Voltage** criteria continue to be met until the **Over Charging Volt Time** timer expires, then the bq20z80 sets [OCHGV] in **Charging Status**, and if [XCHGV] is set in **Charge Fault Cfg**, then the Charge FET and Pre-Charge FET are both opened regardless of their status prior to the fault. This fault condition causes [TCA] in **Battery Status** to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0. If **Voltage** falls below **Over Charging Voltage** criteria any time prior to the expiration of the **Over Charging Volt Time** timer, then the Over Charging Voltage fault process halts and the **Over Charging Volt Time** timer resets. The bq20z80 clears the Over Voltage fault condition when **Voltage** falls to or below **Charging Voltage**. (See **Over Charging Voltage**)

Normal Setting: The default for this register is 2 seconds. This should be sufficient for most applications. This function is not disabled if set to 0. Instead it triggers immediately.

Over Charging Current

When the current as measured by **Current** rises up to or above (**Charging Current** + **Over Charging Current**) then Over Charging Current fault process is triggered which initiates the **Over Charging Current Time** timer. If **Current** falls below (**Charging Current** + **Over Charging Current**) prior to the expiration of the **Over Charging Current Time** timer, then the Over Charging Current fault process halts and the **Over Charging Current Time** timer resets. If the **Current** continues to be above (**Charging Current** + **Over Charging Current**) until the **Over Charging Current Time** timer expires, then the bq20z80 sets [OCHGI] in **Charging Status** and if [XCHGI] is set in **Charge Fault Cfg**, then the Charge FET and Pre-Charge FET are both opened regardless of their status prior to the fault. This fault condition causes [TCA] in **Battery Status** to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0. The bq20z80 clears the Over Current fault condition when **Average Current** falls to or below **Over Charging Recovery Current**.

Normal Setting: This setting should be set high enough to prevent false triggering, but low enough to prevent battery cell damage. 500 mA is the default setting which is sufficient for most applications.

Over Charging Current Time

When the *Over Charging Current* criteria are met, then Over Charging Current fault process is triggered which initiates the *Over Charging Current Time* timer. If the *Over Charging Current* criteria continue to be met until the *Over Charging Current Time* timer expires, then the bq20z80 set the [OCHGI] in **Charging Status** and if [XCHGV] is set in *Charge Fault Cfg*, then the Charge FET and Pre-Charge FET are both opened regardless of their status prior to the fault. This fault condition causes [TCA] in **Battery Status** to be set. It also causes **Charging Current** and **Charging Voltage** to be set to 0. If **Current** falls below *Over Charging Current* criteria any time prior to the expiration of the *Over Charging Current Time* timer, then the Over Charging Current fault process halts and the *Over Charging Current Time* timer resets. The bq20z80 clears the Over Current fault condition when **Average Current** falls to or below *Over Charging Recovery Current*.

Normal Setting: The default for this register is 2 seconds. This is sufficient for most applications. This function is not disabled if set to 0. Instead it triggers immediately.

Over Charging Recov Curr

When the *Over Charging Current* criteria are met to the point of forcing an Over Charging Condition Fault, then the bq20z80 clears the Over Current fault condition when **Average Current** falls to or below *Over Charging Recovery Current*.

Normal Setting: The default for this register is 100 mA. This is sufficient for most applications.

Depleted Voltage

When the voltage measured by **Voltage** falls to *Depleted Voltage* threshold and stays at or below this level for more than *Depleted Voltage Time* seconds, then the bq20z80 sets the [XCHGLV] in **Charging Status** and the [TDA] in **Battery Status**. If [CS_XCHGLV] bit is set in *Charge Fault Cfg*, then the discharge FET is turned off. A charger must be detected as present for a *Depleted Voltage* fault to occur. See *Charger Present* for a description on how to detect a charger.

Normal Setting: This function is not recommended if there is any external voltage source that could interfere with *Charger Present*. Set *Depleted Voltage Timer* to 0 to disable this function. This register is variable depending on the lowest possible system voltage. Set this value just above what the system requires for the lowest possible voltage.

Depleted Voltage Time

See *Depleted Voltage*. The **Voltage** must be equal to or below the Depleted Voltage for at least this time (*Depleted Voltage Time*) for the bq20z80 to register a [XCHGLV] fault in **Charging Status**. If set to 0, then *Depleted Voltage* function is completely disabled.

Normal Setting: The default value for this register is 2 seconds. Ensure that this register is set to prevent false readings or spiked load currents from triggering a premature fault. With high current loads, be sure that this register is set short enough to prevent the system from detecting a low voltage since voltage is normally dropping very rapidly at this level.

Depleted Recovery

When the voltage as measured by **Voltage**, rises to or above this value while charging then the [OCHGLV] flag is cleared in **Charging Status**. If the discharge FET was turned off, it returns to the on state.

Normal Setting: This register should be set at least several hundred millivolts higher than the *Depleted Voltage* to ensure hysteresis through this transition.

Over Charge Capacity

Over Charge Capacity is detected in a two-step process. First the battery must be charged to the point where Remaining Capacity reaches **FCC (Full Charge Capacity)**. Then any charge applied after this point is still measured but not displayed by the bq20z80. When this charge as measured by the bq20z80 reaches a threshold as defined by **FCC + Over Charge Capacity**, then the bq20z80 goes into a charging fault condition. The [OC] in **Charging Status** is set. **Charging Voltage** and **Charging Current** are both set to 0. If [OC] set in *Charge Fault Cfg*, then the Charge FET is turned off.

Normal Setting: This register is application dependent but a good example is 100 to 300 mAh for each cell in parallel. Too small of a value could force false detections, and too large a value could damage the cells if normal charge termination methods fail.

Over Charge Recovery

There are three recovery methods for the bq20z80.

1. The first involves *Over Charge Recover* and only happens if [NR] in *Operation Cfg B* is set. With this setting, the bq20z80 recovers from an overcharged condition with a continuous discharge of "Over Charge Recovery" mAHs.
2. With [NR] cleared in *Operation Cfg B*, the bq20z80 recovers from the overcharge fault with a pack removal and reinsertion ($\overline{\text{PRES}}$ transition).
3. The third recovery happens when **RSOC** falls below the *FC Clear %*. This recovery also is the only one that returns **Charging Voltage** and **Charging Current** to normal.

Normal Setting: This value is normally small. Typically around 2 mAH. Its only purpose is to ensure small discharge spikes or false discharge detections do not clear the condition prematurely.

FC-MTO

If charging current is greater than *Chg Current Threshold* and [FCHG] is set in **Charging Status** for *FC-MTO* time in seconds, then the bq20z80 sets [FC-MTO] (fast time mode timeout) in **Charging Status**, **Charging Voltage** and **Charging Current** are set to 0, [TCA] is set in **Battery Status**, and if [FCMTO] is set in *Charge Fault Cfg* then the Charge FET is turned off. If charging is interrupted ([DSG] in **Battery Status** sets) and an *Over Charging Curr Recov* amount of discharge is detected anytime during the charging process prior to *FC-MTO* timer expiring, then the *FC-MTO* timer is reset and starts counting from 0. The bq20z80 recovers from an *FC-MTO* fault with the following conditions:

1. The fault condition is cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*.
2. If Current falls below *Dsg Current Threshold*
If *FC-MTO* is 0, then this function is disabled.

Normal Settings: The purpose of this register is another form of charge protection. If this timer has timed out, then something has gone wrong and the battery is taking too long to charge. The default setting for this register is 10800 seconds. This may be short for some applications. Be sure and give plenty of time for all possible scenarios. Smaller charge currents may require longer settings. It is also important to note that as a battery ages, the charge time increases due to increased impedance. Setting this value short limits the capacity of aged cells.

PC-MTO

If charging current is greater than *Chg Current Threshold*, and [PCHG] is set in **Charging Status** for *PC-MTO* time in seconds, then the bq20z80 sets [PC-MTO] (precharge time mode timeout) in **Charging Status**, **Charging Voltage** and **Charging Current** are set to 0, [TCA] is set in **Charging Status**, and if [PCMTO] is set in *Charge Fault Cfg* then the Charge FET/Pre-Charge FET is turned off. If charging is interrupted ([DSG] in **Charging Status** sets) and an *Over Charging Curr Recov* amount of discharge is detected anytime during the charging process prior to *FC-MTO* timer expiring, then the *FC-MTO* timer is reset and starts counting from 0. The bq20z80 recovers from a *PC-MTO* fault with the following conditions:

1. The fault condition is cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*.
2. If **Current** falls below *Dsg Current Threshold*
If *PC-MTO* is 0 then this function is disabled.

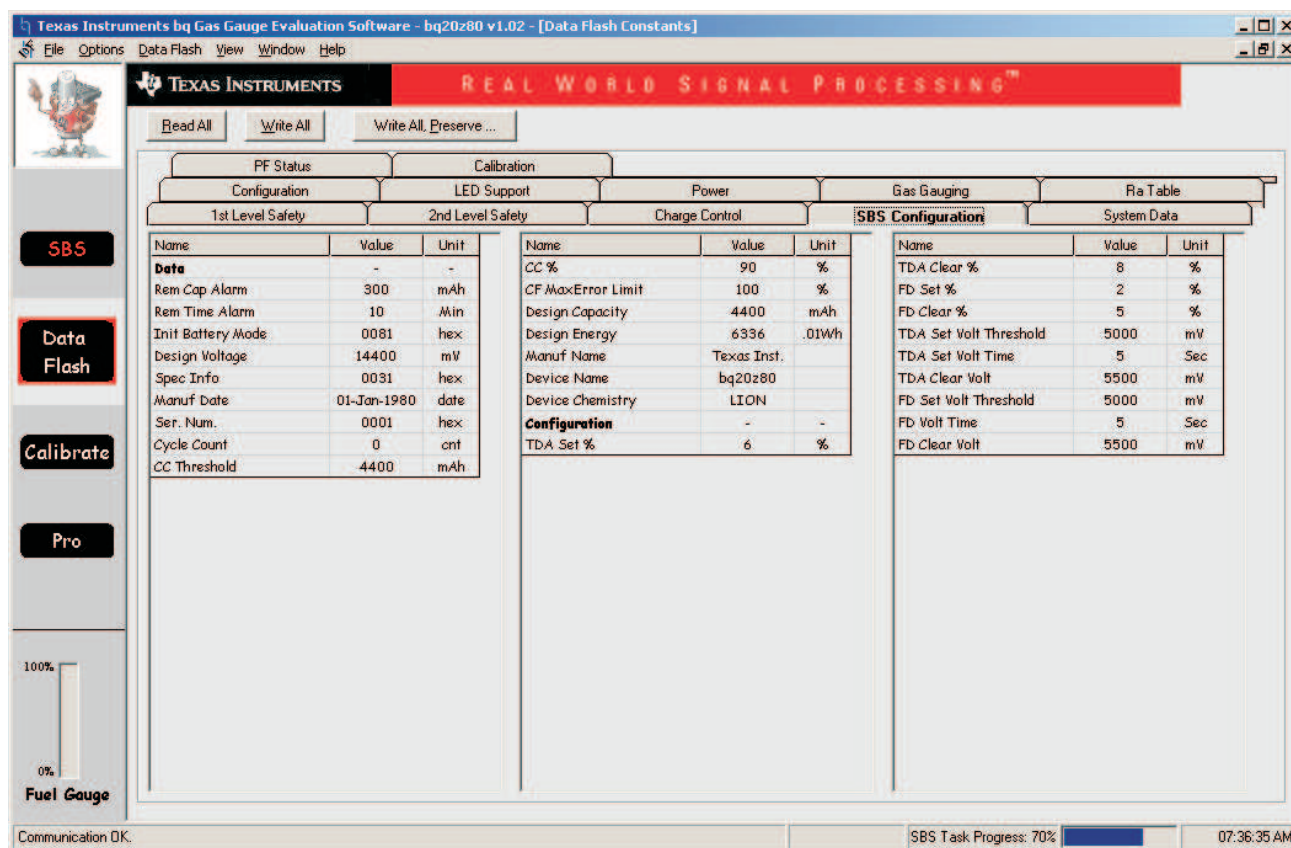
Normal Settings: The purpose of this register is another form of charge protection. If this timer has timed out, then something has gone wrong and the battery is taking too long to charge. The default setting for this register is 3600 seconds. This is good for most applications. Smaller charge currents may require longer settings.

Charge Fault Configuration

—	—	PCMTO	FCMTO	OCHGV	OCHGI	OC	CS_XCHGLV
---	---	-------	-------	-------	-------	----	-----------

- PCMTO: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *PC-MTO* fault condition occurs.
Normal Setting: Default is 0 (disabled)
- FCMTO: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *FC-MTO* fault condition occurs.
Normal Setting: Default is 0 (disabled)
- OCHGV: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *Over Charging Voltage* fault condition occurs.
Normal Setting: Default is 0 (disabled)
- OCHGI: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *Over Charging Current* fault condition occurs.
Normal Setting: Default is 0 (disabled)
- OC: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *Over Charge* fault condition occurs.
Normal Setting: Default is 0 (disabled)
- CS_XCHGLV: If set, then the discharge FET is turned off when a Depleted Voltage fault condition occurs.
Normal Setting: Default is 0 (disabled)

5 SBS Configuration



5.1 Data

Rem Cap Alarm

When the **Remaining Capacity** falls below this value, [RTA] is set in **Battery Status**.

Normal Setting: About 10% of the **Full Charge Capacity**. This value is programmed into **RemainingCapacityAlarm** on device initialization

Rem Time Alarm

When the average time to empty falls below this value, then the [RTA] flag is set in **Battery Status**.

Normal Setting: Approximately 10 minutes. This value is programmed into **RemainingTimeAlarm** on device initialization.

Init Battery Mode

This is the default value loaded into **Battery Mode** on all resets, and when the bq20z80 wakes from sleep. The primary purpose of having an initial value for this register is to enable milliwatt mode whenever the bq20z80 resets or wakes up from sleep.

Normal Setting: In most applications, this register should be 0x0081. If the application requires the bq20z80 to wake in mW mode, then this value can be set to 0x8081. Care should be taken with this setting; however, because the **Battery Mode** register is writable even when the bq20z80 is sealed. The mW mode bit can be accidentally written to a 0.

Design Voltage

This is the theoretical nominal voltage of the battery pack. This value is used in **ATRATE** calculations and milliWatt mode (**Battery Mode** MSByte bit 7).

Normal Setting: This varies by cell manufacturer, but Li-Ion is normally about 3.6-V per cell. See the cell manufacturer data sheet for the exact numbers. This value is programmed into **DesignVoltage** on device initialization.

Spec Info

This performs two purposes. The high byte has the current and voltage multipliers. The bq20z80 does not require any multiplier, so use 0x00. The low byte is the SBS specification revision. See the SBS Implementers Forum web page for more information (<http://www.sbs-forum.org/specs/index.html>).

Normal Setting: 0x0031 for SBS specification v1.1 with PEC error checking, or 0x0021 for SBS specification V1.1 without PEC error checking.

Mfg Date

This is the date of manufacture. It is stored in the Data Flash in packed format. All bqEV Software and bqMTester both accept input of this date in standard date format so the packed format does not need to be used input. It is then translated by the software to packed format. This data does not affect the operation, nor is it used by the part in any way.

Ser Num

This is a 16 bit serial number that does not affect the operation nor is it used by the part in any way. It is normally used for battery identification.

Cycle Count(CC)

There are two methods to increment *Cycle Count*:

1. If [CCT] is set in *Operation Cfg B*, then this CC% is used to increment *Cycle Count*. When the bq20z80 accumulates enough discharge capacity equal to $(CC\% \times \text{Full Charge Capacity})$, then it increments *Cycle Count* by 1. If at any time $(CC\% \times \text{Full Charge Capacity})$ is less than *Cycle Count Threshold*, then the *Cycle Count Threshold* is used to increment *Cycle Count*.
2. If [CCT] is cleared in *Operation Cfg B*, then *Cycle Count Threshold* is always be used to increment *Cycle Count*. When the bq20z80 accumulates enough discharge capacity equal to the *Cycle Count Threshold*, then it increments *Cycle Count* by 1.

This discharge capacity used by either of these methods does not have to be consecutive. The internal register that accumulates the discharge is not cleared at any time except when the internal accumulating register equals the *Cycle Count Threshold* or CC % depending on [CCT]. Then *Cycle Count* is incremented. Every increment of *Cycle Count* between QMAX updates increments **MaxErr** by 0.05%. It takes 20 increments of *Cycle Count* to increment **MaxErr** by 1%, so that it is visible in the SBS register.

Normal Setting: This should be set to 0.

Cycle Count Threshold

If [CCT] is cleared in *Operation Cfg B*, then this value is always used to increment *Cycle Count*. When the bq20z80 accumulates enough discharge capacity equal to the *Cycle Count Threshold*, then it increments *Cycle Count* by 1. This discharge capacity does not have to be consecutive. The internal register that accumulates the discharge is not cleared at any time except when the internal accumulating register equals the *Cycle Count Threshold*, and increments *Cycle Count*. If [CCT] is set, then see *CC%*

Normal Setting: This is normally set to about 80% of the *Design Capacity*.

CC%

If [CCT] is set in *Operation Cfg B*, then this value is used to increment *Cycle Count*. When the bq20z80 accumulates enough discharge capacity equal to $(CC\% \times FCC)$, then it increments *Cycle Count* by 1. If at any time $(CC\% \times \text{Full Charge Capacity})$ is less than *Cycle Count Threshold*, then the *Cycle Count Threshold* is used to increment *Cycle Count*. This discharge capacity does not have to be consecutive. The internal register that accumulates the discharge is not cleared at any time except when the internal accumulating register equals the $(CC\% \times FCC)$, and increments *Cycle Count*. If [CCT] is clear, then see *Cycle Count Threshold*.

Normal Setting: This is normally set to 80–90%. This can be set closer to *FCC* than the *Cycle Count Threshold* method because it tracks with *FCC* as it decreases with age. This keeps cycle count tracking closely with each discharge cycle as the battery ages. Ensure that *Cycle Count Threshold* has a meaningful value even if *CC%* is used because the *Cycle Count Threshold* is used if $(CC\% \times \text{Full Charge Capacity})$ is less than *Cycle Count Threshold*.

CF Max Error Limit

The bq20z80 forces [CF] to be set in **Battery Mode** if *MaxErr* goes above the value stored in this register. This value is used to give an alternate method for setting the [CF] flag in **Battery Mode**, other than the impedance track algorithm. The [CF] flag is a condition request flag indicating the battery would like a full charge/discharge cycle, and rarely is set by impedance track because accurate capacity measurements are always updated.

Normal Setting: This register is normally set to 100 and is in units of %.

Design Capacity

Design Capacity is the data flash location that is reported in the **Design Capacity** register when [CapM] is clear in **Battery Mode**. If [CapM] is set in **Battery Mode**, then *Design Energy* is reported in **Design Capacity**. This value is used also for the *ASOC* calculation by the bq20z80 if [CapM] is cleared in **Battery Mode**.

Normal Setting: This value should be set based on the application battery specification. See the battery manufacturer data sheet.

Design Energy

Design Energy is the data flash location that is reported in the **Design Capacity** register if [CapM] is set in **Battery Mode**. If [CapM] is clear in **Battery Mode**, then *Design Capacity* is reported in *Design Capacity*. This value is used also for the *ASOC* calculation by the bq20z80 if [CapM] is set in **Battery Mode**.

Normal Setting: This value is be set based on the application battery specification. See the battery manufacturer data sheet. At higher rates of discharge, energy is less, so referring to discharge data similar to the typical rate of the user's application is important to obtain a meaningful value.

Manuf Name

String data that can be a maximum of 11 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x20.

Device Name

String data that can be a maximum of 7 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x21.

Device Chemistry

String data that can be a maximum of 4 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x22.

5.2 Configuration

These are alternative methods for setting and clearing [TDA] and [FD] in **Battery Status**. They are in addition to traditional methods or fault conditions explained in other areas of this document.

TDA Set %

If set to a value between 0 and 100 then when **RSOC** falls to or below this value, then [TDA] in **Battery Status** is set. If set to (-)1, then this function is disabled. *TDA Set Volt Threshold* is not affected by this register. They are completely independent. Any fault condition that specifies setting [TDA] is completely unaffected by this register.

Normal Setting: This is user preference. This is the threshold that the bq20z80 requests that discharge be halted because the battery is nearing depletion. If used, it is normally set around 6%. Be sure that if *TDA Clear %* is used, then this should be used as well. They only work together.

TDA Clear %

If set to a value between 0 and 100 then when **RSOC** rises to or above this value after being set by *TDA Set %*, then [TDA] in **Battery Status** is cleared. This register can only be used to clear [TDA] if it was set by *TDA Set %*. If set to (-)1 then this function is disabled. *TDA Clear Volt Threshold* is not affected by this register. They are completely independent.

Normal Setting: This is user preference. If used it is normally set around 8%. Be sure that if *TDA Set %* is used then this should be used as well. They only work together.

FD Set %

If set to a value between 0 and 100 then when **RSOC** falls to or below this value then [FD] in **Battery Status** is set. If set to (-)1 then this function is disabled. *FD Set Volt Threshold* is not affected by this register. They are completely independent. Any fault condition that specifies setting [FD] is completely unaffected by this register.

Normal Setting: This is user preference. This is a stronger request than TDA. The battery is presumed dead at this point. If used it is normally set around 2%. Be sure that if *FD Clear %* is used then this should be used as well.

FD Clear %

If set to a value between 0 and 100 then when **RSOC** rises to or above this value after being set by *FD Set %*, then [FD] in **Battery Status** is cleared. If set to (-)1 then this function is disabled. *FD Clear Volt Threshold* is not affected by this register. They are completely independent.

Normal Setting: This is user preference. If used it is normally set around 5%. If *FD Set %* is used, then this should be used as well. They only work together.

TDA Set Volt Threshold

When battery voltage as measured by **Voltage** falls to or below the *TDA Set Volt Threshold* value for *TDA Set Volt Time* seconds, then [TDA] in **Battery Status** is set. This works completely independent of *TDA Set %*. Any fault condition that specifies setting [TDA] is completely unaffected by this register.

Normal Setting: This is user preference but should be a voltage that the battery is at under normal loads at around 6% **RSOC**.

TDA Set Volt Time

See *TDA Set Volt*. This is the time that the battery voltage must be equal to or below *TDA Set Volt Threshold* before [TDA] is set in **Battery Status**.

Normal Setting: This is normally set to 5 seconds but depends on the application.

TDA Clear Volt Threshold

When battery voltage (as measured by **Voltage**) rises to or above this value, then [TDA] in **Battery Status** is cleared. [TDA] is only cleared with this threshold if it was set by *TDA Set Volt* criteria, and it is not cleared if it was set by any other methods.

Normal Setting: This is user preference but should be a voltage that the battery is at under normal loads at around 8% **RSOC**.

FD Set Volt Threshold

When battery voltage as measured by **Voltage** falls to or below the *FD Set Volt Threshold* value for *FD Set Volt Time* seconds, then [FD] in **Battery Status** is set. This register works completely independent of *FD Set %*. Any fault condition that specifies setting [FD] is completely unaffected by this register.

Normal Setting: This is user preference but should be a voltage that the battery is at under normal loads at around 2% **RSOC**.

FD Set Volt Time

See *FD Set Volt*. This is the time that the battery voltage must be equal to or below *FD Set Volt Threshold* before [FD] is set in **Battery Status**.

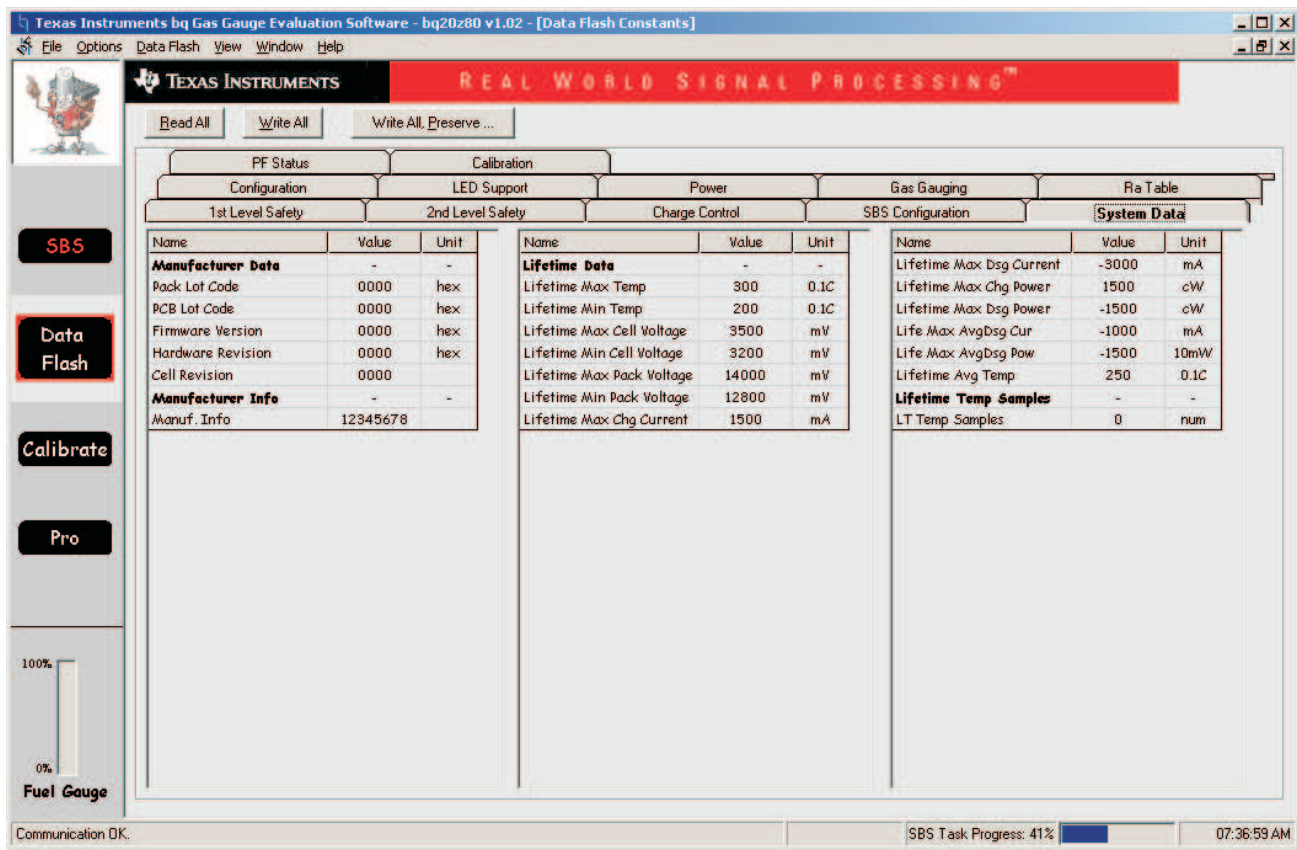
Normal Setting: This is normally set to 5 seconds but depends on the application.

FD Clear Volt Threshold

When battery voltage as measured by **Voltage** rises to or above this value, then [FD] in **Battery Status** is cleared. [FD] is cleared from this threshold only if it was set by *FD Set Volt* criteria.

Normal Setting: This is user preference, but it must be a voltage that the battery is at under normal loads at around 5% **RSOC**.

6 System Data



Name	Value	Unit
Manufacturer Data		
Pack Lot Code	0000	hex
PCB Lot Code	0000	hex
Firmware Version	0000	hex
Hardware Revision	0000	hex
Cell Revision	0000	
Manufacturer Info		
Manuf. Info	12345678	
Lifetime Data		
Lifetime Max Temp	300	0.1C
Lifetime Min Temp	200	0.1C
Lifetime Max Cell Voltage	3500	mV
Lifetime Min Cell Voltage	3200	mV
Lifetime Max Pack Voltage	14000	mV
Lifetime Min Pack Voltage	12800	mV
Lifetime Max Chg Current	1500	mA
System Data		
Lifetime Max Dsg Current	-3000	mA
Lifetime Max Chg Power	1500	cW
Lifetime Max Dsg Power	-1500	cW
Life Max AvgDsg Cur	-1000	mA
Life Max AvgDsg Pow	-1500	10mW
Lifetime Avg Temp	250	0.1C
Lifetime Temp Samples		
LT Temp Samples	0	num

6.1 Manufacturer Data

Pack Lot Code

This is a 16 bit value that does not affect operation nor is it used by the part in any way.

Normal Setting: The most common use of this register is as an extension to the *Serial Number* as a form of pack identification. It is only readable via **Manufacturer Data** (0x23) string read.

PCB Lot Code

This is a 16 bit value that does not affect operation nor is it used by the part in any way.

Normal Setting: The most common use of this register is as an extension to the *Serial Number* as a form of pack identification. It is only readable via **Manufacturer Data** (0x23) string read.

Firmware Version

This is a 16 bit value that does not affect operation nor is it used by the part in any way. It is intended as a firmware revision however it is not protected so it is not reliable. Use **Manufacturing Access Commands** to get a reliable firmware version of the bq20z80.

Normal Setting: This can be used for any user data. It is only readable via **Manufacturer Data** (0x23) string read.

Hardware Revision

This is a 16 bit value that does not affect operation nor is it used by the part in any way. It is intended as a IC hardware revision; however, it is not protected so it is not reliable. Use **Manufacturing Access Commands** to get a reliable firmware version of the bq20z80.

Normal Setting: This can be used for any user data. It is only readable via **Manufacturer Data** (0x23) string read.

Cell Revision

This is a 16 bit value that does not affect operation nor is it used by the part in any way.

Normal Setting: This can be used for any user data. It is only readable via **Manufacturer Data** (0x23) string read.

6.2 Manufacturer Info

Manuf. Info

This is string data that can be any user data. It can be a maximum of 8 characters.

Normal Setting: Can be used for any user data.

6.3 Lifetime Data

Lifetime Max Temp

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum temperature as measured by **Temperature** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Temp* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Temp* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Max Temp* by at least 1°C
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Min Temp

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the minimum temperature as measured by **Temperature** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Min Temp* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Min Temp* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Min Temp* by at least 1°C
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Cell Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum cell voltage as measured by **Cell Voltage (Max)** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Cell Voltage* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Cell Voltage* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Max Cell Voltage* by at least 25 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Min Cell Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the minimum cell voltage as measured by **Cell Voltage (Min)** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Min Cell Voltage* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Min Cell Voltage* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Min Cell Voltage* by at least 25 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Pack Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum pack voltage as measured by **Voltage** is updated continuously in a reserved RAM location. To prevent flash wear out, this RAM only updates with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Pack Voltage* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Max Pack Voltage* by at least 25 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Min Pack Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the minimum cell voltage as measured by **Voltage** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Min Pack Voltage* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Min Pack Voltage* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Min Pack Voltage* by at least 25 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Chg Current

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum current in the charge direction as measured by **Average Current** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Chg Current* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Chg Current* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Max Chg Current* by at least 100 mA.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Dsg Current

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum current in the discharge direction as measured by **Average Current** is updated continuously in a reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Dsg Current* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is less than (–) *Lifetime Max Chg Current* for 60 seconds
2. If the internal RAM location is less than (–) *Lifetime Max Chg Current* by at least 100 mA.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Chg Pwr

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum power in the charge direction as measured by a reserved continually updated average power register (uses **Voltage** × **Current** in an internal averaging algorithm) is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Chg Pwr* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Chg Power* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Max Chg Power* by at least 100 in units of 100 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Dsg Pwr

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum power in the discharge direction as measured by a reserved continually updated average power register (uses **Voltage** × **Current** in an internal averaging algorithm) is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Dsg Power* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is less than (–) *Lifetime Max Chg Current* for 60 seconds.
2. If the internal RAM location is less than (–) *Lifetime Max Chg Current* by at least 100 in units of 100 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Life Max Avg Dsg Pwr

Power is averaged over every discharge cycle. Every discharge cycle an internal unaccessible RAM Register (LastAveragePower) is updated with this average power. The maximum power in the discharge direction as measured by this last average discharge power register (uses **Voltage** × **Current** in an internal averaging algorithm) is updated continuously in a lifetime data reserved RAM location. When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), the *Life Max Avg Dsg Pwr* data flash register is updated from this RAM location but only with any one of the following 3 conditions:

1. Whenever the internal RAM location is **less** than (–) *Lifetime Max Avg Dsg Power* for 60 seconds.
2. If the internal RAM location is **less** than (–) *Lifetime Max Avg Dsg Power* by at least 100 in units of 100 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Life Min Avg Dsg Pwr

Power is averaged over every discharge cycle. Every discharge cycle an internal unaccessible RAM Register (LastAveragePower) is updated with this average power. The minimum power in the discharge direction as measured by this last average discharge power register (uses **Voltage** × **Current** in an internal averaging algorithm) is updated continuously in a lifetime data reserved RAM location. When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), the *Life Min Avg Dsg Pwr* data flash register is updated from this RAM location but only with any one of the following 3 conditions:

1. Whenever the internal RAM location is **greater** than (–) *Lifetime Min Avg Dsg Power* for 60 seconds.
2. If the internal RAM location is **greater** than (–) *Lifetime Min Avg Dsg Power* by at least 100 in units of 100 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Avg Temp

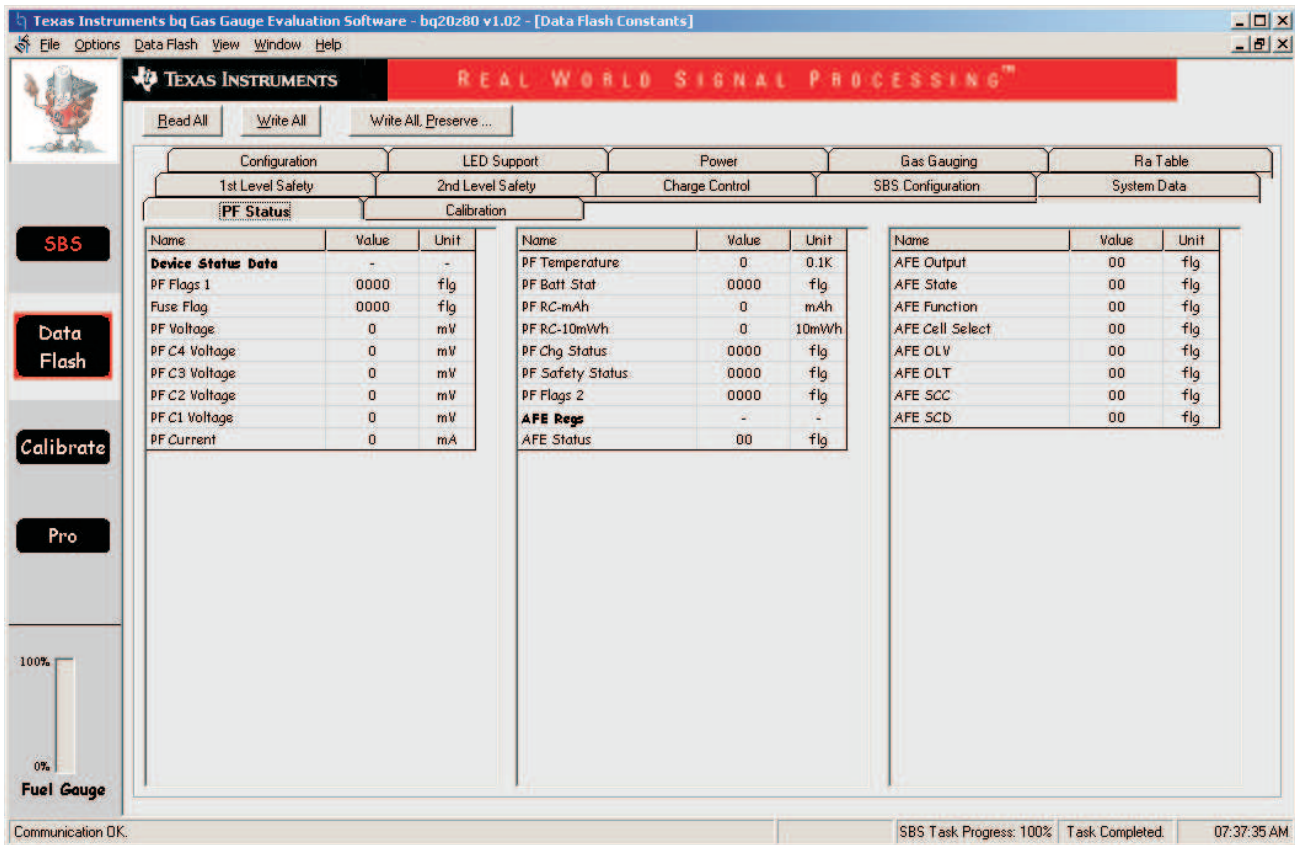
Temperature is averaged over the entire life of the battery. The temperature is sampled from the **Temperature** register every 1/16th of an hour. Then summed given the last Temperature Sum (**Temperature** + Previous **Temperature** Sum) as updated the previous 1/16th of an hour sample and then divided by **LT Temp Samples**. This is then updated continuously in a lifetime data reserved RAM location. To prevent flash wear out, this RAM only updates to data flash when any other Lifetime Data locations update to data flash after meeting their update criteria. Impedance Track must be enabled ([QEN] set in Operation Status) for this data flash update to occur.

6.4 Lifetime Temp Samples

LT Temp Samples

LT Temp Samples are used to compute the **Lifetime Avg Temp**. Temperature is averaged over the entire life of the battery. The temperature is sampled from the **Temperature** register every 1/16th of an hour, then summed given the last Temperature Sum (**Temperature** + Previous **Temperature** Sum) as updated the previous 1/16th of an hour sample and then divided by **LT Temp Samples**. **LT Temp Samples** is then incremented by 1. **LT Temp Samples** is updated continuously in a lifetime data reserved RAM location. To prevent flash wear out, this RAM location only updates when any other Lifetime Data location updates to data flash after meeting their update criteria. Impedance Track™ must be enabled ([QEN] set in Operation Status) for this data flash update to occur.

7 PF Status



The screenshot shows the Texas Instruments bq Gas Gauge Evaluation Software interface. The main window displays the 'PF Status' tab, which is part of the 'Data Flash' section. The interface includes a menu bar (File, Options, Data Flash, View, Window, Help) and a toolbar with buttons for 'Read All', 'Write All', and 'Write All, Preserve...'. The main content area is divided into three columns, each displaying a table of parameters and their values.

Name	Value	Unit
Device Status Data		
PF Flags 1	0000	flg
Fuse Flag	0000	flg
PF Voltage	0	mV
PF C4 Voltage	0	mV
PF C3 Voltage	0	mV
PF C2 Voltage	0	mV
PF C1 Voltage	0	mV
PF Current	0	mA

Name	Value	Unit
PF Temperature	0	0.1K
PF Batt Stat	0000	flg
PF RC-mAh	0	mAh
PF RC-10mWh	0	10mWh
PF Chg Status	0000	flg
PF Safety Status	0000	flg
PF Flags 2	0000	flg
AFE Regs		
AFE Status	00	flg

Name	Value	Unit
AFE Output	00	flg
AFE State	00	flg
AFE Function	00	flg
AFE Cell Select	00	flg
AFE OLV	00	flg
AFE OLT	00	flg
AFE SCC	00	flg
AFE SCD	00	flg

At the bottom of the window, there is a status bar showing 'Communication OK', 'SBS Task Progress: 100%', 'Task Completed', and the time '07:37:35 AM'.

There is no configuration or settings required for the PF Status Class. The entire PF Status class should all be zeros for every register. This class is intended only for reporting failure information to the factory and Texas Instruments. In fact, it only reports any information with catastrophic failures or during development time as a tool to help with configuration or layout issues.

7.1 Device Status Data

PF Flags 1

This location indicates all the causes of permanent failures that have occurred from the time the bq20z80 was last programmed with new firmware or the last time this register was cleared. It is important to understand that more than one fault can be recorded here if multiple faults have occurred. *PF Flags 1* bit locations and definitions correspond to **PF Status**. If the corresponding bit in *PF Flags 1* is enabled in the *Permanent Fail Cfg* register then the bq20z80 attempts to blow the fuse in addition to record the permanent failure in the *PF Flags 1* register. This register is cleared (set to 0x0000) if the manufacturers access clear PF command is sent to the bq20z80 (See the bq20z80 data sheet). This is the only register in the data flash which ignores the disabled data flash writing setting when a permanent failure occurs. (See *Permanent Fail Cfg*)

FBF	–	–	SOPT	S OCD	SOCC	AFE_P	AFE_C
DFF	DFETF	CFETF	CIM	SOTD	SOTC	SOV	PFIN

- **FBF**: Set if *Fuse Fail Limit* fault has occurred and the function is enabled. If the *Fuse Flag* has been set to 0x3672 (*SAFE* pin is driven high and *SAFE* pin is driven low on the bq20z80) and the current as measured by **Current** still exists which is greater than *Fuse Fail Limit* in milliamps, or less than a (–) *Fuse Fail Limit* for *Fuse Fail Time*, then the this flag is set. See *Fuse Fail Limit*.
- **SOPT**: Set if a Safety Open Thermistor Fault has occurred and the function is enabled. If *Open Thermistor Time* is set to 0, then this function is disabled. If [XSOPT] is set in *Permanent Fail Cfg* then 0x3672 is written to the *Fuse Flag*. The *SAFE* pin is driven high and *SAFE* pin is driven low on the bq20z80 (See *SOC Dsg*).
- **S OCD**: Set if a Safety Over Current Discharge Fault has occurred and the function is enabled. If *SOC Dsg Time* is set to 0, then this function is disabled. If [XS OCD] is set in *Permanent Fail Cfg* then 0x3672 is written to the *Fuse Flag*. The *SAFE* pin is driven high and *SAFE* pin is driven low on the bq20z80 (See *SOC Dsg*).
- **SOCC**: Set if a Safety Over Current Charge Fault has occurred and the function is enabled. If *SOC Chg Time* is set to 0, then this function is disabled. If [XS OCC] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The *SAFE* pin is driven high and *SAFE* pin is driven low on the bq20z80 (See *SOC Chg*).
- **AFE_P**: Set if a Periodic AFE Check Fault has occurred and the function is enabled. If *AFE Check Time* is set to 0, then this function is disabled. If [XAFE_P] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The *SAFE* pin is driven high and *SAFE* pin is driven low on the bq20z80 (See *AFE Check Time*).
- **AFE_C**: Set if an AFE Communication Fault has occurred. If *AFE Fail Limit* is set to 0, then this function is disabled. If [XAFE_C] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The *SAFE* pin is driven high and *SAFE* pin is driven low on the bq20z80 (See *AFE Fail Limit*).
- **DFF**: The bq20z80 verifies all data flash writes and will set [DFF] if a Data Flash Verify Fault has occurred Only the setting of [DFF] can be disabled. If [XDFF] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The *SAFE* pin is driven high and *SAFE* pin is driven low on the bq20z80.
- **DFETF**: Set if a Discharge FET Fault has occurred and the function is enabled. If *FET Fail Time* is set to 0, then that function is disabled. If [XDFETF] is set in *Permanent Fail Cfg* then 0x3672 is written to the *Fuse Flag*. The *SAFE* pin is driven high and *SAFE* pin is driven low on the bq20z80 (See *FET Fail Time*).
- **CFETF**: Set if a Charge FET Fault has occurred and the function is enabled. If *FET Fail Time* is set to 0, then that function is disabled. If [XCFETF] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The *SAFE* pin is driven high and *SAFE* pin is driven low on the bq20z80 (See *FET Fail Time*).
- **CIM**: Set if a Cell Imbalance Fault has occurred and the function is enabled. If *Battery Rest Time* is set to 0, then that function is disabled. If [XCIM] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The *SAFE* pin is driven high and *SAFE* pin is driven low on the bq20z80(See *Battery Rest Time*).
- **SOTD**: Set if a Safety Over Temperature Discharge Fault has occurred and the function is enabled. If *SOT Dsg Time* is set to 0, then this function is disabled. if [XSOTD] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The *SAFE* pin is driven high and *SAFE* pin is driven low on the

bq20z80 (See *SOT Dsg*).

- **SOTC**: Set if a Safety Over Temperature Charge Fault has occurred and the function is enabled. If *SOT Chg Time* is set to 0, then this function is disabled. If [XSOTC] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The *SAFE* pin is driven high and *SAFE* pin is driven low on the bq20z80 (See *SOT Chg*).
- **SOV**: Set if a Safety Over Voltage Threshold Fault has occurred and the function is enabled. If *SOV Time* is set to 0, then this function is disabled. If [XSOV] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The *SAFE* pin is driven high and *SAFE* pin is driven low on the bq20z80 (See *SOV Threshold*).
- **PFIN**: The bq20z80 monitors the PFIN line. When the PFIN line goes low for *PFIN Detect Time*, then the bq20z80 attempts to report a PFIN Fault if the function is enabled. If *PFIN Detect Time* is set to 0 then this function is disabled. If [XPFIN] is set in *Permanent Fail Cfg* then 0x3672 is written to the *Fuse Flag*. The *SAFE* pin is driven high and *SAFE* pin is driven low on the bq20z80 (See *PFIN Detect Time*).

Fuse Flag

This is set to 0x3672 when the bq20z80 sets any permanent failure flags in **PF Status**. Otherwise this register is 0x0000. This register is cleared (set to 0x0000) if the manufacturers access clear PF command is sent to the bq20z80. See the bq20z80 Technical Reference Manual ([SLUU241](#)) for more information on clearing permanent failures.

PF Voltage

The **Voltage** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF C1 Voltage

The **Cell Voltage 1** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF C2 Voltage

The **Cell Voltage 2** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF C3 Voltage

The **Cell Voltage 3** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF C4 Voltage

The **Cell Voltage 4** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Current

The **Current** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Temperature

The **Temperature** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Batt Stat

The **Battery Status** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF RC (mAh)

The **Remaining Capacity** register in mAh is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF RC (10mWh)

The **Remaining Capacity** register in mWh is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Charging Status

The **Charging Status** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Safety Status

The **Safety Status** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Flags 2

This register reports the first permanent failure that occurred from the time the bq20z80 was last programmed with new firmware. The difference between this register and PF Flags 1 is that this register only records one failure and it is the first one in a possible series of failures. This method gives a better chance to learn what could have caused a whole series of failures by knowing what the first failure was.

7.2 AFE Regs

All AFE registers are captured at the time that the most recent permanent failure occurred. This subclass should always be 0 unless a permanent failure has occurred.

AFE Status

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE Output

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE State

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE Function

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE Cell Select

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE OLV

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE OLT

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

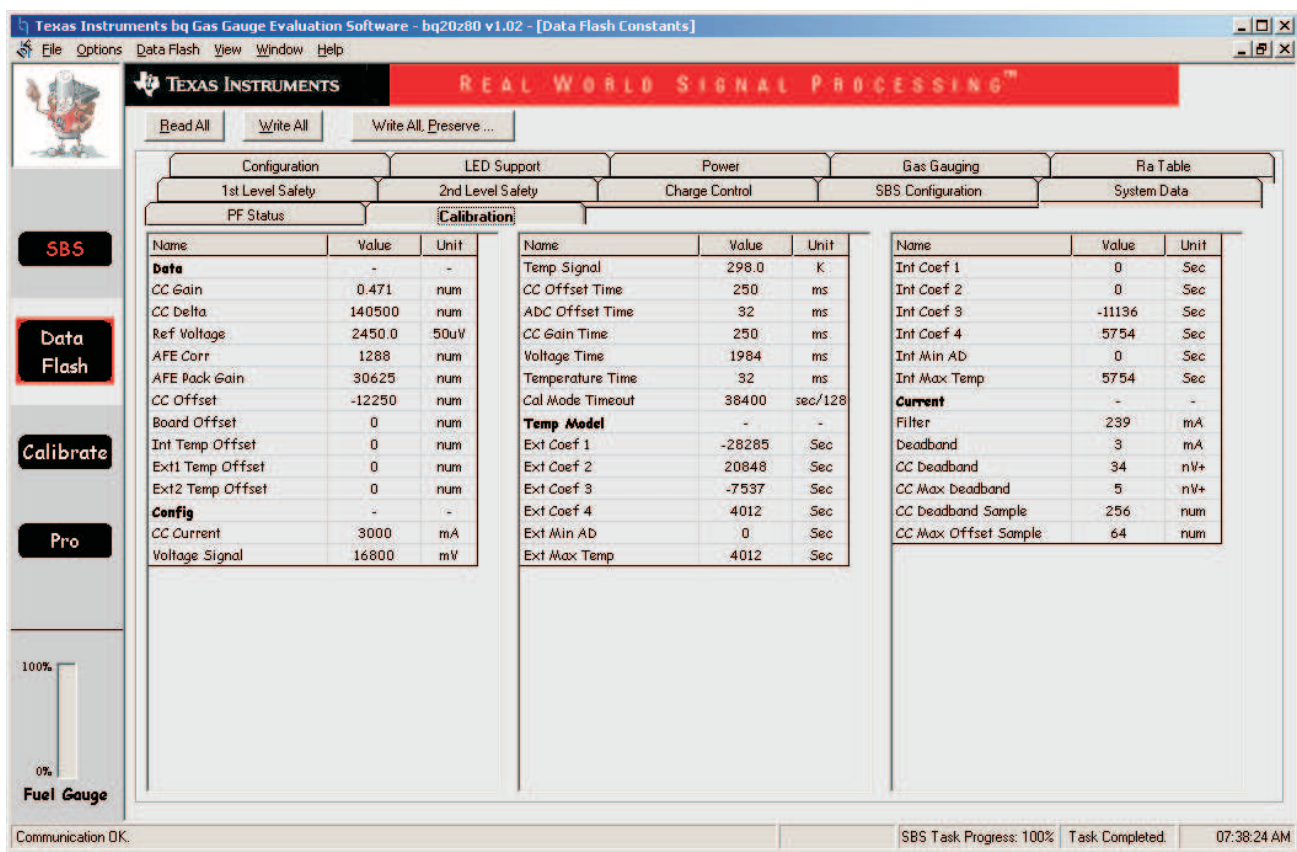
AFE SCC

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE SCD

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

8 Calibration



The screenshot shows the Texas Instruments bq Gas Gauge Evaluation Software interface. The main window is titled "Texas Instruments bq Gas Gauge Evaluation Software - bq20z80 v1.02 - [Data Flash Constants]". The interface includes a menu bar (File, Options, Data Flash, View, Window, Help) and a toolbar with buttons for Read All, Write All, and Write All, Preserve... The main area is divided into several tabs: Configuration, LED Support, Power, Gas Gauging, and Ra Table. Under the Configuration tab, there are sub-tabs for 1st Level Safety, 2nd Level Safety, Charge Control, SBS Configuration, and System Data. The Calibration tab is currently selected, showing three tables of data:

Name	Value	Unit
Data		
CC Gain	0.471	num
CC Delta	140500	num
Ref Voltage	2450.0	50uV
AFE Corr	1288	num
AFE Pack Gain	30625	num
CC Offset	-12250	num
Board Offset	0	num
Int Temp Offset	0	num
Ext1 Temp Offset	0	num
Ext2 Temp Offset	0	num
Config		
CC Current	3000	mA
Voltage Signal	16800	mV

Name	Value	Unit
Temp Signal	298.0	K
CC Offset Time	250	ms
ADC Offset Time	32	ms
CC Gain Time	250	ms
Voltage Time	1984	ms
Temperature Time	32	ms
Cal Mode Timeout	38400	sec/128
Temp Model		
Ext Coef 1	-28285	Sec
Ext Coef 2	20848	Sec
Ext Coef 3	-7537	Sec
Ext Coef 4	4012	Sec
Ext Min AD	0	Sec
Ext Max Temp	4012	Sec

Name	Value	Unit
Int Coef 1	0	Sec
Int Coef 2	0	Sec
Int Coef 3	-11136	Sec
Int Coef 4	5754	Sec
Int Min AD	0	Sec
Int Max Temp	5754	Sec
Current		
Filter	239	mA
Deadband	3	mA
CC Deadband	34	nV+
CC Max Deadband	5	nV+
CC Deadband Sample	256	num
CC Max Offset Sample	64	num

The interface also includes a Fuel Gauge section on the left with a 100% to 0% scale and a "Fuel Gauge" label. At the bottom, there is a status bar showing "Communication OK", "SBS Task Progress: 100%", "Task Completed", and the time "07:38:24 AM".

8.1 Data

Most of these values should never need to be modified by the user. They should only be modified by the Calibration commands in Calibration mode as explained in the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note [SLUA355A](#).

CC Gain

This is the gain factor for calibrating out Sense Resistor, Trace, and internal Coulomb Counter (integrating ADC Delta Sigma) errors. It is used in the algorithm that reports **Current**. The difference between **CC Gain** and **CC Delta** is that the algorithm that reports Current cancels out the time base since **Current** does not have a time component (it reports in mA) and CC Delta requires a time base for reporting **Remaining Capacity** (it reports in mAh).

Normal Setting: *CC Gain* should never need to be modified directly by the user. It is modified by the current calibration function from Calibration Mode. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note [SLUA355A](#) for more information.

CC Delta

This is the gain factor for calibrating out Sense Resistor, Trace, and internal Coulomb Counter (integrating ADC Delta Sigma) errors. It is used in the algorithm that reports charge and discharge in and out of the battery through the **Remaining Capacity** register. The difference between *CC Gain* and *CC Delta* is that the algorithm that reports **Current** cancels out the time base since **Current** does not have a time component (it reports in mA) and *CC Delta* requires a time base for reporting **Remaining Capacity** (it reports in mAh).

Normal Setting: *CC Delta* should never need to be modified directly by the user. It is modified by the current calibration function from Calibration Mode. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note [SLUA355A](#) for more information.

Ref Voltage

The *Ref Voltage* is based on the actual reference voltage that the bq29312A uses for reference when sending voltage readings to the bq20z80. Therefore, this is a required constant in all the bq20z80 voltage computation formulas for displaying individual cell voltages (**Cell Voltage 1-4**) and the computed battery voltage (**Voltage**) in millivolts. By tweaking this value before it is used in the voltage computation formulas, then the errors introduced by the bq20z80 ADC and bq29312A reference are canceled out before they affect the reported voltages.

Normal Setting: *Ref Voltage* should never need to be modified by the user. It is modified by the voltage calibration command in Calibration mode. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note [SLUA355A](#) for more information.

AFE Corr

The AFE gain varies slightly as a function of in the input voltage. This variation is relatively constant and predictable so *AFE Corr* is used to correct for this common mode gain error of the input voltage.

Normal Setting: This register will only need to be changed under special circumstances. Its default setting is 1288. It is not modified by calibration commands.

AFE Pack Gain

The *AFE Pack Gain* is used for calibrating out errors in the bq29312A reference and bq20z80 ADC. It is used for reporting the **Pack Voltage** as measured on the PACK pin of the bq29312A. Therefore, this is a required constant in all the bq20z80 voltage computation formulas for displaying **Pack Voltage** in millivolts. By tweaking this value before it is used in the voltage computation formulas, then it changes the gain of the reported voltage which gives a method for calibrating this reported voltage.

Normal Setting: *AFE Pack Gain* may not need to be calibrated depending on the application. Unless **Pack Voltage** is used for display by the application then it will only be used for charger detection, and it does not need to be accurate for function. *AFE Pack Gain* should never need to be modified by the user. It is modified by the pack voltage calibration command in Calibration mode. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note [SLUA355A](#) for more information.

CC Offset

There are 2 offsets for calibrating the offset of the internal Coulomb Counter, board layout, sense resistor, copper traces and other offsets from the Coulomb Counter readings. *CC Offset* is the calibration value that primarily corrects for the offset error of the bq20z80 Coulomb Counter circuitry. The other offset calibration is *Board Offset* described below. To minimize external influences when doing *CC Offset* calibration either by either automatic *CC Offset* calibration or by the *CC Offset* calibration function in Calibration Mode an internal short is places across the SR1 and SR2 pins inside the bq20z80. *CC Offset* is a correction for very small noise/errors; therefore, to maximize accuracy it takes about 20 seconds to calibrate out the offset. Since it is not practical to do a 20 second offset during production, 2 different methods for calibrating *CC Offset* were developed.

- (A) The first method is to calibrate CC Offset by the putting the bq20z80 in Calibration Mode and initiating the CC Offset function as part of the entire bq20z80 calibration suite. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note [SLUA355A](#) for more information on the Calibration Mode. This is a short calibration that is not as accurate as the second method described below. Its primary purpose is to calibrate CC Offset enough so it will not affect any other Coulomb Counter calibrations. This is only intended as a temporary calibration because the automatic calibration described below is done the first time SMBus is low for more than 20 seconds which is a much more accurate calibration.
- (B) During normal Gas Gauge Operation (**Temperature** is between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High*) when the SMBus clock and data lines are low for more than *Bus Low Time* seconds and **Current** is less than *Sleep Current* in milliAmps then an automatic CC Offset calibration is performed. This takes around 16 seconds and is much more accurate than the method in Calibration mode.

Normal Setting: CC Offset should never be modified directly by the user. It is modified by the current calibration function from Calibration Mode or by Automatic Calibration. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note [SLUA355A](#) for more information on calibration.

Board Offset

Board Offset is the second offset register. Its primary purpose is to calibrate all that the CC Offset does not calibrate out. This includes board layout, sense resistor and copper trace and other offsets that are external to the bq20z80 IC. This is a very long calibration and can take up to 20 seconds. Since **Board Offset** is primarily used to cancel out offsets external to the bq20z80 IC then it only has to be done on a sample LOT of bq20z80 modules for a particular PCB design. Then average the results and use this as a Board Offset throughout the life of the design. Anytime a PCB is revised then this should be done again to ensure the offset has not been affected by the board change.

Normal Setting: This value should only be set one time when all the other Data Flash constants are modified during the pack production process. It is important to note that the bq20z80 EV software uses CC Offset Time in the EV software formula for computing board offset. It is recommended that CC Offset Time be modified to 20,000 to get an accurate board offset with the above procedure (See CC Offset Time).

Int Temp Offset

The bq20z80 has a temperature sensor built into the IC. The **Int Temp Offset** is used for calibrating out offset errors in the measurement of the reported **Temperature** if the internal temperature sensor is used. The gain of the internal temperature sensor is accurate enough that a calibration for Gain is not required.

Normal Setting: **Int Temp Offset** should never need to be modified by the user. It is modified by the internal temperature sensor calibration command in Calibration mode. **Int Temp Offset** should only be calibrated if the internal temperature sensor is used. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note [SLUA355A](#) for more information on calibration.

Ext1 Temp Offset

Ext1 Temp Offset is for calibrating the offset of the thermistor connected to the TS1 pin of the bq20z80 as reported by **Temperature**. The gain of the thermistor is accurate enough that a calibration for gain is not required.

Normal Setting: **Ext1 Temp Offset** should never need to be modified by the user. It is modified by the external temperature sensor calibration command in Calibration mode. **Ext1 Temp Offset** should only be calibrated if a thermistor is connected to the TS1 pin of the bq20z80. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note [SLUA355A](#) for more information on calibration.

Ext2 Temp Offset

Ext2 Temp Offset is for calibrating the offset of the thermistor connected to the TS2 pin of the bq20z80 as reported by **Temperature**. The gain of the thermistor is accurate enough that a calibration for gain is not required.

Normal Setting: *Ext2 Temp Offset* should never need to be modified by the user. It is modified by the external temperature sensor calibration command in Calibration mode. *Ext2 Temp Offset* should only be calibrated if the a thermistor is connected to the TS1 pin of the bq20z80. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note [SLUA355A](#) for more information on calibration.

8.2 Config

These are all setting for adjusting Calibration Mode applied voltage, current, and temperature as well as the times associated with these calibrations. The Times should not need to be modified with normal applications. The values in Data Flash for these registers are defaults for Calibration Mode. If no other values are assigned to the calibration commands associated with each of these registers when in Calibration Mode then these default values is used. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note [SLUA355A](#) for more information on calibration.

CC Current

This register holds the default current that is applied during the calibration process while in Calibration mode. If, while in calibration mode, the *CC Current* is not modified by calibration command then this value is what is used to calibrate *CC Gain* and *CC Delta*. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z80.

Normal Setting: This depends on the sense resistor used. Higher currents increase the voltage across the SR1 and SR2 pins which decreases noise and offset errors. It also increases the calibration accuracy because the granularity has less effect on the measurements. Good numbers for a 10 milliohm sense resistor are 2 to 3 amps.

Voltage Signal

This register holds the default voltage that is applied during the calibration process while in Calibration Mode. If, while in calibration mode, the *Voltage Signal* is not modified by calibration command then this value is what is used to calibrate *Reference Voltage* and *AFE Pack Gain*. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z80. This value is a pack voltage, not a cell voltage.

Normal Setting: This depends on the number of cells, but it is good idea to use a voltage that is within the normal operating voltages of the cells used in the application times the number of cells.

Temperature Signal

This register holds the default Temperature that is applied during the calibration process while in Calibration Mode. If, while in calibration mode, the *Temperature Signal* is not modified by calibration command then this value is what is used to calibrate all the Temperature inputs that are used in this application. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z80.

Normal Setting: This value more than any of the others must be modified using the calibration commands in Calibration Mode instead of using this Data Flash location because temperature is continually changing.

CC Offset Time

CC Offset Time is the time that the calibration command for initiating a *CC Offset* calibration will take to do a *CC Offset* calibration. This is also used in Board Offset calibration in the bq20z80 EV software.

Normal Setting: The default is 250 and the units are in milliseconds. Only use values in multiples of 250 ms. The calibration function rounds the *CC Offset Time* down to the next lower multiple of 250 ms if an exact multiple of 250 is not used. It reports a calibration error if a value less than 250 is used. Remember that this is only a temporary calibration to minimize offset effects on other CC calibrations. The Automatic Offset calibration that happens during normal Gas Gauging mode does a more accurate calibration. It is important to note that this is also used by the bq20z80 EV software to do Board Offset calibration. It is a good idea to increase this number to 20,000 to get a very accurate board offset measurement for production testing (see Board Offset) .

ADC Offset Time

ADC Offset Time is the time that the calibration command for initiating an ADC Offset calibration takes for an ADC Offset calibration. *ADC Offset* is not associated with a Data Flash location, but it is done every time Automatic *ADC Offset* is done in Gas Gauging mode and should be initiated at the same time as *ADC Offset* when in Calibration Mode.

Normal Setting: The default is 32 and the units are in milliseconds. Only use values in multiples of 32 ms. The calibration function rounds the ADC Offset Time down to the next lower multiple of 32 ms if an exact multiple of 32 is not used. It reports a calibration error if a value less than 32 is used. Remember that this is only a temporary calibration. The Automatic Offset calibration that happens during normal Gas Gauging mode keeps this value accurate.

CC Gain Time

CC Gain Time is the time that the calibration command for initiating a CC Gain calibration takes for a *CC Gain Time* calibration. It uses the value in *CC Current* over *CC Gain Time* to do the calibration.

Normal Setting: The default is 250 and the units are in milliseconds. Only use values in multiples of 250 ms. The calibration function will round the *CC Gain Time* down to the next lower multiple of 250 ms if an exact multiple of 250 is not used. It reports a calibration error if a value less than 250 is used. Depending on the current used, it is possible that 250 ms not enough time for a good calibration. It is recommended that 500 ms to 1000 ms be used for best results.

Voltage Time

Voltage Time is the time that the calibration commands for initiating a Reference Voltage or *AFE Pack Gain* calibration takes for a *Reference Voltage* or *AFE Pack Gain* calibration. These commands use the value in *Voltage Signal* over *Voltage Time* to do the calibration.

Normal Setting: The default is 1984 and the units are in milliseconds. Only use values in multiples of 1984 ms. The calibration function will round the *Voltage Time* down to the next lower multiple of 1984 ms if an exact multiple of 1984 is not used. It will report a calibration error if a value less than 1984 is used.

Temperature Time

Temperature Time is the time that the calibration commands for initiating any of the 3 temperature calibrations takes for the respective calibrations. These commands uses the value in *Temperature Signal* over *Temperature Time* to do the calibration.

Normal Setting: The default is 32 and the units are in milliseconds. Only use values in multiples of 32 ms. The calibration function rounds the *Temperature Time* down to the next lower multiple of 32 ms if an exact multiple of 32 is not used. It will report a calibration error if a value less than 32 is used.

Cal Mode Timeout

Cal Mode Timeout is the maximum amount of time allowed for all calibrations to complete before the bq20z80 reverts to Gas Gauge mode automatically. The timer for this function starts when the Call Mode command is initiated.

Normal Setting: The purpose of this function is ensure that the bq20z80 has the ability to get out of Calibration Mode on its own if it was accidentally put into Calibration Mode for any unknown reason. The default for this register is 38400 which is in units of seconds/128. This translates to 5 minutes. It is unlikely that this register will need to be modified.

8.3 Temp Model

None of these registers must not be changed for any reason. The only reason these values are listed is for the purpose of using a different thermistor; however, this is not recommended, and has not been tested with the bq20z80.

Ext Coef 1, Ext Coef 2, Ext Coef 3, Ext Coef 4

These are the coefficients for a close approximation curve match formula to the temperature curve specified for the Semitec 103AT Thermistor.

Ext Min AD

This is the minimum ADC value allowed for the Temperature conversion formula.

Normal Setting: This value is 0 and should not be changed.

Ext Max Temp

This is the maximum temperature value allowed for the Temperature conversion formula.

Normal Setting: This value is 4012 and should not be changed.

Int Coef 1, Int Coef 2, Int Coef 3, Int Coef 4

These are the coefficients for a close approximation curve match formula to the temperature curve specified for the Semitec 103AT Thermistor.

Int Min AD

This is the minimum ADC value allowed for the Temperature conversion formula. Normal Setting: This value is 0 and should not be changed.

Int Max Temp

This is the maximum temperature value allowed for the Temperature conversion formula.

Normal Setting: This value is 4012 and should not be changed.

8.4 Current

Filter

This constant defines the filter constant used in the **Average Current** formula. This is a very common question how this is calculated. The formula used to compute **Average Current** is :

$$\text{New (Average Current)} = A \times \text{Old (Average Current)} + (1-A) \times \text{Current}$$

$$A = \text{Filter}/256. \text{ Default value is 239}$$

The time constant = 1 sec/ln(1/a) (default 14.5 sec)

Normal Setting: It is unlikely that this value should ever need to be changed.

Deadband

The purpose of the *Deadband* is to create a filter window to the reported **Current** register where the current is reported as 0. Any negative current above this value or any positive current below this value is displayed as 0.

Normal Setting: This defaults to 3 mA. There are not many reasons to change this value. Here are a few.

1. If the bq20z80 is not calibrated.
2. *Board Offset* has not been characterized.
3. If the PCB layout has issues that cause inconsistent board offsets from board to board.
4. An extra noisy environment in conjunction with number 3.

If this value must be modified be sure and verify the CC Deadband as well.

CC Deadband

This is also referred to as Digital Filter. This works much in the same way as the *Deadband* except it works for capacity counting on the **Remaining Capacity** register. Any absolute voltage between SR1 and SR2 below this value does not contribute to capacity measurement. The purpose of this is to minimize the possibility of unwanted noise from being counted towards capacity.

Normal Setting: The default for this register is 34 and it is in units of 290 nanovolts. This gives a *CC Deadband* of 9.86 μV . This value is most likely too small for most applications. A better value would be 2 or 3 times this default. Unlike *Deadband* this value is not influenced by what value of sense resistor is used since this value is stored in microvolts and not milli-amps.

CC Max Deadband

This constant defines the limit in coulomb counter counts (about 10 $\mu\text{V}/\text{cnt}$) at which the coulomb counter input is measured using a sample size defined by *CC Deadband Sample*. A larger sample size is needed to measure greater resolution than can be measured with a single sample.

Normal Setting: This value should not need to be modified for any normal setting of the *CC Deadband*.

CC Deadband Sample

This constant defines the sample size of coulomb counter conversions used to measure the coulomb counter input for *CC Deadband* evaluation. A larger sample size is needed to measure greater resolution than can be measured with a single sample.

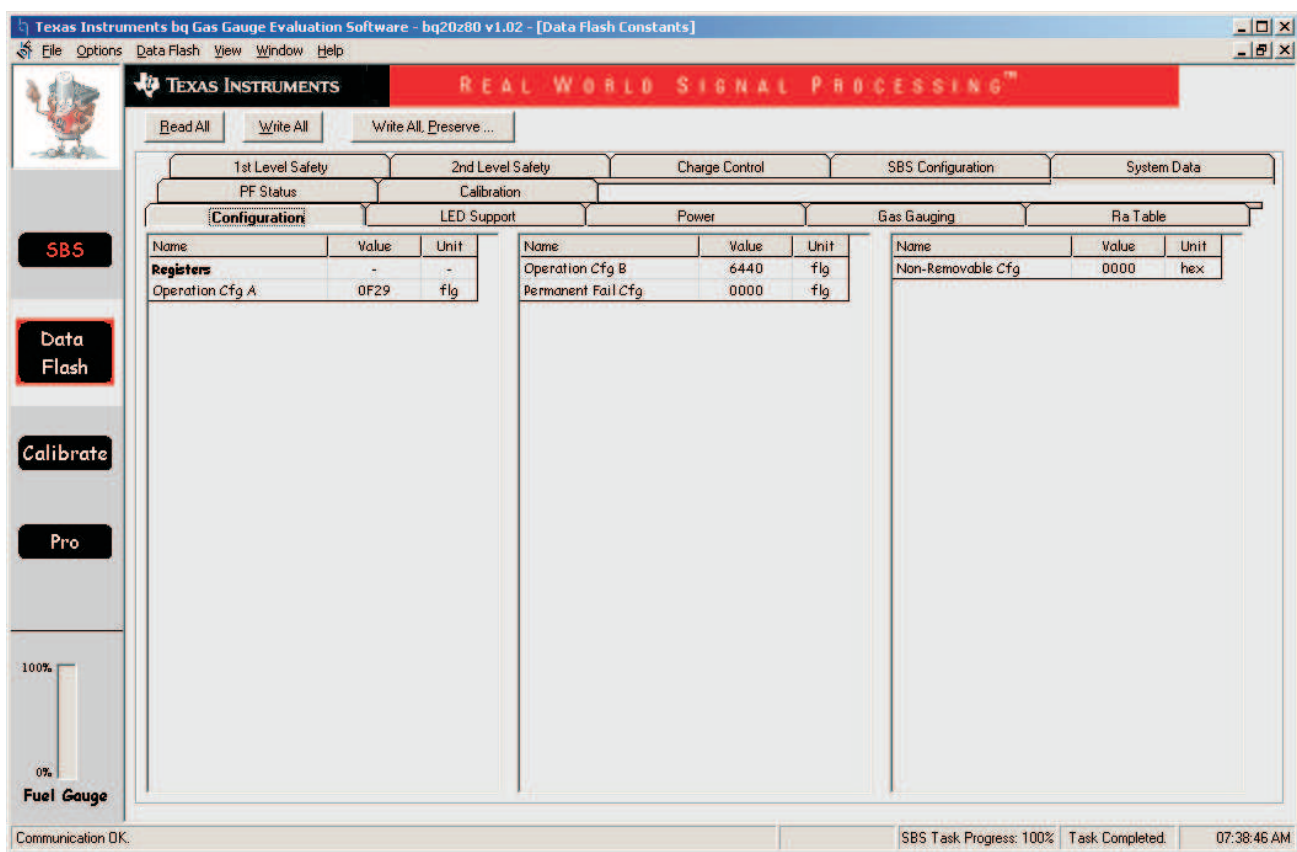
Normal Setting: This value should not need to be modified for any normal setting of the *CC Deadband*.

CC Offset Sample

CC Offset Sample is the number of coulomb counter readings that are required for an automatic *CC Offset* calibration. This is not to be confused with the *CC Offset* calibration done in Calibration Mode. This calibration is only done when SMBus clock and data lines are low for more than *Bus Low Time* seconds and **Current** is below *Sleep Current*.

Normal Setting: This default value is 64. There are 4 coulomb counter conversions per second. This results in a 16 second *CC Offset* calibration

9 Configuration



9.1 Registers

Operation Cfg A

This register is used to enable or disable various functions on the bq20z80. These bits are continued in *Operation Cfg B*.

LEDR	LEDRCA	CHGLED	DMODE	LED1	LED0	CC1	CC0
–	–	SLEEP	TEMP1	TEMP0	SLED	ZVCHG1	ZVCHG0

- LEDR [15]: This bit is useful to watch for device resets. If enabled, it activates the LED display with the present **RSOC** state after a reset has occurred. LEDs operate exactly the same as a DISP button transition function (See **LED Support** class).
 - 0: LEDs do not illuminate on reset
 - 1: LEDs illuminate in the same manner as a DISP button press after a reset has occurred.

Normal Setting: This bit defaults to a 0 which should be used in production. This bit should normally only be set during development.

LEDRCA [14]: If enabled, this bit forces the bq20z80 to force the LEDs to flash with a period of ($2 \times \text{LED Flash Rate}$) whenever [RCA] is set in **Battery Status** and the LEDs are activated. In Discharge Mode ([DSG] flag clear in **Battery Status**), a transition from high to low on the DISP pin of the bq2z80 (DISP button transition) is required to activate the LEDs. During Charge ([DSG] flag clear in **Battery Status**), if [CHGLED] set in *Operation Cfg A*, then DISP button transition is not required because the LEDs are activated (See **LED Support** class).

 - 0: LEDs do not flash at the *LED Flash Rate* period with [RCA] set in **Battery Status**.
 - 1: LEDs do flash at ($2 \times \text{LED Flash Rate}$) period with [RCA] set in **Battery Status** if activated.

Normal Setting: This bit defaults to a 0. It is set based on user preference.

- CHGLED [13]: If enabled, this bit forces the bq20z80 to activate the LED display whenever charging (**Current** greater than *CHG Current Threshold*). LEDs operate exactly the same as a DISP button transition function except they do not time out and deactivate until **Current** is less than *CHG Current Threshold*. (See **LED Support** class)
 - 0: LEDs do not illuminate on reset
 - 1: LEDs illuminate in the same manner as a DISP button press.

Normal Setting: This bit defaults to a 0. It is set based on user preference.

- DMODE [12]: This is the Display Mode bit which refers to LED configuration. If the Display mode bit is 0, then the display is in "Relative Mode". If it is 1, then it is in "Absolute Mode". In relative mode, the LED display is based on a percentage of the **Full Charge Capacity**, which is stored in the **RSOC** register. If it is in absolute mode, then the LED display is based on a percentage of **Design Capacity**, which is stored in the **ASOC** register.
 - 0: Number of LEDs that illuminated when activated are based on **RSOC**.
 - 1: Number of LEDs that illuminated when activated are based on **ASOC**.

Normal Setting: This bit defaults to a 0 which is Relative Mode. This is the most common mode that customers use. It is important to note that **ASOC** can be greater than 100%. The LEDs treat any **ASOC** greater than 100% as 100%

- LED1, 0 [11, 10]: These bits are used to inform the bq20z80 of the number of LEDs that are being used in the application.
 - 1,1 = 5 LEDs
 - 1,0 = 4 LEDs
 - 0,1 = 3 LEDs
 - 0,0 = This is for a user defined setting as set in the **LED Support** class.

Normal Setting: The default setting for these bits is both bits set. This is based on user preference and application.

- CC1,0 [9,8]: These bits are used to inform the bq20z80 of the number of Li-Ion battery cells in a series for the application. This setting is critical for every aspect of the Data Flash configuration with regards to voltage based functions.
 - 1,1 = 4 series cell application
 - 1,0 = 3 series cell application
 - 0,1 = 2 series cell application
 - 0,0 = Reserved (Not Valid)

Normal Setting: The default value for these bits are both set for a 4-series cell application. These bits are application and user dependant.

- **RESERVED [7,6]:** These bits are reserved
- **SLEEP [5]:** This bit enables or disables the ability to go to sleep when SMBus Clock and Data lines go low for Bus Low Time and **Current** is below *Sleep Current* (See *Sleep Current* and *Bus Low Time*)
 - 0: bq20z80 do not go to sleep with the above criteria
 - 1: bq20z80 do go to sleep when the sleep criteria is set

Normal Setting: This bit defaults to a 1 which should be used in most applications. There are few reasons for this bit to be set to 0.
- **Temp1,0 [4,3]:** These bits are used to tell the bq20z80 the temperature sensor configuration. The bq20z80 can use up to 2 external sensors and there is also an internal sensor available if needed. All of these sensors are able to use various configurations to report temperature in the **Temperature** register.
 - 1,1 = The Average of TS1 and TS2 external inputs are used to generate **Temperature**.
 - 1,0 = Greater Value of TS1 and TS2 external inputs are used to generate **Temperature**.
 - 0,1 = Only Temperature sensor TS1 is used to generate **Temperature**.
 - 0,0 = Only internal temperature sensor is used to generate **Temperature**.

Normal Setting: The default setting for these bits is [Temp1] cleared and [Temp0] set. This requires one external temperature sensor on TS1. The bq20z80 default configuration is for a Semitec 103AT thermistor as briefly described in the **Temp Model** subclass (See **Temp Model**). The internal temperature sensor is slightly less accurate than using a Semitec 103AT and is not recommended. It also is not as accurate because it cannot be put as close to the battery cells in the application as can be done with an external thermistor.
- **SLED [2]:** The serial LED option can be used to implement a much brighter display at the expense of additional hardware components. With the parallel connection, the 3.3 V output from the bq29312A. is used to power the LEDs. Using that approach, current in each LED should be limited to 3 mA. With the serial option, all LEDs can be powered from the battery voltage and driven in series through a simple constant current regulator. The current is then diverted to ground at the various nodes between the series LEDs in order to program the desired pattern. If this function is enabled, then the Permanent Failure display mode using the LEDs is disabled. (See *Operation Cfg B*). The 2 options for this bit are:
 - 0: Parallel LED configuration
 - 1: Serial LED Configuration

Normal Setting: This bit defaults to a 0 which should be used in production for most applications. Given that serial LEDs require more components and 3 mA is usually sufficient for most applications then 0 is the most common setting for this bit.
- **ZVCHG1,0 [1,0]:** These bits are also known as Pre-Charge 1,0. These bits are used to tell the bq20z80 how the Pre-Charge circuit is configured in the application. It tells the bq2z80 what pin on the bq29312A to use for Pre-Charge functions when required.
 - 1,1 = No action is taken in Pre-Charge functions with this setting.
 - 1,0 = OD pin is used for Pre-Charge functions.
 - 0,1 = Charge FET is used for Pre-Charge functions.
 - 0,0 = ZVCHG FET is being used for Pre-Charge functions.

Normal Setting: If using a separate Pre-Charge FET it is recommended not to use the OD pin for this function because it does not have good “zero volt charging” capabilities when a battery is completely dead. Therefore, the ZVCHG pin should be used because it has excellent clamping abilities. The default is for using the Charge FET pin on the bq29312A.

Operation Cfg B

This register is used to enable or disable various functions on the bq20z80. This is a continuation of *Operation Cfg A*.

PFD1	PFD0	RESCAP	NCSMB	NRCHG	CSYNC	CHGTERM	CCT
CHGSUP	OTFET	CHGFET	CHGIN	NR	CPE	HPE	BCAST

- PFD1,0 [15,14]: These bits are used to configure how the bq20z80 is supposed to display permanent failure data through the LEDs if enabled. If [SLED] set in *Operation Cfg A* then this function is disabled. If there is no permanent failure, then no action is taken on the LEDs even if this function is enabled.
 - 1,1 = Permanent Failure data is displayed on the LEDs after the LEDs display the state of charge data (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) when the DISP button is activated. The DISP button does not have to be activated for more than *LED Hold Time*.
 - 1,0 = Permanent Failure data is disabled with this setting
 - 0,1 = Permanent Failure data is displayed on the LEDs after the LED display indicates the SOC data (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*), but only if DISP button is activated for more than *LED Hold Time*.
 - 0,0 = Permanent Failure display is disabled with this setting

Normal Setting: The default setting here is [PFD1] cleared and [PFD0] set. This gives the ability to get permanent failure data from a damaged battery pack even if communications are not possible as long as the bq20z80 CPU is still functioning.

- RESCAP [13]: The bq20z80 reports **Remaining Capacity** and **Full Charge Capacity** that is falsely lower than the actual capacity of the battery as defined by the *Reserve Cap-mAh* in mAh mode or *Reserve Cap-mWh* in mWh mode (configured by [CAPM] in **Battery Mode**). RESCAP sets a load compensation for this function.
 - 0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity
 - 1: If set to a 1, then a more normal rate of load compensation as defined by Load Select is applied to this reserve capacity. (See **IT Cfg** class)

Normal Setting: This bit defaults to a 1. For most applications, this along with *Load Select* should be left at the default values.

- NCSMB [12]: This bit is used to enable a special mode for the SMBus engine in the bq20z80 where it allows for unlimited timeouts for SMBus communications more like I²C. This mode was made for customers that were using older legacy parts that had longer timeouts and were not SMBus compliant.
 - 0: Timeout extension is disabled.
 - 1: Unlimited Timeout extension enabled.

Normal Setting: The default for this register is 0. It is recommended that this always be set to 0. There have been many complications with customers using this function in the past. When set to a 1, it is important to note that if clocking in data with a SMBus read command and the communication gets interrupted with data low then data can be stuck low until more clocks are sent to finish the communication.

- NRCHG [11]: This bit is used to configure whether or not the bq20z80 turns off the Charge FET when it goes to Sleep if [NR] bit is set in *Operation Cfg B*. If [NR] cleared then this bit is not used.
 - 0: Charge FET turns off in sleep mode as long as the bq20z80 is setup with [NR] set.
 - 1: Charge FET remains on in sleep mode with the [NR] bit set.

Normal Setting: This bit defaults to a 0 which should be used for most applications with [NR] set. This could be a problem for some applications that expect the battery to start charging immediately when charge is applied when asleep.

- CSYNC [10]: This bit is used in the Primary Charge Termination Algorithm (See *Maintenance Current*). When this bit is set, then with a Primary Charge Termination the bq20z80 writes the **Remaining Capacity to Full Charge Capacity**
 - 0: **Remaining Capacity** is not written up to **Full Charge Capacity** on Primary Charge Termination.
 - 1: **Remaining Capacity** is written up to **Full Charge Capacity** on Primary Charge Termination.

Normal Setting: The default setting for this bit is 1. This should be used for most applications to ensure that the Remaining Capacity starts from Full Charge Capacity when the charger terminates charging. This is a synchronization function to ensure the bq20z80 discharges from full when it has been determined that the battery is full.
- CHGTERM [9]: This bit enables the ability for the bq20z80 to turn off [TCA] and [FC] in **Battery Status** after a Primary Charge Termination is detected and then current falls below the *Taper Current* for 2 consecutive periods of *Taper Current Window*.
 - 0: bq20z80 does not clear [TCA] and [FC] in **Battery Status** after a Primary Charge Termination.
 - 1: bq20z80 does clear [TCA] and [FC] in Battery Status after a Primary Charge Termination.

Normal Setting: This bit defaults to 0. This should be acceptable for most applications.
- CCT [8]: This bit configures which method the bq20z80 will use for incrementing **Cycle Count**.
 - 0: If set to 0, then the bq20z80 increments **Cycle Count** by 1 with every cumulative discharge of *Cycle Count Threshold* in mAh. This discharge does not have to be consecutive. The bq20z80 accumulates all discharge current for this calculation even when broken up by periods of charge.
 - 1: if set, then when the bq20z80 accumulates enough discharge capacity equal to $(CC\% \times FCC)$ then it increments *Cycle Count* by 1

Normal Setting: This bit defaults to a 0. This setting is application specific.
- CHGSUSP [7]: This bit enables the ability to turn off the Charge FET and/or Pre-Charge FET in charge suspend mode (See **Charge Control Class**).
 - 0 = The Charge FET is unaffected by any type of charge suspension.
 - 1 = The Charge FET and/or Pre-Charge FET are opened with any charge suspension.

Normal Setting: the default setting for this bit is 0. It is common for this to be set to 1 to give the bq20z80 the control for additional protection.
- OTFET [6]: This bit is used to configure how the bq20z80 controls the current FETs (Charge or Discharge) during *Over Temp Chg* or *Over Temp Dsg* faults. (See *Over Temp Chg* and *Over Temp Dsg*)
 - 0: FET control is unaffected by any *Over Temp Chg* or *Over Temp Dsg* faults.
 - 1: During a *Over Temp Chg* fault the Charge FET is opened. During a *Over Temp Dsg* fault the Discharge FET is opened.

Normal Setting: This bit defaults to a 1 which should be used in production for most applications. Over temperature conditions can be dangerous and every level of protection possible should be used.
- CHGFET [5]: This bit is used to configure how the bq20z80 controls the Charge FETs when [TCA] gets set in **Battery Status**. (See *TCA Set %* for an explanation for when [TCA] gets set).
 - 0: Charge FET is unaffected anytime [TCA] gets set.
 - 1: Charge FET is turned off anytime [TCA] gets set.

Normal Setting: This bit defaults to a 0 which should be used in production for most applications. Setting it to a 1 turns the Charge FET off is only if *Maintenance Current* is set to 0.
- CHGIN [4]: This bit is used to configure how the bq20z80 controls the Charge FETs when in charge inhibit mode. (See *Chg Inhibit Temp Low* and *Chg Inhibit Temp High*).
 - 0: Charge FET is unaffected when in charge inhibit mode.
 - 1: Charge FET is turned off when in charge inhibit mode.

Normal Setting: This bit defaults to a 0 which should be acceptable for most applications. It is important to note that this is different than charge suspend mode because this inhibits the charge cycle from occurring. This function acts while discharging.

- NR [3]: Use this bit to configure the bq20z80 for either a removable or a non removable battery pack. A removable pack uses the System Present pin (PRES) and a nonremovable pack does not. This affects many functions in the bq20z80. Primarily it affects the way it handles recovery methods of most fault conditions. A removable pack can clear many fault conditions by simple removal and reinsertion. With [NR] set, the *NR Config* register is used to enable many nonremovable pack fault recovery methods for use with a removable pack. (See *NR Config* and **Current** subclass in **1st Level Safety** class)
 - 0: Configures battery for removable mode. Transition on System Present pin (PRES) triggers certain recovery functions. *NR Config* can be used to enable nonremovable functions for this mode as well
 - 1: Configures battery for nonremovable mode.

Normal Setting: Default for this bit is application specific. Set to 0 for batteries that are removed, and use the PRES pin. Set to 1 for packs that do not use the PRES pin.

- CPE [2]: This bit enables or disables PEC error correction on SMBus Master Mode messages that the bq20z80 broadcasts to the SMBus Device Address 0x12 (SMBus charger device address) (See SBS and SMBus specification that can be downloaded from the web).
 - 0: No PEC byte is sent to SMBus Device Address 0x12.
 - 1: Every broadcast from the bq20z80 to SMBus Device Address 0x12 includes a PEC byte as the last byte sent.

Normal Setting: If a smart charger (SMBus Device Address 0x12) is used that is PEC capable, then this should be set to a 1. It is always recommended to use PEC when possible.

- HPE [1]: This bit enables or disables PEC error correction on SMBus Master Mode messages that the bq20z80 broadcasts to the SMBus Device Address 0x14 (SMBus Host device address)
 - 0: No PEC byte is set to SMBus Device Address 0x14. (See SBS and SMBus specification that can be downloaded from the web)
 - 1: Every broadcast from the bq20z80 to SMBus Device Address 0x14 includes a PEC byte as the last byte sent.

Normal Setting: If a host (SMBus Device Address 0x14) is PEC capable then this should be set to a 1. It is always recommended to use PEC when possible.

- BCAST [0]: This bit enables or disables Master Mode Message broadcasting periodically to a smart charger or host. The bq20z80 broadcasts are completely disabled (See SBS and SMBus specification that can be downloaded from the web)
 - 0: The bq20z80 never masters the SMBus for any reason.
 - 1: The bq20z80 is enabled to Master the bus periodically to inform a host or charger of critical information

Normal Setting: If a host (SMBus Device Address 0x14) is PEC capable then this should be set to a 1. It is always recommended to use PEC when possible.

Permanent Fail Cfg

This enables or disables the various permanent failure protection functions ability to activate the SAFE outputs (SAFE and SAFE pins) or not when the function is triggered.

–	–	–	XSOPT	XSOCD	XSOCC	XAFE_P	XAFE_C
XDFE	XDFETF	XCFETF	XCIM	XSOTD	XSOTC	XSOV	XPFIN

- RESERVED [15–13]: These bits are reserved.

- XSOPT [12]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with an Open Thermistor failure condition. With this function enabled, the bq20z80 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high, and the $\overline{\text{SAFE}}$ pin did go low. (See *SOC Chg*)
 - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for an Open Thermistor failure condition
 - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for an Open Thermistor failure condition

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOPT] be set for production packs to protect against hazardous failures.

- XSOC [11]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Current in the discharge direction condition. With this function enabled, the bq20z80 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOC Chg*)
 - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over Current in the discharge direction Condition
 - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Safety Over Current in the discharge direction Condition.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOC] be set for production packs to protect against hazardous failures.

- XSOC [10]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Current in the charge direction condition. With this function enabled, the bq20z80 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOC Dsg*).
 - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over Current in the charge direction Condition
 - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Safety Over Current in the charge direction Condition.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOC] be set for production packs to protect against hazardous failures.

- XAFE_P [9]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a periodic AFE verification failure. With this function enabled, the bq20z80 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *AFE Check Time*)
 - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a periodic AFE verification failure.
 - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a periodic AFE verification failure.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XAFE_P] be set for production packs to protect against hazardous failures.

- XAFE_C [8]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with an AFE communication verification failure. With this function enabled the bq20z80 will also write 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *AFE Fail Limit*)
 - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for an AFE communication verification failure.
 - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for an AFE communication verification failure.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XAFE_C] be set for production packs to protect against hazardous failures.

- XDFF [7]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Data Flash verification failure. With this function enabled, the bq20z80 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *PF Flags 1*)
 - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Data Flash verification failure.
 - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Data Flash verification failure.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XDFF] be set for production packs to protect against hazardous failures.

- XDFETF [6]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Discharge FET Failure condition. With this function enabled, the bq20z80 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *FET Fail Limit*)
 - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Discharge FET Failure Condition.
 - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Discharge FET Failure Condition.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XDFETF] be set for production packs to protect against hazardous failures.

- XCFETF [5]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Charge FET Failure condition. With this function enabled, the bq20z80 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *FET Fail Limit*)
 - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Charge FET Failure Condition.
 - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Charge FET Failure Condition.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XCFETF] be set for production packs to protect against hazardous failures.

- XCIM [4]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a extreme Cell Imbalance condition . With this function enabled, the bq20z80 writes 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *Cell Imbalance Fail Voltage*)
 - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a extreme Cell Imbalance Condition.
 - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a extreme Cell Imbalance Condition.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XCIM] be set for production packs to protect against hazardous failures.

- XSOTD [3]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Temperature in the discharge direction condition. With this function enabled, the bq20z80 writes 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOT Chg*)
 - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over Temperature in the discharge direction Condition.
 - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Safety Over Temperature in the discharge direction Condition.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOTD] be set for production packs to protect against hazardous failures.

- XSOTC [2]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Temperature in the charge direction condition . With this function enabled, the bq20z80 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOT Chg*)
 - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over Temperature in the charge direction Condition.
 - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Safety Over Temperature in the charge direction Condition.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOTC] be set for production packs to protect against hazardous failures.

- XSOV [1]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Voltage condition . With this function enabled, the bq20z80 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOV Threshold*).
 - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over Voltage Condition.
 - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Safety Over Voltage Condition.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOV] be set for production packs to protect against hazardous failures.

- XPFIN [0]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a PF input low condition . With this function enabled, the bq20z80 writes 0x3672 in the Fuse Flag to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *PFIN Detect Time*)
 - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a PF input low Condition.
 - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a PF input low Condition.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XPFIN] be set for production packs to protect against hazardous failures.

Non-Removable Cfg

This register affects the way the bq20z80 handles recovery methods for most fault conditions. A removable pack can clear many fault conditions by simple removal and reinsertion. With [NR] set, the *NR Config* register can be used to enable many nonremovable pack fault recovery methods for use with a removable pack. NR Config can be used to enable nonremovable fault recovery functions for a battery pack that is configured as removable.

–	–	OCD	OCC	OCD2	OCC2	–	–
–	–	OC	–	–	AOCD	SCC	SCD

- RESERVED [15, 14]: These bits are reserved
- OCD [13]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z80. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with an Over Current in the discharge direction fault (See *OC (1st Tier) Dsg*).
 - 0: The nonremovable recovery option associated with *OC (1st Tier) Dsg* is not enabled.
 - 1: The nonremovable recovery option associated with *OC (1st Tier) Dsg* is enabled.

Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.

- OCC [12]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z80. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with an Over Current in the charge direction fault (See *OC (1st Tier) Chg*).
 - 0: The nonremovable recovery option associated with *OC (1st Tier) Chg* is not enabled
 - 1: The nonremovable recovery option associated with *OC (1st Tier) Chg* is enabled.

Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.

- OCD2 [11]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z80. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with a second level Over Current in the discharge direction fault (See *OC (2nd Tier) Dsg*).
 - 0: The nonremovable recovery option associated with *OC (2nd Tier) Dsg* is not enabled.
 - 1: The nonremovable recovery option associated with *OC (2nd Tier) Dsg* is enabled.

Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.

- OCC2 [10]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z80. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with a second level Over Current in the charge direction fault (See *OC (2nd Tier) Dsg*).
 - 0: The nonremovable recovery option associated with *OC (2nd Tier) Chg* is not enabled.
 - 1: The nonremovable recovery option associated with *OC (2nd Tier) Chg* is enabled.

Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.

- RESERVED [9-3]: These bits are reserved.
- AOCD [2]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z80. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE Over Current in the discharge direction fault (*AFE OC Dsg*).
 - 0: The nonremovable recovery option associated with *AFE OC Dsg* is disabled.
 - 1: The nonremovable recovery option associated with *AFE OC Dsg* is enabled.

Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- SCC [1]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z80. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE short circuit in the charge direction fault (*AFE SC Chg*).
 - 0: The non removable recovery option associated with *AFE SC Chg* is disabled.
 - 1: The non removable recovery option associated with *AFE SC Chg* is enabled.

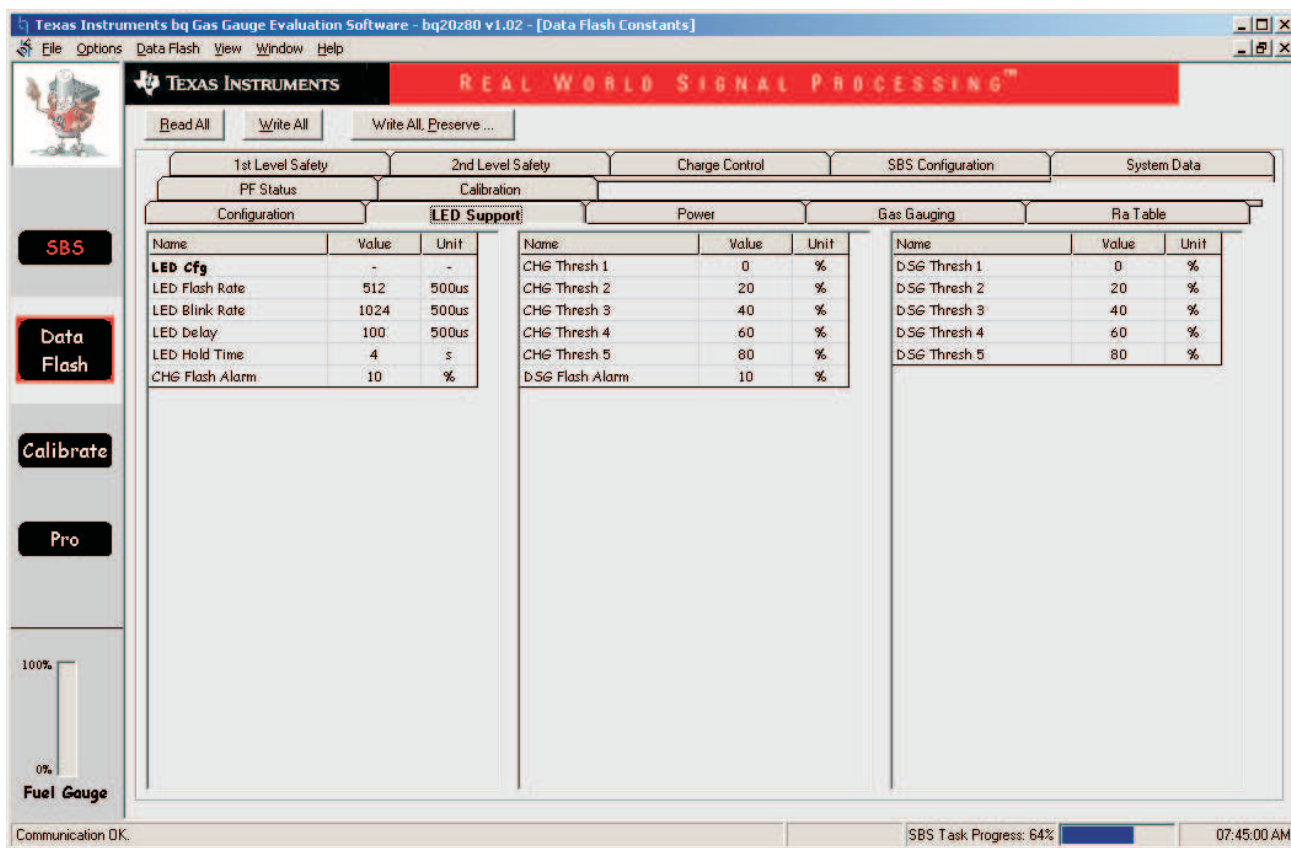
Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- SCD [0]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z80. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE short circuit in the discharge direction fault (*AFE SC Dsg*).
 - 0: The nonremovable recovery option associated with *AFE SC Dsg* is disabled.
 - 1: The nonremovable recovery option associated with *AFE SC Dsg* is enabled.

Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.

10 LED Support

There are 3 different display modes for the LEDs that need clarification to help understand the **LED Support** class.

- **Blinking:** When the display is said to be blinking, then the word “blinking” is used to refer to the LED located closest to the LED used to indicate 100% that is illuminated and “blinking” when the LED display is activated and displaying SOC (state of charge). Only this “topmost” activated LED in the display blinks. All other LEDs that are activated is steady state when activated. (see *LED Blink Rate*)
- **Flashing:** When the display is said to be flashing then the word “flashing” means all LEDs that are activated to indicate the SOC will flash with a period of ($2 \times \text{LED Flash Rate}$).
- **Delay:** When the display is activate, all LEDs that are required to indicate the SOC may not illuminate at the same time. Starting from the LED that represents the lowest SOC, there can be a delay (*LED Delay*) between each LED illuminating from the LED that represents the lowest possible SOC up to the LED that represents the present SOC.



LED Support

Name	Value	Unit
LED Cfg	-	-
LED Flash Rate	512	500us
LED Blink Rate	1024	500us
LED Delay	100	500us
LED Hold Time	4	s
CHG Flash Alarm	10	%

Name	Value	Unit
CHG Thresh 1	0	%
CHG Thresh 2	20	%
CHG Thresh 3	40	%
CHG Thresh 4	60	%
CHG Thresh 5	80	%
DSG Flash Alarm	10	%

Name	Value	Unit
DSG Thresh 1	0	%
DSG Thresh 2	20	%
DSG Thresh 3	40	%
DSG Thresh 4	60	%
DSG Thresh 5	80	%

Communication OK SBS Task Progress: 64% 07:45:00 AM

10.1 LED Cfg

LED Flash Rate

LED Flash Rate is used to configure the periodic rate at which the activated LEDs flashes with a ($2 \times \text{LED Flash Rate}$) period and a 50% duty cycle when the LEDs are required to flash. Only the LEDs that are requested to illuminate based on SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) will flash. LEDs are Required to flash with the following conditions:

1. When Charging ([DSG] cleared in **Battery Status**) with the following conditions:
 - (a) When [CHGLED] set in *Operation Cfg A*
 - (i) [LEDRCA] set in *Operation Cfg A*
 - (ii) [RCA] set in **Battery Status**
 - (b) High to low transition on the DISP pin (button press) with the following requirements:
 - (i) LEDRCA] set in *Operation Cfg A*
 - (ii) [RCA] set in **Battery Status**
2. When Discharging ([DSG] set in **Battery Status**) with a high to low transition on the DISP pin (button press) and the following conditions:
 - (a) LEDRCA] set in *Operation Cfg A*
 - (b) [RCA] set in **Battery Status**

Normal Setting: This setting depends on user preference however for most applications the default is acceptable. **LED Flash Rate** does not affect the operation of the part in any way except the display. The default is 512 and its in units of 500 micro seconds. That means that the default is 256 ms.

LED Blink Rate

The bq20z80 can be configured to blink the topmost LED in the LED display at a rate stored in **LED Blink Rate**. When the LED display is activated, the topmost LED is the illuminated LED closest to the LED that is used to indicate 100% SOC. The topmost LED in the LED string will blink with a ($2 \times \text{LED Blink Rate}$) period and a 50% duty cycle when charging ([DSG] cleared in **Battery Status**) with the following conditions:

- (A) Charging (**Current** > *Chg Current Threshold*) and [CHGLED] set in *Operation Cfg A*.
- (B) High to low transition on the DISP pin (button press)

This function is disabled (no blinking of topmost LED) if **LED Blink Rate** = 0.

Normal Setting: This setting depends on user preference however for most applications the default is acceptable. **LED Blink Rate** does not affect the operation of the part in any way except the display. The default is 1024 and is in units of 500 micro seconds. That means that the default is 512 ms.

LED Delay

The bq20z80 can be configured to put a delay in between the illumination of each LED segment during the display activation sequence. Upon request for activation of the LED display either by button press or charging, the LEDs ramps up to the topmost LED with a delay in between each LED illuminating in the sequence. The topmost LED is the illuminated LED that is closest to the LED that illuminates with 100% SOC when the LEDs are requested. If **LED Delay** = 0 then this function is disabled (no delay between LEDs illuminating).

Normal Setting: This setting depends on user preference however for most applications the default is acceptable. **LED Delay** does not affect the operation of the part in any way except the display. The default for this register is 100 in units of 500 micro seconds. So this would mean the default is 50 ms.

LED Hold Time

LED Hold Time defines the time that the LEDs remain active once all LEDs required to indicate the current SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) are active. When the request is registered, either by high to low transition on the DISP pin (button press) or charging, then the LED activation sequence is initiated then the LEDs must ramp up (see **LED Delay**) to all LEDs illuminating that are requested. When the ramp up completes, then an internal **LED Hold Time** timer is initiated. When the **LED Hold Time** timer expires, the LED display is deactivated.

Normal Setting: This setting depends on user preference however for most applications the default is acceptable. **LED Delay** does not affect the operation of the part in any way except the display. The default for this register is 4 seconds.

CHG Flash Alarm

The value in *CHG Flash Alarm* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear), otherwise this register is ignored. *CHG Flash Alarm* is used in an alternative method for alerting user to a low capacity condition. This function is completely independent of [LEDPCA] set in *Operation Cfg A*. This register is set as a function of SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*). This function only operates when charging. If SOC% is at or below the *CHG Flash Alarm* then the LEDs indicating the SOC% flashes at the *LED Flash Rate* with the following conditions:

- (A) When Charging ([DSG] cleared in **Battery Status**) and [CHGLED] set in *Operation Cfg A*.
- (B) High to low transition on the DISP pin (button press)

Normal Setting: The default setting for this register is 10%. This should be acceptable for most applications.

CHG Thresh 1

The value in *CHG Thresh 1* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in **Battery Status**) for *CHG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 (The LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st LED segment is active with SOC% within 0% to *CHG Thresh 1*.

Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers. Do not set above *CHG Thresh 2*.

CHG Thresh 2

The value in *CHG Thresh 2* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in **Battery Status**) for *CHG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 and LED 2 (The LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st and 2nd LED segments is active with SOC% above *CHG Thresh 1* and equal to or below *CHG Thresh 2*.

Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers. Do not set above *CHG Thresh 3*.

CHG Thresh 3

The value in *CHG Thresh 3* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in **Battery Status**) for *CHG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1, LED2, and LED 3 (The 3rd LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st, 2nd, and 3rd LED segments is active with SOC% above *CHG Thresh 2* and equal to or below *CHG Thresh 3*.

Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers. Do not set above *CHG Thresh 4*.

CHG Thresh 4

The value in *CHG Thresh 4* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in **Battery Status**) for *CHG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1, LED 2, LED 3 and LED 4 (The 4 LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st, 2nd, 3rd, and 4th LED segments is active with SOC% above *CHG Thresh 3* and equal to or below *CHG Thresh 4*.

Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers. Do not set above *CHG Thresh 5*.

CHG Thresh 5

The value in *CHG Thresh 5* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in **Battery Status**) for *CHG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 through LED 5 (The last LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then LED segments 1–5 is active with SOC% above *CHG Thresh 4*.

Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers.

DSG Flash Alarm

The value in *DSG Flash Alarm* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. *Dsg Flash Alarm* is used in an alternative method for alerting user to a low capacity condition. This function is completely independent of [LEDRCA] set in *Operation Cfg A*. This register is set as a function of SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*). This function only operates when discharging ([DSG] set in **Battery Status**). If SOC% is at or below the *Dsg Flash Alarm*, then the LEDs indicating the SOC% flashes at the *LED Flash Rate* with a high to low transition on the DISP pin (button press).

Normal Setting: The default setting for this register is 10%. This should be acceptable for most applications.

DSG Thresh 1

The value in *DSG Thresh 1* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in **Battery Status**) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 (The LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st LED segment is active with SOC% within 0% to *DSG Thresh 1*.

Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers. Do not set above *CHG Thresh 2*.

DSG Thresh 2

The value in *DSG Thresh 2* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in **Battery Status**) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 and LED 2 (The LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st and 2nd LED segments is active with SOC% above *CHG Thresh 1* and equal to or below *DSG Thresh 2*.

Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers. Do not set above *CHG Thresh 3*.

DSG Thresh 3

The value in *DSG Thresh 3* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in **Battery Status**) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1, LED2, and LED 3 (The 3rd LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st, 2nd, and 3rd LED segments is active with SOC% above *CHG Thresh 2* and equal to or below *DSG Thresh 3*.

Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers. Do not set above *CHG Thresh 4*.

DSG Thresh 4

The value in *DSG Thresh 4* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in **Battery Status**) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1, LED 2, LED 3 and LED 4 (The 4th LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st, 2nd, 3rd, and 4th LED segments is active with SOC% above *CHG Thresh 3* and equal to or below *DSG Thresh 4*.

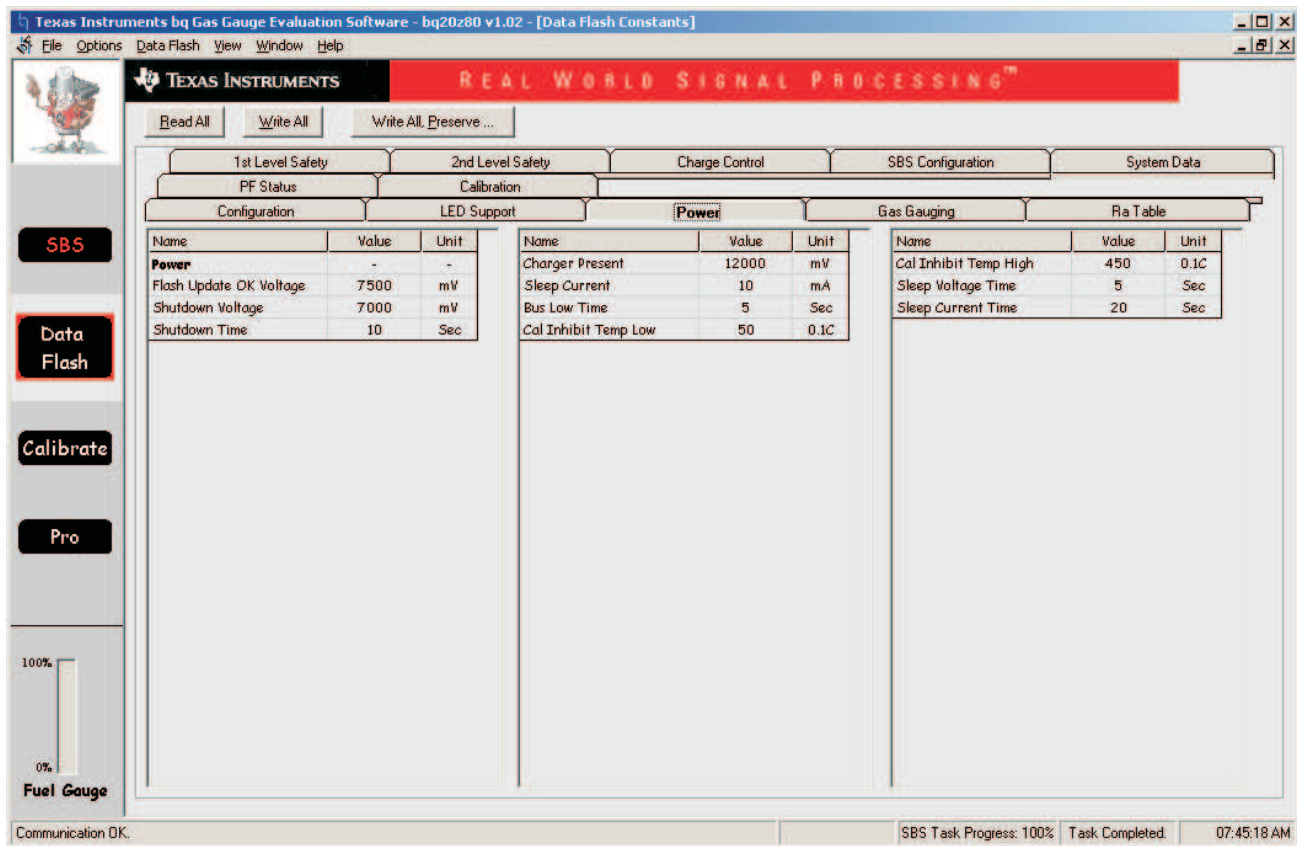
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers. Do not set above *CHG Thresh 5*.

DSG Thresh 5

The value in *DSG Thresh 5* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in **Battery Status**) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 through LED 5 (The last LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then LED segments 1–5 is active with SOC% above *DSG Thresh 4*.

Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers.

11 Power



11.1 Power

Flash Update OK Voltage

This register controls one of several data flash protection features. It is very critical that data flash is not updated when the battery voltage is too low. Data Flash programming takes much more current than normal operation of the bq20z80/bq29312A chipset and with a depleted battery this current can cause the battery voltage to crater (drop dramatically) forcing the bq20z80 into reset before completing a data flash write. The effects of an incomplete Data Flash write can corrupt the memory resulting in unpredictable and extremely undesirable results. The voltage setting in *Flash Update OK Voltage* is used to prevent any writes to the data flash below this value. If a charger is detected then this register is ignored.

Normal Setting: The default for this register is 7500 millivolts. For 2-cell applications, this can cause production issues with writing to the data flash because at nominal cell voltages, 2-cell applications can easily be below 7500 millivolts. The way to solve this problem is to connect a charger voltage to the battery which overrides this register while connected. Ensure that this register is set to a voltage where the battery has plenty of capacity to support data flash writes but below any normal battery operation conditions.

Shutdown Voltage

The bq20z80 goes into shutdown mode when **Voltage** falls below the *Shutdown Voltage* for at least Shutdown Time seconds. Also **Current** must be less than 0 and the **Pack Voltage** must be less than *Charger Present* for the entire time. (See *Shutdown Time*)

Normal Setting: This voltage should be far below any normal operating voltage but above any threshold that can cause damage to the cells. This threshold is met after the Charge and Discharge FETs are turned off from an under voltage fault condition.

Shutdown Time

When the following conditions are met:

1. **Voltage** is below *Shutdown Voltage*.
2. **Current** is less than 0.
3. **Pack Voltage** less than *Charger Present*

Then the *Shutdown Time* timer is initiated. If the above conditions remain until the *Shutdown Time* timer expires, then the bq20z80 goes into shutdown mode. Every time the bq20z80 wakes up from shutdown mode, then the *Shutdown Time* timer is reset meaning it is not possible for the bq20z80 to go back into shutdown mode for *Shutdown Time* seconds after waking. When in shutdown mode, VCC is completely removed from the bq20z80 by the bq29312A. (See *Shutdown Voltage*)

Normal Setting: The default for this register is 10 seconds. Between 10–20 seconds is acceptable for most applications. It is recommended not to go below 10 seconds to prevent an oscillation going into and out of shutdown mode.

Charger Present

A charger is deemed present when **Pack Voltage** is at or above this level.

Normal Setting: It is important to note that a charger detection because this function prevents shutdown by either a **Manufacture Access** command or *Shutdown Voltage*. Some applications with external voltage sources can confuse the shutdown detection which prevents the bq20z80 shutdown mode from functioning properly. The bq29312A wakes up with a voltage above the “Start-up” voltage which is a wake up feature built into the bq29312A (see the bq29312A data sheet ([SLUS629A](#))). If there is an external voltage source that has a voltage above the “Start-up” voltage threshold, but below the *Charger Present* threshold, then the bq20z80 oscillates between awake and shutdown. This causes abnormal operational side effects. Therefore, it is recommended that *Charger Present* be set to 3500 mV if there are any external voltage sources. Otherwise, this voltage can be set to between $(3000-4000 \text{ mV per cell}) \times (\text{number of cells})$.

Sleep Current

When **Current** is less than *Sleep Current* or greater than $(-)\text{Sleep Current}$ in milliAmps and the following conditions are met:

1. **Temperature** is between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High*
2. SMBus clock and data lines are low for more than *Bus Low Time seconds*.
3. [Sleep] is set in *Operation Cfg A*.

Then the bq20z80 does a *CC Offset* calibration, and then goes to sleep.

Normal Setting: This setting should be below any normal application currents. The default is 10 mA which should be sufficient for most applications.

Bus Low Time

When SMBus clock and data lines are low for more than *Bus Low Time* seconds and the following conditions are met:

1. **Current** is less than *Sleep Current* or greater than $(-)\text{Sleep Current}$ in milliAmps
2. **Temperature** is between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High*.

Then the bq20z80 does a *CC Offset* calibration and then goes to sleep. [Sleep] in *Operation Cfg A* does not affect the calibration portion of this detection.

Normal Setting: This setting should be below any normal application currents. The default is 5 seconds which should be sufficient for most applications. Do not go below 2 seconds to protect against false triggering.

Cal Inhibit Temp Low

For the bq20z80 to perform a *CC Offset* and ADC offset calibration prior to entering sleep mode, **Temperature** must be between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High* along with the following conditions:

1. **Current** is less than *Sleep Current* or greater than $(-)\text{Sleep Current}$ in milliAmps.
2. SMBus clock and data lines are low for more than *Bus Low Time seconds*.

Normal Setting: The default for this application is 5° or 50 in 0.1°C units. This should not need to be changed. The bq20z80 does not need to do a *CC Offset* calibration every time the bq20z80 goes to sleep and it definitely does not need to do it at extreme temperatures to prevent temperature drift from decreasing the offset calibration accuracy.

Cal Inhibit Temp High

For the bq20z80 to perform a *CC Offset* and internal ADC offset calibration prior to entering sleep mode, **Temperature** must be between *Cal Inhibit Temp High* and *Cal Inhibit Temp High* along with the following conditions:

1. **Current** is less than *Sleep Current* or greater than (–)*Sleep Current* in milliAmps
2. SMBus clock and data lines are low for more than *Bus Low Time* seconds

Normal Setting: The default for this application is 45° or 450 in 0.1°C units. This should not need to be changed. The bq20z80 does not need to do a *CC Offset* calibration every time the bq20z80 goes to sleep and it definitely does not need to do it at extreme temperatures to prevent temperature drift from decreasing the offset calibration accuracy.

Sleep Voltage Time

While in sleep mode, the bq20z80 wakes up to measure and updates **Voltage**, **Cell Voltage(All)** and **Temperature** every *Sleep Voltage Time* in seconds.

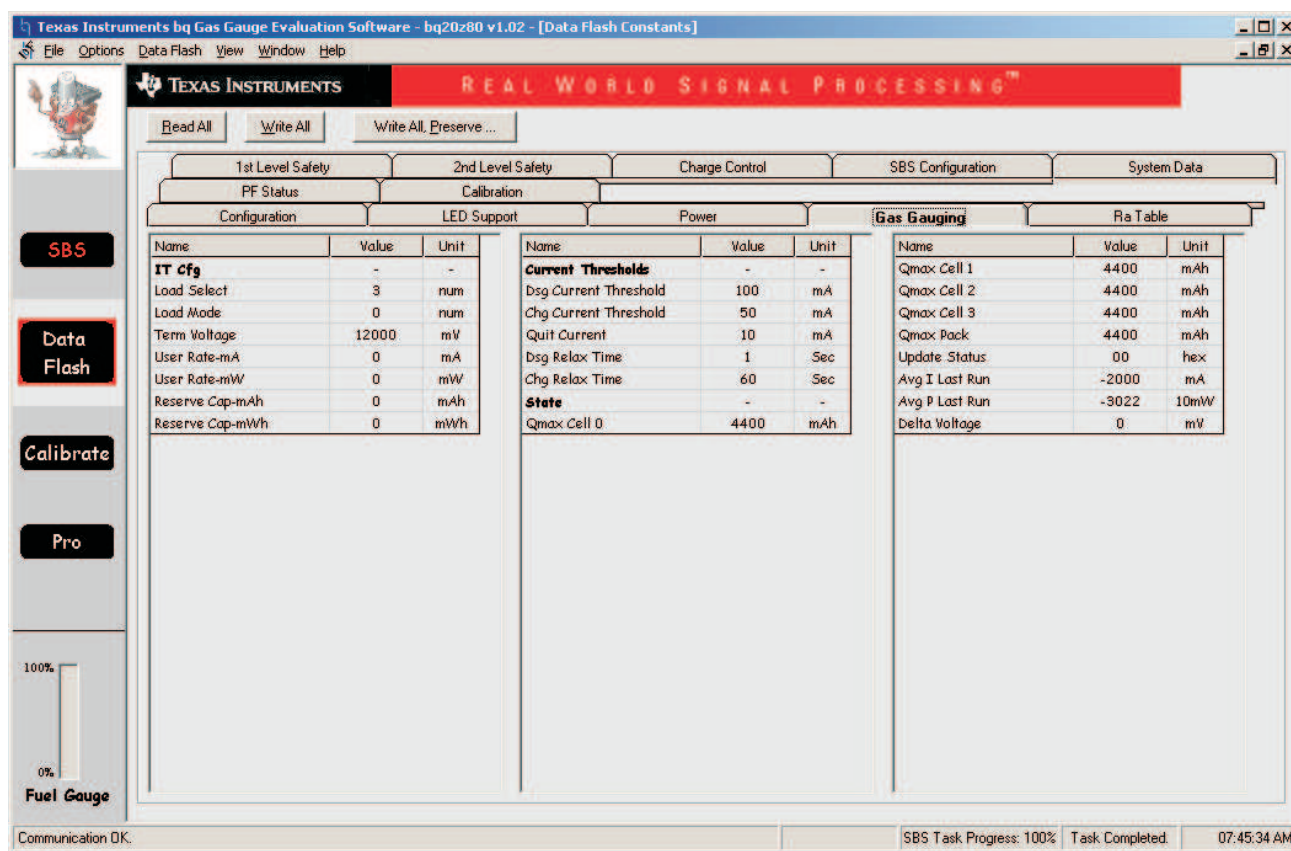
Normal Setting: The default for this register is 5 seconds. It is important to note for the settings of this register that it takes time to measure and update the voltage and temperature registers and the bq20z80 is awake and consuming power during this process. The more the bq20z80 is awake, the more it consumes. There is a trade off between voltage detection and power consumption. It is also important to note that the bq29312A (AFE) protection is still active and not affected by sleep.

Sleep Current Time

While in sleep mode, the bq20z80 wakes up to measure and update **Current** and **Average Current** every *Sleep Current Time* in seconds. Immediately after this update the bq20z80 goes back to sleep unless **Current** is above *Sleep Current* during one of these wake up periods. If it is above *Sleep Current*, then the part stays awake until the sleep conditions are met again (See *Sleep Current*).

Normal Setting: The default for this register is 20 seconds. It is important to note for the settings of this register that it takes about 1 second to measure and update the current registers and the bq20z80 is awake and consuming power during this process. The more the bq20z80 is awake, the more it consumes. There is a trade off between current detection and power consumption. It is also important to note that the bq29312A (AFE) protection is still active and not affected by sleep.

12 Gas Gauging



12.1 IT Config

Load Select

Load Select defines the type of power or current model to be used for Remaining Capacity computation in the Impedance Track™ algorithm. If *Load Mode* = Constant Current then the following options are available:

- 0 = Average discharge current from previous cycle: There is an internal register that records the average discharge current through each entire discharge cycle. The previous average is stored in this register.
- 1 = Present average discharge current: This is the average discharge current from the beginning of this discharge cycle till present time.
- 2 = **Current**: based off of **Current**
- 3 = **Average Current** (default): based off the **Average Current**
- 4 = **Design Capacity** / 5: C Rate based off of **Design Capacity** / 5 or a C / 5 rate in mA.
- 5 = **AtRate** (mA): Use whatever current is in **AtRate**
- 6 = *User_Rate-mA*: Use the value in *User_Rate-mA*. This gives a completely user configurable method.

If *Load Mode* = Constant Power then the following options are available:

- 0 = Average discharge power from previous cycle: There is an internal register that records the average discharge power through each entire discharge cycle. The previous average is stored in this register.
- 1 = Present average discharge power: This is the average discharge power from the beginning of this discharge cycle till present time.
- 2 = **Current × Voltage**: based off of **Current** and **Voltage**
- 3 = **Average Current × Voltage** (default): based off the **Average Current** and **Voltage**
- 4 = **Design Energy / 5**: C Rate based off of **Design Energy / 5** or a C / 5 rate in mA
- 5 = **AtRate** (10 mW): Use whatever value is in **AtRate**.
- 6 = **User_Rate-10mW**: Use the value in **User_Rate-mW**. This gives a completely user configurable method.

Normal Setting: The default for this register is 3 which should be acceptable for most applications. This is application dependent.

Load Mode

Load Mode is used to select either the constant current or constant power model for the Impedance Track™ algorithm as used in *Load Select*. (See *Load Select*)

- 0: Constant Current Model
- 1: Constant Power Model

Normal Setting: This is normally set to Current Model but It is application specific. If the application load profile more closely matches a constant power model, then set to 1. This provides a better estimation of remaining run-time, especially close to the end of discharge where current increases to compensate for decreasing battery voltage.

Term Voltage

Term Voltage is used in the Impedance Track™ algorithm to help compute **Remaining Capacity**. This is the absolute minimum voltage for end of discharge, where the remaining chemical capacity is assumed as zero.

Normal Setting: This register is application dependent. It should be set based on battery cell specifications to prevent damage to the cells or the absolute minimum system input voltage taking into account impedance drop from the PCB traces, FETs, and wires.

User Rate-mAh

User Rate-mAh is only used if *Load Select* is set to 6 and *Load Mode* = 0. If these criteria are met then the current stored in this register is used for the **Remaining Capacity** computation in the Impedance Track™ algorithm. This is the only function that uses this register.

Normal Setting: It is unlikely that this register is used. An example application that would require this register is one that has increased predefined current at the end of discharge. With this type of discharge, it is logical to adjust the rate compensation to this period because the IR drop during this end period is effected the moment Term Voltage is reached.

User Rate-10mWh

User Rate-10mWh is only used if *Load Select* is set to 6 and *Load Mode* = 1. If these criteria are met then the power stored in this register is used for the **Remaining Capacity** computation in the Impedance Track™ algorithm. This is the only function that uses this register.

Normal Setting: It is unlikely that this register is used. An example application that would require this register is one that has increased predefined power at the end of discharge. With this application. it is logical to adjust the rate compensation to this period because the IR drop during this end period is effected the moment Term Voltage is reached.

Reserve Cap-mAh

Reserve Cap-mAh determines how much actual remaining capacity exists after reaching SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) = 0% before *Term Voltage* is reached. This register is only used if *Load Mode* is set to 0. There are 2 ways to interpret this register depending on [RESCAP] in *Operation Cfg B*:

- [RESCAP]=0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity
- [RESCAP]=1: If set to a 1, then a higher rate of load compensation as defined by *Load Select* is applied to this reserve capacity. (See *Load Select*)

This register is only used if in mA mode (configured by [CAPM] in **Battery Mode**).

Normal Setting: This register defaults to 0 which disables this function. This is the most common setting for this register. This register is application dependent. This is a specialized function for allowing time for a controlled shutdown after 0% capacity is reached. There are other functions that can serve this purpose like *Remaining Time Alarm* or *Remaining Capacity Alarm*.

Reserve Cap-10mWh

Reserve Cap-10mWh determines how much actual remaining capacity exists after reaching SOC% (**ASOC** or **RSOC** depending on [DMODE] in *Operation Cfg A*) = 0% before *Term Voltage* is reached. This register is only used if *Load Mode* is set to 1. There are 2 ways to interpret this register depending on [RESCAP] in *Operation Cfg B*:

- 0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity
- 1: If set to a 1, then a more normal rate of load compensation as defined by *Load Select* is applied to this reserve capacity. (See *Load Select*)

This register is only used if in mW mode (configured by [CAPM] in **Battery Mode**).

Normal Setting: This register defaults to 0 which basically disables this function. This is the most common setting for this register. This register is application dependent. This is a specialized function for allowing time for a controlled shutdown after 0% capacity is reached. There are other functions that can serve this purpose like *Remaining Time Alarm* or *Remaining Capacity Alarm*.

12.2 Current Thresholds

Dsg Current Threshold

This register is used as a threshold by many functions in the bq20z80 to determine if actual discharge current is flowing into and out of the part. This is independent from [DSG] in **Battery Status** which indicates whether the bq20z80 is in discharge mode or charge mode.

Normal Setting: SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. If the bq20z80 is charging, then [DSG] is 0 and any other time (**Current** less than or equal to 0) the [DSG] flag is equal to 1. Many algorithms in the bq20z80 require more definitive information about whether current is flowing in either the charge or discharge direction. *Dsg Current Threshold* is used for this purpose. The default for this register is 100 mA which should be sufficient for most applications. This threshold should be set low enough to be below any normal application load current but high enough to prevent noise or drift from affecting the measurement.

Chg Current Threshold This register is used as a threshold by many functions in the bq20z80 to determine if actual charge current is flowing into and out of the part. This is independent from [DSG] in **Battery Status** which indicates whether the bq20z80 is in discharge mode or charge mode. **Normal Setting:** SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. Basically, if the bq20z80 is charging then [DSG] is 0 and any other time (Current less than or equal to 0) the [DSG] flag is equal to 1. Many algorithms in the bq20z80 require more definitive information about whether current is flowing in either the charge or discharge direction. This is what *Dsg Current Threshold* is used for. The default for this register is 100 mA which should be sufficient for most applications. This threshold should be set low enough to be below any normal application load current but high enough to prevent noise or drift from affecting the measurement.

Quit Current

The *Quit Current* is used as part of the Impedance Track™ algorithm to determine when the bq20z80 goes into relaxation mode from a current flowing mode in either the charge direction or the discharge direction. Either of the following criteria must be met to enter relaxation mode:

1. **Current** is less than (–)*Quit Current* and then goes within (±)*Quit Current* for *Dsg Relax Time*.
2. **Current** is greater than *Quit Current* and then goes within (±)*Quit Current* for *Chg Relax Time*.

After about 30 minutes in relaxation mode, the bq20z80 attempts to take accurate OCV readings. An additional requirement of $dV/dt < 4$ microvolts/sec (delta voltage over delta time) is required for the bq20z80 to do Qmax updates. These updates are used in the Impedance Track™ algorithms.

Normal Setting: It is critical that the battery voltage be relaxed during OCV readings to get the most accurate results. This current must not be higher than C/20 when attempting to go into relaxation mode; however, it should not be so low as to prevent going into relaxation mode due to noise. This should always be less than *Chg Current Threshold* or *Dsg Current Threshold*.

Dsg Relax Time

The *Dsg Relax Time* is used in the function to determine when to go into relaxation mode. When **Current** is less than $(-)\text{Quit Current}$ and then goes within $(\pm)\text{Quit Current}$ the *Dsg Relax Time*, timer is initiated. If the current stays within $(\pm)\text{Quit Current}$ until the *Dsg Relax Time* timer expires, then the bq20z80 goes into relaxation mode. After about 30 minutes in relaxation mode, the bq20z80 attempts to take accurate OCV readings. An additional requirement of $dV/dt < 4$ microvolts/sec (delta voltage over delta time) is required for the bq20z80 to do Qmax updates. These updates are used in the Impedance Track™ algorithms.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This is application specific.

Chg Relax Time

The *Chg Relax Time* is used in the function to determine when to go into relaxation mode. When **Current** is greater than *Quit Current* and then goes within $(\pm)\text{Quit Current}$ the *Chg Relax Time*, timer is initiated. If the current stays within $(\pm)\text{Quit Current}$ until the *Chg Relax Time* timer expires, then the bq20z80 goes into relaxation mode. After about 30 minutes in relaxation mode, the bq20z80 attempts to take accurate OCV readings. An additional requirement of $dV/dt < 4$ microvolts/sec (delta voltage over delta time) is required for the bq20z80 to do Qmax updates. These updates are used in the Impedance Track™ algorithms.

Normal Setting: This is application specific.

12.3 State

Qmax Cell 0

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z80 continuously during use to keep capacity measuring as accurate as possible.

Normal Setting: Initially should be set to battery cell data-sheet capacity.

Qmax Cell 1

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z80 continuously during use to keep capacity measuring as accurate as possible.

Normal Setting: Initially should be set to battery cell data-sheet capacity.

Qmax Cell 2

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z80 continuously during use to keep capacity measuring as accurate as possible.

Normal Setting: Initially should be set to battery cell data sheet capacity.

Qmax Cell 3

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z80 continuously during use to keep capacity measuring as accurate as possible.

Normal Setting: Initially should be set to battery cell data-sheet capacity.

Qmax Pack

This is the maximum capacity of the entire battery pack. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated to the lowest chemical capacity of all the cells (*Qmax Cell 0* – *Qmax Cell 3*) by the bq20z80 continuously during use to keep capacity measuring as accurate as possible.

Normal Setting: Initially should be set to battery cell data sheet capacity. It is updated with the capacity of the lowest cell during use. This is because the capacity of the entire battery is only as much as the capacity of the lowest cell. When that cell is empty, it does not matter if any other cells have capacity.

Update Status

There are 2 bits in this register that are important.

- Bit 1 (0x02) indicates that the bq20z80 has learned new Qmax parameters and is accurate.
- Bit 2 (0x04) indicates whether Impedance Track™ algorithm is enabled.

The remaining bits are reserved.

Normal Setting: These bits are user configurable; however, bit 1 is also a status flag that can be set by the bq20z80. These bits should never be modified except when creating a golden image file as explained in the application note “Preparing Optimized Default Flash Constants for specific Battery Types” (see [SLUA334](#).pdf). Bit 1 is updated as needed by the bq20z80 and Bit 2 is set with

Manufacturers Access command 0x0021.

Avg I Last Run

The bq20z80 logs the **Current** averaged from the beginning to the end of each discharge cycle. It stores this average current from the previous discharge cycle in this register.

Normal Setting: This register should never need to be modified. It is only updated by the bq20z80 when required.

Avg P Last Run

The bq20z80 logs the power averaged from the beginning to the end of each discharge cycle. It stores this average power from the previous discharge cycle in this register. To get a correct average power reading the bq20z80 continuously multiplies **Current** times **Voltage** to get power. It then logs this data to derive the average power.

Normal Setting: This register should never need to be modified. It is only updated by the bq20z80 when the required.

Delta Voltage

The exact computation of this register is very complex so this description, while not exact, gives the general formula. Delta Voltage is derived as a function average Voltage versus immediate **Voltage**. The average **Voltage** is a localized average over the most recent few seconds. The *Delta Voltage* is the maximum (average **Voltage** – **Voltage**) at any given time. This register is only updated whenever the algorithm computes a value greater than the previous. Every SOC gridpoint (see *Cell0 R_a0*) causes a sort of reset of this computation. To prevent a 0 value in this register and to give more meaning, the reset algorithm uses a percentage of the previous SOC gridpoint *Delta Voltage* to compute a reset value and then starts the process of computing maximum *Delta Voltage* values again.

Normal Setting: This register should never need to be modified. It is only updated by the bq20z80 when required.

Each subclass (R_a0-R_a3 and R_a0x-R_a3x) in the Ra Table class is a separate profile of resistance values normalized at 0 degrees for each of the cells in a design (cells 0–3) There are 2 profiles for each cell. They are denoted by the x or absence of the x at the end of the subclass Title:

R_a0 or **R_a0x** for cell 0

R_a1 or **R_a1x** for cell 1

R_a2 or **R_a2x** for cell 2

R_a3 or **R_a3x** for cell 3

The purpose for 2 profiles for each series cell is to ensure that at any given time there is at least one profile is enabled and being used while attempts can be made to update the alternate profile without interference. Having 2 profiles also helps reduce stress on the Flash Memory. At the beginning of each of the 8 subclasses (profiles) is a flag called *CellM R_a flag* or *xCellM R_a flag* where “M” is the cell number (0-3). This flag is a status flag indicates the validity of the table data associated with this flag and whether this particular table is enabled/disabled. There are 2 bytes in each flag:

1. The LSB (least significant byte) indicates whether the table is currently enabled or disabled. It has the following options:
 - (a) 0x00 : means the table has had a resistance update in the past; however, it is not the currently enabled table for this cell. (the alternate table for the indicated cell must be enabled at this time)
 - (b) 0xff: This means that the values in this table are default values. This table resistance values have never been updated, and this table is not the currently enabled table for this cell. (the alternate table for the indicated
 - (c) 0x55: This means that this table is enabled for the indicated cell (the alternate table must be disabled at this time.) cell must be enabled at this time)
2. The MSB (Most significant byte) indicates that status of the data in this particular table. The possible values for this byte are:
 - (a) 0x00: The data associated with this flag has had a resistance update and the *QMax Pack* has been updated
 - (b) 0x05: The resistance data associated with this flag has been updated and the pack is no longer discharging (this is prior to a *Qmax Pack* update).
 - (c) 0x55: The resistance data associated with this flag has been updated and the pack is still discharging (Qmax update attempt not possible until discharging stops).
 - (d) 0xff: The resistance data associated with this flag is all default data.

This data is used by the bq20z80 to determine which tables need updating and which tables are being used for the Impedance Track™ algorithm.

Normal Setting: This data is used by the bq20z80 Impedance Track™ algorithm. The only reason this data is displayed and accessible is to give the user the ability to update the resistance data on golden image files. This description of the *xCellM R_a flags* are intended for information purposes only. It is not intended to give a detailed functional description for the bq20z80 resistance algorithms.

Cell0 R_a0 – Cell0 R_a14,

Cell2 R_a0 – Cell2 R_a14,

xCell0 R_a0 – xCell0 R_a14,

xCell2 R_a0 – xCell2 R_a14,

Cell1 R_a0 – Cell1 R_a14,

Cell3 R_a0 – Cell3 R_a14,

xCell1 R_a0 – xCell1 R_a14,

xCell3 R_a0 – xCell3 R_a14,

There are 15 values for each R_a subclass in the **Ra Table** class. Each of these values represent a resistance value normalized at 0°C for the associated *Qmax Pack* based SOC gridpoint as found by the following rules:

For *CellN R_aM* where:

1. if $0 \leq M \leq 8$: The data is the resistance normalized at 0° for: $SOC = 100\% - (M \times 10\%)$
2. if $9 \leq M \leq 14$: The data is the resistance normalized at 0 degrees for: $SOC = 100\% - [80\% + (M - 8) \times 3.3\%]$

This gives a profile of resistance throughout the entire SOC profile of the battery cells concentrating more on the values closer to 0%.

Normal Setting: SOC as stated in this description is based on *Qmax Pack*. It is not derived as a function of RSOC or ASOC. These resistance profiles are used by the bq20z80 for the Impedance Track™ algorithm. The only reason this data is displayed and accessible is to give the user the ability to update the resistance data on golden image files. This resistance profile description is for information purposes only. It is not intended to give a detailed functional description for the bq20z80 resistance algorithms. It is important to note that this data is in units of milliohms and is normalized to 0°C. Useful observations to note with this data throughout the application development cycle:

1. Watch for negative values in the **Ra Table** class. There should never be negative numbers in profiles anywhere in this class.
2. Watch for smooth consistent transitions from one profile gridpoint value to the next throughout each profile. As the bq20z80 does resistance profile updates these values should be roughly consistent from one learned update to another without huge jumps in consecutive gridpoints.

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