Application Report
SLUA808–May 2017

Layout Guidelines for the bq2570x Switching Charger

Wang Li

ABSTRACT

For a high-frequency, switching regulated, power-supply design, layout is very important for EMI performance, thermal performance, and component selection. Specifically, the bq2570x buck-boost charger includes buck-switching FETs, boost-switching FETs, and a novel input-current sensing circuit which needs a careful layout design. This application note gives layout guidelines to optimize the bq2570x switching mode charger layout.

Contents

List of Figures

Trademarks

1 Power Stage Layout Guideline

A synchronous buck power stage has two states: Q1 on and Q2 off state (input current loop in Figure 1); Q1 off and Q2 on state (output current loop in Figure 1). If it is assumed that the inductor current L filters out most of its AC current, the high-frequency loop is the difference between the Q1 on state and Q1 off state. The switching noise comes from this high-frequency loop because the magnetic field keeps changing in this loop area for every switching cycle. For the same principle, the boost switching FETs and output capacitor loop is the boost mode high-frequency loop (Figure 2). To minimize the switching noise and minimize the voltage spike across the switching MOSFET, it is necessary to keep this loop as small and short as possible.

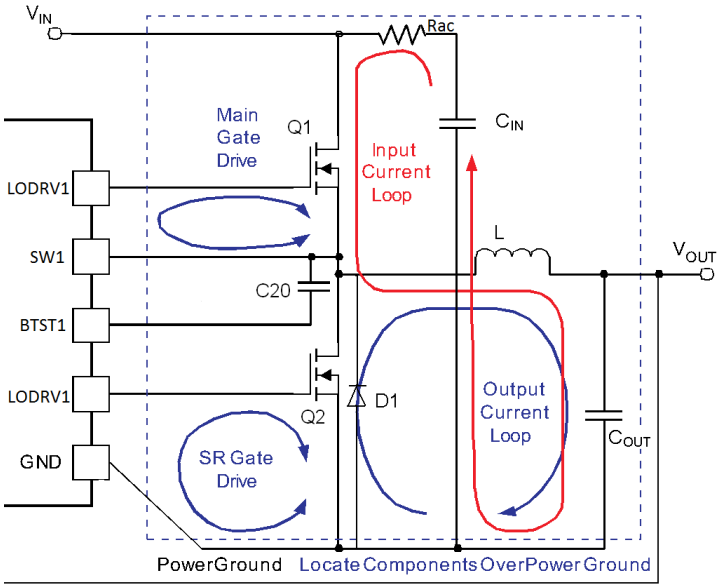


Figure 1. Synchronous Buck Power Stage

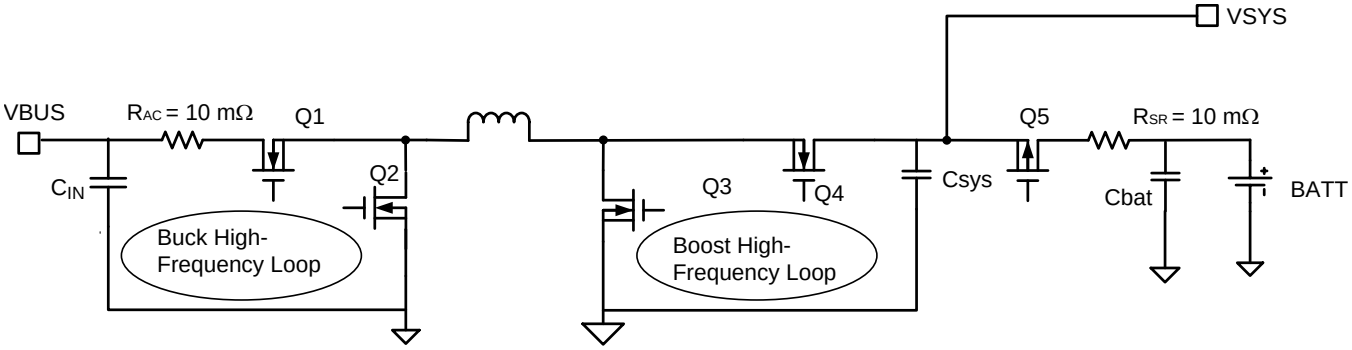


Figure 2. Buck and Boost Power Stage High-Frequency Loop

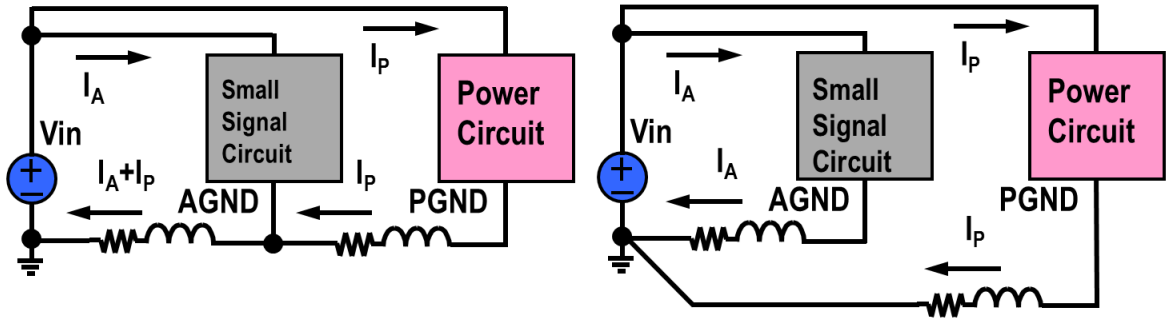
Make all of the power (high current) traces as short, direct, and thick as possible. Keep the loop area small. This reduces the EMI radiated; parasitic inductance and resistance which, in turn, reduces noise spikes, ringing, and power losses. A high-frequency capacitor can return high-frequency noise to ground. TI recommends a small-size capacitor between the switching FET ground and the high-side FET drain. This solution works effectively between the 100-MHz and 200-MHz range.

2 Ground Connection Guideline

Control all parasitic inductance within an acceptable level. With a reasonable parasitic inductance, a high di/dt trace can still generate a noise voltage. If this noise can be coupled to other sensitive circuits, the noise path from the noise source circuit to the other small signal circuit must be eliminated.

In Figure 3, the power circuit represents a power stage circuit, such as power FETs and filter inductor and capacitors; the small signal circuit represents the charge controller; charging parameter setting circuit; sensing circuits; communication circuit or all other small current circuits.

The ground current to the power circuit should not go through the small signal circuit ground. So, high di/dt noise in the power circuit does not affect the small signal circuit.



A. Power circuit noise couples to Analog circuit B. Power circuit noise decouples to Analog circuit

Figure 3. Ground Layout Example

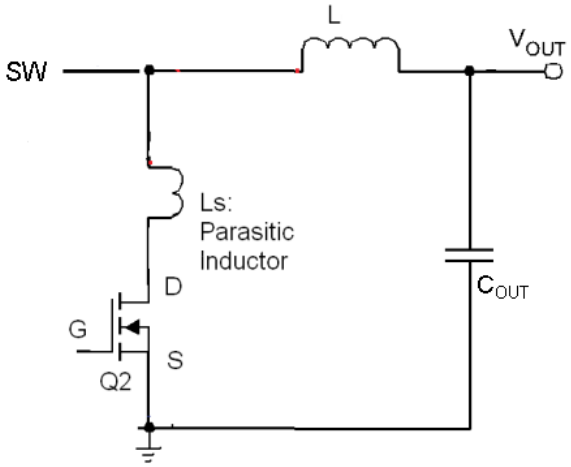


Figure 4. Parasitic Inductor Model

If this negative voltage on the parasitic inductor (Ls) is high enough, it biases an internal PN diode in the SW pin ESD cell, injecting minority carriers into the substrate. This substrate current is collected by adjacent circuits, and then an abnormal mode may be triggered. Position the IC close to the low-side switching ground of the FET.

3 Small-Signal Circuit Capacitor Layout Guideline

The VBUS pin, REGN pin, VDDA, and BTST pin requests a local bypass filter capacitor. Those **capacitors can filter out high-frequency noise and can also act as a small local power supply for ICs**. The REGN and BTST capacitor could have a high di/dt during the power FET switching. Put the REGN and BTST capacitors as close as possible to the charge IC.

COMP1 and COMP2 are related to the loop control of the converter and PFM and PWM operation control. To avoid the extra ground noise, use an independent ground route back to IC pin ground.

The ILIM_HIZ pin, IADP pin, IBAT pin and PSYS pin are small analog signal pins. Put the capacitor near the charger IC.

SCL, SDA, CHRG_OK, EN_OTG, PROCHOT, CELL_BATPRES, CMPIN and CMPOUT are also small signal pins Do not let a high current circuit share the ground with them.

4 Reduce Noise Coupling Guideline

4.1 Reduce Noise Coupling on Current Sensing Circuit

The current sensing resistor should have a Kelvin connection. Route the sense trace close to each other from the sensing resistor back to the IC to minimize loop area and do not route the sense trace through the high-frequency loop or near switching FETs, inductor, or high di/dt trace. Keep the trace as short as possible. Also, do not let the ACP/ACN sensing trace share with the VBUS trace, this can introduce noise to the input current sensing.

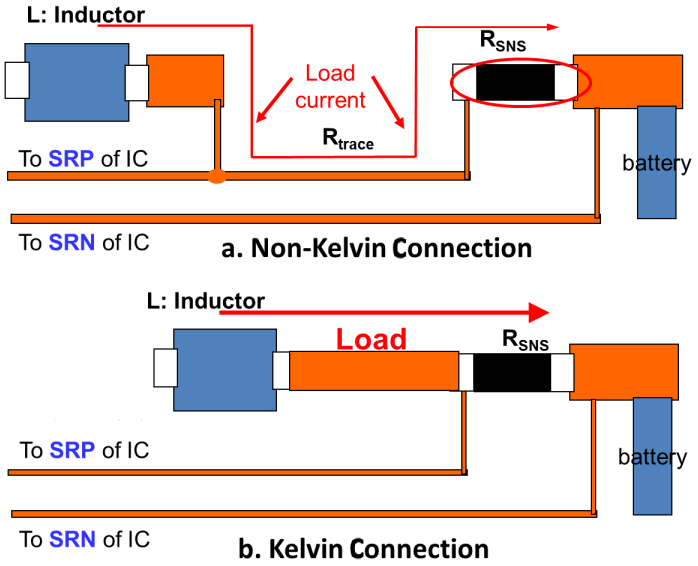


Figure 5. Non-Kelvin (a) and Kelvin Connections (b)

4.2 Reduce Switching Node Copper Coupling

The switching node voltage swings from high input or output voltage to ground every switching cycle. Keep the switching node pad, copper or trace between inductor, source of high-side MOSFET, and the drain of the low-side MOSFET as small as possible to reduce the parasitic capacitance between switching node and any other components and to minimize the radiated EMI emission. Also, do not route small signal traces above or underneath the switching node polygon directly.

4.3 Power Stage Component Placement and Ground Layer Guideline

A power ground layer is commonly used on a switching converter layout. The ground layer has a heavy copper coverage which spreads the heat quicker and shields the noise from the power stage component. If the ground layer is the next layer following the power stage layer, the ground layer copper gets the lowest thermal resistance; smallest high-frequency loop area and shield most of the rest circuit from the high-noise power stage. Also, if all high-current loop components are pout on the same layer, the magnetic field lines are vertical to the board. So, the ground copper layer can provide the best shielding performance between the power stage circuit and other small signal circuits on the board.

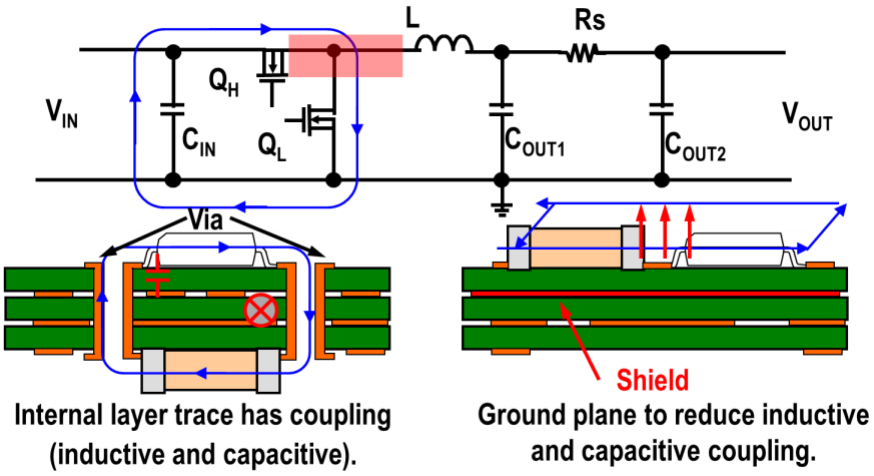


Figure 6. Power Stage Component Placement and Ground Layer

5 Gate-Drive Layout Guideline

Keep the gate-drive loop impedance (HIDRV-gate-source-SW and LODRV-gate-source-PGND) as low as possible. Widen the HIDRV and LODRV trace to the gate of the MOSFET enough to handle a high-peak current spike. Minimize the inductance of gate-drive traces. Keep gate-drive traces as short and wide as practical and include a return path directly below the gate trace. The use of a ground plane is a desirable way to return ground signals.

6 Design Example

The bq2570x evaluation module is a good example for PCB layout. See the *bq2570x Evaluation Module* user's guide (SLUUBG6) for the layout detail.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265