Application Report
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# Achieving the Optimal Thermal Performance for Chip Scale Package

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**ABSTRACT**

The Wafer Chip Scale Package (WCSP) is getting more popular in portable electronics due to its better electrical parameters, smaller size, and lower manufacturing cost. For example, for the same die size power conversion integrated circuit (IC), higher efficiency can be achieved in WCSP than the Quad Flat No-Leads (QFN) package. However, how to dissipate the power loss in a smaller area and keep the IC temperature cool becomes a big challenge, as this is critical for user experience in a power conversion IC. Printed-circuit board (PCB) layout plays a crucial role in achieving the best thermal performance. This application note details an experimental study of several versions of PCB layout and demonstrated techniques in PCB layout that can help improve WCSP thermal performance including power loss reduction, heat dissipation optimization, and other methods to keep temperature cool.

## Trademarks



## 1 Introduction

The silicon chip can be packaged with many options. QFN and WCSP are among the most popular options for the power converters. The QFN package fully encloses the silicon die in a plastic casing, making contacts to the circuit board through bond wires and lead frame, while the WCSP package makes direct interconnection from the silicon chip to the PCB through solder balls (shown in Figure 1). This reduces the footprint on the board to the minimum because the footprint is exactly the same size as the die. It also minimizes the parasitic resistance, inductance, and the weight by getting rid of extra bond wires, lead frame, and encapsulation. There is minimum electrical distance between the circuitry on the silicon and PCB. The interconnection is direct and through a very wide channel, namely solder ball array. By completely eliminating the wire bonds as well as any substrate related impedance, WCSP provides excellent electrical performance. It helps to achieve a total solution with better efficiency, less expense, smaller footprint size, lower height, and lighter weight.

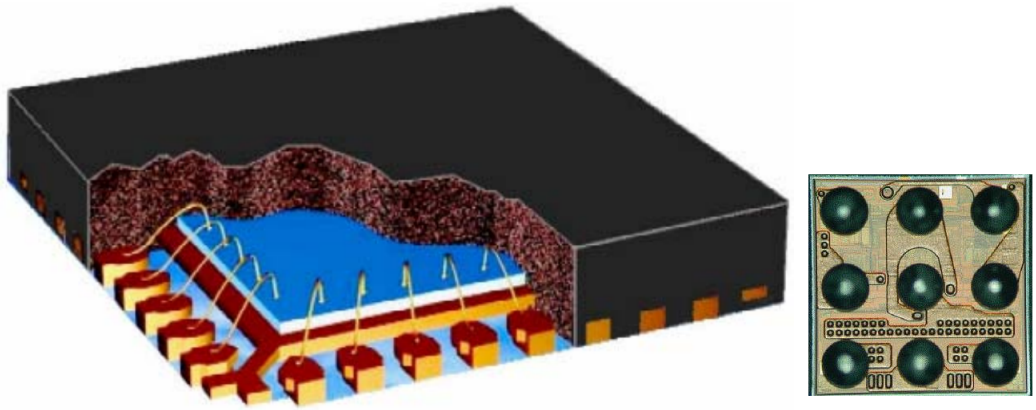

**Figure 1. Comparison of QFN (Left) and WCSP (Right) Package**

These unique features make WCSP very attractive in portable devices, such as smart phones, navigation devices, tablets, and so forth. More and more ICs have adopted this package, including power conversion devices such as a charger. Although the efficiency is higher due to lower resistance, the remaining challenge is how to achieve the best thermal performance. Due to the small size, the WCSP package has higher junction-to-ambient thermal resistance ($R_{\theta JA}$). For the same IC, QFN $R_{\theta JA}$ is about 32.6°C/W while WCSP can go as high as 55.8°C/W. Remaining cool during high power operation, like high current charging, becomes very challenging.

This application note presents the experimental study about how to achieve the best thermal performance by comparing several versions of PCB layout for a high current battery charger. The techniques to help not only reduce power loss, but also facilitate thermal dissipation have been demonstrated with experimental verification of improved WCSP thermal performance.

## 2 Power Loss Reduction

The most popular charger used in high power applications is a switching charger. There are three major components of power losses related to the battery charger IC: conduction loss, switching loss, and gate driver loss.

PCB layout plays a very important role in reducing the switching loss and conduction loss. The switching rising and falling time are one of the important factors of the switching loss. For a good layout, it is critical to place all key components in the proper place and to rout them properly so that high-frequency current path loop is minimized and does not have a big impact to the switching time as Figure 1 shows. The layout also helps the reduction of copper conduction loss on the trace. Another benefit of the minimized input current loop also alleviates the electrical and magnetic field radiation and high-frequency resonant problems.

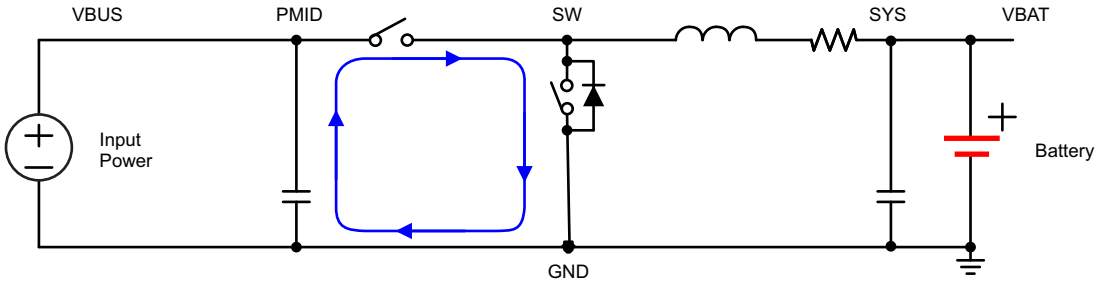


**Figure 2. High-Frequency Current Loop in a Switching Charger**

When efficiency is in the 90% range, power loss is about 10%. Thus, a 1% addition to a higher efficiency will bring in about a 10% reduction on power loss, and hence a big percentage reduction on temperature increase as a large portion of the lost power is converted into heat.

Due to the smaller size of WCSP, component placement becomes even more critical. For applications with constrained area, there would be not enough space to place all key components in ideal locations. IC pins are crowded into a square or rectangle array and it is difficult to make traces out. Priorities must be taken.

First, decoupling capacitors should be put as close as possible to the converter input (for example, PMID in Figure 2) and output (for example, SYS in Figure 2) pins, traces should be the widest and the shortest. The area enclosed by the high-frequency current loop (be sure to include GND return path) should be kept to a minimum. All duplicate WCSP balls for each power pin should be used and connected. Maximum copper pours should be applied to high-current traces. This will not only reduce the voltage drop on the copper trace, thus generate less heat, but also help dissipate heat from the IC.

Next, inductors and other capacitors should be placed as close as possible to the corresponding IC pins. Place all decoupling capacitors close to their respective IC pins and as close as possible to GND.

Finally, the layout must manage GND appropriately. A dedicated GND plane is highly recommended. Make GND readily accessible to all return paths. Remaining portions of the PCB should be covered by GND with copper pour since copper is a good thermal conductor.

Figure 3 and Figure 4 are example layouts (Design #1), using the bq25898 IC (schematic simplified in Figure 2). All critical components (for example, capacitors of PMID, SYS, VBUS, and BAT) were put close to the die to reduce high-frequency current loop area. Maximum copper pours were used for all power lines. The entire PCB was almost covered by copper. On the right side are the top and bottom layout, on the left are thermal images of the PCB.

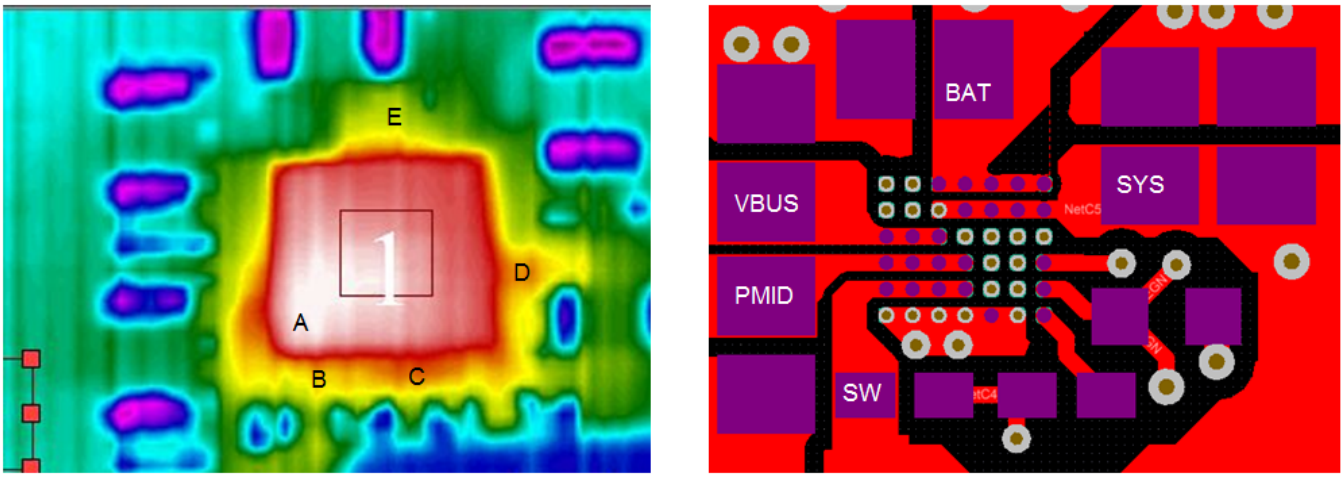


**Figure 3. Top Layer Layout and Thermal Image of Design #1**

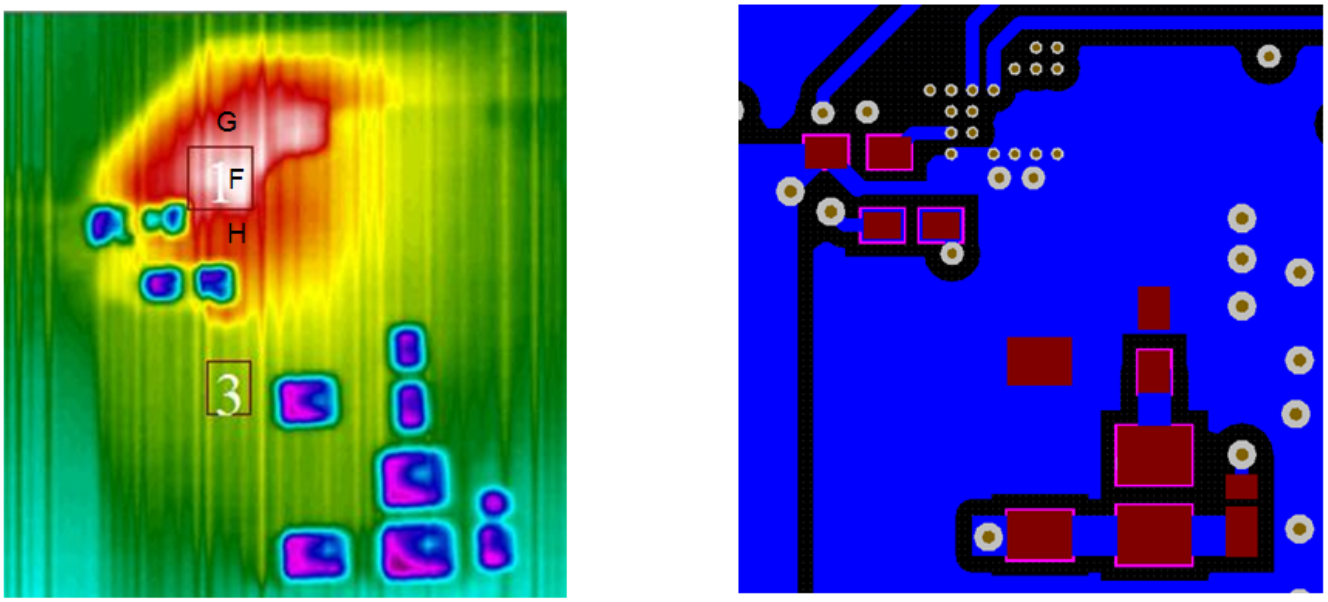


**Figure 4. Bottom Layer Layout and Thermal Image Of Design #1**

The thermal images were taken when the charger was operated with a 9-V adapter, 3.9-V battery, and 3-A charging current. There are some interesting points as labeled with alphabetic letters in Figure 3 and Figure 4:

- The lower left hand corner area, **A**, is where PMID, SW, and PGND are located. IR and switching losses are concentrated in this corner of the die. It easily becomes the hottest spot of the die.
- **B** and **C** are the PGND copper pour. Ideally this copper should be as big as possible. However, this PGND is trapped inside the SW-SYS-PGND loop. Bigger PGND pour will make the loop area bigger, thus more loss in power.
- **C** shares the same Cu pour as **B**, but **C** has no vias and is running a lot hotter than **B**. This shows the importance of Vias!

- Area **D** heat is carried out by short traces, but goes no further, thus it also gets hot.
- Area **E** is the high current BAT pin. Current flows out of the chip into battery from here. Unlike other power pins PMID or SYS, the BAT pin is at the edge. To take advantage of the multiple solder balls of this pin, copper trace is placed perpendicular to the ball line so that current is flowing at maximum from all balls. The triangle cut in the copper pour is intended to guide the current flow so that it is not overcrowded at the corner ball. However, it seems to block heat dissipation.
- Area **F** is the hottest area of the back side as multiple vias are concentrated here. Vias help transfer heat from the top to the bottom layer, but they do not seem to dissipate well after that. This is more obvious at **G**, where no copper is present.
- The copper vacancy in area **G** traps heat!
- Area **H** has similar via numbers but a much larger copper pour connected, thus it is cooler than **F**.

As seen in this analysis, even though there are a lot of considerations in this layout, further optimization is still needed.

## 3 Further Improvement With Layout

Knowing more optimization is needed, a new layout was implemented to optimize heat dissipation (Design #2). One major change was making the IC PGND a bigger copper pour. This further shortens the return path for PMID cap. Vias now connect SW to the inductor. Observe how the thermal picture changes in Figure 5 and Figure 6.

- As expected, the lower left hand corner, **A**, is still the hottest part of the die. However, the heat is spread across to the remaining die, rather than being contained within a smaller area.
- **B** and **C** are now one big PGND copper pour that serves like a heat sink and makes this edge of IC the coolest.
- **C** no longer shows any difference from **B**.
- **D** does not improve as some signal must be run out.
- With the triangle cut removed, **E** is sinking heat at full scale.
- **F** remains the hottest on the back side because of heat carried from the top layer by vias and PCB. The hot area has reduced dramatically due to the re-route of several lines.
- **G** is much cooler, due to the large GND copper pour connection.
- **H** is also much cooler, a big GND helps spread out the heat.

With this optimized PCB layout, temperature increase is reduced by 1°C to 3°C, depending on the test environment.

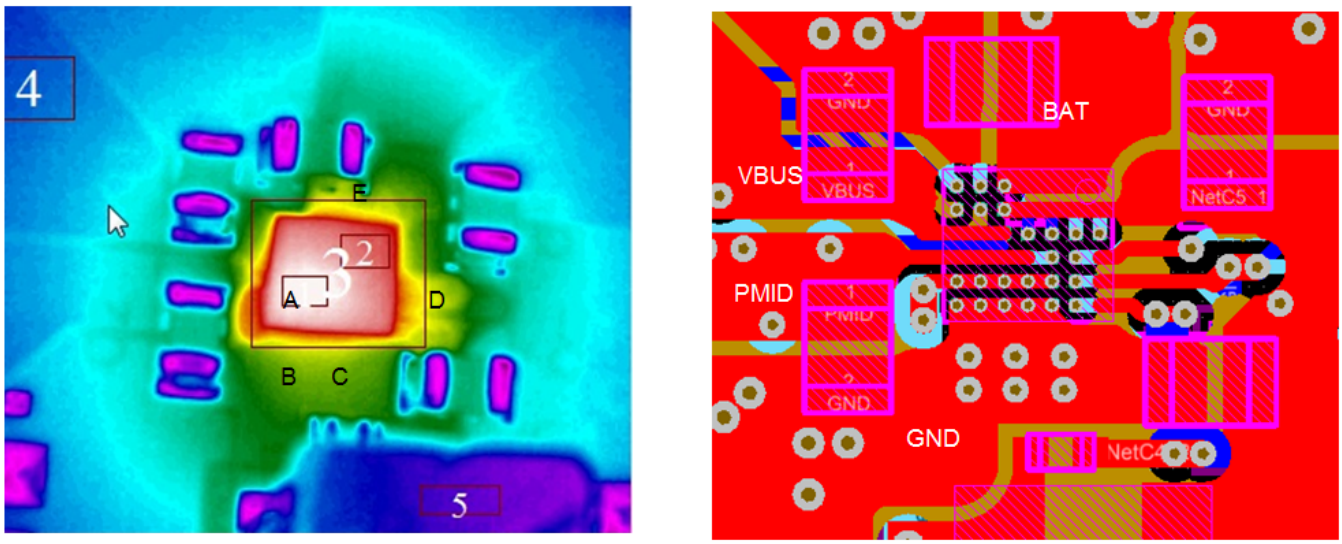


**Figure 5. Top Layer Layout and Thermal Image of Design #2**

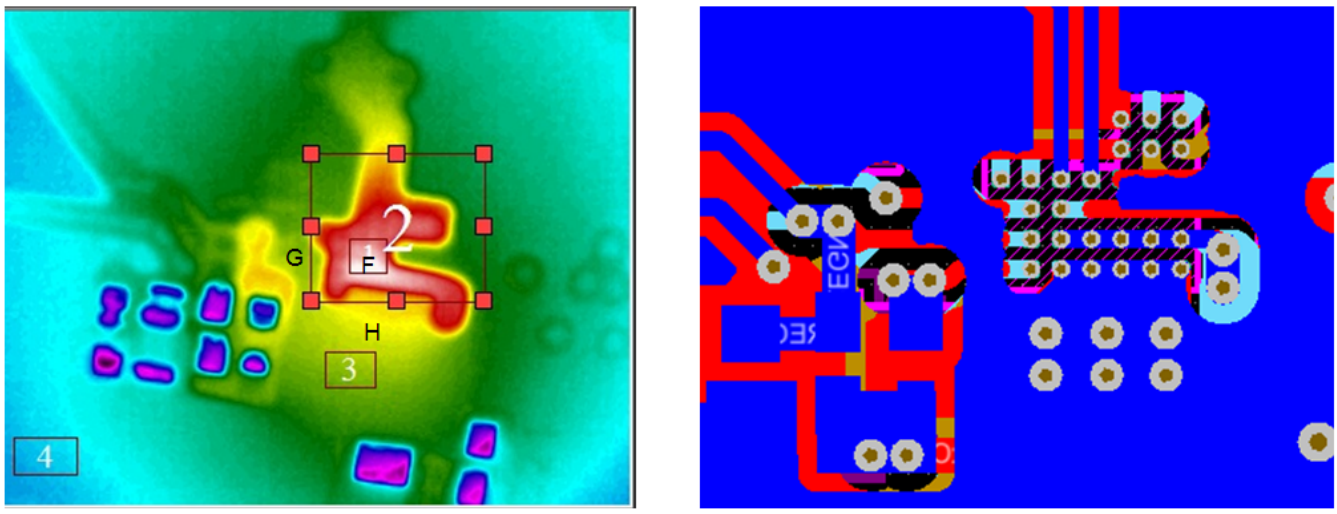


**Figure 6. Bottom Layer Layout and Thermal Image of Design #2**

## 4 Other Considerations

This design uses 1-oz copper. The results of this report show that thicker copper serves as a better heat sink and further improves thermal performance. However, using thicker copper is usually constrained by WCSP ball and pad size, and pitch. TI recommends checking with the PCB manufacturer before increasing the copper thickness.

Dielectric layer thickness is also intentionally reduced in this design. Our study shows thicker dielectric layer makes heat dissipation worse.

Table 1 shows an example of layer stack. Top and bottom layers are used for critical high-current traces. The second layer is a GND plane. The third layer is for other signals.

**Table 1. Example Layer Stack Structure**

| Layer Name | Type | Material | Thickness (mil) | Dielectric Material | Dielectric Constant |
|---|---|---|---|---|---|
| Top overlay | Overlay | | | | |
| Top solder | Solder mask/coverlay | Surface material | 0.4 | Solder resist | 3.5 |
| Top layer | Signal | Copper | 1.4 | | |
| Dielectric1 | Dielectric | Core | 6.6 | FR-4 High TG | 4.2 |
| Signal layer 1 | Signal | Copper | 1.4 | | |
| Dielectric2 | Dielectric | Prepreg | 6.6 | FR-4 High TG | 4.2 |
| Signal layer 2 | Signal | Copper | 1.4 | | |
| Dielectric3 | Dielectric | Core | 6.6 | FR-4 High TG | 4.2 |
| Bottom layer | Signal | Copper | 1.4 | | |
| Bottom solder | Solder mask/coverlay | Surface material | 0.4 | Solder resist | 3.5 |
| Bottom overlay | Overlay | | | | |

Stitching vias are often overlooked but important. In a charger, high current traces may run on two layers to reduce the trace resistance. This is the perfect place to apply stitching vias. It not only helps to reduce connection resistance electrically, but also helps with thermal dissipation. From our experiment, it also significantly reduces electromagnetic interference (EMI). Figure 7 shows an example of stitching vias on PMID and GND copper pours.

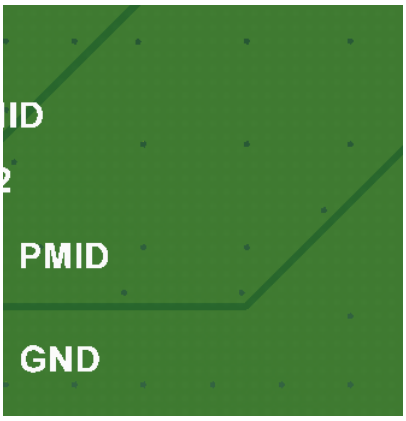


**Figure 7. Stitching Vias on PMID and GND Copper Pours Example**

Using proper soldering techniques when soldering the WCSP IC onto the PCB ensures good electrical and thermal contact between the IC and PCB. A guide box (white square box in Figure 8) is usual helpful for manual soldering.

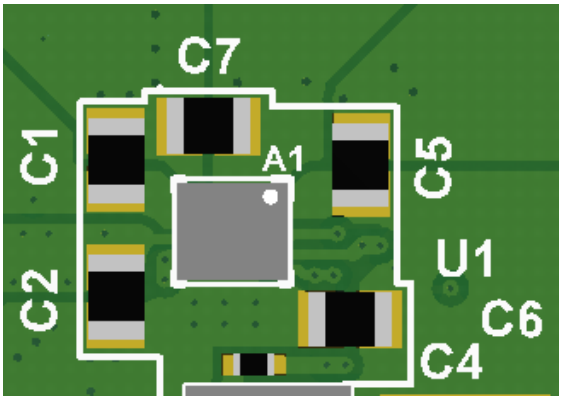


**Figure 8. Die-Size Guide Box With Pin 1 Position Example**

## 5 Summary

This application note studied and experimented with several versions of PCB layout for a high-current battery charger. The demonstrated techniques can help reduce power loss and facilitate thermal dissipation. With an optimized PCB layout, temperature increase can be reduced by 1°C to 3°C, depending on the test environment. If used together with system-level optimization (such as heat sink, heat block, and better air flow, and so forth), the results can be even better.

## 6 References

1. Sreenivasan Koduri et al. Proceedings of the 17th International Symposium on Power Semiconductor Devices and IC's (2005), Santa Barbara, CA.
2. Frank Mortan and Lance Wright, *Quad Flatpack No-Lead Logic Packages* (SCBA017)
3. *bq25898, bq25898D I²C Controlled Single Cell 4-A Fast Charger with MaxCharge™ Technology for High Input Voltage and Adjustable Voltage USB On-the-Go Boost Mode* (SLUSCI7)
4. *bq2426x 3-A, 30-V, Host-Controlled Single-Input, Single-Cell Switched-Mode Li-Ion Battery Charger With Power-Path Management and USB-OTG Support* (SLUSBU4)

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