Using the bq3285/7E in a Green or Portable Environment

Introduction

The bq3285/7E Real-Time Clock is a PC/AT-compatible real-time clock that incorporates three enhanced features to facilitate power management in Green desktop or portable computers:

- 32kHz output
- 128 extra bytes of CMOS nonvolatile SRAM
- Alarm interrupt active in battery-backup mode

The 32kHz output provides a clock signal for power management timers and DRAM refresh control in power-sensitive systems. The output must be enabled with software and appears on the SQW pin.

Most RTCs and chip sets on the market have 114 bytes of general-purpose CMOS RAM. The bq3285/7E adds 128 additional bytes of memory to give the designer and user greater flexibility in defining system configuration settings. The added CMOS RAM is paged to by asserting the EXTRAM pin on the bq3285/7E. It can be used to store power management time-out settings, plug-and-play configuration data, or additional chip set parameters.

The bq3285/7E allows the alarm interrupt from the real-time clock to be active when no power is applied to the part. This enables a properly designed system to be programmed to "wake-up" from a power-off state and perform a function, minimizing the system on time.

32.768kHz Output

The bq3285/7E can be configured to generate a buffered 32.768kHz output on the SQW pin. This signal can be used as a timebase for system timers in a power management environment and as a clock reference for DRAM refresh.

In a Green or portable system, a number of timers are needed to track system and peripheral activity in order to enter different power states and turn off peripherals like hard drives and monitors. For example, a power-managed system may require countdown power state timers to transition the computer from full operation to doze, standby, and suspend states. Peripheral timers may be needed to count how long each peripheral has been inactive. Some chip sets allow the DRAM refresh rate to be slowed to rates based on the 32kHz timer when in suspended states. The power management controller (PMC) on the core logic takes the timer inputs and minimizes system power consumption by generating the appropriate control signals to the rest of the system.

Enabling the 32.768kHz Output

The 32.768kHz output is only available when V_{CC} to the RTC is valid (5V ± 10%). The following settings in the control registers A, B, and C enable the 32.768kHz output onto the SQW pin.

1. Set the Register A OS2–OS0 bits as shown:

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0
-	0	1	1	-	-	-	-

2. Set the Register B SQWE bit as shown:

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	HF	DSE	RS0
-	-	-	-	1	-	-	-

3. Set the Register C 32KE bit as shown:

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	32KE	0	0
-	-	-	-	-	1	-	-

The above settings do not affect the periodic interrupt rate or other time-keeping functions.

Disabling the 32.768kHz Output

The 32.768kHz output is disabled under the following conditions.

1. Clearing either of the SQWE/32KE bits or the OS1/OS0 bits in the above registers.
2. Asserting the $\overline{RST}$ pin low.
3. Putting the device in battery-backup mode ($V_{CC} < V_{BC}$).

Extra CMOS NVSRAM

Because bit 7 at I/O port address 70H in a PC/AT environment is the NMI, additional I/O ports are needed to access the extra 128 bytes of CMOS RAM. The following table shows the I/O ports used by the PC/AT BIOS to access CMOS RAM. Note the CMOS RAM includes the RTC information in the uppermost 14 locations.

I/O Address	Read/ Write	Description
070H	W	CMOS RAM address register port, where: Bit 7 = 1; NMI disabled = 0; NMI enabled Bits 6–0 = Register and CMOS RAM address
071H	R/W	CMOS RAM data register port
074H	W	Extended CMOS RAM address register port, least-significant byte
075H	W	Extended CMOS RAM address register port, most-significant byte
076H	R/W	Extended CMOS RAM data register port

The two CMOS RAM data areas are shown below.

Data Area	I/O Locations	Size (bytes)	Description
Default CMOS Data Area	070H and 071H	Default: 64 Maximum: 128	All BIOS variations use this area to store RTC, POST, and system configuration data.
Extended CMOS RAM Data Area	074H, 075H, and 076H	Default: 2K Maximum: 64K	The PS/2 uses this area to store POS data. The Intel SL uses 074H and 076H to provide "extended" 128 CMOS RAM bytes for APM data.

The EXTRAM pin controls access to the extra 128 bytes of memory on the bq3285/7E. The EXTRAM signal can be generated in two ways:

1. Hook up SA3, SA2, or SA1 from the ISA address bus to the EXTRAM pin. The address/data ports through which the "extra" 128 bytes are accessed depend on which address line is used, as shown in the following table.

Address Line	I/O Ports	Read/ Write	Description
SA3	078H	W	Extra CMOS RAM address register port, where: Bit 7 = Reserved Bits 6–0 = Extra CMOS RAM address
SA3	079H	R/W	Extra CMOS RAM data register port
SA2	074H	W	Same as 078H
SA2	075H	R/W	Same as 079H
SA1	072H	W	Same as 078H
SA1	073H	R/W	Same as 079H

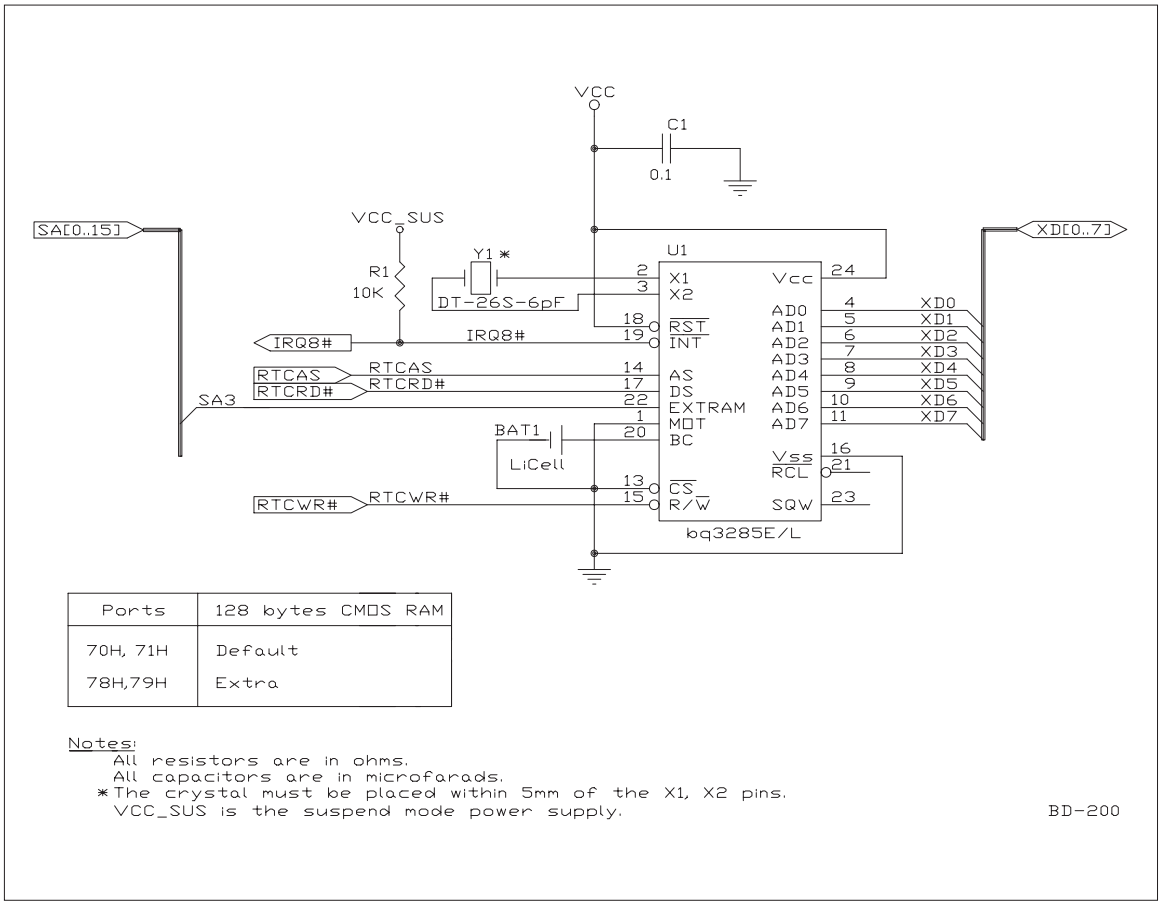
Any one of the above $\overline{I/O}$ port pairs that asserts RTC control signal AS, DS, or $\overline{WR}$ should be selected.

2. Hook up an unused general-purpose I/O port pin to EXTRAM pin. When this pin is asserted high on a write to the assigned I/O port, successive accesses to port 070H and 071H are directed to the extra 128-byte RAM bank.

Refer to Figure 1 for a diagram of a complete PC/AT interface.

Alarm Interrupt

The alarm interrupt on the bq3285/7E functions with or without V_{CC} power. It can be used in a power-managed system to wake the system up from suspend mode or turn the system or parts of the system on from the power-off mode. In suspend mode, most of the computer is shut down except for the power management controller and the DRAM. The PMC needs an interrupt from a push-button resume switch, an incoming modem ring, or the RTC to resume operation. The bq3285/7E RTC can either be left on or turned off during suspend mode depending on the level of functionality required. In 0V suspend mode, the 32kHz output may not be needed because all the DRAM information is stored to disk and refresh is not required. In this case, the bq3285/7E can be powered off during suspend and still be able to supply



Ports	128 bytes CMOS RAM
70H, 71H	Default
78H,79H	Extra

Notes:
All resistors are in ohms.
All capacitors are in microfarads.
*The crystal must be placed within 5mm of the X1, X2 pins.
VCC_SUS is the suspend mode power supply.

BD-200

Figure 1. bq3285/7E PC/AT Design Example

the alarm interrupt to the power management controller. In 3V/5V suspend where the DRAM is kept alive, the bq3285/7E should be in the powered-up mode. This has little impact on power consumption, however, because the bq3285/7E has low standby current when deselected.

The bq3285/7E can be also be used to turn a system on from the power-off mode for periods of short duration. Figure 2 shows how this could be implemented. The $\overline{INT}$ pin alerts the power management controller, which in turn activates a p-FET to turn on the necessary subsystems to perform the required function. After completion of the task, the system shuts down except for the power management controller.

PC/AT Environment

Most advanced power-managed chip sets have a direct input for a 32kHz signal. A common way of generating this signal is to use a CMOS buffered inverter like the MC14069 with a 32.768kHz quartz crystal and R-C components. The bq3285/7E contains its own built-in 32.768kHz quartz crystal for the real-time clock oscillator. To eliminate redundancy and component count, the 32kHz output on the bq3285/7E SQW pin can be used in place of the MC14069, external crystal, and other passive components. The SQW pin has not been used in PC/AT designs in the past, so using it for this function does not impact other aspects of the motherboard design.

Figure 3 shows a real-time clock and timer generation using the MC146818A and the MC14069 in conjunction with Green core logic chips. Figure 4 shows the much simplified bq3285/7E design using the 32kHz output on the SQW pin and the extra NVSRAM enabled. Ports 70H and 71H address the upper 128 bytes of CMOS RAM including the RTC information. Ports 78H and 79H address the extra 128 bytes of CMOS RAM.

From a software standpoint, the PC BIOS must incorporate the appropriate routine to enable the 32kHz output and use the extra NVSRAM. The 32kHz enable routine should be placed as part of the system cold-boot initialization procedure.

Other Considerations

If the height of the bq3285/7E DIP module is an issue in portable designs, the part is also available in a 300-mil SOIC and a 150-mil SSOP (bq3285ES and bq3285ESS). Both variations provide direct connections for an external crystal and battery. The devices are also available with 3V V_{CC} operation (bq3285LS and bq3285LSS) for use in 3V systems.

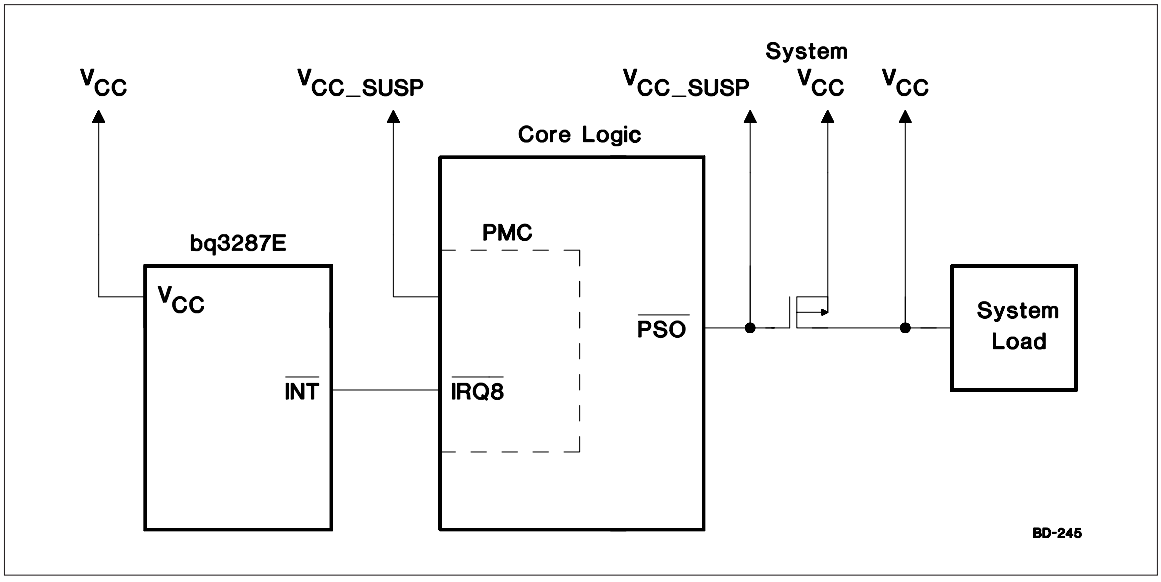


Figure 2. System Wake-up Alarm

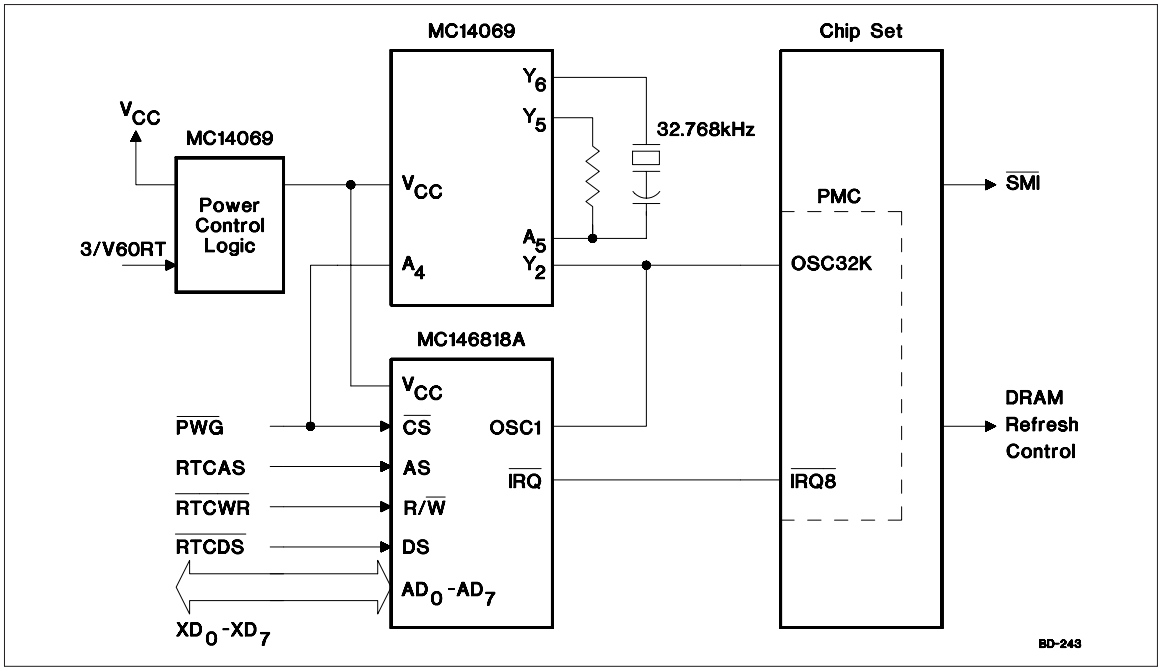


Figure 3. MC14069 Implementation

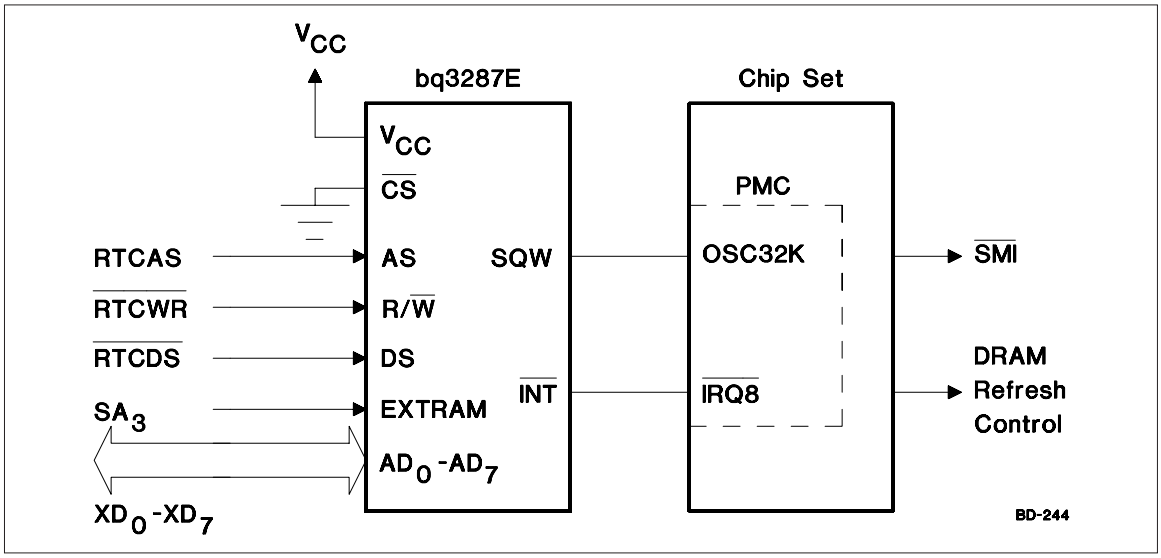


Figure 4. bq3285/7E Implementation

Notes

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.