Application Report
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bq77905 Shutdown for Current Reduction

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BMS: Battery Monitoring & Protection

ABSTRACT

The *bq77905 3-5S Low-Power Protector* for lithium-ion batteries features a low 6-µA typical supply current to extend battery life. Power tools or other applications where the battery is in storage or unused for long periods may want to prevent battery discharge during idle times. The schematic examples and test results in this document help the battery electronics designer when implementing a circuit topology to reduce battery current.

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Trademarks

1 Introduction

The bq77905 3-5S low-power protector is an easy-to-use component for lithium-ion battery circuits. With the common simple schematic shown in Figure 1, the part is continuously powered. The current load on the battery is the low IC operating current, the load current of the R_{GS} resistors, and the open wire test currents. The low operating current of the bq77905 can give a long battery life, but some systems which are infrequently used may want to reduce the current.

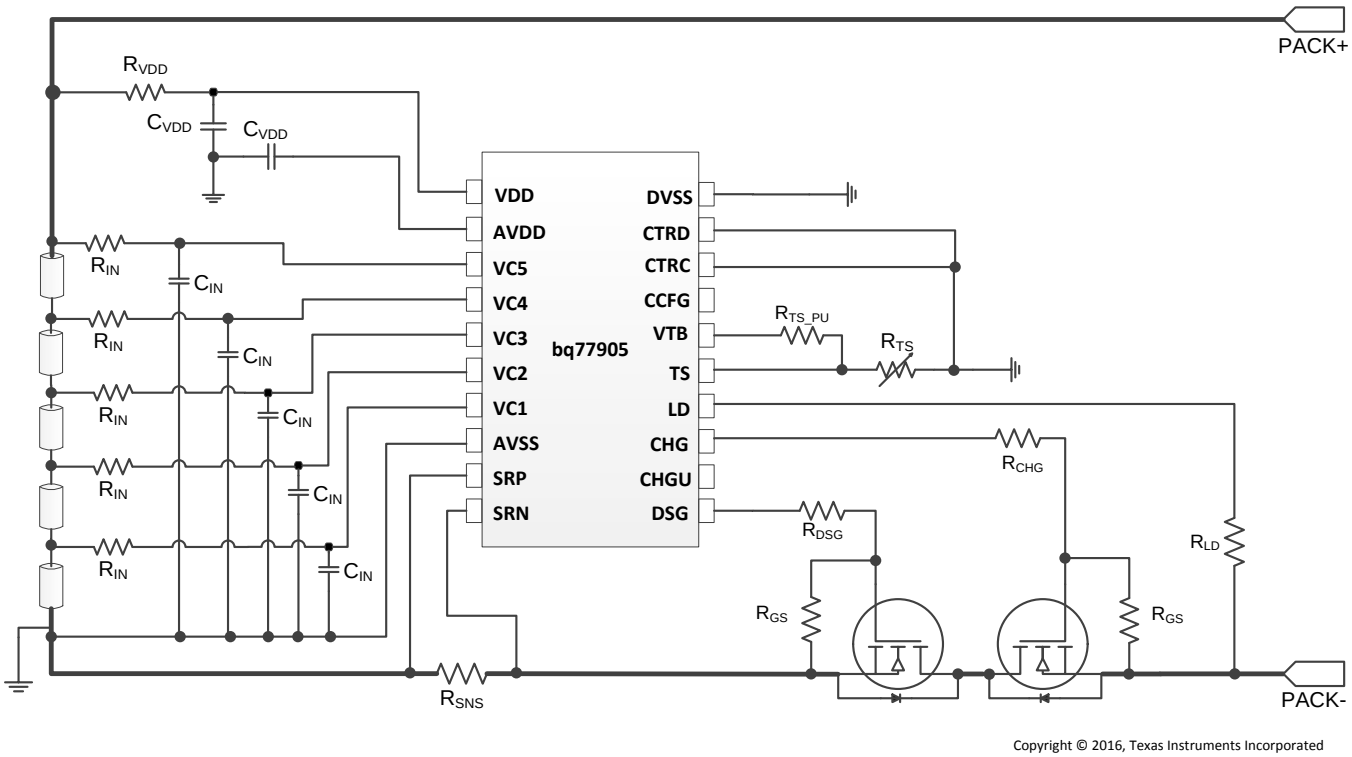

Figure 1. Common Circuit Implementation

2 Single Device

A typical attempt to reduce current is to disconnect power to the IC VDD pin while leaving the remainder of the IC connected similar to Figure 2. This approach is not effective with the bq77905 since there are internal leakage paths between VC5 and VDD. Disconnecting VDD with VC5 connected biases the part in a way which increases total current and provides an incorrect voltage for the top cell due to the voltage drop on the VC5 resistor.

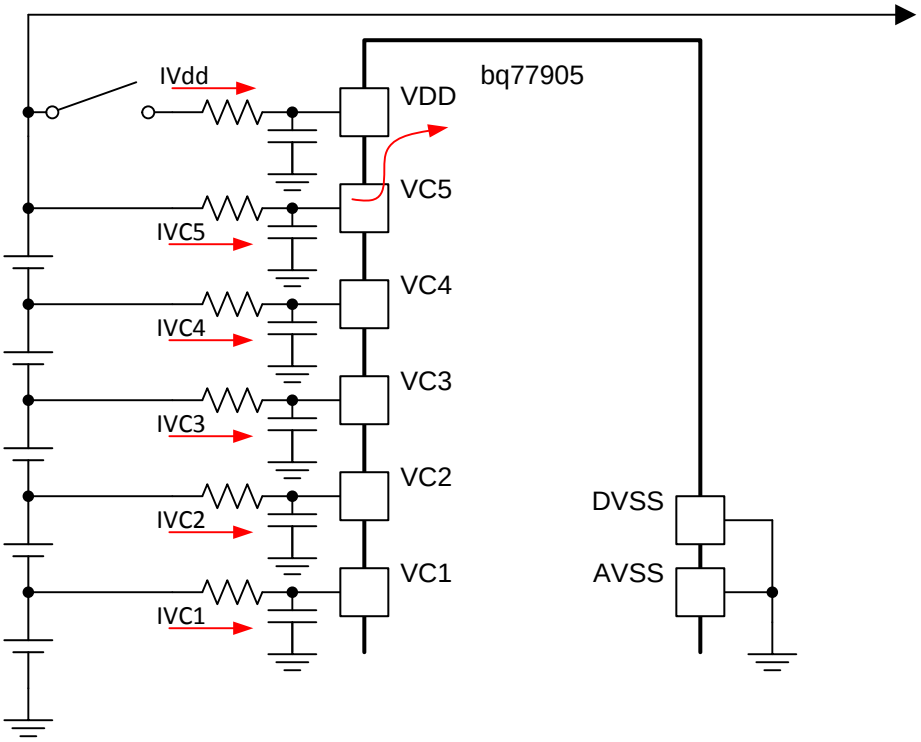

Figure 2. Ineffective VDD Switch

Table 1. Input Current Comparison

Input	Input Current, µA			
	Switch VDD Only		Switch Cell 5	
	ON	OFF	ON	OFF
VDD	6.03	0.000	6.03	0.000
VC5	0.109	37.6	0.109	0.000
VC4	0.114	0.114	0.115	0.000
VC3	0.112	0.112	0.113	0.000
VC2	0.101	0.101	0.102	0.000
VC1	0.108	0.108	0.109	0.000

Moving the switch from the VDD to the common net from cell 5 breaks both the VDD and VC5 inputs to the part. This eliminates the current into the part. When the part shuts down, the open wire test current to the lower input pins is turned off. Figure 3 shows the switch in the cell 5 connection. Table 1 shows a comparison of switching only VDD and switching the common cell 5 connection.

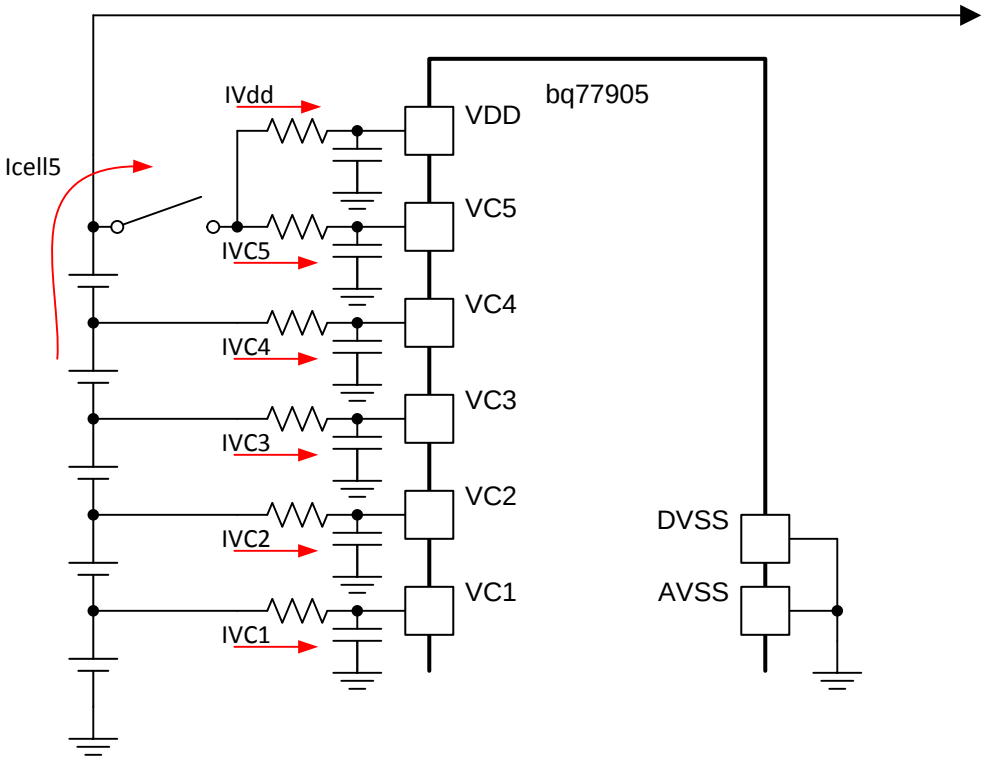

Figure 3. Shutdown Circuit

A switch can be implemented and controlled as desired in the system. One method is to control a P-channel FET with either an N-channel FET or NPN. Figure 4 shows an example circuit with an ENABLE signal that could be connected to PACK+ to enable the pack. Table 2 shows the value used for the example test. With a low duty cycle the ON current is not a significant concern, but values could be optimized and transient protection added for a system design.

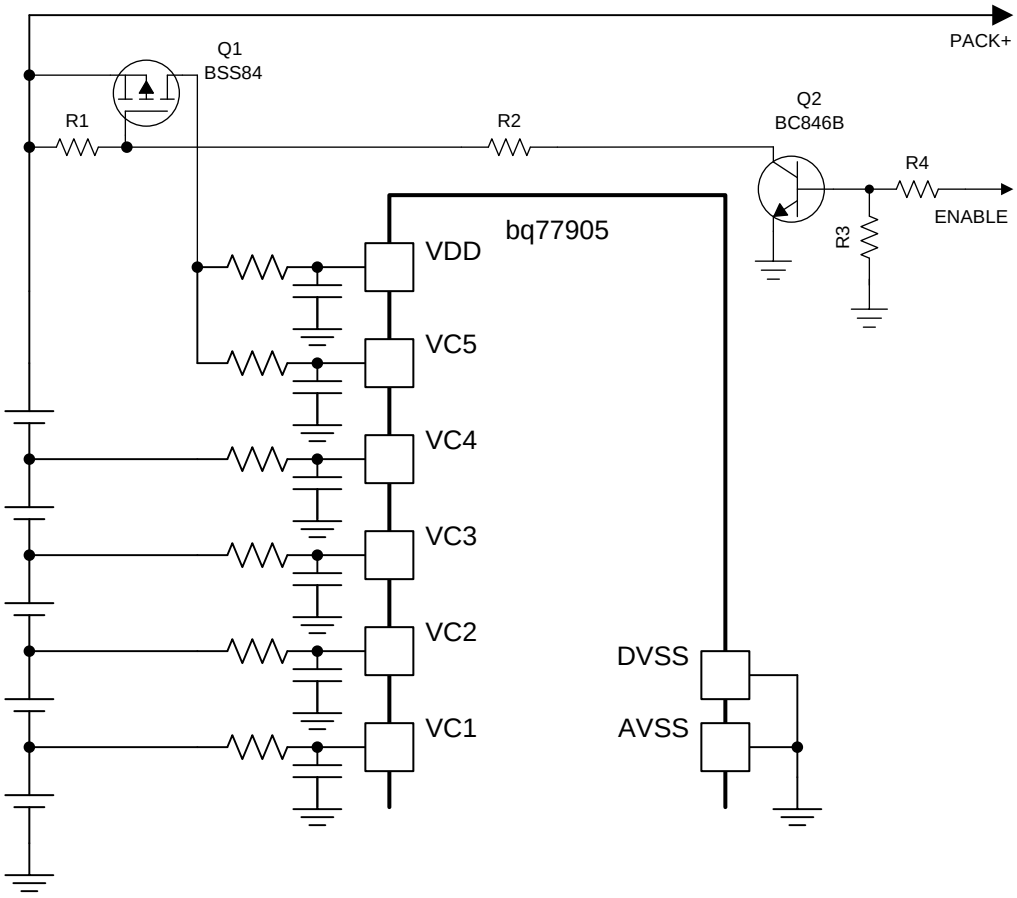

Figure 4. Single Device Shutdown Example

Table 2. Single Device Shutdown Example Component Values

Reference Designator	Value (kΩ)
R1	510
R2	510
R3	5.1
R4	30

Figure 5 shows example waveforms when ENABLE is disconnected from PACK+. The 10-MΩ scope probes load the circuit and will decrease the turn off time. The gate voltage falls as VDD drops until the gate is turned off by undervoltage or the shutdown threshold. With the drop in gate voltage, the part should not be turned off when the pack is loaded.

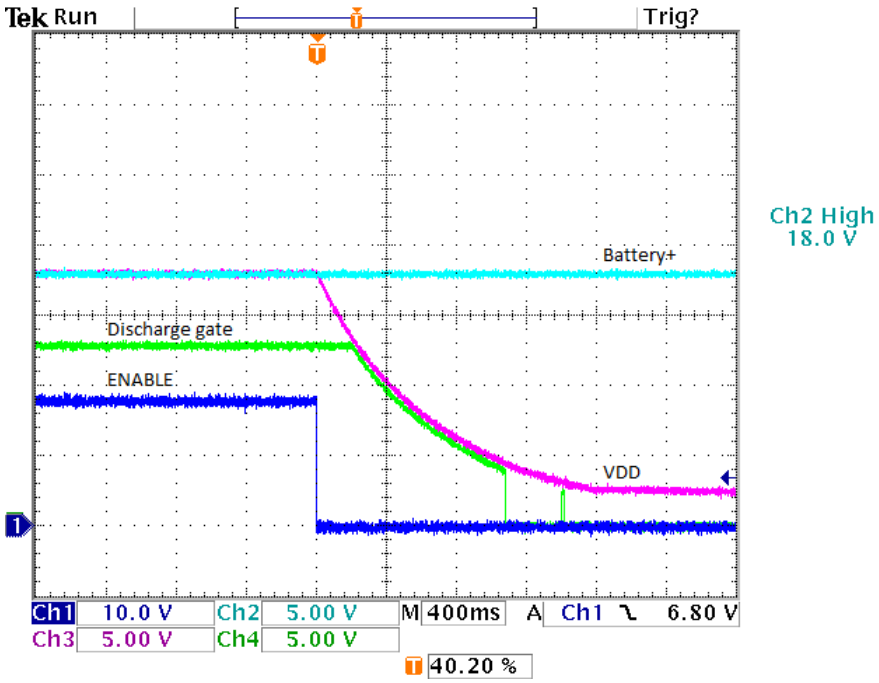

Figure 5. Single Device Turn Off

3 Stacked Devices

When devices are stacked for higher cell count packs the top cell for each part needs to be switched, but there is another consideration. The stacking interface includes a clamp to the VDD of the next lower part. This clamp can power the lower part from the FET outputs of the upper part since, even when off, the DSG and CHGU pins cannot fall substantially below the VSS voltage of the upper device. Figure 6 shows a switching concept and the internal clamps that prevent the power down of the lower part.

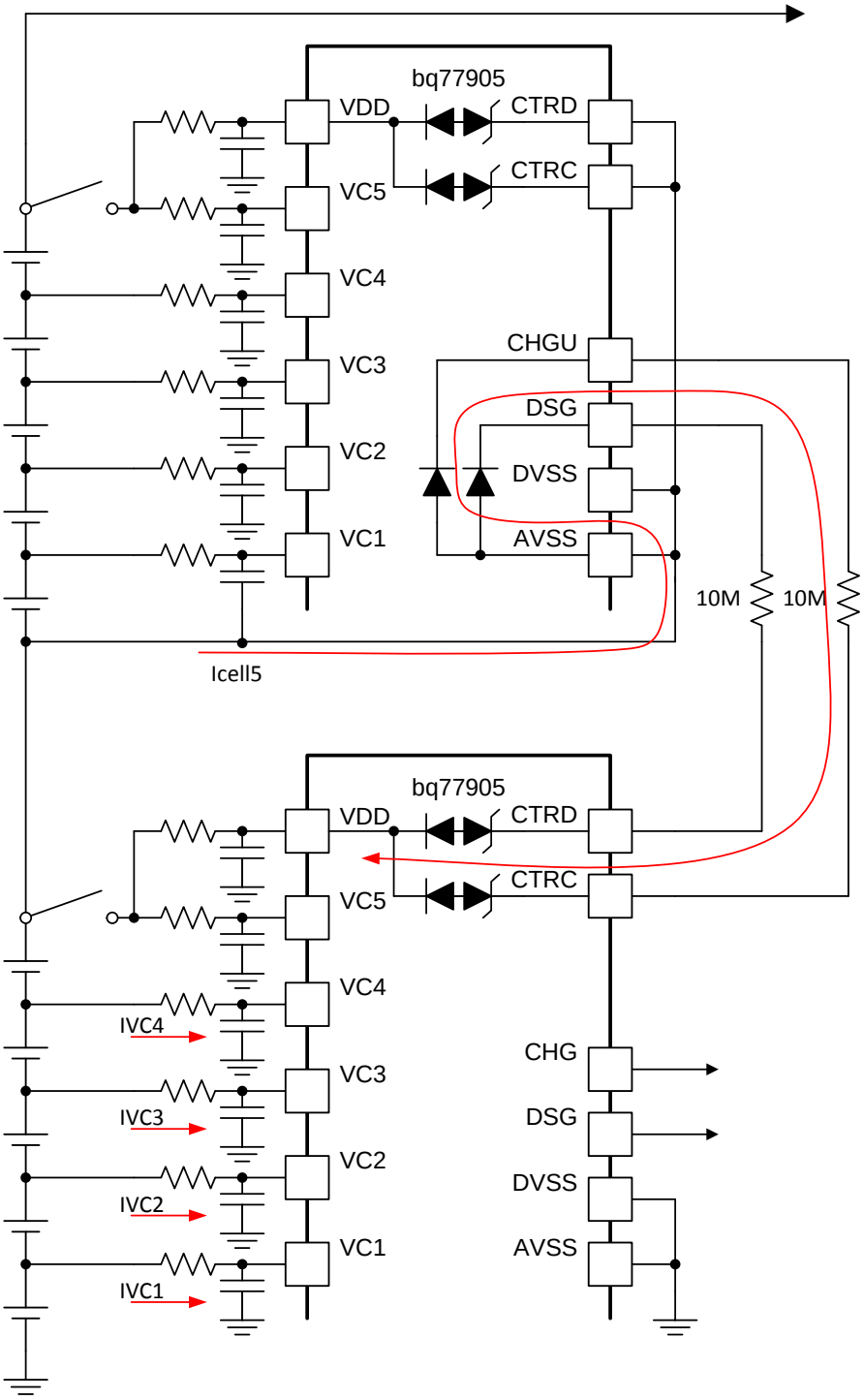

Figure 6. Ineffective Switch With Stacked Devices Due To Leakage Path

Figure 7 shows an example of switching only the upper cells to the devices. The scope probes load the circuit but the variation of VDD1 can be observed as the lower part oscillates between the V_{SHUT} and V_{POR} and levels.

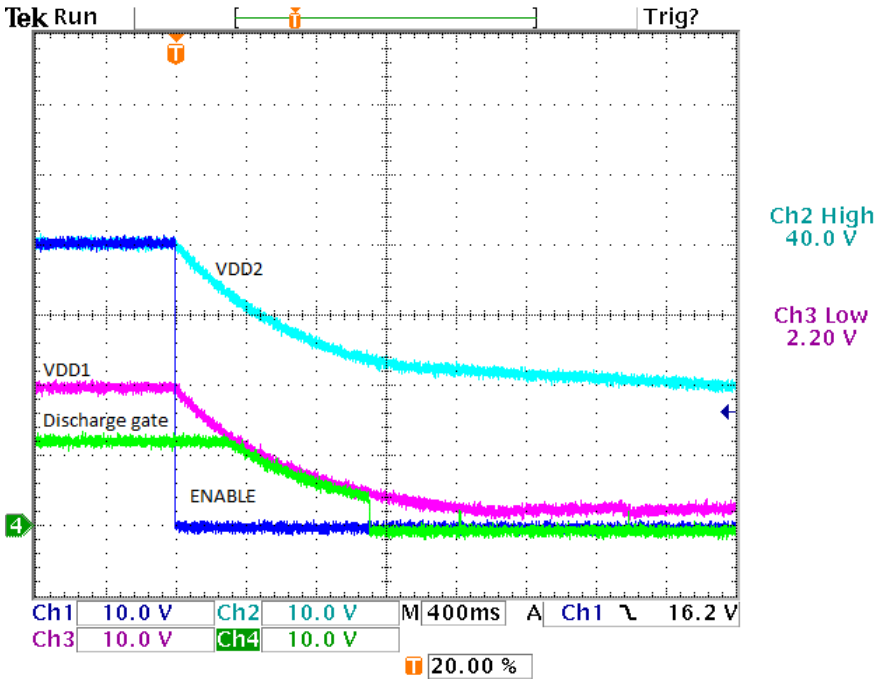

Figure 7. Stacked Circuit Shutdown With CTRC and CTRD Leakage

To avoid the leakage from the upper FET outputs to the lower device power through the substrate diodes, the upper FET control signals must be allowed to fall below the VSS level. This function is built into the CHG pin, but must be externally implemented with the DSG pin. To prevent the CTRD and CTRC pins of the lower device from falling to VSS, and re-enabling the FETs in the case of a fault with the upper device during operation, diodes are used from the VDD pin of the lower device.

Figure 8 shows a circuit proposal to allow shutdown of stacked devices avoiding the leakage into CTRC and CTRD. A specification concern may exist for some user's since the maximum $V_{CTR(DIS)}$ for the stacking input is 0.7 V while the maximum $V_{(FETOFF)}$ is 0.5 V. This apparently provides little margin, however CHG is not held at the maximum and is allowed to fall below VSS. The designer should satisfy themselves the circuit will work in their application before implementing this design.

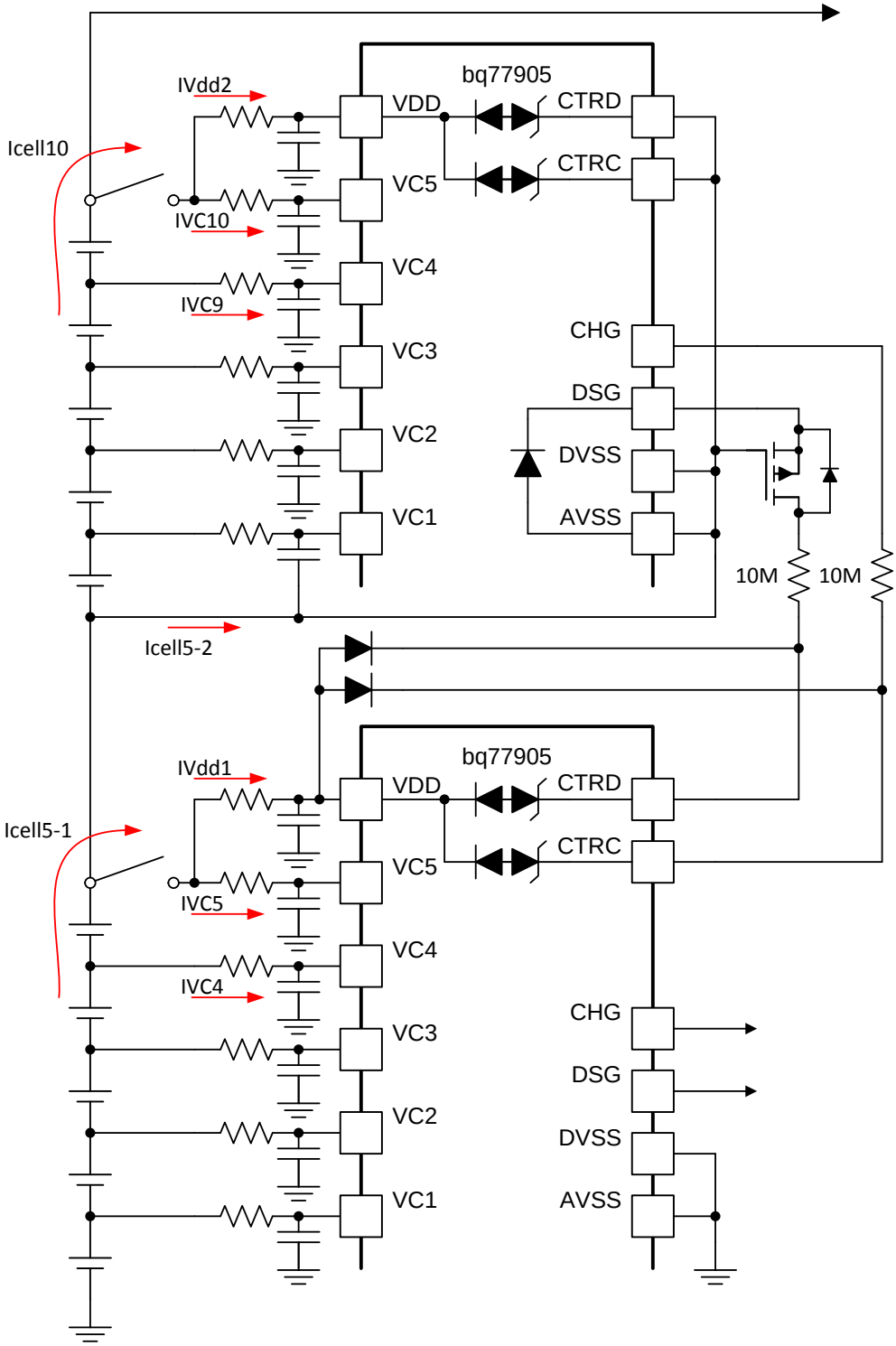

Figure 8. Stacked Device Shutdown Circuit

Figure 9 shows a test circuit which implements switches for both upper and lower devices and the proposal to prevent pullup through the CTRC and CTRD pins. The pack is enabled when ENABLE is connected to PACK+. R5 and R6 provide a load on the entire battery while R1 and R2 load only the lower cells. A compensating load could be added from Q3 drain to the upper VSS, but was not implemented in this circuit. Other switch configurations could be implemented, use appropriate transient protection for a system design.

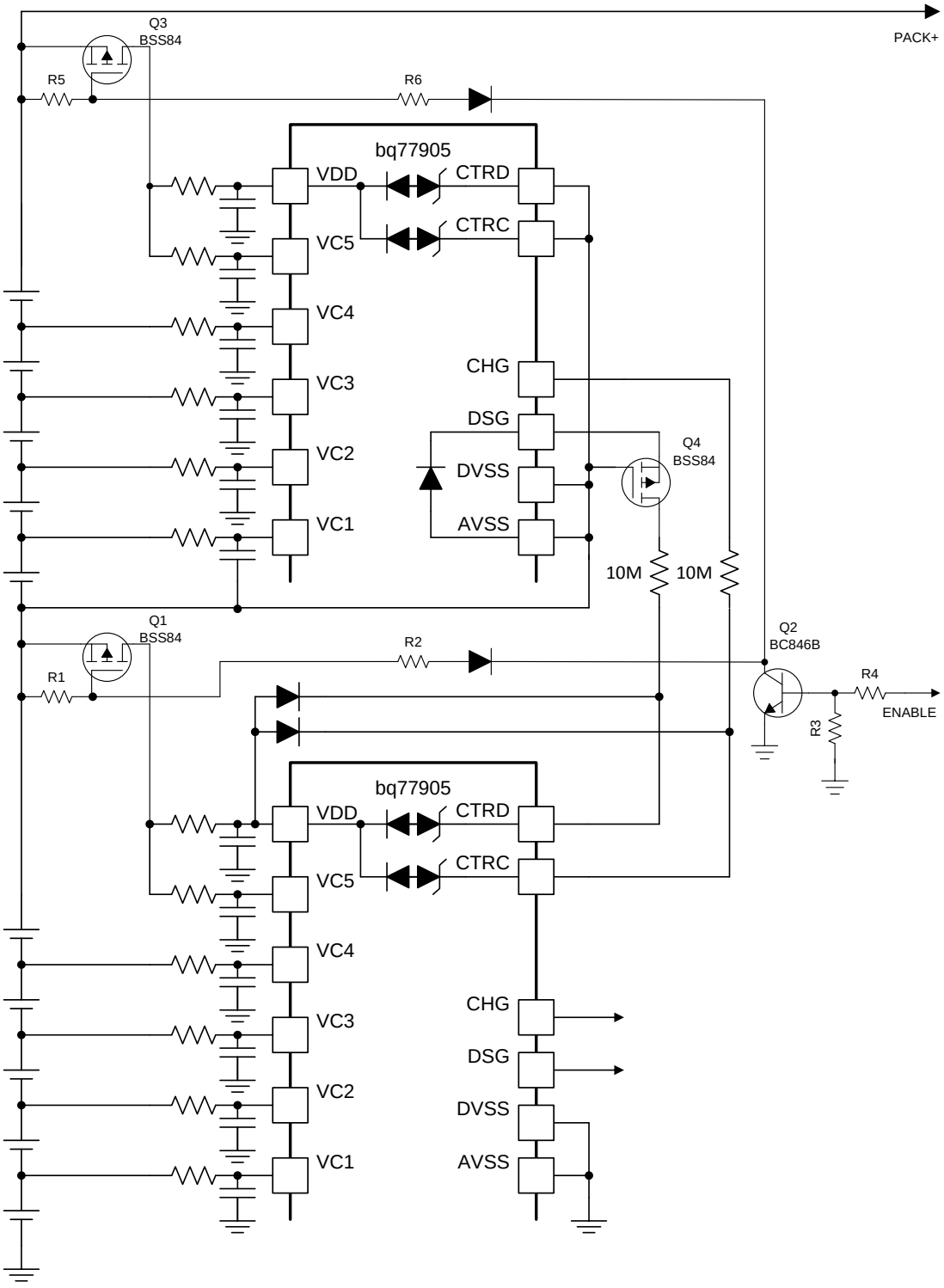

Figure 9. Stacked Switch Example Test Circuit

The circuit was tested with the component values shown in Table 3. With the circuit enabled, the circuit operates as expected. Figure 10 shows the operation of the FET controls in response to an overtemperature on the top device. When the upper device CHG and DSG are off, CTRC and CTRD of the lower device are held near the VDD level and the lower DSG and CHG turn off.

Table 3. Stacked Switch Circuit Component Values

Reference Designator	Value (Ω)
R1	510 k
R2	510 k
R3	5.1 k
R4	62 k
R5	510 k
R6	1.5 M
(diodes)	1N4148 type

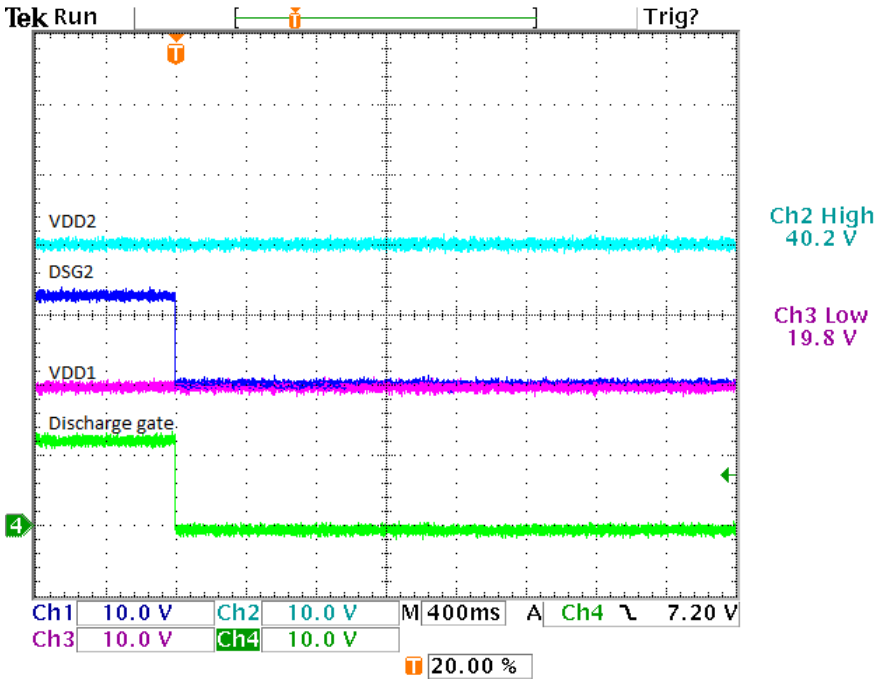

Figure 10. Overtemperature Fault on Top Device

Figure 11 shows the response when ENABLE is disconnected from PACK+. Like the single device, the discharge gate voltage drops as VDD1 falls. The upper device VDD falls to the cell 5 level. VDD1, the lower device VDD falls toward VSS. Without the leakage into CTRC and CTRD, VDD1 continues to fall slowly after the device enters shutdown. The load on the bottom 5 cells which cause voltage variation of VDD1 shown in Figure 7 is not present with this circuit.

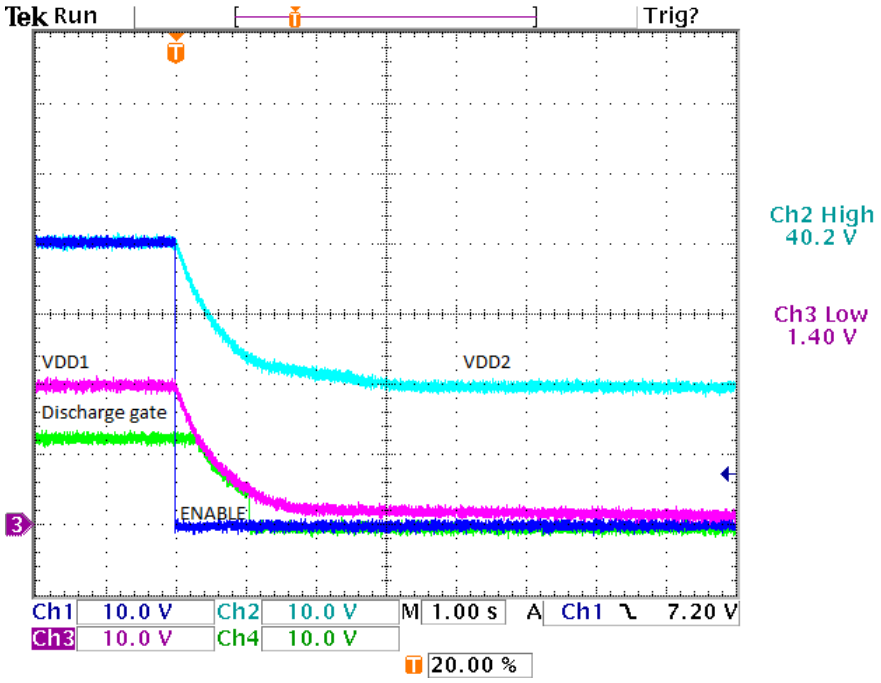

Figure 11. Stacked Devices Turn Off Using Test Circuit

4 References

For additional information, refer to the following documents available at www.ti.com.

- Texas Instruments, *bq77905, bq77904 3-5S Ultra Low-Power Voltage, Current, Temperature, and Open Wire Stackable Lithium-ion Battery Protector Data Sheet*
- Texas Instruments, *bq77905 3-5S Low-Power Protector Evaluation Module User's Guide*
- Texas Instruments, (*bq77905 20S Cell Stacking Configuration Application Report*)

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