

2.4-GHz RF Front End, 14-dBm output power

FEATURES

- Seamless Interface to 2.4-GHz Low Power RF Devices from Texas Instruments
- Up to +14-dBm (25mW) Output Power
- 6-dB Typical Improved Sensitivity on CC24xx and CC2500, CC2510, and CC2511
- Few External Components
 - Integrated Switches
 - Integrated Matching Network
 - Integrated Balun
 - Integrated Inductors
 - Integrated PA
 - Integrated LNA
- Digital Control of LNA Gain by HGM Pin
- 100-nA in Power Down (EN = PAEN = 0)
- Low Transmit Current Consumption
 - 22-mA at 3-V for +12-dBm, PAE = 23%
- Low Receive Current Consumption
 - 3.4-mA for High Gain Mode
 - 1.8-mA for Low Gain Mode
- 4.6-dB LNA Noise Figure, including T/R Switch and external antenna match
- RoHS Compliant 4x4-mm QFN-16 Package
- 2.0-V to 3.6-V Operation

APPLICATIONS

- All 2.4-GHz ISM Band Systems
- Wireless Sensor Networks
- Wireless Industrial Systems
- IEEE 802.15.4 and ZigBee Systems
- Wireless Consumer Systems
- Wireless Audio Systems

DESCRIPTION

CC2590 is a cost-effective and high performance RF Front End for low-power and low-voltage 2.4-GHz wireless applications.

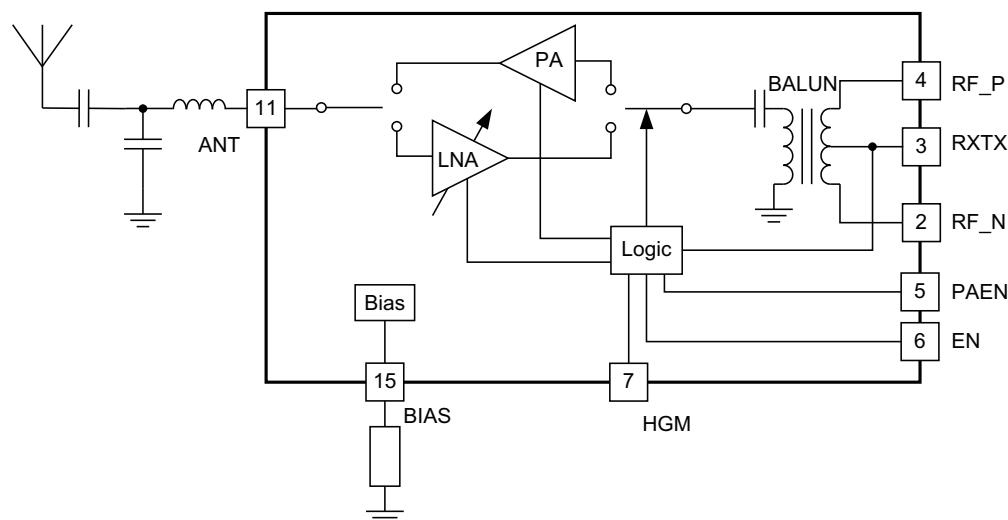
CC2590 is a range extender for all existing and future 2.4-GHz low-power RF transceivers, transmitters and System-on-Chip products from Texas Instruments.

CC2590 increases the link budget by providing a power amplifier for increased output power, and an LNA with low noise figure for improved receiver sensitivity.

CC2590 provides a small size, high output power RF design with its 4x4-mm QFN-16 package.

CC2590 contains PA, LNA, switches, RF-matching, and balun for simple design of high performance wireless applications.

CC2590 BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

Under no circumstances must the absolute maximum ratings be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

| PARAMETER | | VALUE | UNIT |
|------------------------------|--|----------------------------------|------|
| Supply voltage | All supply pins must have the same voltage | –0.3 to 3.6 | V |
| Voltage on any digital pin | | –0.3 to $V_{DD} + 0.3$, max 3.6 | V |
| Input RF level | | +10 | dBm |
| Storage temperature range | | –50 to 150 | °C |
| Reflow soldering temperature | According to IPC/JEDEC J-STD-020 | 260 | °C |
| ESD | Human Body Model, all pins except pin 10 | 2000 | V |
| | Human Body Model, pin 10 | 1900 | V |
| | Charged Device Model | 1000 | V |

RECOMMENDED OPERATING CONDITIONS

The operating conditions for CC2590 are listed below.

| PARAMETER | | MIN | MAX | UNIT |
|---------------------------|--|------|--------|------|
| Ambient temperature range | | –40 | 85 | °C |
| Operating supply voltage | | 2.0 | 3.6 | V |
| Operating frequency range | | 2400 | 2483.5 | MHz |

ELECTRICAL CHARACTERISTICS

$T_C = 25^\circ\text{C}$, $V_{DD} = 3.0\text{V}$, $f_{RF} = 2440\text{MHz}$ (unless otherwise noted). Measured on CC2590EM reference design including external matching components.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----|------|----------|---------------|
| Receive current, High Gain Mode | HGM = 1 | | 3.4 | 4.0 | mA |
| Receive current, Low Gain Mode | HGM = 0 | | 1.8 | 2.0 | mA |
| Transmit current | $P_{IN} = 0.5\text{ dBm}$, $P_{OUT} = 12.2\text{ dBm}$ | | 22.1 | | mA |
| | $P_{IN} = -3.5\text{ dBm}$, $P_{OUT} = 10.0\text{ dBm}$ | | 16.8 | | mA |
| Transmit current | No input signal | | 8.0 | 10.0 | mA |
| Power down current | EN = PAEN = 0 | | 0.1 | 0.3 | μA |
| High input level (control pins) | EN, PAEN, HGM, RXTX | 1.3 | | V_{DD} | V |
| Low input level (control pins) | EN, PAEN, HGM, RXTX | | | 0.3 | V |
| Power down - Receive mode switching time | | | 1.4 | | μs |
| Power down - Transmit mode switching time | | | 0.8 | | μs |
| RF Receive | | | | | |
| Gain, High Gain Mode | HGM = 1 | | 11.4 | | dB |
| Gain, Low Gain Mode | HGM = 0 | | 0 | | dB |
| Gain variation, 2400 – 2483.5 MHz, High Gain Mode | HGM = 1 | | 1.2 | | dB |
| Gain variation, 2.0V – 3.6V, High Gain Mode | HGM = 1 | | 1.7 | | dB |
| Noise figure, High Gain Mode | HGM = 1, including internal T/R switch and external antenna match | | 4.6 | | dB |
| Input 1 dB compression, High Gain Mode | HGM = 1 | | –21 | | dBm |

ELECTRICAL CHARACTERISTICS (continued)

$T_C = 25^\circ\text{C}$, $V_{DD} = 3.0\text{V}$, $f_{RF} = 2440\text{MHz}$ (unless otherwise noted). Measured on CC2590EM reference design including external matching components.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|------|-----|------|
| Input IP3, High Gain Mode | HGM = 1 | | -9 | | dBm |
| Input reflection coefficient, S11 | HGM = 1, measured at antenna port | | -19 | | dB |
| RF Transmit | | | | | |
| Gain | | | 14.1 | | dB |
| Output power, P_{OUT} | $P_{IN} = 4.5\text{ dBm}$ | | 13.8 | | dBm |
| | $P_{IN} = 0.5\text{ dBm}$ | | 12.2 | | dBm |
| | $P_{IN} = -3.5\text{ dBm}$ | | 10.0 | | dBm |
| Power Added Efficiency, PAE | $P_{IN} = 0.5\text{ dBm}$ | | 23.5 | | % |
| Output 1 dB compression | | | 10.4 | | dBm |
| Output IP3 | | | 23 | | dBm |
| Output power variation over frequency | 2400 – 2483.5 MHz, $P_{IN} = 0.5\text{ dBm}$ | | 0.3 | | dB |
| Output power variation over power supply | 2.0V – 3.6V, $P_{IN} = 0.5\text{ dBm}$ | | 3.2 | | dB |
| Output power variation over temperature | -40°C – 85°C, $P_{IN} = 0.5\text{ dBm}$ | | 1.1 | | dB |
| 2nd harmonic power | The 2nd harmonic can be reduced to below regulatory limits by using an external LC filter and antenna. See application note AN032 for regulatory requirements. | | -14 | | dBm |
| 3rd harmonic power | The 3rd harmonic can be reduced to below regulatory limits by using an external LC filter and antenna. See application note AN032 for regulatory requirements. | | -28 | | dBm |

DEVICE INFORMATION

The CC2590 pinout and description are shown in Figure 1 and Table 1, respectively.

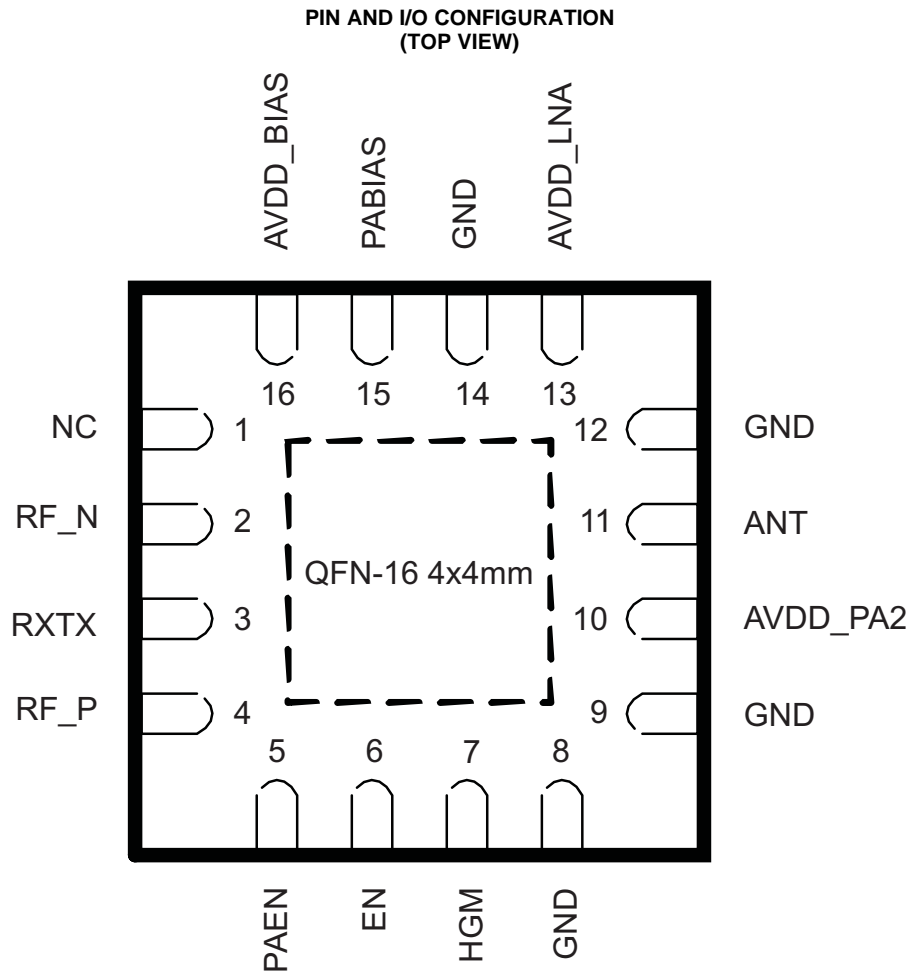


Figure 1.

NOTE:

The exposed die attach pad **must** be connected to a solid ground plane as this is the primary ground connection for the chip. Inductance in vias to the pad should be minimized. It is highly recommended to follow the reference layout. Changes will alter the performance. Also see the PCB landpattern information in this data sheet.

For best performance, minimize the length of the ground vias, by using a 4-layer PCB with ground plane as layer 2 when CC2590 is mounted onto layer 1.

Table 1. PIN FUNCTIONS

| PIN | | TYPE | DESCRIPTION |
|--------------|-----------|----------------|---|
| NO. | NAME | | |
| — | GND | Ground | The exposed die attach pad must be connected to a solid ground plane. See CC2590EM reference design for recommended layout. |
| 1 | NC | | Not Connected |
| 2 | RF_N | RF | RF interface towards CC24xx or CC25xx device. |
| 3 | RXTX | Analog/Control | RXTX switching voltage when connected to CC24xx devices. See Table 3 , Table 4 , and Table 5 for details. |
| 4 | RF_P | RF | RF interface towards CC24xx or CC25xx device |
| 5 | PAEN | Digital Input | Digital control pin. See Table 3 , Table 4 , and Table 5 for details. |
| 6 | EN | Digital Input | Digital control pin. See Table 3 , Table 4 , and Table 5 for details. |
| 7 | HGM | Digital Input | Digital control pin. HGM=1 → Device in High Gain Mode HGM=0 → Device in Low Gain Mode (RX only) |
| 8, 9, 12, 14 | GND | Ground | Secondary ground connections. Should be shorted to the die attach pad on the top PCB layer. |
| 10 | AVDD_PA2 | Power | 2.0-V – 3.6-V Power. PCB trace to this pin serves as inductive load to PA. See CC2590EM reference design for recommended layout. |
| 11 | ANT | RF | Antenna interface. |
| 13 | AVDD_LNA | Power | 2.0-V – 3.6-V Power. PCB trace to this pin serves as inductive load to LNA. See CC2590EM reference design for recommended layout. |
| 15 | BIAS | Analog | Biasing input. Resistor between this node and ground sets bias current to PAs. |
| 16 | AVDD_BIAS | Power | 2.0-V – 3.6-V Power. |

CC2590EM Evaluation Module

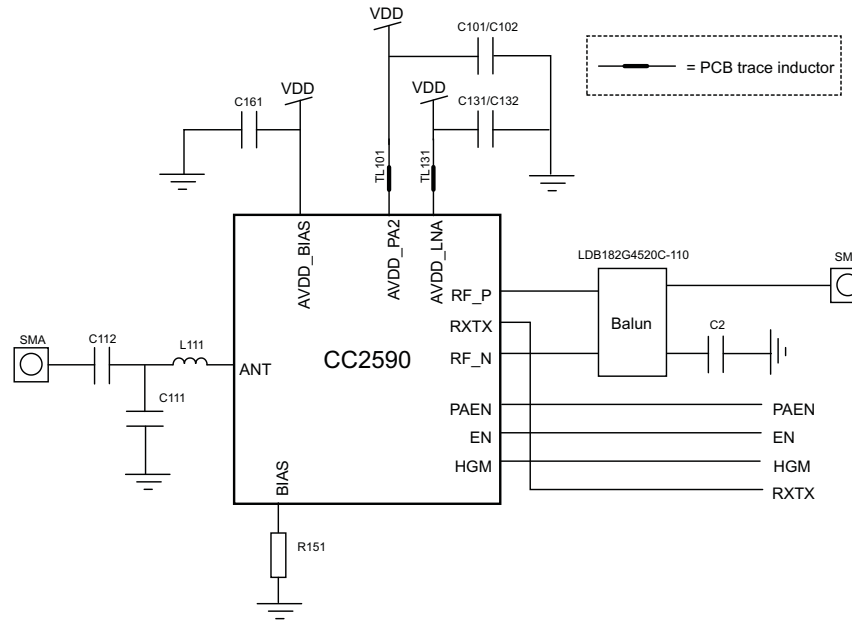


Figure 2. CC2590EM Evaluation Module

Table 2. List of Materials (See CC2590EM Reference Design)

| DEVICE | FUNCTION | VALUE |
|----------------------|---|---|
| L112 | Part of antenna match. | 1.5 nH: LQW15AN1N5B00 from Murata |
| C111 | Part of antenna match. | 0.5 pF, GRM1555C1HR50BZ01 from Murata |
| C112 | DC block. | 47 pF, GRM1555C1H470JZ01 from Murata |
| C161 | Decoupling capacitor. | 1 nF: GRM1555C1H102JA01 from Murata |
| C101/C102 | Decoupling. Will affect PA resonance. See CC2590EM reference design for placement. | 27 pF 1 nF. The smallest cap closest to CC2590. 27 pF: GRM1555C1H270JZ01 from Murata 1 nF: GRM1555C1H102JA01 from Murata |
| C131/C132 | Decoupling. Will affect LNA resonance. See CC2590EM reference design for placement. | 18 pF 1 nF. The smallest cap closest to CC2590. 18 pF: GRM1555C1H180JZ01 from Murata 1 nF: GRM1555C1H102JA01 from Murata |
| C2 | Decoupling of external balun | 1 nF: LWQ15AN1N5B00 from Murata |
| TL101 ⁽¹⁾ | Transmission line. Will affect PA resonance. (simulated inductance: 0.87nH) | See CC2590EM reference design. Transmission line: Length ≈ 40 mil, Width = 8 mil |
| TL131 | Transmission line. Will affect LNA resonance. (simulated inductance: 1.64nH) | See CC2590EM reference design. Transmission line: Length ≈ 100 mil, Width = 8 mil |
| R151 | Bias resistor | 4.3 kΩ: RK73H1ETTP4301F from Koa |

(1) Transmission lines are measured from edge of pad of the CC2590 footprint to edge of pad of DC coupling capacitor. The length of the transmission lines depend on the distance to the ground plane. If another PCB stack up is chosen the length of the transmission lines needs to be adjusted.

PCB description: 4 layer PCB 1.6mm

- Copper 1: 35 μm
- Dielectric 1-2: 0.35 mm (e.g. 2x Prepreg 7628 AT05 47% Resin)
- Copper 2: 18 μm
- Dielectric 2-3: 0.76 mm (4 x 7628M 43% Resin)
- Copper 3: 18 μm
- Dielectric 3-4: 0.35 mm (e.g. 2x Prepreg 7628 AT05 47% Resin)
- Copper 4: 35 μm

DE104iML or equivalent substrate (Resin contents around 45%, which gives Er=4.42 at 2.4GHz, TanD=0.016)

TYPICAL CHARACTERISTICS

LNA GAIN AND NOISE FIGURE
VS
FREQUENCY

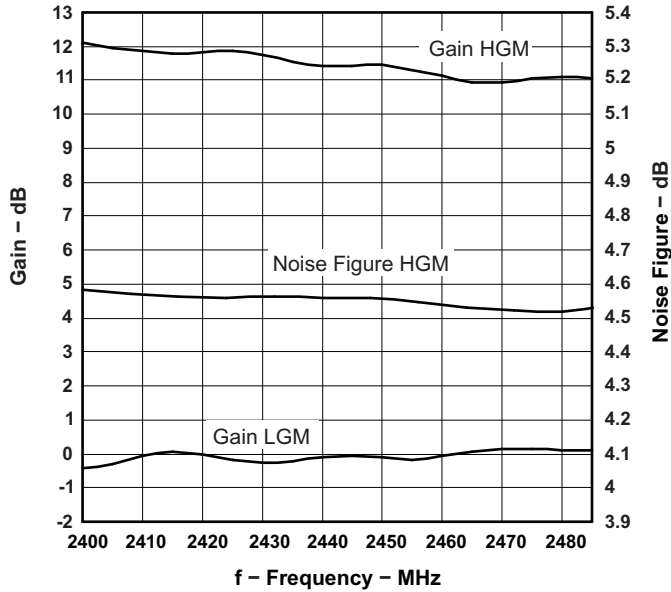


Figure 3.

LNA GAIN
VS
TEMPERATURE

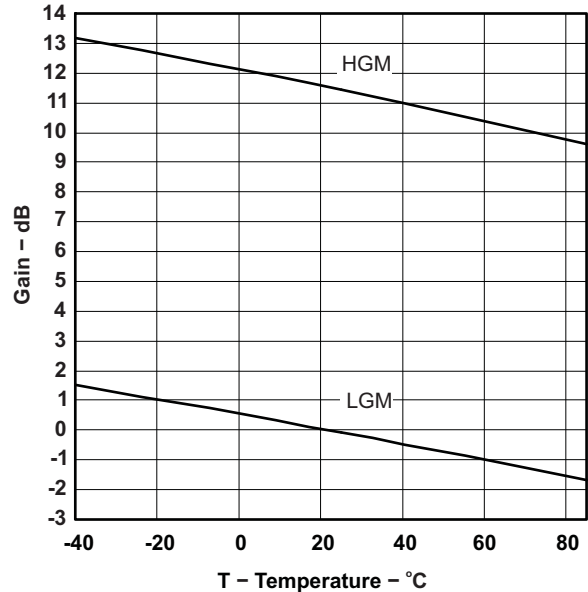


Figure 4.

LNA GAIN
VS
POWER SUPPLY

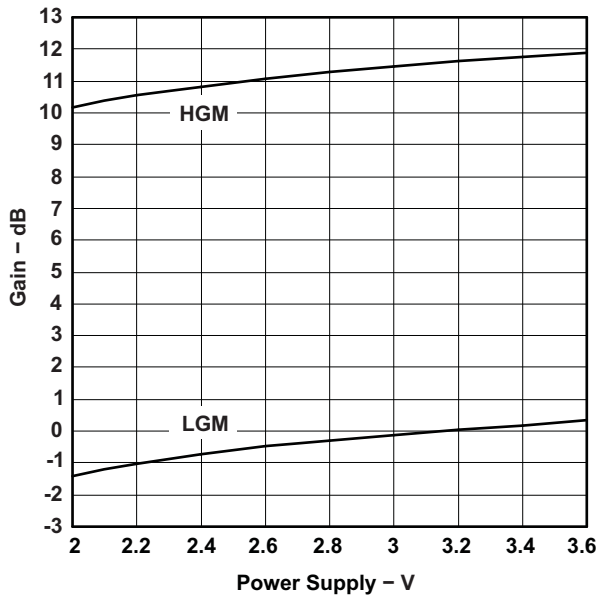


Figure 5.

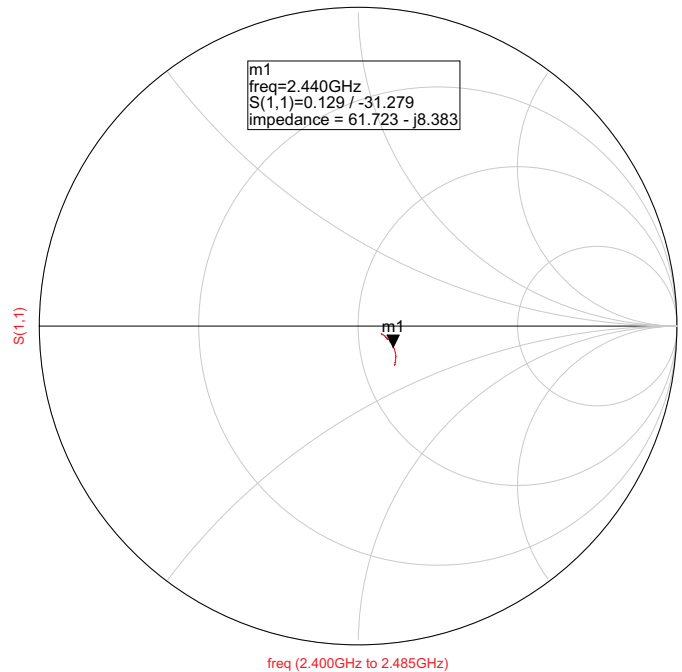


Figure 6. Input Impedance of LNA Measured from Antenna Port on CC2590EM

TYPICAL CHARACTERISTICS (continued)

OUTPUT POWER, PAE AND CURRENT CONSUMPTION VS INPUT POWER

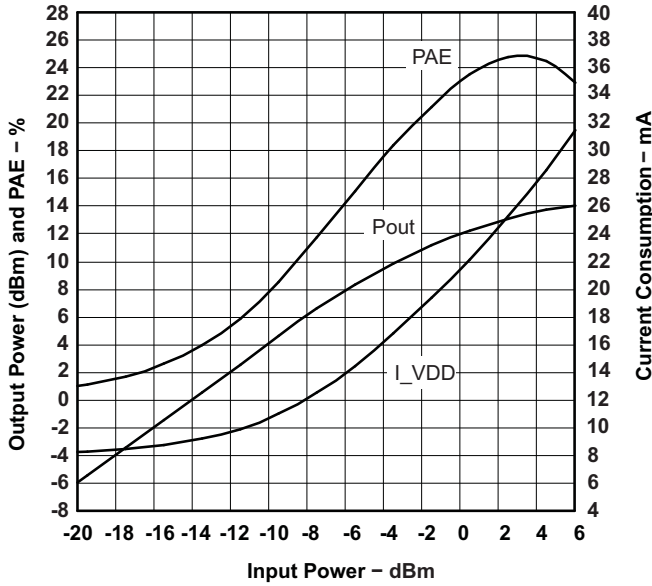


Figure 7.

OUTPUT POWER, PAE AND CURRENT CONSUMPTION VS FREQUENCY

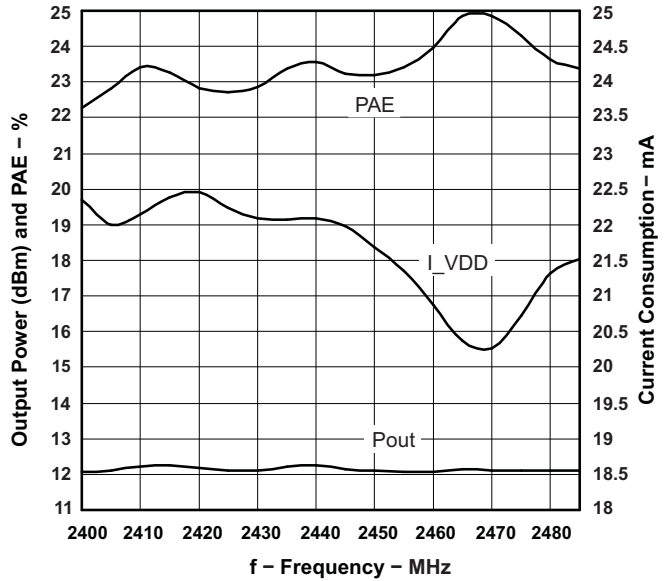


Figure 8.

OUTPUT POWER, PAE AND CURRENT CONSUMPTION VS TEMPERATURE

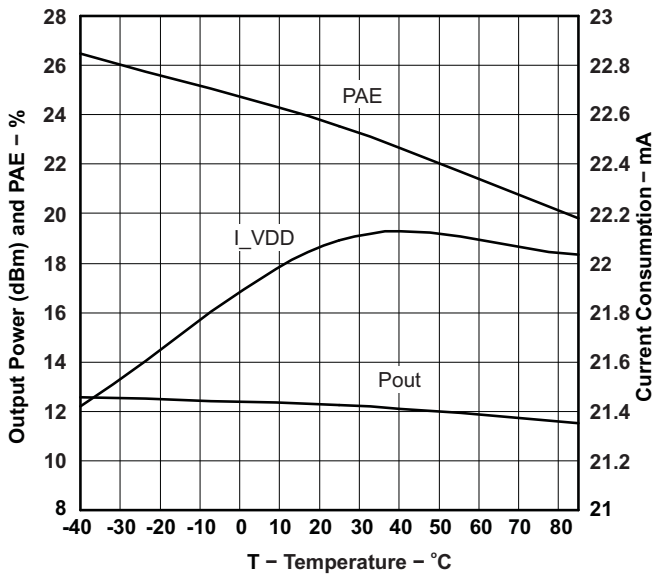


Figure 9.

OUTPUT POWER, PAE AND CURRENT CONSUMPTION VS POWER SUPPLY

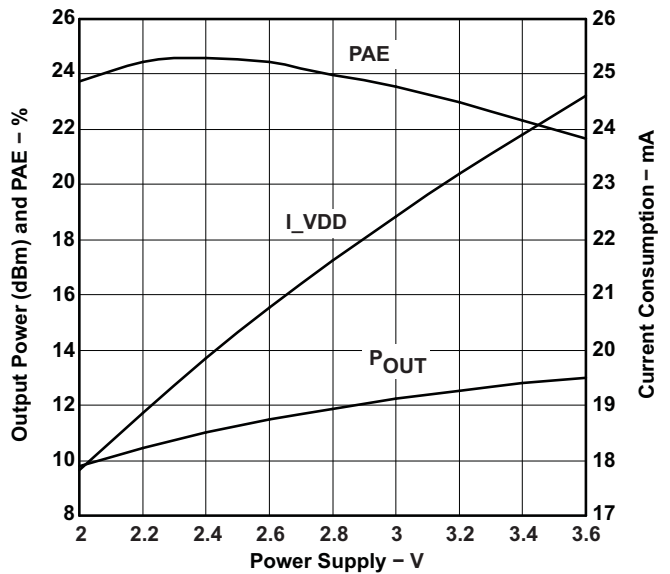


Figure 10.

Controlling the Output Power from CC2590

The output power of CC2590 is controlled by controlling the input power. The CC2590 PA is designed to work in compression (class AB), and the best efficiency is reached when a strong input signal is applied.

Input Levels on Control Pins

The four digital control pins (PAEN, EN, HGM, RXTX) have built-in level-shifting functionality, meaning that if the CC2590 is operating from a 3.6-V supply voltage, the control pins will still sense 1.6-V - 1.8-V signals as logical '1'.

An example of the above would be that RXTX is connected directly to the RXTX pin on CC24xx, but the global supply voltage is 3.6-V. The RXTX pin on CC24xx will switch between 0-V (RX) and 1.8-V(TX), which is still a high enough voltage to control the mode of CC2590.

The input voltages should however not have logical '1' level that is higher than the supply.

Connecting CC2590 to a CC24xx Device

Table 3. Control Logic for Connecting CC2590 to a CC24xx Device

| PAEN = EN | RXTX | HGM | MODE OF OPERATION |
|-----------|------|-----|-------------------|
| 0 | X | X | Power Down |
| 1 | 0 | 0 | RX Low Gain Mode |
| 1 | 0 | 1 | RX High Gain Mode |
| 1 | 1 | X | TX |

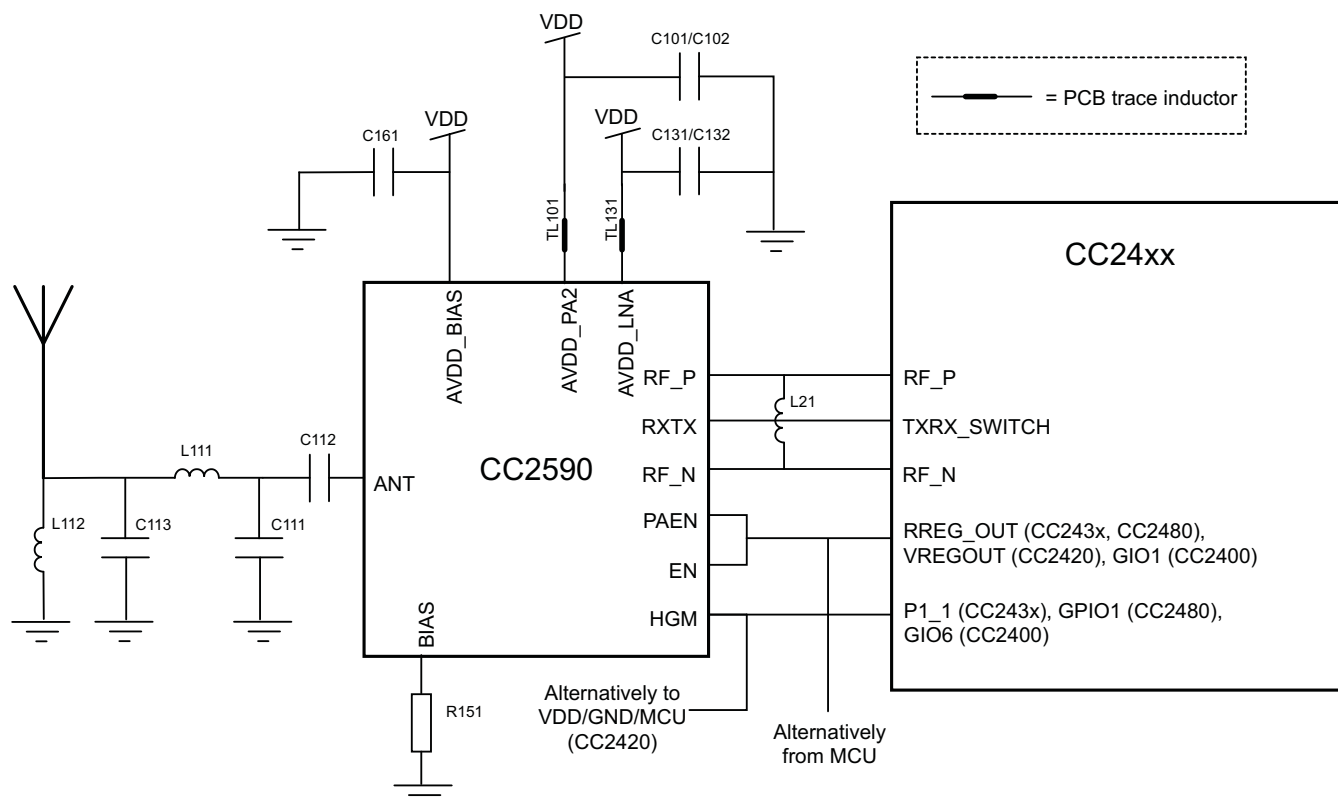


Figure 11. CC2590 + CC24xx Application Circuit

Connecting CC2590 to the CC2500, CC2510, or CC2511 Device

Table 4. Control Logic for Connecting CC2590 to a CC2500/10/11 Devices

| PAEN | EN | RXTX | HGM | MODE OF OPERATION |
|------|----|------|-----|-------------------|
| 0 | 0 | NC | X | Power Down |
| 0 | 1 | NC | 0 | RX Low Gain Mode |
| 0 | 1 | NC | 1 | RX High Gain Mode |
| 1 | 0 | NC | X | TX |
| 1 | 1 | NC | X | Not allowed |

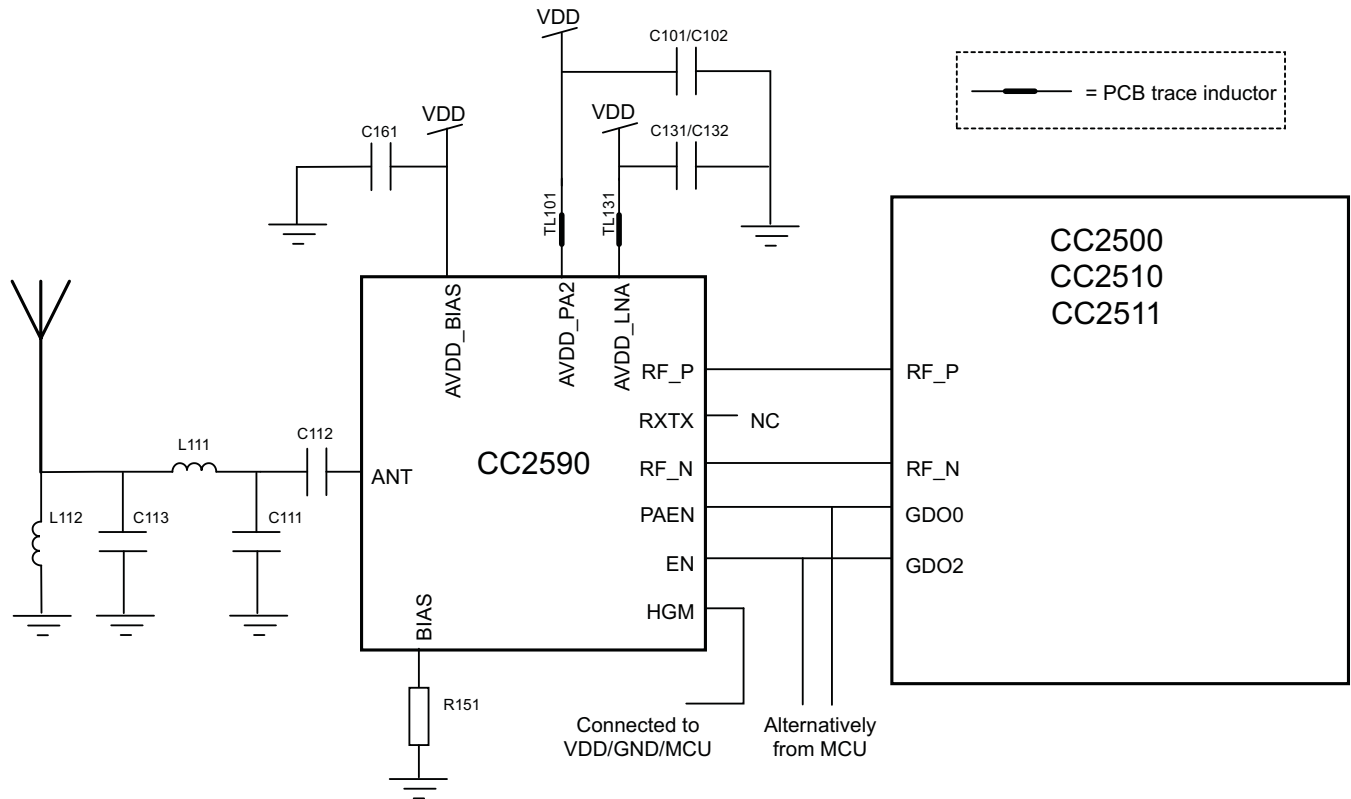


Figure 12. CC2590 + CC2500/10/11 Device Application Circuit

Connecting CC2590 to a CC2520 Device

Table 5. Control Logic for Connecting CC2590 to a CC2520 Device

| PAEN | EN | RXTX | HGM | MODE OF OPERATION |
|------|----|------|-----|-------------------|
| 0 | 0 | NC | X | Power Down |
| 0 | 1 | NC | 0 | RX Low Gain Mode |
| 0 | 1 | NC | 1 | RX High Gain Mode |
| 1 | 0 | NC | X | TX |
| 1 | 1 | NC | X | Not allowed |

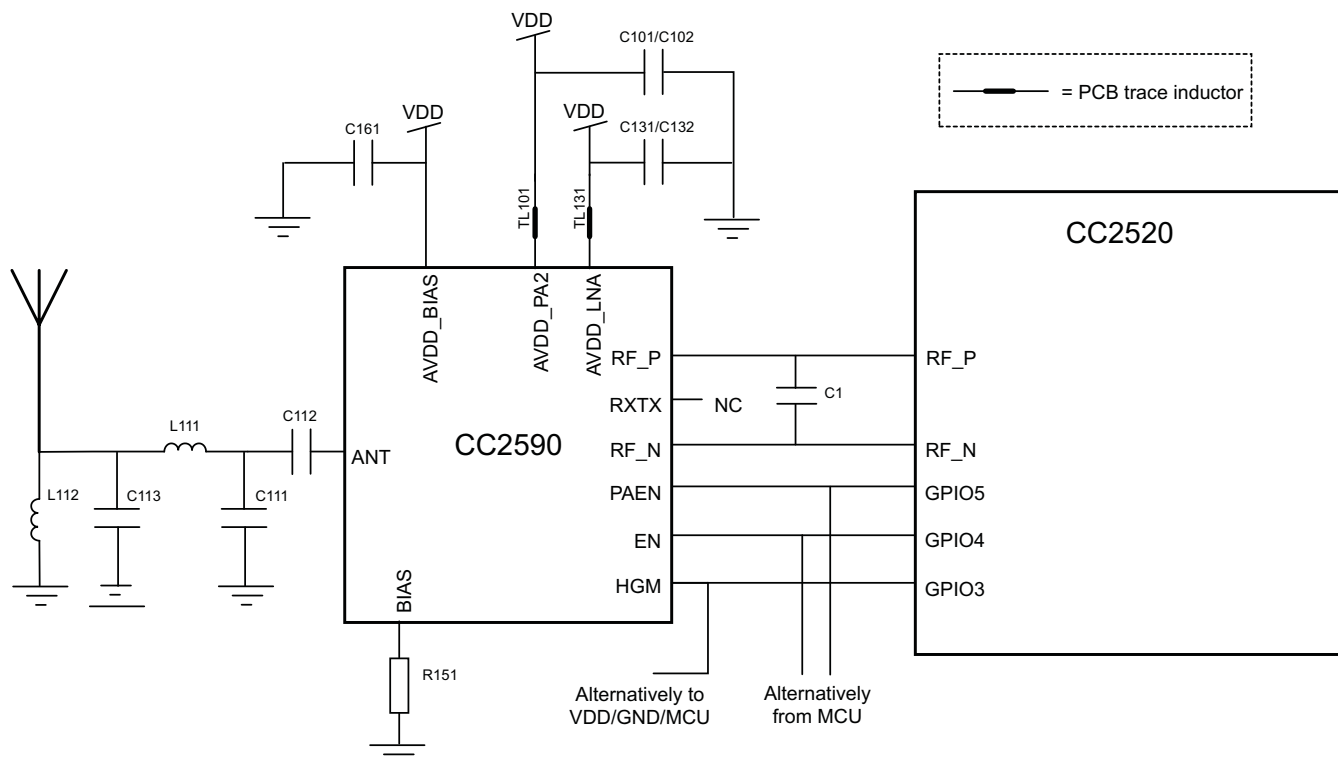


Figure 13. CC2590 + CC2520 Application Circuit

PCB Layout Guidelines

The exposed die attach pad must be connected to a solid ground plane as this is the primary ground connection for the chip. Inductance in vias to the pad should be minimized. It is highly recommended to follow the reference layout. Changes will alter the performance. Also see the PCB landpattern information in this data sheet. For best performance, minimize the length of the ground vias, by using a 4-layer PCB with ground plane as layer 2 when CC2590 is mounted onto layer 1.

PCB trace inductors are used to be able to optimize the inductance value, and they are too small to be replaced by discrete inductors. The placement of the power supply decoupling capacitors C101/C102 and C131/C132 are important to set the PCB trace inductance values accurately.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CC2590RGVR | ACTIVE | VQFN | RGV | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CC2590 | Samples |
| CC2590RGVRG4 | ACTIVE | VQFN | RGV | 16 | 2500 | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| CC2590RGVT | ACTIVE | VQFN | RGV | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CC2590 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CC2590RGVR | VQFN | RGV | 16 | 2500 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CC2590RGVT | VQFN | RGV | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CC2590RGVR | VQFN | RGV | 16 | 2500 | 367.0 | 367.0 | 35.0 |
| CC2590RGVT | VQFN | RGV | 16 | 250 | 210.0 | 185.0 | 35.0 |

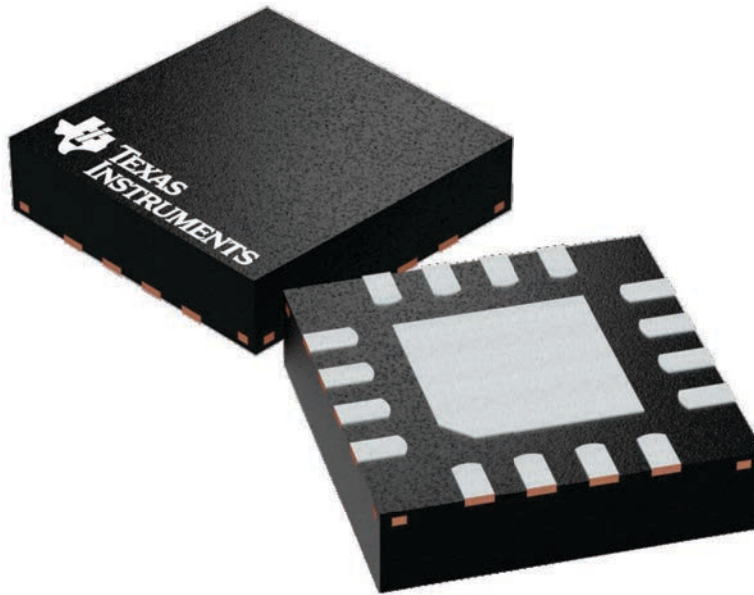
GENERIC PACKAGE VIEW

RGV 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

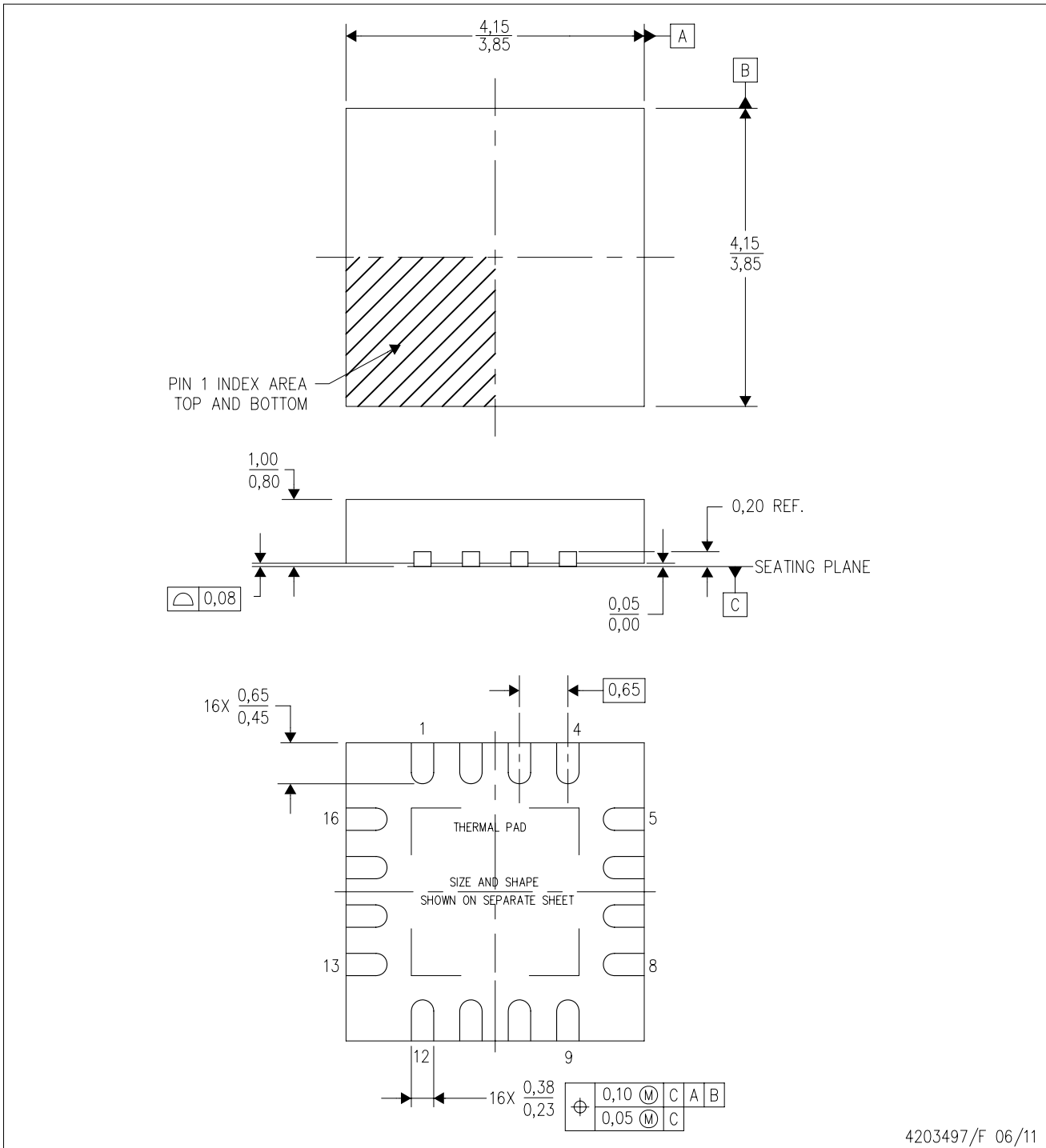


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224748/A

RGV (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203497/F 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGV (S-PVQFN-N16)

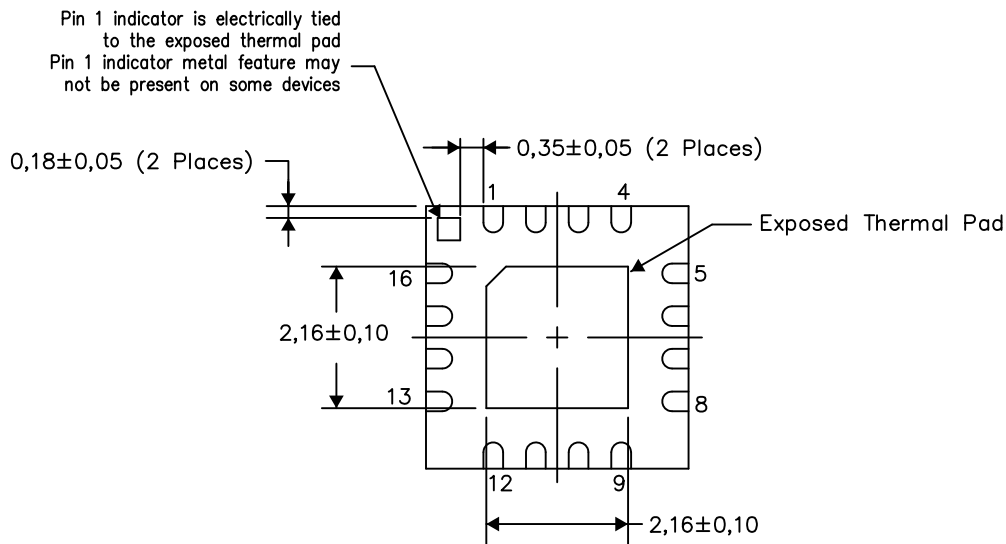
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206351-2/L 05/13

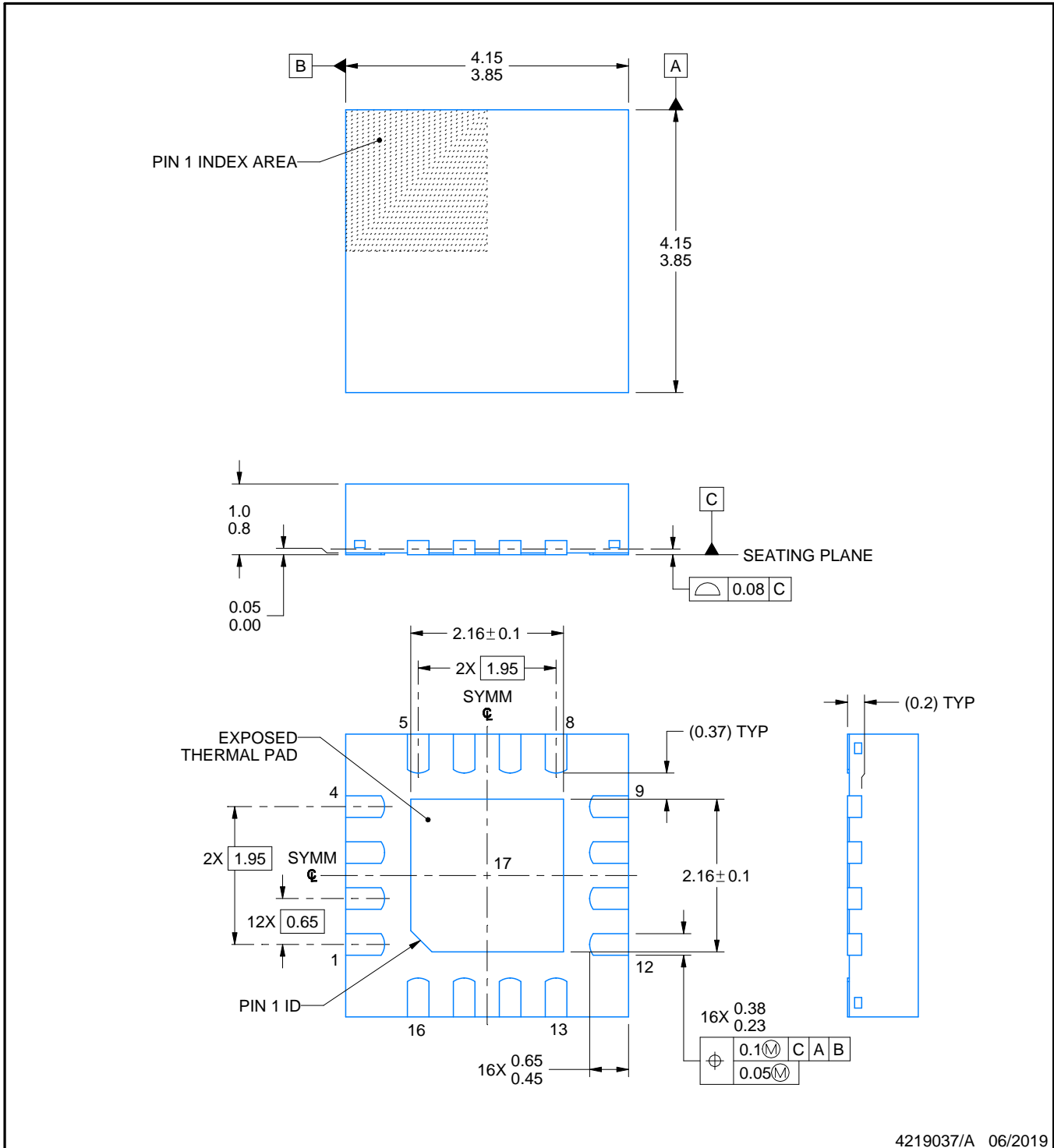
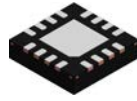
NOTE: All linear dimensions are in millimeters

RGV (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for solder mask tolerances.



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NOTES:

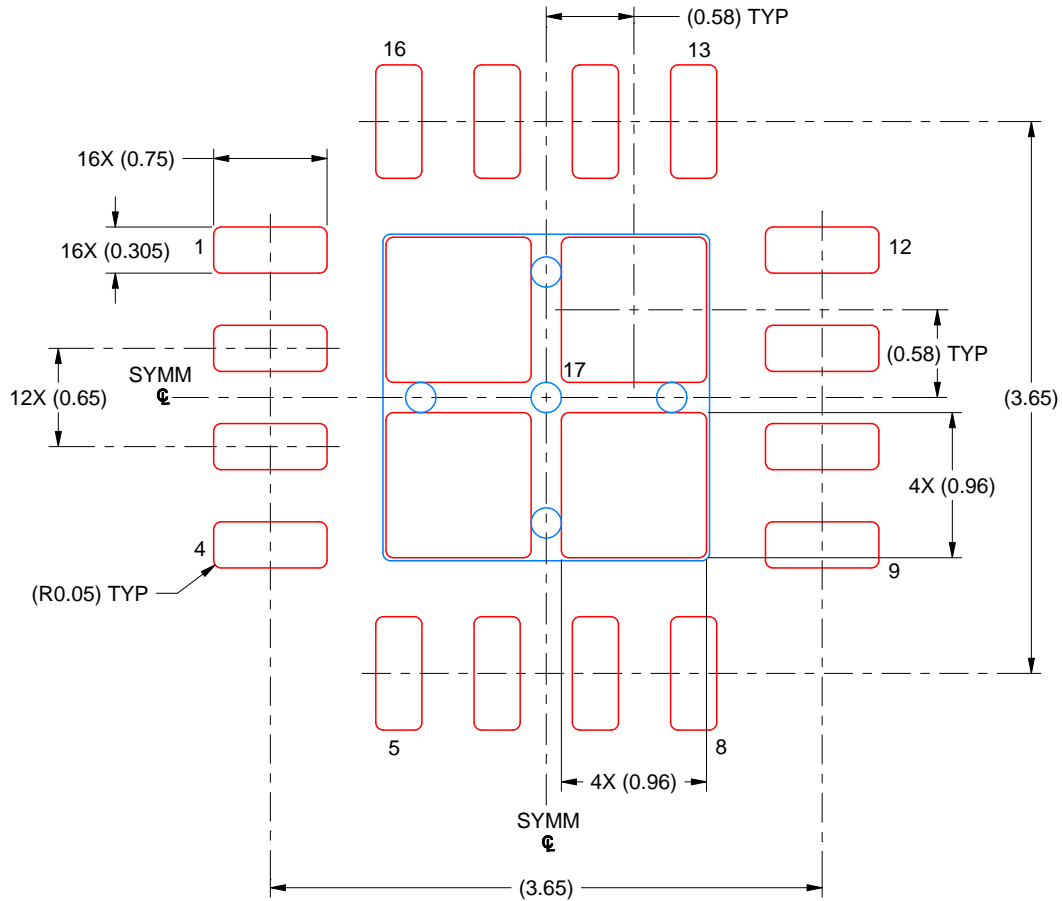
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

RGV0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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