User's Guide
SWRU536–January 2019

CC3x35 SimpleLink™ Wi-Fi® and IoT solution layout guidelines

The CC3x35 SimpleLink™ Wi-Fi® device is part of the SimpleLink™ microcontroller (MCU) platform that consists of Wi-Fi®, *Bluetooth*® low energy, Sub-1 GHz and host MCUs. All share a common, easy-to-use development environment with a single core software development kit (SDK) and rich tool set. A one-time integration of the SimpleLink™ platform lets you add any combination of devices from the portfolio into your design. The ultimate goal of the SimpleLink™ platform is to achieve 100 percent code reuse when your design requirements change. For more information, visit www.ti.com/simplelink

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Trademarks

1 Introduction

This user's guide provides the design guidelines of the 4-layer PCB used for the CC3135 and CC3235 SimpleLink™ Wi-Fi® family of devices from Texas Instruments™. The CC3135 and CC3235 are available in quad flat no-leads (QFNS) packages. When designing the board, follow the suggestions in this document to optimize performance of the board.

This user's guide includes the following:

- A brief overview of the SimpleLink™ Wi-Fi® family of devices
- Overview of the PCB specification, components placement, and board layer information
- Layout guidelines that describe the main sections of the board such as radio frequency (RF), power, clock, digital input and output, and the ground

Each section can be independently read. This user's guide focuses on the CC3235-LAUNCHXL board as the layout for the CC3235 device, which is a superset of the CC3135 device. Any exceptions to this layout are explained separately. The CC3235-LAUNCHXL is also referred to as LaunchPad™ (LP).

In addition to this user's guide, TI recommends verifying the schematic board design with the *CC3135, CC3235 SimpleLink™ Wi-Fi® Hardware Design Checklist*.

Start the design with the industry's first Internet-on-a chip™. Created for the Internet of Things (IoT), the SimpleLink™ Wi-Fi® family has several variants. The CC3135 SimpleLink™ Wi-Fi® and IoT solution dramatically simplify the implementation of Internet connectivity. This product integrates all protocols for Wi-Fi® and Internet, which greatly minimizes host microcontroller (MCU) software requirements. The CC3235 device is a dual band wireless MCU that integrates a high-performance Arm® Cortex®-M4 MCU with the CC3135 network processor subsystem, allowing customers to develop an entire application with a single integrated chip (IC). With on-chip Wi-Fi®, Internet, and robust security protocols, no prior Wi-Fi® experience is needed for faster development. SimpleLink™ Wi-Fi® is a complete platform solution that includes:

- Various tools and software
- Sample applications
- User's guides and programming guides
- Reference designs
- TI E2E™ support community

The devices are available in a QFN package that simplify the layout design.

NOTE: All figures and references in this document apply to Rev. A and Rev. B. Most of the document also applies to higher revisions, unless otherwise stated. For the exact list of changes made across board revisions, see the Revision History.

2 PCB Specification

2.1 PCB Stackup

Table 1 shows an example stackup used to construct the CC3235-LAUNCHXL Rev. A. The user can alter the layer stackup based on their requirements, but the impedance of the 50-Ω lines must be recalculated. Reducing the distance from Layer 1 (L1) to Layer 2 (L2) helps improve the power grounding and the RF decoupling, because it lowers the overall through inductance. TI recommends keeping the distance from L1 to L2 similar to, or lower than the recommended value.

Table 1. Example Stackup

Type	Layer (Layer Name)	Dielectric Constant	Height (mil)
Mask		4.1	.8
Copper	L1 (Top)		1.69
FR-4		3.9	9.3
Copper	L2 (GND)		1.42
FR-4		4.24	24.02
Copper	L3 (Signal)		1.42
FR-4		3.9	9.3
Copper	L4 (Signal)		1.69
Mask		4.1	.8
	Tolerance = ±10%	Total	50.44

2.2 PCB Design Rules

Table 2 lists the PCB design rules.

Table 2. PCB Design Rules

Parameter	Value	Comments
Number of layers	4	—
Thickness	50.44 mil ±10%	For greater thickness, increase the distance between L2 and L3.
Size of PCB	2.3” × 4.1”	Can be altered to suit the customer requirement. A smaller PCB size results in poor antenna performance. A size of 2.3” × 2.2” is verified for the CC3135 device.
Dielectric	FR4	—
Surface finish	ENIG	
Minimum track width	6 mils	Minimum track width can be reduced, but the cost would increase.
Minimum spacing	6 mils	Minimum spacing can be reduced, but the cost would increase.
Mid drill diameter	8 mils	8-mil diameter drill is used on the CC3235x-LAUNCHXL Rev A board. 12-mil diameter drill is used on the CC3135 device because it has less pins to route.
Copper thickness	1 oz	—
Lead free / ROHS	Yes	—
Impedance control	Yes, 50Ω	50Ω controlled impedance trace of 15 mils wide on the L1 with respect to L2 ground (GND). Air gap = 10 mils.(1)
Impedance variation	±10%	—

(1) These calculations are based on a coplanar waveguide with ground (CPW-G) not microstrip. The estimation could be performed using tools like AWR TX Line, Saturn PCB Toolkit, and Agilent ADS, among others.

2.3 Layer Information

Table 3 describes the 4-layer PCB configuration.

Table 3. 4-Layer PCB

Layer	Usage	Notes
1	Signal plus RF	RF trace is a Coplanar Waveguide with ground routed on the L2 ground.
2	GND	Reference plane for the RF and power ground. The power plane has special routing to improve the spectral mask performance.
3	Power plus signal	The power planes for the power amplifier, analog blocks, and the main input supply are routed on this layer.
4	Power plus signal	All remaining signals are routed on this layer.

3 Layout Information

The complete layout package in Altium format is available for download from *CC3135, CC3235 SimpleLink™ Wi-Fi® Hardware Design Checklist*.

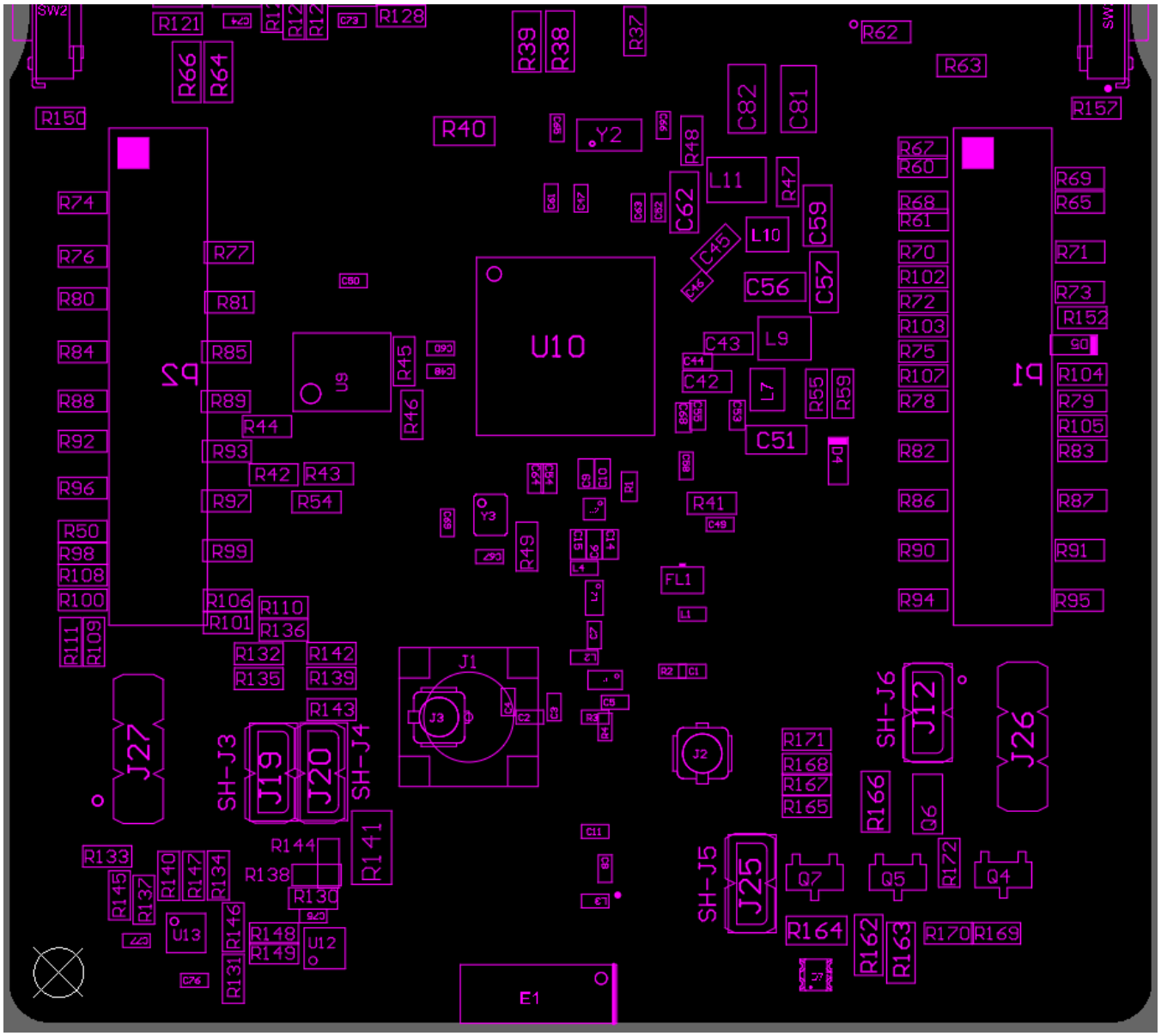
CAUTION

TI recommends copying the exact layout of the engine area, which is marked by a box on the silkscreen, to ensure optimum performance as measured on the CC3x35 reference boards. Failure to adhere to this recommendation can lead to performance degradation, including spectral mask degradation, error vector magnitude (EVM) failures, and power supply instability.

3.1 Components Placement

Figure 1 shows the placement of the CC3235 LaunchPad™ components. This placement provides optimum performance of the device. Users must take great care of the power inductors components to ensure reduced emissions and optimum EVM and mask performance. Place the power inductors very close to the device, and minimize the length of the power traces. The CC3x35 device is sensitive to the layout of components of DC/DC converters, and placement can impact the performance of the device.

Figure 1. CC3235XX-LAUNCHXL RevA Placement Diagram

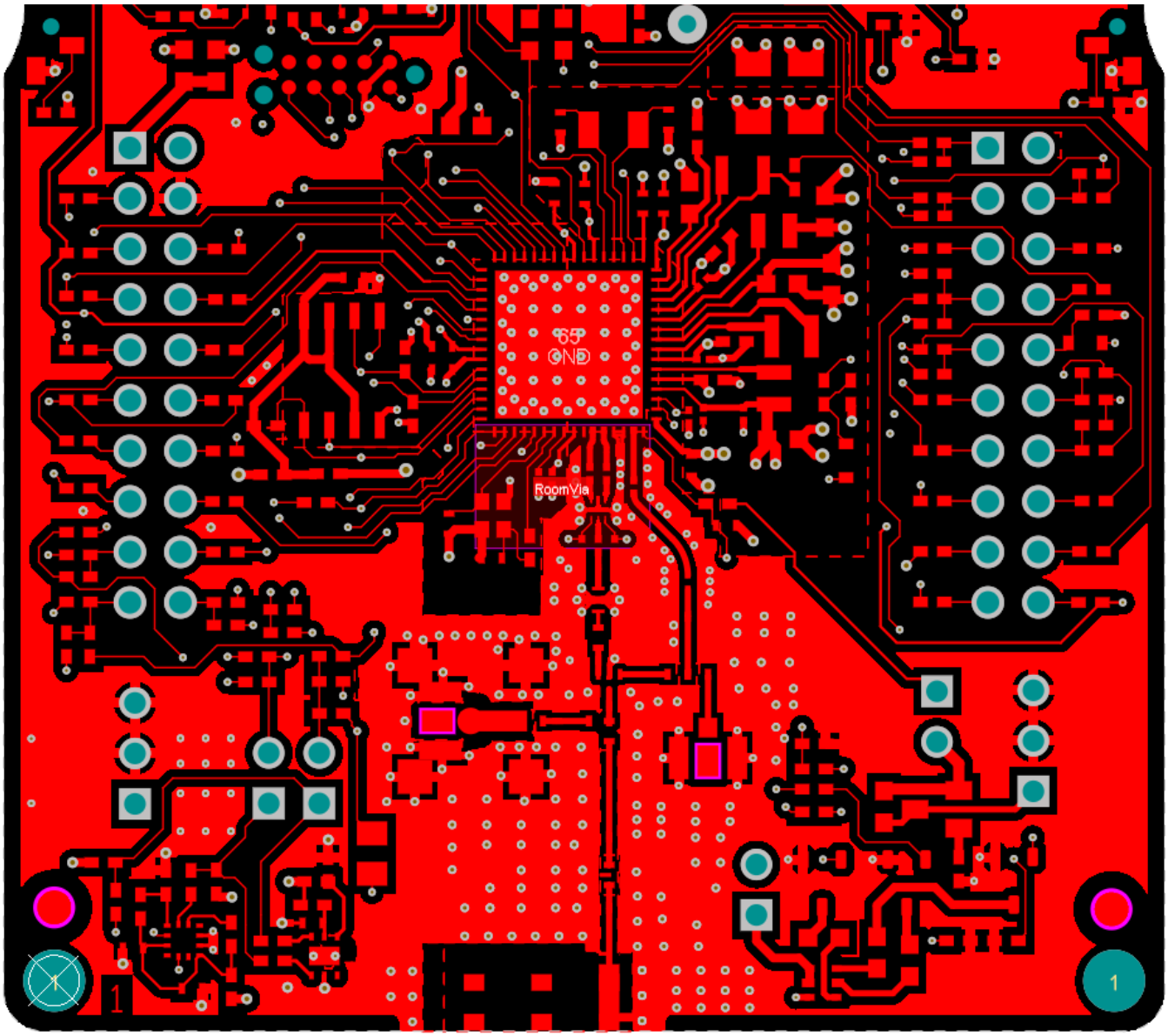


3.2 Layer Information

3.2.1 Layer 1

Figure 2 shows layer 1 (L1) where most of the routing is performed, to avoid vias on the board. The trace widths are maximized for high-current pins and minimized for signal pins. For example, the signal pins can be routed with 6 mils (4 mils if possible), and the power pins with 12 mils and greater.

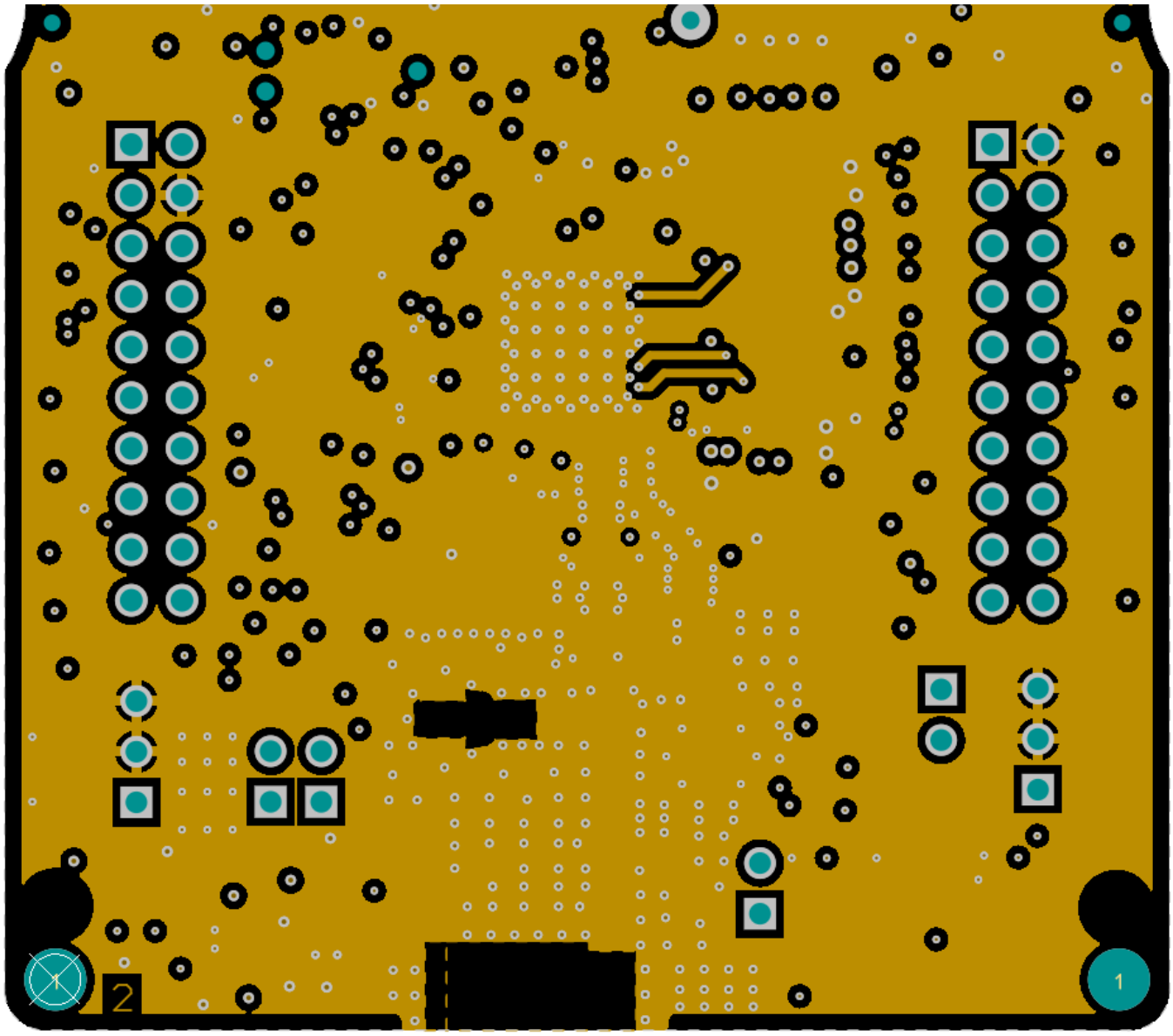
Figure 2. Layer 1



3.2.2 Layer 2

Figure 3 shows layer 2 (L2), the primary ground plane for the board reference. L2 has a void for the antenna section, which is reflected on all the layers, per the antenna guidelines. Three traces are routed on the GND layer. These traces are return current path for the input decoupling capacitors (C47, C48, and C49) routed on L2 using thick traces, to isolate the RF ground from the noisy supply ground. This routing is an example of single-point grounding where the return currents are not made to flow on the ground plane. This grounding avoids the common impedance coupling between the DC/DC converter and RF sections, which is required to improve the IEEE spectral mask margins. The SMA / u.FL path is referenced to layer 3 (L3) with void placed on the GND layer (L2) for optimal RF performance and reduced loss particularly at higher frequency

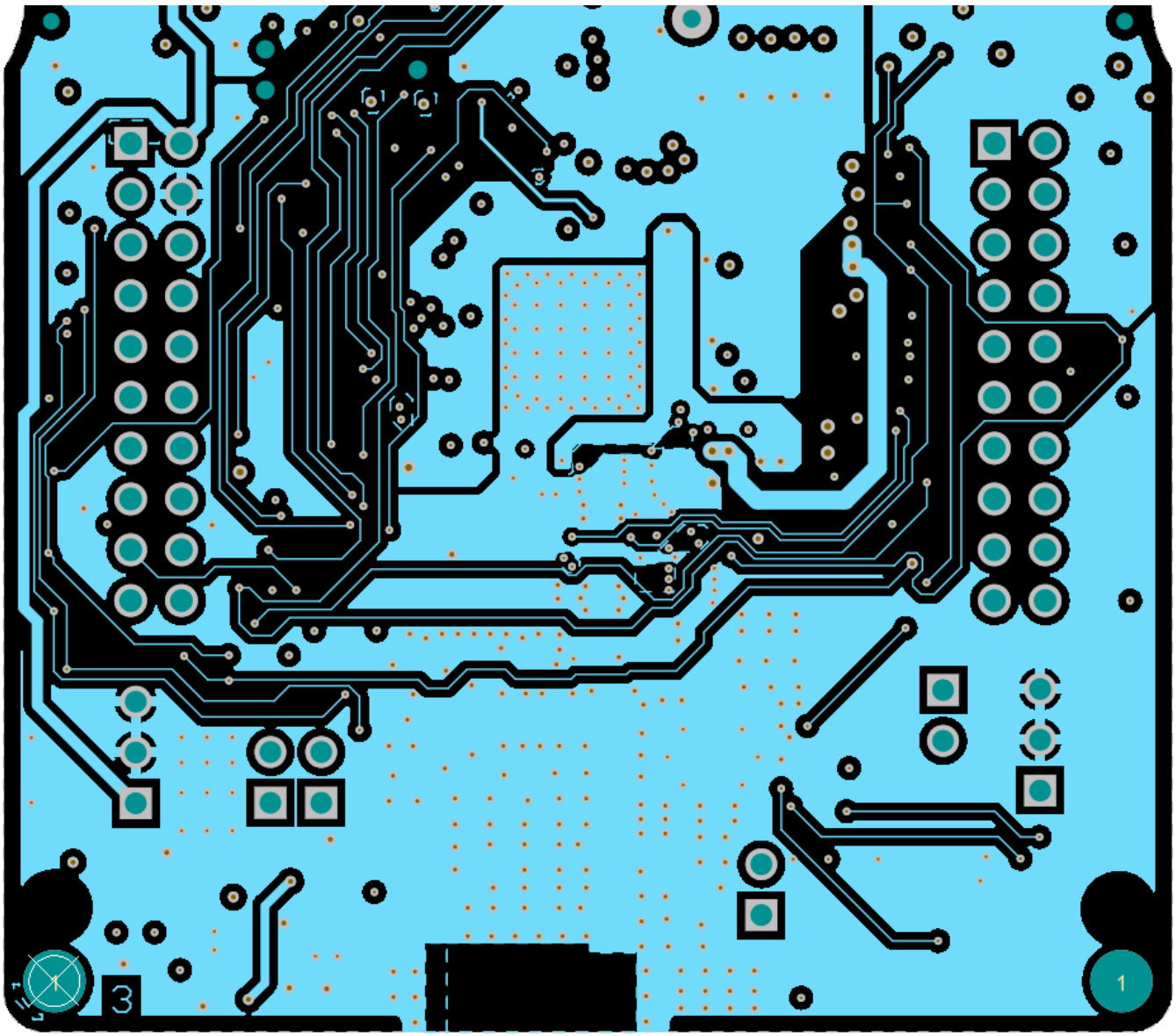
Figure 3. Layer 2



3.2.3 Layer 3

Figure 4 shows layer 3 (L3) that routes the power lines to the device. Power planes are necessary for the power amplifier (PA) and the main supply input to the device. More details are available in subsequent sections.

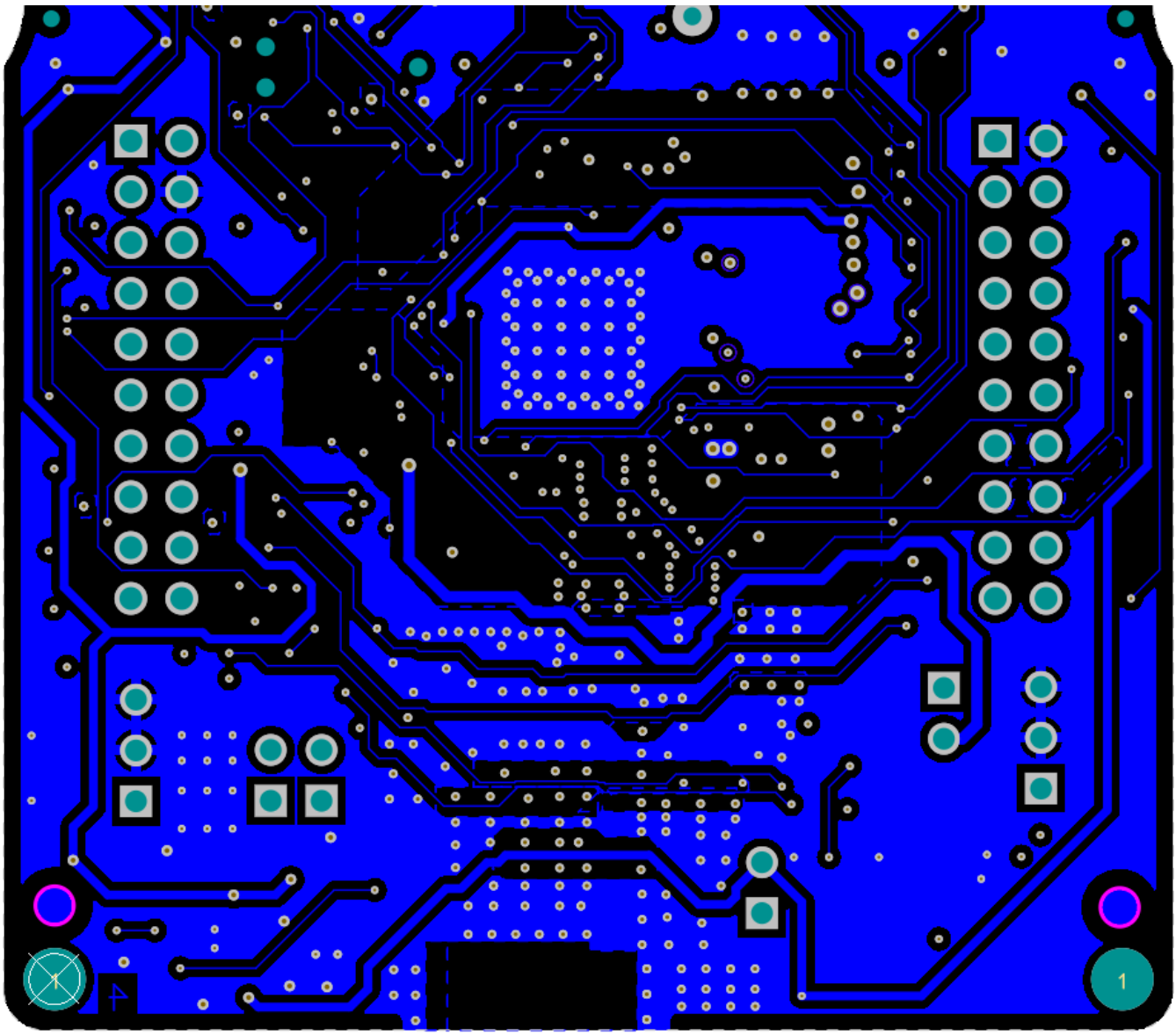
Figure 4. Layer 3



3.2.4 Layer 4

Figure 5 shows layer 4 (L4) that routes the power and signal lines on the board. L4 is also the main power dissipation GND layer for the QFN package. Users must maximize the bottom GND plane for the best thermal performance.

Figure 5. Layer 4

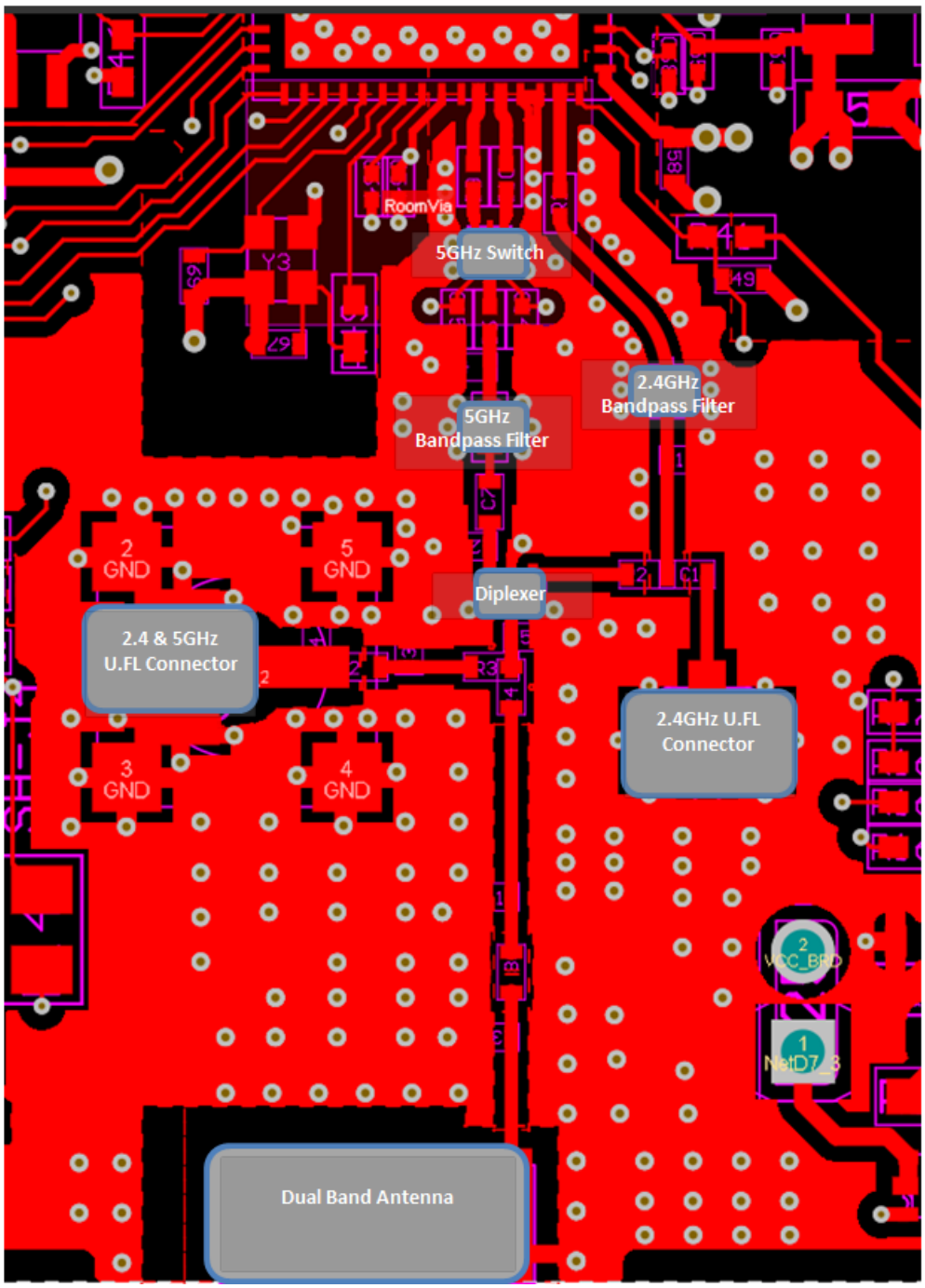


4 Layout Guidelines

4.1 RF Section

Figure 6 shows the RF section, shows the RF section, which require special care for the layout to keep the WLAN RF performance . The RF section must be laid out correctly to get the optimum performance from the device. A poor layout can cause performance degradation for the output power, EVM, sensitivity, and spectral mask.

Figure 6. RF Section Layout



4.1.1 Antenna Placement and Routing

The antenna is the element which converts the guided waves on the PCB traces to the free-space electromagnetic radiation. The placement and layout of the antenna is key to increased range and data rates.

Table 4 explains the guidelines that must be observed for the antenna.

Figure 7. Antenna Placement

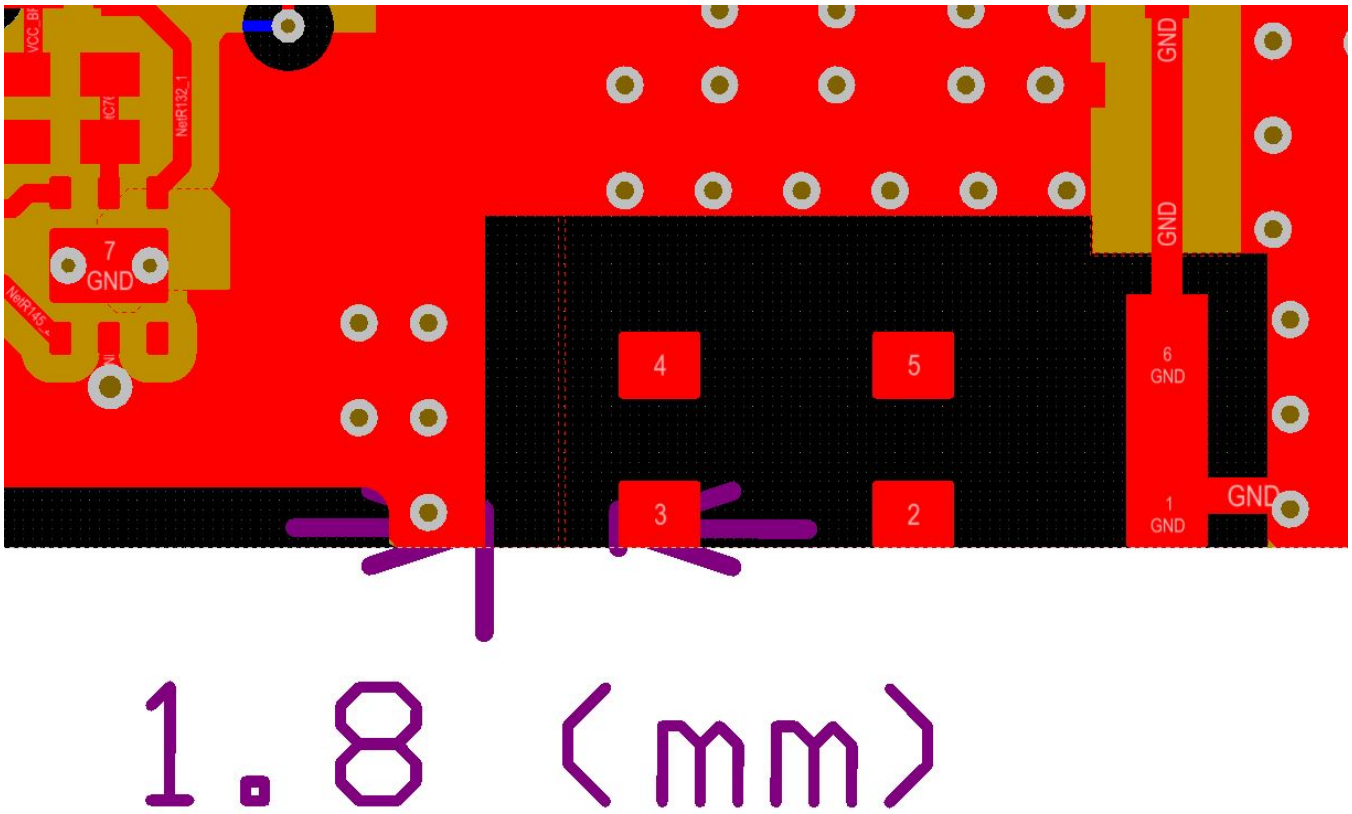


Table 4. Antenna Guidelines

Sr No.	Guidelines
1	Place the antenna on an edge or corner of the PCB, depending on the manufacturer's recommendation. For the LAUNCHXL-CC3235x, the recommendation from the antenna manufacturer is to place the antenna centered and on the edge of the board.
2	When using the recommended antenna, ensure that the antenna spacing to ground is 1.8 mm, as shown in Figure 7.
3	Ensure no signals are routed across the antenna element, or void space, on all layers of the PCB.
4	Most antennas, including the chip antenna used on the TI reference designs, require ground clearance on all layers of the PCB. Ensure that the ground is cleared on inner layers as well.
5	Ensure there is provision to place π matching components for the antenna. The antenna must be tuned for best return loss when the complete board is assembled. Any plastic or casing must also be mounted while tuning the antenna, because this can impact the impedance.
6	Ensure the antenna impedance is 50 Ω, because the device is rated to work only with a 50-Ω system. A voltage standing-wave ratio (VSWR) of 2:1 is acceptable.
7	For a printed antenna, ensure that the simulation is performed with the solder mask considered.
8	Recommend the antenna has a near omnidirectional pattern. Peaks and nulls could cause reception problems if the access point is aligned with the null of the CC3235 board antenna.
9	For optimal antenna performance, ensure adequate ground plane around the antenna on all layers.

Table 5 describes the recommended components.

Table 5. Recommended Components

Choice	Part Number	Manufacturer	Notes
1	AH316M245001-T	Taiyo Yuden	Can be placed on the edge of the PCB, and uses less PCB space . (2.4GHz only)
2	RFANT5220110A2T	Walsim	Must be placed on the corner of the PCB (2.4GHz only)
3	M830520	Ethertronics	Place on edge of board per manufacturers recommendation (Dual Band Antenna)

Table 6 describes the characteristics of the recommended antenna.

Table 6. Characteristics of Recommended 2.4-GHz Antenna

Parameter	Specification
Frequency bandwidth	2.4 GHz to 2.5 GHz
Typical peak gain	+1.9 dBi
Average gain at OMNI plane	0 dBi
Efficiency (typical)	–1.3 dB (73%)
VSWR	2:1

Table 7 describes the characteristics of the recommended dual band antenna.

Table 7. Characteristics of Recommended Dual Band Antenna

Parameter	Specification	Specification
Frequency bandwidth	2.4 GHz to 2.5 GHz	4.9 GHz to 5.8 GHz
Typical peak gain	+1 dBi	+2.6 dBi
Average gain at OMNI plane	+0.5 dBi	+1 dBi
Efficiency (typical)	–2.08 dB (62%)	–2.52 dB (56%)
VSWR	2.6:1 max	3.0:1 max

4.1.2 Diplexer Placement and Routing

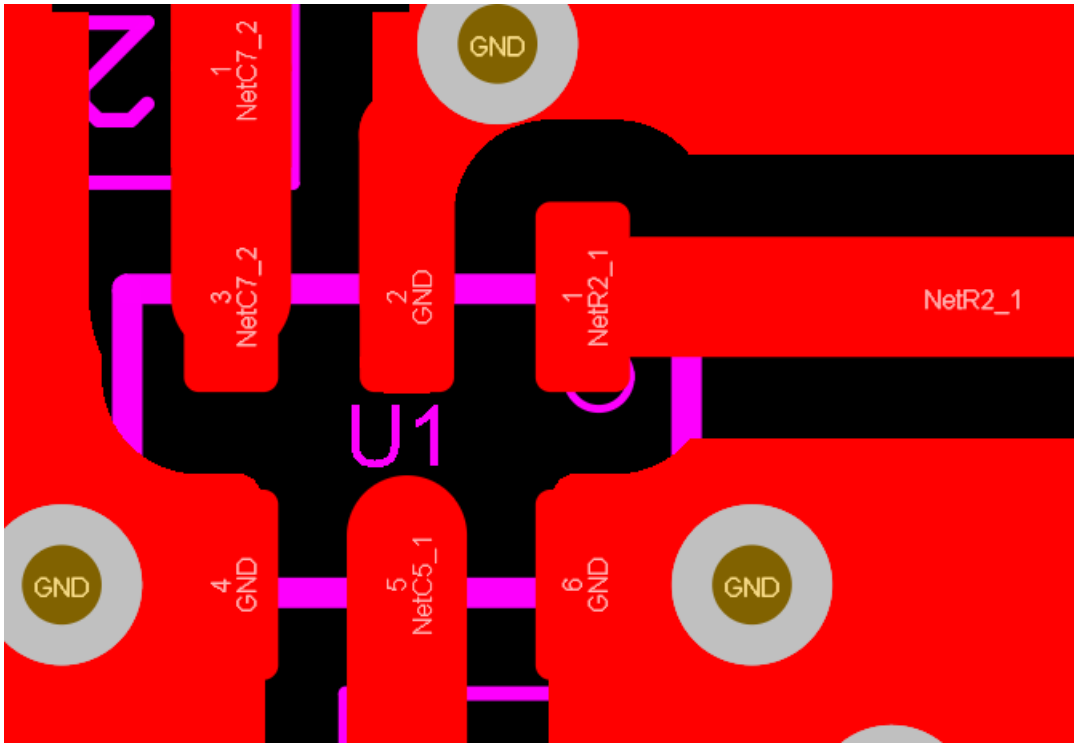
The diplexer is a passive element used to split/combine signals from the antenna port into the 2.4GHz and 5GHz port. When placing the diplexer on the board ensure the high and low band signal are routed to the right port per manufacturers specification. Table 8 list the recommended part number

Table 8. Recommended Part Numbers

Choice	Part Number	Manufacturer	Notes
1	DPX165950DT-8148A1	TDK	-

Figure 8 shows the diplexer routing. Ensure the ground pads of the diplexer have a good ground connection to the L2 ground plane using vias

Figure 8. Diplexer Placement



4.1.3 Filter Placement and Routing

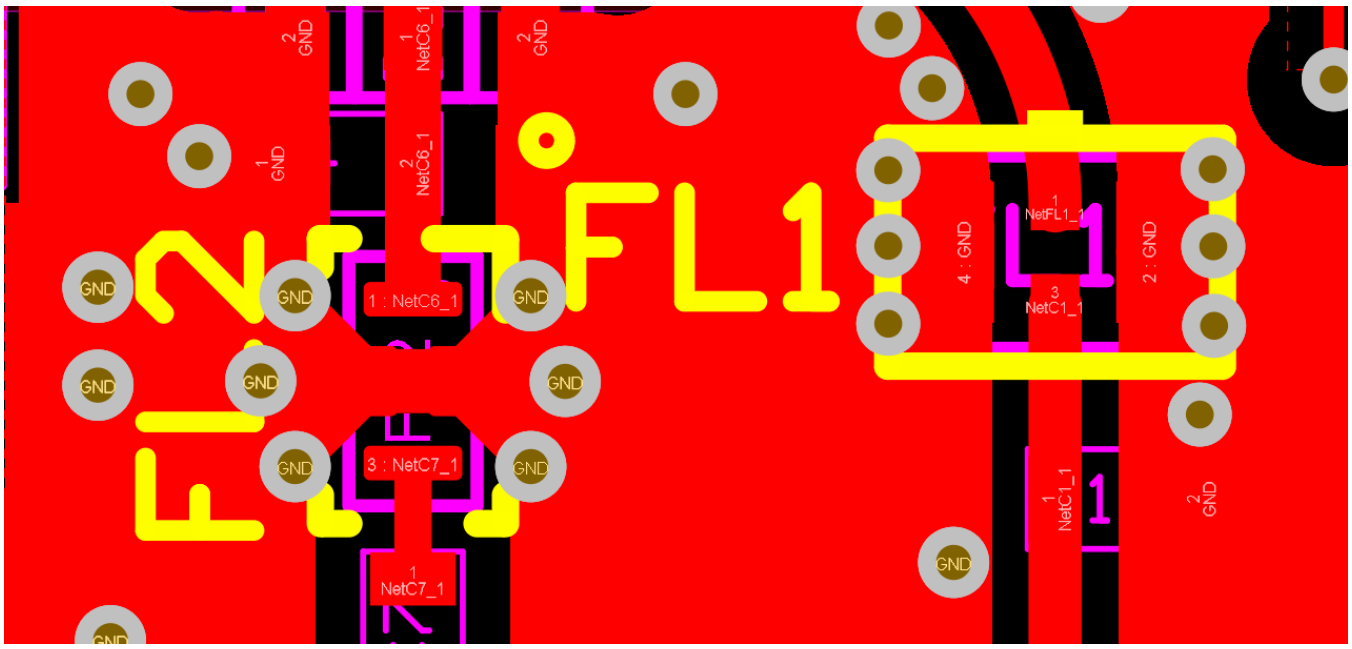
The RF filter on the board performs the important function of attenuating the out-of-band emissions from the device. Table 9 lists the recommended part numbers.

Table 9. Recommended Part Numbers

Choice	Part Number	Manufacturer	Notes
1	DEA202450BT-1294C1-H	TDK/Epcos	Lowest insertion loss (used on TI EVM)
2	RFBPF2012080AC2T00	Walsin/Passive components	Evaluated by TI to meet emission norms
3	DEA165538BT-2236B1-H	TDK	Multilayer Band Pass Filter For 5GHz WLAN

Figure 9 shows the RF filter routing.

Figure 9. Filter Placement



The RF filter must be placed close to the device pin, between the antenna and the device. The RF filter should have a good ground connection to the L2 ground plane. TI recommends adding at least two ground vias near the ground pins to ensure good RF grounding.

Table 10 explains the filter routing guidelines.

Table 10. Filter Guidelines

Sr No	Guidelines	Notes
1	Route the RF lines at the input and output of the filter using appropriate transmission line and ground structure.	Consider the structure that offers the best isolation between the input and output, reduced field fringing and
2	Where feasible, use via stitching along the RF trace to reduce emissions, and keep the fields confined to the trace boundary.	CPW with GND and via stitching, microstrip, stripline can be accurately simulated using 3D EM tools like EESOF, ADS etc
3	Use a Z_O of 50 Ω with only a tolerance of 10%. Use the stackup and trace width provided for reference in Table 2.	—
4	Add multiple ground vias for the filter ground pads, as close as possible. A minimum of two vias per GND pad is recommended.	—
5	To achieve the specifications of the filter attenuation, the minimum isolation between the input and output ports of the filter must be at least 60 dB (measured without the filter).	—
6	The solder paste on the ground pin is split into halves to ensure a reliable solder joint. Having a single ground on the paste causes the component to lift up during reflow.	—

4.1.4 Switch Placement and Routing

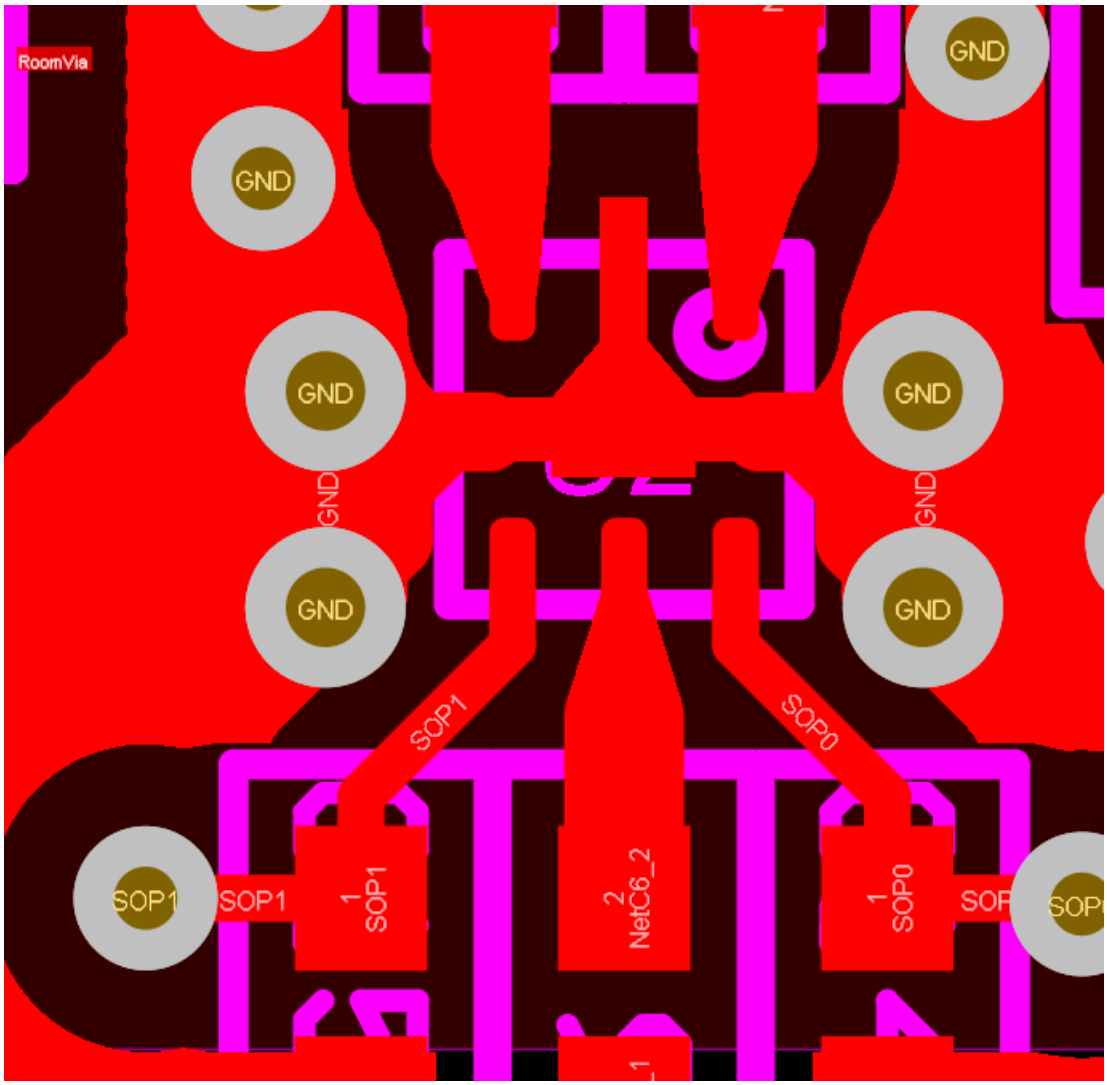
The SPDT RF switch is for insertion or isolation of signals on 5-GHz RX and TX ports to/from the output port depending on the state of the control pins (SOP 0 and SOP1). Table 11 lists the recommended part numbers.

Table 11. Recommended Part Numbers

Choice	Part Number	Manufacturer	Notes
1	RTC6608OSP	Richwave	-

Figure 10 shows the RF switch routing.

Figure 10. Switch Placement



The RF switch should have a good ground connection to the L2 ground plane. TI recommends adding at least two ground vias on both sides ground pad to ensure good RF grounding. Care must be taken in routing the path to the control pins to ensure minimal noise on line

Table 12 explains the filter routing guidelines.

Table 12. RF Switch Guidelines

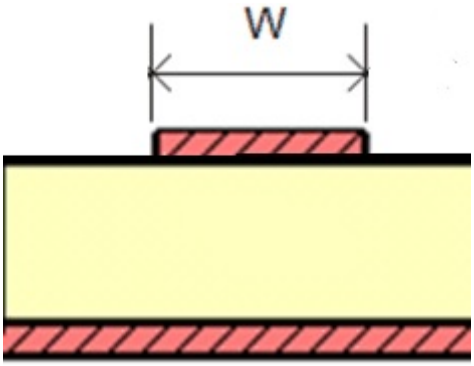
Sr No	Guidelines	Notes
1	Dc blocking is required on the RF ports on both the input and output	-
2	Exposed pad must be connected to GND for best performance	-

4.1.5 Transmission Line

The 3rd generation of the SimpleLink™ device, CC3235 and CC3135, employs both microstrip and CPW-G due to size and space constraints. The RF signal is routed from the QFN using microstrip transmission line.

Figure 11 shows the micro strip setup .

Figure 11. Microstrip Transmission Line



The RF signal from the device is routed to the antenna using a CPW-G structure. This structure offers the maximum isolation across the filter gap, and the best possible shielding to the RF lines. In addition to the ground on L1, placing GND vias along the line also provides additional shielding.

Figure 12 shows the CPW-G with via stitching.

Figure 12. Coplanar Waveguide (Cross Section) With GND and Via Stitching

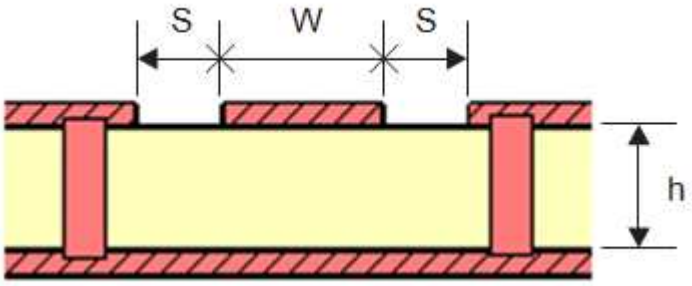
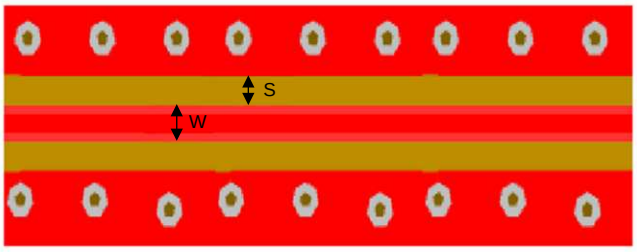


Figure 13 shows the top view of the CPW-G.

Figure 13. Coplanar Waveguide With GND (Top View)



For minimal reflections due to mismatch ensure there is no abrupt change in width of the trace. TI recommends tapering/filleting the trace to the component pads where possible. The RF trace bends must be made with gradual curves, avoid 90-degree bends and sharp corners. Impedance matching networks should also be implemented to ensure continuous 50 ohms impedance. See Section 4.1.6 for more information.

Figure 14. Filleting and Tapering of the Line

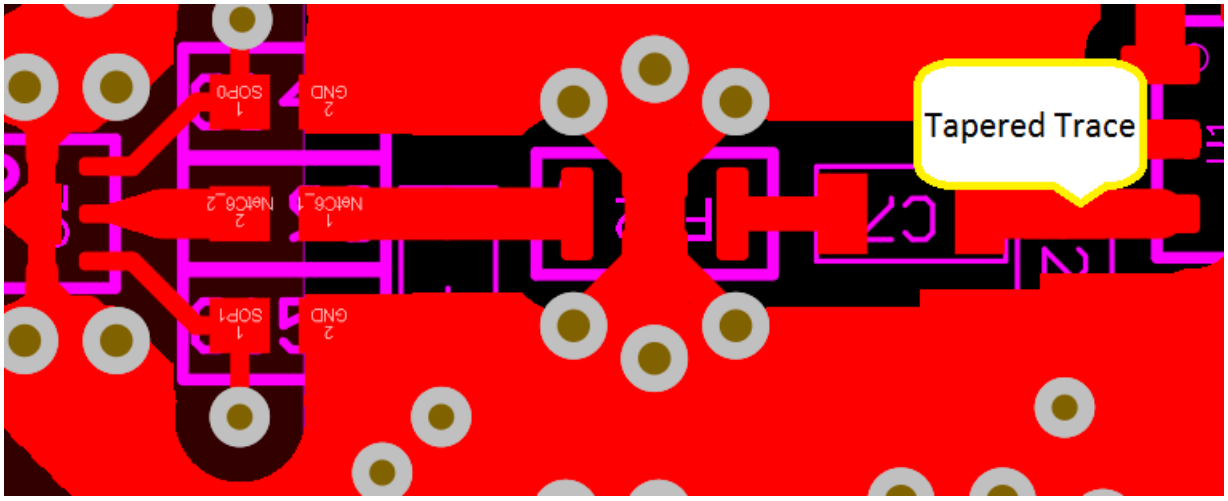


Table 13 provides the recommended values for the PCB.

Table 13. Recommended Values for the PCB

Parameter	Value	Units and Comments
W	16.7	mils
S	37.9	mils
H	9.3	mils
Ɛr (1)	3.9	Dielectric constant

(1) Ɛr is assumed to be of an FR-4 substrate.

4.1.6 Impedance Matching

Impedance matching is the process of equating the complex impedance of the transmission line to the load in order to minimize reflection in the line that results in power loss. Figure 16 shows the S-Parameter profile of the Gen 3 board when simulated using a perfect transmission with 50 ohms impedance.

S parameter is a good indication of the transmission and reflection loss on the line, it describes the frequency response of a multiport network. Transmission loss Sij (dB) indicates the response at port i due to signal at port j, a well designed RF path should show Sij closer to 0. Reflection loss Sii (Sjj) indicates the response at port i (j) due to signal at port i (j), it is a measure of the amount signal echoed back to the excited port. TI recommends a reflection loss less than -9.5dB at the frequency band of interest.

Figure 15. CC3235 ADS RF Simulation Configuration

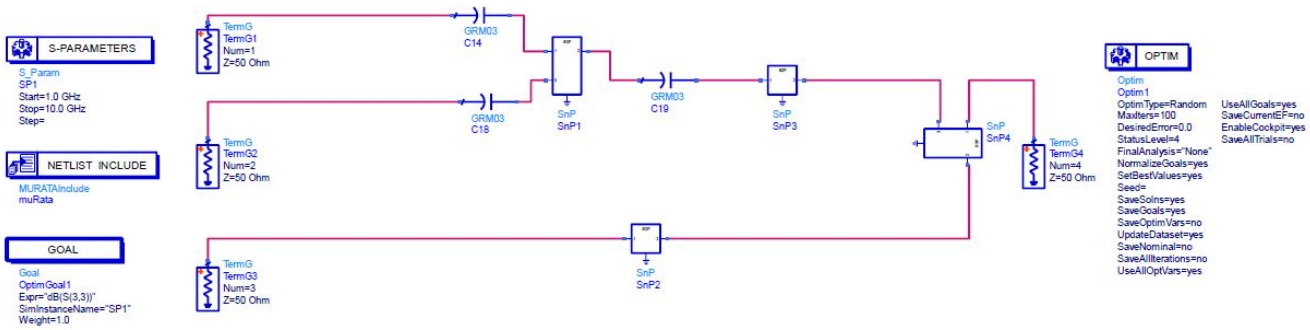
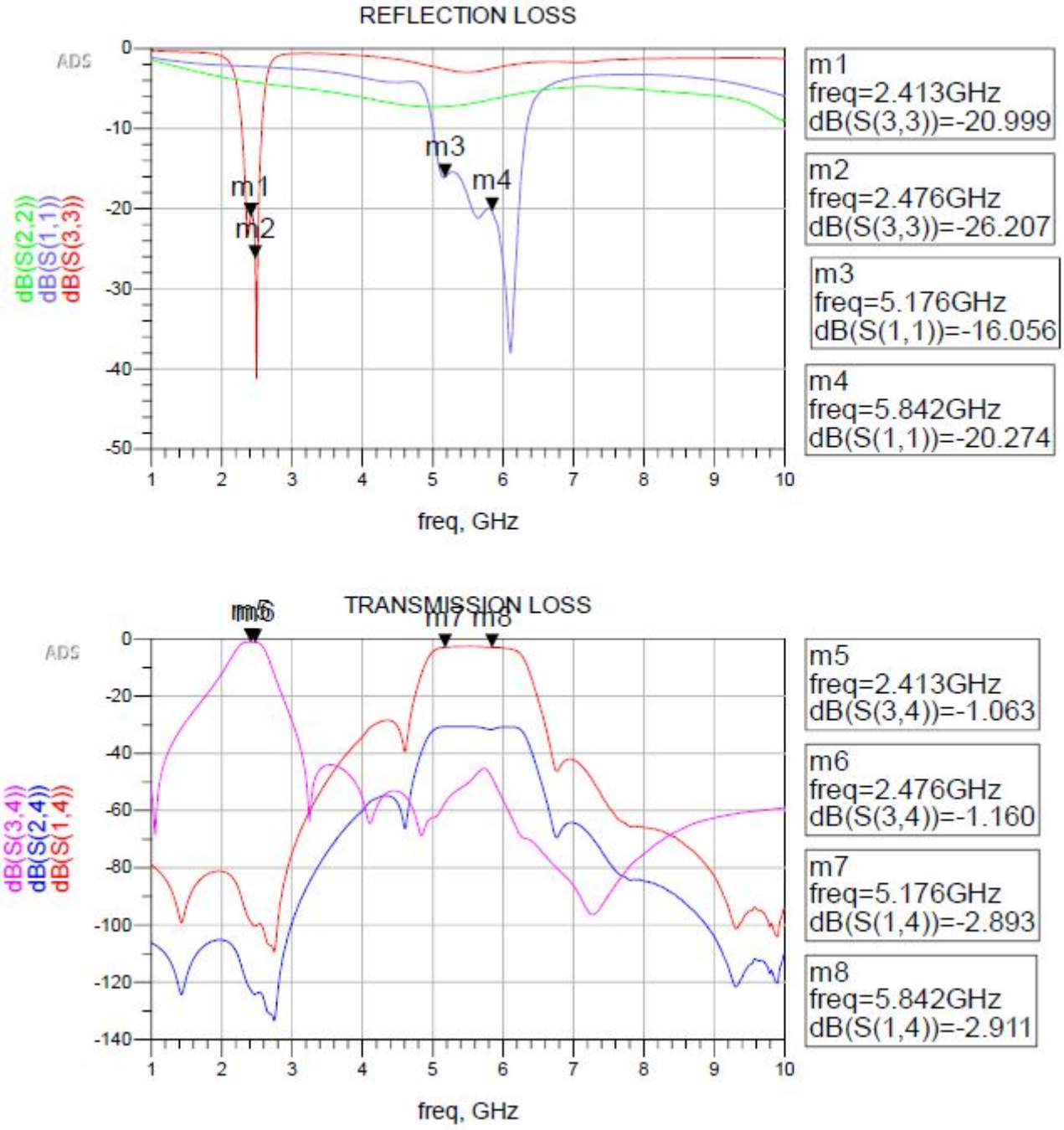
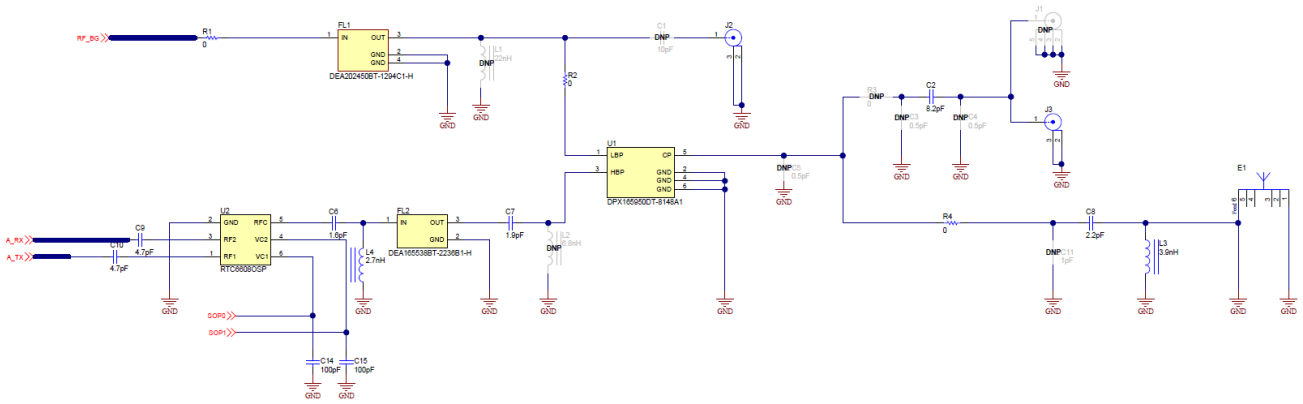


Figure 16. Reflections and Transmission Profiles Using Ideal 50 ohms Transmission Line



In practical applications, capacitive and inductive parasitics from other traces, non-ideal components, manufacturing defects and cascaded passive components results in deviation from the required 50 ohms impedance. TI recommends placing π / L matching network between the components, the network can be tuned post manufacture and unneeded components DNPed as shown in Figure 17 .

Figure 17. CC3235 RF Section Schematic



4.2 DC/DC Loop Considerations

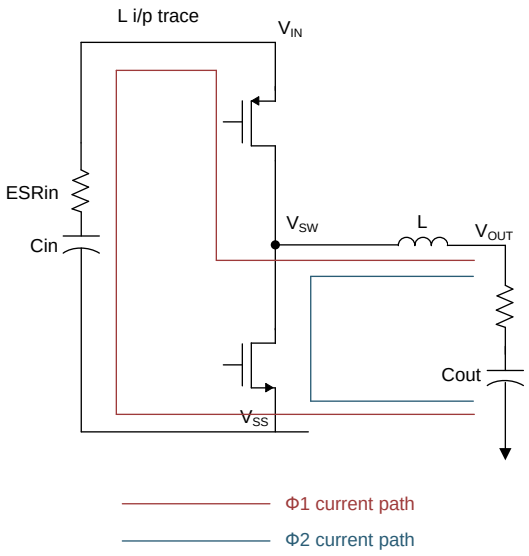
Three critical DC/DC converters must be considered for the CC31xx and CC32xx devices:

- Analog DC/DC converter
- PA DC/DC converter
- Digital DC/DC converter

Each converter requires an external inductor and capacitor that must be laid out with care. When laying out the power components, DC current loops are formed.

Figure 18 shows the two loops that are formed.

Figure 18. DC Loop Currents



The most important loop is shown in red. This loop travels from V_{SS}, through Cin, and finally through inductor L that is on the switching node (V_{SW}) before returning to V_{SS}. On this loop there is a lot of high-frequency switching current, and therefore it must be localized to the shortest possible loop, which in turn also minimizes the loop area. Reducing the loop area is important because the higher the loop area, the higher the radiated magnetic field, causing a major source of noise propagation on the board. In addition, the input capacitor must be as close as possible to the V_{IN} and V_{SW} pins. **Also, the ground node of the input capacitor must have its return path, the thermal pad of the device with its inductance of the trace minimized.** Figure 19 shows the critical trace inductances that must be minimized.

Figure 19. Critical Trace Inductances

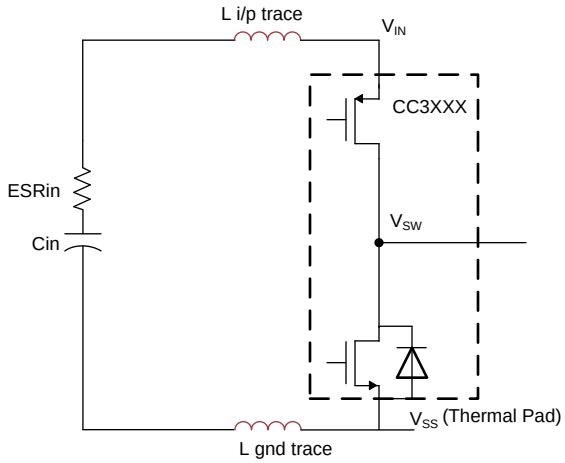


Table 14 describes the maximum allowable trace inductance for the three DC/DC converters.

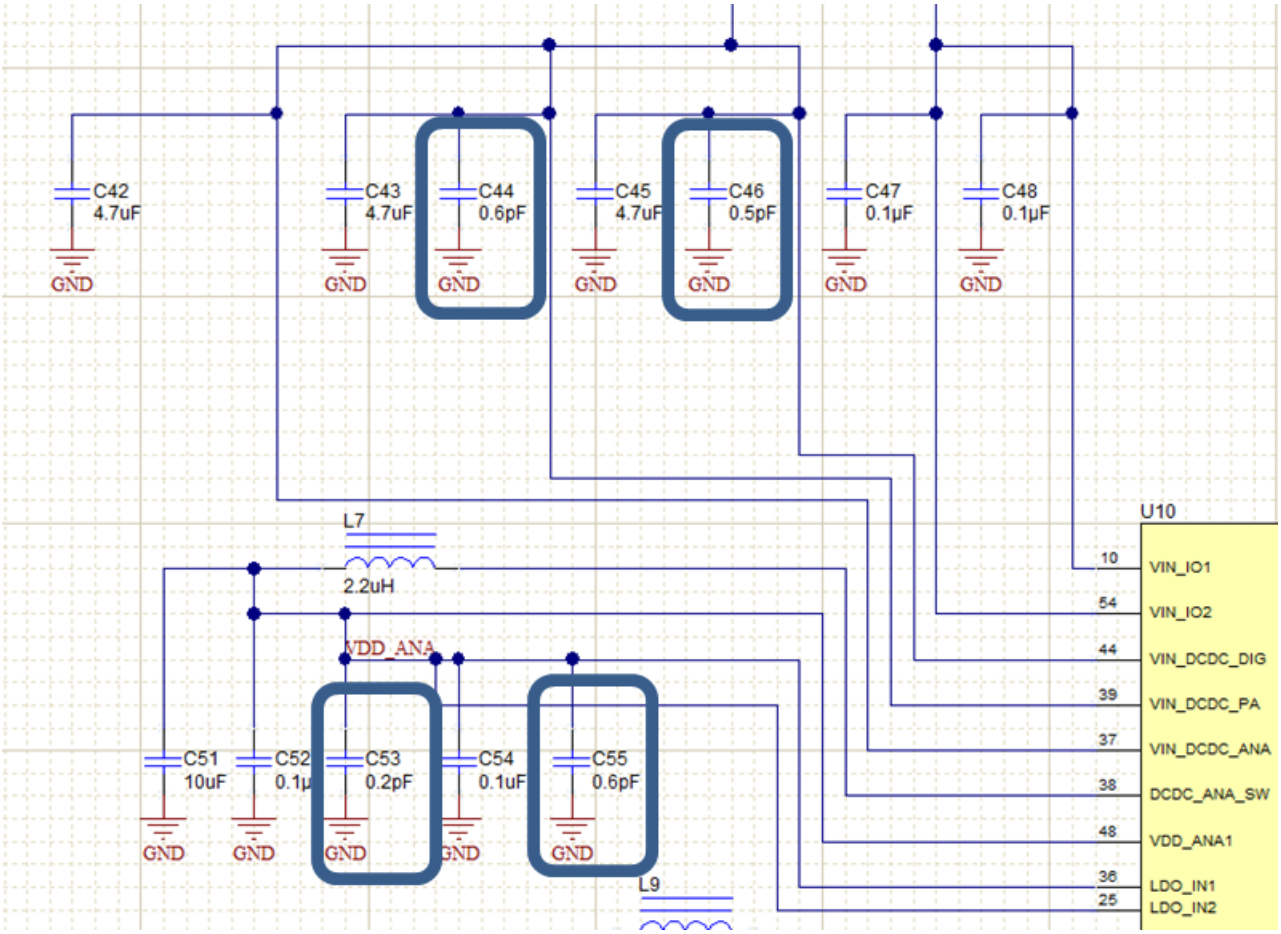
Table 14. Critical Board Trace Inductances

Device Pin Number	Pin Name	Maximum Trace Inductance Pin to Cin (L i/p trace)	Maximum Trace Inductance Cin Ground to V_{ss} (L GND trace)
37	VIN_DCDC_ANA	2 nH	0.5 nH
39	VIN_DCDC_PA	2 nH	0.5 nH
44	VIN_DCDC_DIG	3 nH	0.8 nH

4.2.1 Additional Filtering Considerations

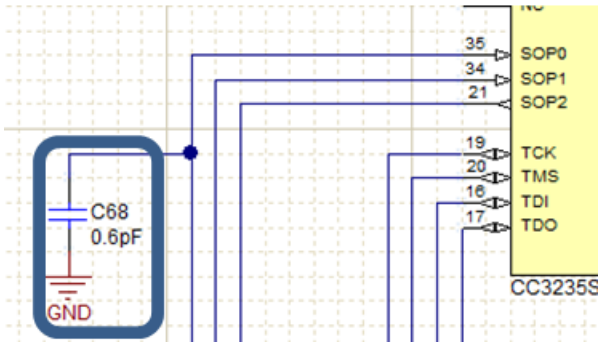
With the addition of 5 GHz, extra filtering capacitors need to be added to pin 36, 39, 44. Figure 20 shows the schematic for the extra caps.

Figure 20. 5-GHz DC/DC Filtering



A capacitor also needs to be added to the SOP0 line. Figure 21 shows the schematic of the SOP2 capacitor.

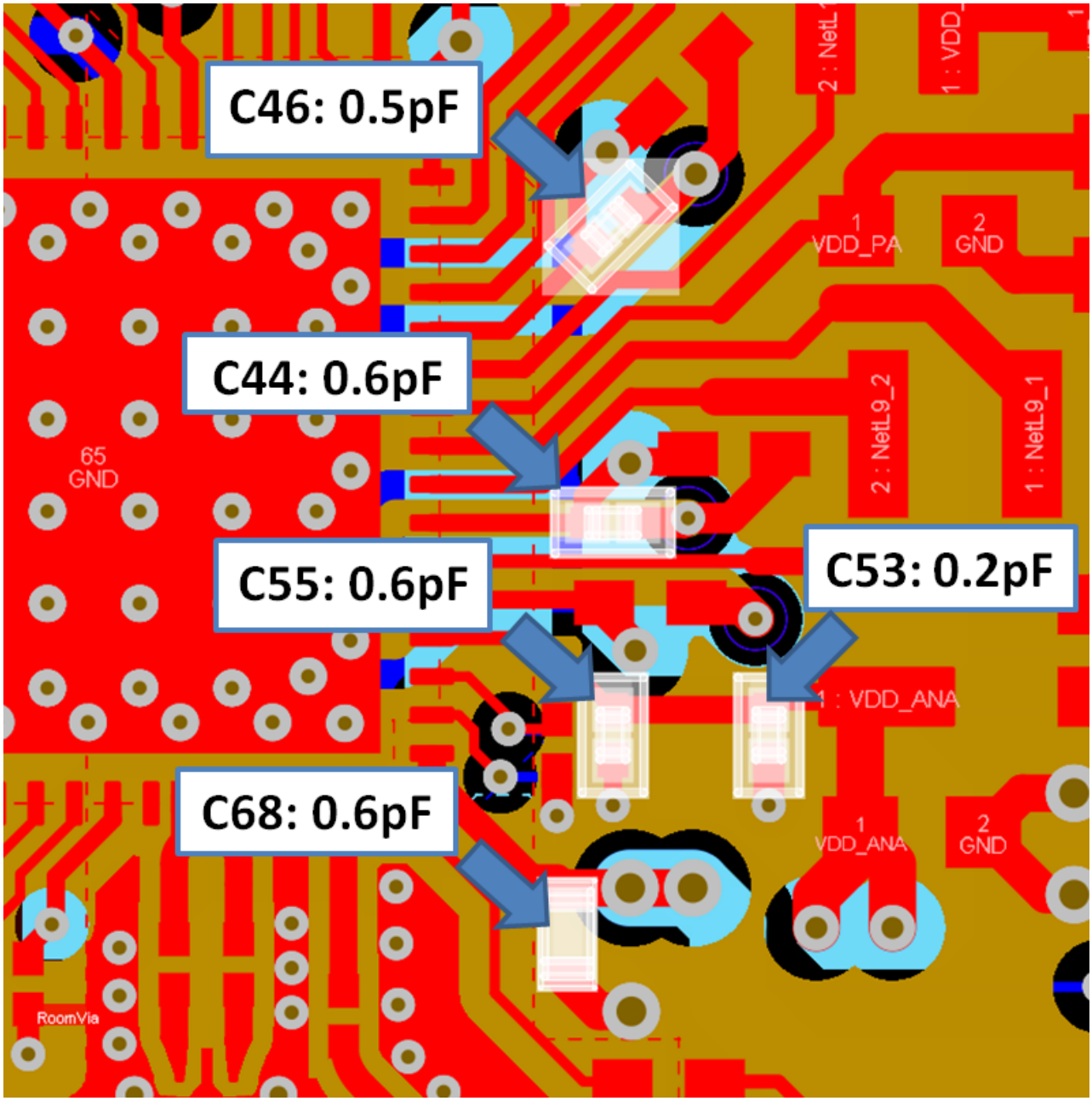
Figure 21. 5-GHz SOP0 Filtering



These Capacitor values were selected based on there parasitic effects at higher frequency. These components help filter spurs in the 7-10 GHz band. When selecting capacitors, use either the same capacitors or capacitors with similar parasitics.

Figure 22 shows the layout placement for these capacitors on the LAUNCHXL-CC3235x.

Figure 22. Layout for 5-GHz DC/DC and SOP2 Filtering



Reference Designator	Pin Name	Value	Size	Recommended Part Number
C44,C55,C68	Pin 36, 39, 35	0.6 pF	0201	GJM0335C1ER60BB01D
C46	Pin 44	0.5 pF	0201	GJM0335C1ER50BB01D
C53	Pin 36	0.2 pF	0201	GJM0335C1ER20BB01D

4.2.2 Inductors and Capacitors for DC/DC Converters

The components used in the power-management section of the design are critical to achieving the required performance. Table 15 shows the recommendations that should be chosen.

Table 15. Recommended Inductor and Capacitors

Reference Designator	Critical BOM	Value	Size	Current or Voltage Rating	Recommended Part Number	Description
L7	ANA DCDC OUT	2.2 µH	1008	1.2 A	LQM2MPN2R2NG0	Inductor 2.2 µH 20% 1008
L9	PA DCDC OUT	1 µH	1008	1.6 A	LQM2HPN1R0MG0L	Inductor 1 µH 20% 1008
L10	DIG DCDC OUT	2.2 µH	1008	1.2 A	LQM2MPN2R2NG0	Inductor 2.2 µH 20% 1008
L11	FLASH DCDC OUT	10 µH	1007	0.7 A	MLP2520S100MT0S1	Fixed Ind 10 µH 700MA 280 MOHM, ±20%
C42, C43, C45	Input supply decap	4.7 µF	0402	6.3 V	JMK105BC6475MV-F	Capacitor, Ceramic, 4.7 µF 6.3 V X6S 0402, ±20%
C62	ANA DCDC OUT	10 µF	0603	10 V	LMK107BC6106MA-T	Capacitor, Ceramic, 10 µF 6.3 V X6S 0603, ±20%
C59	DIG DCDC OUT	10 µF	0603	10 V	LMK107BC6106MA-T	Capacitor, Ceramic, 10 µF 6.3 V X6S 0603, ±20%
C62	FLASH DCDC OUT	10 µF	0603	10 V	LMK107BC6106MA-T	Capacitor, Ceramic, 10 µF 6.3 V X6S 0603, ±20%
C56, C57	PA DCDC OUT	22 µF	0603	4 V	GRM188C80G226ME15J	Capacitor, Ceramic, 22 µF 4 V X6S 0603

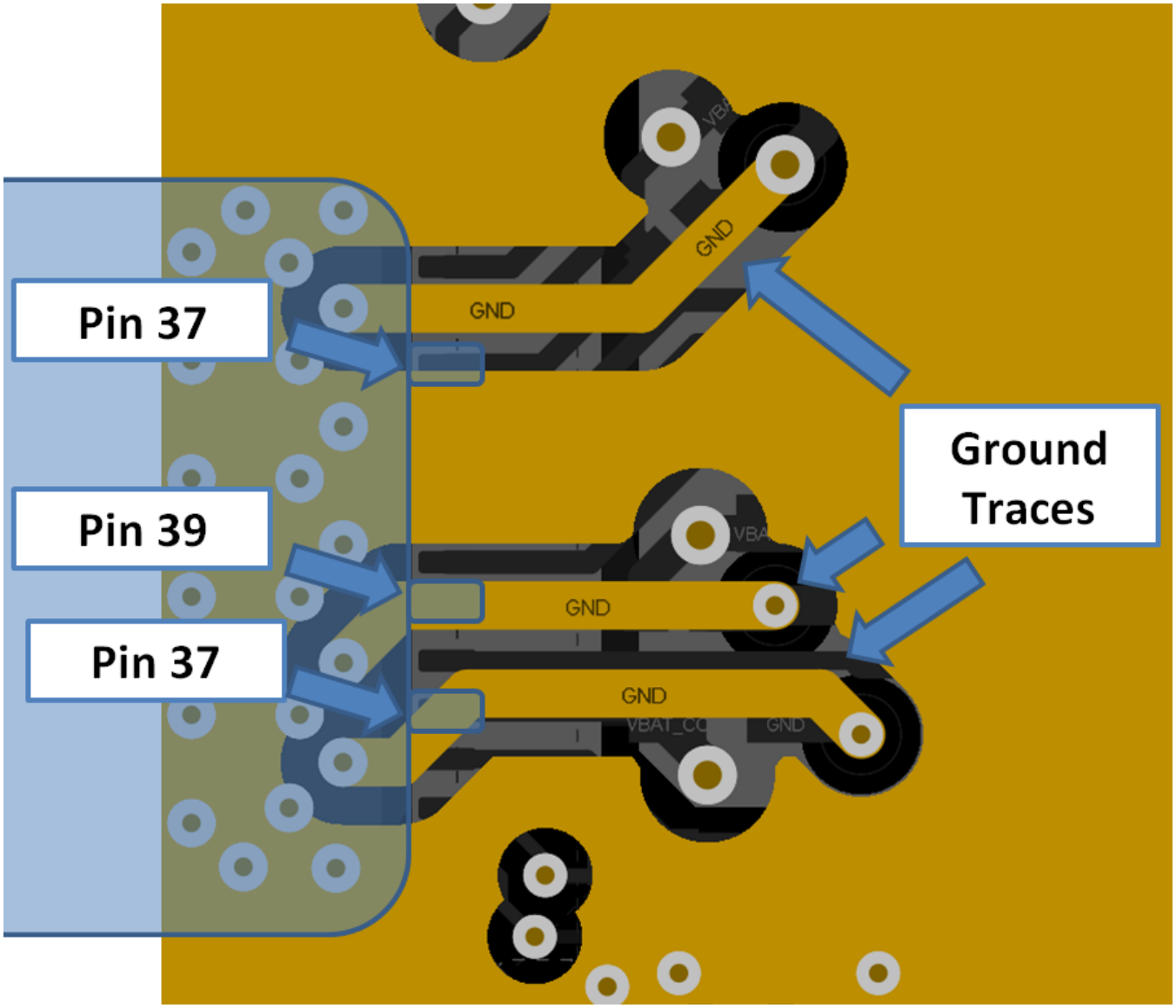
4.2.3 Design Considerations

The following design guidelines must be followed when laying out the CC31xx or CC32xx device:

- Route all of the input decoupling capacitors on L2 using thick traces, to isolate the RF ground from the noisy supply ground. This step is also required to meet the IEEE spectral mask specifications.
- Maintain the thickness of power traces to be greater than 12 mils. Take special consideration for power amplifier supply lines (pin 33, 40, 41, and 42) and all input supply pins (pin 37, 39, and 44).
- Ensure the shortest grounding loop for the PLL supply decoupling capacitor (pin 24).
- Place all decoupling capacitors as close as possible to the respective pins.
- Power budget: The CC32xx device can consume up to 450 mA for 3.3 V and 670 mA for 2.1 V for 24 ms during the calibration cycle.
- Ensure the power supply is designed to source this current without any issues. The complete calibration (TX and RX) can take up to 17 mJ of energy from the battery over a time of 24 ms.
- The CC3X20 device contains many high-current input pins. Ensure the trace feeding these pins is capable of handling the following currents:
  - PA DCDC input (pin 39) maximum 1 A
  - ANA DCDC input (pin 37) maximum 600 mA
  - DIG DCDC input (pin 44) maximum 500 mA
  - PA DCDC switching nodes (pins 40 and 41) maximum 1 A
  - PA DCDC output node (pin 42) maximum 1 A
  - ANA DCDC switching node (pin 38) maximum 600 mA
  - DIG DCDC switching node (pin 43) maximum 500 mA
  - PA supply (pin 33) maximum 500 mA

Figure 23 shows the ground routing for the input decoupling capacitors.

Figure 23. Ground Routing for the Input Decoupling Capacitors



The ground return for the input capacitors are routed on L2 to reduce the EMI and improve the spectral mask. This routing must be strictly followed because it is critical for the overall performance of the device.

4.3 Clock Section

4.3.1 32-kHz RTC Crystal

The 32.768-kHz crystal should be placed close to the QFN package. Ensure the load capacitance is tuned based on the board parasitic, so that the frequency tolerance is within ±150 ppm.

Table 16 describes the characteristics of the recommended 32K crystal.

Table 16. Characteristics of Recommended 32-kHz Crystal

Parameter	Specification
Nominal frequency	32.768 kHz
Tolerance with temperature and aging	±150 ppm
ESR	70 kΩ (maximum)

4.3.2 40-MHz Crystal

The 40-MHz crystal should be placed close to the QFN package. Ensure the load capacitance is tuned based on the board parasitic, so that the frequency tolerance is within ±10 ppm at room temperature. The total frequency accuracy for the crystal across parts, temperature, and with aging, should be ±20 ppm to meet the WLAN specifications. In addition, ensure no high-frequency lines are routed closer to the XTAL routing, to avoid any phase noise degradation. See CC31xx and CC32xx Frequency Tuning for frequency tuning information.

Table 17 describes the characteristics of the recommended 40-MHz crystal.

Table 17. Characteristics of Recommended 40-MHz Crystal

Parameter	Specification
Nominal frequency	40 MHz
Tolerance	±5 ppm
Load capacitance	8 pF
Temperature stability	±15 ppm (-40℃ - 95℃)
Aging	±3 (5-years)
ERS	40 Ω (maximum)

4.4 Digital Input and Output (I/O) Section

Route the serial peripheral interface (SPI) and universal asynchronous receiver/transmitter (UART) lines away from any RF traces, because these digital I/O lines are high-frequency lines, and can cause interference to the RF signal.

Keep the length of the high-speed lines as short as possible to avoid transmission line effects. Keep the line lower than 1/10 of the rise time of the signal, to ignore transmission line effects. This recommendation is required only if the traces cannot be kept short. Place the resistor at the source end, closer to the device driving the signal.

Add series-terminating resistors for each high-speed line (for example, SPI_CLK, SPI_DATA) to match the driver impedance to the line. Typical terminating resistor values range from 27 Ω to 36 Ω for a 50-Ω line impedance.

Route high-speed lines with a ground reference plane continuously below it to offer good impedance throughout, and help shield the trace against EMI.

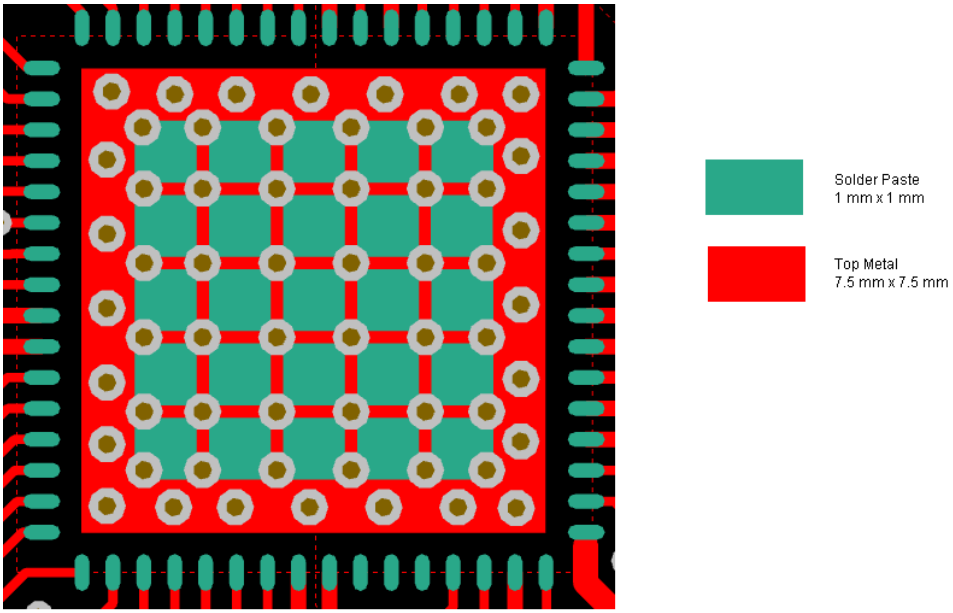
Avoid stubs on high-speed lines to minimize the reflections. If the line must be routed to multiple locations, use a separate line driver for each line.

If the lines are longer compared to the rise time, add series-terminating resistors near the driver for each high-speed line (for example, SPI_CLK, SPI_DATA) to match the driver impedance to the line. Typical terminating resistor values range from 27 Ω to 36 Ω for a 50-Ω line impedance.

4.5 QFN Ground

Figure 24 shows ground vias placed on the ground pad to ensure optimal thermal dissipation. The via drill size can be from 8 mils to 12 mils.

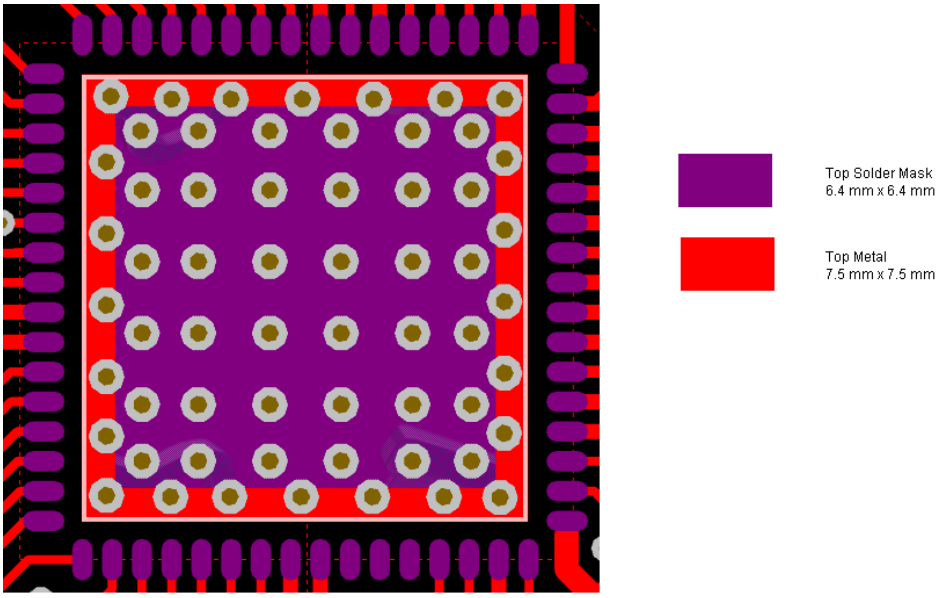
Figure 24. Ground Vias on Ground Pad



- Open the solder mask on the vias on the bottom side for better soldering yield. This process is called *via encroaching*.
- Figure 25 shows solder paste split into smaller blocks to avoid component lifting while soldering or reflow.
- Solder paste should cover at least 75% of the ground tab of the QFN.
- The metal layers on L1 under the device are expanded beyond the thermal pad dimensions. This step specifically improves the spectral mask and EVM performance. Also, the additional vias placed along the edge of the package help suppress EMI emissions.
- Although the metal on L1 below the QFN is oversized, the solder mask remains smaller to fit the thermal pad dimensions on the device.

For the exact dimensions of the metal pad, solder mask, and the paste layers, see the CC3135 SimpleLink™ Wi-Fi® BoosterPack™ Design Files and the CC3235S/CC3235SF SimpleLink™ Wi-Fi® LaunchPad™ Design Files.

Figure 25. Top Metal and Solder Mask (Reduced Mask Area)



5 Summary

This document presented an introduction to designing a 4-layer PCB for the CC3135 and CC3235 SimpleLink™ Wi-Fi® devices, easy to lay out QFN packaged family of devices. In addition to the recommendations presented here, see the CC3135 SimpleLink™ Wi-Fi® BoosterPack™ Design Files and the CC3235S/CC3235SF SimpleLink™ Wi-Fi® LaunchPad™ Design Files.

6 Additional References

1. Texas Instruments, CC31xx and CC32xx main landing page
2. *CC3135 SimpleLink™ Wi-Fi®, Dual-Band Network Processor, Solution for MCU Applications Data Sheet*
3. *CC3235S and CC3235SF SimpleLink™ Wi-Fi®, Dual-Band, Single-Chip Solution Data Sheet*

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