TEXAS INSTRUMENTS

Signal Switch

Including Digital/Analog/Bilateral Switches and Voltage Clamps

Data Book

Introducing Three New Bus-Switch Families

- *CB3Q High-Bandwidth Bus Switch*
- *CB3T Low-Voltage Translator Bus Switch*
- *CBT-C Bus Switch With –2-V Undershoot Protection*

January 2004 *Logic Products*

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0104

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INTRODUCTION

The Texas Instruments signal-switch portfolio has been expanded, with the introduction of the CB3Q, CB3T, and CBT-C bus-switch families. These new FET bus switches provide high-performance, low-power replacements for standard bus-interface devices when signal buffering (current drive) is not required. The CB3Q, CB3T, and CBT-C bus-switch families optimize next-generation datacom, networking, computing, portable communications, and consumer electronics designs by supporting both digital and analog applications, including PCI interface, USB interface, memory interleaving, bus isolation, and low-distortion signal gating (see www.ti.com/signalswitches).

CB3Q: 2.5-V/3.3-V Low-Voltage High-Bandwidth Bus-Switch Family

CB3Q is a high-bandwidth (up to 500 MHz) FET bus-switch family utilizing a charge pump to elevate the gate voltage of the pass transistor, providing low and flat ON-state resistance (r_{on}) characteristics. The low and flat ON-state resistance allows minimal propagation delay and supports rail-to-rail I/O (RRIO) switching on the data input/output (I/O) ports. The CB3Q family also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the CB3Q family provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

CB3T: 2.5-V/3.3-V Low-Voltage Translator Bus-Switch Family

CB3T is a high-speed TTL-compatible FET bus-switch family with low ON-state resistance (r_{on}), allowing minimal propagation delay. The CB3T family fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The CB3T family supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels. This voltage translation feature allows the CB3T family to provide a high-performance interface between components (memory, processors, logic ASICs, I/O peripherals, etc.) common in mixed 2.5-V to 5-V system environments. Specifically designed to support today's portable computing and communications applications, the CB3T family provides a high-performance low-power interface solution ideally suited for low-power portable equipment.

CBT-C: 5-V Bus-Switch Family With –2-V Undershoot Protection

CBT-C is a high-speed TTL-compatible FET bus-switch family with low ON-state resistance (r_{on}), allowing minimal propagation delay. The new CBT-C family offers numerous enhancements over the original CBT family, including –2-V undershoot protection, faster enable/disable times, and an I_{off} feature for partial-power-down mode operation. The improved undershoot characteristics of the CBT-C family are particularly important in system environments where signal reflections and undershoot are common. Without such protection, an undershoot event could cause a switch in the OFF state to be turned ON, creating bus contention and possible data corruption. The active undershoot-protection circuitry on the A and B ports of the CBT-C family provides protection for undershoots up to –2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

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Application Report
SZZA036B - May 2003

Understanding and Interpreting Standard-Logic Data Sheets

Stephen M. Nolan and Jose M. Soltero

Standard Linear & Logic

ABSTRACT

Texas Instruments (TI) standard-logic products data sheets include descriptions of functionality and electrical specifications for the devices. Each specification includes acronyms, numerical limits, and test conditions that may be foreign to the user. The proper understanding and interpretation of the direct, and sometimes implied, meanings of these specifications is essential to correct product selection and associated circuit design. This application report explains each data-sheet parameter in detail, how it affects the device, and, more important, how it impacts the application. This will enable component and system-design engineers to derive the maximum benefit from TI logic devices.

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Introduction

To assist component and system-design engineers in selecting Texas Instruments (TI) standard-logic products, this application report is a synopsis of the information available from a typical TI data sheet. Information includes a brief description of terms, definitions, and testing procedures currently used for commercial and military specifications. Symbols, terms, and definitions generally are in accordance with those currently agreed upon by the JEDEC Solid State Technology Association for use in the USA and by the International Electrotechnical Commission (IEC) for international use. This application report is organized into five main sections:

1. *Introduction*
2. *Top-Level Look at the TI Data Sheet.* Overall layout and component parts of a data sheet are explained.
3. *Dissecting the TI Logic Data Sheet*. JEDEC definition, the TI definition, an explanation, and, where possible, helpful hints are presented for each specification term commonly found in TI logic data sheets.
4. *Logic Compatibility.* Information in TI logic data sheets for determining the interface compatibility between different logic families is explained.
5. End matter, including the *Conclusion*, *Acknowledgments*, and *References* sections.

Top-Level Look at the TI Logic Data Sheet

The TI logic data sheet presents pertinent technical information for a particular device and is organized for quick access. This application report dissects a typical TI logic data sheet and describes the organization of all data sheets.

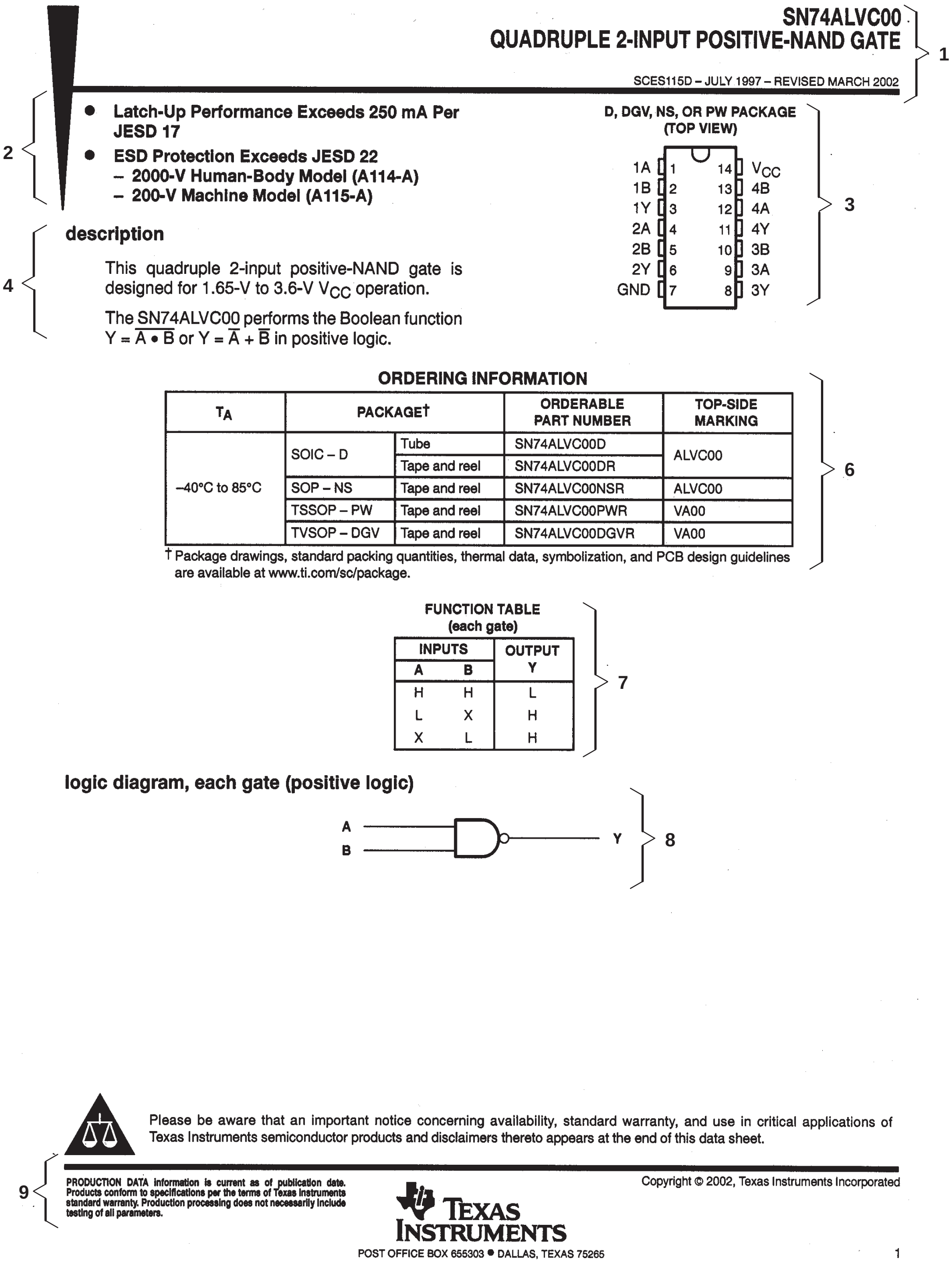
Typically, there are ten sections in TI logic data sheets:

1. Summary device description
2. Absolute maximum ratings
3. Recommended operating conditions
4. Electrical characteristics
5. Live-insertion specifications
6. Timing requirements
7. Switching characteristics
8. Noise characteristics
9. Operating characteristics
10. Parameter measurement information

Summary Device Description

The first section of a data sheet contains all of the general information about a device (see Figure 1). This information includes:

1. Title, literature number, and dates of origination and revision, as applicable
2. Description of the main features and benefits of the device, also known as features bullets
3. Package options and pinouts
4. Description
5. BGA packaging top-view illustration and terminal assignments table, if applicable (not illustrated in Figure 1)
6. Ordering information
7. Function table
8. Logic diagram (positive logic)
9. Product-development-stage note



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SN74ALVC00
QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCES115D – JULY 1997 – REVISED MARCH 2002

- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**

D, DGV, NS, OR PW PACKAGE
(TOP VIEW)

1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 V_{CC}
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y

description

This quadruple 2-input positive-NAND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVC00 performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tube	SN74ALVC00D	ALVC00
		Tape and reel	SN74ALVC00DR	
	SOP – NS	Tape and reel	SN74ALVC00NSR	ALVC00
	TSSOP – PW	Tape and reel	SN74ALVC00PWR	VA00
	TVSOP – DGV	Tape and reel	SN74ALVC00DGVR	VA00

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic diagram, each gate (positive logic)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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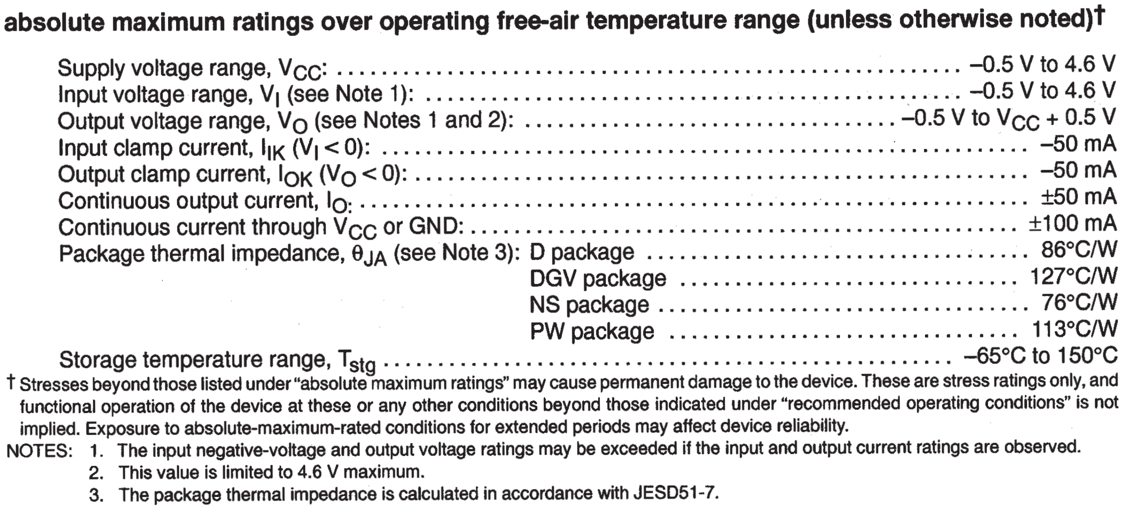
Figure 1. Example of Summary Device Description

Absolute Maximum Ratings

The *absolute maximum ratings* section (Figure 2) specifies the stress levels that, if exceeded, may cause permanent damage to the device. However, these are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Also, exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

As Figure 2 indicates, there are two absolute maximums that may be exceeded under certain conditions. The input and output voltage ratings, V_I and V_O, may be exceeded if the input and output maximum clamp-current ratings, I_{IK} and I_{OK}, are observed.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}:		–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1):		–0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2):		–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$):		–50 mA
Output clamp current, I_{OK} ($V_O < 0$):		–50 mA
Continuous output current, I_O:		±50 mA
Continuous current through V_{CC} or GND:		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	D package	86°C/W
	DGV package	127°C/W
	NS package	76°C/W
	PW package	113°C/W
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD51-7.

Figure 2. Example of Absolute Maximum Ratings Section

Helpful Hint:

All currents are defined with respect to conventional current flow into the respective terminal of the integrated circuit. This means that any current that flows out of the respective terminal is considered to be a negative quantity.

All limits are given according to the absolute-magnitude convention, with a few exceptions. In this convention, maximum refers to the greater magnitude limit of a range of like-signed values; if the range includes both positive and negative values, both limit values are maximums. Minimum refers to the smaller magnitude limit of a range of like-signed values; if the range includes both positive and negative values, the minimum is implicitly zero. The most common exceptions to the use of the absolute magnitude convention are temperature and logic levels. Here, zero does not represent the least-possible quantity, so the algebraic convention is commonly accepted. In this case, maximum refers to the most-positive value.

Recommended Operating Conditions

The *recommended operating conditions* section of the data sheet sets the conditions over which Texas Instruments specifies device operation (see Figure 3). These are the conditions that the application circuit should provide to the device for it to function as intended. The limits for items that appear in this section are used as test conditions for the limits that appear in the *electrical characteristics*, *timing requirements*, *switching characteristics*, and *operating conditions* sections.

recommended operating conditions (see Note 4)

			SN54LVTH16646		SN74LVTH16646		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

PRODUCT PREVIEW

NOTE 1: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

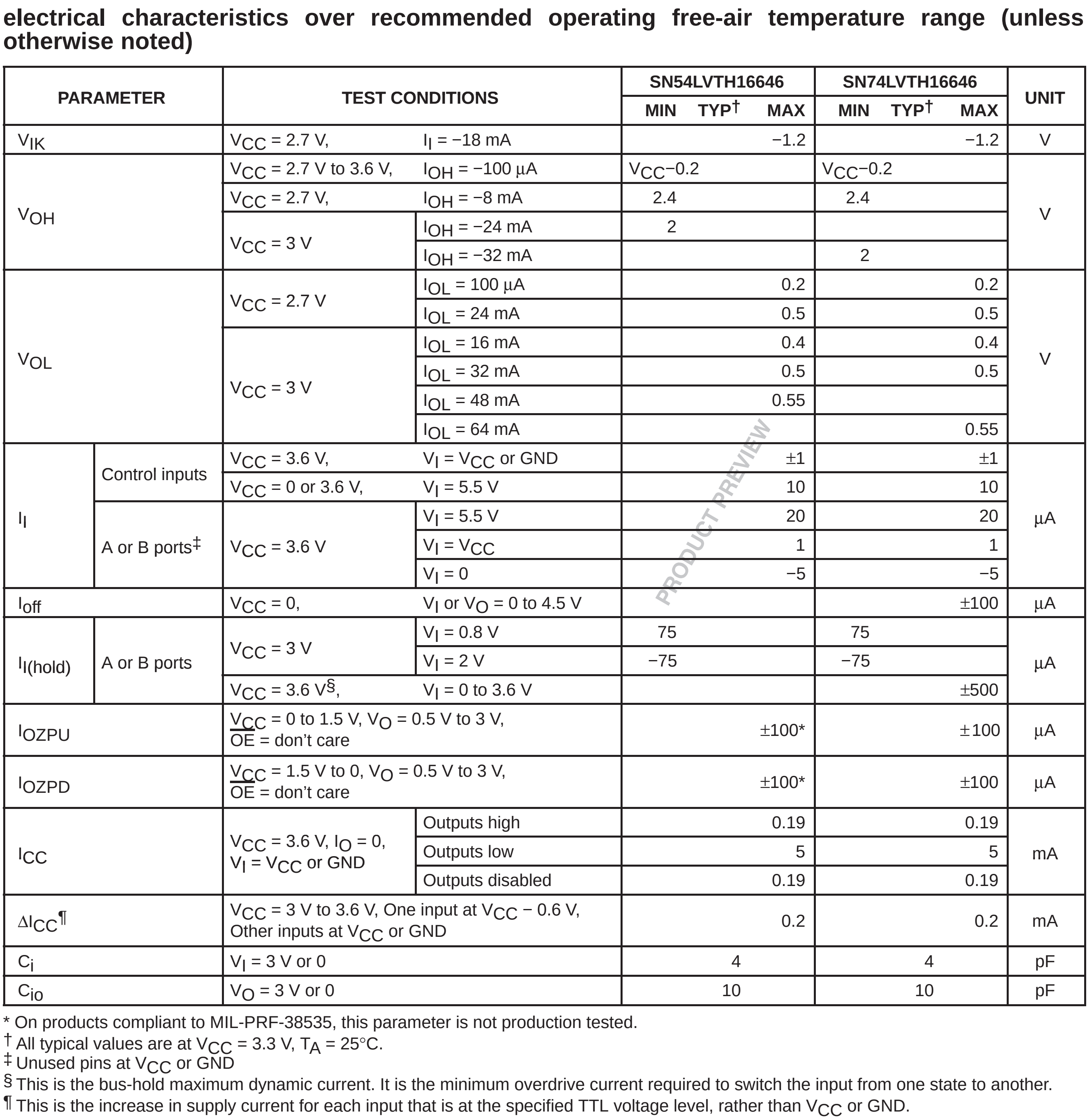
Figure 3. Example Recommended Operating Conditions Section

Electrical Characteristics

The *electrical characteristics over recommended free-air temperature range* table, also known in the industry as the dc table, provides the specified electrical-characteristic limits of the device when tested under the conditions in the recommended operating conditions table, as given specifically for each parameter (see Figure 4).

Helpful Hint:

Although some parameters, such as C_i and C_{io}, can be tested with an ac signal, sometimes the electrical characteristics table is called the dc section.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16646			SN74LVTH16646			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 2.7 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 2.7 V to 3.6 V,	I_{OH} = −100 µA	V_{CC}−0.2			V_{CC}−0.2			V
		V_{CC} = 2.7 V,	I_{OH} = −8 mA	2.4			2.4			
		V_{CC} = 3 V	I_{OH} = −24 mA	2						
			I_{OH} = −32 mA				2			
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 24 mA			0.5			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	µA
		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	
	A or B ports‡	V_{CC} = 3.6 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			1			1	
			V_I = 0			−5			−5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
$I_{I(hold)}$	A or B ports	V_{CC} = 3 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	−75			−75			
		V_{CC} = 3.6 V§,	V_I = 0 to 3.6 V						±500	
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100*			±100	µA
I_{OZPD}		V_{CC} = 1.5 V to 0, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100*			±100	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}¶		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		V_I = 3 V or 0			4			4		pF
C_{io}		V_O = 3 V or 0			10			10		pF

PRODUCT PREVIEW

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ Unused pins at V_{CC} or GND

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Figure 4. Example Electrical-Characteristics Section

Live-Insertion Specifications

The *live-insertion* section of the data sheet provides information about the parameters needed for true live insertion. These parameters include I_{off}, I_{OZPU}, I_{OZPD}, and BIAS V_{CC} for precharging purposes. An example of a typical live-insertion section is shown in Figure 5.

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	−1		µA

Figure 5. Example Live-Insertion Section

Timing Requirements

The *timing requirements* section of the data sheet is similar to the *recommended operating conditions* section (see Figure 6). These are timings that the application circuit should provide to the device for it to function as intended. This section addresses the timing relationships between transitions of one or more input signals that are necessary to ensure device functionality and applies only to sequential-logic devices (e.g., flip-flops, latches, and registers).

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

			SN54LVTH16646				SN74LVTH16646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150		150		150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	Data high	1.2		1.5		1.2		1.5		ns
		Data low	2		2.8		2		2.8		
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	Data high	0.5		0		0.5		0		ns
		Data low	0.5		0.5		0.5		0.5		

PRODUCT PREVIEW

Figure 6. Example Timing-Requirements Section

Switching Characteristics

The *switching characteristics* section of the data sheet, also known in the industry as the ac table, includes those parameters that specify how fast the outputs will respond to signal changes at the inputs under specified conditions of supply voltage, temperature, and load (see Figure 7).

Helpful Hint:

The switching characteristics table sometimes is called the ac section, and should not be confused with the ac small-signal performance because switching characteristics describe the large-signal transient response of the circuit.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16646				SN74LVTH16646					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}			150		150		150			150		MHz
t_{PLH}	CLKBA or CLKAB	A or B	1.3	4.5		5	1.3	2.8	4.2		4.7	ns
t_{PHL}			1.3	4.5		5	1.3	2.8	4.2		4.7	
t_{PLH}	A or B	B or A	1	3.6		4.1	1	2.4	3.4		3.9	ns
t_{PHL}			1	3.6		4.1	1	2.1	3.4		3.9	
t_{PLH}	SBA or SAB‡	A or B	1	4.7		5.6	1	2.8	4.5		5.4	ns
t_{PHL}			1	4.7		5.6	1	3	4.5		5.4	
t_{PZH}	$\overline{OE}$	A or B	1	4.5		5.4	1	2.5	4.3		5.2	ns
t_{PZL}			1	4.5		5.4	1	2.6	4.3		5.2	
t_{PHZ}	$\overline{OE}$	A or B	2	5.8		6.3	2	4	5.6		6.1	ns
t_{PLZ}			2	5.6		6.3	2	3.6	5.4		6.1	
t_{PZH}	DIR	A or B	1	4.6		5.5	1	3	4.4		5.3	ns
t_{PZL}			1	4.6		5.5	1	3	4.4		5.3	
t_{PHZ}	DIR	A or B	1.5	6		7.1	1.5	3.9	5.7		6.8	ns
t_{PLZ}			1.5	5.5		6	1.5	3.6	5.2		5.7	

PRODUCT PREVIEW

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

Figure 7. Example of Switching-Characteristics Section

Noise Characteristics

This section indicates a device's noise performance due to power-rail and ground-rail bounce associated with the high peak currents during dynamic switching (see Figure 8).

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHCT16541			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.3		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 2: Characteristics are for surface-mount packages only.

Figure 8. Example Noise-Characteristics Section

Operating Characteristics

The *operating characteristics* section of the data sheet includes the parameter that specifies the power-dissipation capacitance (C_{pd}) in a CMOS device (see Figure 9). For additional information on how C_{pd} is measured and used to calculate total CMOS-device power consumption in the application, refer to the TI application report, *CMOS Power Consumption and C_{pd} Calculation*, literature number SCAA035.

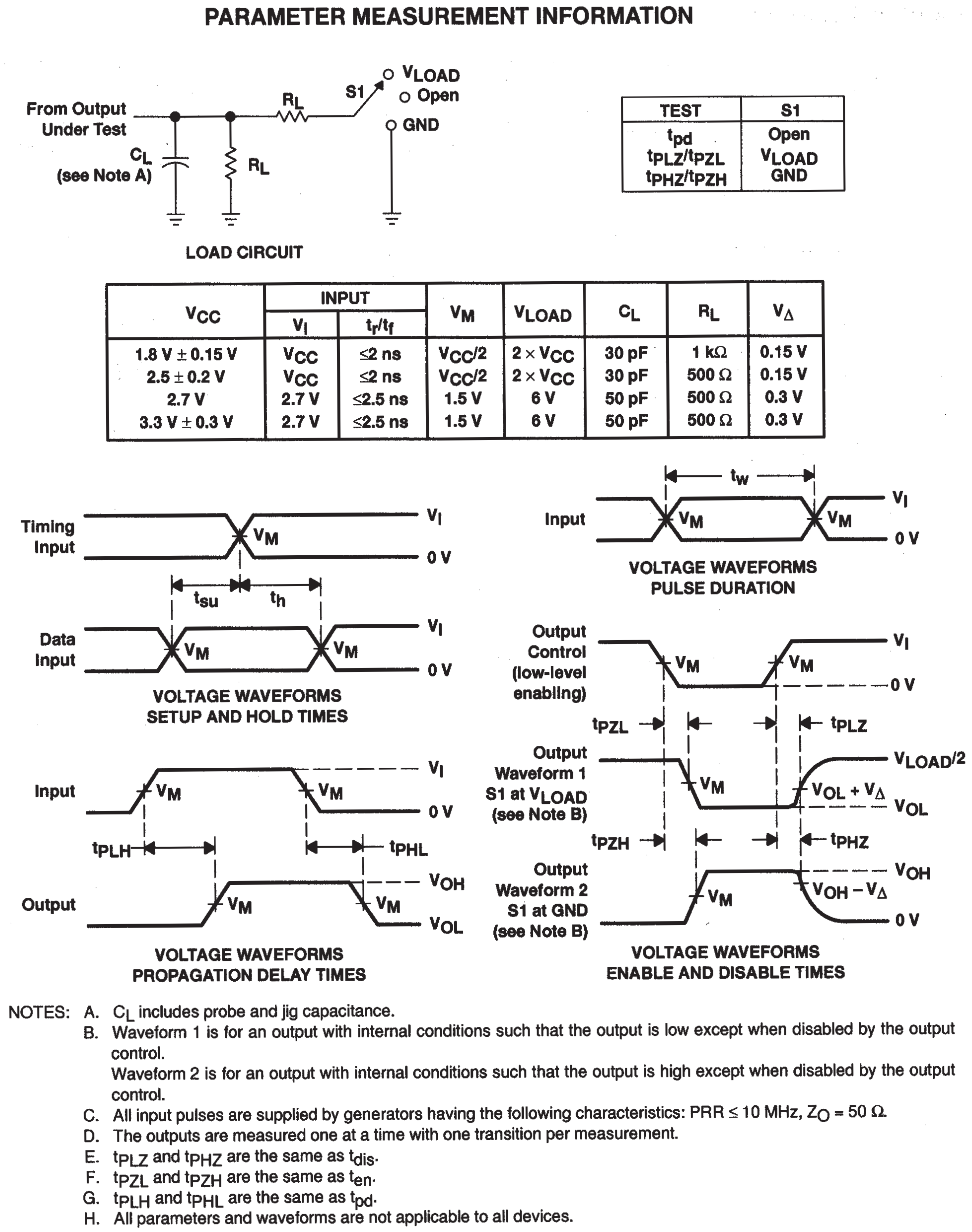
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per gate	C_L = 0, f = 10 MHz	20	21	23	pF

Figure 9. Example of Operating-Characteristics Section

Parameter Measurement Information

The *parameter measurement information* section of the data sheet illustrates the test loads and waveforms that are used when testing the device (see Figure 10).



PARAMETER MEASUREMENT INFORMATION

From Output Under Test
CL (see Note A)
RL
RL
S1
VLOAD
Open
GND
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V

Timing Input
VI
VM
0 V
tsu
th
Data Input
VM
VM
VI
0 V
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES
Input
tw
VM
VM
VI
0 V
VOLTAGE WAVEFORMS PULSE DURATION
Input
VM
VM
VI
0 V
tPLH
tPHL
Output
VM
VM
VOH
VOL
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES
Output Control (low-level enabling)
VM
VM
VI
0 V
tPZL
tPLZ
Output Waveform 1 S1 at VLOAD (see Note B)
VM
VLOAD/2
VOL + VΔ
VOL
tPZH
tPHZ
Output Waveform 2 S1 at GND (see Note B)
VM
VOH
VOH − VΔ
0 V
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
  Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 10. Example Parameter Measurement Information Section

Dissecting the TI Logic Data Sheet

In the following paragraphs, the TI logic data sheet is dissected, and every section and specification is explained in detail.

Summary Device Description

Title, Literature Number, and Dates of Origination and Revision

The device number and title appear at the top of every page. The device number is the number of the parent device. The fully qualified part number for a specific device can be found in the *Orderable Part Number* table. Figure 11 is a chart to help decode information in the TI logic-device part number.

The literature number is a unique identifier used by TI to identify, store, and retrieve a data sheet in internal files.

The month and year of origination is the first date of publication of the data sheet. If a data sheet is modified, the revision date (month and year) is added. If there are multiple revisions, only the latest revision date appears.

Example:	**SN**	**74**	**LVC**		**1G**		**66**		**DBV**	**R**
	1	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*

1 Standard Prefix

Examples: SN − Standard Prefix
SNJ − Conforms to MIL-PRF-38535 (QML)

2 Temperature Range

Examples: 54 − Military
74 − Commercial

3 Family

Examples: Blank = Transistor-Transistor Logic (TTL)
ABT − Advanced BiCMOS Technology
ABTE/ETL − Advanced BiCMOS Technology/ Enhanced Transceiver Logic
AC/ACT − Advanced CMOS Logic
AHC/AHCT − Advanced High-Speed CMOS Logic
ALB − Advanced Low-Voltage BiCMOS
ALS − Advanced Low-Power Schottky Logic
ALVC − Advanced Low-Voltage CMOS Technology
ALVT − Advanced Low-Voltage BiCMOS Technology
AS − Advanced Schottky Logic
AUC − Advanced Ultra Low-Voltage CMOS Logic
AVC − Advanced Very Low-Voltage CMOS Logic
BCT − BiCMOS Bus-Interface Technology
CBT − Crossbar Technology
CBTLV − Low-Voltage Crossbar Technology
CD4000 − CMOS B-Series Integrated Circuits
F − F Logic
FB − Backplane Transceiver Logic/Futurebus+
FCT − Fast CMOS TTL Logic
GTL − Gunning Transceiver Logic
GTLP − Gunning Transceiver Logic Plus
HC/HCT − High-Speed CMOS Logic
HSTL − High-Speed Transceiver Logic
LS − Low-Power Schottky Logic
LV − Low-Voltage CMOS Technology
LVC − Low-Voltage CMOS Technology
LVT − Low-Voltage BiCMOS Technology
PCA/PCF − I^{2}C Inter-Integrated Circuit Applications
S − Schottky Logic
SSTL/SSTV − Stub Series-Terminated Logic
TVC − Translation Voltage Clamp Logic
VME − VERSAmodule Eurocard Bus Technology

4 Special Features

Examples: Blank = No Special Features
C − Configurable V_{CC} (LVCC)
D − Level-Shifting Diode (CBTD)
H − Bus Hold (ALVCH)
K − Undershoot-Protection Circuitry (CBTK)
R − Damping Resistor on Inputs/Outputs (LVCR)
S − Schottky Clamping Diode (CBTS)
Z − Power-Up 3-State (LVCZ)

5 Bit Width

Examples: Blank = Gates, MSI, and Octals
1G − Single Gate
2G − Dual Gate
3G − Triple Gate
8 − Octal IEEE 1149.1 (JTAG)
16 − Widebus™ (16, 18, and 20 bit)
18 − Widebus IEEE 1149.1 (JTAG)
32 − Widebus+™ (32 and 36 bit)

6 Options

Examples: Blank = No Options
2 − Series Damping Resistor on Outputs
4 − Level Shifter
25 − 25-Ω Line Driver

7 Function

Examples: 244 − Noninverting Buffer/Driver
374 − D-Type Flip-Flop
573 − D-Type Transparent Latch
640 − Inverting Transceiver

8 Device Revision

Examples: Blank = No Revision
Letter Designator A−Z

9 Packages

Commercial: D, DW − Small-Outline Integrated Circuit (SOIC)
DB, DBQ, DCT, DL − Shrink Small-Outline Package (SSOP)
DBB, DGV − Thin Very Small-Outline Package (TVSOP)
DBQ − Quarter-Size Small-Outline Package (QSOP)
DBV, DCK, DCY, PK − Small-Outline Transistor (SOT)
DCU − Very Thin Shrink Small-Outline Package (VSSOP)
DGG, PW − Thin Shrink Small-Outline Package (TSSOP)
FN − Plastic Leaded Chip Carrier (PLCC)
GGM, GKE, GKF, ZKE, ZKF − MicroStar BGA™ Low-Profile Fine-Pitch Ball Grid Array (LFBGA)
GQL, GQN, ZQL, ZQN − MicroStar Jr.™ Very-Thin-Profile Fine-Pitch Ball Grid Array (VFBGA)
N, NT, P − Plastic Dual-In-Line Package (PDIP)
NS, PS − Small-Outline Package (SOP)
PAG, PAH, PCA, PCB, PM, PN, PZ − Thin Quad Flatpack (TQFP)
PH, PQ, RC − Quad Flatpack (QFP)
PZA − Low-Profile Quad Flatpack (LQFP)
RGY − Quad Flatpack No Lead (QFN)
YEA, YZA − NanoStar™ and NanoFree™ Die-Size Ball Grid Array (DSBGA[†])

Military: FK − Leadless Ceramic Chip Carrier (LCCC)
GB − Ceramic Pin Grid Array (CPGA)
HFP, HS, HT, HV − Ceramic Quad Flatpack (CQFP)
J, JT − Ceramic Dual-In-Line Package (CDIP)
W, WA, WD − Ceramic Flatpack (CFP)

10 Tape and Reel

Devices in the DB and PW package types include the R designation for reeled product. Existing product inventory designated LE may remain, but all products are being converted to the R designation.

Examples: Old Nomenclature − SN74LVTxxxDBLE
New Nomenclature − SN74LVTxxxADBR

LE − Left Embossed (valid for DB and PW packages only)
R − Standard (valid for all surface-mount packages)

There is no functional difference between LE and R designated products, with respect to the carrier tape, cover tape, or reels used.

[†] DSBGA is the JEDEC reference for wafer chip scale package (WCSP).

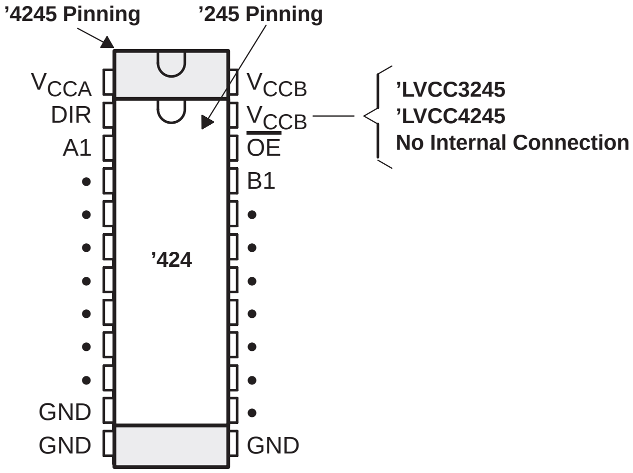
Figure 11. Device Number and Package Designators for TI Devices

Special features of TI standard logic devices are designated in the device number by abbreviations, as listed below and defined in the following paragraphs.

Blank − No special features
C − Configurable V_{CC}
D − Level-shifting diode
H − Bus hold
K − Undershoot-protection circuitry
R − Damping resistor on inputs/outputs
S − Schottky clamping diode
Z − Power-up 3-state

Configurable V_{CC} (C)

Configurable V_{CC} is a feature of devices that are designed as dual-supply level shifters, e.g., SN74LVCC3245 and SN74LVCC4245. Using these devices allows selection of the voltage to be applied to V_{CC} on the B-port side (V_{CCB}) and/or A-port side (V_{CCA}) (see Figure 12).



	V_{CCA} A PORT	V_{CCB} B PORT	TRANSLATION (BIDIRECTIONAL FLOW)
SN74LVCC3245A	2.3 V−3.6 V	3 V−5.5 V	2.5 V to 3.3 V or 3.3 V to 5 V
SN74LVCC4245A	5 V	3 V−5 V	5 V to 3.3 V

Figure 12. Example of Configurable V_{CC} Devices

Designers can use these devices in existing single-voltage systems. When systems become mixed-voltage systems, these devices do not need to be replaced, allowing for quicker time to market.

Level-Shifting Diode (D)

Devices with D as part of the device number have an integrated diode in the V_{CC} line. Examples are crossbar switches SN74CBTD3306 (with the integrated diode) and SN74CBT3306 (without the integrated diode). These devices allow 5-V to 3.3-V translation if no drive is required. Bidirectional data transmission is allowed between 5-V TTL and 3.3-V LVTTL, whereas only unidirectional level translation is allowed from 5-V CMOS to 3.3-V LVTTL (see Figure 13). The integrated diode saves designers both board space and component cost.

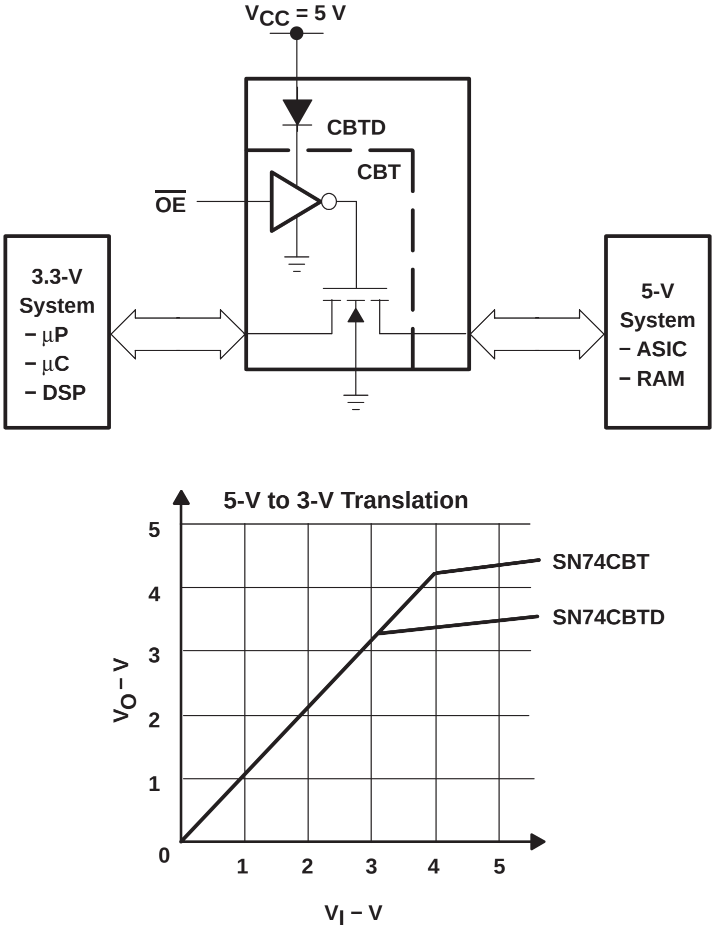

V_{CC} = 5 V
CBTD
CBT
$\overline{OE}$
3.3-V System
− µP
− µC
− DSP
5-V System
− ASIC
− RAM
5-V to 3-V Translation
SN74CBT
SN74CBTD
V_O − V
V_I − V
0
1
2
3
4
5

Figure 13. CBT vs CBTD With Internal Diode

Bus-Hold (H)

A bus-hold circuit is implemented in selected logic families to help solve the floating-input problem inherent in all CMOS inputs (refer to the application report, *Implications of Slow or Floating CMOS Inputs,* literature number SCBA004). The bus-hold circuit maintains the last known input state into the device and, as an additional benefit, pullup or pulldown resistors no longer are needed (see Figure 14). The advantages of devices with this circuit are board-space savings and reduced component costs.

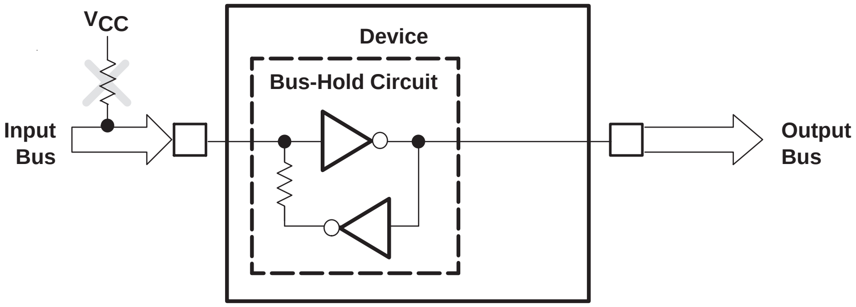

V_{CC}
Input Bus
Device
Bus-Hold Circuit
Output Bus

Figure 14. Benefit of Using Bus-Hold Devices

Damping Resistor on Inputs/Outputs (R)

Series damping resistors (SDR), denoted by R in the device number, are included at all input/output and output ports of designated devices (see Figure 15). The SDRs limit the current, thereby reducing signal undershoot and overshoot noise. Additionally, SDRs make line termination easier, which improves signal quality by reducing ringing and line reflections.

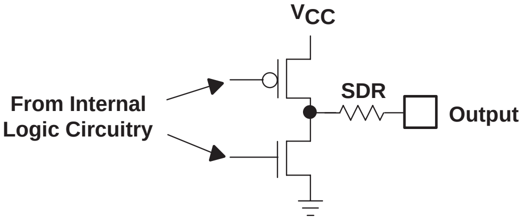


Figure 15. Series-Damping-Resistor Option

Schottky Clamping Diode (S)

Schottky diodes are incorporated in inputs and outputs to clamp undershoot (see Figure 16). The Schottky diodes prevent undershoot signals from dropping below a specified level, reducing the possibility of damage to connected devices by large undershoots that can occur without the Schottky diodes.

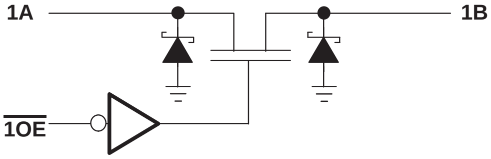
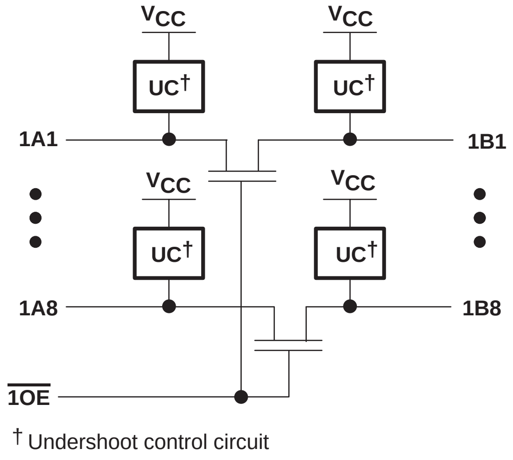


Figure 16. Schottky Clamping-Diode Device Schematic

Undershoot-Protection Circuitry (K)

TI undershoot-protection circuitry (UPC) functions similarly to Schottky clamping diodes, with one major difference. UPC is an active clamping structure. UPC can greatly reduce undershoot voltage, increasing protection from corrupted data (see Figure 17).


VCC
VCC
UC†
UC†
1A1
1B1
VCC
VCC
UC†
UC†
1A8
1B8
1OE
† Undershoot control circuit

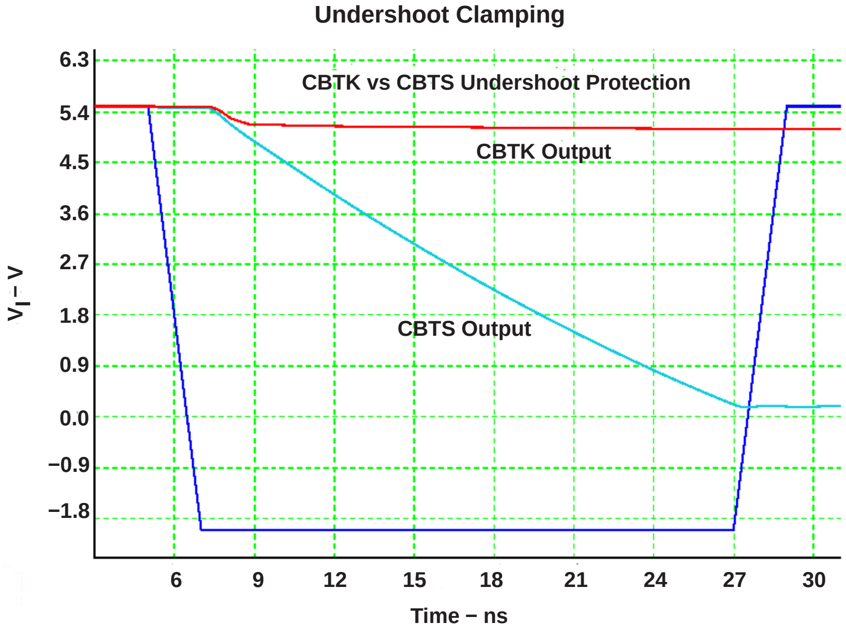


Figure 17. Undershoot-Protection Circuitry in K-Option Devices

Power-Up 3-State (Z)

The power-up 3-state (PU3S) feature ensures valid output levels during power up and ensures the valid high-impedance state during power down. The output enable pin ($\overline{\text{OE}}$) must be tied high (to V_{CC}) through an external pullup resistor (see Figure 18). For more information, see I_{OZPD} and I_{OZPU} specifications in the *electrical characteristics* section.

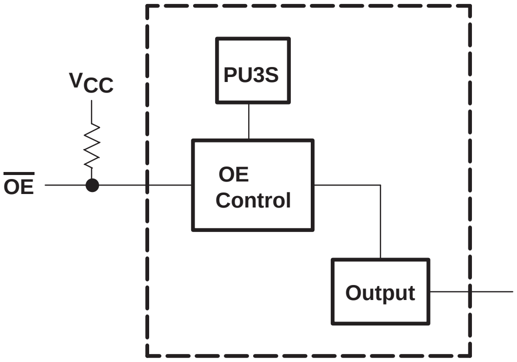


Figure 18. PU3S Circuit Implementation

Features Bullets

The *features bullets* section highlights information about the salient functions, features, and benefits of the device. Some features bullets provide an indication of functionality and application of the device, such as “Eight D-type Flip-Flops in a Single Package”, “3-State Outputs”, “Carry Output for N-bit Cascading” (for a binary counter), “Performs Parallel-to-Serial Conversion”, or “Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels”. Some data sheets contain electrostatic discharge (ESD) or latch-up test results and the associated JEDEC test conditions. The following are explanations of some common features bullets.

- Flow-Through Architecture Optimizes PCB Layout

  The data inputs and corresponding outputs are on opposite sides of the package. This feature makes printed circuit board trace routing easier.

- Bus-Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors

  Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. For more information on bus hold refer to the TI application report, *Bus-Hold Circuit*, literature number SCLA015.

- I_{off} Supports Partial-Power-Down Mode Operation

  This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

- I_{off} and Power-Up 3-State Support Hot Insertion

  This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

- I_{off}, Power-up 3-State, and BIAS V_{CC} Support Live Insertion

  This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the input/output connections on a device port, preventing disturbance of active data on the bus during card insertion or removal and permits true live-insertion capability.

Package Options and Pinouts

This section contains a top-view illustration of the leaded-package pinout(s) and a bottom view of certain nonleaded packages. Package dimensions and other package information is available in the *mechanical data* section of the *Semiconductor Group Packaging Outlines Reference Guide*, literature number SSYU001.

Description

The *description* section contains a written detailed explanation of the functionality and features of the device.

BGA Packaging Top-View Illustrations and Pin-Assignments Table

This section contains the top-view illustrations and pin assignments for applicable BGA package types.

Ordering Information

A table is provided that gives the fully qualified orderable part number and topside symbolization for every package option of the device.

TI has converted to an advanced order-entry system that provides significant improvements to all facets of TI business, from production, to order entry, to logistics. One requirement is a limitation of TI part numbers to no more than 18 characters. Based on customer inputs, TI determined that the least-disruptive implementations would be as outlined below:

1. Package alias

   TI uses an alias to denote specific packages for device numbers that exceed 18 characters. Table 1 shows a mapping of package codes to an alias representation.

Table 1. Package Alias

CURRENT PACKAGE CODE	ALIAS
DL	L
DGG/DBB	G
DGV	V
GKE/GKF/GQL	K
DLR	LR − tape/reel packing
DGGR/DBBR	GR − tape/reel packing
DGVR	VR − tape/reel packing
GKER/GKFR/GQLR	KR − tape/reel packing

Current: SN74 ALVCH 162269A DGGR
New: SN74 ALVCH 162269A GR

2. Resistor-option nomenclature

   For device numbers of more than 18 characters and with input and output resistors, TI has adopted a simplified nomenclature to designate the resistor option. This eliminates the redundant “2” (designating output resistors) when the part number also contains an “R” (designating input/output resistors).

   Input/Output Resistor
   Output Resistor
   Current: SN74 ALVCH R 16 2 245 A
   New: SN74 ALVCH R 16 245 A

There is no change to the device or data-sheet electrical parameters. The packages involved and the changes in nomenclature are given in Table 1.

Function Table

The function table illustrates the expected logic values on the outputs, when the inputs have the given stimuli applied.

The following symbols are used in function tables on TI data sheets:

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
⟶ = value/level or resulting value/level is routed to indicated destination
↶ = value/level is re-entered
X = irrelevant (any input, including transitions)
Z = off (high-impedance) state of a 3-state output
a . . . h = the level of steady-state inputs A through H, respectively
Q_0 = level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$ = complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n = level of Q before the most-recent active transition indicated by ↓ or ↑
⊓ = one high-level pulse
⊔ = one low-level pulse
Toggle = each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

In the input columns, if a row contains only the symbols H, L, and/or X, the indicated output is valid when the input configuration is achieved, regardless of the sequence in which it is achieved. The output persists as long as the input configuration is maintained.

In the input columns, if a row contains H, L, and/or X, together with ↑ and/or ↓, the output is valid when the input configuration is achieved, but the transition(s) must occur after steady-state levels are attained. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists as long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. If the output is shown as a pulse, ⊓, or ⊔, the pulse follows the indicated input transition and persists for an interval that is dependent on the circuit.

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, and more. Table 2 is the function table of a 4-bit bidirectional universal shift register.

Table 2. Function Table

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	H	H	H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	L	L	L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first row of the table represents a synchronous clearing of the register and states that, if clear is low, all four outputs will be reset low, regardless of the other inputs, which are denoted by X. In the following rows, clear is inactive (high); therefore, it has no effect.

The second row shows that, as long as the clock input remains low (while clear is high), no other input has any effect, and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Because, on other rows of the table only the rising transition of the clock is shown to be active, the second row implicitly shows that no further change in the outputs occurs while the clock remains high or on the high-to-low transition of the clock.

The third row of the table represents synchronous parallel loading of the register and states that if S1 and S0 are both high, then, without regard to the serial input, the data entered at A is at output Q_A, data entered at B is at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth rows represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D, respectively, and the data previously at Q_D no longer is in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high, and the levels at inputs A through D have no effect.

The sixth and seventh rows represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D now are at Q_B and Q_C, respectively, and the data previously at Q_A no longer is in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low, and the levels at inputs A through D have no effect.

The last row shows that, as long as both inputs are low, no other input has any effect and, as in the second row, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The function table functional tests do not reflect all possible combinations or sequential modes.

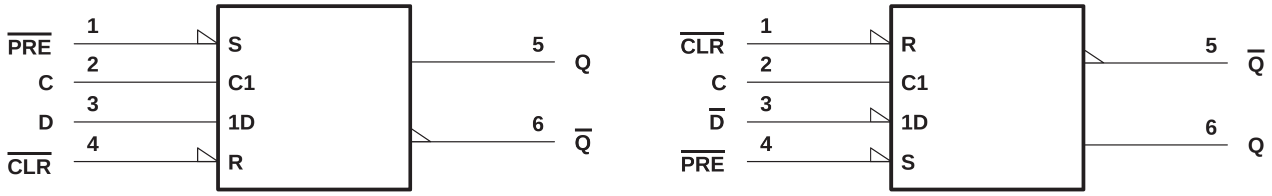
Logic Diagram

The logic diagram is a positive-logic illustration of the Boolean functionality of the device. Furthermore, in some logic-device data sheets that have wide identical configurations, such as a 16-bit or a 32-bit device, the logic diagram often is shown in partial format that includes the unique circuitry and only one of the data paths.

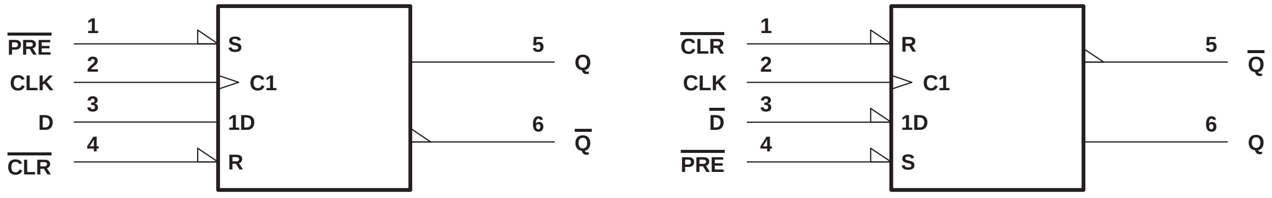
For D-type flip-flops and latches, it is TI convention to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol, based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q, and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear (CLR). Bars are placed over these pin names ($\overline{\text{PRE}}$ and $\overline{\text{CLR}}$) if they are active low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits, $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$, or vice versa. In that case, all the other inputs and outputs should be renamed, as shown Figure 19. Also shown, are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.


$\overline{\text{PRE}}$
C
D
$\overline{\text{CLR}}$
1
2
3
4
S
C1
1D
R
5
6
Q
$\overline{Q}$
$\overline{\text{CLR}}$
C
$\overline{D}$
$\overline{\text{PRE}}$
1
2
3
4
R
C1
1D
S
5
6
$\overline{Q}$
Q

Latch Latch


$\overline{\text{PRE}}$
CLK
D
$\overline{\text{CLR}}$
1
2
3
4
S
C1
1D
R
5
6
Q
$\overline{Q}$
$\overline{\text{CLR}}$
CLK
$\overline{D}$
$\overline{\text{PRE}}$
1
2
3
4
R
C1
1D
S
5
6
$\overline{Q}$
Q

Flip-Flop Flip-Flop

Figure 19. Example Logic Diagrams

The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators (⊵) on $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ remain, as these inputs still are active low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

Product Development Stage Note

The product development stage note is a standard disclaimer placed at the lower left corner of the first page of data sheets, and the words **ADVANCED INFORMATION** or **PRODUCT PREVIEW**, as applicable, appear in the left and right margins of all pages of the data sheet. There is only the product development stage note on the first page for production-data devices. For additional information, see the EIA/JEDEC engineering publication, *Suggested Product-Documentation Classifications and Disclaimers*, JEP103A.

Absolute Maximum Ratings

Supply Voltage, V_{CC}

This is the maximum voltage that can be applied safely to the V_{CC} terminal, with respect to the ground of the device. However, no data-sheet parameters are ensured when a device is operated at the absolute maximum V_{CC} level.

Input Voltage, V_I

This is the maximum voltage that can be applied safely to an input terminal, with respect to the ground of the device. This maximum V_I specification may be exceeded if the output clamp rating, I_{IK}, is observed.

Helpful Hint:

If there are clamp diodes between the device inputs and the V_{CC} supply (see Figure 20) for ESD protection or overshoot clamping, the positive absolute-maximum rating for the input voltage is specified as V_{CC} + 0.5 V. Keeping the applied input voltage less than 0.5 V above V_{CC} ensures that there will not be enough voltage across the clamp diode to forward-bias it and cause current to flow through it. The TI logic families with clamp diodes in the inputs are: AC, ACT, AHC, AHCT, ALB, ALS, ALVC, AS, F, (CD)FCT, HC, HCT, HSTL, LS, PCA, PCF, S, SSTL, and TTL.

If there are no clamp diodes between the device inputs and the V_{CC} supply, the positive absolute maximum rating is a limitation of the process technology and is specified as an absolute voltage (e.g., 5.5 V). The TI logic families without clamp diodes in the inputs are: ABT, ABTE, ALS, ALVT, AUC, AVC, BCT, FB, GTLP, GTL, LS, LV, LVC, LVCZ, LVT, (CY)FCT, SSTV, and VME.

You may exceed the negative input-voltage rating if you ensure that you are not putting too much current through the ground-clamp diode. The I_{IK} absolute maximum rating specifies the maximum current that may be put through the ground-clamp diode.

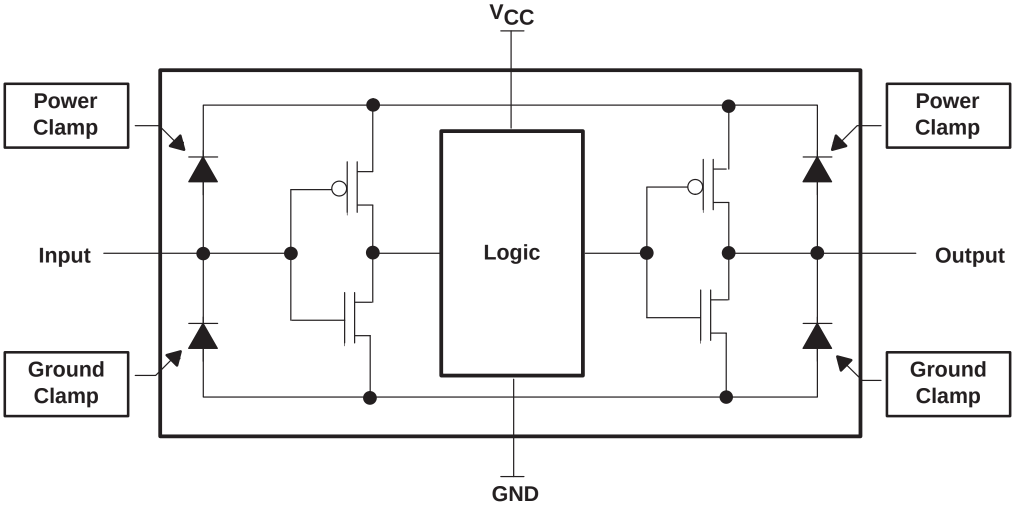


Figure 20. Representation of Typical Logic I/O Clamping Circuits

Output Voltage, V_O

This is the maximum voltage that can be applied safely to an output terminal, with respect to the ground of the device.

Helpful Hint:

If there are clamp diodes between the device outputs and the V_{CC} supply (see Figure 20) for ESD protection or parasitic current paths in the output p-channel pullup transistor, the positive absolute maximum rating for the output voltage is specified as V_{CC} + 0.5 V. This ensures that there will not be enough voltage applied between the output and V_{CC} to forward bias the clamp diode and cause current to flow. You may exceed the negative rating if you ensure that you are not putting too much current through the ground-clamp diode. The maximum current that you may put through the ground-clamp diode is specified in the I_{OK} absolute maximum rating.

If there are no clamp diodes or parasitic current paths in the output p-channel pullup transistor between the device outputs and the V_{CC} supply, the positive absolute maximum rating is a limitation of the process technology and is specified as an absolute voltage.

Voltage Range Applied to Any Output in the High-Impedance or Power-Off State, V_O

This specification is similar to the *Output Voltage, V_O* specification and is used with the *Voltage Range Applied to Any Output in the High State, V_O* specification. On devices with the I_{off} feature, there are no clamp diodes or parasitic current paths in the output p-channel pullup transistor between the device outputs and the V_{CC} supply; the positive absolute-maximum rating is a limitation of the process technology and is specified as an absolute voltage. You may exceed the negative rating if you ensure that you are not putting too much current through the ground-clamp diode. The maximum current that you may put through the ground-clamp diode is specified in the I_{OK} absolute-maximum rating.

Helpful Hint:

This specification is necessary only for devices with the I_{off} feature.

Voltage Range Applied to Any Output in the High State, V_O

This specification is similar to the *Output Voltage, V_O* specification and is used with the *Voltage Range Applied to Any Output in the High-Impedance or Power-Off State, V_O* specification. When the output is enabled and is in the output high state, there is a current path between the output and V_{CC} through the output p-channel pullup transistor. Applying a voltage to the output that is greater than the V_{CC} voltage causes damaging current to flow back from the output into the V_{CC} supply. You may exceed the negative rating if you ensure that you are not putting too much current through the power-clamp diode. The I_{OK} absolute-maximum rating specifies the maximum current that you may put through the ground-clamp diode.

Helpful Hint:

This specification is necessary only for devices with the I_{off} feature.

Input Clamp Current, I_{IK}

This is the maximum current that can flow safely into an input terminal of the device at voltages above or below the normal operating range.

Helpful Hint:

If there are clamp diodes between the device inputs and the V_{CC} supply (see Figure 20), for ESD protection or overshoot clamping, there will be both a positive and negative absolute maximum rating for the input clamp current. If there is only a negative absolute maximum rating, that implies that there is only a ground-clamp diode at the input, not a power-clamp diode.

Output Clamp Current, I_{OK}

This is the maximum current that can flow safely into an output terminal of the device at voltages above or below the normal operating range.

Helpful Hint:

If there are clamp diodes between the device outputs and the V_{CC} supply (see Figure 20), for ESD protection or parasitic current paths in the output p-channel pullup transistor, there will be both a positive and a negative absolute-maximum rating for the output clamp current. If there is only a negative absolute-maximum rating, that implies that there is only a ground-clamp diode at the output, not a power-clamp diode or a parasitic current path in the output p-channel pullup transistor.

Continuous Output Current, I_O

This is the maximum output source or sink current that can flow safely into an output terminal of the device at voltages within the normal operating range.

Continuous Current Through V_{CC} or GND Terminals

This is the maximum current that can flow safely into the V_{CC} or GND terminals of the integrated circuit.

Package Thermal Impedance, Junction-to-Ambient, θ_{JA}

This is the thermal resistance from the operating portion of a semiconductor device to a natural convection (still air) environment surrounding the device. Tested per JEDEC Standard JESD51-3. For additional information, refer to the TI Application Report; *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*, literature number SCZA005.

Storage Temperature Range, T_{stg}

This is the range of temperatures over which a device can be stored without causing excessive degradation of its performance characteristics.

Recommended Operating Conditions

V_{CC} Supply Voltage

JEDEC – The supply voltage applied to a circuit connected to the reference terminal.

TI – The range of supply voltages for which operation of the logic element is specified.

The example in Figure 3 lists 2.7 V as the minimum V_{CC}. No electrical or switching characteristic is specified for V_{CC} less than 2.7 V. Operation outside of the minimum and maximum values is not recommended, and a previously established logic state might not be maintained under such conditions.

Helpful Hint:

Frequently, TI receives requests from customers wanting assurance that TI logic devices will operate properly outside of specified conditions. The logic device may, indeed, perform flawlessly in the application posed by the customer, but TI does not represent that the device will provide the same level of reliability and performance when operated outside of specified conditions.

BIAS V_{CC} Bias Supply Voltage

JEDEC – *no definition offered*

TI – A supply voltage used in generating a precharge voltage that is applied to an I/O for live-insertion purposes.

Power sequencing is critical in live-insertion applications. Therefore, care must be taken with the timing of application of BIAS V_{CC}, V_{CC}, ground, and data input voltages during an insertion or extraction of a daughter card implementing a device with this capability (see the application report, *Logic in Live-Insertion Applications With a Focus on GTLP,* literature number SCEA026).

Helpful Hint:

Texas Instruments offers only three technologies with true live-insertion capabilities: FB, GTLP, and VME.

V_{TT} Termination Voltage

JEDEC – *no definition offered*

TI – A supply voltage used to terminate a bus (most commonly used in open-drain devices) and in generating a reference voltage for differential inputs.

Because open-drain devices such as GTLP and FB cannot raise the output voltage to a high state by their own accord, external resistors, which are tied to an external termination voltage, are used.

Helpful Hint:

V_{TT} determines the high-level voltage value and, since most open-drain technologies can tolerate a wide range of voltage levels, open-drain devices are used quite often in voltage-translation applications.

V_{ref} Reference Voltage

JEDEC – A power supply that acts as a reference for determining internal threshold voltages, but does not supply any substantial power to the device.

TI – A reference bias voltage used to set the switching threshold of differential input devices.

V_{IH} High-Level Input Voltage

JEDEC – V_{IH} min is the least positive (most negative) value of high-level input voltage for which operation of the logic element within specification limits is to be expected. V_{IH} max is the most positive (least negative) value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

TI – An input voltage within the more positive (the less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

A voltage within this range corresponds to the logic-1 state in positive logic. During device testing, V_{IH} min is specified for all inputs. Since V_{IH} min is used to set up V_{OH}, V_{OL}, I_{OZH}, and I_{OZL} tests, all possible combinations of input thresholds may not be verified. The nondata inputs (e.g., direction, clear, enable, and preset) may be considered unused inputs and may not be at threshold conditions. These inputs control functions that can cause all the outputs to switch simultaneously. The noise that can be generated by switching a majority of the outputs at one time can cause significant tester ground and V_{CC} movement. This can result in false test measurements.

Helpful Hint:

Some bipolar-input devices sink a certain amount of current into the input pin, as specified on the data sheet. The higher the V_{IH} voltage is, the more current that will be drawn into the input pin. CMOS-input devices behave in a different manner because, in most cases, the input pin essentially is tied directly to the high-impedance gate of an input inverter. In a static dc state, a CMOS input sinks or sources only a minute amount of leakage current (a few µA). However, it is imperative that for any logic device, but especially for a CMOS input, the input high logic level always be above the recommended V_{IH} min. Failure to do this causes a surge of current to flow through the input inverter from the V_{CC} supply to ground and, subsequently, may destroy the device.

Helpful Hint:

TI data sheets do not specify a V_{IH} max that typically is found in competitor data sheets. Instead, see V_I max for the same value.

Helpful Hint:

Failure to supply a voltage to the input of a CMOS device that meets the V_{IH} or V_{IL} recommended operating conditions can cause: (1) propagation of incorrect logic states, (2) high I_{CC} currents, (3) high input noise gain and oscillations, (4) power- and ground-rail surge currents and noise, and (5) catastrophic device and circuit failure.

Helpful Hint:

A device with an input V_{IH} = 2 V and a V_{IL} = 0.8 V has a TTL-compatible input. A device with the input levels scaled with respect to V_{CC} (e.g., $V_{IH} = 0.7 \times V_{CC}$, $V_{IL} = 0.3 \times V_{CC}$) has CMOS inputs.

V_{IL} Low-level Input Voltage

JEDEC – V_{IL} min is the least-positive (most negative) value of low-level input voltage for which operation of the logic element within specification limits is to be expected. V_{IL} max is the most positive (least negative) value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

TI – An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

A voltage within this range corresponds to the logic-0 state in positive logic. During device testing, V_{IL} max is specified for all inputs. Since V_{IL} max is used to set up V_{OH}, V_{OL}, I_{OZH}, and I_{OZL} tests, all possible combinations of input thresholds may not be verified. The nondata inputs (e.g., direction, clear, enable, and preset) may be considered unused inputs and may not be at threshold conditions. These inputs control functions that can cause all the outputs to switch simultaneously. The noise that can be generated by switching a majority of the outputs at one time can cause significant tester ground and V_{CC} changes. This can result in false test measurements.

Helpful Hint:

Most bipolar-input devices source a certain amount of current out of the input pin, as specified on the data sheet. The lower the V_{IL} voltage is, the more current that will be drawn out of the input pin. CMOS-input devices behave in a different manner because, in most cases, the input pin essentially is tied directly to the gate of an input inverter. In a static dc state, a CMOS input sinks or sources only a minute amount of leakage current (a few µA). However, it is imperative that for any logic device, but especially for a CMOS input, the input low logic level always be below the recommended V_{IL} max. Failure to do this will cause a surge of current to flow through the input inverter from the V_{CC} supply to ground and, subsequently, may destroy the device.

Helpful Hint:

TI data sheets do not specify a V_{IL} min that typically is found in competitor data sheets. Instead, see V_I min for the same value.

Helpful Hint:

Failure to supply a voltage to the input of a CMOS device that meets the V_{IH} or V_{IL} recommended operating conditions can cause: (1) propagation of incorrect logic states, (2) high I_{CC} currents, (3) high input noise gain and oscillations, (4) power- and ground-rail surge currents and noise, and (5) catastrophic device and circuit failure.

Helpful Hint:

A device with an input V_{IH} = 2 V and a V_{IL} = 0.8 V has a TTL-compatible input. A device with the input levels scaled with respect to V_{CC} (e.g., $V_{IH} = 0.7 \times V_{CC}$, $V_{IL} = 0.3 \times V_{CC}$) has CMOS inputs.

I_{OH} High-Level Output Current

JEDEC – The current into the output terminal with input conditions applied that, according to the product specification, establishes a high level at the output.

TI – The current into an output with input conditions applied that, according to the product specification, establishes a high level at the output.

TI data sheets specify currents flowing out of a device as a negative value. I_{OH} max is used as a test condition for V_{OH}. See V_{OH} testing for further details.

Logic output drivers have a maximum current drive capability that they can source and still be able to sustain a valid logic-high level. In a static dc state, where current is drawn continuously from the output, because CMOS drivers operate in the linear region, their behavior is somewhat like a low-impedance resistor and increases in voltage potential (i.e., decreases the V_{OH} level) as the increasing current is sourced out of the output pin during a V_{OH} test. Consequently, a TI logic device operates with a high-level output current that is above the recommended operating range (but below the absolute maximum rating), but TI does *NOT* represent that the device can sustain the specified V_{OH} level or that the device will operate without any reliability concerns.

I_{OHS} Static High-Level Output Current

JEDEC – *no definition offered*

TI – The static and testable current into a Dynamic Output Control (DOC™ circuitry) output with input conditions applied that, according to the product specifications, establishes a static high level at the output. The dynamic drive current is not specified for devices with DOC circuitry outputs because of its transient nature; however, it is similar to the dynamic drive current that is available from a high-drive (nondamping resistor) standard-output device.

TI data sheets specify currents flowing out of a device as a negative value.

DOC circuitry is designed to drive CMOS input devices, which are capacitive in nature, in point-to-point applications (one receiver input per driver output). For this reason, a large static high-level output current is not required. In this case, what matters most is the high transient-drive capability of the output.

For additional information about DOC circuitry, refer to the TI application report, *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

I_{OL} Low-Level Output Current

JEDEC – The current into the output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

TI – The current into an output with input conditions applied that, according to the product specification, establishes a low level at the output.

TI data sheets specify currents flowing out of a device as a negative value. I_{OL} maximum is used as a test condition for V_{OL}. See V_{OL} testing for details.

Logic output drivers have a maximum current-drive capability that they can sink and still be able to sustain a valid logic-low level. In a static dc state where current is continuously drawn into the output, because CMOS drivers operate in the linear region, their behavior will be somewhat like a low-impedance resistor and will increase in voltage potential (i.e., increase the V_{OL} level) as the increasing current is sunk into the output pin during a V_{OL} test. Consequently, a TI logic device will operate with a low-level output current that is above the recommended operating range (but below the absolute maximum rating), but TI does *NOT* represent that the device can sustain the specified V_{OL} level or that the device will operate without any reliability concerns.

I_{OLS} *Static Low-Level Output Current*

JEDEC – *no definition offered*

TI – The static and testable current into a Dynamic Output Control (DOC circuitry) output with input conditions applied that, according to the product specifications, establishes a static low level at the output. The dynamic drive current is not specified for devices with DOC circuitry outputs because of its transient nature; however, it is similar to the dynamic drive current that is available from a high-drive (nondamping resistor) standard-output device.

TI data sheets specify currents flowing out of a device as a negative value.

DOC circuitry is designed to drive CMOS input devices, which are capacitive in nature, in point-to-point applications (one receiver input per driver output). For this reason, a large static low-level output current is not required. What matters most in this case is the high-transient-drive capability of the output.

For additional information about DOC circuitry, refer to the TI application report, *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

V_I *Input Voltage*

JEDEC – The voltage at the input terminals.

TI – The range of input voltage levels over which the logic element is specified to operate.

V_I min and V_I max values are used as test conditions for the I_I, I_{CC}, ΔI_{CC}, C_i, and C_{io} test. See those specifications for details.

Helpful Hint:

If there are clamp diodes between the device inputs and the V_{CC} supply (see Figure 20) for ESD protection or overshoot clamping, the positive absolute maximum rating for the input voltage will be specified as V_{CC} + 0.5 V. Keeping the applied input voltage less than 0.5 V above V_{CC} ensures that there will not be enough voltage across the clamp diode to forward bias it and cause current to flow through it.

You may exceed the negative rating if you ensure that you are not putting too much current through the ground-clamp diode. The maximum current that you may put through the ground-clamp diode is specified in the I_{IK} absolute-maximum rating.

Helpful Hint:

This parameter provides a means to determine if the device is tolerant of a higher voltage than the supply voltage. If the input is overvoltage tolerant, the positive maximum rating for the input voltage will be an absolute voltage rating (e.g., 5.5 V) and will be limited by the capabilities of the wafer-fab process. For example, the LVC technology is specified to operate at a voltage supply no higher than 3.6 V. However, the input voltage is recommended to be 5.5 V maximum. This indirectly states that the device is a 5-V tolerant device. The same can be said about AUC devices because the maximum supply voltage is 2.7 V, whereas the maximum input voltage is 3.6 V, making this technology 3.3-V tolerant.

Helpful Hint:

This parameter explicitly states the recommended minimum and maximum input voltage levels for any input. While the V_I specification typically spans the range from below ground to above V_{CC}, failure to supply a voltage to the input of a CMOS device that meets the V_{IH} or V_{IL} recommended operating conditions can cause: (1) propagation of incorrect logic states, (2) high I_{CC} currents, (3) high input noise gain and oscillations, (4) power- and ground-rail surge currents and noise, and (5) catastrophic device and circuit failure.

V_O Output Voltage

JEDEC – The voltage at the output terminals.

TI – The range of output voltage levels over which the logic element is specified.

V_O min and max values are used as test conditions for I_{OZH} and I_{OZL}. See these tests for details.

Helpful Hint:

The load at the output strictly determines the output voltage. As discussed in the V_{OH} and V_{OL} descriptions, a constant dc current decreases and increases, respectively, the output voltage. For this reason, it is not recommended to drive bipolar inputs with CMOS outputs unless the sum of all bipolar input current is less than the rated I_{OH} and I_{OL} of the CMOS output. Highly capacitive loads, such as any CMOS type input, will not incur any static dc current, so a CMOS output voltage should be close to the rail when asserted high or low. Capacitive loads, not the ultimate static dc voltage level, determine the time it takes for the output to arrive at the logic high or low state.

$\Delta t/\Delta v$ Input Transition Rise or Fall Rate

JEDEC – *no definition offered*

TI – The rate of change of the input voltage waveform during a logic transition (low-to-high or high-to-low).

To avoid output-waveform abnormalities, input voltage transitions should be within the range set forth in the recommended operating conditions.

Customers often place external capacitors on a trace to ensure the driver does not switch rapidly from one logic state to another. This is sometimes done to prevent unwanted overshoot and undershoot voltage conditions that could cause ringing and degrade signal integrity, or in switch debounce circuits. However, this could cause problems at the input; therefore, TI provides input transition rise or fall rates. The problem may not arise due to external capacitive loading, however, but may be the result of choosing a device with a weak driver. In either case, the end result is a voltage waveform that is too slow for the device.

Slow transition rates wreak havoc on CMOS inputs because a slowly changing input voltage will induce a large amount of current from the power supply to ground. This phenomenon is known as *through current*. Through currents are normal ac transient currents, but when they are sustained indefinitely−as are those caused by slow input transition rates−the device will not perform as expected, and its output voltage may oscillate or, even worse, damage the device. This surge of current, if large enough, will disturb the ground reference because of the inductive nature of the package [$V = L \times (di/dt)$] and produce a positive-going glitch on the ground reference. The glitch may, in turn, reduce the relative magnitude, causing the output node of the input inverter to switch states. Ultimately, this erroneous data propagates to the output of the device, thereby causing oscillations. The more inputs that are being switched in the same manner, the worse this condition becomes, as more current is being forced into ground during a short time. TI data sheets specify the slowest input transition rate to avoid this problem. For additional information, refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Helpful Hint:

If you must supply a slowly changing voltage to the input of a logic device, select a device that has Schmitt-trigger inputs. These inputs have been specifically designed to tolerate slow edges. An example of such a device in the LVC family is the SN74LVC14.

$\Delta t/\Delta V_{CC}$ Power-up Ramp Rate

JEDEC – *no definition offered*

TI – The rate of change of the supply voltage waveform during power up.

T_A Operating Free-Air Temperature

JEDEC – *no definition offered*

TI – The range of operating temperatures over which the logic element is specified.

In digital-system design, consideration must be given to thermal management of components. The small size of packages makes this more critical. Figure 21 shows the high-effect (high-K) thermal resistance for the 5-, 14-, 16-, 20-, 24-, 48-, 56-, 64-, and 80-pin packages for various rates of airflow calculated in accordance with JESD51-7.

The thermal resistances in Figure 21 can be used to approximate typical and maximum virtual junction temperatures. In general, the junction temperature for any device can be calculated using the following equation:

$$T_J = R_{\theta JA} \times P_T + T_A$$

Where:
T_J = virtual junction temperature (°C)
$R_{\theta JA}$ = thermal resistance, junction to free air (°C/W)
P_T = total power dissipation of the device (W)
T_A = free-air temperature (°C)

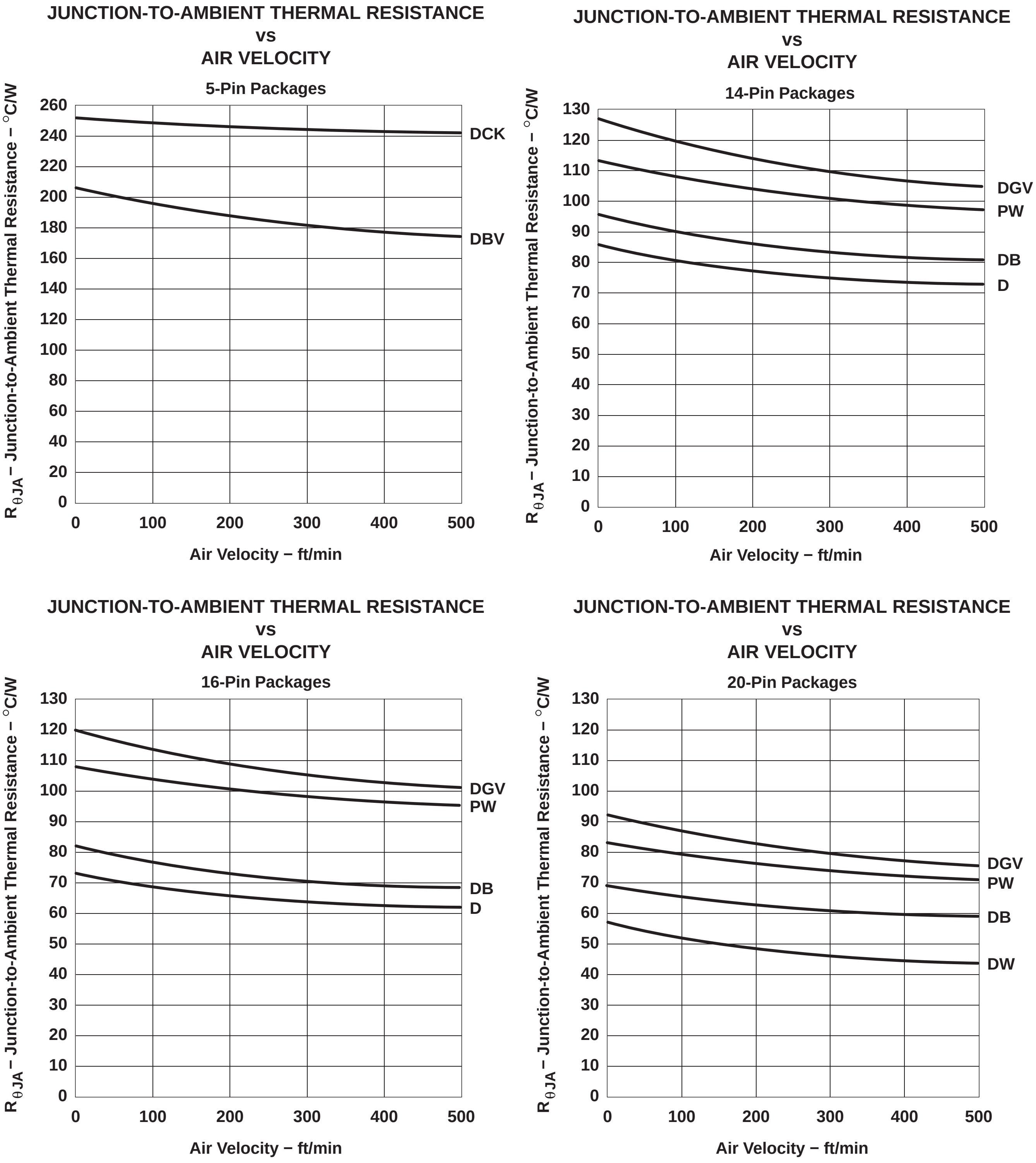


Figure 21. High-K Thermal-Resistance Graphs for 5-, 14-, 16-, 20-, 24-, 48-, 56-, 64-, and 80-Pin Packages

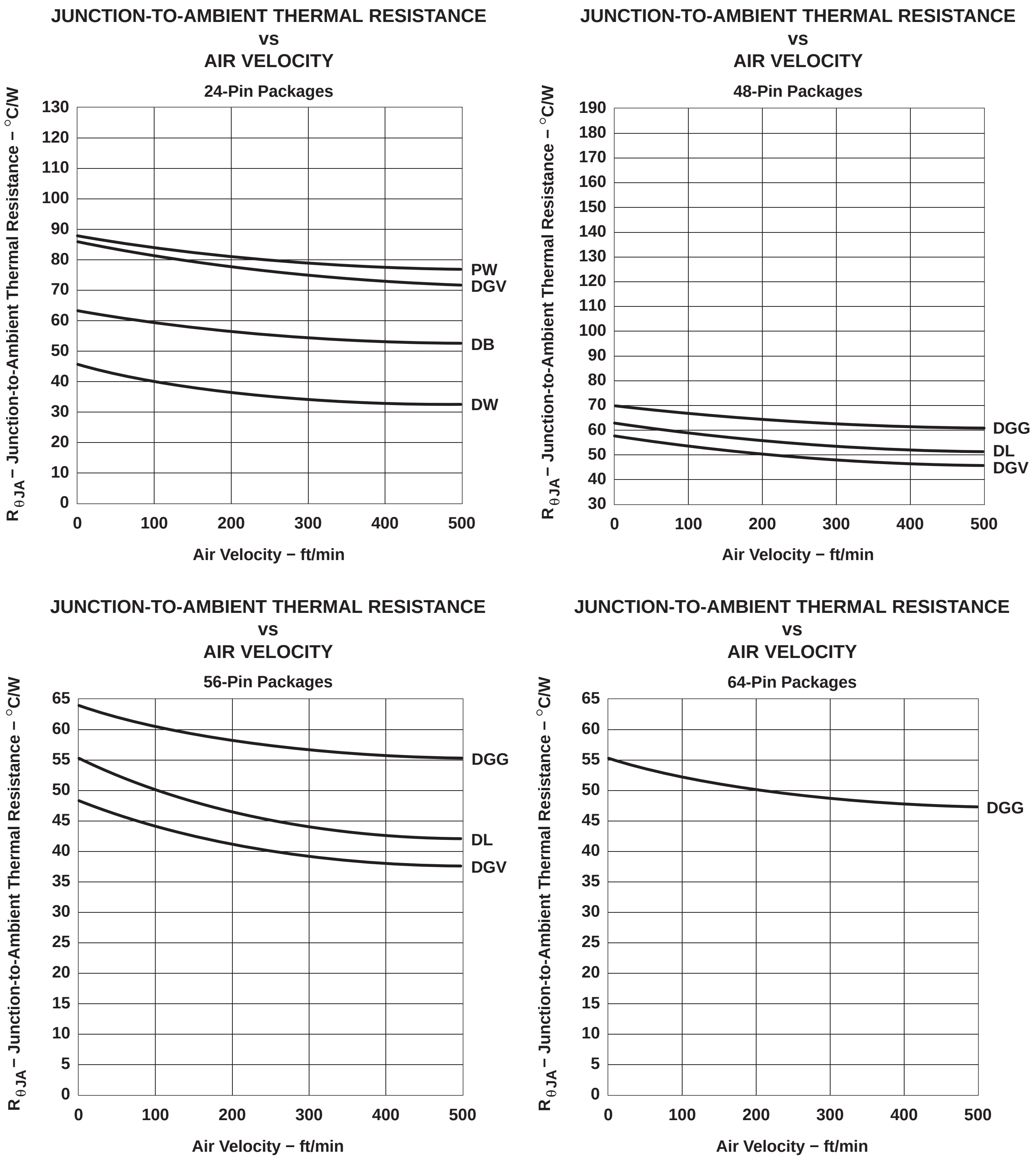


Figure 21. High-K Thermal-Resistance Graphs for 5-, 14-, 16-, 20-, 24-, 48-, 56-, 64-, and 80-Pin Packages (Continued)

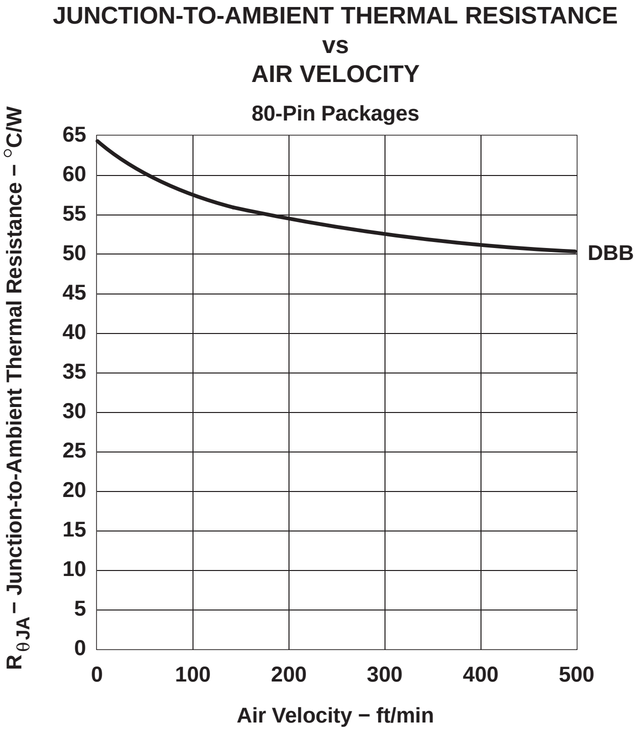


Figure 21. High-K Thermal-Resistance Graphs for 5-, 14-, 16-, 20-, 24-, 48-, 56-, 64-, and 80-Pin Packages (Continued)

Electrical Characteristics

V_{T+} Positive-Going Input Threshold Level

JEDEC – The input threshold voltage when the input voltage is rising.

TI – The voltage level at a transition-operated input that causes operation of the logic element, according to specification, as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

See ΔV_T hysteresis for further information.

V_{T-} Negative-Going Input Threshold Level

JEDEC – The input threshold voltage when the input voltage is falling.

TI – The voltage level at a transition-operated input that causes operation of the logic element according to specification, as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

See ΔV_T hysteresis for further information.

ΔV_T *Hysteresis* $(V_{T+} - V_{T-})$

JEDEC – The difference between the positive-going and negative-going input threshold voltages.

TI – Refer to the JEDEC definition above.

Hysteresis has been incorporated into logic devices for many years and exists in bipolar as well as CMOS circuitry. Although the circuitry is different, the implementation is the same: the input voltage threshold actually changes internally from one level to another, as the input logic level itself switches. Figure 22 is the most common voltage plot for the input and output, as the input transitions from one logic state to the other. Figure 23, however, shows V_{IT+} and V_{IT-} in a voltage vs time waveform.

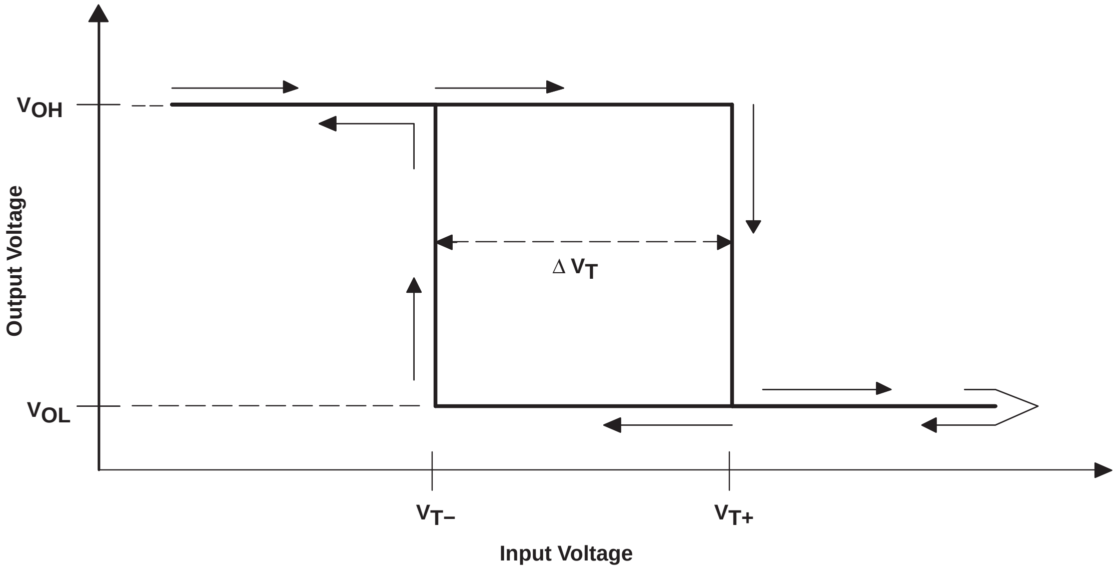


Figure 22. Hysteresis: V_I vs V_O

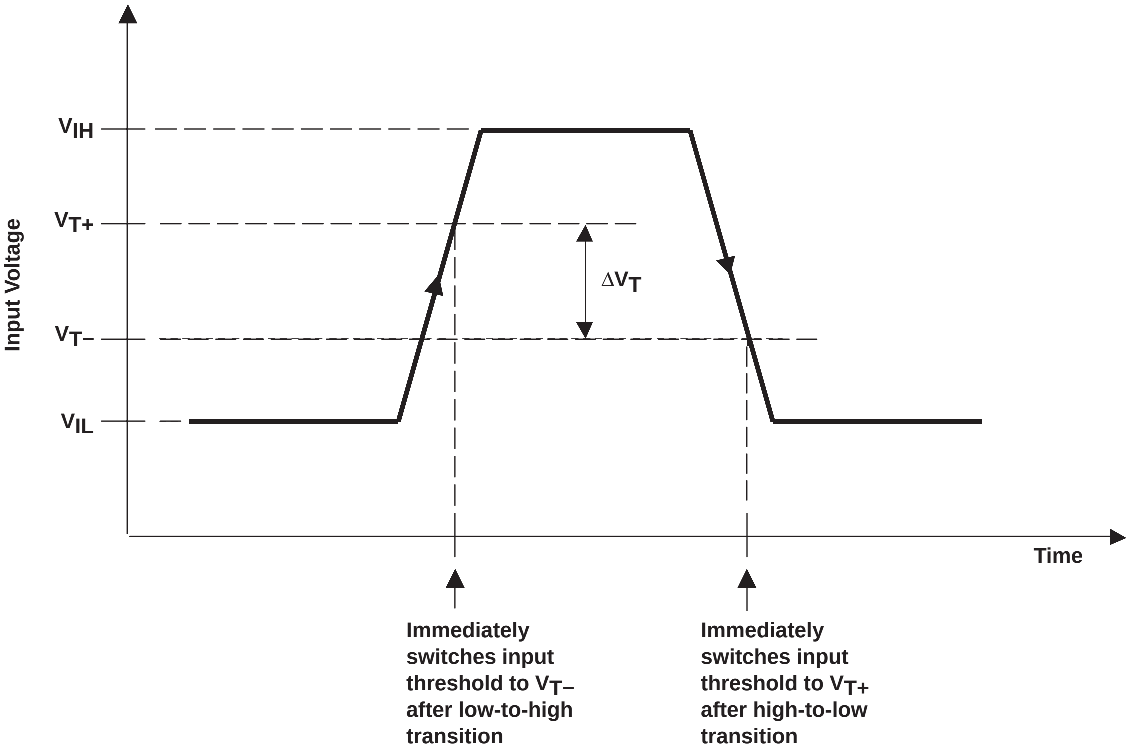

Input Voltage
V_{IH}
V_{T+}
V_{T-}
V_{IL}
ΔV_T
Time
Immediately switches input threshold to V_{T-} after low-to-high transition
Immediately switches input threshold to V_{T+} after high-to-low transition

Figure 23. Hysteresis: Input Voltage vs Time

The benefit of a device that has built-in dc hysteresis is that, depending on the amount of hysteresis and the amount of noise present, the input is immune to such noise. This digital form of filtering out unwanted noise can be beneficial in a system where noise caused by electromagnetic interference (EMI) or crosstalk cannot be reduced. Figures 24 and 25 conceptually depict the functionality of hysteresis.

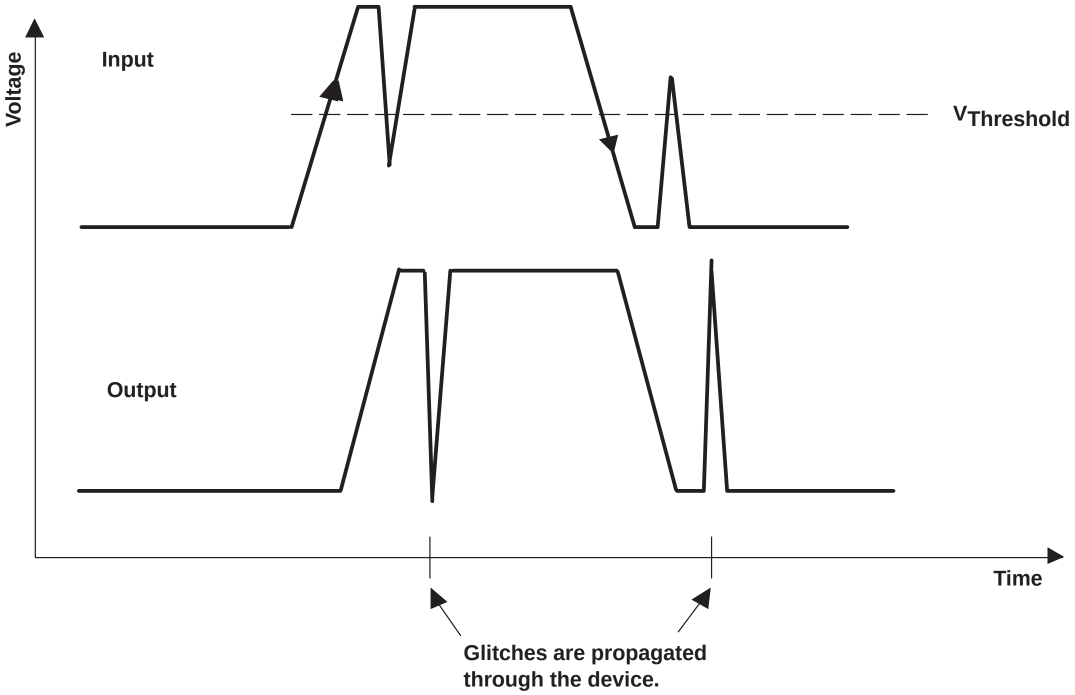


Figure 24. Possible Output-Voltage Outcome for Devices Without Hysteresis

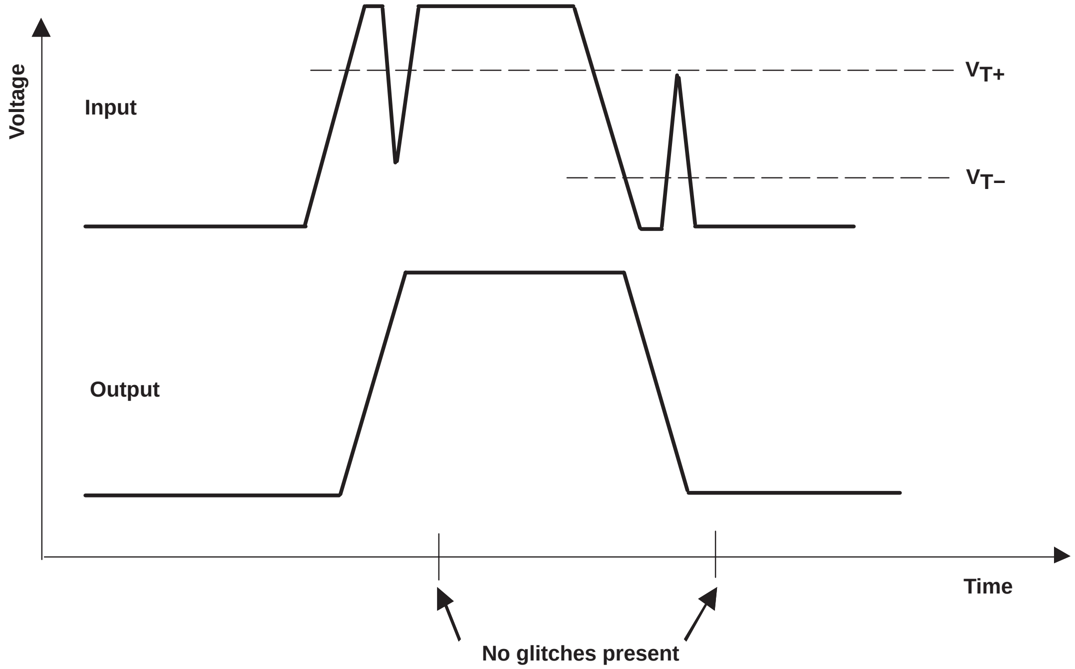


Figure 25. Glitch-Rejection Capabilities of Devices with Hysteresis

V_{IK} *Input Clamp Voltage*

JEDEC – An input voltage in a region of relatively low differential resistance that serves to limit the voltage swing.

TI – The maximum voltage developed across an input diode with test current applied.

Helpful Hint:

The presence of a V_{IK} specification indicates that there is a ground-clamp diode on the input and the V-I characteristics of that diode in its forward-biased region are given.

V_{OH} High-Level Output Voltage

JEDEC – The voltage level at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

TI – The voltage level at an output terminal with input conditions applied that, according to the product specification, establishes a high level at the output.

V_{OH} is tested with input conditions that should cause the output under test to be at a high-level voltage. The output then is forced to source the required current, as defined in the data sheet, and the output voltage is measured. The test is passed if the voltage is greater than V_{OH} min. The input voltage levels used to precondition the device are V_{IL} max and V_{IH} min, as defined in the *recommended operating conditions*. See I_{OH} high-level output current for further information.

Helpful Hint:

Inclusion of a V_{OH} specification with a test condition of $I_{OH} = -100\ \mu A$ is done primarily to indicate that the device has CMOS outputs instead of bipolar (npn or pnp) drivers. Bipolar output transistors typically are not able to swing the output voltages all the way to the power-supply rail or ground rail, even under no-load or lightly loaded conditions. If a device has bipolar outputs, this test condition would not apply and is not included in the data sheet. If you see this specification, you can safely assume the outputs to be of CMOS construction.

V_{OHS} Static High-level Output Voltage

JEDEC – *no definition offered*

TI – The static and testable voltage at a Dynamic Output Control (DOC circuitry) output with input conditions applied that, according to the product specifications, establishes a static high level at the output. The dynamic drive voltage is not specified for devices with DOC circuitry outputs because of its transient nature.

See I_{OHS} static high-level output current for further information.

For additional information about DOC circuitry, refer to the TI application report, *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

V_{OL} Low-Level Output Voltage

JEDEC – The voltage level at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

TI – The voltage level at an output terminal with input conditions applied that, according to the product specification, establishes a low level at the output.

V_{OL} is tested with input conditions that should cause the output under test to be at a low level. The output then is forced to sink the required current, as defined in the data sheet, and the output voltage is measured. The test is passed if the voltage is less than V_{OL} max. The input voltage levels used to precondition the device are V_{IL} max and V_{IH} min, as defined in the recommended operating conditions. See I_{OL} low-level output current for further information.

Helpful Hint:

Inclusion of a V_{OL} specification with a test condition of I_{OL} = 100 µA is done primarily to indicate that the device has CMOS outputs instead of bipolar (npn or pnp) drivers. Bipolar output transistors typically are not able to swing the output voltages all the way to the power-supply rail or ground rail, even under no-load or lightly loaded conditions. If the outputs were bipolar, this test condition would not apply and is not included in the data sheet. If you see this specification, you can safely assume the outputs to be of CMOS construction.

V_{OLS} Static Low-Level Output Voltage

JEDEC – *no definition offered*

TI – The static and testable voltage at a Dynamic Output Control (DOC circuitry) output with input conditions applied that, according to the product specifications, establishes a static low level at the output. The dynamic drive voltage is not specified for devices with DOC circuitry outputs because of its transient nature.

See I_{OLS} static low-level output current for further information.

For additional information about DOC circuitry, refer to the TI application report, *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

r_{on} On-State Resistance

JEDEC – The resistance between specified terminals with input conditions applied that, according to the product specification, will establish minimum resistance (the on-state) between those terminals.

TI – The resistance measured across the channel drain and source (or input and output) of a bus-switch device.

I_I Input Current

JEDEC – The current at the input terminals.

TI – The current into an input (current into a terminal is given as a positive value).

Helpful Hint:

CMOS inputs sink or source only minute amounts of current (commonly called leakage current) because of the behavior of standard CMOS technology, which is voltage controlled instead of current controlled. As a result, this parameter always should have a maximum specification no greater than a few tens of microamperes. For most bipolar inputs, which are current controlled instead of voltage controlled, a large amount of current is normal (a few milliamperes). In fact, a good method to determine if a device has a CMOS input is to examine its maximum input current specification: if this current is approximately the value of leakage current, typically, this means that it is a CMOS input.

Helpful Hint:

For the data signals of a device without bus-hold, the I_I specification includes both input and output leakage currents at the I/O pin. For devices that have bus-hold on the data signals, the I_I specification should apply only to the control inputs because the bus-hold output supplies enough current to overcome any internal input leakage.

An exception to this is an I_I specification for an overvoltage-tolerant bus-hold input with a test condition of $V_I >> V_{CC}$. This is used to indicate that the overvoltage-tolerant bus-hold output has a Schottky blocking diode in series with the output p-channel pullup transistor to V_{CC}, which prevents current from flowing from the output back into the V_{CC} supply. See $I_{I(hold)}$ and I_{off} for more information.

I_{IH} High-Level Input Current

JEDEC – The current into an input terminal when a specified high-level voltage is applied to that input.

TI – The current into an input when a high-level voltage is applied to that input.

Helpful Hint:

I_{IH} and I_{IL} typically are found only on devices with bipolar inputs that usually require a significantly different amount of pulldown current on the input to provide a logic low, rather than pullup current to provide a logic high. CMOS inputs usually have only leakage currents at the inputs and use the I_I parameter, but are measured at both low- and high-bias conditions.

I_{IL} Low-Level Input Current

JEDEC – The current into an input terminal when a specified low-level voltage is applied to that input.

TI – The current out of an input when a low-level voltage is applied to that input.

Helpful Hint:

I_{IH} and I_{IL} typically are found only on devices with bipolar inputs that usually require a significantly different amount of pulldown current on the input to provide a logic low, rather than pullup current to provide a logic high. CMOS inputs usually have only leakage currents at the inputs and use the I_I parameter.

$I_{I(hold)}$ Input Hold Current

JEDEC – *no definition offered*

TI – The input current that holds the input at the previous state when the driving device goes to the high-impedance state.

For additional information about the bus-hold feature, refer to the TI application report, *Bus-Hold Circuit*, literature number SCLA015.

Older technologies, such as ABT, LVT, LVC and ALVC (on devices that have the H option), specify this parameter. This parameter is measured with the minimum V_{CC} and an input bias voltage that is at V_{IH} min and V_{IL} max of the particular input threshold. For example, the ALVC family has a specified V_{IL} max of 0.7 V for a V_{CC} ranging from 2.3 V to 2.7 V, whereas its V_{IH} min is 1.7 V for the same supply voltage. Within a V_{CC} range of 2.7 V to 3.6 V, the input threshold for the ALVC family is V_{IH} min = 2 V and V_{IL} max = 0.8 V. Therefore, with V_{CC} = 2.3 V, $I_{I(hold)}$ is measured with the input voltage set to 0.7 V and 1.7 V. With a V_{CC} = 2.7 V (minimum V_{CC} of 2.3 V to 2.7 V), $I_{I(hold)}$ is measured with the input voltage set to 0.8 V and 2.0 V. This specification explicitly states the minimum amount of current the input structure sources or sinks, with input voltages set to the minimum threshold requirements of the device.

Another parameter that may be included with this $I_{I(hold)}$ specification is the maximum current the device can sink or source as the input transitions from one logic state to another. This maximum current is the minimum amount of drive capability that must be provided by the driver that is connected to this bus-hold input to switch the input stage to the other logic state. In newer technologies such as AVC, the parameters I_{BHH}, I_{BHL}, I_{BHHO}, and I_{BHLO} have been defined with their own separate specifications, but are identical in nature to those that are lumped with the $I_{I(hold)}$ parameter. Figure 26 is a representation of these bus-hold current measurements.

Helpful Hint:

The $I_{I(hold)}$ specification is not used in recent data sheets; instead, I_{BHH}, I_{BHL}, I_{BHHO}, and I_{BHLO} are used.

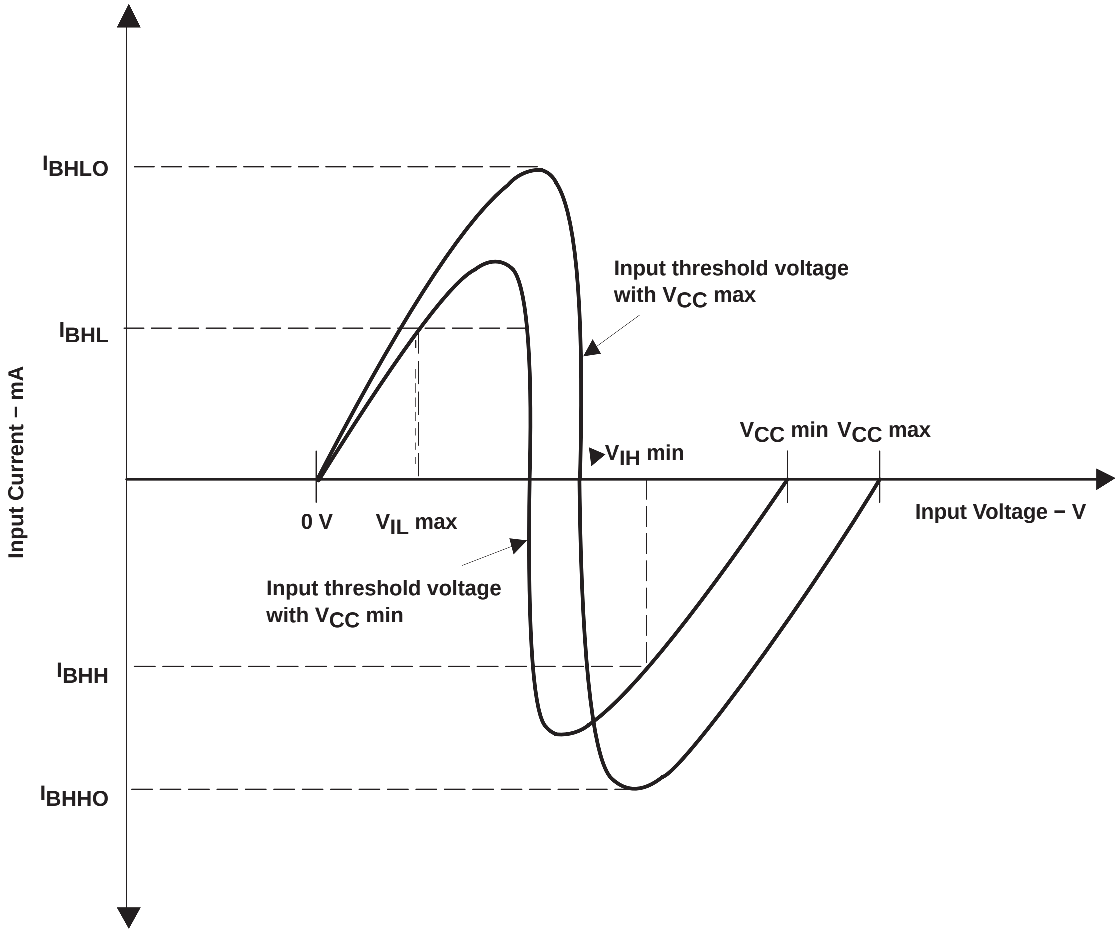


Figure 26. Bus-Hold Currents

I_{BHH} *Bus-Hold High Sustaining Current*

JEDEC – *no definition offered*

TI – The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising the input voltage to V_{CC}, then lowering it to V_{IH} min.

For additional information about the bus-hold feature, refer to the TI application report, *Bus-Hold Circuit*, literature number SCLA015. Also, see $I_{I(hold)}$ input hold current for further information.

I_{BHL} Bus-Hold Low Sustaining Current

JEDEC – *no definition offered*

TI – The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering the input voltage to GND and raising it to V_{IL} max.

For additional information about the bus-hold feature, refer to the TI application report, *Bus-Hold Circuit*, literature number SCLA015. Also, see $I_{I(hold)}$ input hold current for further information.

I_{BHHO} Bus-Hold High Overdrive Current

JEDEC – *no definition offered*

TI – The current that an external driver must sink to switch this node from high to low.

For additional information about the bus-hold feature, refer to the TI application report, *Bus-Hold Circuit*, literature number SCLA015. Also, see $I_{I(hold)}$ input hold current for further information.

I_{BHLO} Bus-Hold Low Overdrive Current

JEDEC – *no definition offered*

TI – The current that an external driver must source to switch this node from low to high.

For additional information about the bus-hold feature, refer to the TI application report, *Bus-Hold Circuit*, literature number SCLA015. Also, see $I_{I(hold)}$ input hold current for further information.

I_{off} Input/Output Power-Off Leakage Current

JEDEC – The current into a circuit node when the device or a portion of the device affecting that circuit node is in the off state.

TI – The maximum leakage current into an input or output terminal of the device, with the specified voltage applied to the terminal and V_{CC} = 0 V.

The I_{off} protection circuitry ensures that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specified voltage while the device is powered down, and is said to support partial-power-down mode of system operation. This condition can occur when subsections of a system are powered down (partial power down) to reduce power consumption. The TI logic families with the I_{off} feature that support partial power down are: AVC, LV, LVC, (CY)FCT, GTL, LS, ALS, and AUC.

All TI standard logic devices with I_{off} allow a maximum of approximately 100 µA to flow under these conditions. Any current in excess of this amount (a pn junction, for example, being forward biased) is not considered normal leakage current. Inherent in all CMOS designs are the parasitic diodes in all n-channel and p-channel FETs, which must be properly biased to prevent unwanted current paths. The output structure of a typical CMOS output is shown in Figure 27.

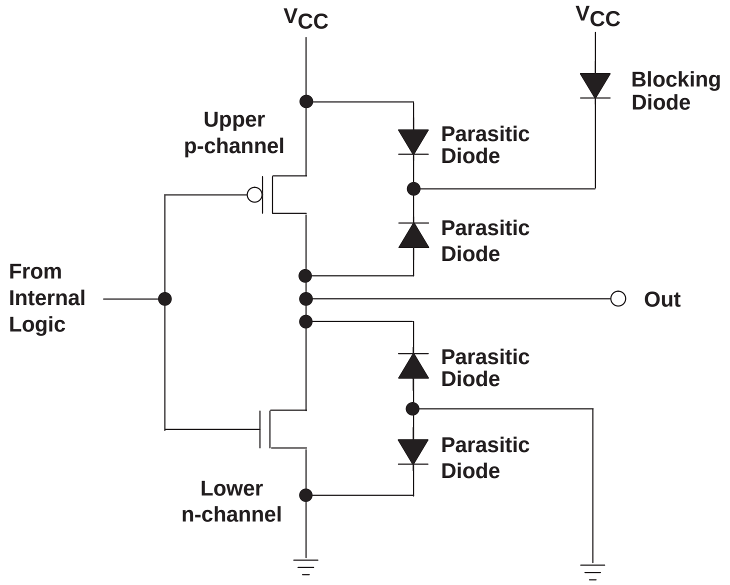


Figure 27. Typical CMOS Totem-Pole Output With I_{off}

The common cathode connection for the parasitic diodes on the p-channel MOS transistor is called the back gate and, typically, is tied to the highest potential on the device (V_{CC}, in the case of TI logic devices). For p-channel transistors, which are directly connected to external pins, the back gate is blocked with a diode to prevent excess currents flowing from the external pin to the supply-voltage V_{CC} when the output voltage is greater than V_{CC} by at least 0.7 V. This blocking diode is a subcircuit of the complete I_{off} circuitry found in several logic families, such as ABT and LVC. The other portion of the I_{off} circuit is not shown, but is, essentially, added FET circuitry that prevents the upper output p-channel from turning on during a partial-power-down event. The output n-channel, however, does not pose a problem because the parasitic diode already blocks current when the device is powered down and the output is biased high.

Figure 28 shows a typical CMOS input structure with bus-hold circuitry, which is essentially a weak latch that holds the previous state of the input inverter. The blocking diode is, again, required in the upper p-channel transistor that is connected to the external input pin. A non-bus-hold device does not require a blocking diode, as there is no p-channel source or drain connected to an external pin.

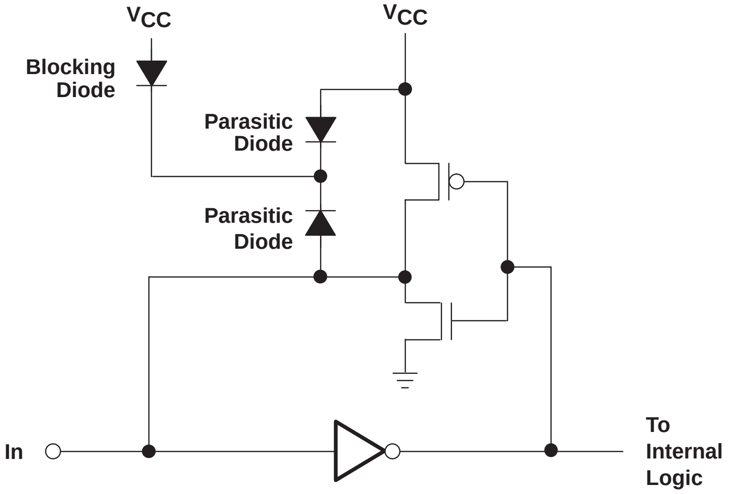


Figure 28. Typical CMOS Input With Bus-Hold and I_{off}

I_{OZ} *Off-State (High-Impedance State) Output Current (of a 3-State Output)*

JEDEC – *no definition offered*

TI – The current flowing into an output with the input conditions applied that, according to the product specification, establishes the high-impedance state at the output

TI data sheets specify currents flowing out of a device as a negative value.

The electrical characteristic, I_{OZ}, is verified utilizing the I_{OZH} and I_{OZL} tests. Two tests are required to verify the integrity of both the p- and n-channel transistors.

Helpful Hint:

For bidirectional (transceiver) devices that have bus hold on the data input/output pins, there should not be an I_{OZ} specification because the bus-hold output supplies enough current to overcome any internal output leakage.

An exception to this is an I_{OZH} specification for an overvoltage-tolerant bus-hold output with a test condition of $V_O >> V_{CC}$. This is used to indicate that the overvoltage-tolerant bus-hold output has a Schottky blocking diode in series with the output p-channel pullup transistor to V_{CC} and I_{off} circuitry, preventing the upper p-channel from turning on, which prevents current from flowing from the output back into the V_{CC} supply. See $I_{I(hold)}$ and I_{off} for more information.

I_{OZH} *Off-State Output Current With High-Level Voltage Applied*

JEDEC – *no definition offered*

TI – The current flowing into a 3-state output with input conditions established that, according to the product specification, will establish the high-impedance state at the output with a high-level voltage applied to the output.

This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled. I_{OZH} is tested by applying the specified voltage to the output and measuring the current into the device with the output in the high-impedance state. Input conditions that would establish a low level on the output if it were enabled are $V_{IL} = V_{IL}$ max and $V_{IH} = V_{IH}$ min. Each output is tested individually. For example, the unused inputs are at $V_{IL} = 0$ or $V_{IH} = V_{CC}$ for AC devices and $V_{IL} = 0$ or $V_{IH} = 3$ V for ACT devices, depending on the desired state of the outputs not being tested.

Helpful Hint:

An I_{OZH} specification on bidirectional (transceiver) devices with bus hold on the data input/output pins, with a test condition of $V_O >> V_{CC}$, indicates that the overvoltage-tolerant bus-hold output has a Schottky blocking diode in series with the output p-channel pullup transistor to V_{CC}. This diode prevents current flowing from the output back into the V_{CC} supply. See $I_{I(hold)}$ and I_{off} for more information.

I_{OZL} Off-State Output Current With Low-Level Voltage Applied

JEDEC – *no definition offered*

TI – The current flowing into a 3-state output with input conditions established that, according to the product specification, will establish the high-impedance state at the output, with a low-level voltage applied to the output.

This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled. I_{OZL} is tested by applying the specified voltage to the output and measuring the current into the device with the output in the high-impedance state. Input conditions that would establish a high level on the output if it were enabled are $V_{IL} = V_{IL}$ max and $V_{IH} = V_{IH}$ min. Each output is tested individually.

I_{OZPD} Power-Down Off-State (High-Impedance State) Output Current (of a 3-State Output)

JEDEC – *no definition offered*

TI – The current flowing into an output that is switched to or held in the high-impedance state as the device is being powered down to $V_{CC} = 0$ V.

TI data sheets specify currents flowing out of a device as a negative value.

Power-up 3-state (PU3S) circuitry is characterized by the parameters I_{OZPD} and I_{OZPU}. For hot-insertion support, I_{off}, and the addition of I_{OZPD} and I_{OZPU} are necessary. The TI logic families with the I_{off} and PU3S features that support hot insertion are: ABT (some), ALVT, BCT, LVT, and LVCZ.

While I_{off} is tested in a steady-state dc environment, PU3S is checked dynamically by ramping the power supply from 0 V to its maximum recommended value, then back to 0 V. The power-up and power-down ramp rates also affect the internal circuitry, but a ramp rate faster than 20 μs/V is not recommended for GTLP devices, for example, and slower than that (~200 μs/V) for older logic technologies. This ramp rate sometimes is specified as $\Delta t/\Delta V_{CC}$ in the *recommended operating conditions* section of the data sheet. Because typical power supplies power up within a few milliseconds (due, in part, to the enormous capacitance distributed throughout a PCB), the PU3S circuit should function properly in all applications.

PU3S circuitry disables the logic device outputs at a V_{CC} range of 0 V to a specified power-supply voltage trip point, regardless of the state of the output enable pin. At a certain guard-banded voltage above this supply voltage, the device will assert a voltage at the output, as indicated by its respective bit input-voltage logic level. This is true only if the voltage at the input of the output-enable pin enables the outputs during normal operation of the device. If the output is required to be in the high-impedance state while the device is being powered up or powered down throughout the entire range, the output-enable pin must be set to disable the output.

The voltage-versus-time plot shown in Figure 29 demonstrates how PU3S functions. As the device is being powered up, until it reaches the minimum V_{CC} supply voltage (labeled *Supply Trip Point* in Figure 29), the device output remains in the high-impedance state and remains at the pullup voltage, as defined by the load at the output. Once the internal PU3S circuitry determines that the supply voltage is slightly above this trip point, the device resumes normal functionality and enables the output. In this case, the input pin is such that the output goes low when enabled. The falling edge of the power-supply voltage shows similar results: just before V_{CC} reaches this trip point, the output is disabled.

For further information on power-up 3-state, refer to the TI application report, *Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices*, literature number SZZA033.

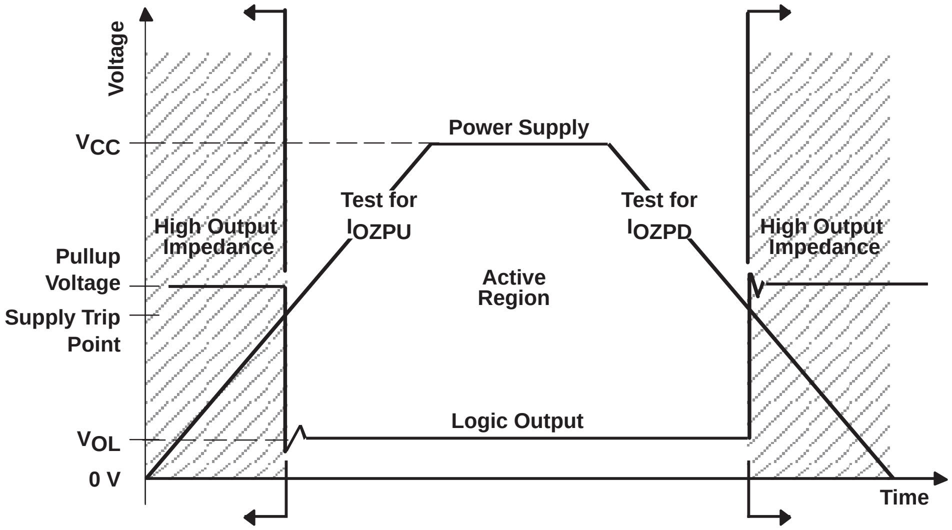


Figure 29. TI Logic Device I/O Text for I_{OZPU} and I_{OZPD}

I_{OZPU} Power-Up Off-State (High-Impedance State) Output Current (of a 3-State Output)

JEDEC – *no definition offered*

TI – The current flowing into an output that is switched to or held in the high-impedance state as the device is being powered up from V_{CC} = 0 V.

See I_{OZPD} power-down off-state output current for further information.

TI data sheets specify currents flowing out of a device as a negative value.

I_{CEX} Output High Leakage Current

JEDEC – *no definition offered*

TI – The maximum leakage current into an output that is in the high state and $V_O = V_{CC}$.

I_{CC} Supply Current

JEDEC – I_{CCH} is the current into a supply terminal of an integrated circuit when the output is (all outputs are) at a high-level voltage. I_{CCL} is the current into a supply terminal of an integrated circuit when the output is (all outputs are) at a low-level voltage.

TI – The current into the V_{CC} supply terminal of an integrated circuit.

This parameter is the current into the V_{CC} supply terminal of an integrated circuit under static no-load conditions. I_{CC} is tested by applying the specified V_{CC} level and measuring the current into the device.

The outputs of the device are left open, while all inputs—control and data—are biased to either V_{CC} or GND. For CMOS technologies, this is done to eliminate any current that may be caused by any input conditions or output loads.

ΔI_{CC} *Supply-Current Change*

JEDEC – *no definition offered*

TI – The increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

If n inputs are at voltages other than 0 V or V_{CC}, the increase in supply current will be $n \times I_{CC}$. The change in supply current (I_{CC}) is tested by applying the specified V_{CC} level, setting one input lower than V_{CC} (for example, V_{CC} – 0.6 V for LVC and ALVC devices) and all other inputs the same as the I_{CC} test, at 0 V or V_{CC}, then measuring the current into the device (see Figure 30). The outputs of the device are open, as well. The ΔI_{CC} specification typically is useful only on CMOS products that are designed to be operated at 5 V or 3.3 V because its purpose is to provide information about the supply-current performance of the CMOS device when driven by 5-V TTL signal levels.

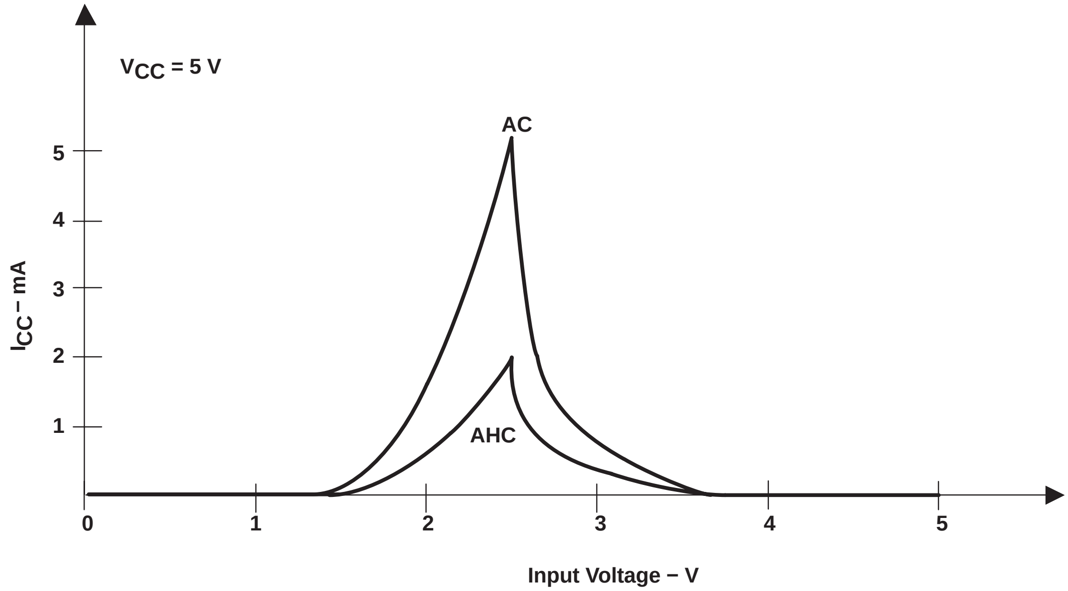


Figure 30. Example Typical AC and AHC I_{CC} vs Input Voltage

Helpful Hint:

Use the ΔI_{CC} specification as a reference when driving a CMOS device input with a TTL output driver.

Helpful Hint:

The ΔI_{CC} specification also demonstrates the high currents that can occur if V_{IH} and V_{IL} recommended operating conditions are not observed.

C_i *Input Capacitance*

JEDEC – *no definition offered*

TI – The capacitance of an input terminal of the device.

This parameter is the internal capacitance encountered at an input of the device. The values that are given are not production-tested values. Normally, they are typical values given for the benefit of the designer. These values are established by the design, process, and package of the device.

C_{io} *Input/Output Capacitance*

JEDEC – *no definition offered*

TI – The capacitance of an input/output (I/O) terminal of the device with the input conditions applied that, according to the product specification, establishes the high-impedance state at the output.

This parameter is the internal capacitance encountered at an input/output (I/O) of the device. The values that are given are not production-tested values. Normally, they are typical values given for the benefit of the designer. These values are established by the design, process, and package of the device.

C_o *Output Capacitance*

JEDEC – *no definition offered*

TI – The capacitance of an output terminal of the device with the input conditions applied that, according to the product specification, establishes the high-impedance state at the output.

This parameter is the internal capacitance encountered at an output of the device. The values that are given are not production-tested values. Normally, they are typical values given for the benefit of the designer. These values are defined by the design, process, and package of the device.

Live-Insertion Specifications

In addition to the following parameters, I_{off}, I_{OZPU}, and I_{OZPD} are specified in the live-insertion table because these parameters are necessary for live-insertion applications and typically are not stated in the *electrical characteristics section* of the data sheet, if already mentioned in this section.

I_{CC} *(BIAS* V_{CC}*) BIAS* V_{CC} *Current*

JEDEC – *no definition offered*

TI – This specification defines the maximum current at the BIAS V_{CC} pin during the ramp up or ramp down of the V_{CC} voltage.

V_O *Output Bias Voltage*

JEDEC – *no definition offered*

TI – This specification defines the range of voltages that will be applied to the output pin when the device is powered down.

I_O Output Bias Current

JEDEC – *no definition offered*

TI – This specification defines the minimum current measured at the output pin when the device is powered down.

Timing Requirements

f_{clock} Clock Frequency

JEDEC – *no definition offered*

TI – This specification defines the range of clock frequencies over which a bistable device can be operated while maintaining stable transitions between logic levels at the outputs.

The f_{clock} parameter is tested by driving the clock input with a predetermined number of pulses. The output then is checked for the correct number of output transitions corresponding to the number of input pulses applied. The output is loaded as defined in the data-sheet specifications. Each output is individually tested and not checked simultaneously with other recommended operating conditions or propagation delays. For counters, shift registers, or any other devices for which the state of the final output is dependent on the correct operation of the previous outputs, f_{clock} will be tested only on the final output, unless specified independently in the data sheet. Full functionality testing is not performed during f_{clock} testing or f_{max} testing.

Helpful Hint:

The f_{max} and f_{clock} parameters are two sides of the same coin. The f_{clock} parameter tells you, the user, how fast you can reliably switch the input to the device. The f_{max} parameter informs TI when to reject a device that fails to function below a minimum speed. If you are a device user, you should simply disregard the f_{max} specification and use the f_{clock} specification.

Helpful Hint:

For products that are not clocked (e.g., buffers and transceivers) for which you would like to know the maximum operating frequency, an estimate is the f_{clock} value from a comparable clocked part. For example, an LVC16245 maximum data frequency is conservatively similar to the LVC16374 maximum clock frequency. However, this is highly dependent upon load, and is a rule-of-thumb only.

t_w Pulse Duration (Width)

JEDEC – The time interval between the specified reference points on the two transitions of the pulse waveform.

TI – The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is specified (see Figure 31). Pulse duration is tested by applying a pulse to the specified input for a time period equal to the minimum specified in the data sheet. The device passes if the outputs switch to their expected logic levels and fails if they do not. Pulse-duration times are not checked simultaneously with other inputs or other recommended operating conditions.

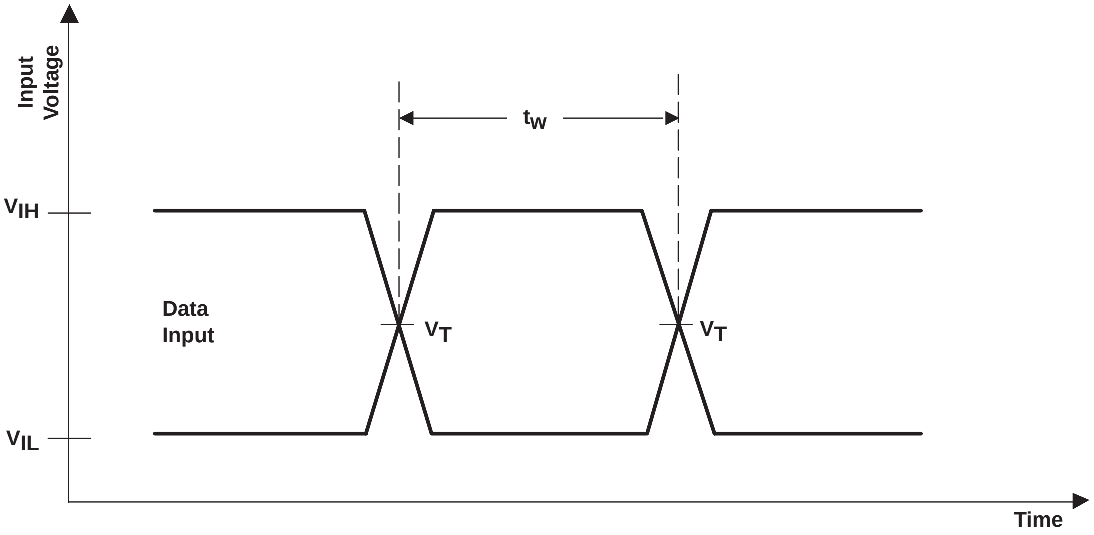


Figure 31. Pulse Duration

t_{su} *Setup Time*

JEDEC – The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

TI – The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.

NOTE: 1. The setup time is the time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is specified.

NOTE: 2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is specified.

Setup time is tested by switching an input to a fixed logic level at a specified time before the transition of the other input (see Figure 32). The device passes if the outputs switch to their expected logic levels and fails if they do not. Setup times are not checked simultaneously with other inputs or other recommended operating conditions. For additional information about setup time, refer to the TI application report, *Metastable Response in 5-V Logic Circuits*, literature number SDYA006.

t_h *Hold Time*

JEDEC – The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

TI – The time interval during which a signal is retained at a specified input after an active transition occurs at another specified input.

NOTE: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital signal operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

NOTE: 2. The hold time may have a negative value, in which case, the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

Hold time is tested by holding an input at a fixed logic level for the specified time after the transition of the other input (see Figure 32). The device passes if the outputs switch to their expected logic levels and fails if they do not. Hold times are not checked simultaneously with other inputs or other recommended operating conditions. For additional information about hold time, refer to the TI application report; *Metastable Response in 5-V Logic Circuits*, literature number SDYA006.

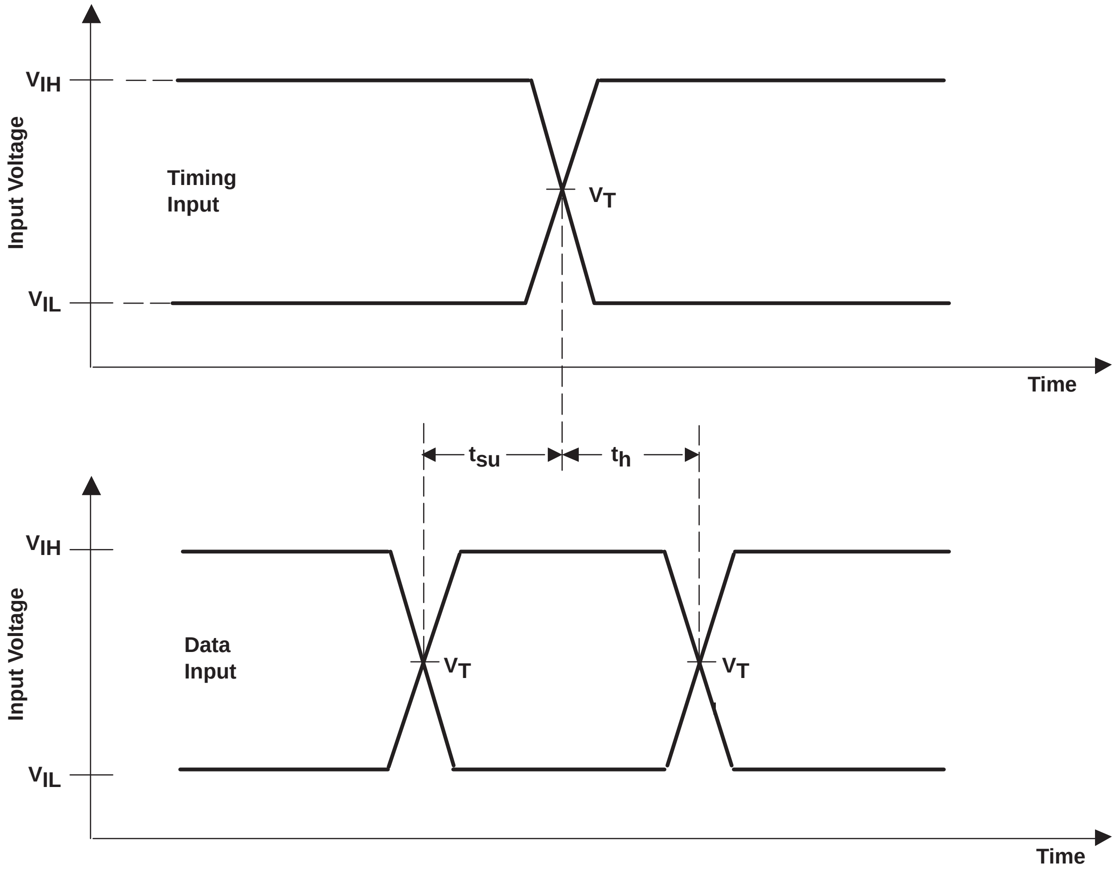


Figure 32. Setup and Hold Times

Switching Characteristics

f_{max} Maximum Clock Frequency

JEDEC – The highest frequency at which a clock input of an integrated circuit can be driven, while maintaining proper operation.

TI – The highest rate at which the clock input of a bistable circuit can be driven through its required sequence, while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

The f_{max} value is the value of the upper limit of the f_{clock} specification, and is specified in the data sheet as a minimum limit. The circuit is specified to operate up to the minimum frequency value. See f_{clock} for additional f_{max} testing information. Due to test-machine capability limitations, it may be necessary to test f_{max} or minimum recommended operating conditions (i.e., pulse duration, setup time, hold time) in accordance with the following paragraph.

The f_{max} parameter may be tested in either of two ways. One method is to test simultaneously the responses to the symmetrical clock-high and clock-low pulse durations that correspond to the period of the specified minimum value of f_{max}. The second method is to test individually the responses to the minimum clock-high and clock-low pulse durations under specified load conditions. A pulse generator is used to propagate a signal through the device to verify device operation with the minimum pulse duration. When clock-high and clock-low pulse durations are equal to or less than the corresponding f_{max} pulse duration, f_{max} testing suffices for testing clock-high and clock-low pulse durations.

Helpful Hint:

The f_{max} and f_{clock} parameters are two sides of the same coin. The f_{clock} parameter tells you, the user, how fast you can reliably switch the input to the device. The f_{max} parameter informs TI when to reject a device that fails to function below a minimum speed. If you are a device user, you should simply disregard the f_{max} specification and use the f_{clock} specification.

Helpful Hint:

For products that are not clocked (e.g., buffers and transceivers) for which you would like to know the maximum operating frequency, an estimate is the f_{clock} value from a comparable clocked part. For example, an LVC16245 maximum data frequency is conservatively similar to the LVC16374 maximum clock frequency. However, this is highly dependent upon load and is a rule-of-thumb only.

t_{pd} Propagation Delay Time

JEDEC – The time interval between specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

TI – The time between the specified reference points on the input and output voltage waveforms, with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH}).

A common misconception about logic devices is that the maximum data-signaling rate (or maximum frequency, as it is commonly misnamed) is equal to the inverse of the propagation delay. The maximum data rate on buffers is dependent on several factors, such as propagation delay matching, input sensitivity, and output edge rates. A device can have a high maximum signaling rate if the propagation delays from low-to-high and high-to-low are matched, the input is fast enough to respond to the fast data rate, and the output edge rate does not interfere with the low and high-level steady states. Clocked devices behave in the same manner, but now the set-up and hold times must be taken into account.

Helpful Hint:

The maximum value of t_{PD} simply is the worst case of t_{PHL} or t_{PLH}.

Helpful Hint:

Bus switch devices such as CBT and CBTLV typically are specified with a maximum limit of 0.25 ns. This limit is not a measured value, but is derived from the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

t_{PHL} Propagation Delay Time, High-Level to Low-Level Output

JEDEC – The time interval between specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

TI – The time between the specified reference points on the input and output voltage waveforms, with the output changing from the defined high level to the defined low level.

Propagation delay time, t_{PHL}, is tested by causing a transition on the specified input that causes the designated output to switch from a high logic level to a low logic level. For example, the transition applied is 0 V to V_{CC} or V_{CC} to 0 V for AC devices and 0 V to 3 V or 3 V to 0 for ACT devices. Trip points used for the timing measurements and output loads used during testing are defined in the individual data sheets in the *parameter measurement information* section, typically found after the *switching characteristics over recommended ranges of supply and operating free-air temperature* table. Propagation delay time, t_{PHL}, is not checked simultaneously with other outputs or with other recommended operating conditions. The time between the specified reference point on the input voltage waveform and the specified reference point on the output voltage waveform is measured.

t_{PLH} Propagation Delay Time, Low-Level to High-Level Output

JEDEC – The time interval between specified reference points on the input and output voltage waveforms with the specified output changing from the defined low level to the defined high level.

TI – The time between the specified reference points on the input and output voltage waveforms, with the output changing from the defined low level to the defined high level.

Propagation delay time, t_{PLH}, is tested by causing a transition on the specified input that causes the designated output to switch from a low logic level to a high logic level. For example, the transition applied is 0 V to V_{CC} or V_{CC} to 0 V for AC devices and 0 V to 3 V or 3 V to 0 for ACT devices. Trip points used for the timing measurements and output loads used during testing are defined in the individual data sheets in the *parameter measurement information* section, typically found after the *switching characteristics over recommended ranges of supply and operating free-air temperature* table. Propagation delay time, t_{PLH}, is not checked simultaneously with other outputs or with other recommended operating conditions. The time between the specified reference point on the input voltage waveform and the specified reference point on the output voltage waveform is measured.

t_{en} Enable Time (of a 3-State or Open-Collector Output)

JEDEC – The propagation time between specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

TI – The propagation time between the specified reference points on the input and output voltage waveforms, with the output changing from the high-impedance (off) state to either of the defined active levels (high or low).

NOTE: Open-collector outputs change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.

t_{PZH} *Enable Time (of a 3-State Output) to High Level*

JEDEC – The propagation time between specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to the defined high level.

TI – The time interval between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from the high-impedance (off) state to the defined high level.

This parameter is the propagation delay time between the specified reference point on the input voltage waveform and the specified reference point on the output voltage waveform, with the 3-state output changing from the high-impedance (off) state to the defined high level. Output enable time, t_{PZH}, is tested by generating a transition on the specified input that will cause the designated output to switch from the high-impedance state to a high logic level. Trip points used for the timing measurements and output loads used during testing are defined in the individual data sheets in the *parameter measurement information* section, typically found after the *switching characteristics over recommended ranges of supply and operating free-air temperature* table. Output enable time, t_{PZH}, is not checked simultaneously with other outputs or with other recommended operating conditions. Outputs not being tested should be set to a condition that minimizes switching currents. The tested output load includes a pulldown resistor to obtain a valid logic-low level when the output is in the high-impedance state.

t_{PZL} *Enable Time (of a 3-State Output) to Low Level*

JEDEC – The propagation time between specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to the defined low level.

TI – The time interval between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from the high-impedance (off) state to the defined low level.

This parameter is the propagation delay time between the specified reference point on the input voltage waveform and the specified reference point on the output voltage waveform, with the 3-state output changing from the high-impedance (off) state to the defined low level. Output enable time, t_{PZL}, is tested by generating a transition on the specified input that will cause the designated output to switch from the high-impedance state to a low logic level. Trip points used for the timing measurements and output loads used during testing are defined in the individual data sheets in the *parameter measurement information* section, typically found after the *switching characteristics over recommended ranges of supply and operating free-air temperature* table. Output enable time, t_{PZL}, is not checked simultaneously with other outputs or with other recommended operating conditions. Outputs not being tested should be set to a condition that minimizes switching currents. The tested output load includes a pullup resistor to obtain a valid logic-high level when the output is in the high-impedance state.

t_{dis} *Disable Time (of a 3-State or Open-Collector Output)*

JEDEC – *no definition offered*

TI – The propagation time between the specified reference points on the input and output voltage waveforms, with the output changing from either of the defined active levels (high or low) to the high-impedance (off) state.

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.

t_{PHZ} *Disable Time (of a 3-State Output) From High Level*

JEDEC – The propagation time between specified reference points on the input and output voltage waveforms with the output changing from the defined high level to a high-impedance (off) state.

TI – The time interval between the specified reference points on the input and the output voltage waveforms, with the 3-state output changing from the defined high level to the high-impedance (off) state.

t_{PLZ} *Disable Time (of a 3-State Output) From Low Level*

JEDEC – The propagation time between specified reference points on the input and output voltage waveforms with the output changing from the defined low level to a high-impedance (off) state.

TI – The time interval between the specified reference points on the input and the output voltage waveforms, with the 3-state output changing from the defined low level to the high-impedance (off) state.

t_f *Fall Time*

JEDEC – The time interval between one reference point on a waveform and a second reference point of smaller magnitude on the same waveform.

TI – The time interval between two reference points (90% and 10%, unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level.

t_r *Rise Time*

JEDEC – The time interval between one reference point on a waveform and a second reference point of greater magnitude on the same waveform.

TI – The time interval between two reference points (10% and 90%, unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level.

Slew Rate

JEDEC – *no definition offered*

TI – The voltage rate of change of an output ($\Delta V/\Delta t$).

$t_{sk(i)}$ *Input Skew*

JEDEC – The magnitude of the difference in propagation delay times between two inputs and a single output of an integrated circuit at identical operating conditions.

TI – The difference between any two propagation delay times that originate at different inputs and terminate at a single output. Input skew describes the ability of a device to manipulate (stretch, shrink, or chop) a clock signal. Typically, this is accomplished with a multiple-input gate wherein one of the inputs acts as a controlling signal to pass the clock through. $t_{sk(i)}$ describes the ability of the gate to shape the pulse to the same duration, regardless of the input used as the controlling input.

$t_{sk(l)}$ *Limit Skew*

JEDEC – The difference between (1) the greater of the maximum specified values of propagation delay times t_{PLH} and t_{PHL}, and (2) the lesser of the minimum specified values of propagation delay times t_{PLH} and t_{PHL}.

TI – The difference between: the greater of the maximum specified values of t_{PLH} and t_{PHL} and the lesser of the minimum specified values of t_{PLH} and t_{PHL}. Limit skew is not directly observed on a device. It is calculated from the data-sheet limits for t_{PLH} and t_{PHL}. $t_{sk(l)}$ quantifies for the designer how much variation in propagation delay time is induced by operation over the entire ranges of supply voltage, temperature, output load, and other specified operating conditions. Specified as such, $t_{sk(l)}$ also accounts for process variation. In fact, all other skew specifications ($t_{sk(o)}$, $t_{sk(i)}$, $t_{sk(p)}$, and $t_{sk(pr)}$) are subsets of $t_{sk(l)}$; they never are greater than $t_{sk(l)}$.

$t_{sk(o)}$ *Output Skew*

JEDEC – The skew time between two outputs of a single integrated circuit with all driving inputs switching simultaneously and the outputs switching in the same direction while driving identical loads.

TI – The skew between specified outputs of a single logic device, with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

$t_{sk(p)}$ *Pulse Skew*

JEDEC – The magnitude of the difference between the propagation delay times t_{PHL} and t_{PLH} when a single switching input causes one or more outputs to switch.

TI – The magnitude of the time difference between the propagation delay times, t_{PHL} and t_{PLH}, when a single switching input causes one or more outputs to switch.

$t_{sk(pr)}$ *Process Skew*

JEDEC – The part-to-part skew time between corresponding terminals of two samples of an integrated circuit from a single manufacturer.

TI –The magnitude of the difference in propagation delay times between corresponding terminals of two logic devices when both logic devices operate with the same supply voltages, operate at the same temperature, have identical package styles, have identical specified loads, have identical internal logic functions, and have the same manufacturer.

Helpful Hint:

Process variation is the only factor that affects process skew.

Noise Characteristics

$V_{OL(P)}$ Quiet Output, Maximum Dynamic V_{OL}

JEDEC – *no definition offered*

TI – The maximum positive voltage level at an output terminal with input conditions applied that, according to the product specification, establishes a low level at the specified output and a high-to-low transition at all other outputs.

Commonly called ringback, this parameter is the peak voltage of an output in the quiescent low condition, while all other outputs are switched from high to low (see Figure 33). Sometimes called a one-quiet-low test, this is a simultaneous switching measurement and indicates a device's noise performance due to power-rail and ground-rail bounce caused by the high peak currents during dynamic switching. $V_{OL(P)}$ also can apply to a switching output just after a high-to-low transition.

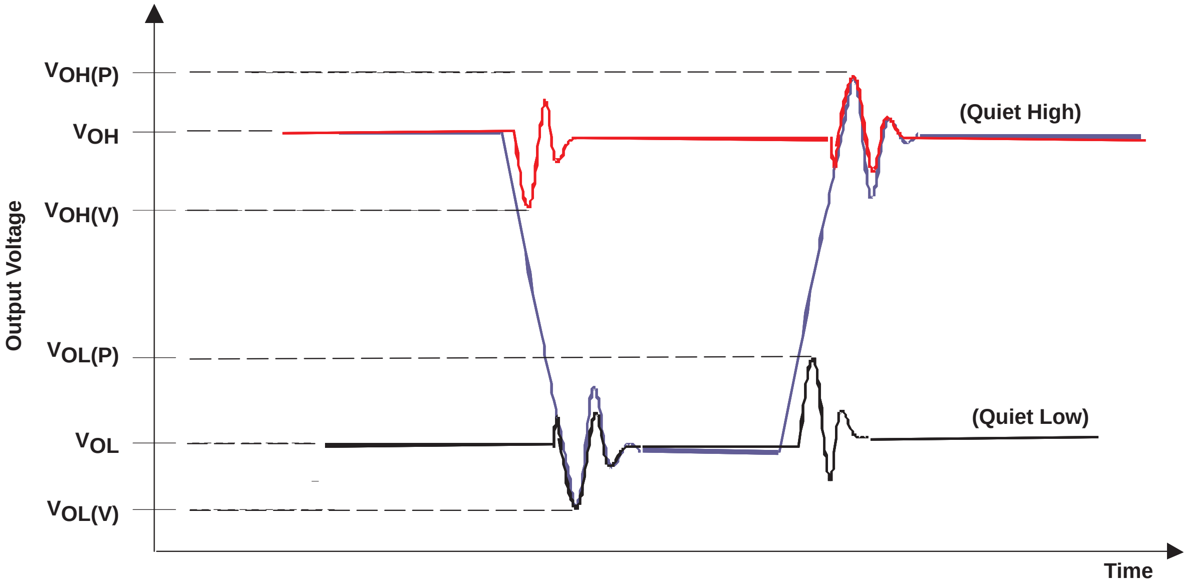


Figure 33. Output Noise Characteristics

$V_{OL(V)}$ Quiet Output, Minimum Dynamic V_{OL}

JEDEC – *no definition offered*

TI – The maximum negative voltage level at an output terminal with input conditions applied that, according to the product specification, establishes a low level at the specified output and a high-to-low transition at all other outputs.

Commonly called undershoot, this parameter is the valley voltage of an output in the quiescent low condition, while all other outputs are switched from high to low (see Figure 33). Sometimes called a one-quiet-low test, this is a simultaneous-switching measurement and indicates a device's noise performance due to power-rail and ground-rail bounce caused by the high peak currents during dynamic switching. $V_{OL(V)}$ also can apply to a switching output during a high-to-low transition.

$V_{OH(P)}$ Quiet Output, Maximum Dynamic V_{OH}

JEDEC – *no definition offered*

TI – The maximum positive voltage level at an output terminal with input conditions applied that, according to the product specification, establish a high level at the specified output and a low-to-high transition at all other outputs.

Commonly called overshoot, this parameter is the peak voltage of an output in the quiescent high condition, while all other outputs are switched from low to high (see Figure 33). Sometimes called a one-quiet-high test, this is a simultaneous-switching measurement and indicates a device's noise performance due to power-rail and ground-rail bounce caused by the high peak currents during dynamic switching. $V_{OH(P)}$ also can apply to a switching output during a low-to-high transition.

$V_{OH(V)}$ Quiet Output, Minimum Dynamic V_{OH}

JEDEC – *no definition offered*

TI – The minimum positive voltage level at an output terminal with input conditions applied that, according to the product specification, establishes a high level at the specified output and a low-to-high transition at all other outputs.

Commonly called ringback, this parameter is the valley voltage of an output in the quiescent high condition, while all other outputs are switched from low to high (see Figure 33). Sometimes called a one-quiet-high test, this is a simultaneous-switching measurement and indicates a device's noise performance due to power-rail and ground-rail bounce caused by the high peak currents during dynamic switching. $V_{OH(V)}$ also can apply to a switching output just after a low-to-high transition.

$V_{IH(D)}$ High-Level Dynamic Input Voltage

JEDEC – *no definition offered*

TI – An input voltage during dynamic switching conditions within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

High-level dynamic input voltage is a measurement of the shift of the input threshold due to noise generated while under the multiple-outputs-switching condition, with outputs operating in phase. This test is package and test-environment sensitive.

$V_{IL(D)}$ Low-Level Dynamic Input Voltage

JEDEC – *no definition offered*

TI – An input voltage during dynamic switching conditions within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

Low-level dynamic input voltage is a measurement of the shift of the input threshold due to noise generated while under the multiple-outputs-switching condition, with outputs operating in phase. This test is package and test-environment sensitive.

Operating Characteristics

C_{pd} Power-Dissipation Capacitance

JEDEC – *no definition offered*

TI – This parameter is the equivalent capacitance used to determine the no-load dynamic power dissipation per logic function for CMOS devices. $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$

The C_{pd} test is a measure of the dynamic power a device requires with a specific load. The values given on the data sheet are typical values that are not production tested. These values are defined by the design and process of the device. For more information on C_{pd}, refer to the TI application report, *CMOS Power Consumption and C_{pd} Calculation*, literature number SCAA035.

Parameter Measurement Information

The *parameter measurement information* (PMI) section of a data sheet is a graphical illustration of the test conditions used to characterize a logic device. Usually, this includes a load schematic, example waveforms with measurement points, and related notes. The PMI that is attached to each data sheet typically is a generic PMI for the entire logic family, and may include additional information that is not used for that specific device. For example, the *voltage waveforms for enable and disable times* (which are used on devices with 3-state outputs) may be included in the data sheet of a device without 3-state outputs. Therefore, this is superfluous information for that device and can be disregarded. The PMI may include the test information for multiple V_{CC}s in one page, with a table of test-load circuit and measurement point information, or the test information for each separate V_{CC} range at which the device operates may be in separate PMI pages, in which case the V_{CC} range will be stated at the top of the PMI illustration. Relevant load and test setup information also is included in the *footnotes* at the bottom of the PMI illustration.

Logic Compatibility

Logic compatibility has become more prevalent since the first 3.3-V logic devices were introduced into the market, thus creating an evolutionary trend in logic ICs. This trend demands that lower power-supply-voltage devices have the capability to communicate with older 5-V devices. In time, power-supply nodes have decreased even further mainly due to power-consumption reduction. This reduction in supply nodes, coupled with the fact that 5-V systems are not only still in use, but thriving, has forced logic manufacturers to provide logic devices that are compatible with technologies from several different output-voltage levels (see Table 3).

Table 3. Key Parameters per Technology for Logic Compatibility

TECHNOLOGY	PORT(S)	V_{CC} MIN (V)	I/O VOLTAGE TOLERANCE (V)	V_{IH} MIN (V)	V_{IL} MAX (V)	V_{OH} MIN AT GIVEN CURRENT (V)	V_{OL} MAX AT GIVEN CURRENT (V)
ABT	A and B	4.5	5	2	0.8	2.5 (at −3 mA)	Not specified
						2 (at −32 mA)	Not specified
						Not specified	0.55 (at 64 mA)
AHC	A and B	2	V_{CC} + 0.5	1.5	0.5	Not specified	
		3	V_{CC} + 0.5	2.1	0.9	2.48 (at −4 mA)	0.44 (at 4 mA)
		4.5	V_{CC} + 0.5	Not Specified		3.8 (at −8 mA)	0.44 (at 8 mA)
		5.5	V_{CC} + 0.5	3.85	1.65	Not specified	

NOTE: These values are general technology performance characteristics. Because these values are derived from standard ‘245 or ’16245 functions, carefully read the data sheet for each device for exact performance values.

Suppose you have created Table 3 above, which details the most important parameters discussed in the previous section that affect the compatibility of one device to another. Using the table to determine if a port from one technology is compatible to another, simply compare the V_{OH} min and V_{OL} max levels to the input threshold (V_{IH} min and V_{IL} max). If the output dc steady-state logic-high and logic-low voltage levels (V_{OH} and V_{OL}) are outside of the minimum V_{IH} and maximum V_{OL} range of an input port, then, in general, one can consider these two ports compatible (see Figure 34).

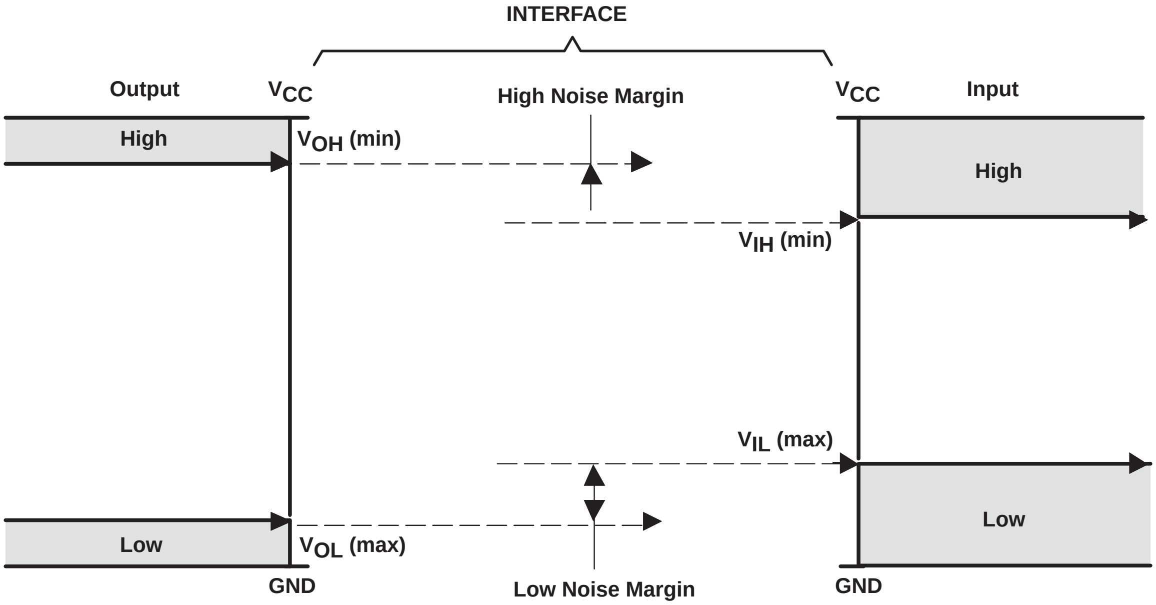


Figure 34. Logic Compatibility Between I/Os

For example, is the A-port output of an ABT device compatible with a B-port input of the same technology? Because the input of an ABT device is CMOS technology (I_I input current was discussed for determination of CMOS or bipolar input type), if it is connected in a point-to-point topology with an ABT output, the static dc current will be very low-leakage current range−and the V_{OH} level will not be lower than 2.5 V and the V_{OL} level will be no greater than 0.55 V. The input threshold to any ABT input port is set at the standard TTL/LVTTL threshold of 0.8 V – 2 V. Because the V_{OH} level of 2.5 V is greater than the minimum V_{IH} level of 2 V, and the V_{OL} level of 0.55 V is less than the maximum V_{IL} level of 0.8 V, these two ports are considered compatible.

Care must be taken when driving bipolar inputs because of the excessive currents at the input. If sufficiently large, the V_{OH} level could drop (or, conversely, the V_{OL} level could increase) to a level that violates the input threshold of the receiver.

Another major consideration is the voltage tolerance of the I/O structure. Simply because the previous conditions were satisfied, that does not mean I/Os are compatible. Take, for example, the same ABT output, which, if driving a CMOS input, will provide a V_{OH} level that will not be lower than 2.5 V and a V_{OL} level that will be no greater than 0.55 V, to drive an AHC input (which is CMOS) powered with a 3-V supply. The input threshold is met (i.e., 2.5 V > 2.1 V and 0.55 V < 0.9 V), but the I/O voltage tolerance is only 3.5 V (3 V + 0.5 V). An ABT output is very capable of producing voltage logic-high levels greater than 3.5 V; therefore, an ABT (5-V V_{CC}) output is not compatible to an AHC input powered with a 3-V supply.

Conclusion

The information in this application report is provided so that the designer can derive the maximum amount of information about standard-logic devices from the device data sheets. Texas Instruments provides this information to ease the task of the designer in incorporating standard-logic products into new system designs and upgrading legacy systems.

Acknowledgements

The authors thank Michael Cooper, Craig Spurlin, Mac McCaughey, and Sandi Denham for reviewing the document and providing meaningful feedback.

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2. *Semiconductor Group Packaging-Outlines Reference Guide*, literature number SSYU001, Texas Instruments.
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4. *CMOS Power Consumption and C_{pd} Calculation*, literature number SCAA035, Texas Instruments.
5. *Bus-Hold Circuit*, literature number SCLA015, Texas Instruments.
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7. *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*, literature number SCZA005, Texas Instruments.

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12. *Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices*, literature number SZZA033

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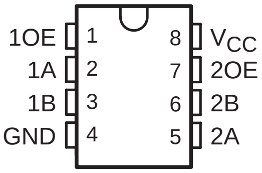
SN74CB3Q3305
DUAL FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

SCDS141A − OCTOBER 2003 − REVISED NOVEMBER 2003

- **High-Bandwidth Data Path (Up To 500 MHz[†])**
- **5-V Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 3 Ω Typical)**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
  - **0- to 3.3-V Switching With 2.5-V V_{CC}**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 3.5 pF Typical)**
- **Fast Switching Frequency (f_{OE} = 20 MHz Max)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 0.25 mA Typical)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface, Bus Isolation, Low-Distortion Signal Gating**

[†] For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CB3Q3305 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3305 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

ORDERING INFORMATION

T_A	PACKAGE[‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TSSOP − PW	Tube	SN74CB3Q3305PW	BU305
		Tape and reel	SN74CB3Q3305PWR	

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The SN74CB3Q3305 is organized as two 1-bit switches with separate output-enable (1OE, 2OE) inputs. It can be used as two 1-bit bus switches, or as one 2-bit bus switch. When OE is high, the associated 1-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is low, the associated 1-bit bus switch is OFF and a high-impedance state exists between the A and B ports.

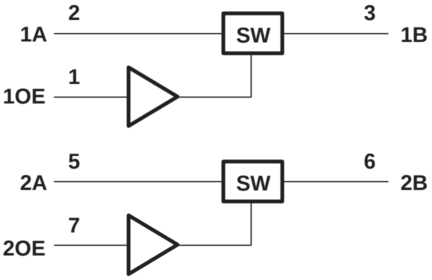
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

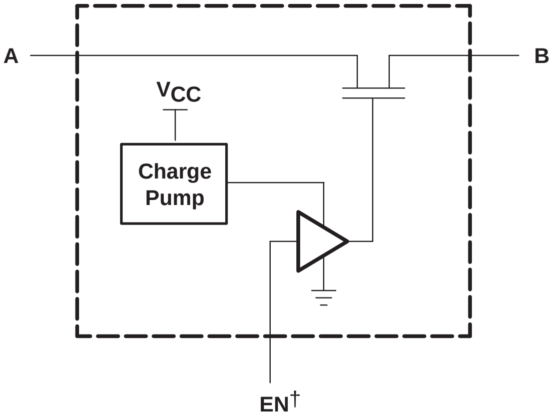
FUNCTION TABLE
(each bus switch)

INPUT OE	INPUT/OUTPUT A	FUNCTION
H	B	A port = B port
L	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±64 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5)	88°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA				−1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	µA
I_{OZ}‡		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		0.25	0.7	mA
ΔI_{CC}§	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			25	µA
I_{CCD}¶	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,			0.040	0.045	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		3.5	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		8	10.5	pF
r_{on}#		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		3	8	Ω
			V_I = 1.7 V,	I_O = −15 mA		3.5	9	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		3.5	8	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

¶ This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

# Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
f_{OE}‖	OE	A or B		10		20	MHz
t_{pd}☆	A or B	B or A		0.09		0.15	ns
t_{en}	OE	A or B	1	5	1	4.5	ns
t_{dis}	OE	A or B	1	4.5	1	5	ns

‖ Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1$ MΩ, C_L = 0)

☆ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

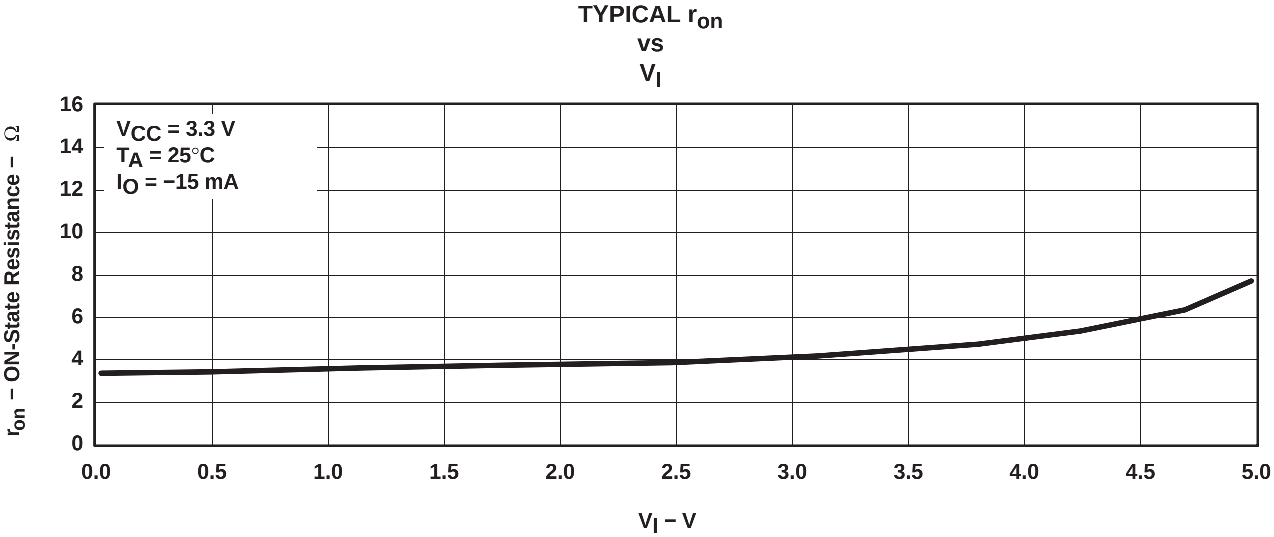


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

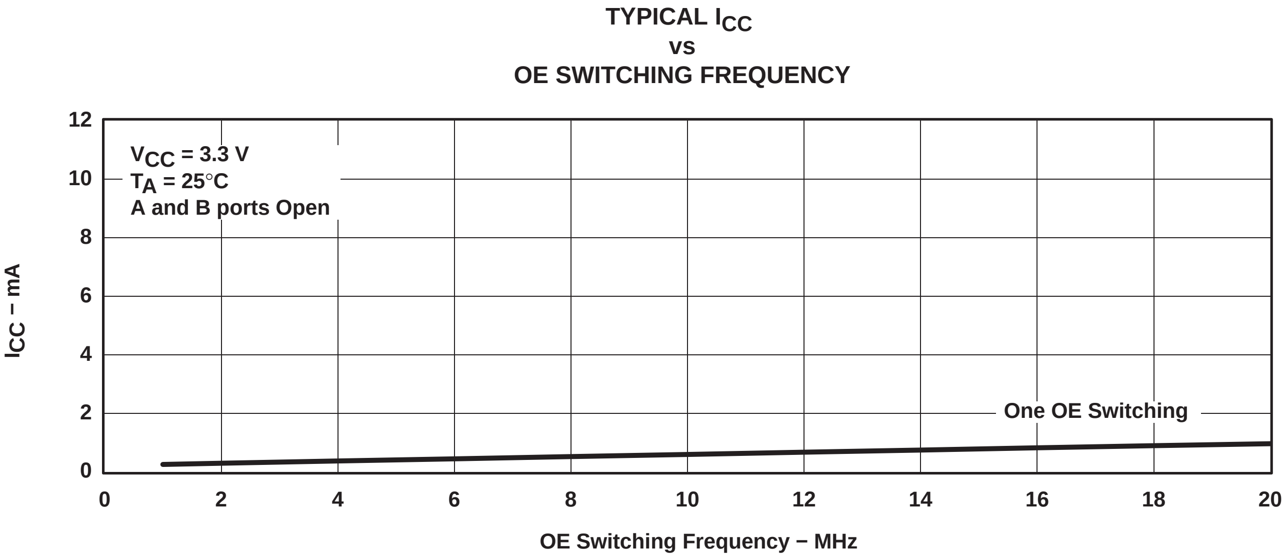
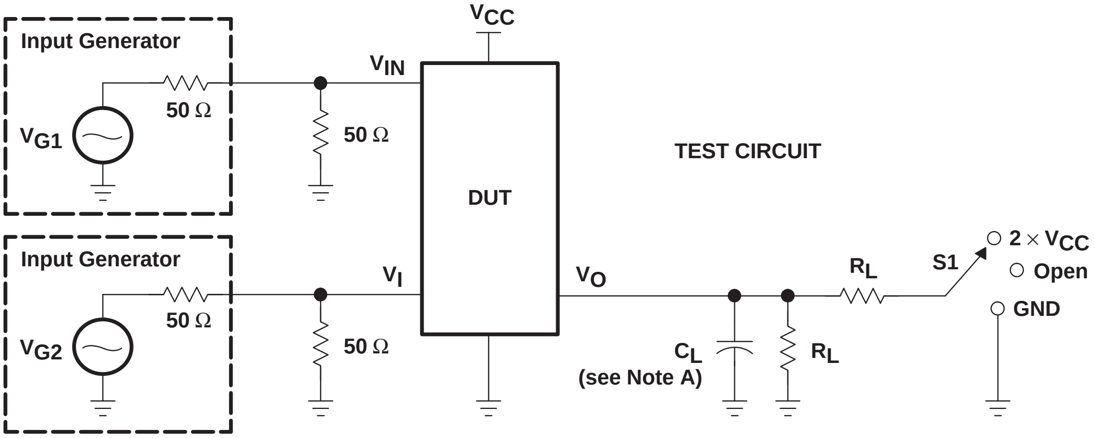
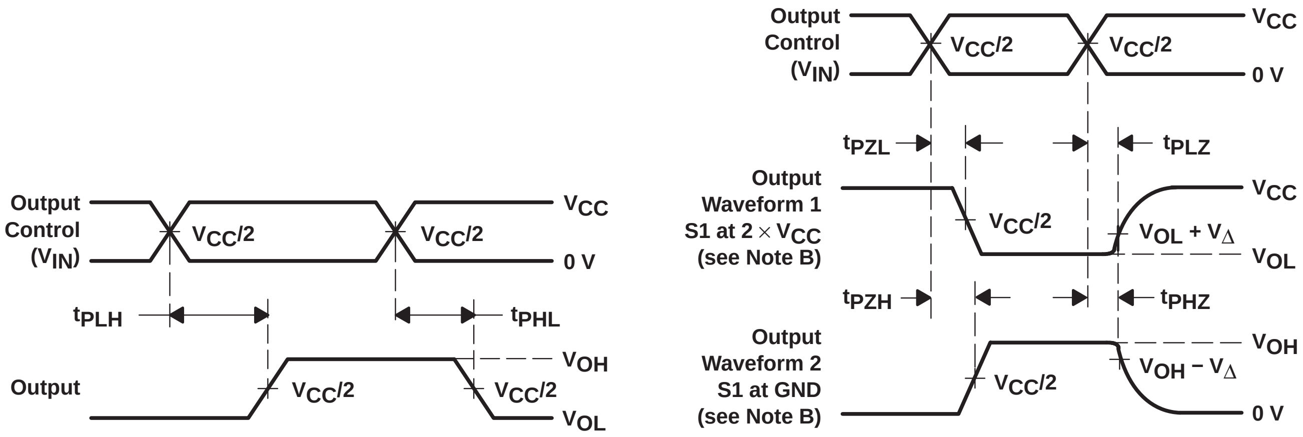


Figure 2. Typical I_{CC} vs OE Switching Frequency, V_{CC} = 3.3 V

PARAMETER MEASUREMENT INFORMATION


V_{CC}
Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

SN74CB3Q3306A
DUAL FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE, HIGH-BANDWIDTH BUS SWITCH

SCDS113D − DECEMBER 2002 − REVISED NOVEMBER 2003

- **High-Bandwidth Data Path (Up to 500 MHz[†])**
- **5-V Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 4 Ω Typical)**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
  - **0- to 3.3-V Switching With 2.5-V V_{CC}**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 3.5 pF Typical)**
- **Fast Switching Frequency ($f_{\overline{OE}}$ = 20 MHz Max)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 0.25 mA Typical)**
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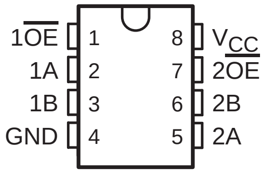
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface, Bus Isolation, Low-Distortion Signal Gating**

[†] For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CB3Q3306A is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3306A provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

ORDERING INFORMATION

T_A	PACKAGE[‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TSSOP − PW	Tube	SN74CB3Q3306APW	BU306A
		Tape and reel	SN74CB3Q3306APWR	

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The SN74CB3Q3306A is organized as two 1-bit switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. It can be used as two 1-bit bus switches, or as one 2-bit bus switch. When $\overline{OE}$ is low, the associated 1-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 1-bit bus switch is OFF and a high-impedance state exists between the A and B ports.

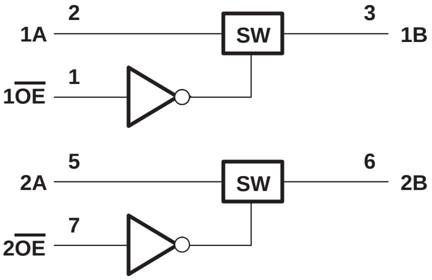
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

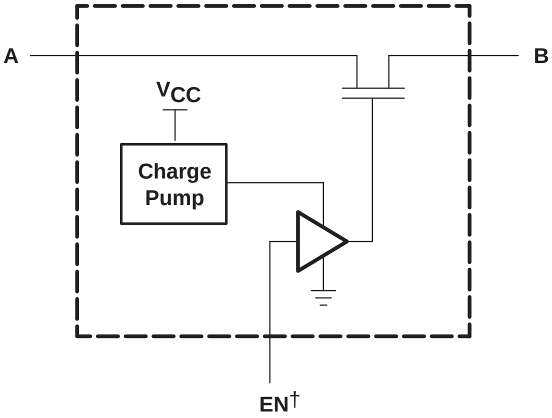
FUNCTION TABLE
(each bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±64 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5)	88°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA				−1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	μA
I_{OZ}[‡]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	μA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		0.25	0.7	mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			25	μA
I_{CCD}[¶]	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,			0.03	0.1	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		3.5	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		8	10.5	pF
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		4	8	Ω
			V_I = 1.7 V,	I_O = −15 mA		5	9	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		4	6	
			V_I = 2.4 V,	I_O = −15 mA		5	8	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$[‖]	$\overline{OE}$	A or B		10		20	MHz
t_{pd}[☆]	A or B	B or A		0.2		0.2	ns
t_{en}	$\overline{OE}$	A or B	1.5	6.5	1.5	5.5	ns
t_{dis}	$\overline{OE}$	A or B	1	6	1	5	ns

[‖] Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1$ MΩ, C_L = 0)

[☆] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

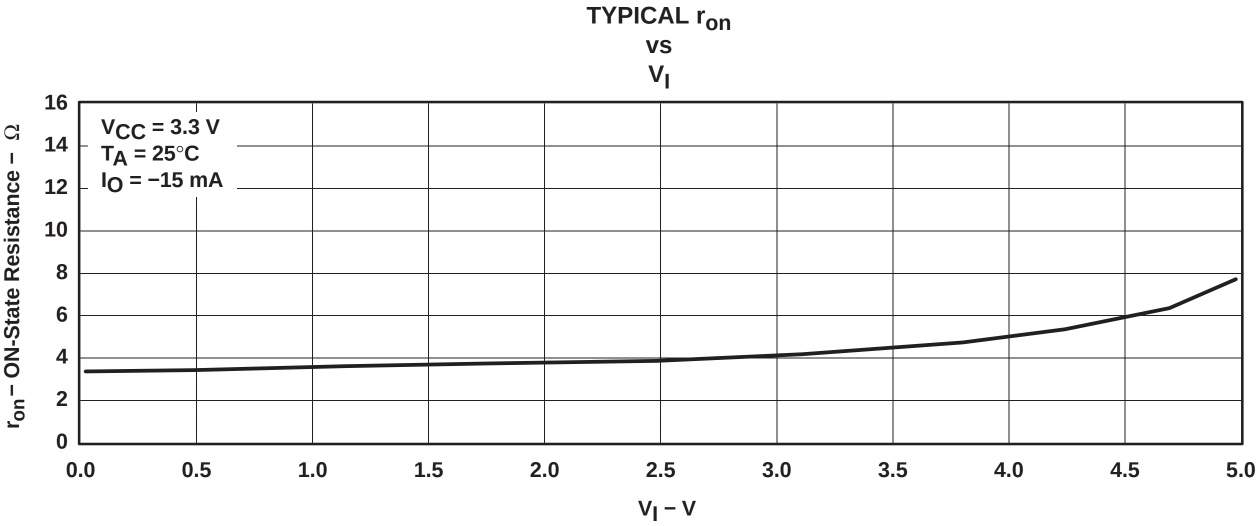


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

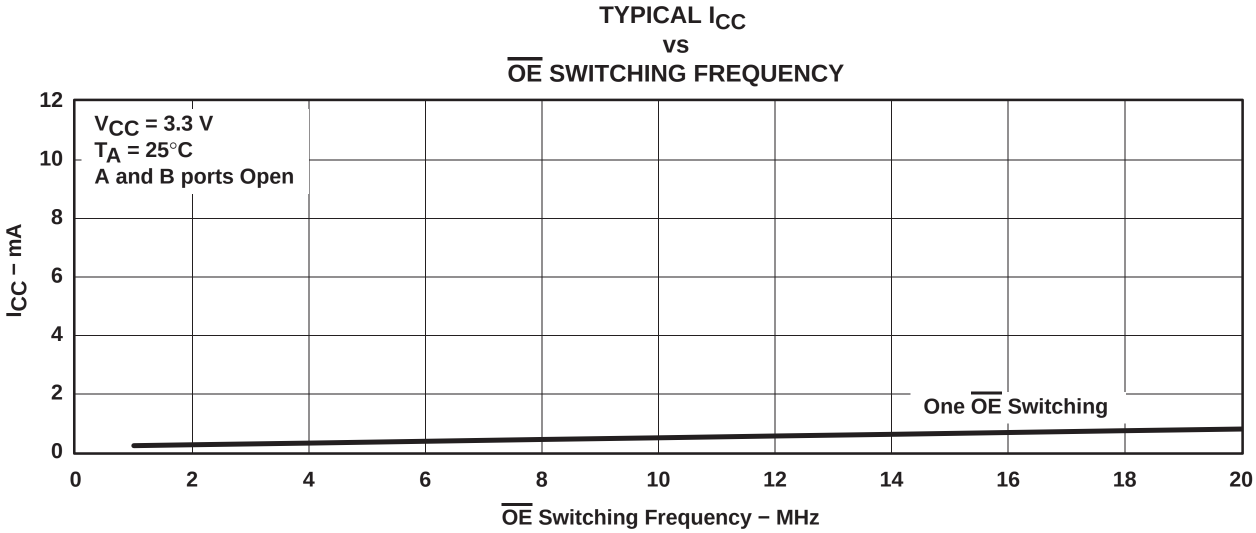
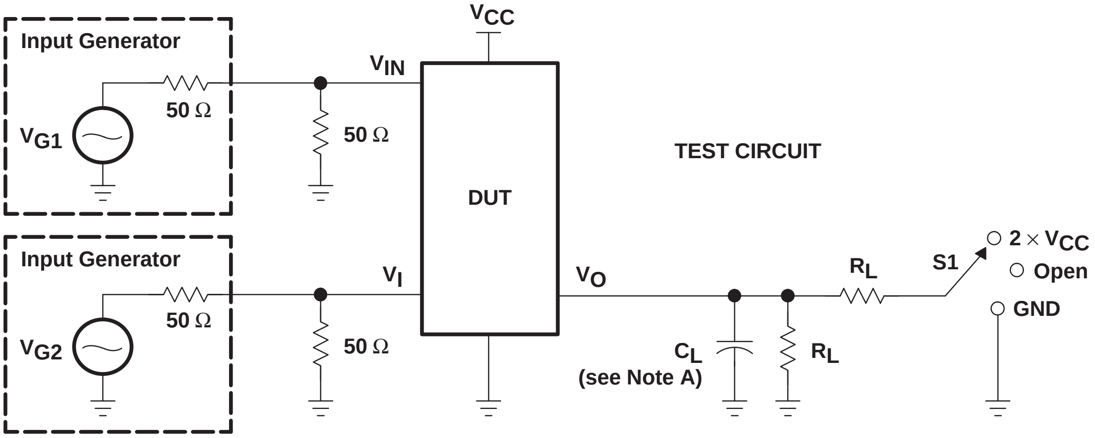
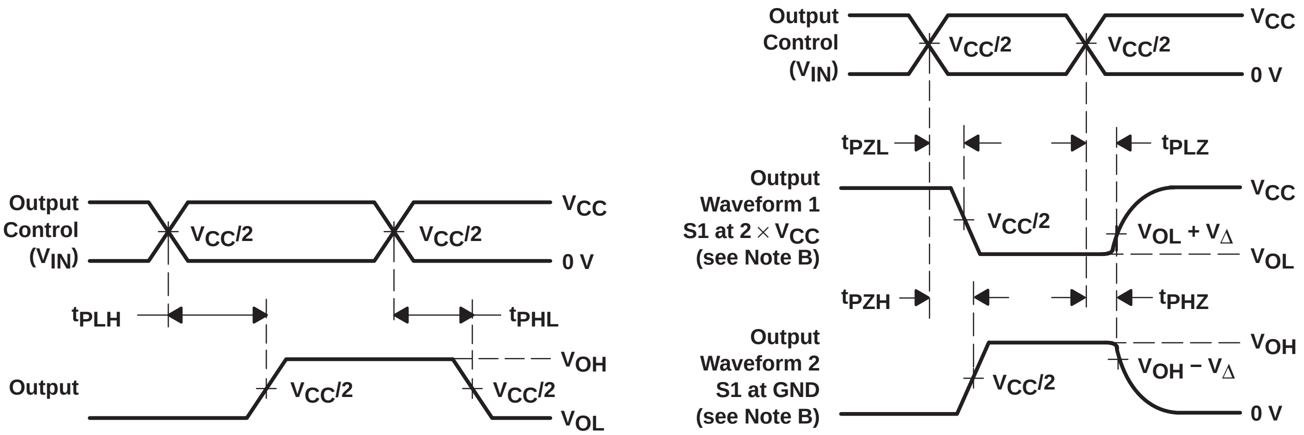


Figure 2. Typical I_{CC} vs $\overline{OE}$ Switching Frequency, V_{CC} = 3.3 V

PARAMETER MEASUREMENT INFORMATION


VCC
Input Generator
VG1
50 Ω
VIN
50 Ω
DUT
TEST CIRCUIT
Input Generator
VG2
50 Ω
VI
50 Ω
VO
CL
(see Note A)
RL
RL
S1
2 × VCC
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V


Output Control (VIN)
VCC/2
VCC/2
VCC
0 V
tPLH
tPHL
Output
VCC/2
VCC/2
VOH
VOL
Output Control (VIN)
VCC/2
VCC/2
VCC
0 V
tPZL
tPLZ
Output Waveform 1 S1 at 2 × VCC (see Note B)
VCC/2
VOL + VΔ
VCC
VOL
tPZH
tPHZ
Output Waveform 2 S1 at GND (see Note B)
VCC/2
VOH − VΔ
VOH
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

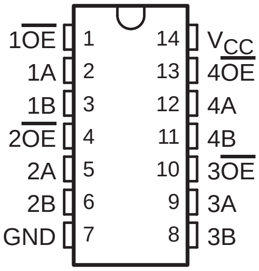
SN74CB3Q3125
QUADRUPLE FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

SCDS143A – OCTOBER 2003 − REVISED NOVEMBER 2003

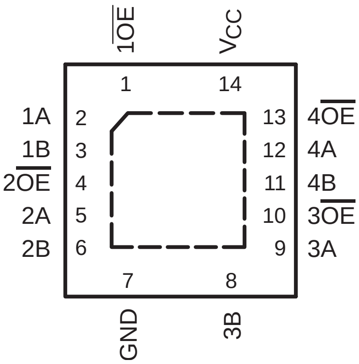
- **High-Bandwidth Data Path (Up To 500 MHz[†])**
- **5-V Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 3 Ω Typical)**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
  - **0- to 3.3-V Switching With 2.5-V V_{CC}**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 4 pF Typical)**
- **Fast Switching Frequency ($f_{\overline{OE}}$ = 20 MHz Max)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 0.3 mA Typical)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface, Bus Isolation, Low-Distortion Signal Gating**

[†] For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

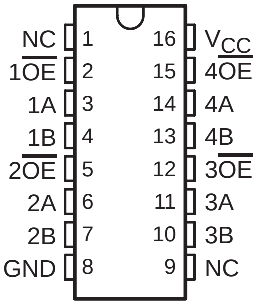
DGV OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



DBQ PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The SN74CB3Q3125 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3125 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

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description/ordering information (continued)

The SN74CB3Q3125 is organized as four 1-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$) inputs. It can be used as four 1-bit bus switches, or as one 4-bit bus switch. When $\overline{OE}$ is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

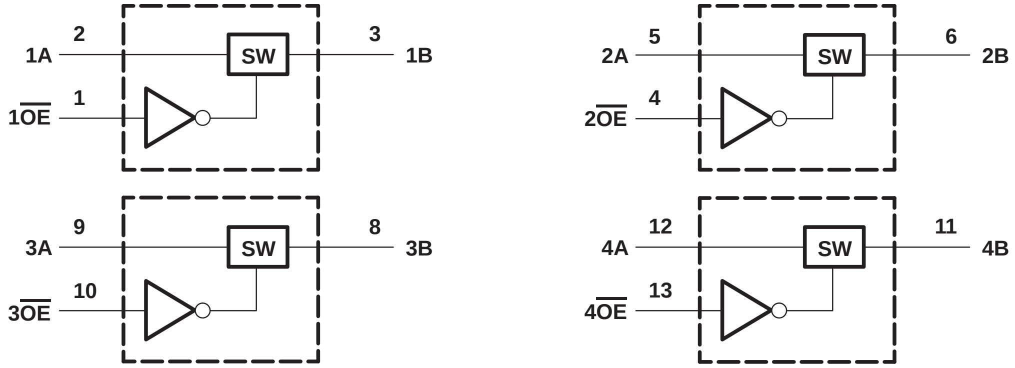
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CB3Q3125RGYR	BU125
	SSOP (QSOP) − DBQ	Tape and reel	SN74CB3Q3125DBQR	BU125
	TSSOP − PW	Tube	SN74CB3Q3125PW	BU125
		Tape and reel	SN74CB3Q3125PWR	
	TVSOP − DGV	Tape and reel	SN74CB3Q3125DGVR	BU125

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each bus switch)

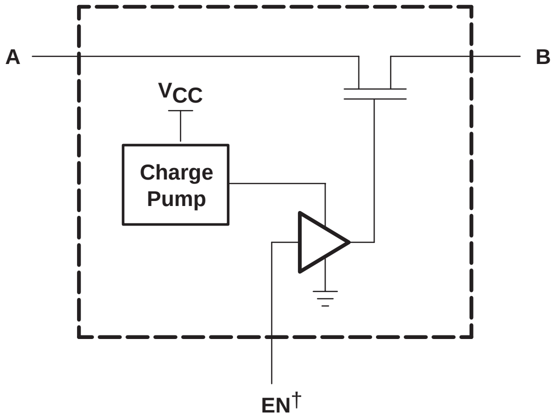
INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



Pin numbers shown are for the DGV, PW, and RGY packages.

simplified schematic, each FET switch (SW)



[†] EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} (V_{IN} < 0)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O}$ < 0)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±64 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DBQ package	90°C/W
(see Note 5): DGV package	127°C/W
(see Note 5): PW package	113°C/W
(see Note 6): RGY package	47°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

[‡] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA				−1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	μA
I_{OZ}[‡]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	μA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		0.3	1	mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			30	μA
I_{CCD}[¶]	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,			0.04	0.2	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		4	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		8	10	pF
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		4	8	Ω
			V_I = 1.7 V,	I_O = −15 mA		4	9	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		4	6	
			V_I = 2.4 V,	I_O = −15 mA		4	8	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$[∥]	$\overline{OE}$	A or B		10		20	MHz
t_{pd}[☆]	A or B	B or A		0.12		0.2	ns
t_{en}	$\overline{OE}$	A or B	1.5	6.7	1.5	6.6	ns
t_{dis}	$\overline{OE}$	A or B	1	4.6	1	5.3	ns

[∥] Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1\ M\Omega$, C_L = 0)

[☆] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

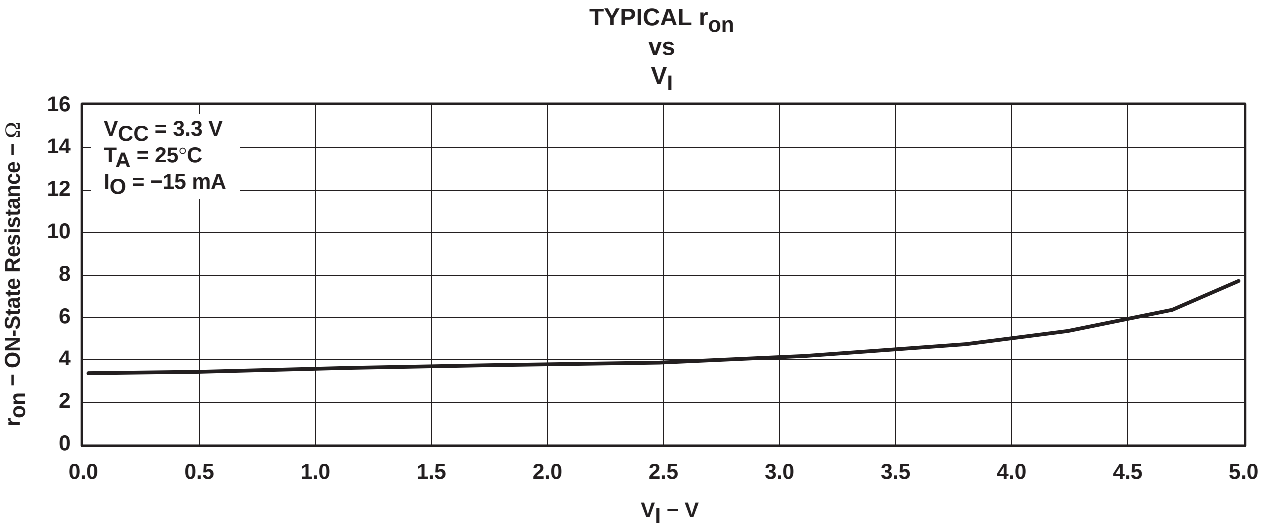


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

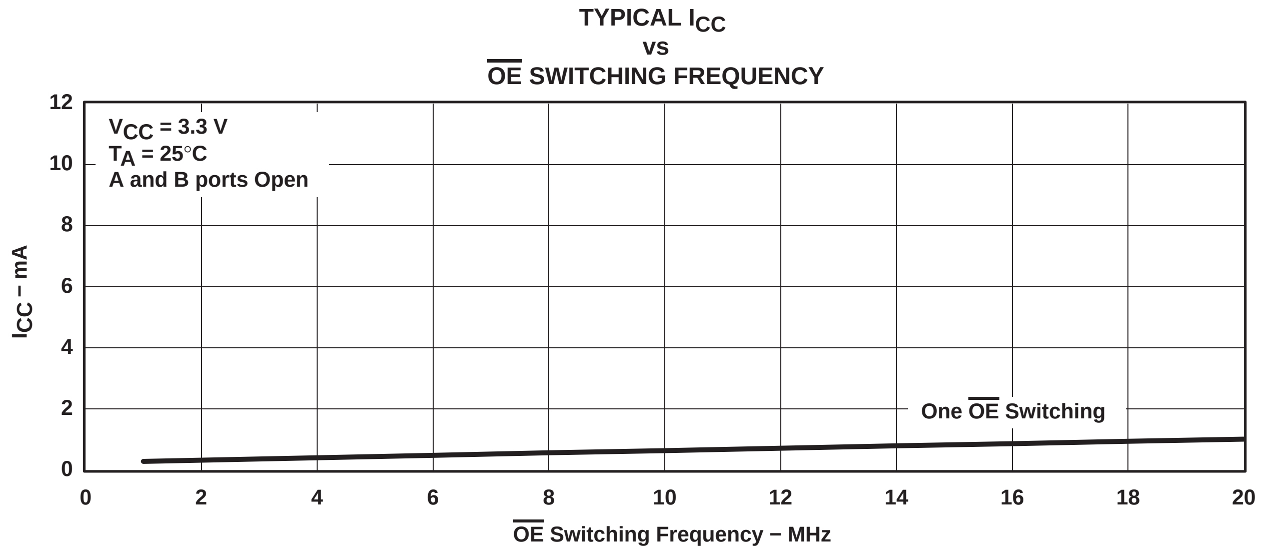
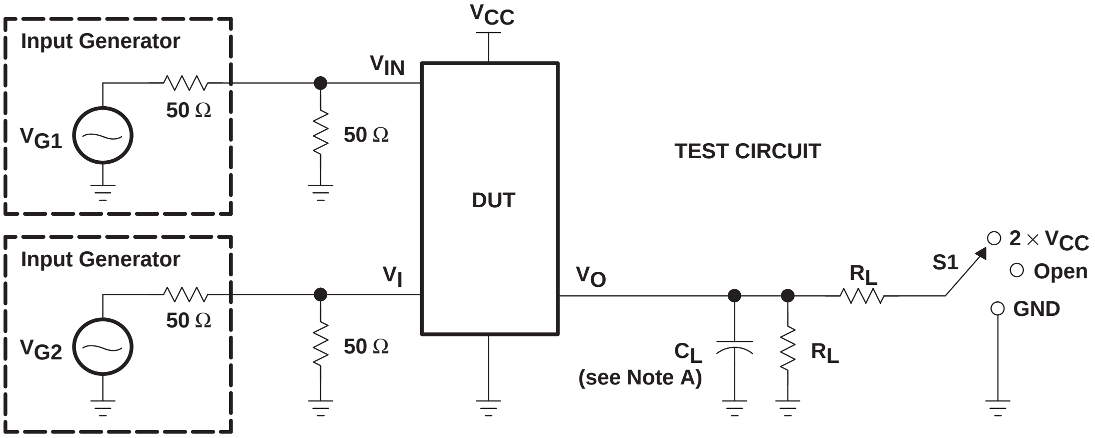
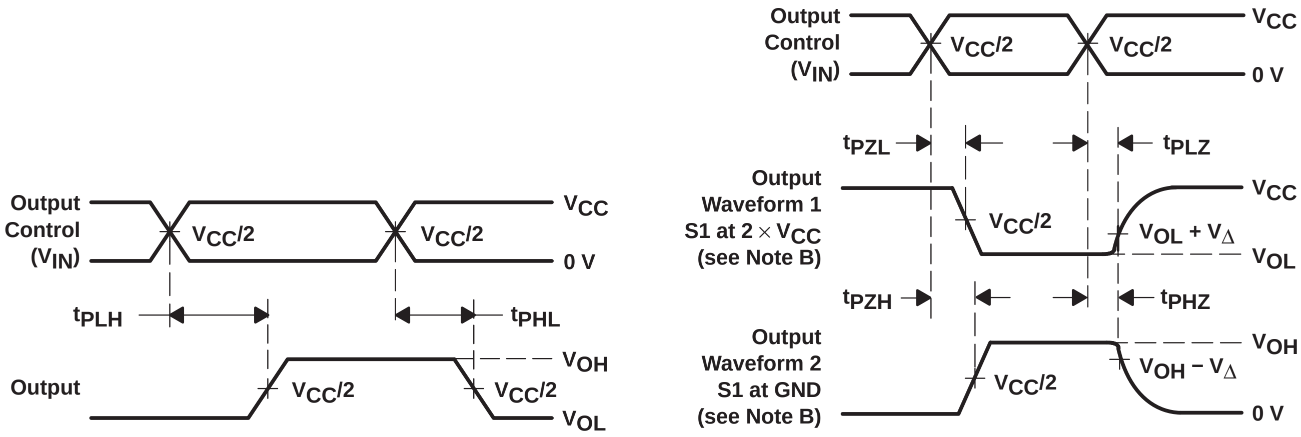


Figure 2. Typical I_{CC} vs $\overline{OE}$ Switching Frequency, V_{CC} = 3.3 V

PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
50 Ω
V_{IN}
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
50 Ω
V_I
V_O
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_{Δ}
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
$V_{OL} + V_{\Delta}$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
$V_{OH} - V_{\Delta}$
V_{OH}
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

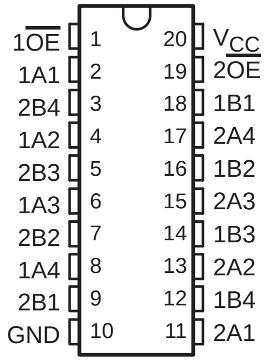
SN74CB3Q3244
8-BIT FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

SCDS154A − OCTOBER 2003 − REVISED NOVEMBER 2003

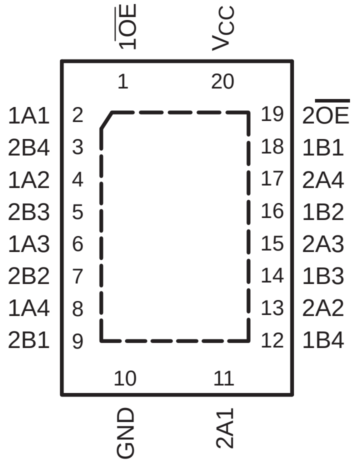
- **High-Bandwidth Data Path (Up To 500 MHz[†])**
- **5-V-Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
  - **0- to 3.3-V Switching With 2.5-V V_{CC}**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion**
- **Fast Switching Frequency**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

[†] For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)


1$\overline{\text{OE}}$ 1
1A1 2
2B4 3
1A2 4
2B3 5
1A3 6
2B2 7
1A4 8
2B1 9
GND 10
20 V_{CC}
19 2$\overline{\text{OE}}$
18 1B1
17 2A4
16 1B2
15 2A3
14 1B3
13 2A2
12 1B4
11 2A1

RGY PACKAGE
(TOP VIEW)


1$\overline{\text{OE}}$
V_{CC}
1
20
1A1 2
2B4 3
1A2 4
2B3 5
1A3 6
2B2 7
1A4 8
2B1 9
19 2$\overline{\text{OE}}$
18 1B1
17 2A4
16 1B2
15 2A3
14 1B3
13 2A2
12 1B4
10
11
GND
2A1

PRODUCT PREVIEW

description/ordering information

The SN74CB3Q3244 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3244 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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PRODUCT PREVIEW

description/ordering information (continued)

The SN74CB3Q3244 is organized as two 4-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. It can be used as two 4-bit bus switches or as one 8-bit bus switch. When $\overline{OE}$ is low, the associated 4-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 4-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

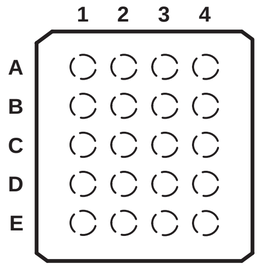
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CB3Q3244RGYR	
	SOIC − DW	Tube	SN74CB3Q3244DW	
		Tape and reel	SN74CB3Q3244DWR	
	SSOP − DB	Tape and reel	SN74CB3Q3244DBR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CB3Q3244DBQR	
	TSSOP − PW	Tape and reel	SN74CB3Q3244PWR	
	TVSOP − DGV	Tape and reel	SN74CB3Q3244DGVR	
	VFBGA − GQN	Tape and reel	SN74CB3Q3244GQNR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

GQN PACKAGE
(TOP VIEW)



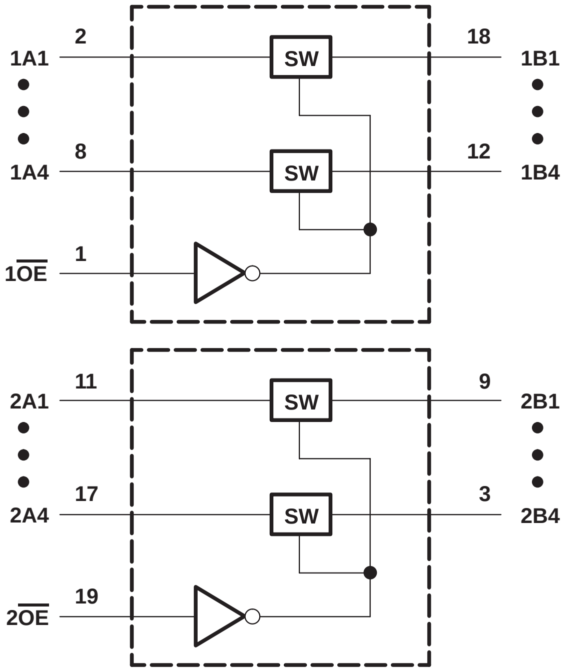
terminal assignments

	1	2	3	4
A	1A1	$1\overline{OE}$	V_{CC}	$2\overline{OE}$
B	1A2	2A4	2B4	1B1
C	1A3	2B3	2A3	1B2
D	1A4	2A2	2B2	1B3
E	GND	2B1	2A1	1B4

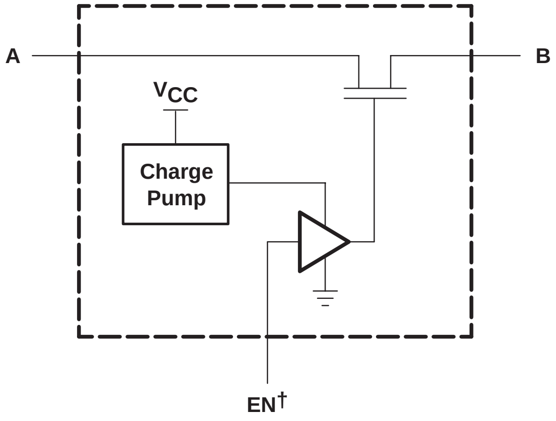
FUNCTION TABLE
(each 4-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)


1A1
2
SW
18
1B1
1A4
8
SW
12
1B4
1OE
1
2A1
11
SW
9
2B1
2A4
17
SW
3
2B4
2OE
19

simplified schematic, each FET switch (SW)


A
B
V_{CC}
Charge Pump
EN†

† EN is the internal enable signal applied to the switch.

PRODUCT PREVIEW

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . −0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$) . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$) . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . ±64 mA
Continuous current through V_{CC} or GND terminals . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DB package . . . . 70°C/W
(see Note 5): DBQ package . . . . 68°C/W
(see Note 5): DGV package . . . . 92°C/W
(see Note 5): DW package . . . . 58°C/W
(see Note 5): GQN package . . . . 78°C/W
(see Note 5): PW package . . . . 83°C/W
(see Note 6): RGY package . . . . 37°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA					V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V					µA
I_{OZ}[‡]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND				µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0				µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND				mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND				µA
I_{CCD}[¶]	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,					mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0					pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0				pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0				pF
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA				Ω
			V_I = 1.7 V,	I_O = −15 mA				
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA				
			V_I = 2.4 V,	I_O = −15 mA				

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$[‖]	$\overline{OE}$	A or B					MHz
t_{pd}[☆]	A or B	B or A					ns
t_{en}	$\overline{OE}$	A or B					ns
t_{dis}	$\overline{OE}$	A or B					ns

[‖] Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1$ MΩ, C_L = 0)

[☆] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

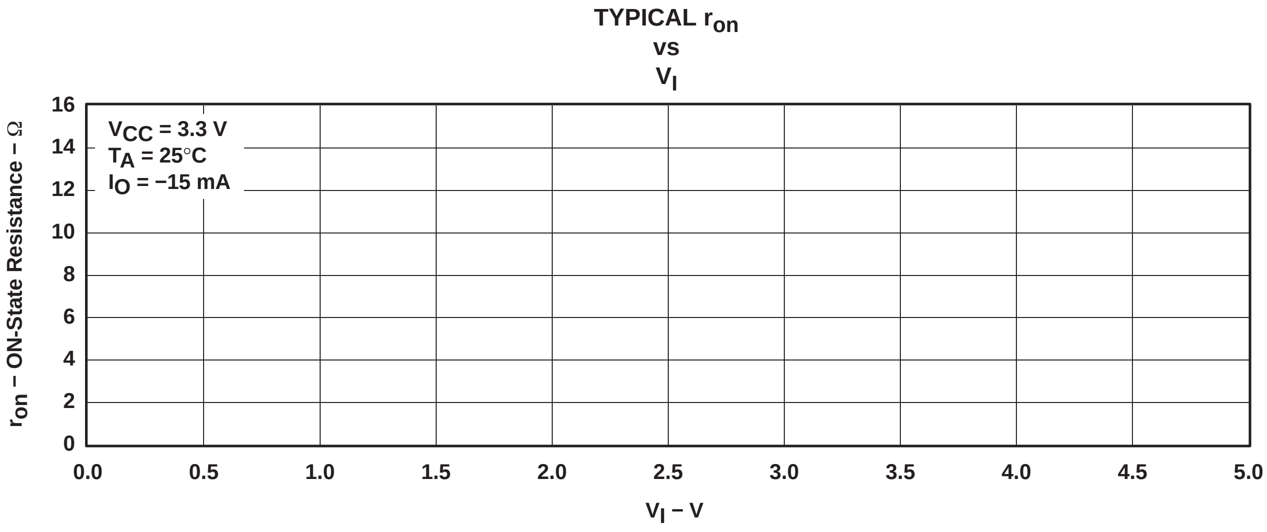


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

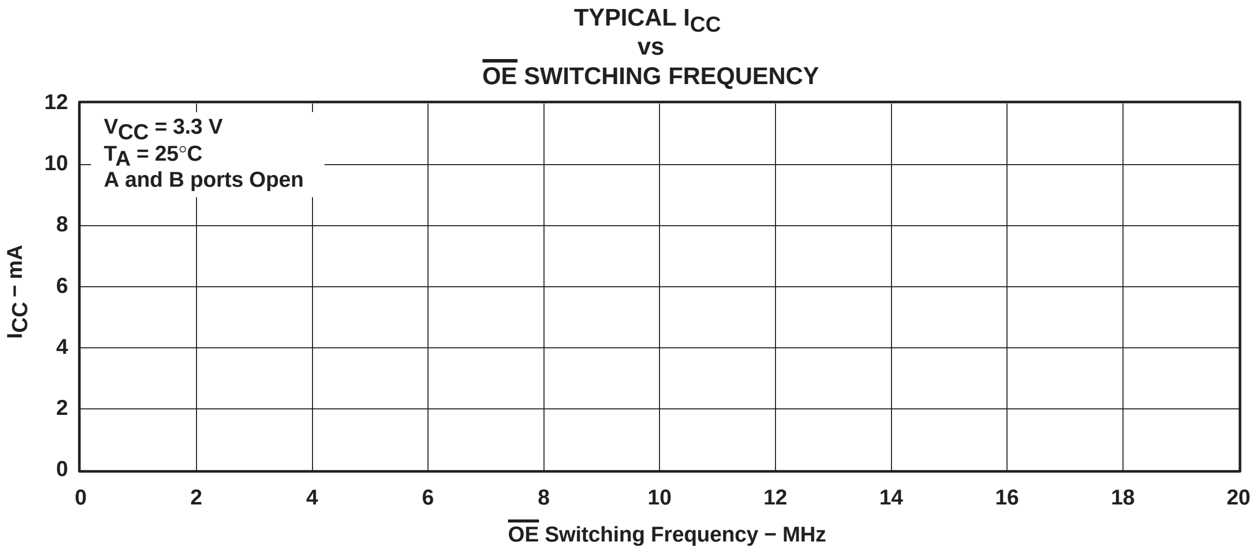
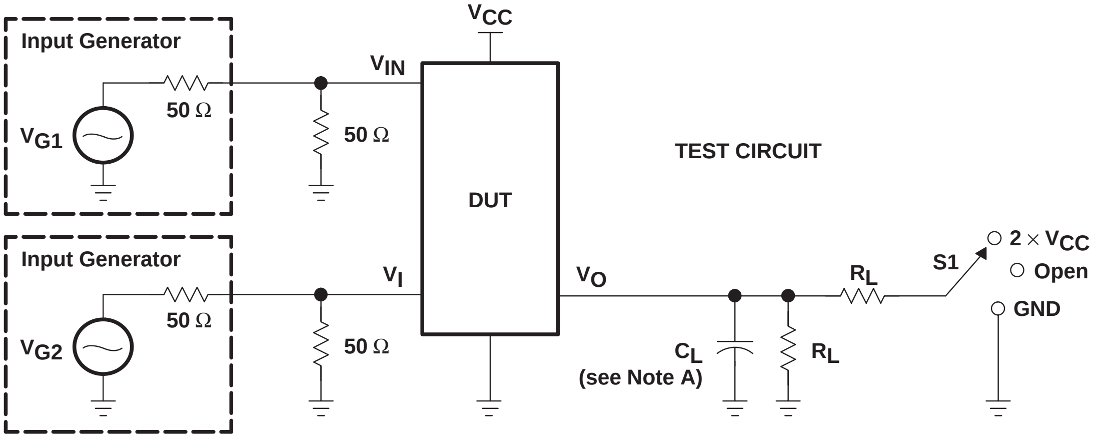


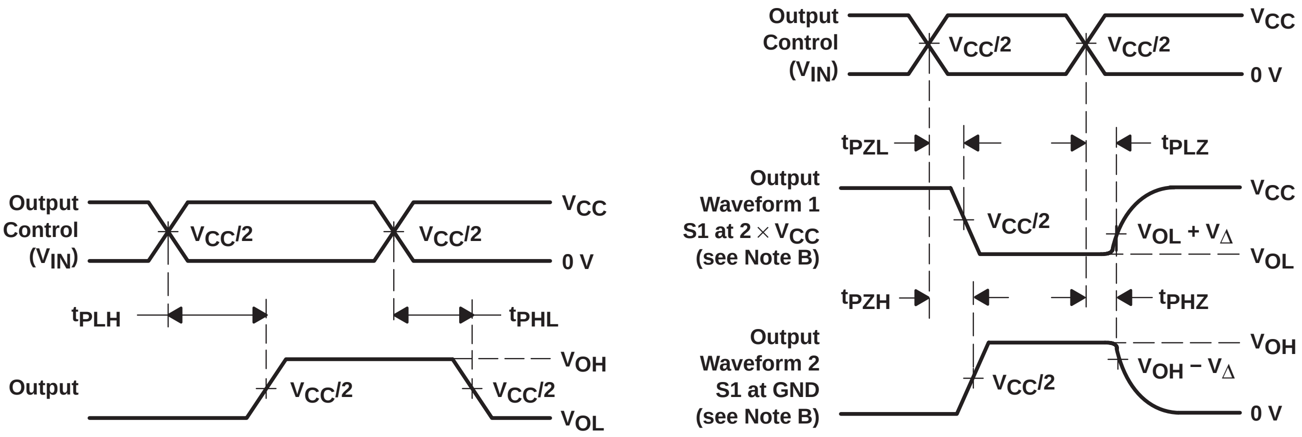
Figure 2. Typical I_{CC} vs $\overline{OE}$ Switching Frequency, V_{CC} = 3.3 V

PARAMETER MEASUREMENT INFORMATION



Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V



Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
V_{OL} + V_Δ
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
V_{OH} − V_Δ
V_{OH}
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

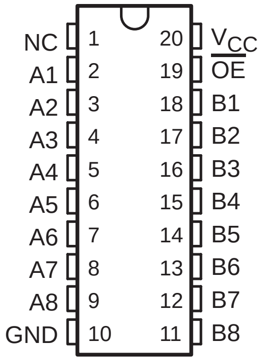
PRODUCT PREVIEW

SN74CB3Q3245
8-BIT FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

SCDS124B − JULY 2003 − REVISED NOVEMBER 2003

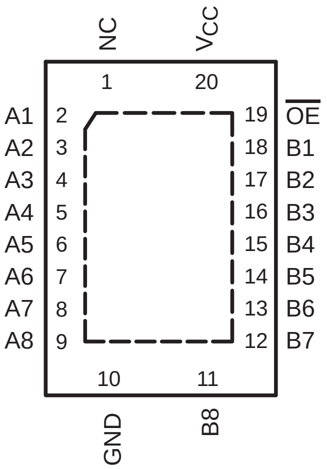
- **High-Bandwidth Data Path (Up to 500 MHz[†])**
- **Equivalent to IDTQS3VH384 Device**
- **5-V Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 4 Ω Typical)**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
  - **0- to 3.3-V Switching With 2.5-V V_{CC}**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 3.5 pF Typical)**
- **Fast Switching Frequency ($f_{\overline{OE}}$ = 20 MHz Max)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 1 mA Typical)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

RGY PACKAGE
(TOP VIEW)



NC − No internal connection

[†] For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TEXAS INSTRUMENTS

description/ordering information

The SN74CB3Q3245 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3245 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3245 is organized as an 8-bit bus switch with a single output-enable ($\overline{\text{OE}}$) input. When $\overline{\text{OE}}$ is low, the bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{\text{OE}}$ is high, the bus switch is OFF and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

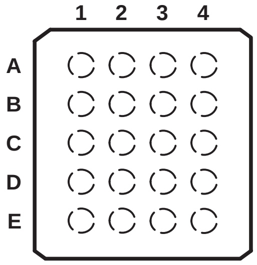
To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CB3Q3245RGYR	BU245
	SSOP (QSOP) − DBQ	Tape and reel	SN74CB3Q3245DBQR	CB3Q3245
	TSSOP − PW	Tube	SN74CB3Q3245PW	BU245
		Tape and reel	SN74CB3Q3245PWR	
	TVSOP − DGV	Tape and reel	SN74CB3Q3245DGVR	BU245
	VFBGA − GQN	Tape and reel	SN74CB3Q3245GQNR	BU245

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

GQN PACKAGE
(TOP VIEW)



terminal assignments

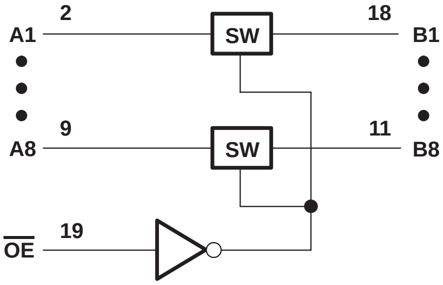
	1	2	3	4
A	A1	NC	V_{CC}	$\overline{\text{OE}}$
B	A3	B2	A2	B1
C	A5	A4	B4	B3
D	A7	B6	A6	B5
E	GND	A8	B8	B7

NC − No internal connection

FUNCTION TABLE

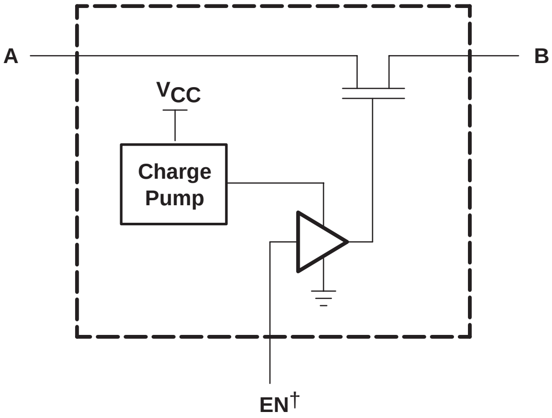
INPUT $\overline{\text{OE}}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)


A1
2
SW
18
B1
A8
9
SW
11
B8
OE
19

Pin numbers shown are for the DBQ, DGV, PW, and RGY packages.

simplified schematic, each FET switch (SW)


A
B
V_{CC}
Charge Pump
EN†

† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±64 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DBQ package	68°C/W
(see Note 5): DGV package	92°C/W
(see Note 5): GQN package	78°C/W
(see Note 5): PW package	83°C/W
(see Note 6): RGY package	37°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA				−1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	µA
I_{OZ}[‡]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		1	2	mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			30	µA
I_{CCD}[¶]	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,			0.30	0.35	mA/MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		3.5	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		9	11	pF
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		4	8	Ω
			V_I = 1.7 V,	I_O = −15 mA		4.5	9	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		4	6	
			V_I = 2.4 V,	I_O = −15 mA		4	8	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$[‖]	$\overline{OE}$	A or B		10		20	MHz
t_{pd}[☆]	A or B	B or A		0.12		0.20	ns
t_{en}	$\overline{OE}$	A or B	1.5	7.5	1.5	6.5	ns
t_{dis}	$\overline{OE}$	A or B	1	6.5	1	6.5	ns

[‖] Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1\ M\Omega$, C_L = 0)

[☆] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

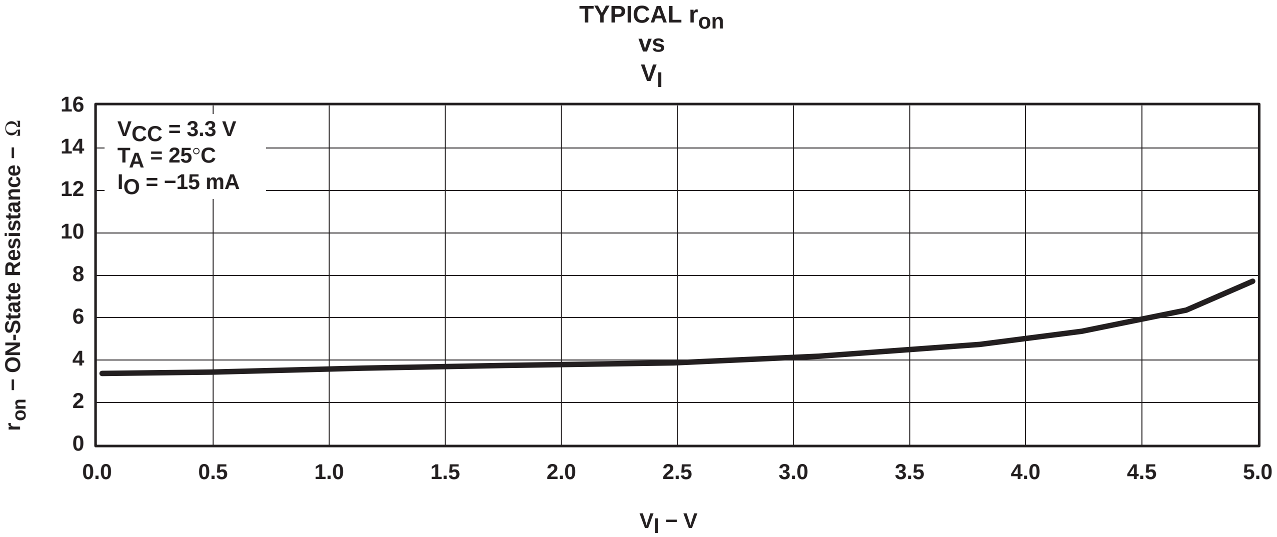


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

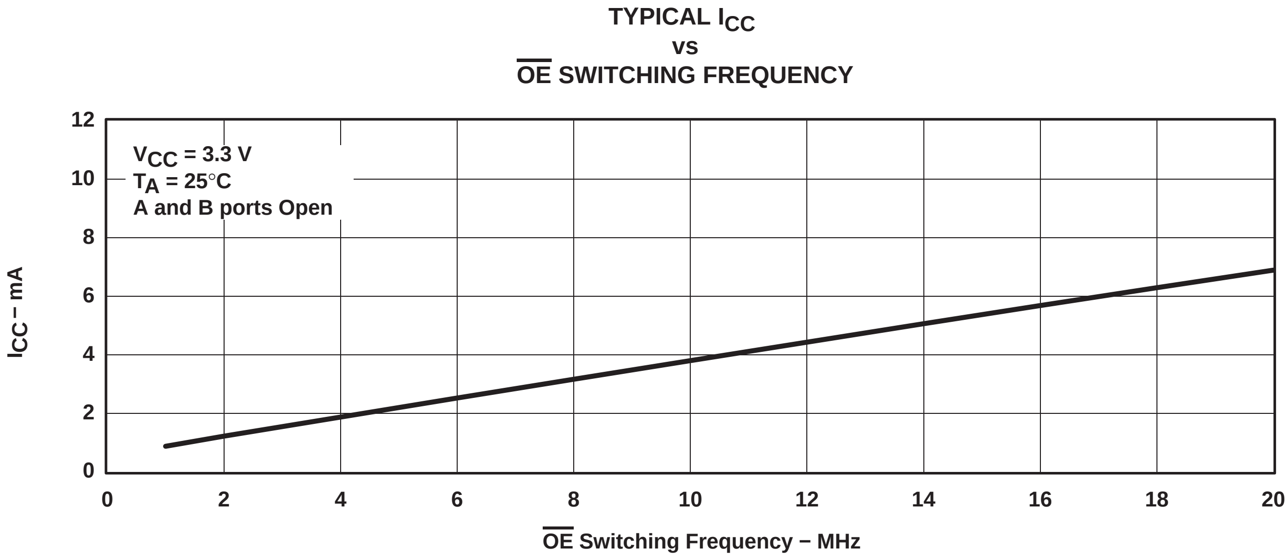
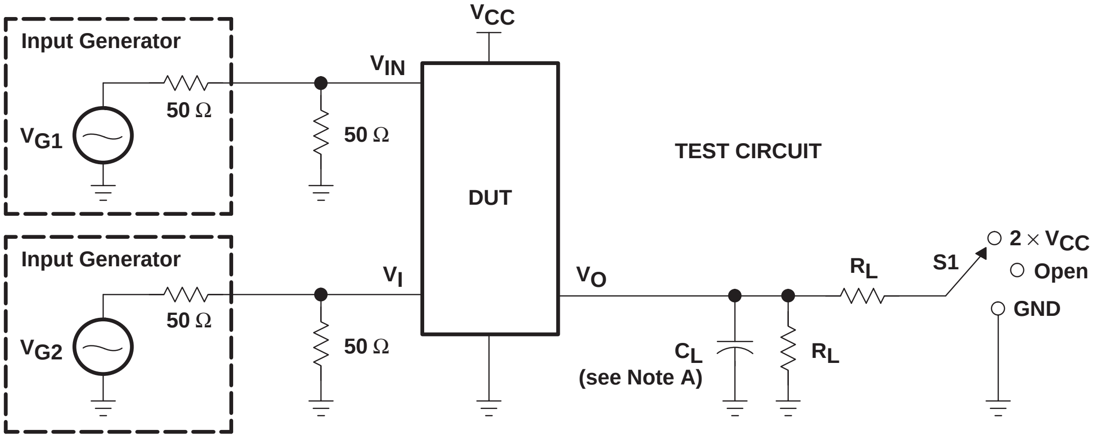
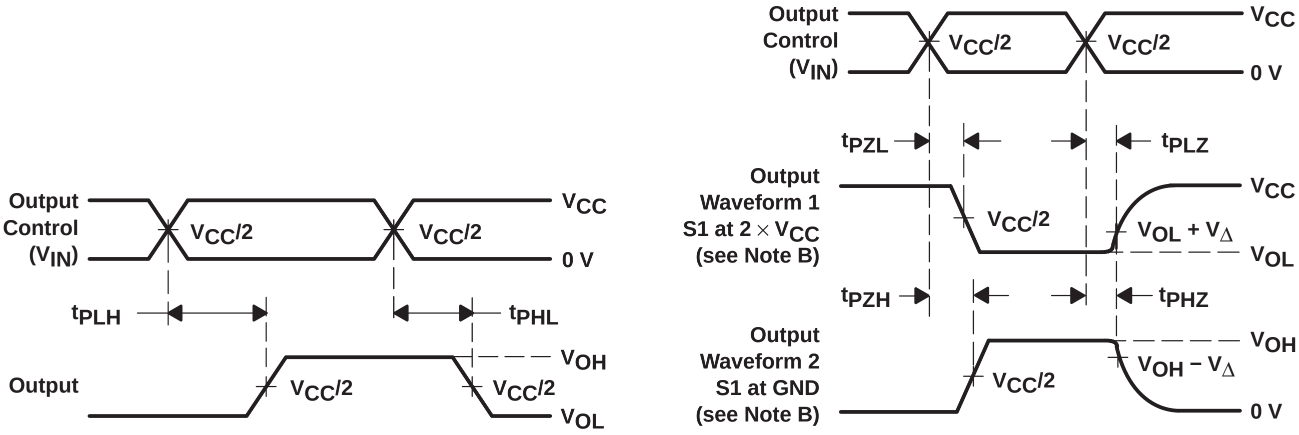


Figure 2. Typical I_{CC} vs $\overline{OE}$ Switching Frequency, V_{CC} = 3.3 V

PARAMETER MEASUREMENT INFORMATION


VCC
Input Generator
VIN
50 Ω
VG1
50 Ω
TEST CIRCUIT
DUT
Input Generator
VI
VO
RL
S1
2 × VCC
Open
GND
50 Ω
VG2
50 Ω
CL
(see Note A)
RL

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V


Output Control (VIN)
VCC/2
VCC/2
VCC
0 V
tPLH
tPHL
Output
VCC/2
VCC/2
VOH
VOL
Output Control (VIN)
VCC/2
VCC/2
VCC
0 V
tPZL
tPLZ
Output Waveform 1 S1 at 2 × VCC (see Note B)
VCC/2
VOL + VΔ
VCC
VOL
tPZH
tPHZ
Output Waveform 2 S1 at GND (see Note B)
VCC/2
VOH − VΔ
VOH
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

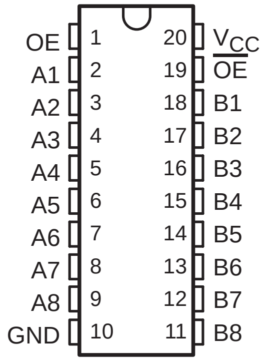
SN74CB3Q3345
8-BIT FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

SCDS144A − OCTOBER 2003 − REVISED NOVEMBER 2003

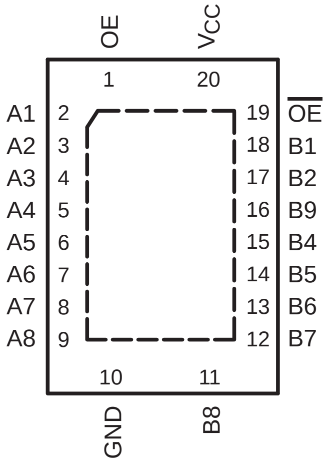
- **High-Bandwidth Data Path (Up To 500 MHz[†])**
- **5-V Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 4 Ω Typical)**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
  - **0- to 3.3-V Switching With 2.5-V V_{CC}**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 4 pF Typical)**
- **Fast Switching Frequency ($f_{\overline{OE}}$ = 20 MHz Max)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 0.7 mA Typical)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

[†] For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information

The SN74CB3Q3345 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3345 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3384A is organized as an 8-bit bus switch with two output-enable (OE, $\overline{OE}$) inputs. When OE is high or $\overline{OE}$ is low, the bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is low and $\overline{OE}$ is high, the bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

ORDERING INFORMATION

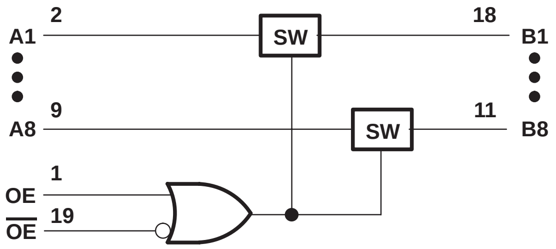
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CB3Q3345RGYR	BU345
	SSOP (QSOP) − DBQ	Tape and reel	SN74CB3Q3345DBQR	CB3Q3345
	TSSOP − PW	Tube	SN74CB3Q3345PW	BU345
		Tape and reel	SN74CB3Q3345PWR	
	TVSOP − DGV	Tape and reel	SN74CB3Q3345DGVR	BU345

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

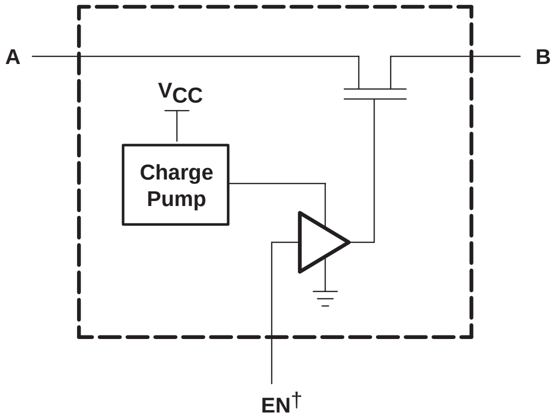
FUNCTION TABLE

INPUTS		INPUT/OUTPUT A	FUNCTION
OE	$\overline{OE}$		
H	X	B	A port = B port
X	L	B	A port = B port
L	H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} (V_{IN} < 0)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O}$ < 0)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±64 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DBQ package	68°C/W
(see Note 5): DGV package	92°C/W
(see Note 5): PW package	83°C/W
(see Note 6): RGY package	37°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA				−1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	μA
I_{OZ}[‡]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	μA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		0.7	2	mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			30	μA
I_{CCD}[¶]	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,			0.13	0.14	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		3.5	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		9	11.5	pF
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		4	8	Ω
			V_I = 1.7 V,	I_O = −15 mA		4.5	9	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		4	6	
			V_I = 2.4 V,	I_O = −15 mA		4.5	8	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
f_{OE} or $f_{\overline{OE}}$[‖]	OE or $\overline{OE}$	A or B		10		20	MHz
t_{pd}[☆]	A or B	B or A		0.12		0.2	ns
t_{en}	OE or $\overline{OE}$	A or B	1.5	7.7	1.5	6.5	ns
t_{dis}	OE or $\overline{OE}$	A or B	1	6.9	1	6.8	ns

[‖] Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1$ MΩ, C_L = 0)

[☆] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

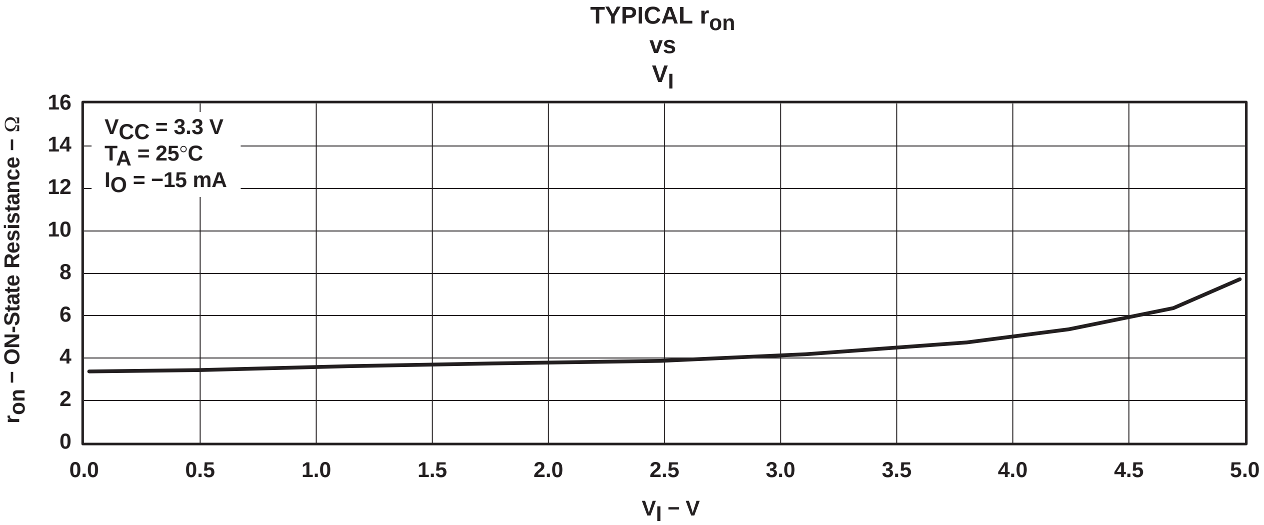


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

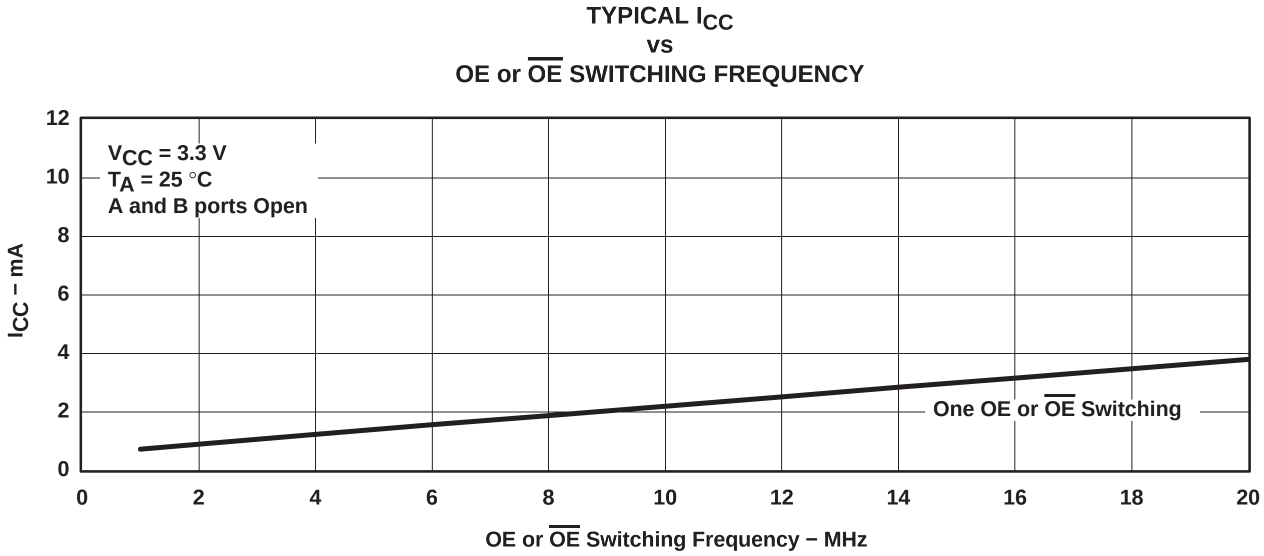
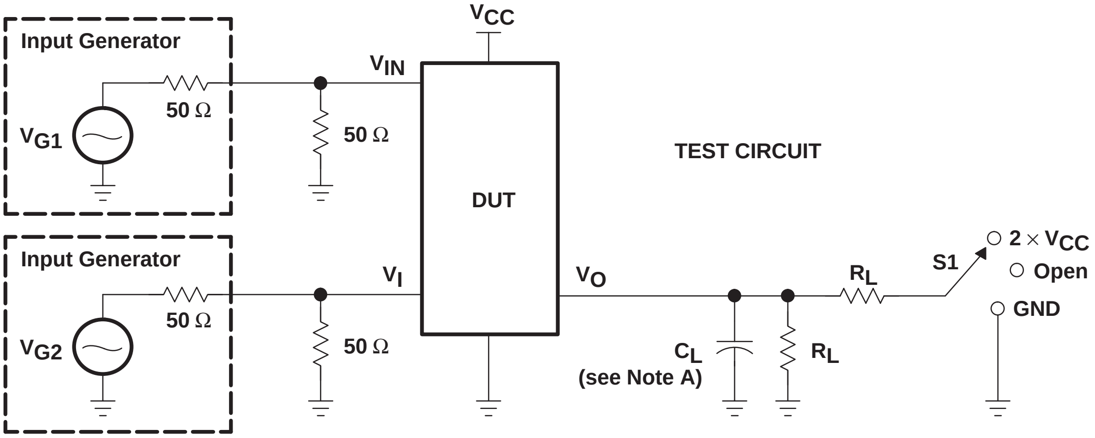
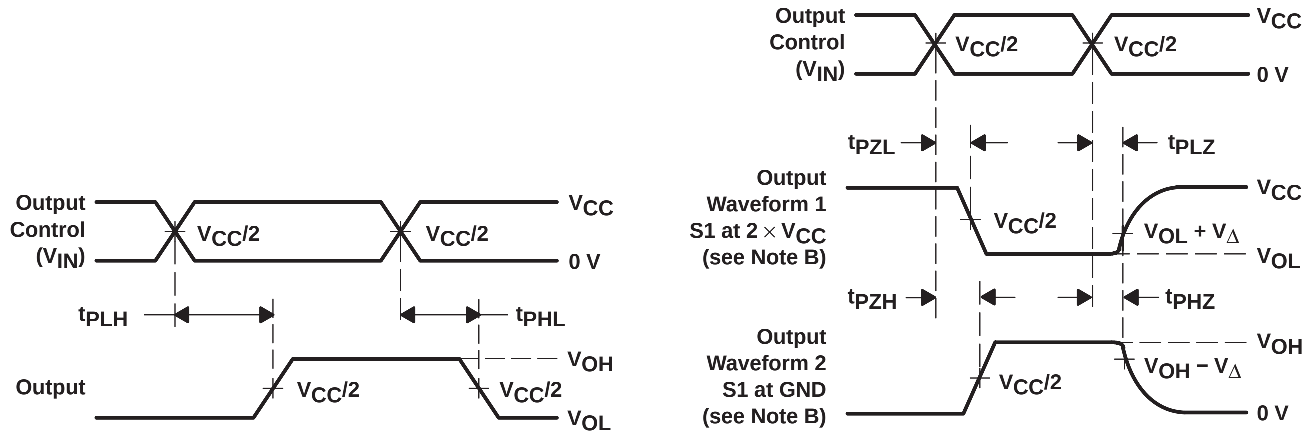


Figure 2. Typical I_{CC} vs OE or $\overline{OE}$ Switching Frequency, V_{CC} = 3.3 V

PARAMETER MEASUREMENT INFORMATION


V_{CC}
Input Generator
V_{IN}
50 Ω
V_{G1}
50 Ω
TEST CIRCUIT
DUT
Input Generator
V_I
V_O
R_L
S1
2 × V_{CC}
Open
GND
50 Ω
V_{G2}
50 Ω
C_L
(see Note A)
R_L

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

SN74CB3Q3384A
10-BIT FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

SCDS114D − DECEMBER 2002 − REVISED NOVEMBER 2003

- **High-Bandwidth Data Path (Up To 500 MHz†)**
- **5-V Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 3 Ω Typical)**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
  - **0- to 3.3-V Switching With 2.5-V V_{CC}**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 4 pF Typical)**
- **Fast Switching Frequency ($f_{\overline{OE}}$ = 20 MHz Max)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 1 mA Typical)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

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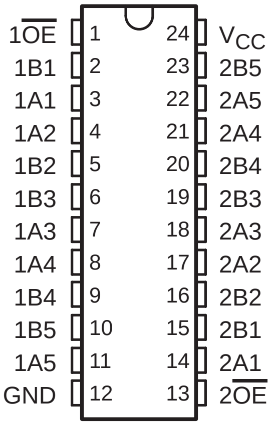
† For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QSOP − DBQ	Tape and reel	SN74CB3Q3384ADBQR	CB3Q3384A
	TSSOP − PW	Tube	SN74CB3Q3384APW	BU384A
		Tape and reel	SN74CB3Q3384APWR	
	TVSOP − DGV	Tape and reel	SN74CB3Q3384ADGVR	BU384A

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The SN74CB3Q3384A is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3384A provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3384A is organized as two 5-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. It can be used as two 5-bit bus switches, or as one 10-bit bus switch. When $\overline{OE}$ is low, the associated 5-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 5-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

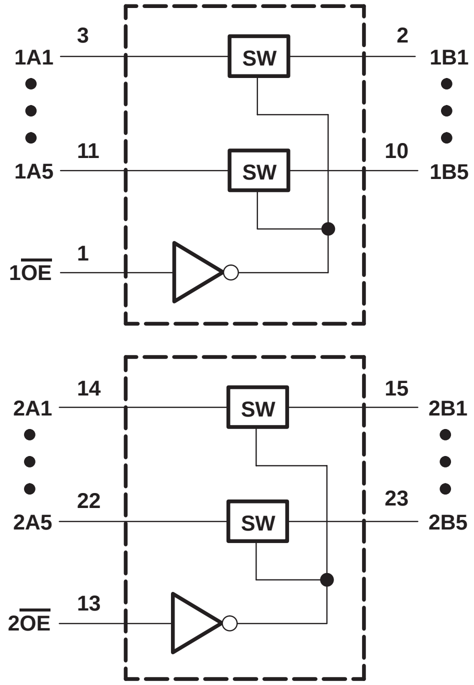
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

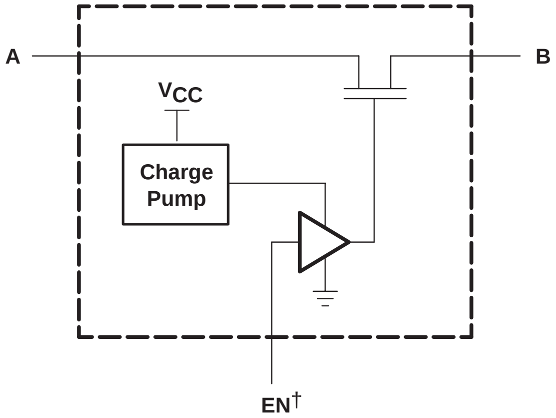
FUNCTION TABLE
(each 5-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±64 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DBQ package	61°C/W
DGV package	86°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA				−1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	μA
I_{OZ}[‡]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	μA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		1	2	mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			30	μA
I_{CCD}[¶]	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,			0.15	0.25	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		3.5	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		8	10	pF
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		3	8	Ω
			V_I = 1.7 V,	I_O = −15 mA		3.5	9	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		3.5	8	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$[‖]	$\overline{OE}$	A or B		10		20	MHz
t_{pd}[☆]	A or B	B or A		0.09		0.15	ns
t_{en}	$\overline{OE}$	A or B	1.5	7.2	1.5	6	ns
t_{dis}	$\overline{OE}$	A or B	1.5	6.6	1.5	6.6	ns

[‖] Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1$ MΩ, C_L = 0)

[☆] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

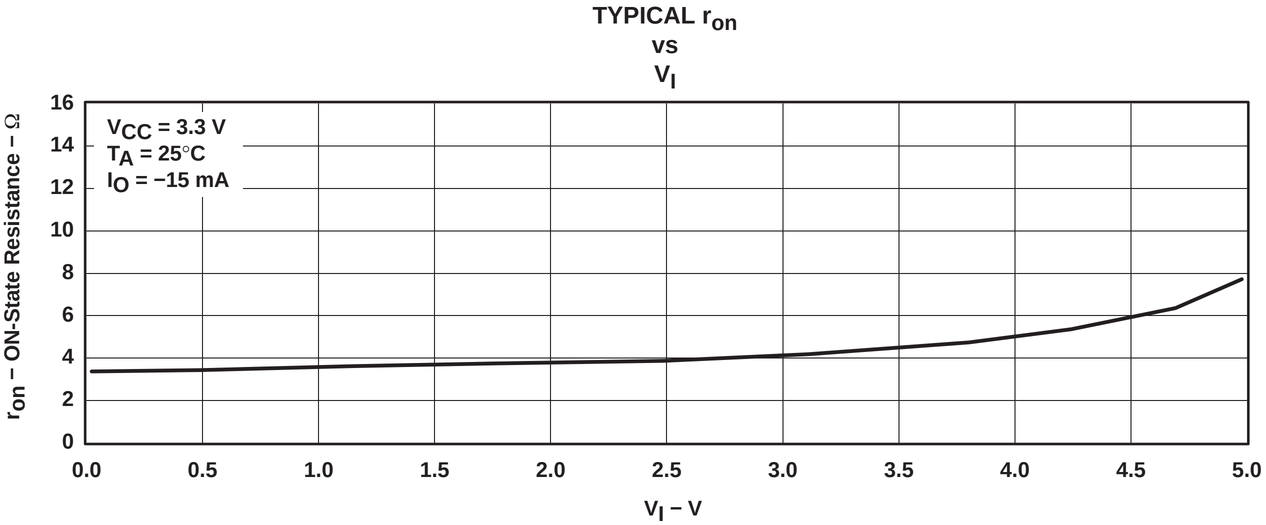


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

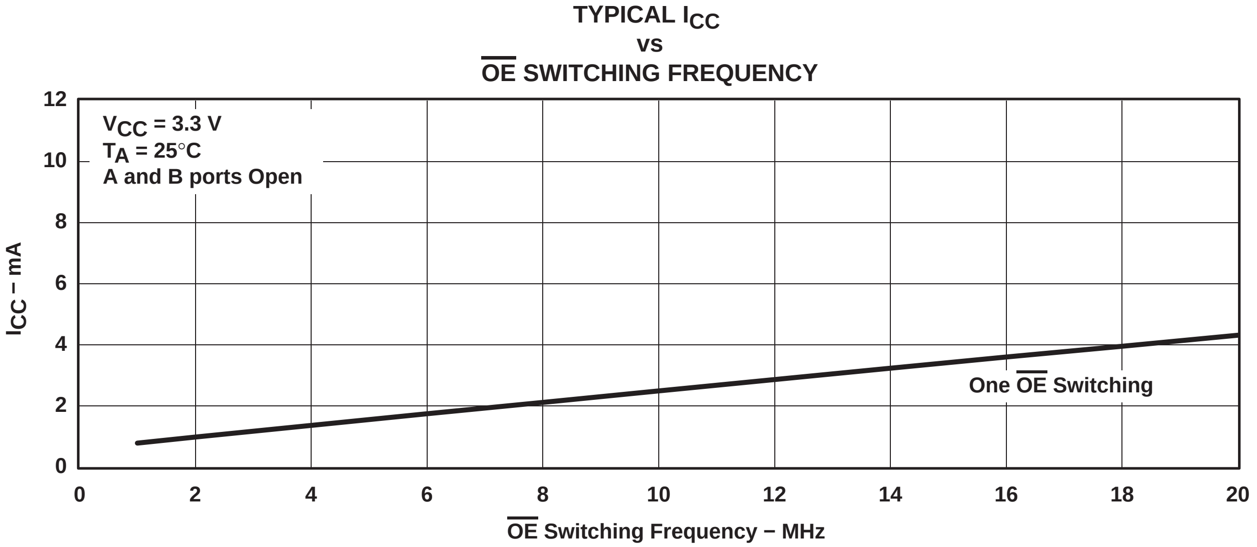
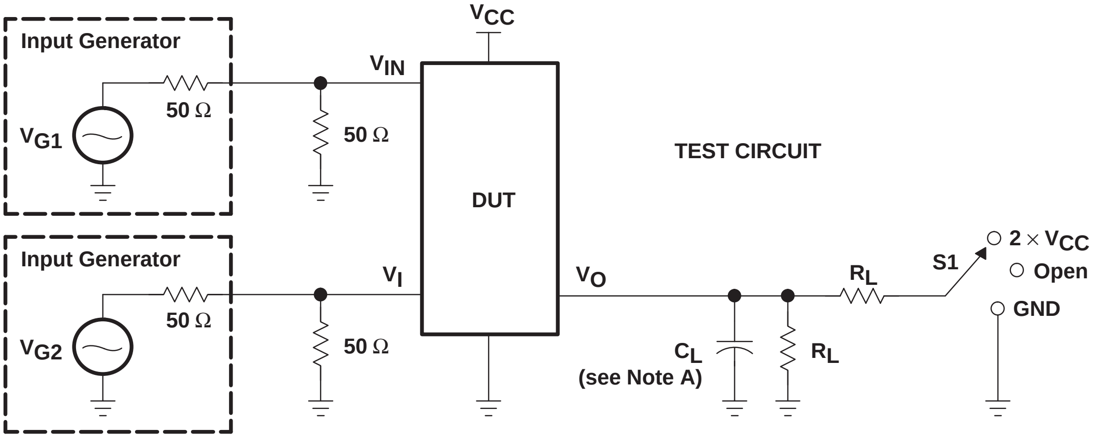
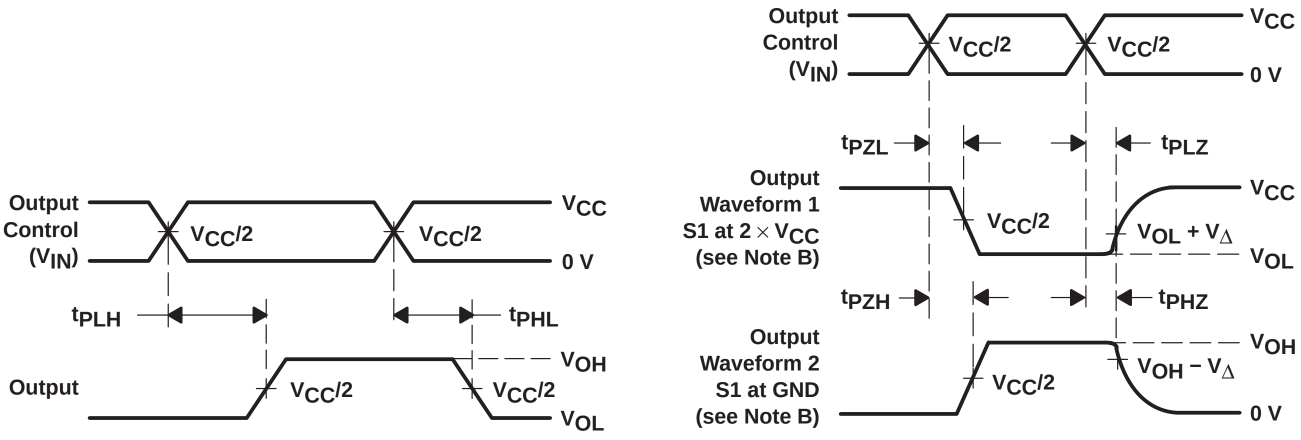


Figure 2. Typical I_{CC} vs $\overline{OE}$ Switching Frequency, V_{CC} = 3.3 V

PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_{CC}
DUT
TEST CIRCUIT
V_O
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

SN74CB3Q6800
10-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS
2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

SCDS142A − OCTOBER 2003 − REVISED NOVEMBER 2003

- **High-Bandwidth Data Path (Up To 500 MHz†)**
- **5-V Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 4.5 Ω Typical)**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
  - **0- to 3.3-V Switching With 2.5-V V_{CC}**
- **B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot-Plugging**
- **Supports PCI Hot Plug**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 3.5 pF Typical)**
- **Fast Switching Frequency ($f_{\overline{ON}}$ = 20 MHz Max)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 0.75 mA Typical)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

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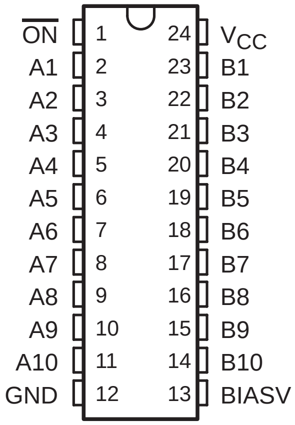
† For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



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TEXAS INSTRUMENTS

description/ordering information

The SN74CB3Q6800 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q6800 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q6800 is a 10-bit bus switch with a single output-enable ($\overline{\text{ON}}$) input. When $\overline{\text{ON}}$ is low, the 10-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{\text{ON}}$ is high, the 10-bit bus switch is OFF and a high-impedance state exists between the A and B ports. The B port is precharged to bias voltage (BIASV) through the equivalent of a 10-kΩ resistor when $\overline{\text{ON}}$ is high, or if the device is powered down (V_{CC} = 0 V).

During insertion (or removal) of a card into (or from) an active bus, the card’s output voltage may be close to GND. When the connector pins make contact, the card’s parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method will ensure that any glitch produced by insertion (or removal) of the card will not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\text{ON}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

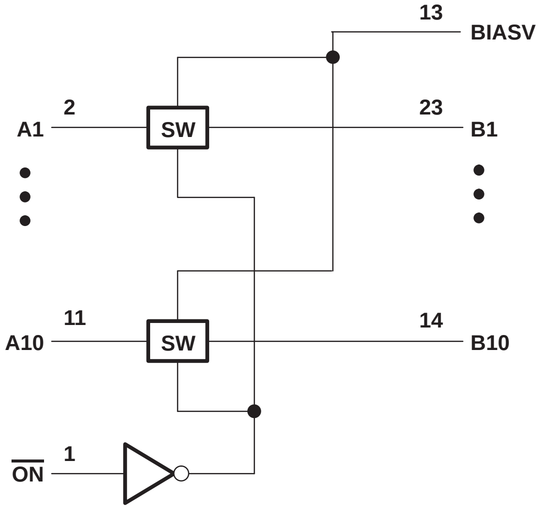
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP (QSOP) − DBQ	Tape and reel	SN74CB3Q6800DBQR	CB3Q6800
	TSSOP − PW	Tube	SN74CB3Q6800PW	BY800
		Tape and reel	SN74CB3Q6800PWR	
	TVSOP − DGV	Tape and reel	SN74CB3Q6800DGVR	BY800

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

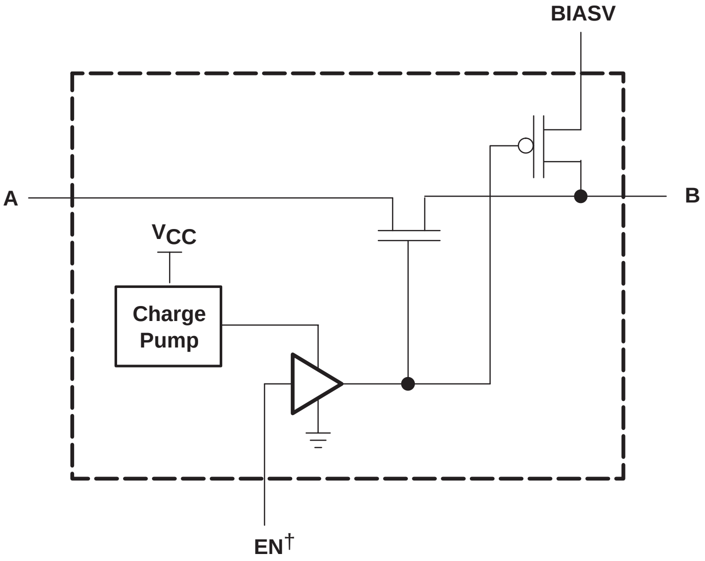
FUNCTION TABLE

INPUT $\overline{\text{ON}}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect B port = BIASV

logic diagram (positive logic)


13
BIASV
2
A1
SW
23
B1
11
A10
SW
14
B10
1
$\overline{ON}$

simplified schematic, each FET switch (SW)


BIASV
A
B
V_{CC}
Charge Pump
EN†

† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
BIAS supply voltage range, BIASV	−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±64 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DBQ package	61°C/W
DGV package	86°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
BIASV	Bias supply voltage		0	5	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. BIASV is a supply voltage, not a control input.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA				−1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	µA
I_O	B port	V_{CC} = 3.V,	BIASV = 2.4 V, V_O = 0,	Switch OFF, V_{IN} = V_{CC} or GND		0.2		mA
I_{OZ}[‡]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		0.75	2	mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			30	µA
I_{CCD}[¶]	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,			0.38	0.45	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		3.5	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		9	11	pF
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		4.5	8	Ω
			V_I = 1.7 V,	I_O = −15 mA		4.8	9	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		4.5	6	
			V_I = 2.4 V,	I_O = −15 mA		4.6	8	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	
$f_{\overline{ON}}$[‖]		$\overline{ON}$	A or B		10		20	MHz
t_{pd}[☆]		A or B	B or A		0.135		0.225	ns
t_{PZH}	BIASV = GND	$\overline{ON}$	A or B	1.5	8.5	1.5	6.7	ns
t_{PZL}	BIASV = 3 V			1.5	8.5	1.5	6.7	
t_{PHZ}	BIASV = GND	$\overline{ON}$	A or B	1	5	1	5	ns
t_{PLZ}	BIASV = 3 V			1	6.9	1	6.9	

[‖] Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1$ MΩ, C_L = 0).

[☆] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

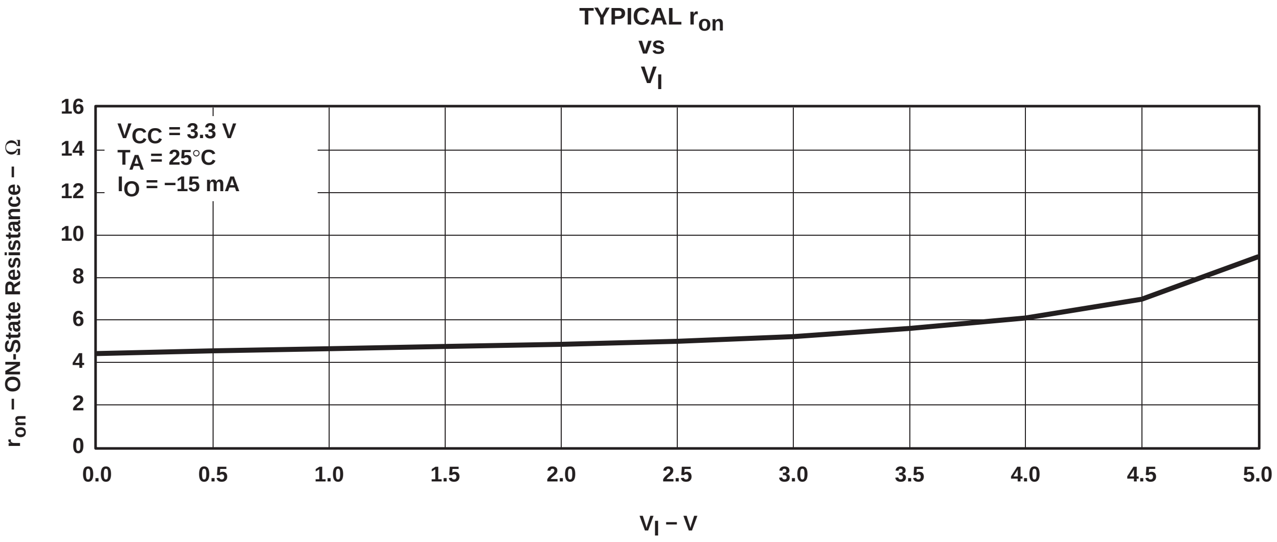


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

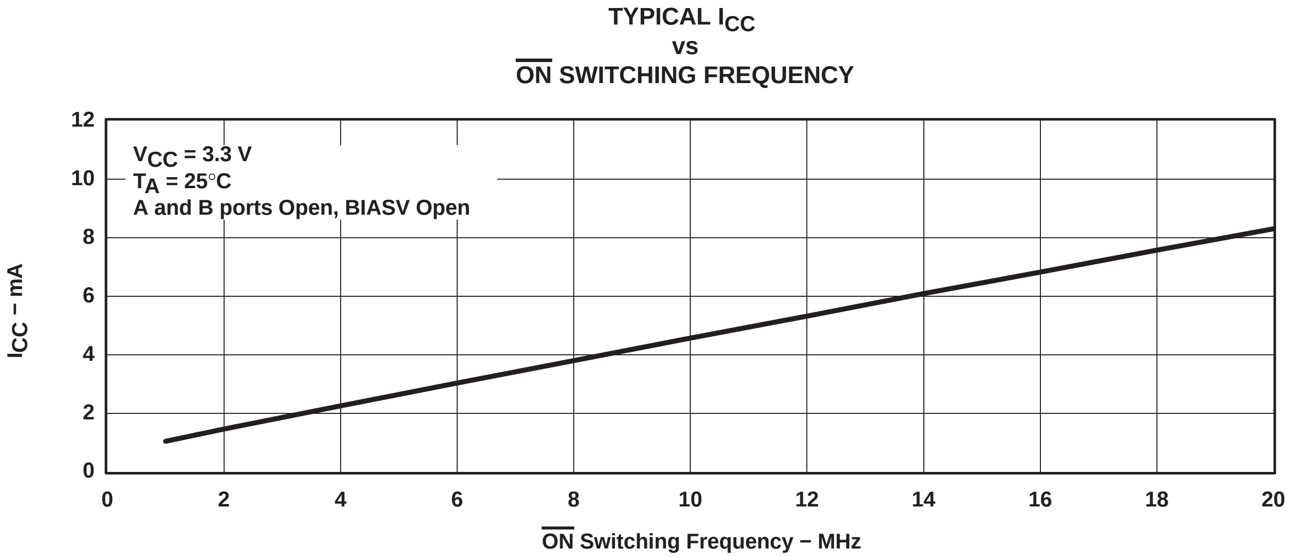
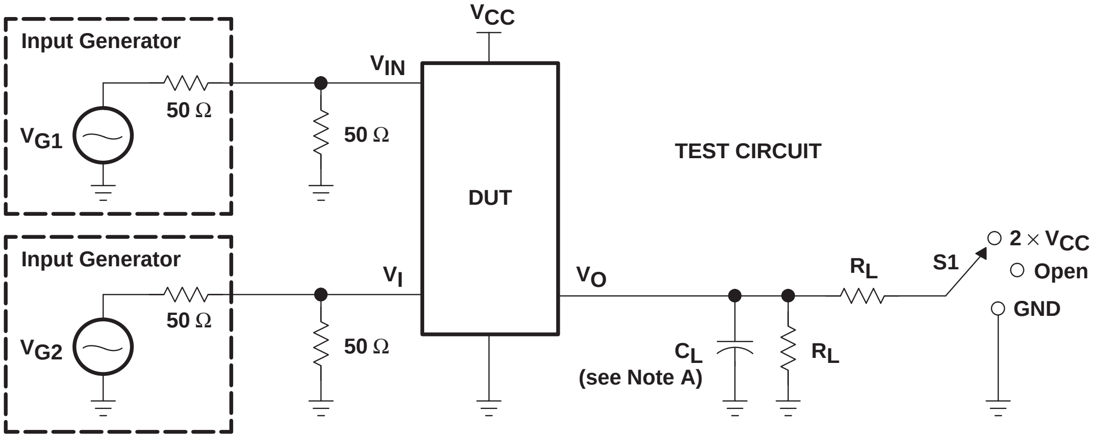
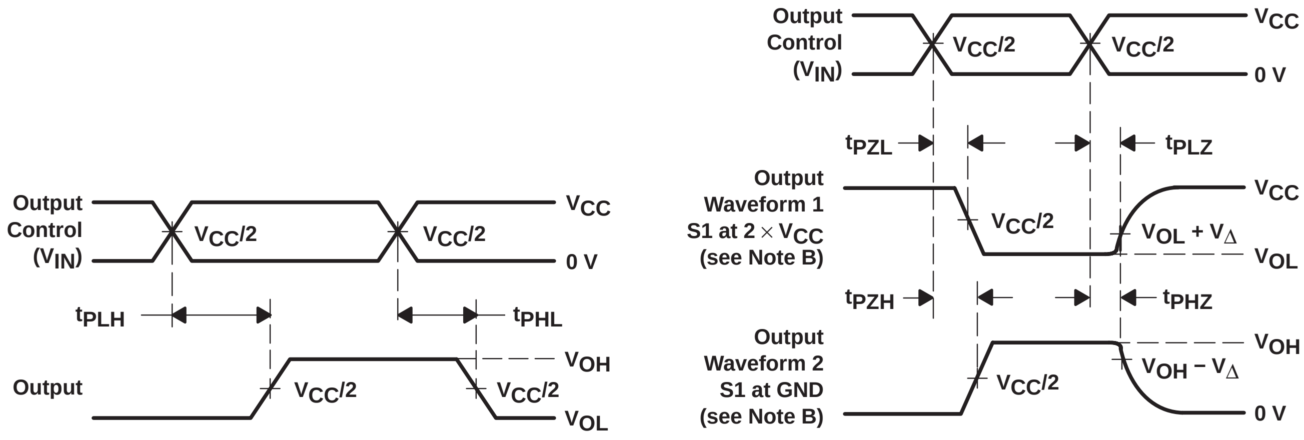


Figure 2. Typical I_{CC} vs $\overline{ON}$ Switching Frequency, V_{CC} = 3.3 V

PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
R_L
S1
2 × V_{CC}
Open
GND
C_L
(see Note A)
R_L

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
$V_{OH} − V_\Delta$
V_{OH}
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le$ 2.5 ns, $t_f \le$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

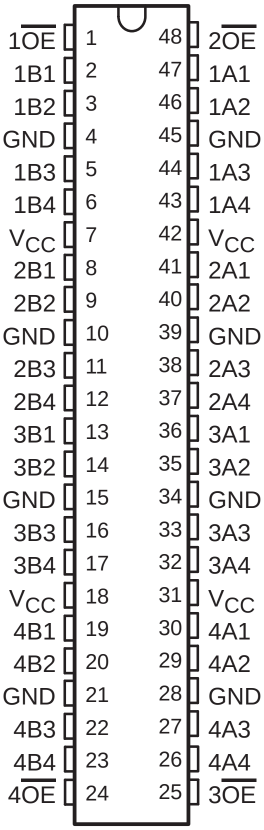
SN74CB3Q16244
16-BIT FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

SCDS155A − OCTOBER 2003 − REVISED NOVEMBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **High-Bandwidth Data Path (Up To 500 MHz[†])**
- **5-V-Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
  - **0- to 3.3-V Switching With 2.5-V V_{CC}**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion**
- **Fast Switching Frequency**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

[†] For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


1$\overline{\text{OE}}$ 1 48 2$\overline{\text{OE}}$
1B1 2 47 1A1
1B2 3 46 1A2
GND 4 45 GND
1B3 5 44 1A3
1B4 6 43 1A4
V_{CC} 7 42 V_{CC}
2B1 8 41 2A1
2B2 9 40 2A2
GND 10 39 GND
2B3 11 38 2A3
2B4 12 37 2A4
3B1 13 36 3A1
3B2 14 35 3A2
GND 15 34 GND
3B3 16 33 3A3
3B4 17 32 3A4
V_{CC} 18 31 V_{CC}
4B1 19 30 4A1
4B2 20 29 4A2
GND 21 28 GND
4B3 22 27 4A3
4B4 23 26 4A4
4$\overline{\text{OE}}$ 24 25 3$\overline{\text{OE}}$

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PRODUCT PREVIEW

description/ordering information

The SN74CB3Q16244 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q16244 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q16244 is organized as four 4-bit bus switches with separate output-enable (1$\overline{\text{OE}}$, 2$\overline{\text{OE}}$, 3$\overline{\text{OE}}$, 4$\overline{\text{OE}}$) inputs. It can be used as four 4-bit bus switches, two 8-bit bus switches, or as one 16-bit bus switch. When $\overline{\text{OE}}$ is low, the associated 4-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{\text{OE}}$ is high, the associated 4-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

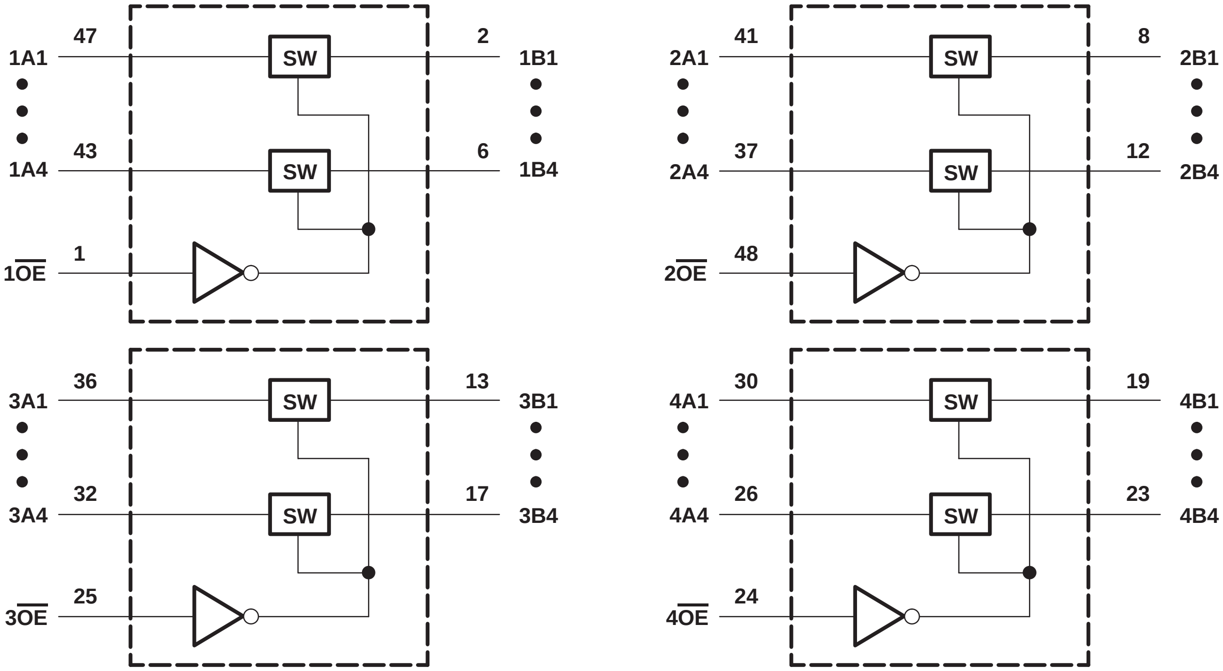
T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CB3Q16211DL	
		Tape and reel	SN74CB3Q16211DLR	
	TSSOP − DGG	Tape and reel	SN74CB3Q16211DGGR	
	TVSOP − DGV	Tape and reel	SN74CB3Q16211DGVR	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

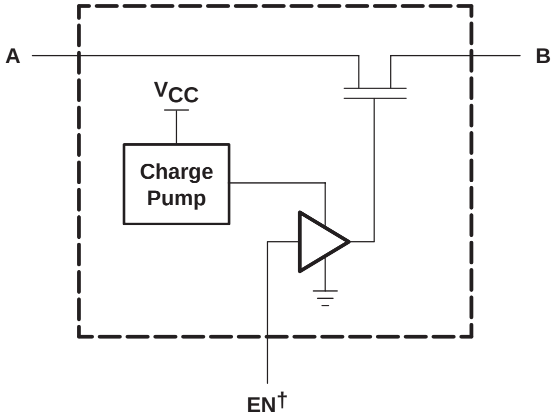
FUNCTION TABLE
(each 4-bit bus switch)

INPUT $\overline{\text{OE}}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)


1A1
47
SW
2
1B1
1A4
43
SW
6
1B4
1$\overline{OE}$
1
2A1
41
SW
8
2B1
2A4
37
SW
12
2B4
2$\overline{OE}$
48
3A1
36
SW
13
3B1
3A4
32
SW
17
3B4
3$\overline{OE}$
25
4A1
30
SW
19
4B1
4A4
26
SW
23
4B4
4$\overline{OE}$
24

simplified schematic, each FET switch (SW)


A
B
V_{CC}
Charge Pump
EN†

† EN is the internal enable signal applied to the switch.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±64 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA					V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V					µA
I_{OZ}[‡]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND				µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0				µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND				mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND				µA
I_{CCD}[¶]	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,					mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0					pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0				pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0				pF
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA				Ω
			V_I = 1.7 V,	I_O = −15 mA				
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA				
			V_I = 2.4 V,	I_O = −15 mA				

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$[‖]	$\overline{OE}$	A or B					MHz
t_{pd}[☆]	A or B	B or A					ns
t_{en}	$\overline{OE}$	A or B					ns
t_{dis}	$\overline{OE}$	A or B					ns

[‖] Maximum switching frequency for control input (V_O > V_{CC}, V_I = 5 V, R_L ≥ 1 MΩ, C_L = 0)

[☆] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PRODUCT PREVIEW

PRODUCT PREVIEW

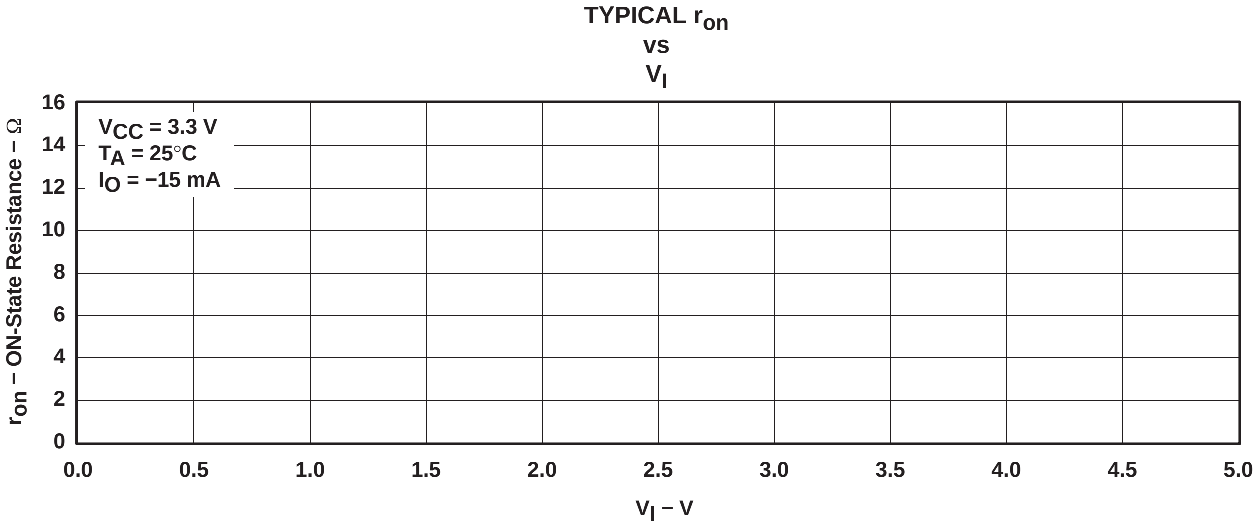


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

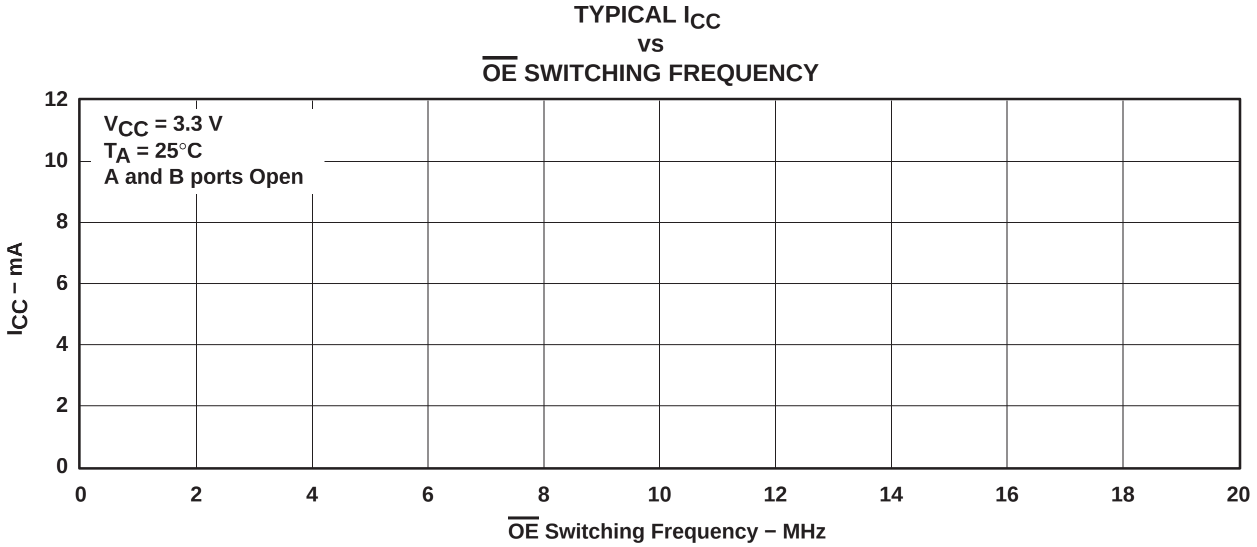
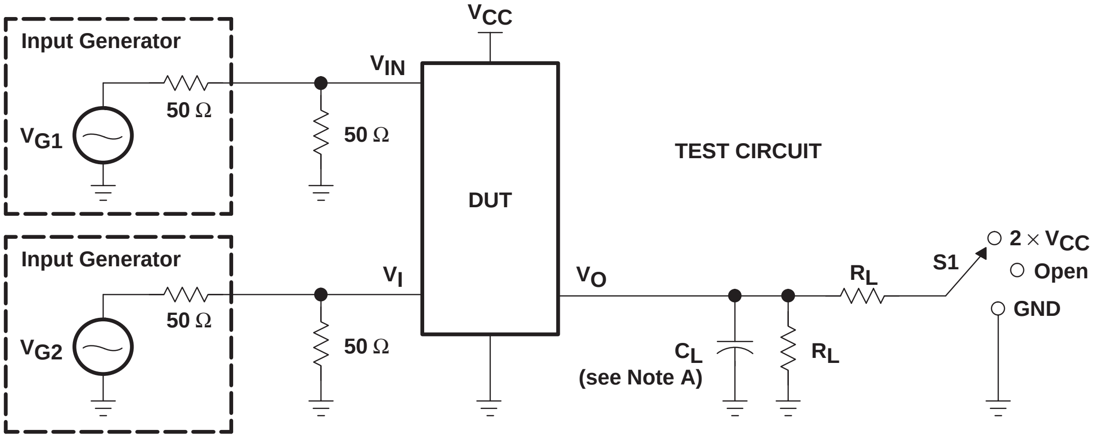
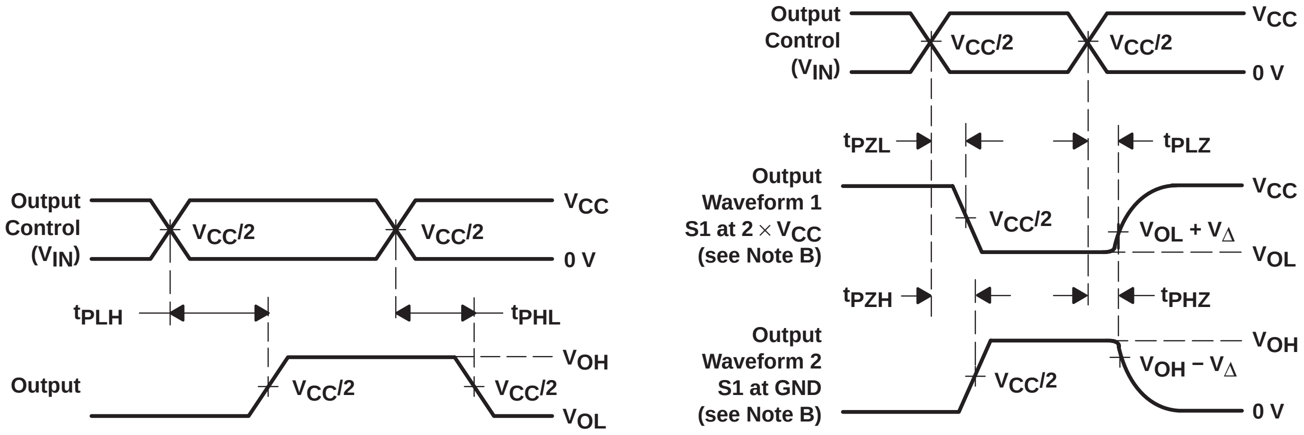


Figure 2. Typical I_{CC} vs $\overline{OE}$ Switching Frequency, V_{CC} = 3.3 V

PARAMETER MEASUREMENT INFORMATION


V_{CC}
Input Generator
V_{IN}
50 Ω
V_{G1}
50 Ω
TEST CIRCUIT
DUT
Input Generator
V_I
V_O
R_L
S1
○ 2 × V_{CC}
○ Open
○ GND
50 Ω
V_{G2}
50 Ω
C_L
(see Note A)
R_L

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
V_{CC}
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

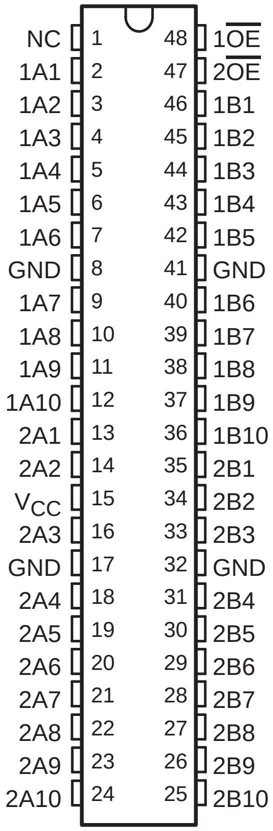
Figure 3. Test Circuit and Voltage Waveforms

SN74CB3Q16210
20-BIT FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

SCDS151A − OCTOBER 2003 − REVISED NOVEMBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **High-Bandwidth Data Path (Up To 500 MHz[†])**
- **5-V-Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
  - **0- to 3.3-V Switching With 2.5-V V_{CC}**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion**
- **Fast Switching Frequency**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1 48 1$\overline{OE}$
1A1 2 47 2$\overline{OE}$
1A2 3 46 1B1
1A3 4 45 1B2
1A4 5 44 1B3
1A5 6 43 1B4
1A6 7 42 1B5
GND 8 41 GND
1A7 9 40 1B6
1A8 10 39 1B7
1A9 11 38 1B8
1A10 12 37 1B9
2A1 13 36 1B10
2A2 14 35 2B1
V_{CC} 15 34 2B2
2A3 16 33 2B3
GND 17 32 GND
2A4 18 31 2B4
2A5 19 30 2B5
2A6 20 29 2B6
2A7 21 28 2B7
2A8 22 27 2B8
2A9 23 26 2B9
2A10 24 25 2B10

NC − No internal connection

PRODUCT PREVIEW

[†] For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

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PRODUCT PREVIEW

description/ordering information

The SN74CB3Q16210 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q16210 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q16210 is organized as two 10-bit bus switches with separate output-enable (1$\overline{OE}$, 2$\overline{OE}$) inputs. It can be used as two 10-bit bus switches, or as one 20-bit bus switch. When $\overline{OE}$ is low, the associated 10-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 10-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

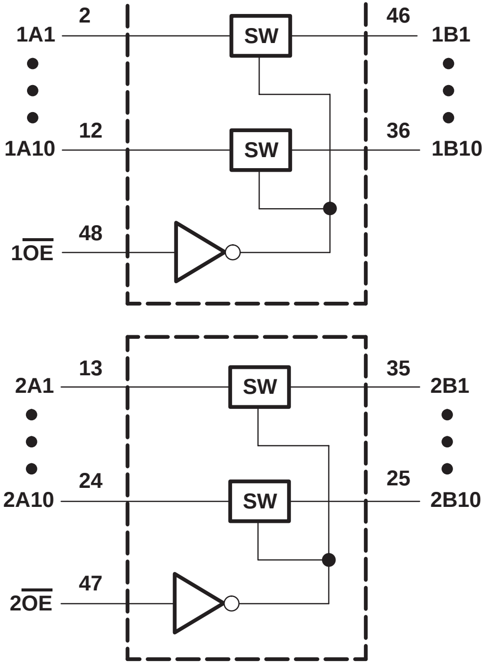
T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CB3Q16210DL	
		Tape and reel	SN74CB3Q16210DLR	
	TSSOP − DGG	Tape and reel	SN74CB3Q16210DGGR	
	TVSOP − DGV	Tape and reel	SN74CB3Q16210DGVR	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

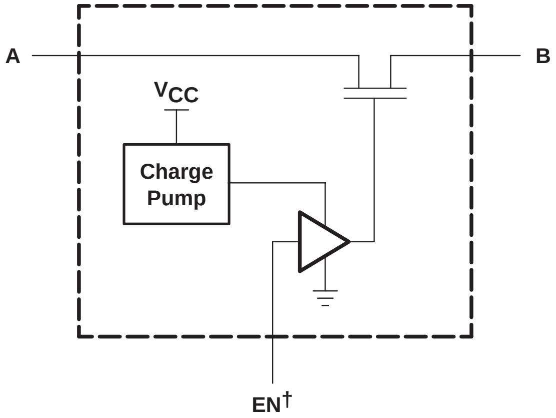
FUNCTION TABLE
(each 10-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)


1A1
2
SW
46
1B1
1A10
12
SW
36
1B10
1$\overline{OE}$
48
2A1
13
SW
35
2B1
2A10
24
SW
25
2B10
2$\overline{OE}$
47

simplified schematic, each FET switch (SW)


A
B
V_{CC}
Charge Pump
EN†

† EN is the internal enable signal applied to the switch.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±64 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA					V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V					µA
I_{OZ}[‡]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND				µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0				µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND				mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND				µA
I_{CCD}[¶]	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,					mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0					pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0				pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0				pF
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA				Ω
			V_I = 1.7 V,	I_O = −15 mA				
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA				
			V_I = 2.4 V,	I_O = −15 mA				

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$[‖]	$\overline{OE}$	A or B					MHz
t_{pd}[☆]	A or B	B or A					ns
t_{en}	$\overline{OE}$	A or B					ns
t_{dis}	$\overline{OE}$	A or B					ns

[‖] Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1$ MΩ, C_L = 0)

[☆] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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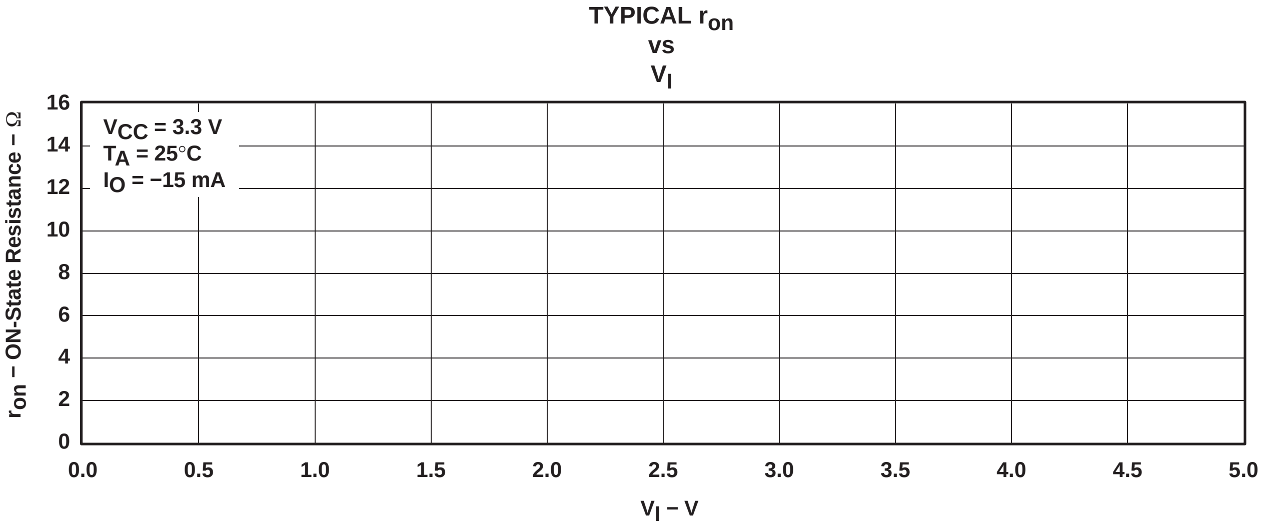


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

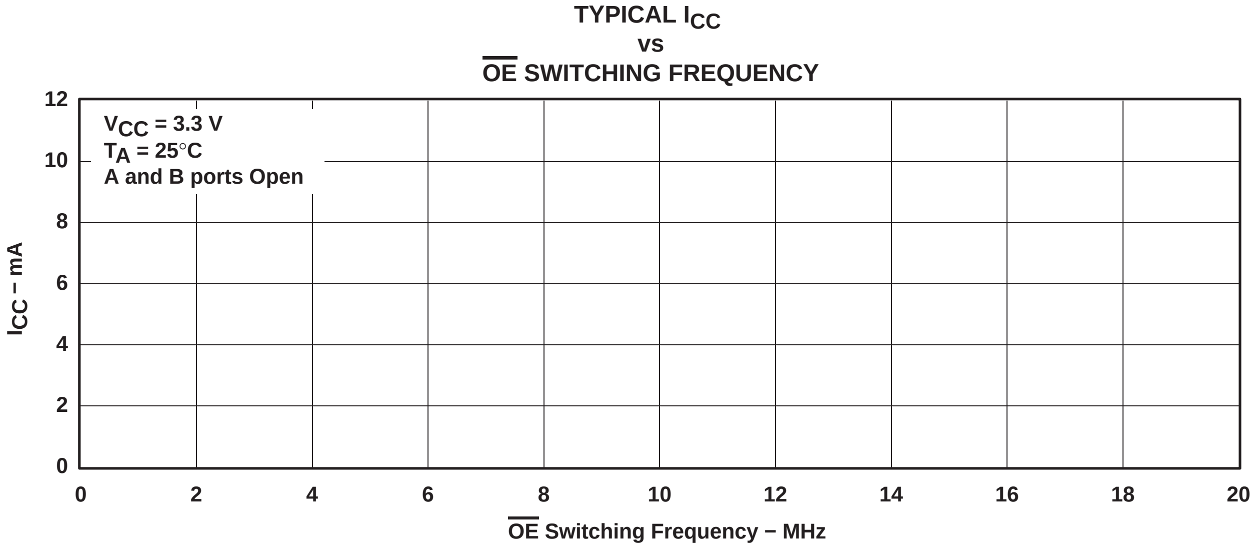
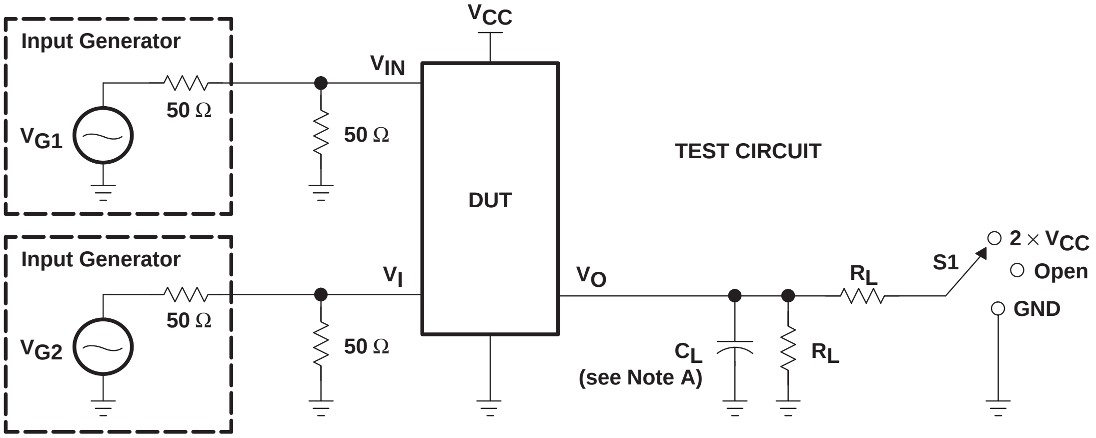


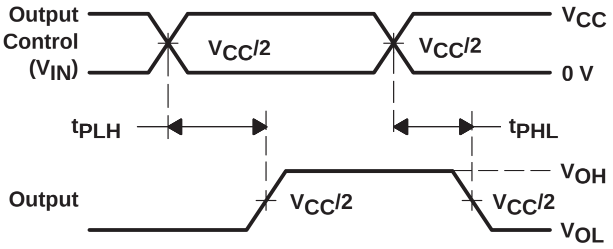
Figure 2. Typical I_{CC} vs $\overline{OE}$ Switching Frequency, V_{CC} = 3.3 V

PRODUCT PREVIEW

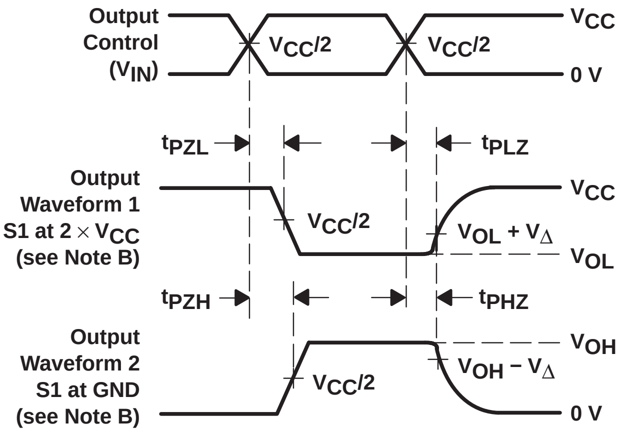
PARAMETER MEASUREMENT INFORMATION


VCC
Input Generator
VIN
50 Ω
VG1
50 Ω
TEST CIRCUIT
DUT
Input Generator
VI
VO
RL
S1
2 × VCC
Open
GND
50 Ω
VG2
50 Ω
CL
(see Note A)
RL

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V


Output
Control
(VIN)
VCC/2
VCC/2
VCC
0 V
tPLH
tPHL
VOH
Output
VCC/2
VCC/2
VOL

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)


Output
Control
(VIN)
VCC/2
VCC/2
VCC
0 V
tPZL
tPLZ
Output
Waveform 1
S1 at 2 × VCC
(see Note B)
VCC/2
VCC
VOL + VΔ
VOL
tPZH
tPHZ
Output
Waveform 2
S1 at GND
(see Note B)
VOH
VOH − VΔ
VCC/2
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

PRODUCT PREVIEW

SN74CB3Q16211
24-BIT FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

SCDS152A − OCTOBER 2003 − REVISED NOVEMBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **High-Bandwidth Data Path (Up To 500 MHz†)**
- **5-V-Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
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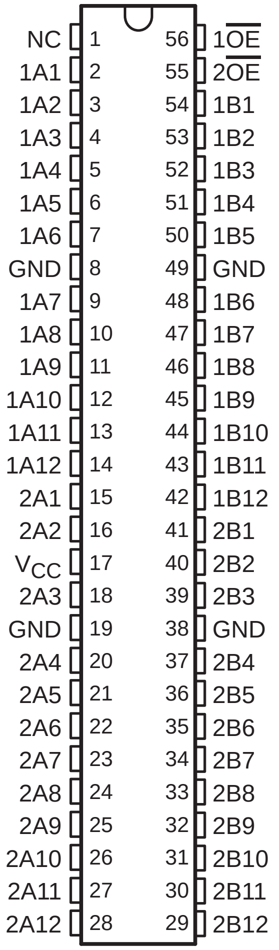
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

† For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NC 1 56 $1\overline{OE}$
1A1 2 55 $2\overline{OE}$
1A2 3 54 1B1
1A3 4 53 1B2
1A4 5 52 1B3
1A5 6 51 1B4
1A6 7 50 1B5
GND 8 49 GND
1A7 9 48 1B6
1A8 10 47 1B7
1A9 11 46 1B8
1A10 12 45 1B9
1A11 13 44 1B10
1A12 14 43 1B11
2A1 15 42 1B12
2A2 16 41 2B1
V_{CC} 17 40 2B2
2A3 18 39 2B3
GND 19 38 GND
2A4 20 37 2B4
2A5 21 36 2B5
2A6 22 35 2B6
2A7 23 34 2B7
2A8 24 33 2B8
2A9 25 32 2B9
2A10 26 31 2B10
2A11 27 30 2B11
2A12 28 29 2B12

NC − No internal connection

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PRODUCT PREVIEW

description/ordering information

The SN74CB3Q16211 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q16211 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q16211 is organized as two 12-bit bus switches with separate output-enable (1$\overline{OE}$, 2$\overline{OE}$) inputs. It can be used as two 12-bit bus switches, or as one 24-bit bus switch. When $\overline{OE}$ is low, the associated 12-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 12-bit bus switch is OFF and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

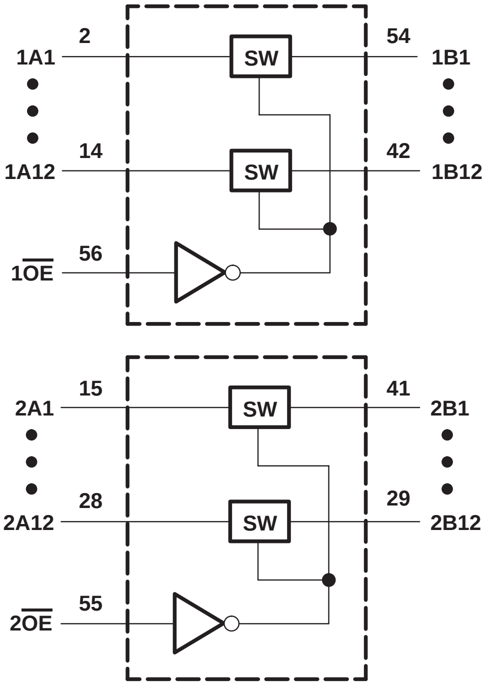
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CB3Q16211DL	
		Tape and reel	SN74CB3Q16211DLR	
	TSSOP − DGG	Tape and reel	SN74CB3Q16211DGGR	
	TVSOP − DGV	Tape and reel	SN74CB3Q16211DGVR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

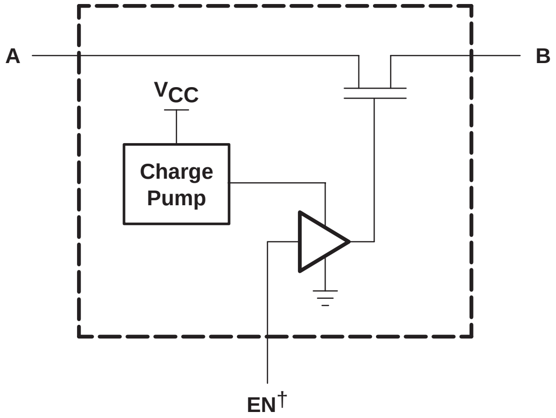
FUNCTION TABLE
(each 12-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)


1A1
2
SW
54
1B1
1A12
14
SW
42
1B12
1OE
56
2A1
15
SW
41
2B1
2A12
28
SW
29
2B12
2OE
55

simplified schematic, each FET switch (SW)


A
B
V_{CC}
Charge Pump
EN†

† EN is the internal enable signal applied to the switch.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±64 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA					V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V					µA
I_{OZ}[‡]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND				µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0				µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND				mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND				µA
I_{CCD}[¶]	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,					mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0					pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0				pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0				pF
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA				Ω
			V_I = 1.7 V,	I_O = −15 mA				
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA				
			V_I = 2.4 V,	I_O = −15 mA				

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$[‖]	$\overline{OE}$	A or B					MHz
t_{pd}[☆]	A or B	B or A					ns
t_{en}	$\overline{OE}$	A or B					ns
t_{dis}	$\overline{OE}$	A or B					ns

[‖] Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1\ M\Omega$, C_L = 0)

[☆] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PRODUCT PREVIEW

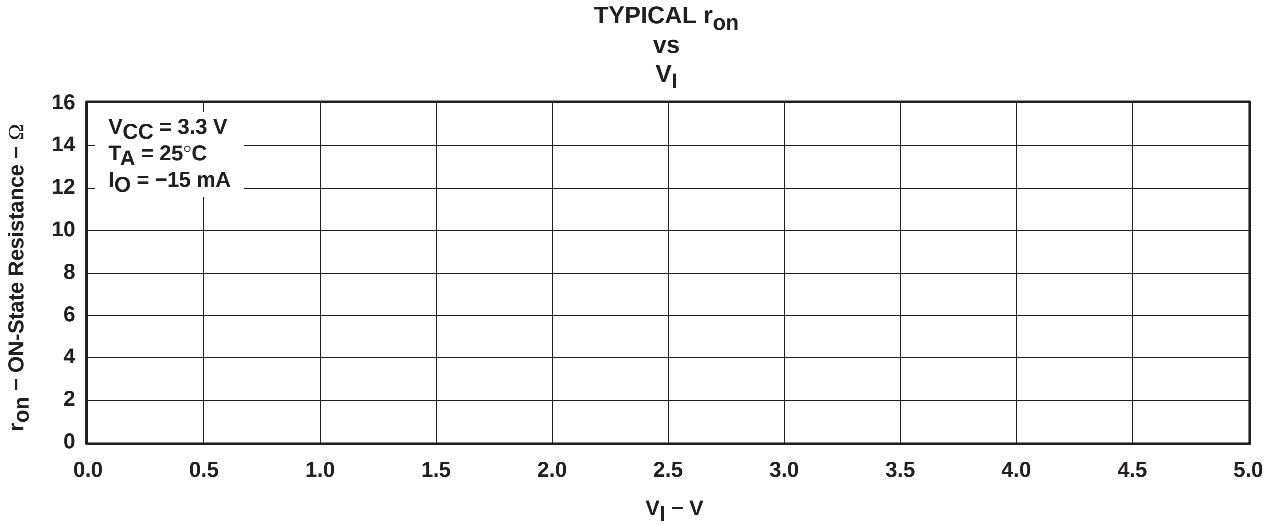


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

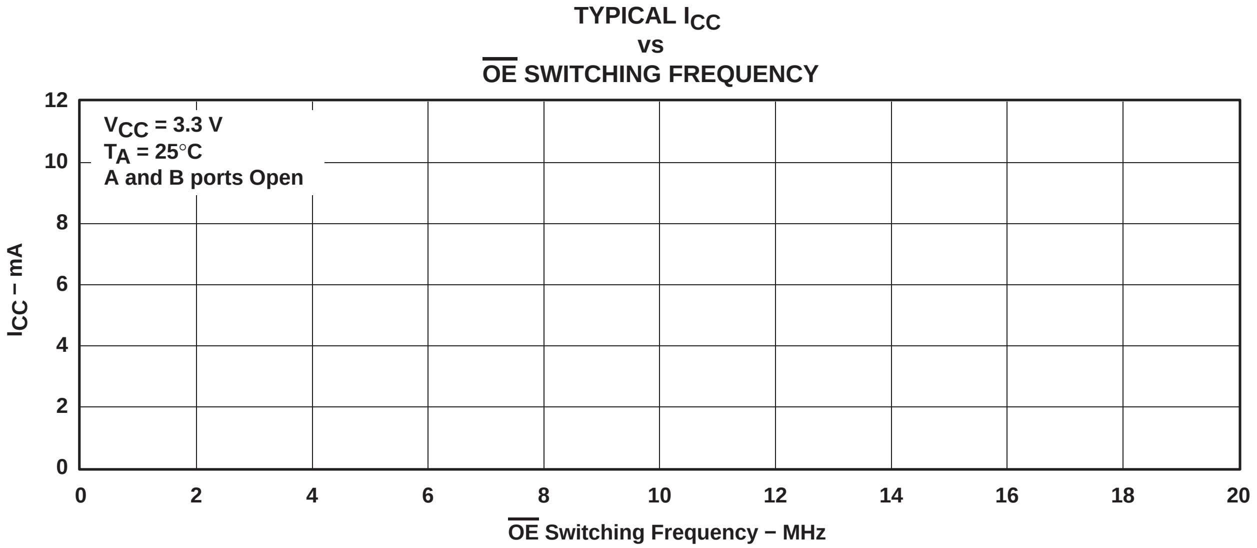
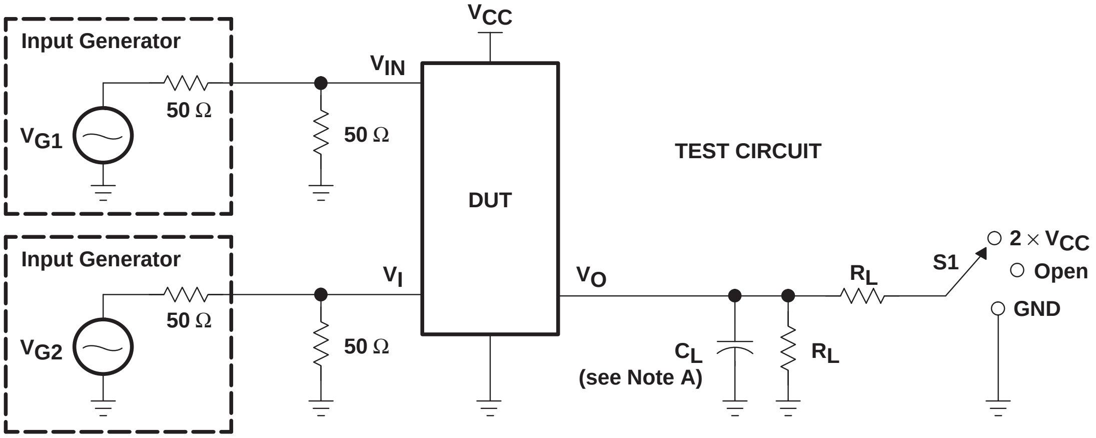
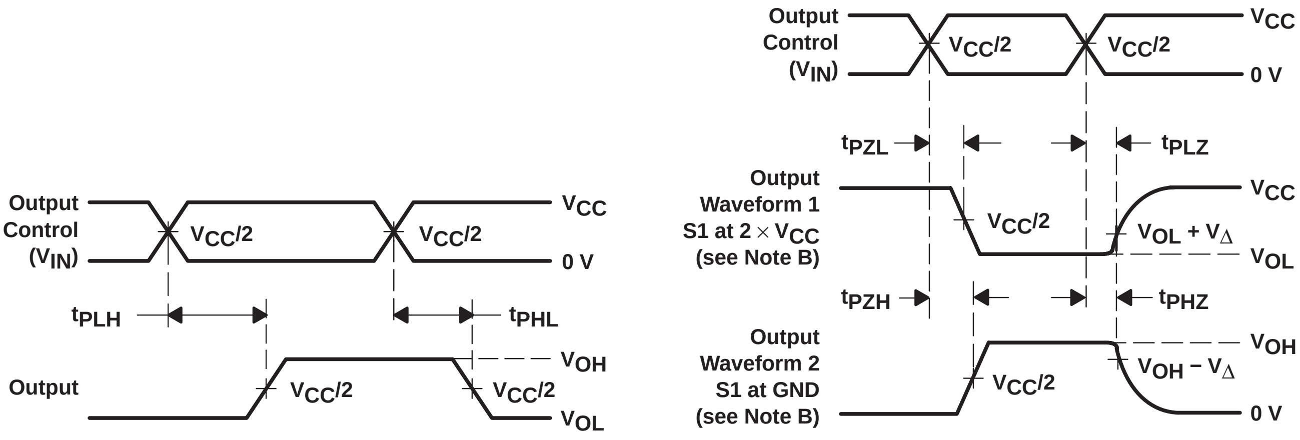


Figure 2. Typical I_{CC} vs $\overline{OE}$ Switching Frequency, V_{CC} = 3.3 V

PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
50 Ω
V_{IN}
Input Generator
V_{G2}
50 Ω
50 Ω
V_I
V_{CC}
DUT
TEST CIRCUIT
V_O
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
V_{CC}
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

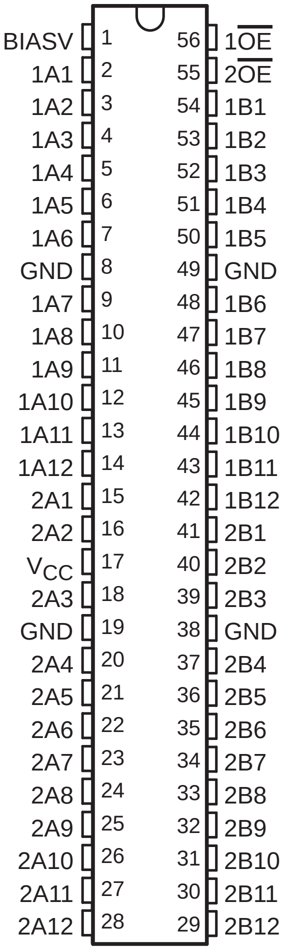
PRODUCT PREVIEW

SN74CB3Q16811
24-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS
2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

SCDS153A − OCTOBER 2003 − REVISED NOVEMBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **High-Bandwidth Data Path (Up To 500 MHz[†])**
- **5-V-Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
  - **0- to 3.3-V Switching With 2.5-V V_{CC}**
- **B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot-Plugging**
- **Supports PCI Hot Plug**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion**
- **Fast Switching Frequency**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



BIASV 1 56 1$\overline{\text{OE}}$
1A1 2 55 2$\overline{\text{OE}}$
1A2 3 54 1B1
1A3 4 53 1B2
1A4 5 52 1B3
1A5 6 51 1B4
1A6 7 50 1B5
GND 8 49 GND
1A7 9 48 1B6
1A8 10 47 1B7
1A9 11 46 1B8
1A10 12 45 1B9
1A11 13 44 1B10
1A12 14 43 1B11
2A1 15 42 1B12
2A2 16 41 2B1
V_{CC} 17 40 2B2
2A3 18 39 2B3
GND 19 38 GND
2A4 20 37 2B4
2A5 21 36 2B5
2A6 22 35 2B6
2A7 23 34 2B7
2A8 24 33 2B8
2A9 25 32 2B9
2A10 26 31 2B10
2A11 27 30 2B11
2A12 28 29 2B12

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[†] For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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PRODUCT PREVIEW

description/ordering information

The SN74CB3Q16811 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q16811 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q16811 is organized as two 12-bit bus switches with separate output-enable (1$\overline{\text{OE}}$, 2$\overline{\text{OE}}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When $\overline{\text{OE}}$ is low, the associated 12-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{\text{OE}}$ is high, the associated 12-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. The B port is precharged to BIASV through the equivalent of a 10-kΩ resistor when $\overline{\text{OE}}$ is high, or if the device is powered down (V_{CC} = 0 V).

During insertion (or removal) of a card into (or from) an active bus, the card's output voltage may be close to GND. When the connector pins make contact, the card's parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method will ensure that any glitch produced by insertion (or removal) of the card will not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

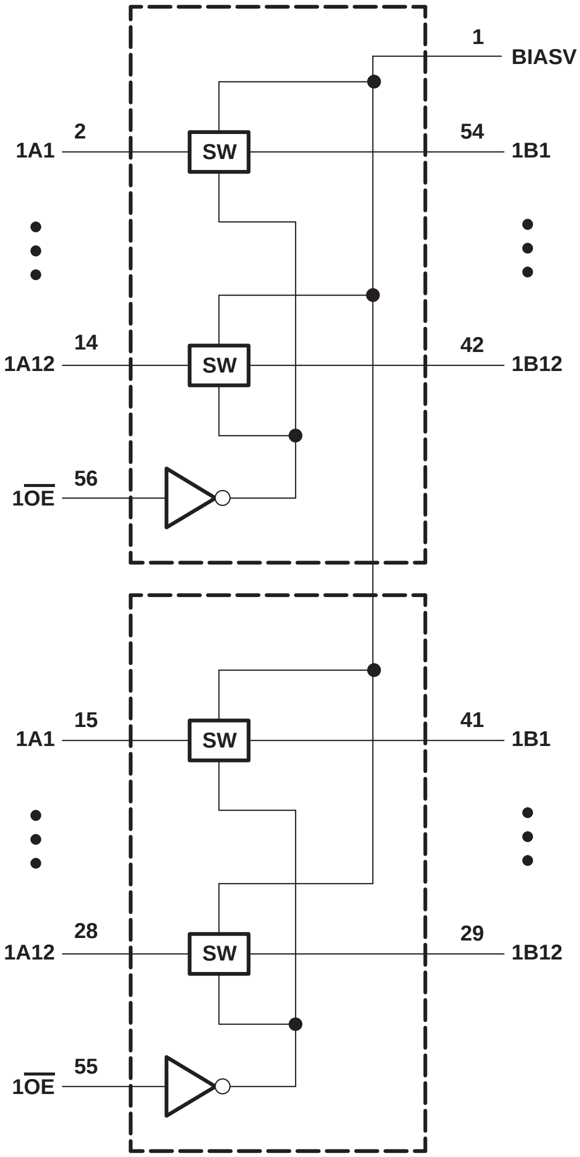
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CB3Q16811DL	
		Tape and reel	SN74CB3Q16811DLR	
	TSSOP − DGG	Tape and reel	SN74CB3Q16811DGGR	
	TVSOP − DGV	Tape and reel	SN74CB3Q16811DGVR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 12-bit bus switch)

INPUT $\overline{\text{OE}}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect B port = BIASV

logic diagram (positive logic)


1
BIASV
2
1A1
SW
54
1B1
14
1A12
SW
42
1B12
56
1OE
15
1A1
SW
41
1B1
28
1A12
SW
29
1B12
55
1OE

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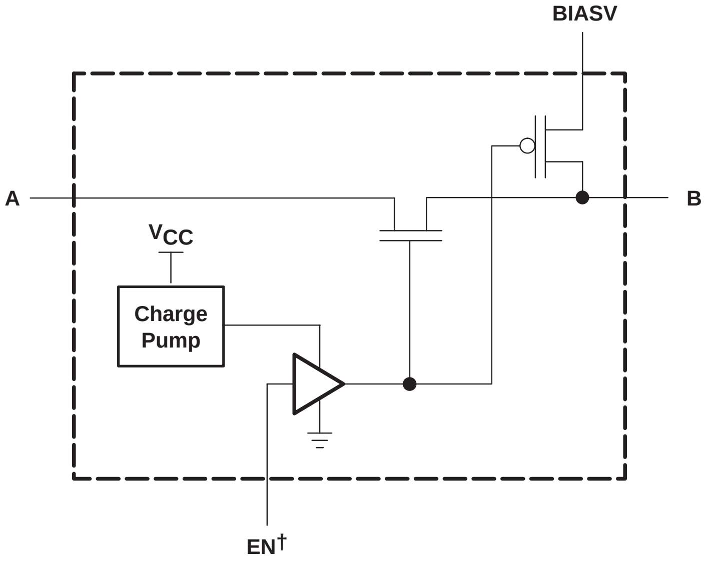
simplified schematic, each FET switch (SW)



[†] EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
BIAS supply voltage range, BIASV	−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±64 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DGG package	64°C/W
DGV package	48°C/W
DL package	56°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

[‡] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
BIASV	Bias supply voltage		0	5	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. BIASV is a supply voltage, not a control input.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA					V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V					µA
I_O	B port	V_{CC} = 3.V,	BIASV = 2.4 V, V_O = 0,	Switch OFF, V_{IN} = V_{CC} or GND				mA
I_{OZ}[‡]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND				µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0				µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND				mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND				µA
I_{CCD}[¶]	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,					mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0					pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0				pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0				pF
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA				Ω
			V_I = 1.7 V,	I_O = −15 mA				
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA				
			V_I = 2.4 V,	I_O = −15 mA				

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

PRODUCT PREVIEW

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$[†]		$\overline{OE}$	A or B					MHz
t_{pd}[‡]		A or B	B or A					ns
t_{PZH}	BIASV = GND	$\overline{OE}$	A or B					ns
t_{PZL}	BIASV = 3 V							
t_{PHZ}	BIASV = GND	$\overline{OE}$	A or B					ns
t_{PLZ}	BIASV = 3 V							

[†] Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1$ MΩ, C_L = 0).

[‡] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

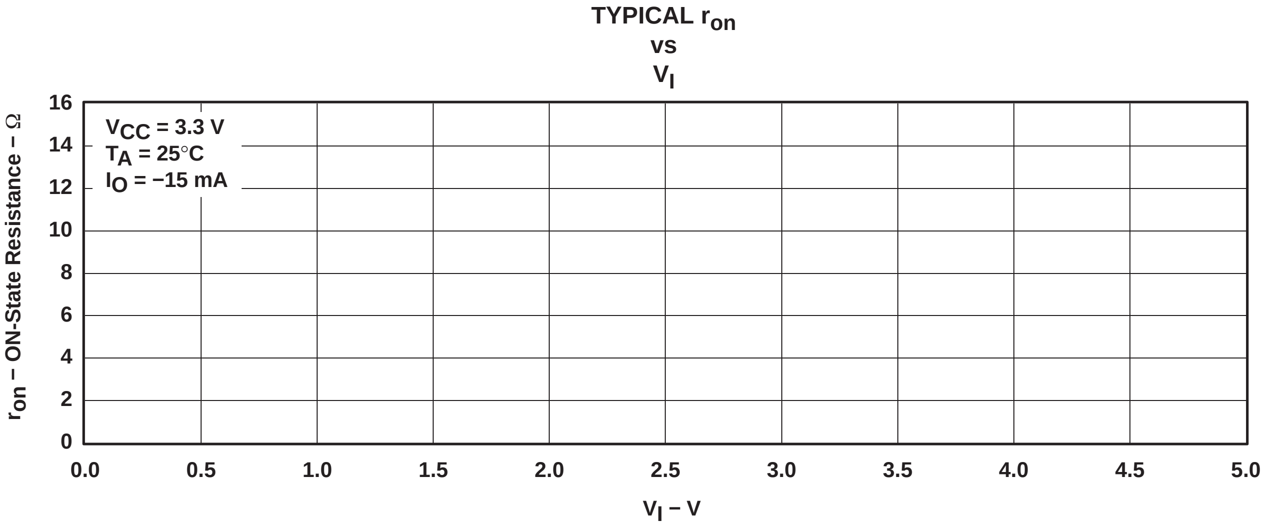


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

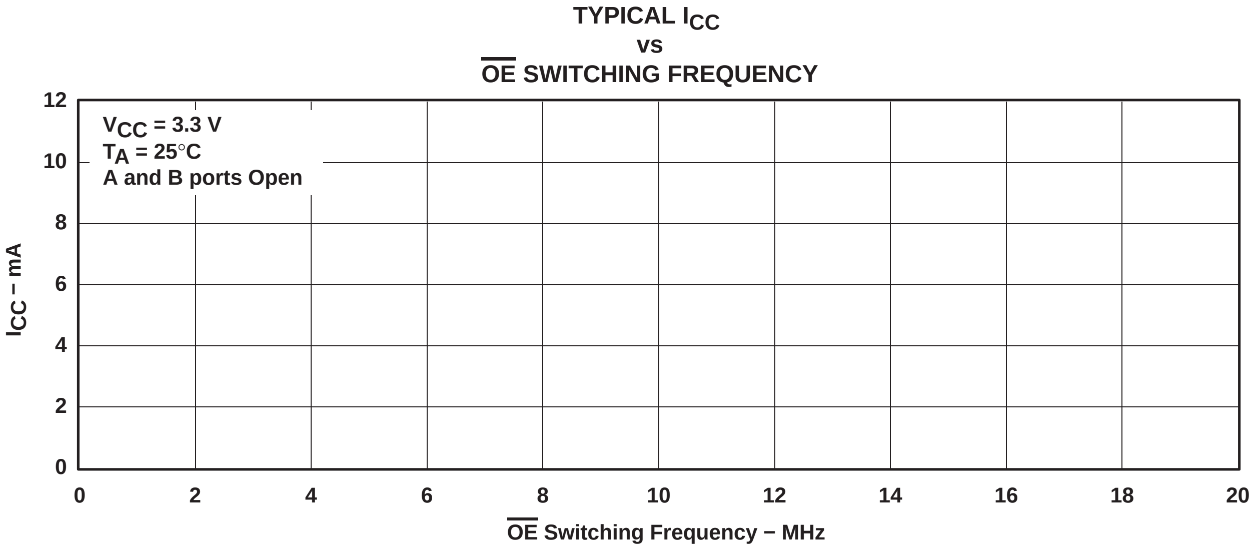
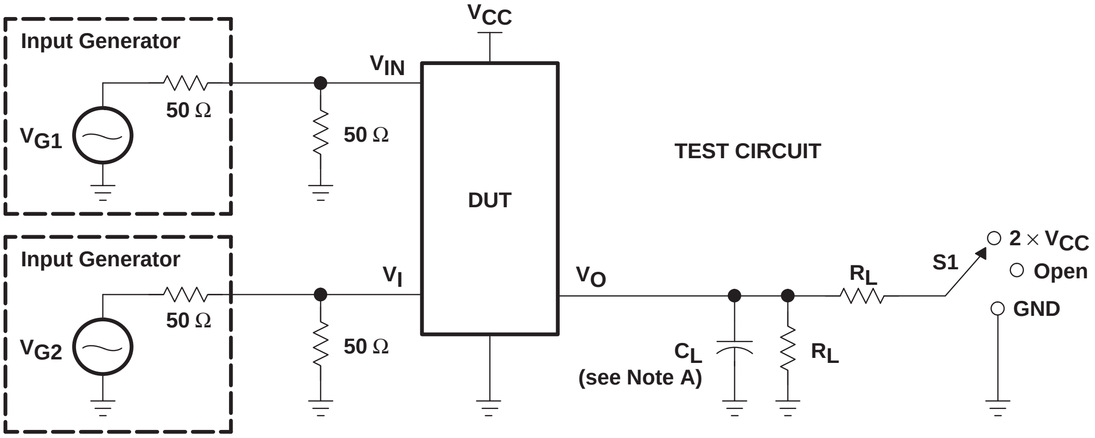


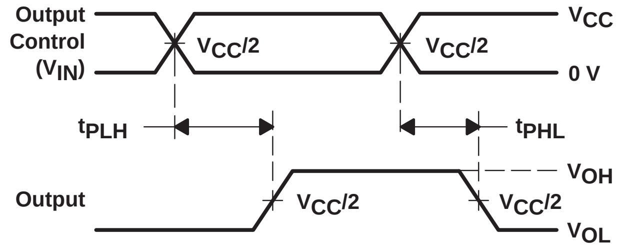
Figure 2. Typical I_{CC} vs $\overline{OE}$ Switching Frequency, V_{CC} = 3.3 V

PRODUCT PREVIEW

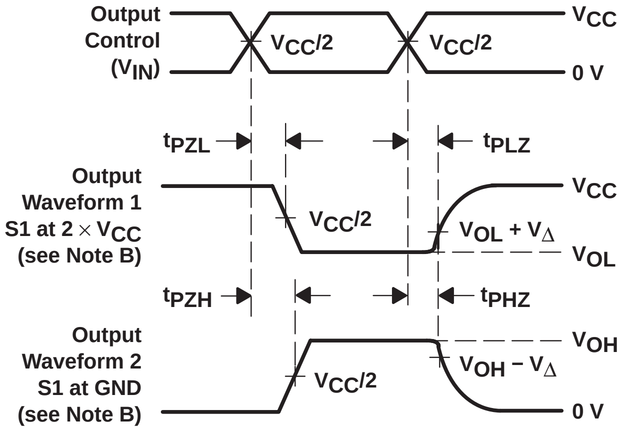
PARAMETER MEASUREMENT INFORMATION


VCC
Input Generator
VIN
50 Ω
VG1
50 Ω
TEST CIRCUIT
DUT
Input Generator
VI
VO
2 × VCC
S1
RL
Open
GND
50 Ω
VG2
50 Ω
CL
(see Note A)
RL

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V


Output
Control
(VIN)
VCC/2
VCC/2
VCC
0 V
tPLH
tPHL
VOH
Output
VCC/2
VCC/2
VOL

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)


Output
Control
(VIN)
VCC/2
VCC/2
VCC
0 V
tPZL
tPLZ
Output
Waveform 1
S1 at 2 × VCC
(see Note B)
VCC/2
VOL + VΔ
VCC
VOL
tPZH
tPHZ
Output
Waveform 2
S1 at GND
(see Note B)
VCC/2
VOH − VΔ
VOH
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

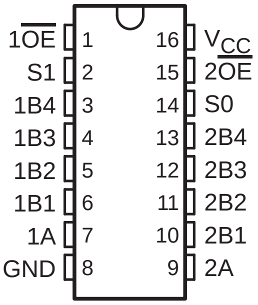
SN74CB3Q3253
DUAL 1-OF-4 FET MULTIPLEXER/DEMULTIPLEXER 2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

SCDS145A − OCTOBER 2003 − REVISED NOVEMBER 2003

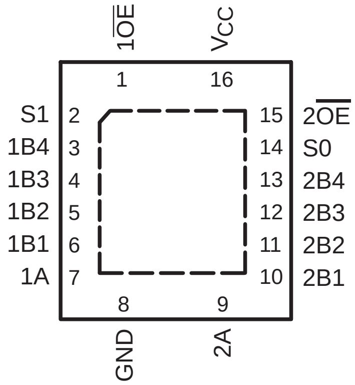
- **High-Bandwidth Data Path (Up To 500 MHz[†])**
- **5-V Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 4 Ω Typical)**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
  - **0- to 3.3-V Switching With 2.5-V V_{CC}**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 3.5 pF Typical)**
- **Fast Switching Frequency ($f_{\overline{OE}}$ = 20 MHz Max)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 0.6 mA Typical)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface Bus Isolation, Low-Distortion Signal Gating**

[†] For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

The SN74CB3Q3253 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3253 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The SN74CB3Q3253 is organized as two 1-of-4 multiplexers/demultiplexers with separate output-enable (1$\overline{\text{OE}}$, 2$\overline{\text{OE}}$) inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When $\overline{\text{OE}}$ is low, the associated multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{\text{OE}}$ is high, the associated multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

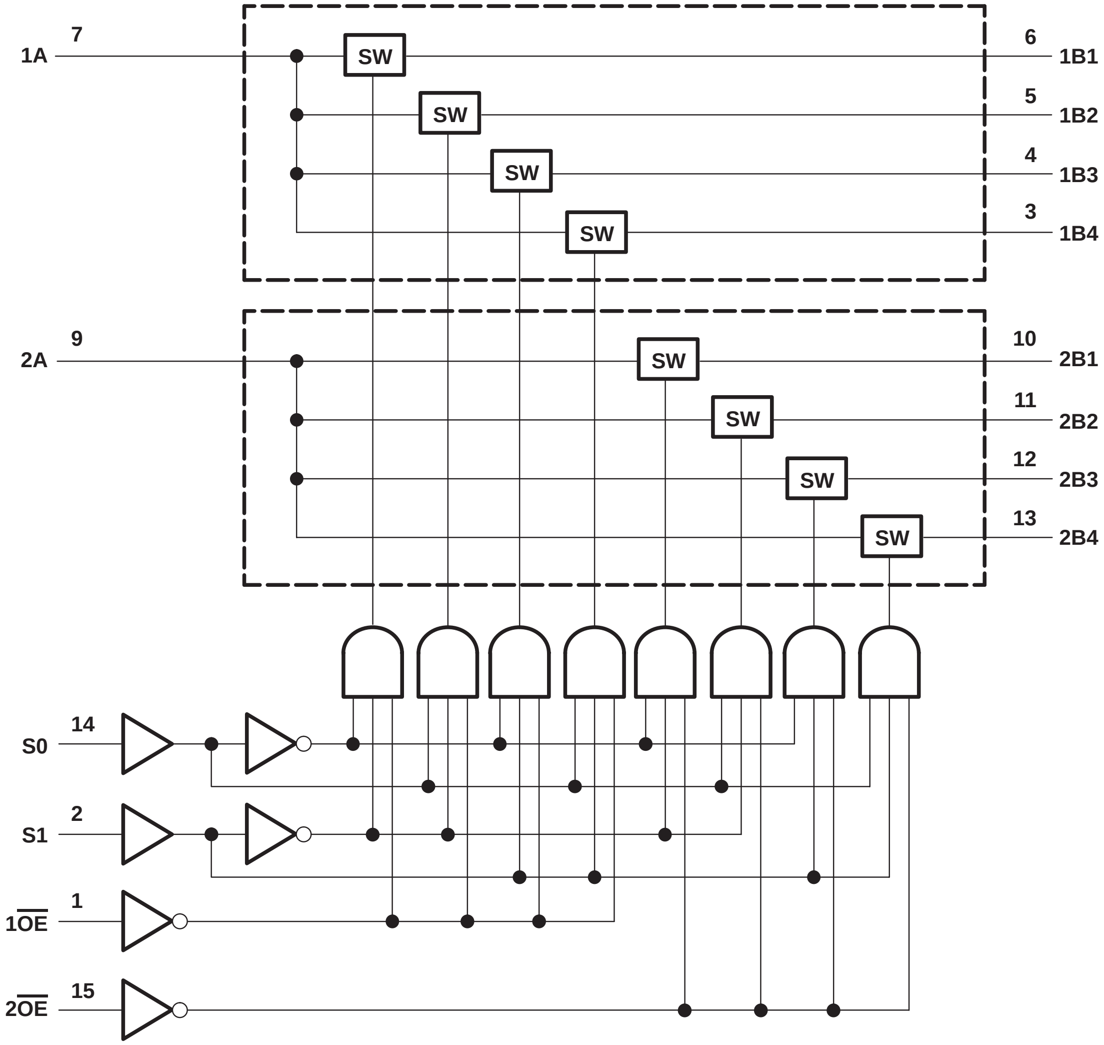
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CB3Q3253RGYR	BU253
	SSOP (QSOP) − DBQ	Tape and reel	SN74CB3Q3253DBQR	BU253
	TSSOP − PW	Tube	SN74CB3Q3253PW	BU253
		Tape and reel	SN74CB3Q3253PWR	
	TVSOP − DGV	Tape and reel	SN74CB3Q3253DGVR	BU253

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

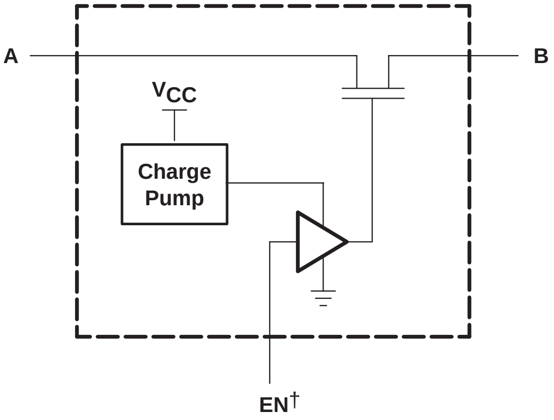
FUNCTION TABLE
(each multiplexer/demultiplexer)

INPUTS			INPUT/OUTPUT A	FUNCTION
$\overline{\text{OE}}$	S1	S0		
L	L	L	B1	A port = B1 port
L	L	H	B2	A port = B2 port
L	H	L	B3	A port = B3 port
L	H	H	B4	A port = B4 port
H	X	X	Z	Disconnect

logic diagram (positive logic)


1A
7
SW
SW
SW
SW
6
1B1
5
1B2
4
1B3
3
1B4
2A
9
SW
SW
SW
SW
10
2B1
11
2B2
12
2B3
13
2B4
S0
14
S1
2
1OE
1
2OE
15

simplified schematic, each FET switch (SW)


A
B
V_{CC}
Charge Pump
EN†

† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±64 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DBQ package	90°C/W
(see Note 5):	DGV package	120°C/W
(see Note 5):	PW package	108°C/W
(see Note 6):	RGY package	39°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA				−1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	μA
I_{OZ}[‡]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	μA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		0.6	2	mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			30	μA
I_{CCD}[¶]	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,	$\overline{\text{OE}}$ input		0.15	0.16	mA/ MHz
				S input		0.04	0.05	
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		8	11	pF
	B port	V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		3.5	4.5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		13	17	pF
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		4	10	Ω
			V_I = 1.7 V,	I_O = −15 mA		4.5	11	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		3.5	8	
			V_I = 2.4 V,	I_O = −15 mA		4	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$ or f_S[‖]	$\overline{\text{OE}}$ or S	A or B		10		20	MHz
t_{pd}[☆]	A or B	B or A		0.12		0.18	ns
$t_{pd(s)}$	S	A	1.5	6.7	1.5	5.9	ns
t_{en}	S	B	1.5	6.7	1.5	5.9	ns
	$\overline{\text{OE}}$	A or B	1.5	6.7	1.5	5.9	
t_{dis}	S	B	1	6.1	1	6.1	ns
	$\overline{\text{OE}}$	A or B	1	6.1	1	6.1	

[‖] Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1$ MΩ, C_L = 0).

[☆] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

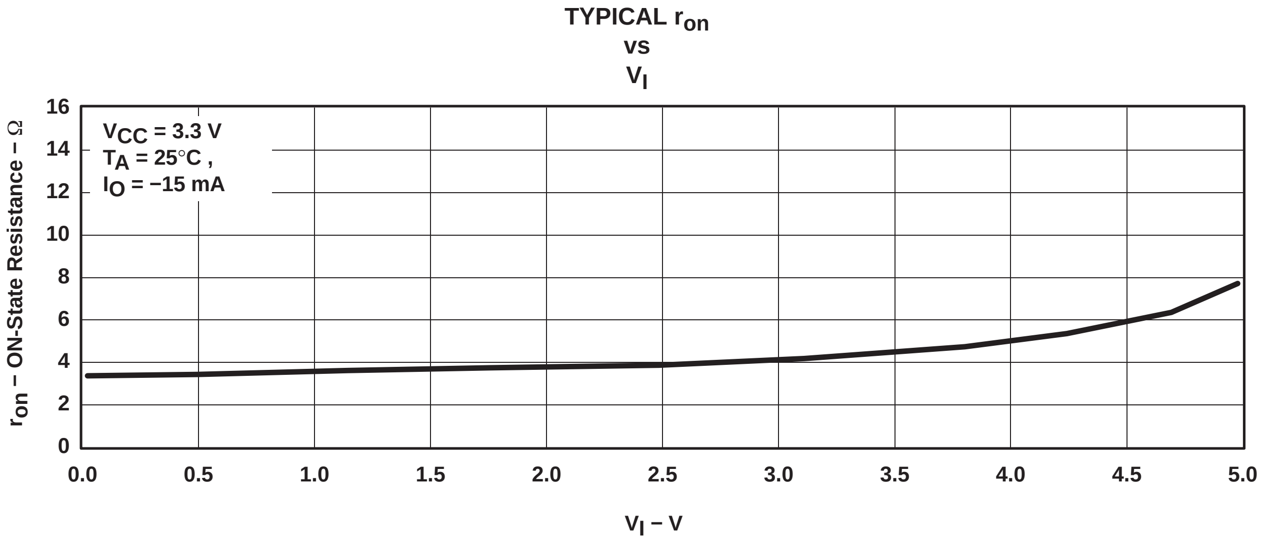


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

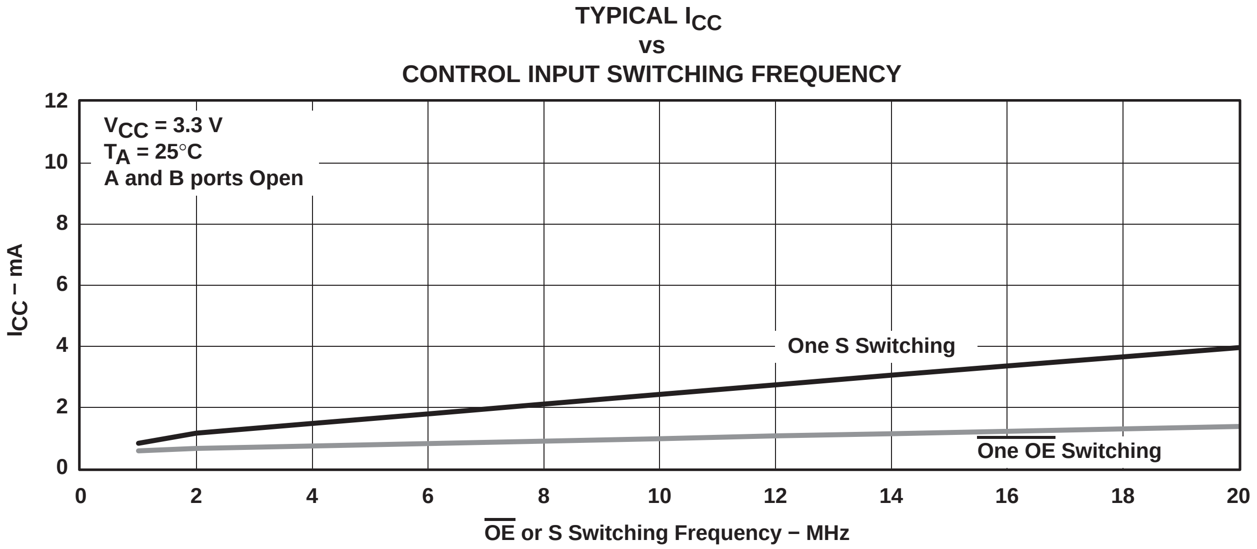
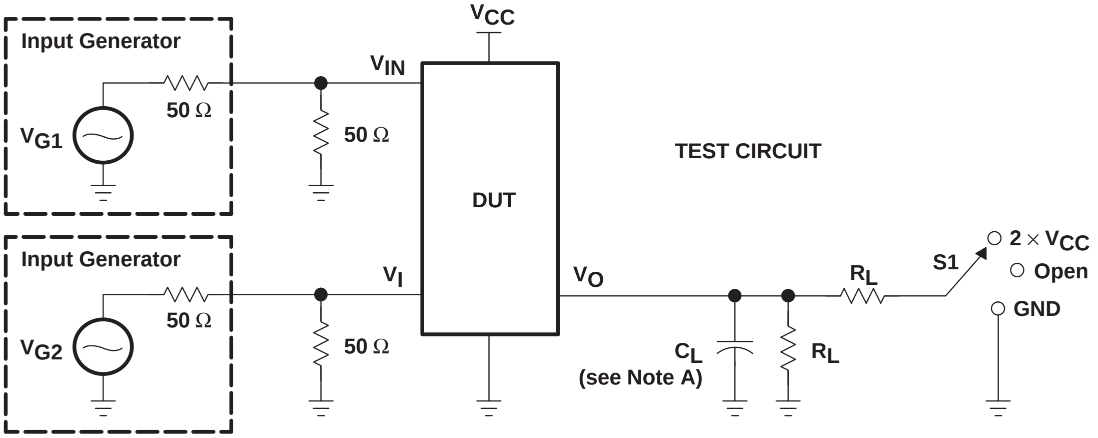
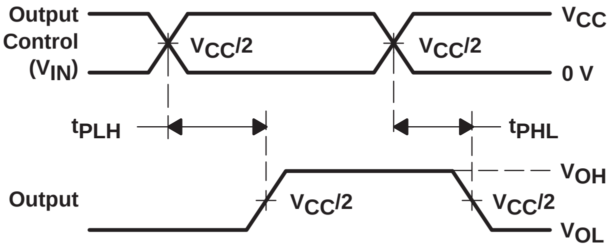


Figure 2. Typical I_{CC} vs $\overline{\text{OE}}$ or S Switching Frequency, V_{CC} = 3.3 V

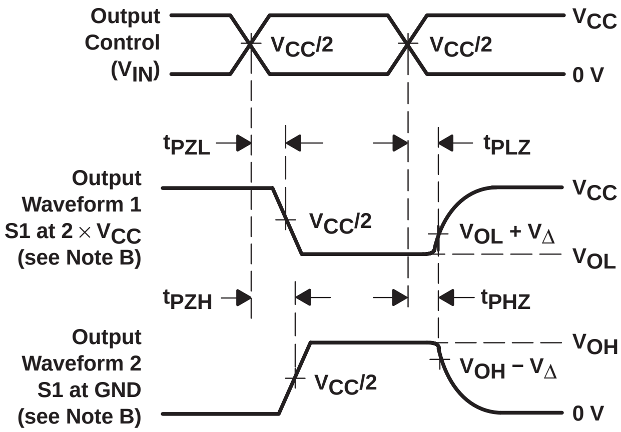
PARAMETER MEASUREMENT INFORMATION


V_{CC}
Input Generator
V_{G1}
50 Ω
50 Ω
V_{IN}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
50 Ω
V_I
V_O
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

SN74CB3Q3257
4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER
2.5-V/3.3-V LOW-VOLTAGE, HIGH-BANDWIDTH BUS SWITCH

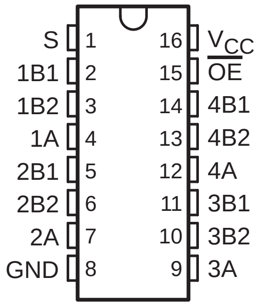
SCDS135A – SEPTEMBER 2003 − REVISED NOVEMBER 2003

- **High-Bandwidth Data Path (Up to 500 MHz†)**
- **5-V Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 4 Ω Typical)**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
  - **0- to 3.3-V Switching With 2.5-V V_{CC}**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 3.5 pF Typical)**
- **Fast Switching Frequency ($f_{\overline{OE}}$ = 20 MHz Max)**

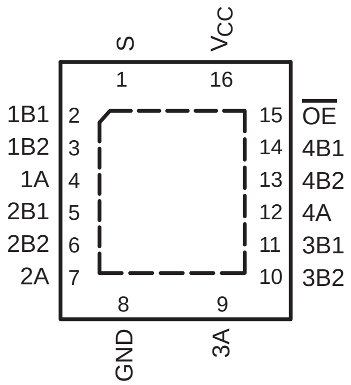
† For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 0.7 mA Typical)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface, Bus Isolation, Low-Distortion Signal Gating**

DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CB3Q3257RGYR	BU257
	SSOP (QSOP) − DBQ	Tape and reel	SN74CB3Q3257DBQR	BU257
	TSSOP − PW	Tape and reel	SN74CB3Q3257PWR	BU257
	TVSOP − DGV	Tape and reel	SN74CB3Q3257DGVR	BU257

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

description/ordering information (continued)

The SN74CB3Q3257 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3257 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3257 is a 4-bit 1-of-2 high-speed FET multiplexer/demultiplexer with a single output-enable ($\overline{OE}$) input. The select (S) input controls the data path of the multiplexer/demultiplexer. When $\overline{OE}$ is low, the multiplexer/demultiplexer is enabled and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the multiplexer/demultiplexer is disabled and a high-impedance state exists between the A and B ports.

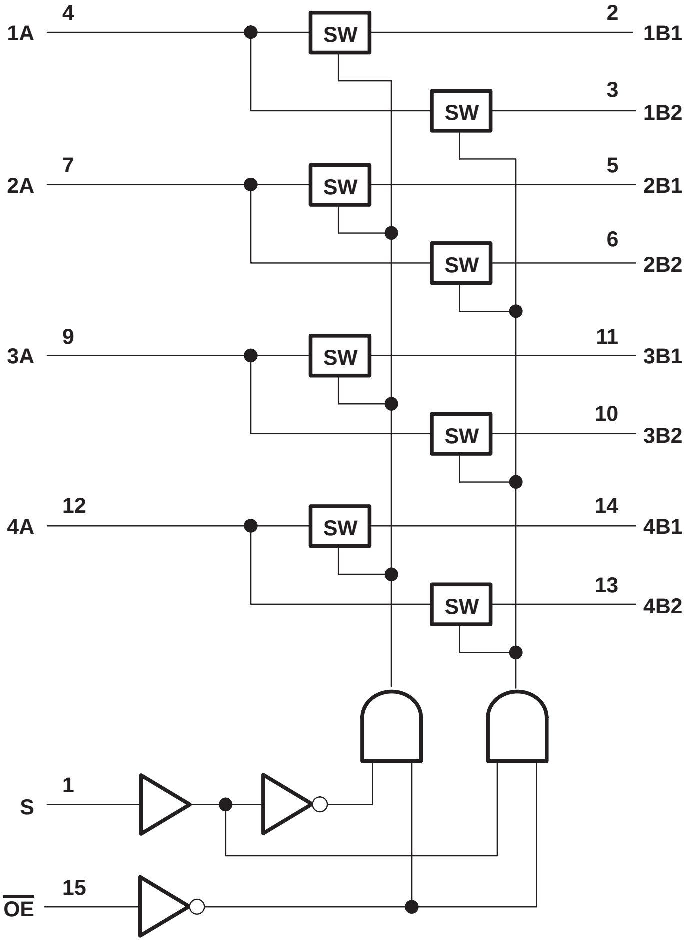
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered-down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

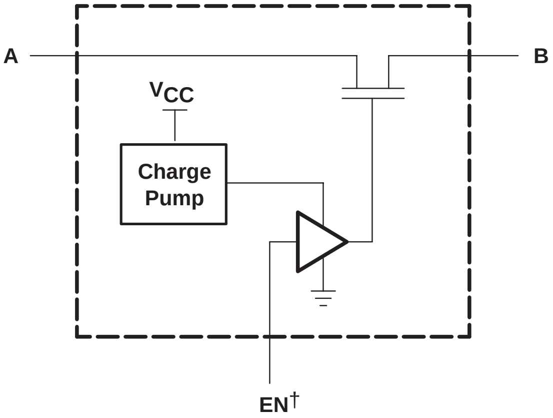
FUNCTION TABLE

INPUTS		INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S		
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect

logic diagram (positive logic)


1A
4
2
1B1
3
1B2
2A
7
5
2B1
6
2B2
3A
9
11
3B1
10
3B2
4A
12
14
4B1
13
4B2
SW
S
1
OE
15

simplified schematic, each FET switch (SW)


A
B
V_{CC}
Charge Pump
EN†

† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, I_{IO} (see Note 4)	±64 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): D package	73°C/W
(see Note 5): DB package	82°C/W
(see Note 5): DBQ package	90°C/W
(see Note 5): DGV package	120°C/W
(see Note 5): PW package	108°C/W
(see Note 6): RGY package	39°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA				−1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	μA
I_{OZ}[‡]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	μA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		0.7	1.5	mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			30	μA
I_{CCD}[¶]	Per control input	V_{CC} = 3.6 V, A and B ports open, Control input switching at 50% duty cycle				0.3	0.35	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		5.5	7	pF
	B port	V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		3.5	5	pF
$C_{io(ON)}$	A port	V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		10.5	13	pF
	B port					10.5	13	
r_{on}[#]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		4	8	Ω
			V_I = 1.7 V,	I_O = −15 mA		4	9	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		4	6	
			V_I = 2.4 V,	I_O = −15 mA		4	8	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$ or f_S[‖]	$\overline{OE}$ or S	A or B		10		20	MHz
t_{pd}[☆]	A or B	B or A		0.12		0.2	ns
$t_{pd(s)}$	S	A	1.5	6.5	1.5	5.5	ns
t_{en}	S	B	1.5	6.5	1.5	5.5	ns
	$\overline{OE}$	A or B	1.5	6.5	1.5	5.5	
t_{dis}	S	B	1	6	1	6	ns
	$\overline{OE}$	A or B	1	6	1	6	

[‖] Maximum switching frequency for control inputs ($V_O > V_{CC}$, V_I = 5 V, $R_L \geq 1$ MΩ, C_L = 0).

[☆] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

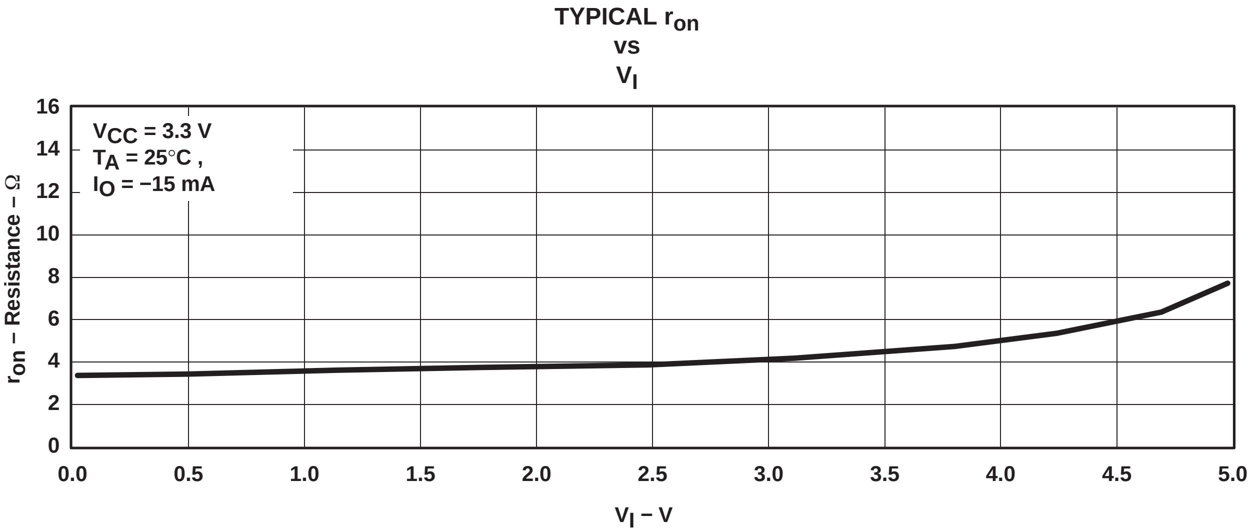


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

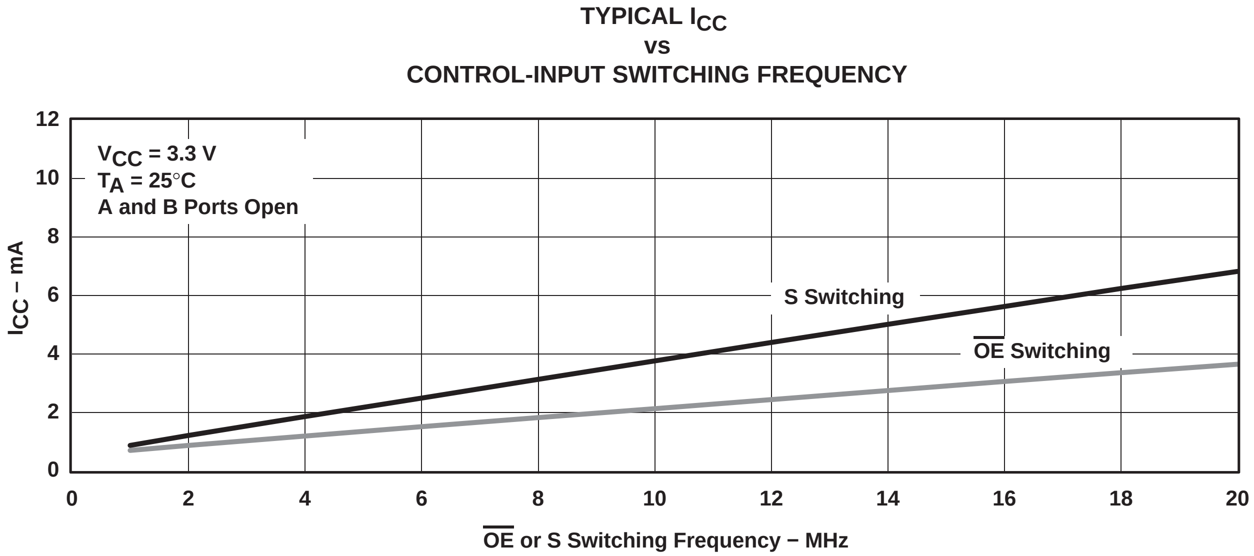
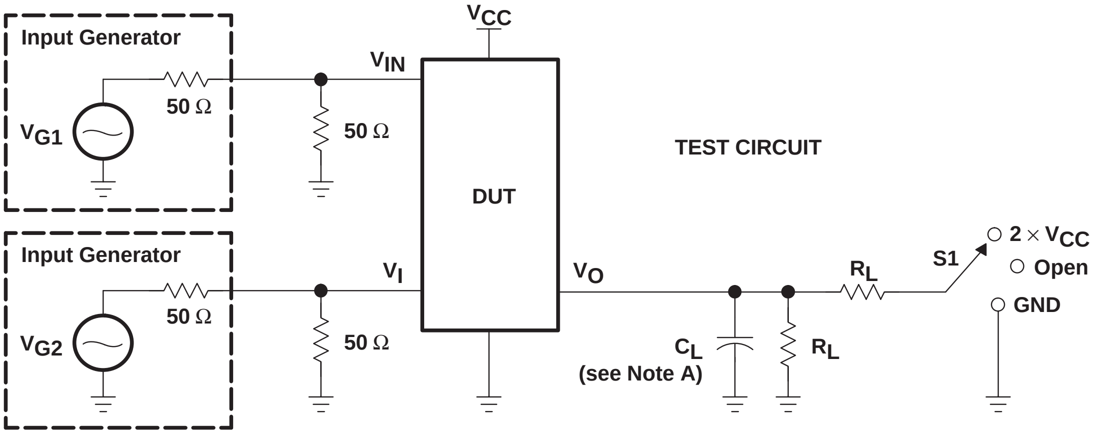
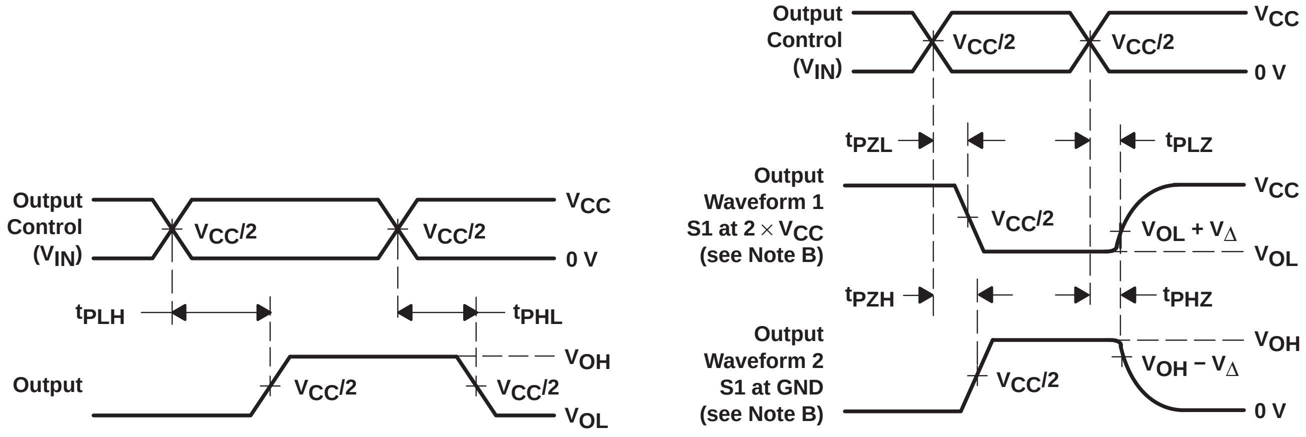


Figure 2. Typical I_{CC} vs $\overline{OE}$ or S Switching Frequency, V_{CC} = 3.3 V

PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
50 Ω
V_{IN}
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
50 Ω
V_I
V_O
C_L
(see Note A)
R_L
R_L
S1
○ 2 × V_{CC}
○ Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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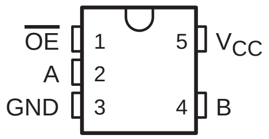
SN74CB3T1G125
SINGLE FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS150 − OCTOBER 2003

- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation On All Data I/O Ports**
  - **5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}**
- **5-V Tolerant I/Os With Device Powered-Up or Powered-Down**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 5 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 20 µA Max)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, USB Interface, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

DBV OR DCK PACKAGE
(TOP VIEW)



description/ordering information

The SN74CB3T1G125 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T1G125 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

The SN74CB3T1G125 is a 1-bit bus switch with a single ouput-enable ($\overline{OE}$) input. When $\overline{OE}$ is low, the bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the bus switch is OFF, and a high-impedance state exists between the A and B ports.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	SOT (SOT-23) − DBV	Tape and reel	SN74CB3T1G125DBVR	W25_
	SOT (SC-70) − DCK	Tape and reel	SN74CB3T1G125DCKR	WM_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ The actual top-side marking has one additional character that designates the assembly/test site.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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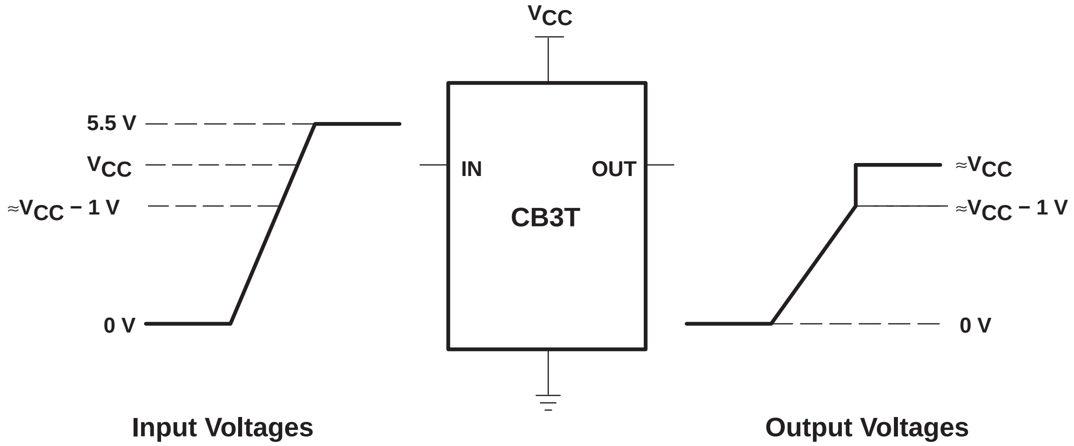
description/ordering information (continued)


V_{CC}
5.5 V
V_{CC}
$\approx V_{CC} - 1$ V
0 V
IN
OUT
CB3T
$\approx V_{CC}$
$\approx V_{CC} - 1$ V
0 V
Input Voltages
Output Voltages

NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} − 1 V, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage-Translation Characteristics

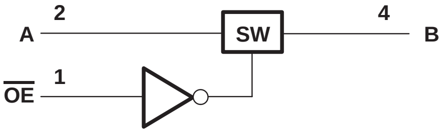
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

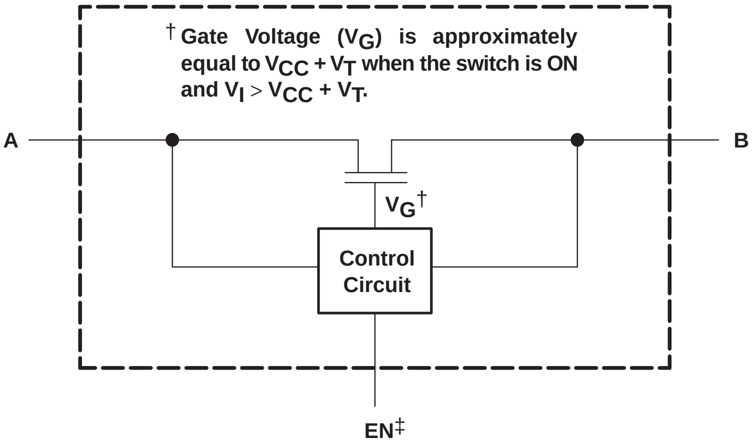
FUNCTION TABLE

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)


A
2
SW
4
B
$\overline{OE}$
1

simplified schematic, each FET switch (SW)



† Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.

‡ EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} (see Note 1)		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DBV package	206°C/W
	DCK package	252°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = −18 mA				−1.2	V
V_{OH}		See Figures 3 and 4					
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 3.6 V to 5.5 V or GND				±10	µA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} − 0.7 V to 5.5 V			±20	µA
			V_I = 0.7 V to V_{CC} − 0.7 V			−40	
			V_I = 0 to 0.7 V			±5	
I_{OZ}‡		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND				±10	µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0,				10	µA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND			20	µA
			V_I = 5.5 V			20	
ΔI_{CC}§	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				300	µA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND			3		pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND			5		pF
$C_{io(ON)}$		V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V		4		pF
			$V_{I/O}$ = GND		12		
r_{on}¶		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA		5	8	Ω
			I_O = 16 mA		5	8	
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA		5	7	
			I_O = 32 mA		5	7	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

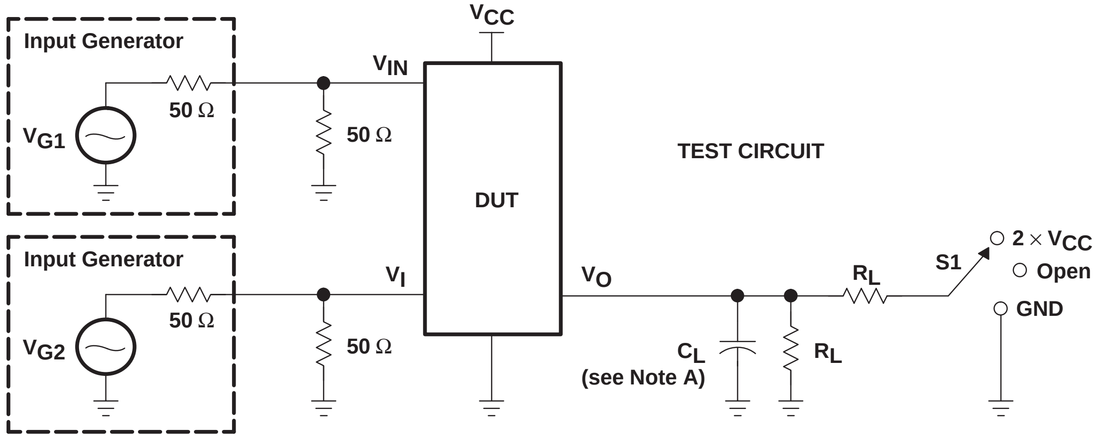
¶ Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

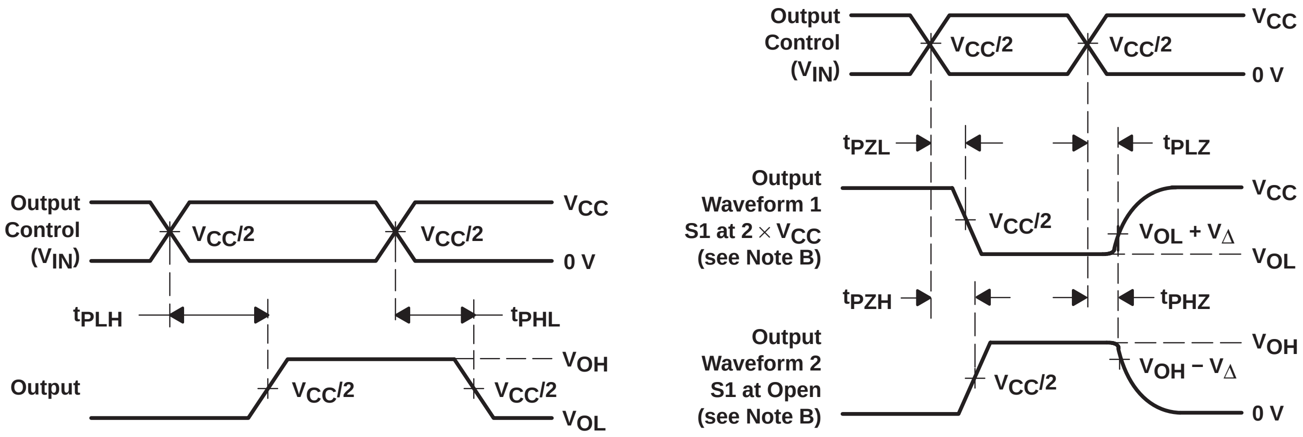
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	7.5	1	6.5	ns
t_{dis}	$\overline{OE}$	A or B	1	5.5	1	6	ns

[†] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION


V_{CC}
Input Generator
V_{IN}
50 Ω
V_{G1}
50 Ω
TEST CIRCUIT
DUT
Input Generator
V_I
V_O
R_L
S1
2 × V_{CC}
Open
GND
50 Ω
V_{G2}
50 Ω
C_L
(see Note A)
R_L

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

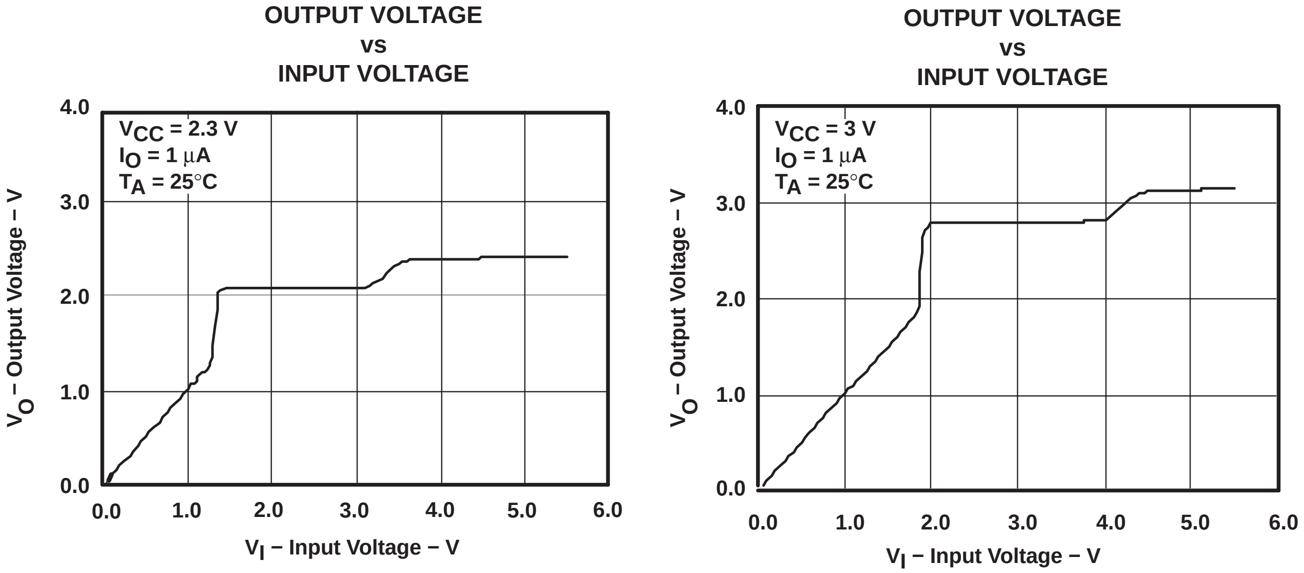


Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS (continued)

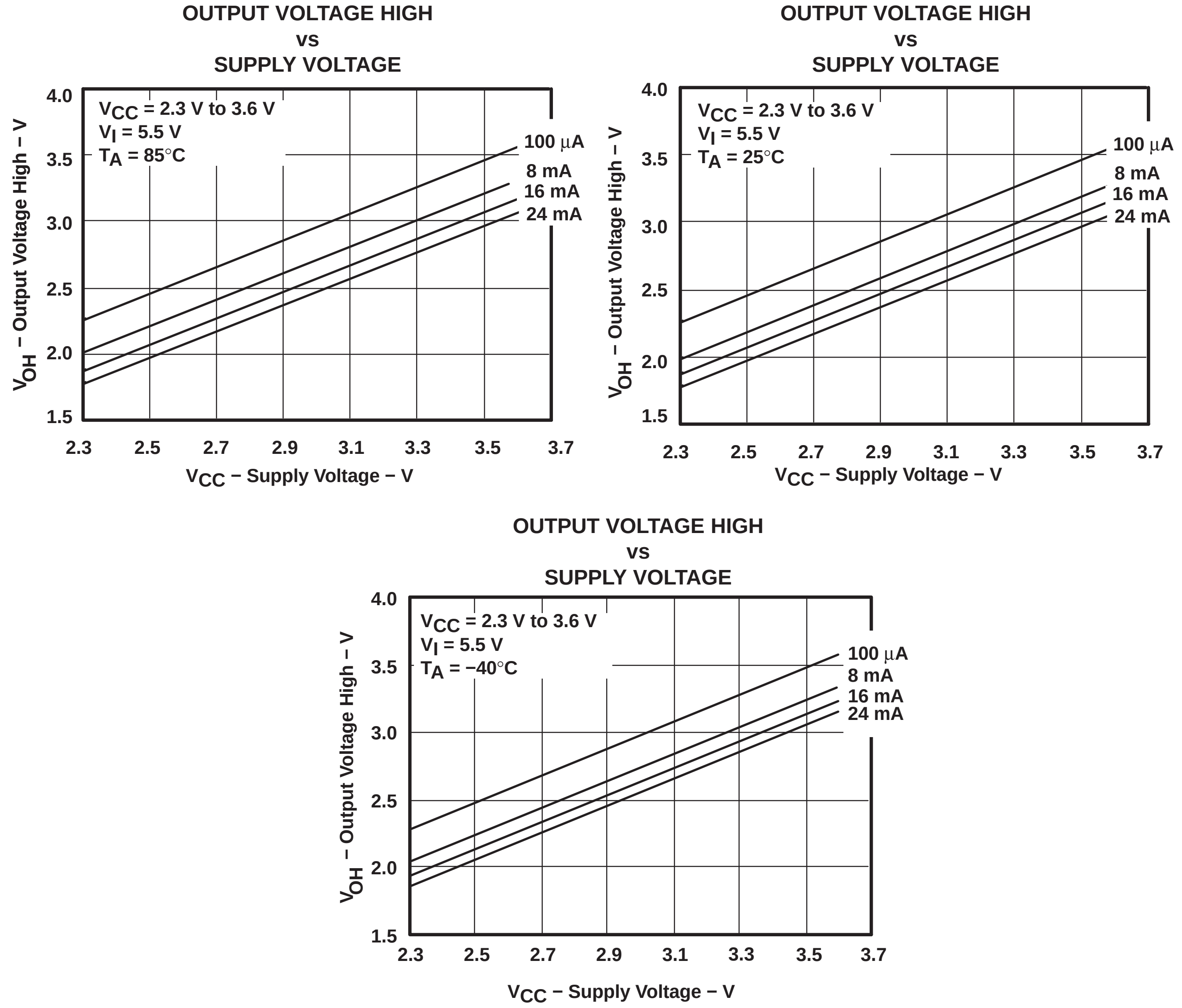


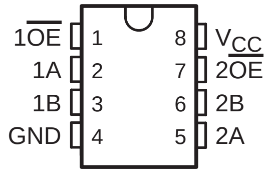
Figure 4. V_{OH} Values

SN74CB3T3306
DUAL FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS119A − JANUARY 2003 − REVISED OCTOBER 2003

- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation On All Data I/O Ports**
  - **5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}**
- **5-V Tolerant I/Os With Device Powered-Up or Powered-Down**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 5 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 4.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 20 μA Max)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, USB Interface, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

DCT OR DCU PACKAGE
(TOP VIEW)



description/ordering information

The SN74CB3T3306 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3306 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

The SN74CB3T3306 is organized as two 1-bit bus switches with separate ouput-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When $\overline{OE}$ is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	SSOP − DCT	Tape and reel	SN74CB3T3306DCTR	WA6_ _ _
	VSSOP − DCU	Tape and reel	SN74CB3T3306DCUR	WA6_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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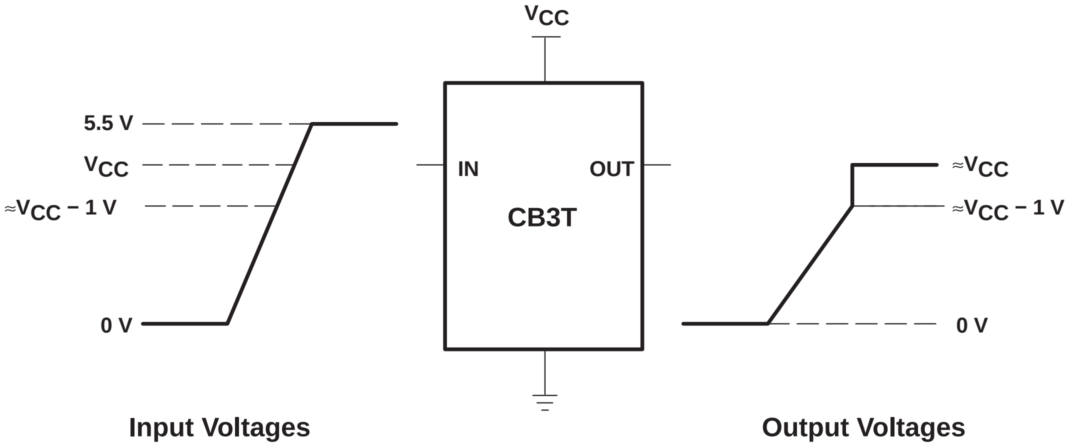
description/ordering information (continued)


V_{CC}
5.5 V
V_{CC}
≈V_{CC} − 1 V
0 V
IN
OUT
CB3T
≈V_{CC}
≈V_{CC} − 1 V
0 V
Input Voltages
Output Voltages

NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} − 1 V, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage-Translation Characteristics

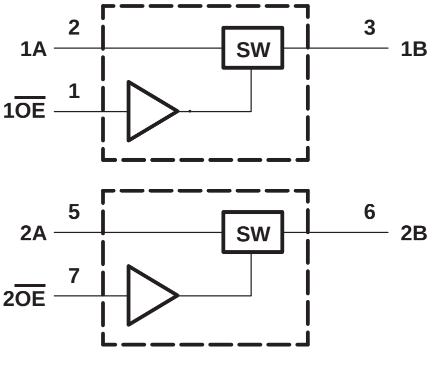
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

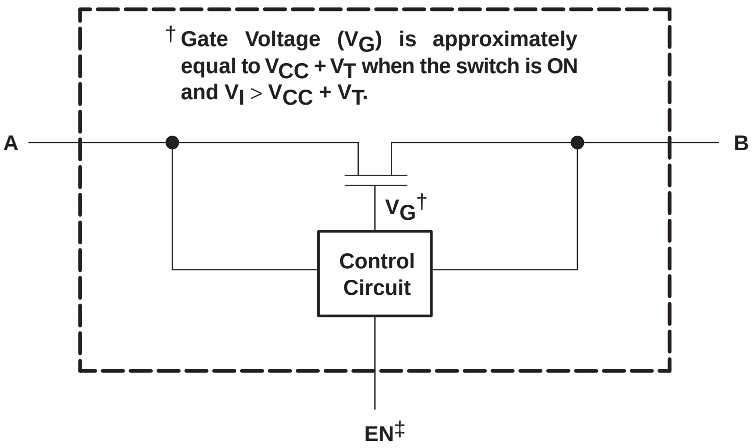
FUNCTION TABLE
(each bus switch)

INPUT $\overline{\text{OE}}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)


2
3
1A
SW
1B
1
$1\overline{\text{OE}}$
5
6
2A
SW
2B
7
$2\overline{\text{OE}}$

simplified schematic, each FET switch (SW)


† Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
A
B
V_G†
Control Circuit
EN‡

‡ EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} (see Note 1)		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DCT package	220°C/W
	DCU package	227°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = −18 mA				−1.2	V
V_{OH}		See Figures 3 and 4					
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 3.6 V to 5.5 V or GND				±10	μA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} − 0.7 V to 5.5 V			±20	μA
			V_I = 0.7 V to V_{CC} − 0.7 V			−40	
			V_I = 0 to 0.7 V			±5	
I_{OZ}‡		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND				±10	μA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0,				10	μA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND			20	μA
			V_I = 5.5 V			20	
ΔI_{CC}§	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				300	μA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND			3		pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND			4.5		pF
$C_{io(ON)}$		V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V		4		pF
			$V_{I/O}$ = GND		15		
r_{on}¶		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA		5	8	Ω
			I_O = 16 mA		5	8	
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA		5	7	
			I_O = 32 mA		5	7	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

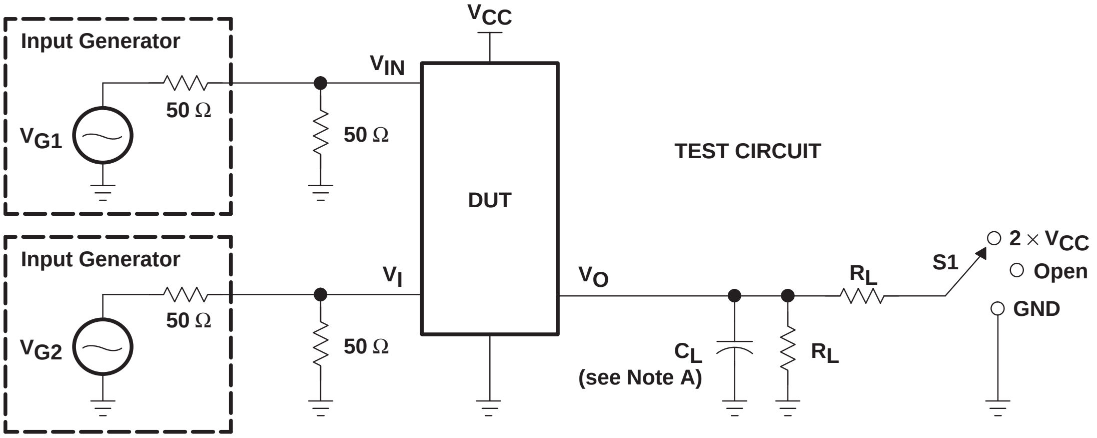
¶ Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

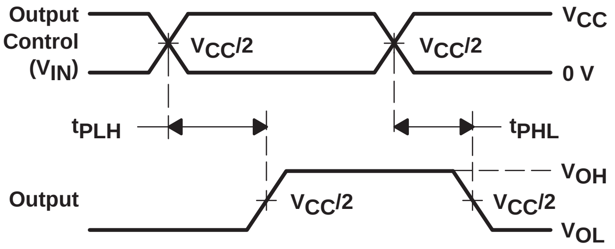
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}†	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	8.5	1	6.5	ns
t_{dis}	$\overline{OE}$	A or B	1	9	1	9	ns

† The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

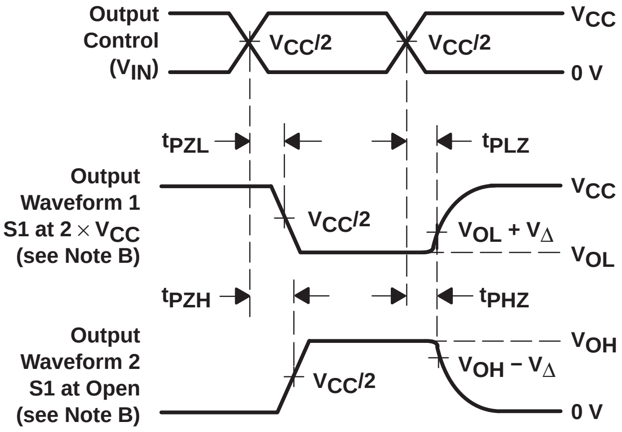
PARAMETER MEASUREMENT INFORMATION


Input Generator
VG1
50 Ω
Input Generator
VG2
50 Ω
VIN
50 Ω
VI
50 Ω
VCC
DUT
TEST CIRCUIT
VO
CL
(see Note A)
RL
RL
S1
2 × VCC
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V


Output
Control
(VIN)
VCC/2
VCC/2
VCC
0 V
tPLH
tPHL
Output
VCC/2
VCC/2
VOH
VOL

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)


Output
Control
(VIN)
VCC/2
VCC/2
VCC
0 V
tPZL
tPLZ
Output
Waveform 1
S1 at 2 × VCC
(see Note B)
VCC/2
VOL + VΔ
VCC
VOL
tPZH
tPHZ
Output
Waveform 2
S1 at Open
(see Note B)
VCC/2
VOH − VΔ
VOH
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

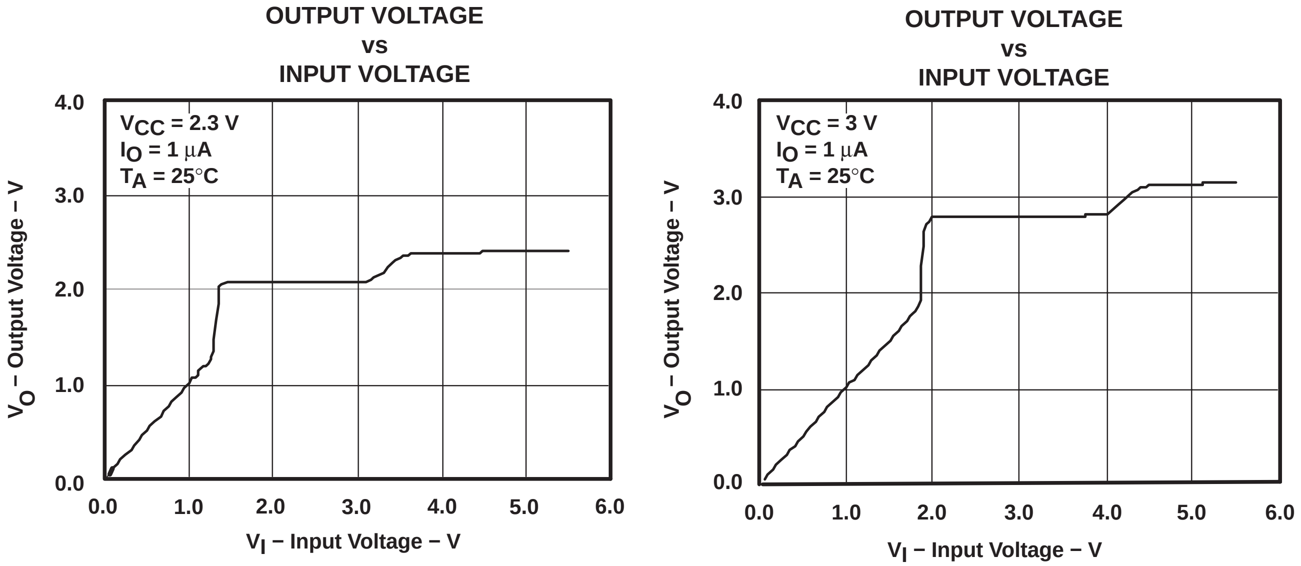


Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS (continued)

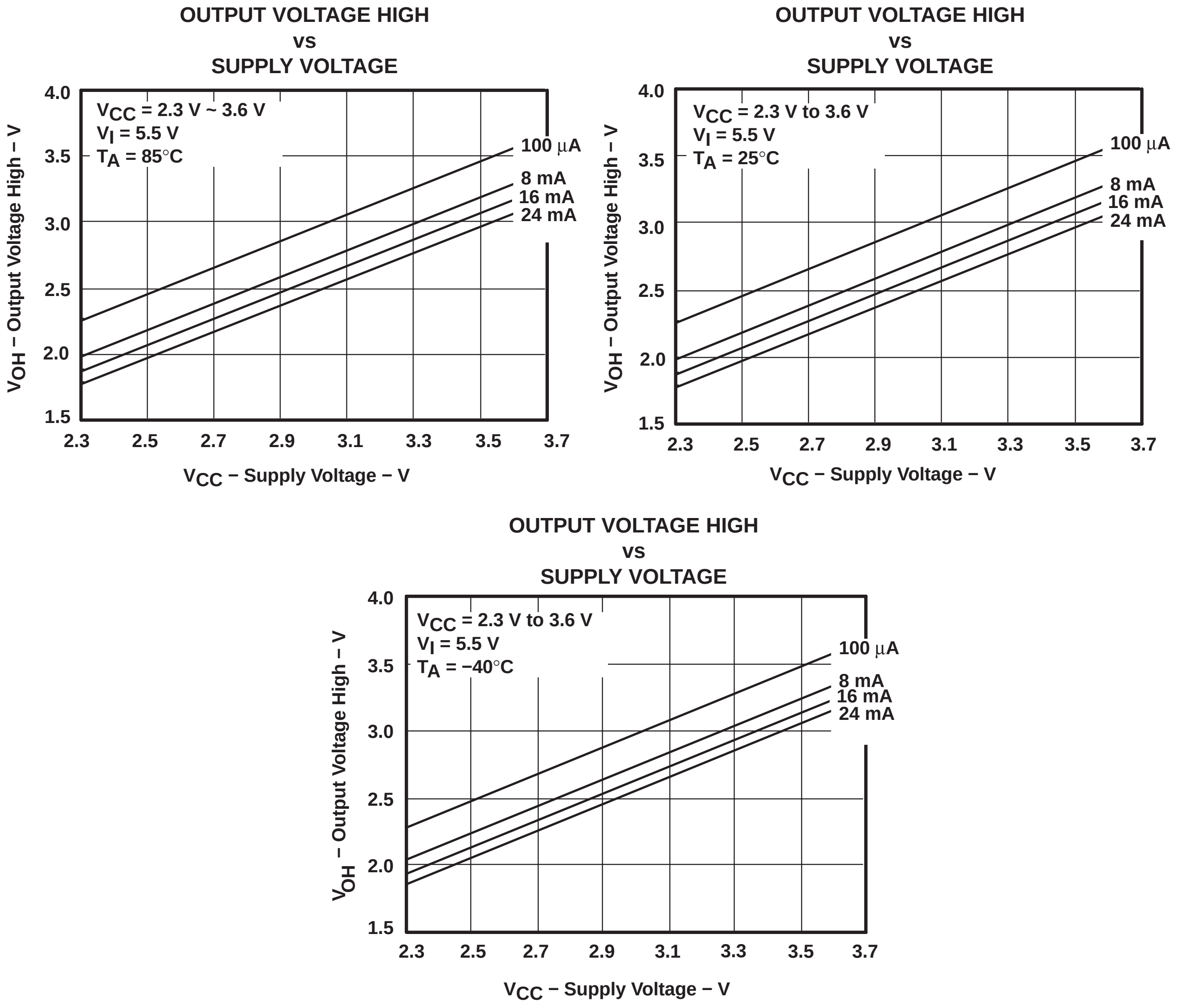


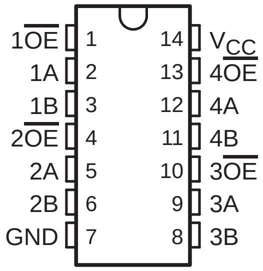
Figure 4. V$_{OH}$ Values

SN74CB3T3125
QUADRUPLE FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS120A − FEBRUARY 2003 − REVISED OCTOBER 2003

- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation On All Data I/O Ports**
  - **5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}**
- **5-V Tolerant I/Os With Device Powered-Up or Powered-Down**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 5 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 4.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 20 µA Max)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, USB Interface, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

DGV OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CB3T3125 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3125 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TSSOP − PW	Tube	SN74CB3T3125PW	KS125
		Tape and reel	SN74CB3T3125PWR	
	TVSOP − DGV	Tape and reel	SN74CB3T3125DGVR	KS125

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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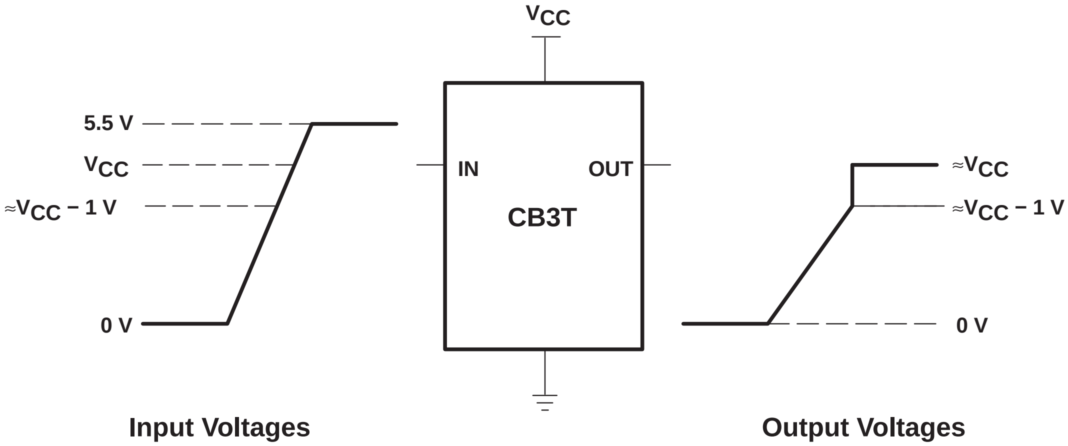
description/ordering information (continued)



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} − 1 V, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage-Translation Characteristics

The SN74CB3T3125 is organized as four 1-bit bus switches with separate output-enable (1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$) inputs. It can be used as four 1-bit bus switches or as one 4-bit bus switch. When $\overline{OE}$ is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 1-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

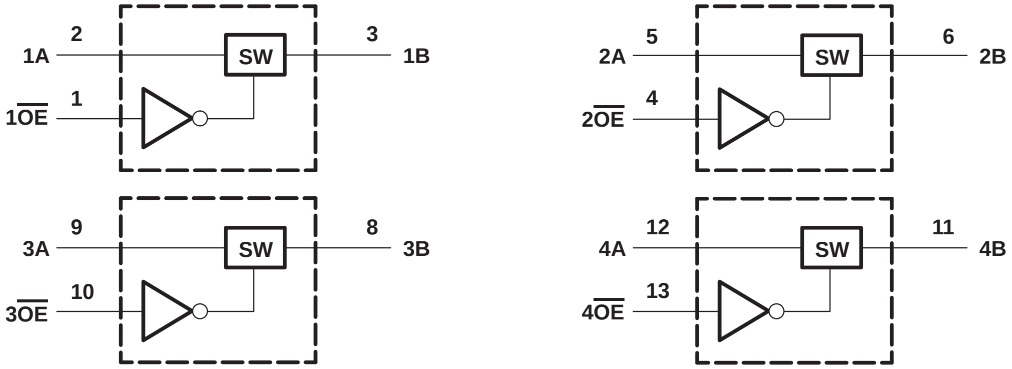
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

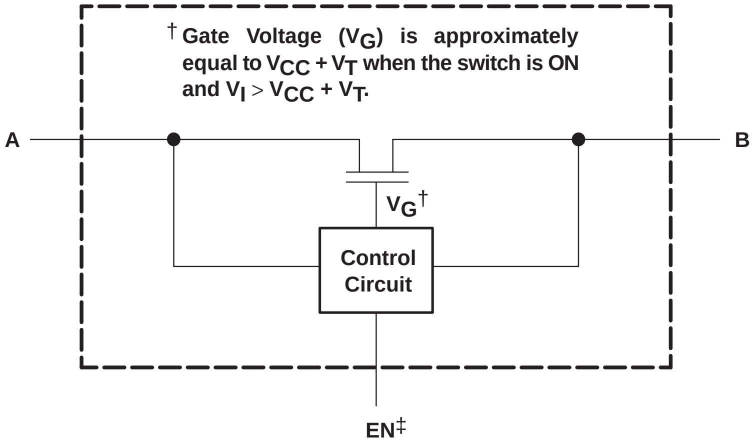
FUNCTION TABLE
(each bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)


† Gate Voltage (V_G) is approximately equal to V_{CC} + V_T when the switch is ON and V_I > V_{CC} + V_T.
A
B
V_G†
Control Circuit
EN‡

‡ EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} (see Note 1)	−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DGV package	127°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = −18 mA				−1.2	V
V_{OH}		See Figures 3 and 4					
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 3.6 V to 5.5 V or GND				±10	μA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} − 0.7 V to 5.5 V			±20	μA
			V_I = 0.7 V to V_{CC} − 0.7 V			−40	
			V_I = 0 to 0.7 V			±5	
I_{OZ}[‡]		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND				±10	μA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0,				10	μA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND			20	μA
			V_I = 5.5 V			20	
ΔI_{CC}[§]	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				300	μA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND			3		pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND			4.5		pF
$C_{io(ON)}$		V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V		4		pF
			$V_{I/O}$ = GND		10		
r_{on}[¶]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA		5	8	Ω
			I_O = 16 mA		5	8	
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA		5	7	
			I_O = 32 mA		5	7	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

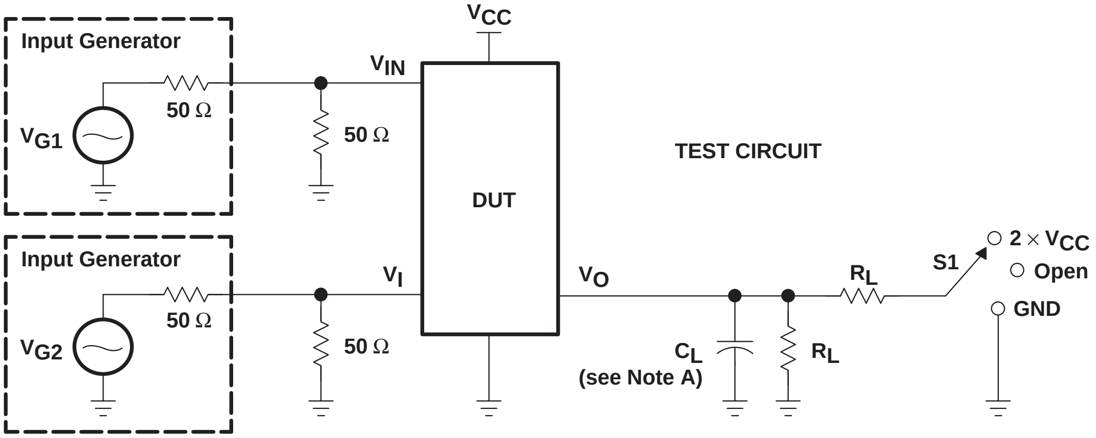
[¶] Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

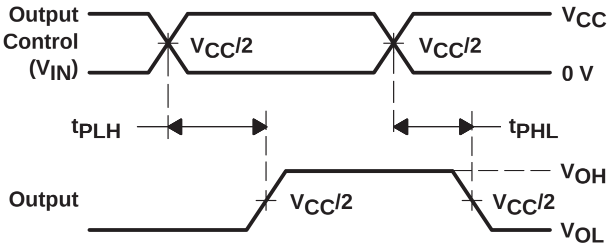
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	8.5	1	4.4	ns
t_{dis}	$\overline{OE}$	A or B	1	9	1	9	ns

[†] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

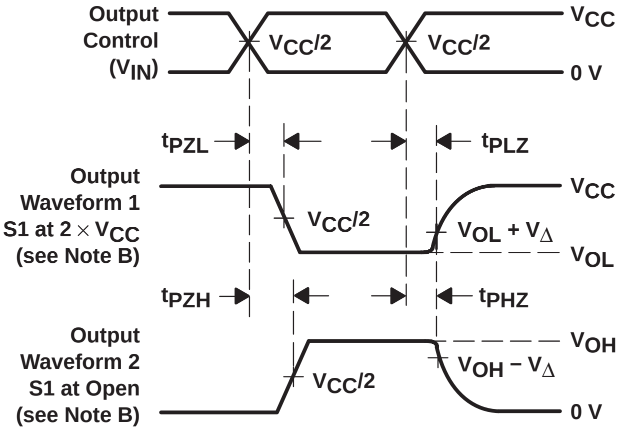
PARAMETER MEASUREMENT INFORMATION


V_{CC}
Input Generator
V_{G1}
50 Ω
50 Ω
V_{IN}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
50 Ω
V_I
V_O
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
V_{CC}
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
$V_{CC}/2$
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

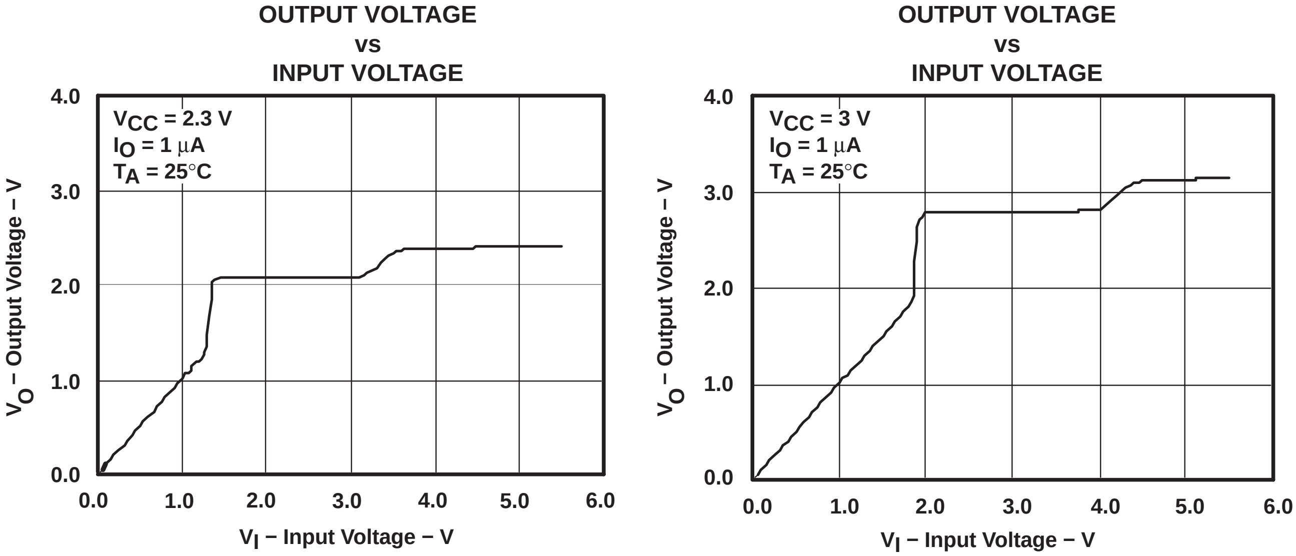


Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS (continued)

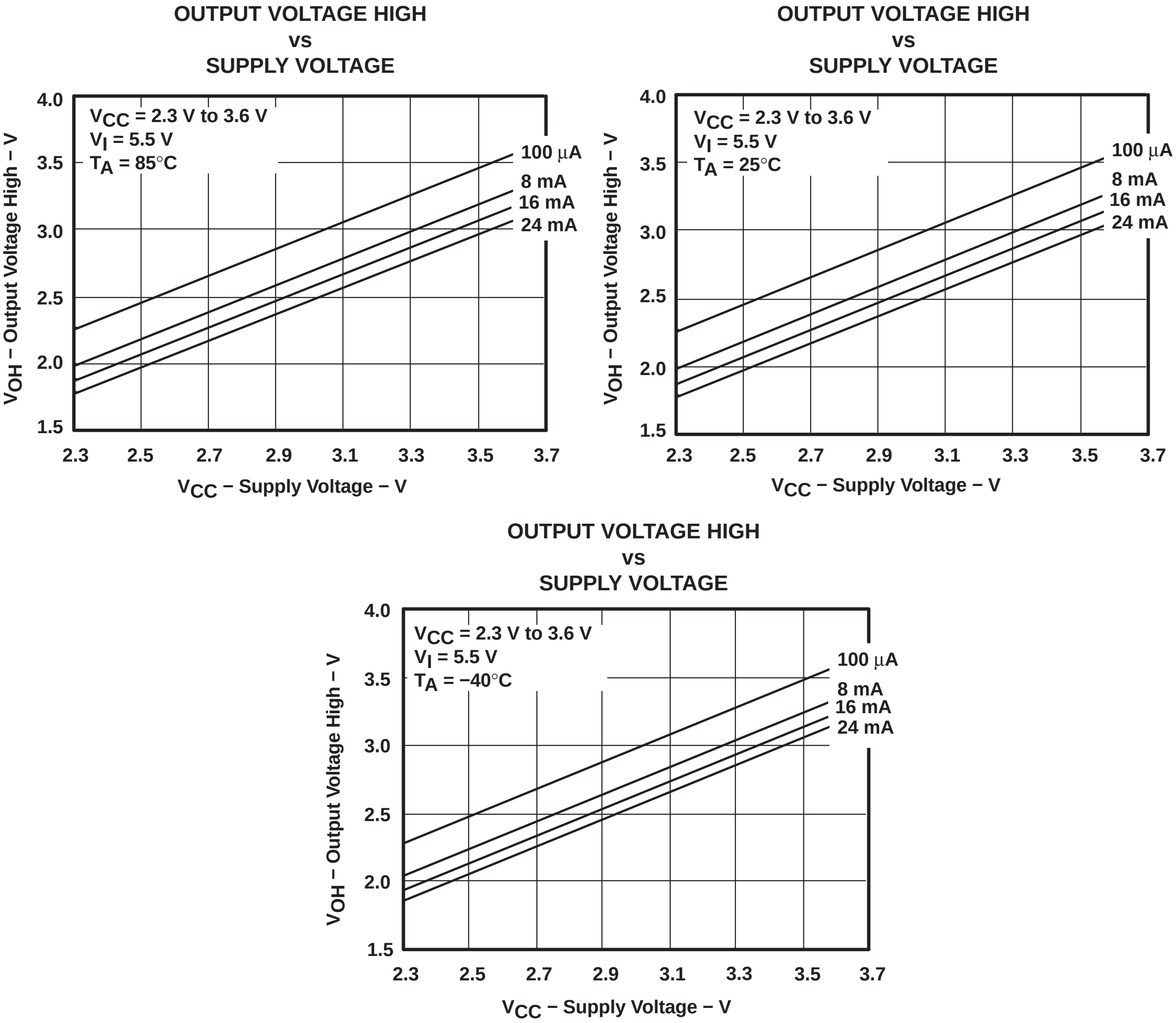


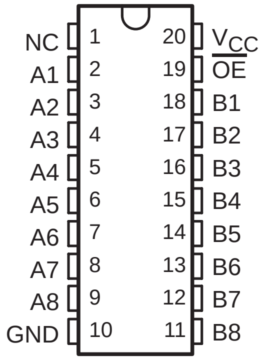
Figure 4. V_{OH} Values

SN74CB3T3245
8-BIT FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER

SCDS136 − OCTOBER 2003

- **Standard ’245-Type Pinout**
- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation On All Data I/O Ports**
  - **5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}**
- **5-V-Tolerant I/Os With Device Powered-Up or Powered-Down**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 5 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 40 μA Max)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, PCI Interface, USB Interface, Memory Interleaving, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The SN74CB3T3245 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3245 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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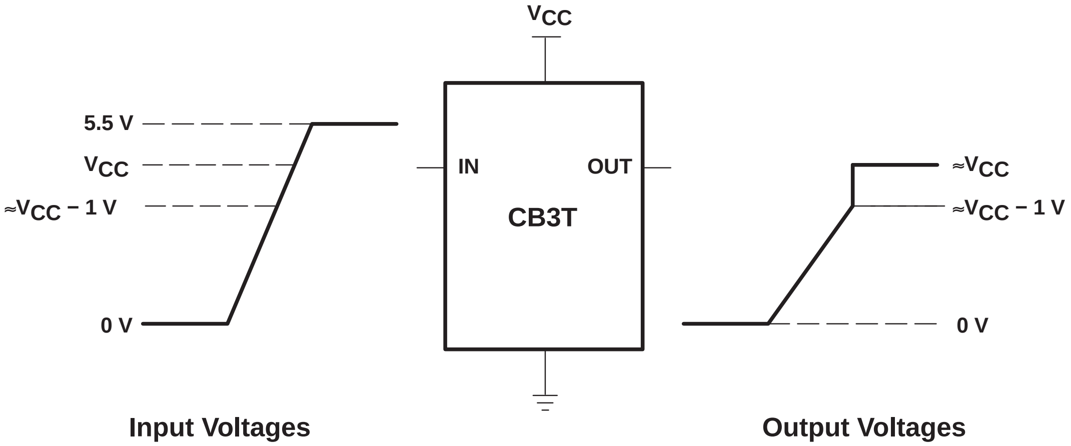
description/ordering information (continued)



NOTE A: If the input high-voltage (V_{IH}) level is greater than or equal to V_{CC} − 1 V, and less than or equal to 5.5 V, then the output high-voltage(V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage Translation Characteristics

The SN74CB3T3245 is an 8-bit bus switch with a single ouput-enable ($\overline{OE}$) input and a standard ’245 pinout. When $\overline{OE}$ is low, the 8-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the 8-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

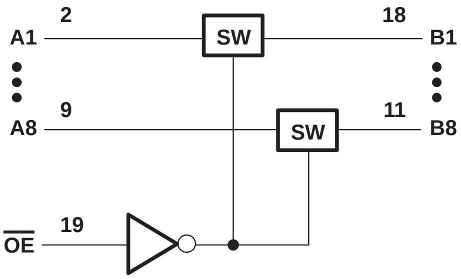
T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CB3T3245DW	CB3T3245
		Tape and reel	SN74CB3T3245DWR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CB3T3245DBQR	CB3T3245
	TSSOP − PW	Tube	SN74CB3T3245PW	KS245
		Tape and reel	SN74CB3T3245PWR	
	TVSOP − DGV	Tape and reel	SN74CB3T3245DGVR	KS245

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

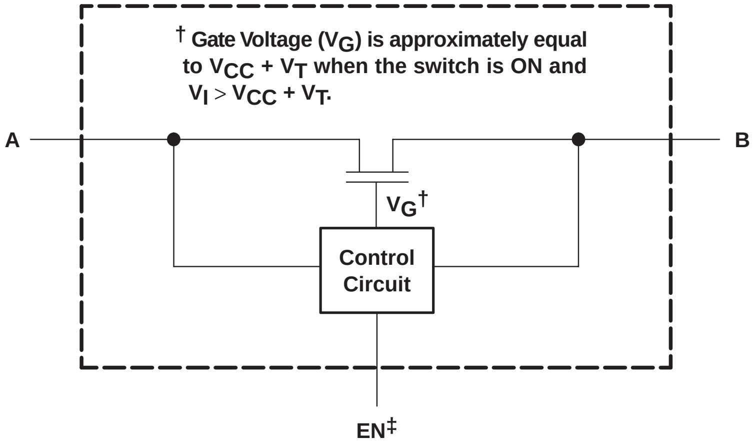
FUNCTION TABLE

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)


† Gate Voltage (VG) is approximately equal to VCC + VT when the switch is ON and VI > VCC + VT.
A
B
VG†
Control Circuit
EN‡

‡ EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} (see Note 1)		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DBQ package	68°C/W
	DGV package	92°C/W
	DW package	58°C/W
	PW package	83°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = −18 mA				−1.2	V
V_{OH}		See Figures 3 and 4					
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 3.6 V to 5.5 V or GND				±10	μA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} − 0.7 V to 5.5 V			±20	μA
			V_I = 0.7 V to V_{CC} − 0.7 V			−40	
			V_I = 0 to 0.7 V			±5	
I_{OZ}‡		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND				±10	μA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0,				10	μA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND			40	μA
			V_I = 5.5 V			40	
ΔI_{CC}§	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				300	μA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND			4		pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND			5		pF
$C_{io(ON)}$		V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V		5		pF
			$V_{I/O}$ = GND		13		
r_{on}¶		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA		5	8.5	Ω
			I_O = 16 mA		5	8.5	
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA		5	7	
			I_O = 32 mA		5	7	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

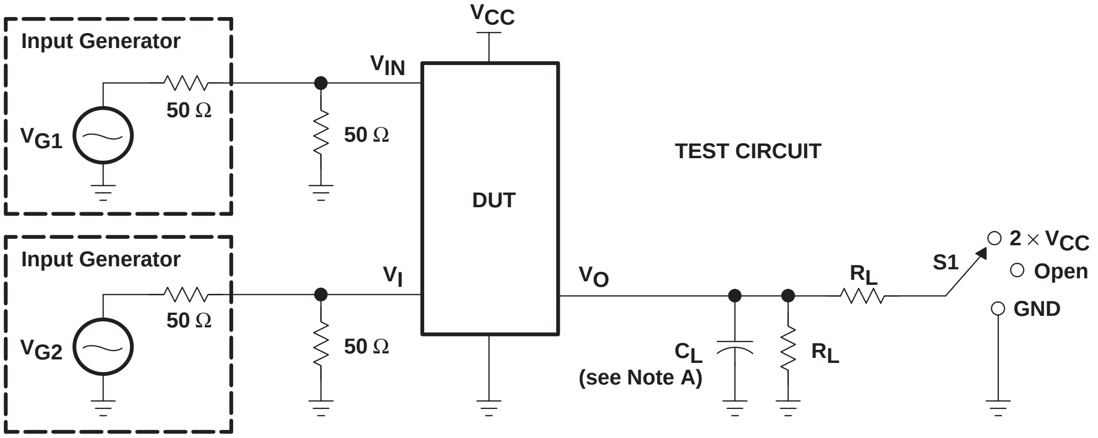
¶ Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

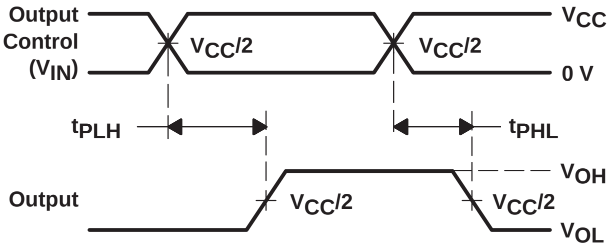
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	10.5	1	8	ns
t_{dis}	$\overline{OE}$	A or B	1	5.5	1	7.5	ns

[†] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

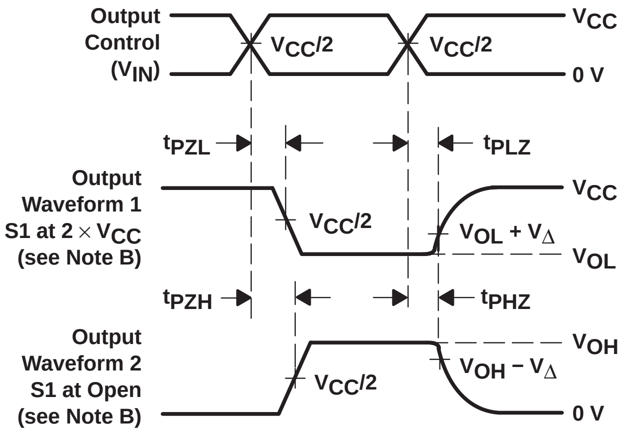
PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
50 Ω
V_{IN}
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
50 Ω
V_I
V_O
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
V_{CC}/2
V_{CC}/2
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
V_{CC}/2
V_{CC}/2
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

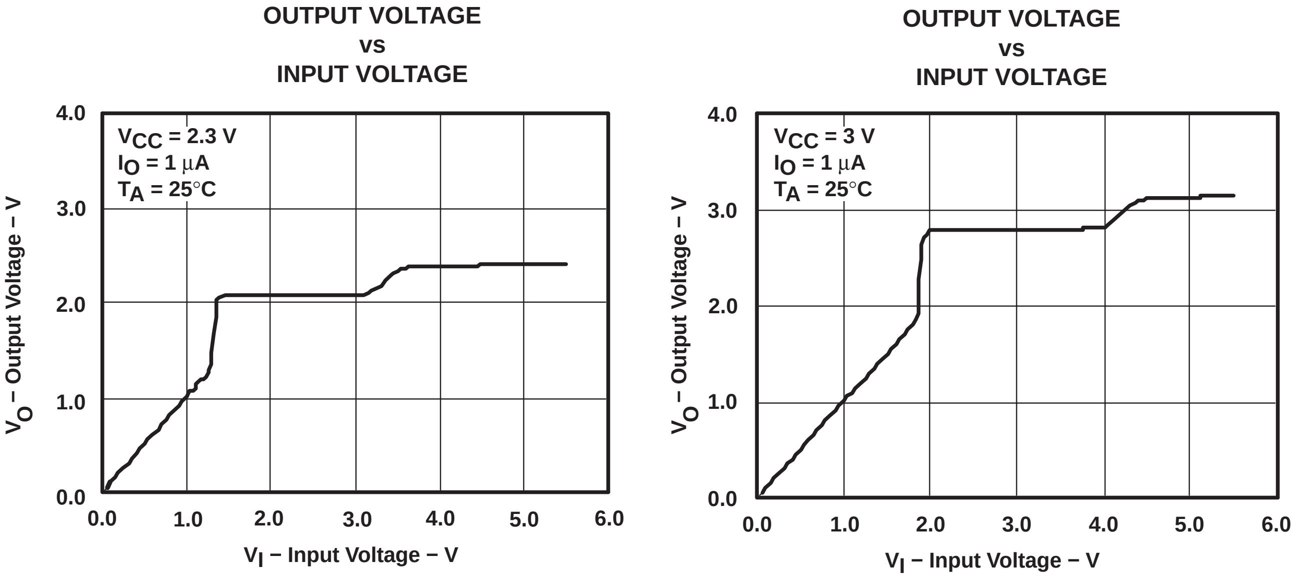

Output Control (V_{IN})
V_{CC}/2
V_{CC}/2
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
V_{CC}/2
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
V_{CC}/2
$V_{OH} - V_\Delta$
V_{OH}
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

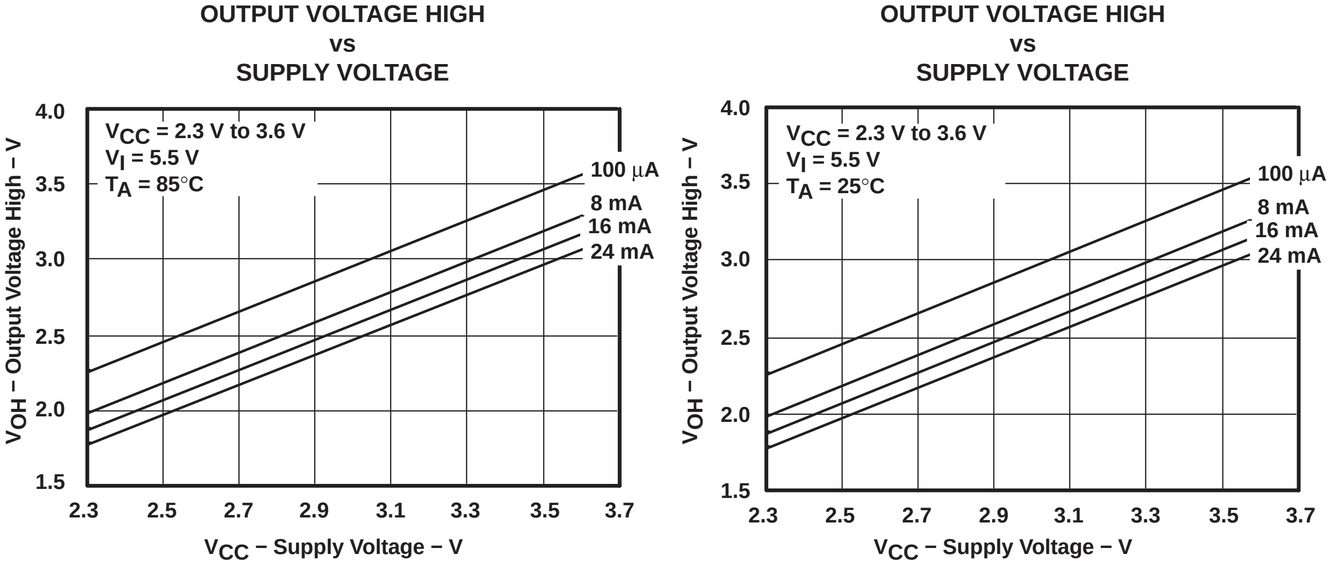


OUTPUT VOLTAGE vs INPUT VOLTAGE

OUTPUT VOLTAGE vs INPUT VOLTAGE

Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS (continued)



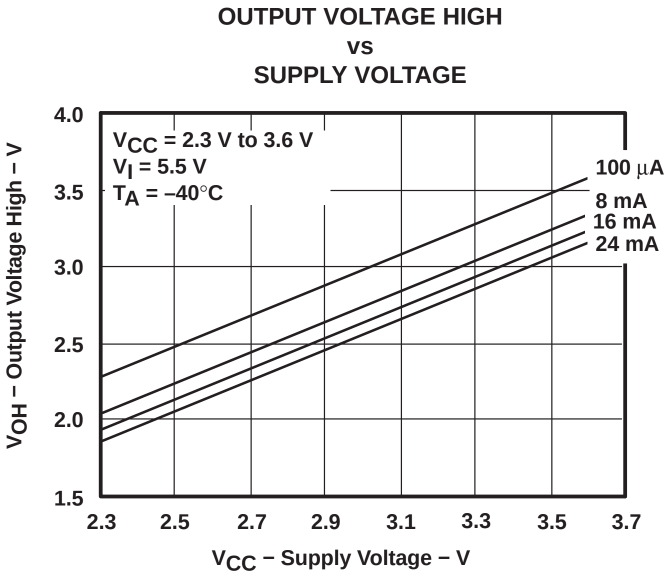


Figure 4. V_{OH} Values

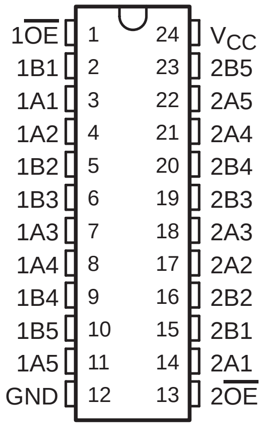
SN74CB3T3384
10-BIT FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER

SCDS159 − OCTOBER 2003

- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation On All Data I/O Ports**
  - **5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}**
- **5-V-Tolerant I/Os With Device Powered-Up or Powered-Down**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics**
- **Low Input/Output Capacitance Minimizes Loading**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, PCI Interface, Memory Interleaving, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

PRODUCT PREVIEW

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CB3T3384DW	
		Tape and reel	SN74CB3T3384DWR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CB3T3384DBQR	
	TSSOP − PW	Tape and reel	SN74CB3T3384PWR	
	TVSOP − DGV	Tape and reel	SN74CB3T3384DGVR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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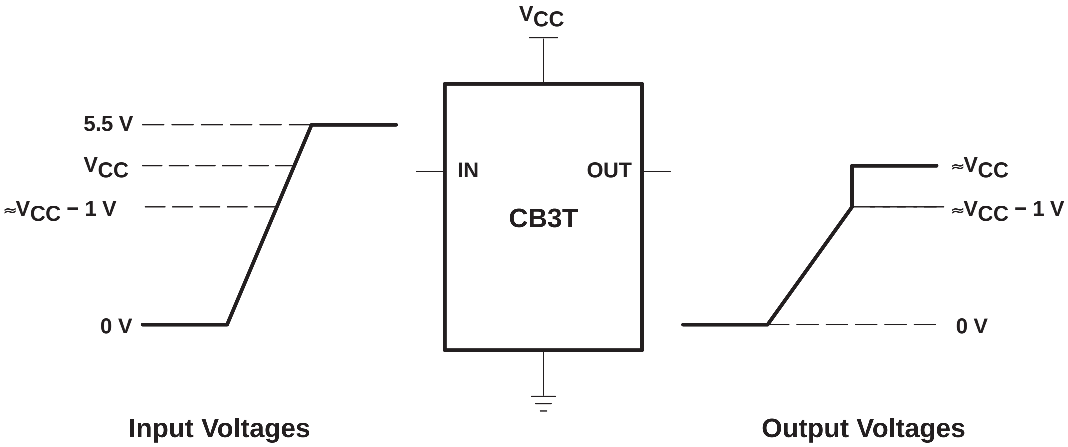
description/ordering information (continued)

The SN74CB3T3384 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3384 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} − 1 V, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage Translation Characteristics

The SN74CB3T3384 is organized as two 5-bit bus switches with separate ouput-enable (1$\overline{OE}$, 2$\overline{OE}$) inputs. It can be used as two 5-bit bus switches or as one 10-bit bus switch. When $\overline{OE}$ is low, the associated 5-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 5-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

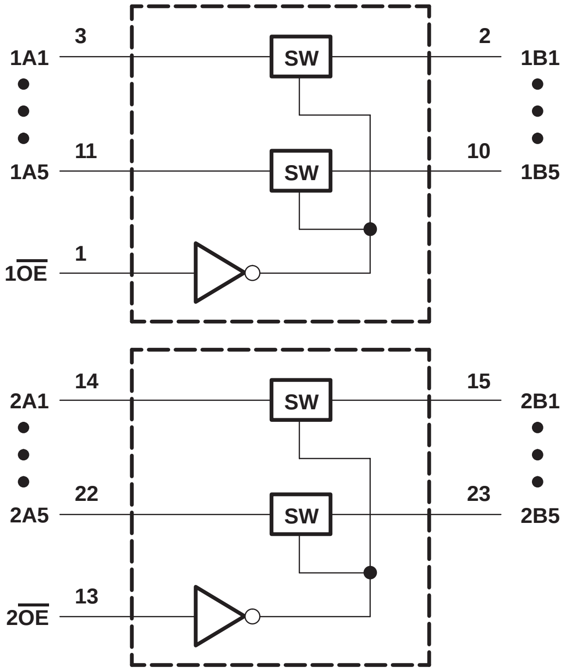
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each 5-bit bus switch)

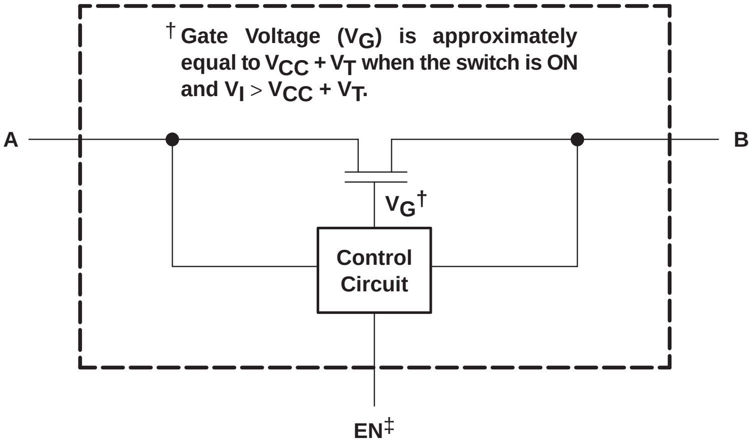
INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

PRODUCT PREVIEW

logic diagram (positive logic)


3
1A1
2
1B1
SW
11
1A5
10
1B5
SW
1
1OE
14
2A1
15
2B1
SW
22
2A5
23
2B5
SW
13
2OE

simplified schematic, each FET switch (SW)


† Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
A
B
V_G†
Control Circuit
EN‡

‡ EN is the internal enable signal applied to the switch.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . −0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . −0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$) . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$) . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . ±128 mA
Continuous current through V_{CC} or GND terminals . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DBQ package . . . . 61°C/W
DGV package . . . . 86°C/W
DW package . . . . 46°C/W
PW package . . . . 88°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = −18 mA					V
V_{OH}		See Figures 3 and 4					
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 3.6 V to 5.5 V or GND					µA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} − 0.7 V to 5.5 V				µA
			V_I = 0.7 V to V_{CC} − 0.7 V				
			V_I = 0 to 0.7 V				
I_{OZ}[‡]		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND					µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0,					µA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND				µA
			V_I = 5.5 V				
ΔI_{CC}[§]	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND					µA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND					pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND					pF
$C_{io(ON)}$		V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V				pF
			$V_{I/O}$ = GND				
r_{on}[¶]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA				Ω
			I_O = 16 mA				
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA				
			I_O = 32 mA				

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

PRODUCT PREVIEW

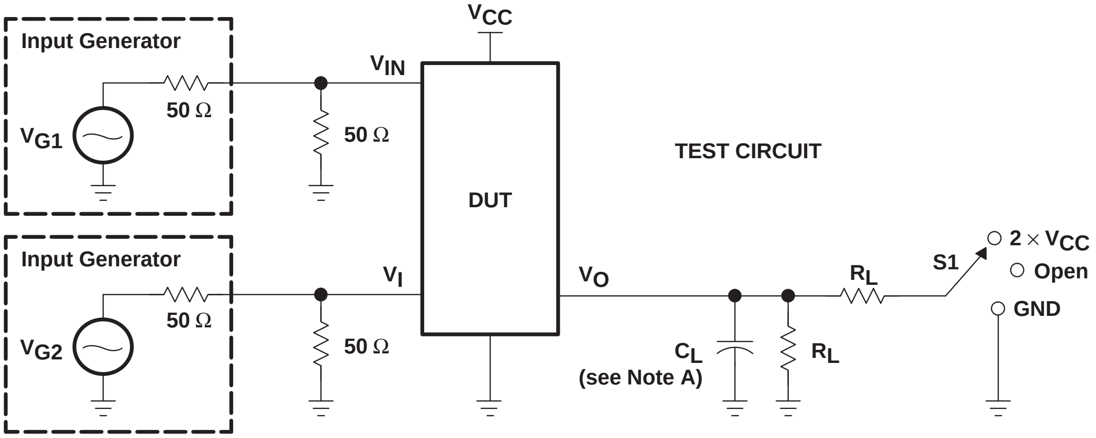
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A					ns
t_{en}	$\overline{OE}$	A or B					ns
t_{dis}	$\overline{OE}$	A or B					ns

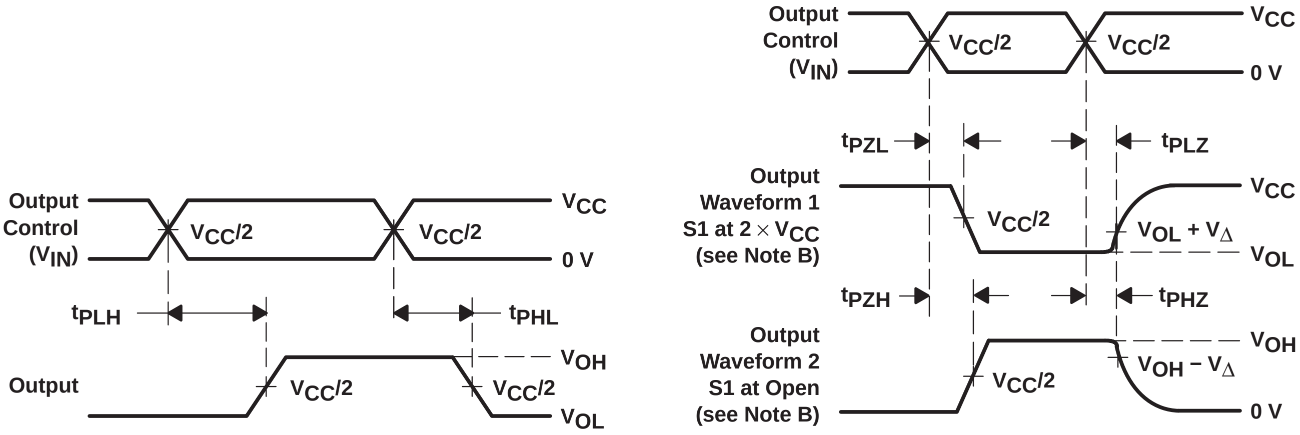
[†] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
50 Ω
V_{IN}
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
50 Ω
V_I
V_O
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
V_{CC}
V_{OL} + V_Δ
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
$V_{CC}/2$
V_{OH}
V_{OH} − V_Δ
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

PRODUCT PREVIEW

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

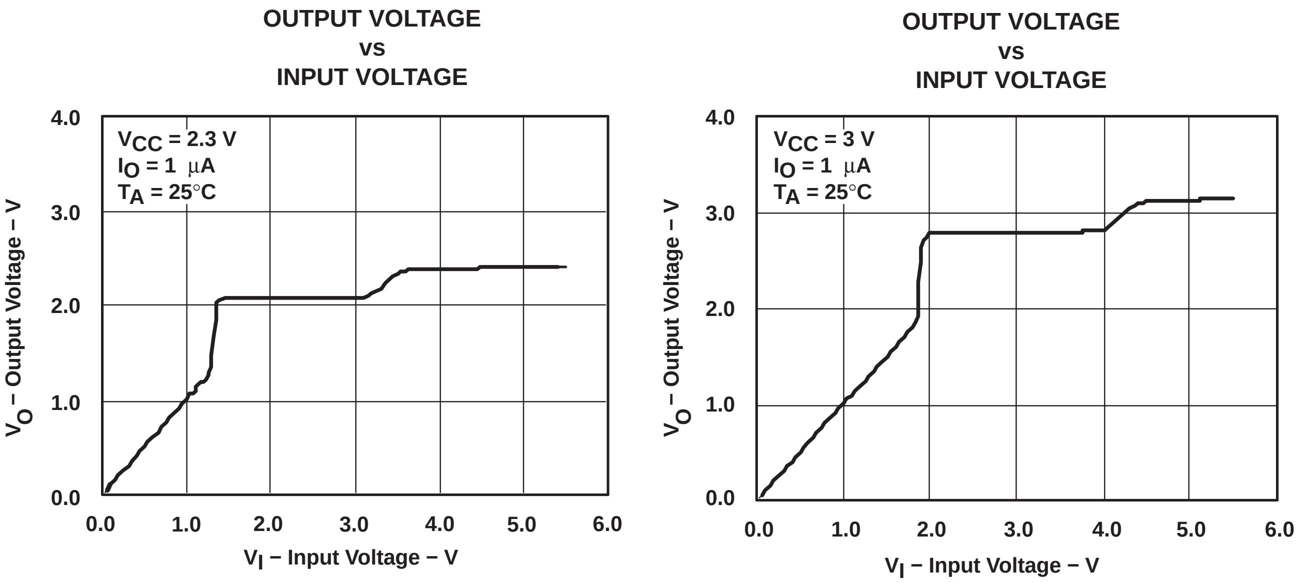


Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS (continued)

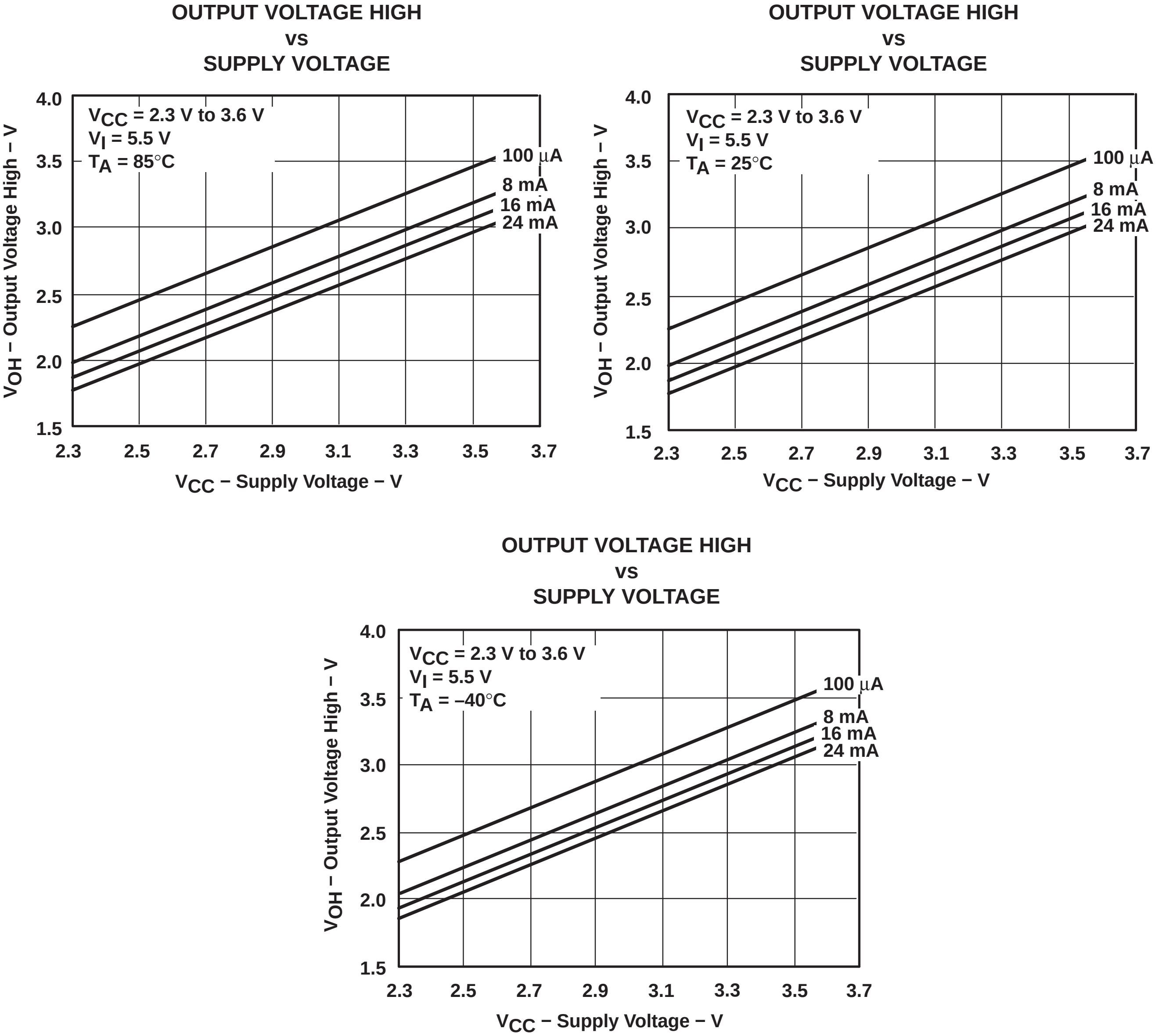


Figure 4. V_{OH} Values

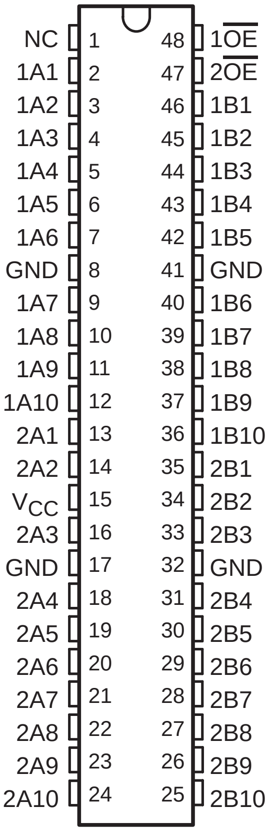
PRODUCT PREVIEW

SN74CB3T16210
20-BIT FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER

SCDS156 − OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation On All Data I/O Ports**
  - **5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}**
- **5-V-Tolerant I/Os With Device Powered-Up or Powered-Down**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics**
- **Low Input/Output Capacitance Minimizes Loading**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, PCI Interface, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1 48 $1\overline{OE}$
1A1 2 47 $2\overline{OE}$
1A2 3 46 1B1
1A3 4 45 1B2
1A4 5 44 1B3
1A5 6 43 1B4
1A6 7 42 1B5
GND 8 41 GND
1A7 9 40 1B6
1A8 10 39 1B7
1A9 11 38 1B8
1A10 12 37 1B9
2A1 13 36 1B10
2A2 14 35 2B1
V_{CC} 15 34 2B2
2A3 16 33 2B3
GND 17 32 GND
2A4 18 31 2B4
2A5 19 30 2B5
2A6 20 29 2B6
2A7 21 28 2B7
2A8 22 27 2B8
2A9 23 26 2B9
2A10 24 25 2B10

NC − No internal connection

PRODUCT PREVIEW

description/ordering information

The SN74CB3T16210 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T16210 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

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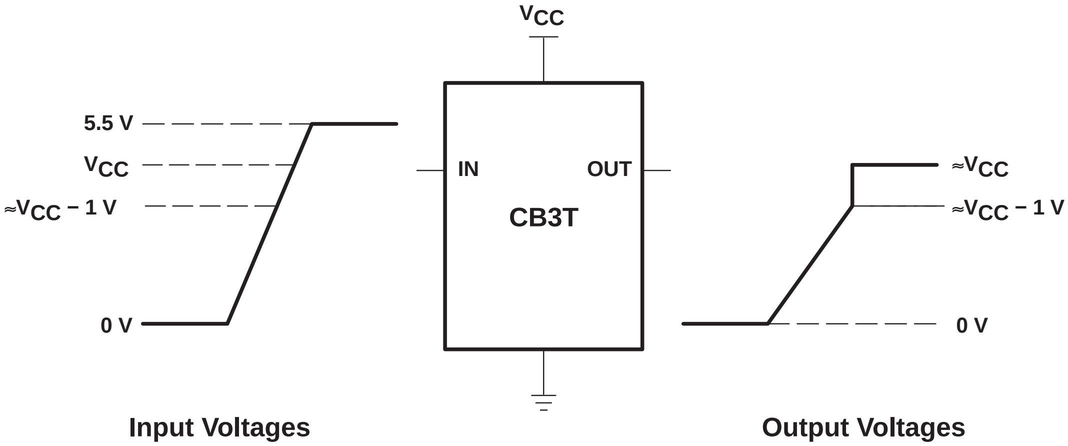
description/ordering information (continued)



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} − 1 V, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage Translation Characteristics

The SN74CB3T16210 is organized as two 10-bit bus switches with separate ouput-enable (1$\overline{OE}$, 2$\overline{OE}$) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When $\overline{OE}$ is low, the associated 10-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 10-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CB3T16210DL	
		Tape and reel	SN74CB3T16210DLR	
	TSSOP − DGG	Tube	SN74CB3T16210DGG	
		Tape and reel	SN74CB3T16210DGGR	
	TVSOP − DGV	Tape and reel	SN74CB3T16210DGVR	

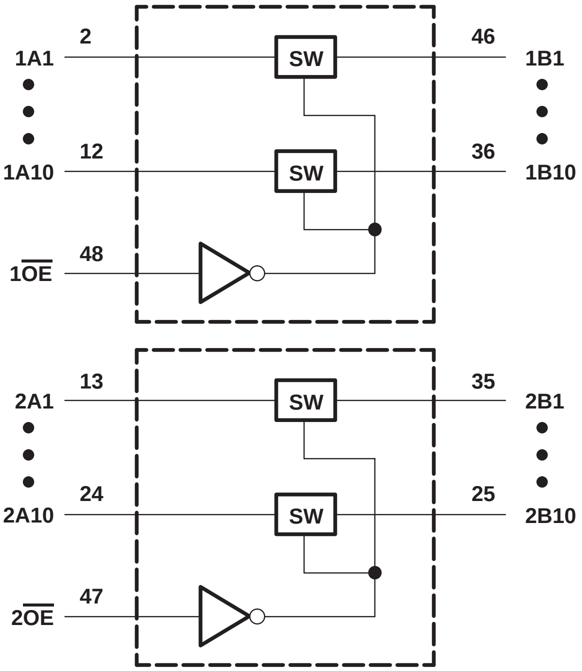
[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 10-bit bus switch)

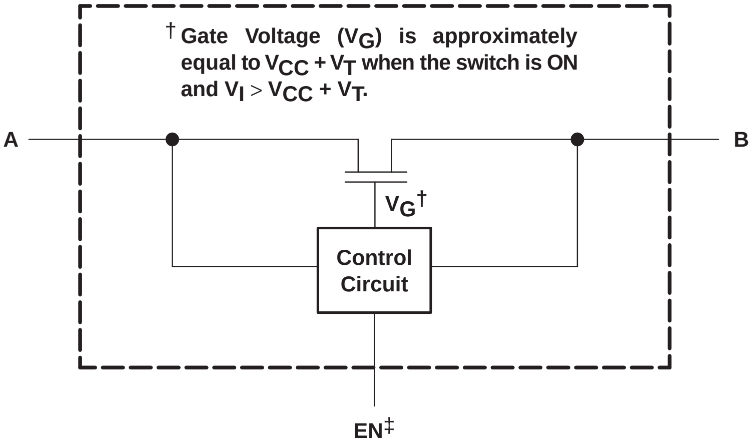
INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

PRODUCT PREVIEW

logic diagram (positive logic)


1A1
2
46
1B1
SW
1A10
12
36
1B10
SW
1$\overline{OE}$
48
2A1
13
35
2B1
SW
2A10
24
25
2B10
SW
2$\overline{OE}$
47

simplified schematic, each FET switch (SW)


A
B
V_G†
Control Circuit
EN‡

† Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.

‡ EN is the internal enable signal applied to the switch.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = −18 mA					V
V_{OH}		See Figures 3 and 4					
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 3.6 V to 5.5 V or GND					µA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} − 0.7 V to 5.5 V				µA
			V_I = 0.7 V to V_{CC} − 0.7 V				
			V_I = 0 to 0.7 V				
I_{OZ}‡		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND					µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0,					µA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND				µA
			V_I = 5.5 V				
ΔI_{CC}§	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND					µA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND					pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND					pF
$C_{io(ON)}$		V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V				pF
			$V_{I/O}$ = GND				
r_{on}¶		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA				Ω
			I_O = 16 mA				
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA				
			I_O = 32 mA				

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

PRODUCT PREVIEW

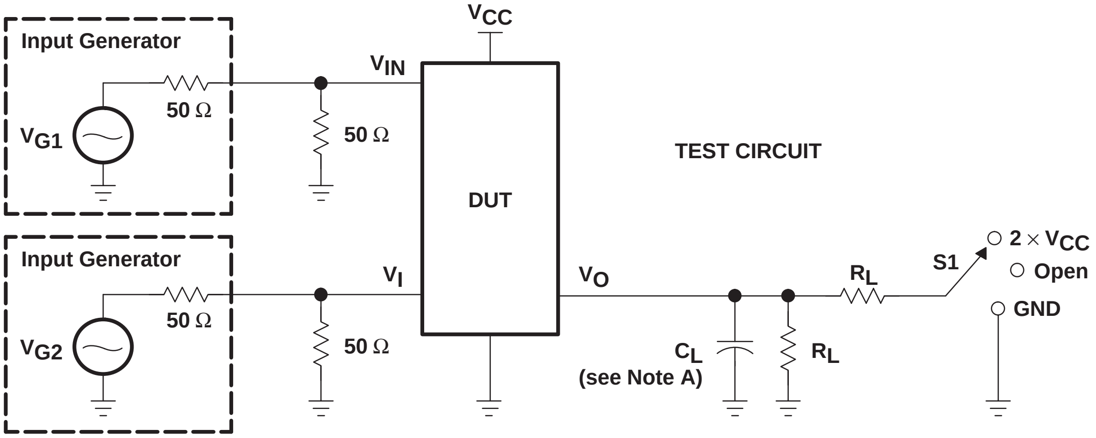
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A					ns
t_{en}	$\overline{OE}$	A or B					ns
t_{dis}	$\overline{OE}$	A or B					ns

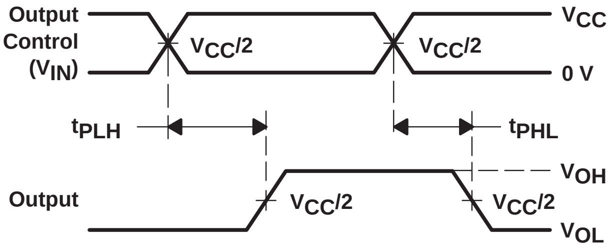
[†] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PRODUCT PREVIEW

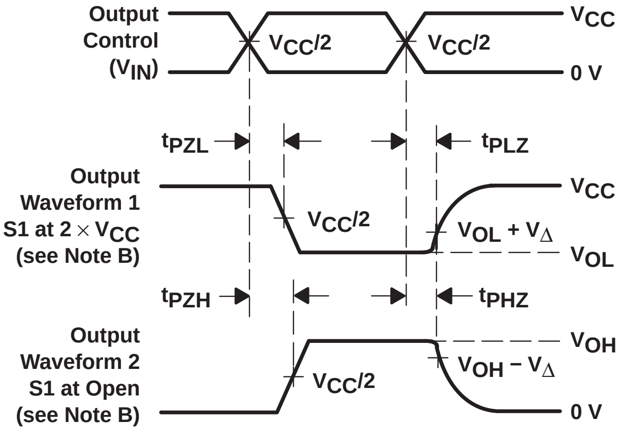
PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V


Output
Control
(V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)


Output
Control
(V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 2 × V_{CC}
(see Note B)
$V_{CC}/2$
V_{CC}
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
$V_{CC}/2$
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

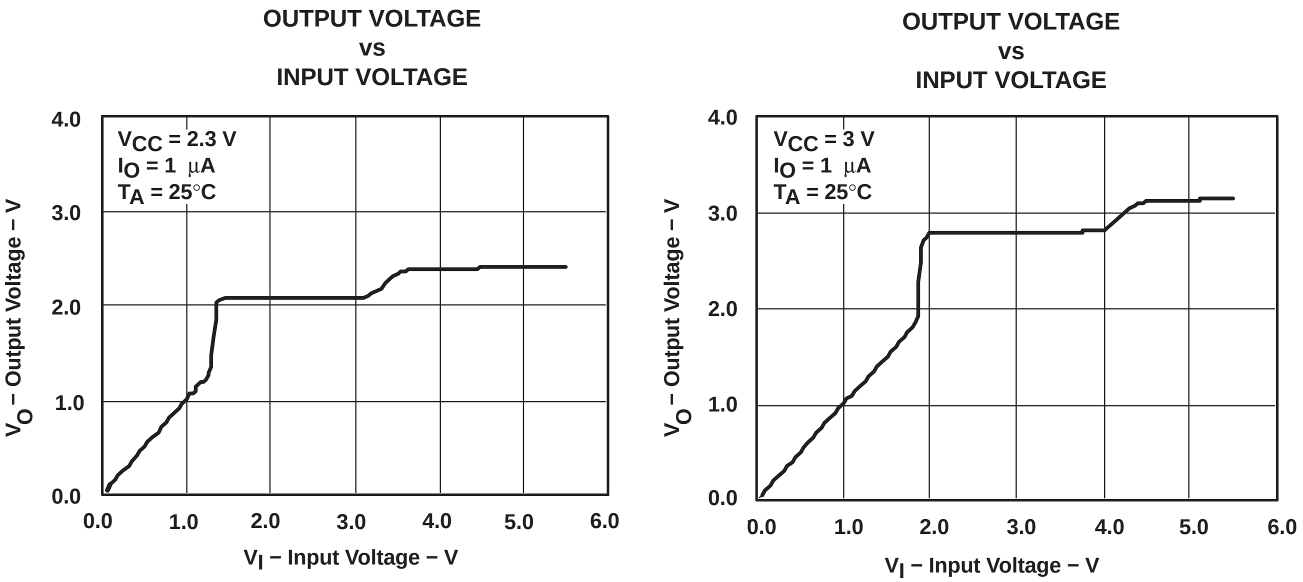
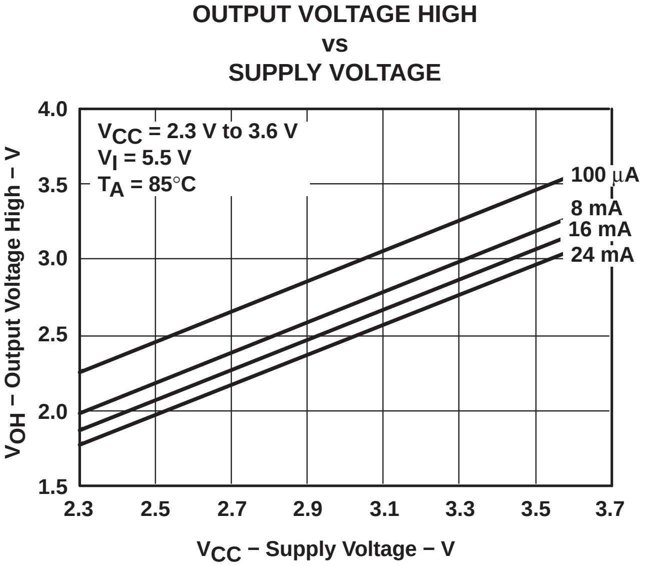
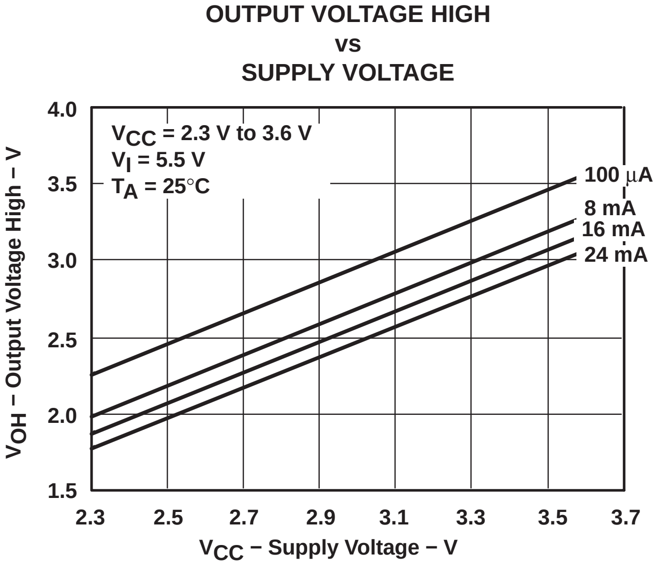


Figure 3. Data Output Voltage vs Data Input Voltage

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)





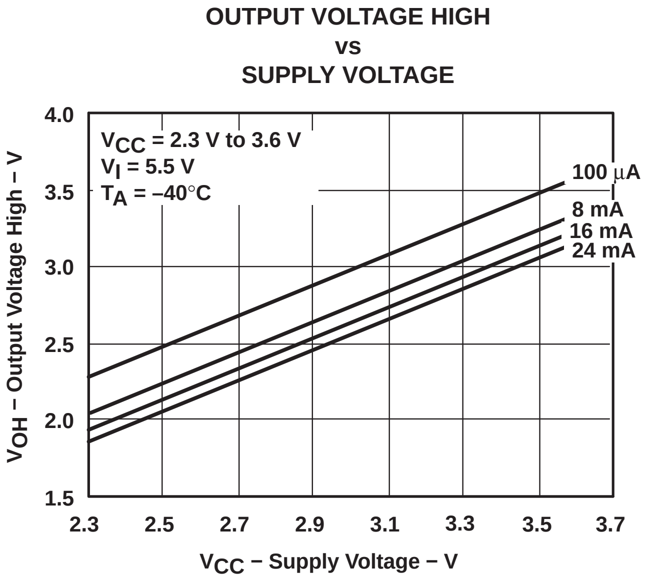


Figure 4. V_{OH} Values

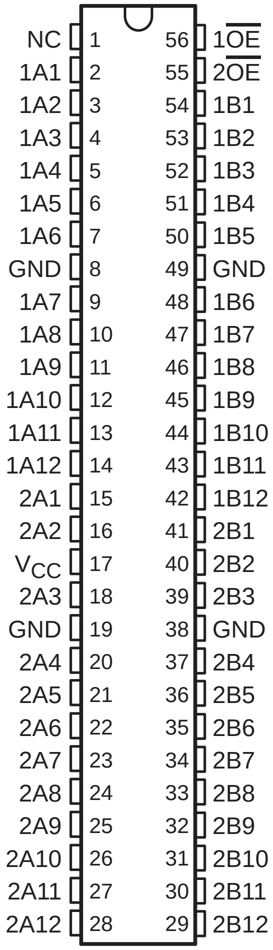
PRODUCT PREVIEW

SN74CB3T16211
24-BIT FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS147 − OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation On All Data I/O Ports**
  - **5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}**
- **5-V Tolerant I/Os With Device Powered-Up or Powered-Down**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 5 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 70 μA Max)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, PCI Interface, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1
1A1 2
1A2 3
1A3 4
1A4 5
1A5 6
1A6 7
GND 8
1A7 9
1A8 10
1A9 11
1A10 12
1A11 13
1A12 14
2A1 15
2A2 16
V_{CC} 17
2A3 18
GND 19
2A4 20
2A5 21
2A6 22
2A7 23
2A8 24
2A9 25
2A10 26
2A11 27
2A12 28
56 $1\overline{OE}$
55 $2\overline{OE}$
54 1B1
53 1B2
52 1B3
51 1B4
50 1B5
49 GND
48 1B6
47 1B7
46 1B8
45 1B9
44 1B10
43 1B11
42 1B12
41 2B1
40 2B2
39 2B3
38 GND
37 2B4
36 2B5
35 2B6
34 2B7
33 2B8
32 2B9
31 2B10
30 2B11
29 2B12

NC − No internal connection

description/ordering information

The SN74CB3T16211 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T16211 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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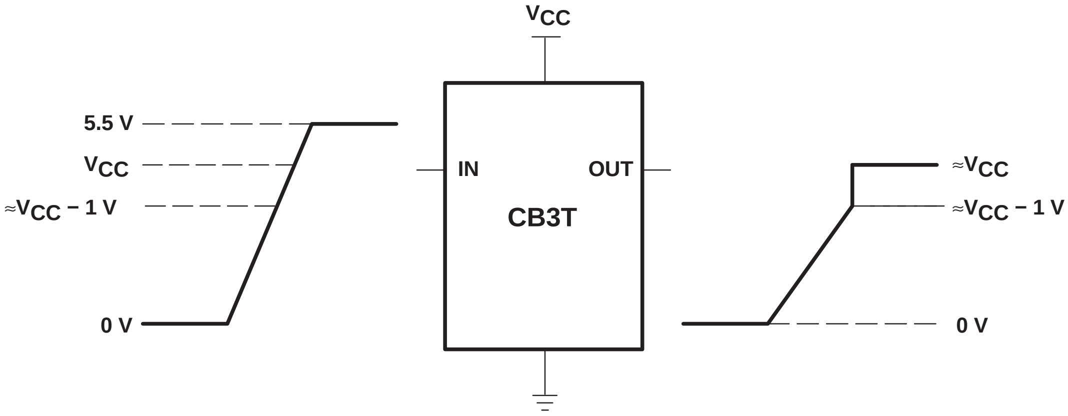
description/ordering information (continued)



Input Voltages **Output Voltages**

NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} − 1 V, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage-Translation Characteristics

The SN74CB3T16211 is organized as two 12-bit bus switches with separate ouput-enable (1$\overline{\text{OE}}$, 2$\overline{\text{OE}}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When $\overline{\text{OE}}$ is low, the associated 12-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{\text{OE}}$ is high, the associated 12-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

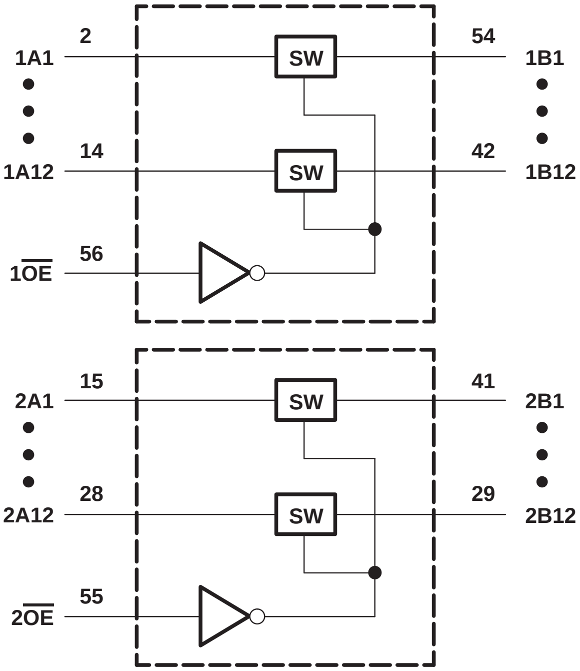
T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CB3T16211DL	CB3T16211
		Tape and reel	SN74CB3T16211DLR	
	TSSOP − DGG	Tube	SN74CB3T16211DGG	CB3T16211
		Tape and reel	SN74CB3T16211DGGR	
	TVSOP − DGV	Tape and reel	SN74CB3T16211DGVR	KR211

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

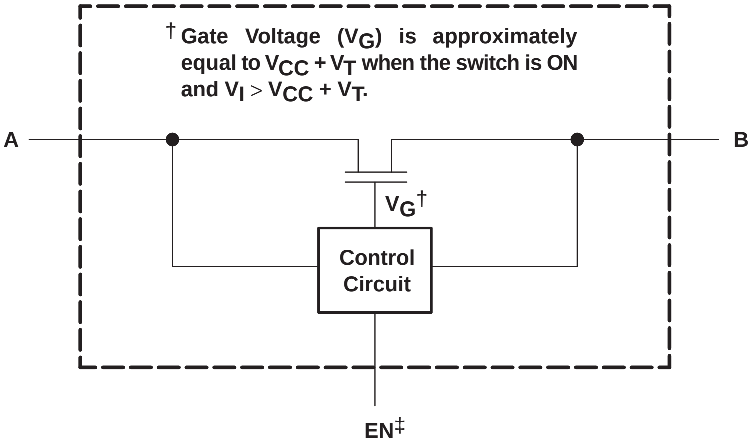
FUNCTION TABLE
(each 12-bit bus switch)

INPUT $\overline{\text{OE}}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)


1A1
2
SW
54
1B1
1A12
14
SW
42
1B12
1OE
56
2A1
15
SW
41
2B1
2A12
28
SW
29
2B12
2OE
55

simplified schematic, each FET switch (SW)


A
B
VG†
Control Circuit
EN‡

† Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.

‡ EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = −18 mA				−1.2	V
V_{OH}		See Figures 3 and 4					
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 3.6 V to 5.5 V or GND				±10	µA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} − 0.7 V to 5.5 V			±20	µA
			V_I = 0.7 V to V_{CC} − 0.7 V			−40	
			V_I = 0 to 0.7 V			±5	
I_{OZ}‡		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND				±10	µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0,				10	µA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND			70	µA
			V_I = 5.5 V			70	
ΔI_{CC}§	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				300	µA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND			4		pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND			5		pF
$C_{io(ON)}$		V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V		5		pF
			$V_{I/O}$ = GND		13		
r_{on}¶		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA		5	9.5	Ω
			I_O = 16 mA		5	9.5	
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA		5	8.5	
			I_O = 32 mA		5	8.5	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

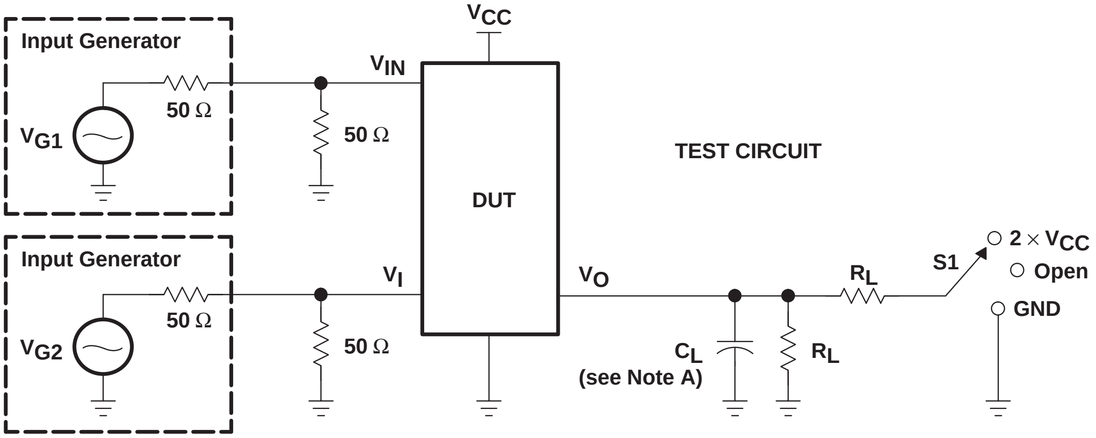
¶ Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

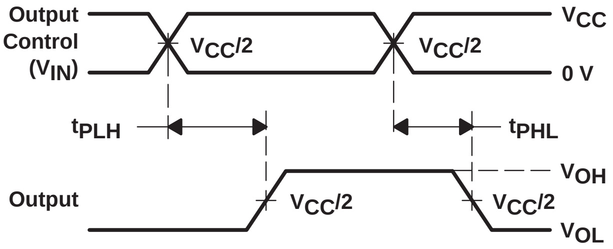
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	12	1	10	ns
t_{dis}	$\overline{OE}$	A or B	1	7.5	1	8.5	ns

[†] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

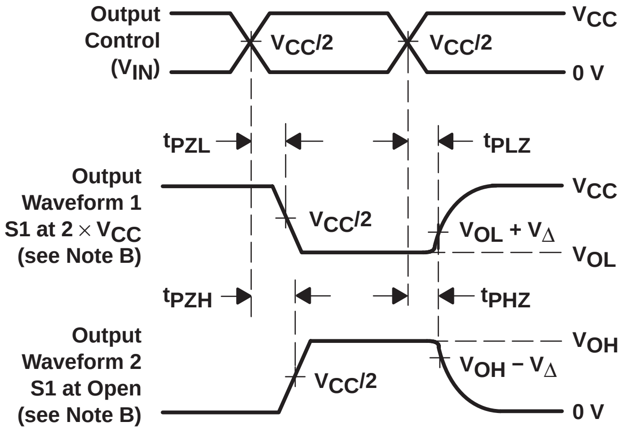
PARAMETER MEASUREMENT INFORMATION


V_{CC}
Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V


Output
Control
(V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

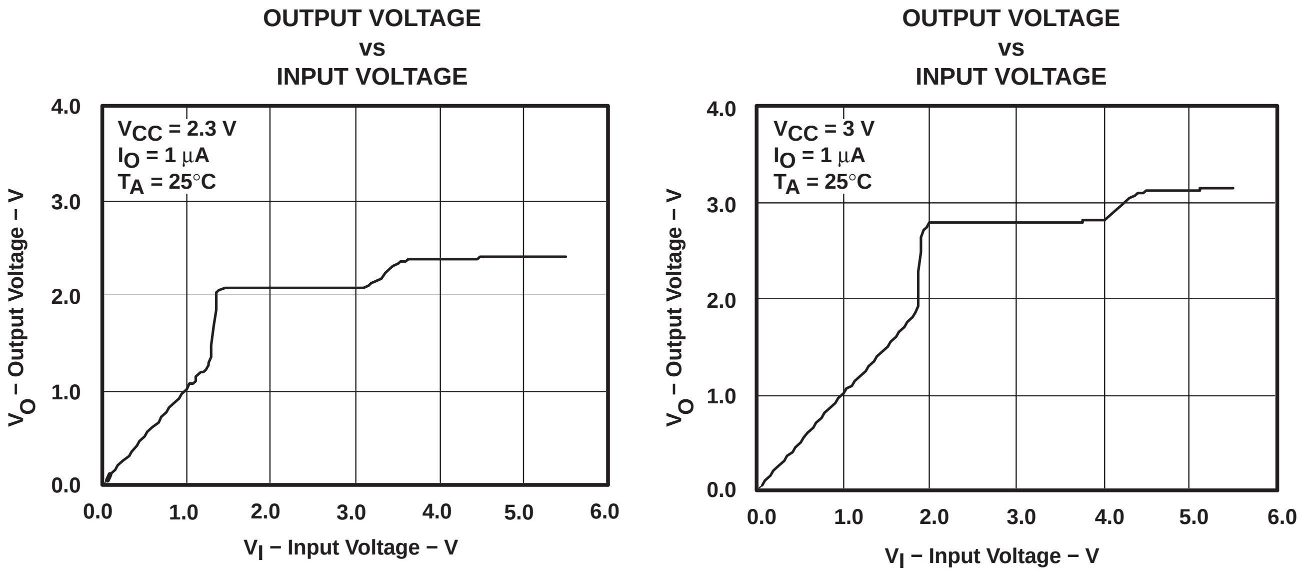

Output
Control
(V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 2 × V_{CC}
(see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

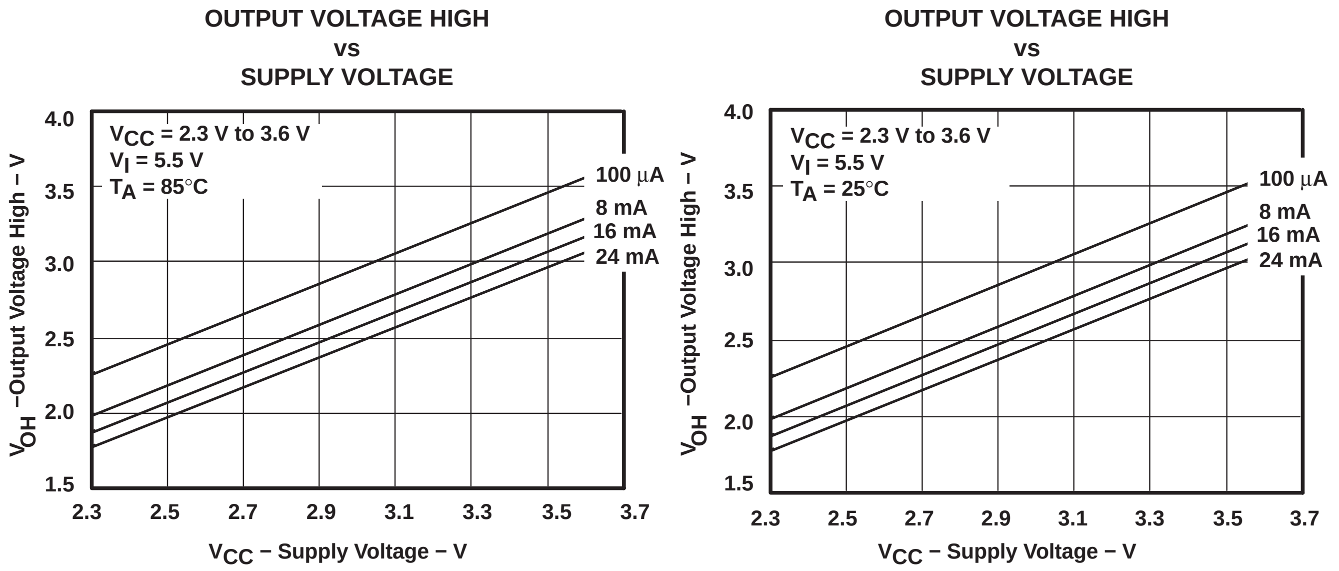


OUTPUT VOLTAGE vs INPUT VOLTAGE

OUTPUT VOLTAGE vs INPUT VOLTAGE

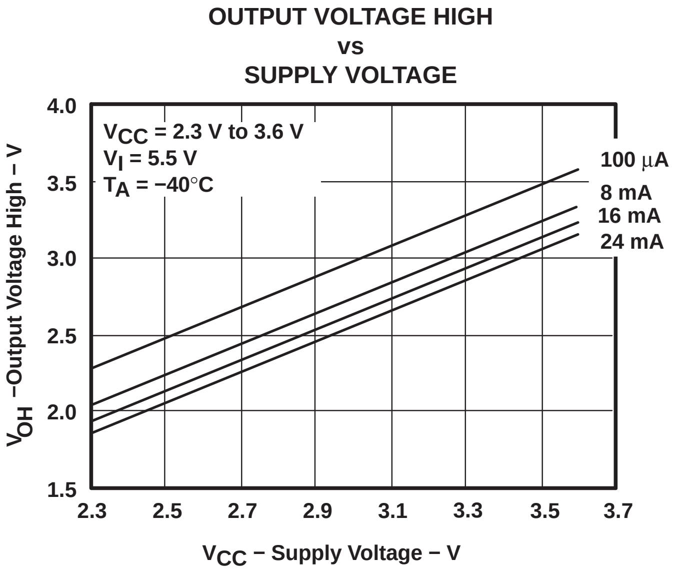
Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS (continued)



OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE

OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE



OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE

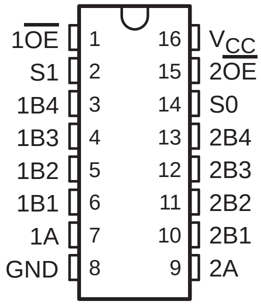
Figure 4. V_{OH} Values

SN74CB3T3253
DUAL 1-OF-4 FET MULTIPLEXER/DEMULTIPLEXER
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS148 − OCTOBER 2003

- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation On All Data I/O Ports**
  - **5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}**
- **5-V Tolerant I/Os With Device Powered-Up or Powered-Down**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 5 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 20 μA Max)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, USB Interface, Memory Interleaving, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

D, DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CB3T3253 is a high-speed TTL-compatible FET multiplexer/demultiplexer with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3253 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

The SN74CB3T3253 is organized as two 1-of-4 multiplexer/demultiplexers with separate output-enable (1$\overline{OE}$, 2$\overline{OE}$) inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When $\overline{OE}$ is low, the associated multiplexer/demultiplexer is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated multiplexer/demultiplexer is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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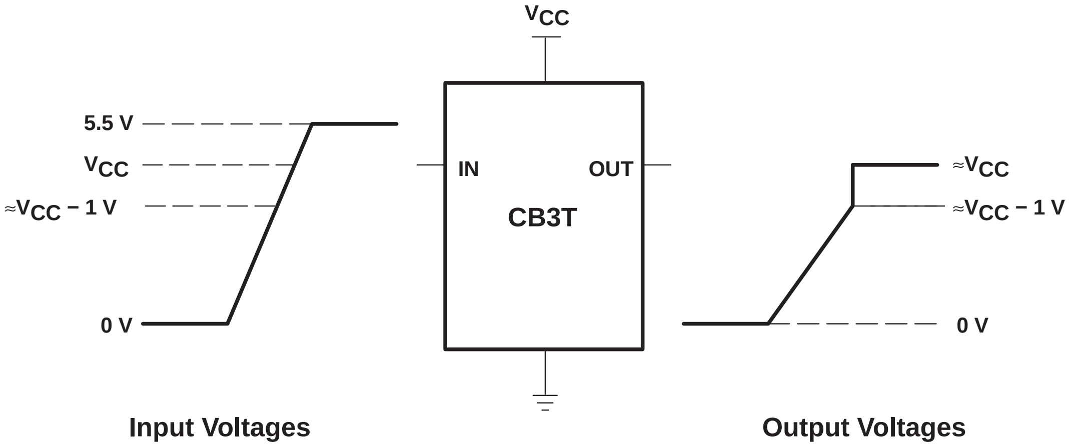
description/ordering information (continued)



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} − 1 V, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage-Translation Characteristics

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

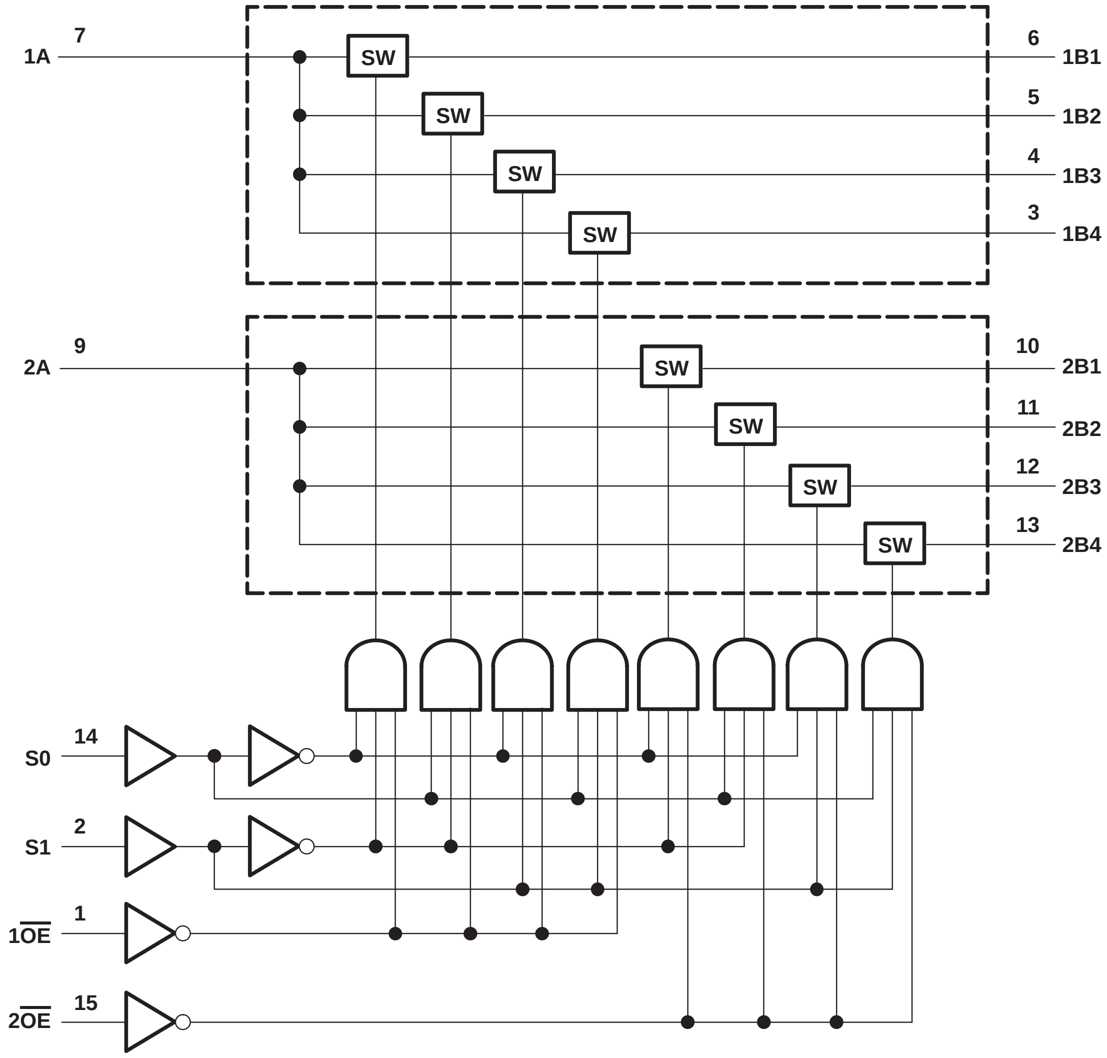
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − D	Tube	SN74CB3T3253D	CB3T3253
		Tape and reel	SN74CB3T3253DR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CB3T3253DBQR	KS253
	TSSOP − PW	Tube	SN74CB3T3253PW	KS253
		Tape and reel	SN74CB3T3253PWR	
	TVSOP − DGV	Tape and reel	SN74CB3T3253DGVR	KS253

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

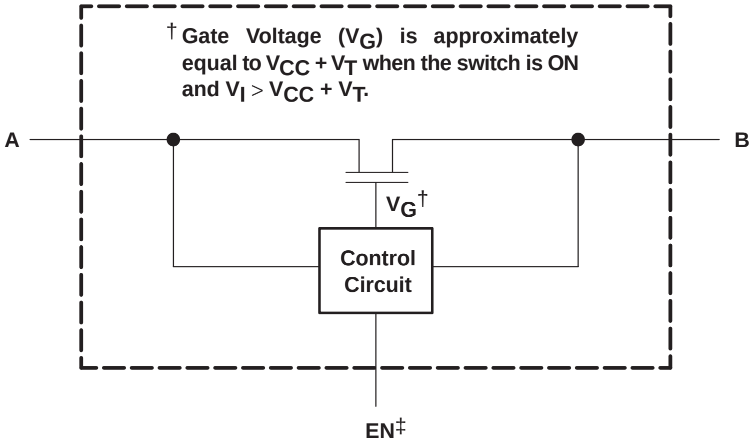
FUNCTION TABLE
(each multiplexer/demultiplexer)

INPUTS			INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S1	S0		
L	L	L	B1	A port = B1 port
L	L	H	B2	A port = B2 port
L	H	L	B3	A port = B3 port
L	H	H	B4	A port = B4 port
H	X	X	Z	Disconnect

logic diagram (positive logic)


1A
7
SW
SW
SW
SW
6
1B1
5
1B2
4
1B3
3
1B4
2A
9
SW
SW
SW
SW
10
2B1
11
2B2
12
2B3
13
2B4
S0
14
S1
2
1OE
1
2OE
15

simplified schematic, each FET switch (SW)


† Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
A
B
V_G†
Control Circuit
EN‡

‡ EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} (see Note 1)		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	D package	73°C/W
	DBQ package	90°C/W
	DGV package	120°C/W
	PW package	108°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{IK}		$V_{CC} = 3$ V, $I_I = -18$ mA				−1.2	V
V_{OH}		See Figures 3 and 4					
I_{IN}	Control inputs	$V_{CC} = 3.6$ V, $V_{IN} = 3.6$ V to 5.5 V or GND				±10	μA
I_I		$V_{CC} = 3.6$ V, Switch ON, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC} - 0.7$ V to 5.5 V			±20	μA
			$V_I = 0.7$ V to $V_{CC} - 0.7$ V			−40	
			$V_I = 0$ to 0.7 V			±5	
I_{OZ}[‡]		$V_{CC} = 3.6$ V, $V_O = 0$ to 5.5 V, $V_I = 0$, Switch OFF, $V_{IN} = V_{CC}$ or GND				±10	μA
I_{off}		$V_{CC} = 0$, $V_O = 0$ to 5.5 V, $V_I = 0$,				10	μA
I_{CC}		$V_{CC} = 3.6$ V, $I_{I/O} = 0$, Switch ON or OFF, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC}$ or GND			20	μA
			$V_I = 5.5$ V			20	
ΔI_{CC}[§]	Control inputs	$V_{CC} = 3$ V to 3.6 V, One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND				300	μA
C_{in}	Control inputs	$V_{CC} = 3.3$ V, $V_{IN} = V_{CC}$ or GND			3		pF
$C_{io(OFF)}$	A port	$V_{CC} = 3.3$ V, $V_{I/O} = 5.5$ V, 3.3 V, or GND, Switch OFF, $V_{IN} = V_{CC}$ or GND			12		pF
	B port				5		
$C_{io(ON)}$	A port	$V_{CC} = 3.3$ V, Switch ON, $V_{IN} = V_{CC}$ or GND	$V_{I/O} = 5.5$ V or 3.3 V		10		pF
			$V_{I/O} =$ GND		22		
	B port		$V_{I/O} = 5.5$ V or 3.3 V		4		
			$V_{I/O} =$ GND		22		
r_{on}[¶]		$V_{CC} = 2.3$ V, TYP at $V_{CC} = 2.5$ V, $V_I = 0$	$I_O = 24$ mA		5	8	Ω
			$I_O = 16$ mA		5	8	
		$V_{CC} = 3$ V, $V_I = 0$	$I_O = 64$ mA		5	7	
			$I_O = 32$ mA		5	7	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at $V_{CC} = 3.3$ V (unless otherwise noted), $T_A = 25°C$.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

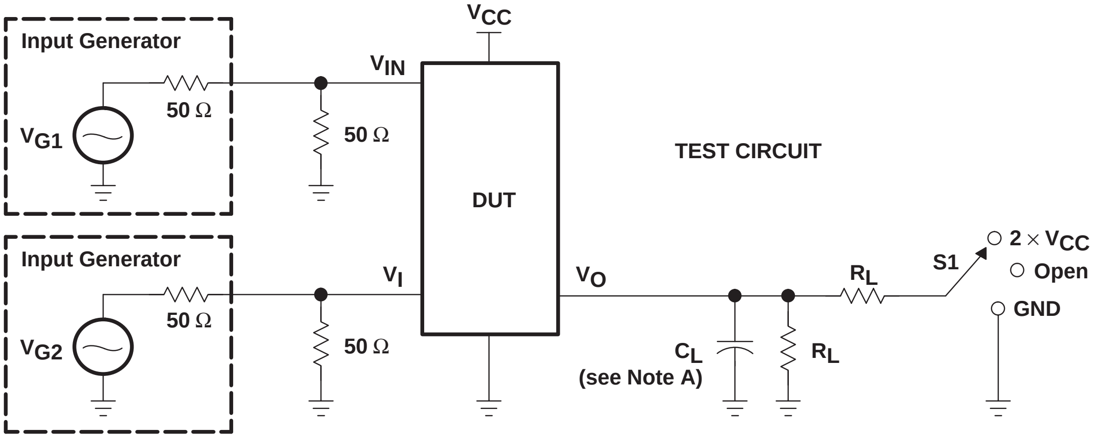
[¶] Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

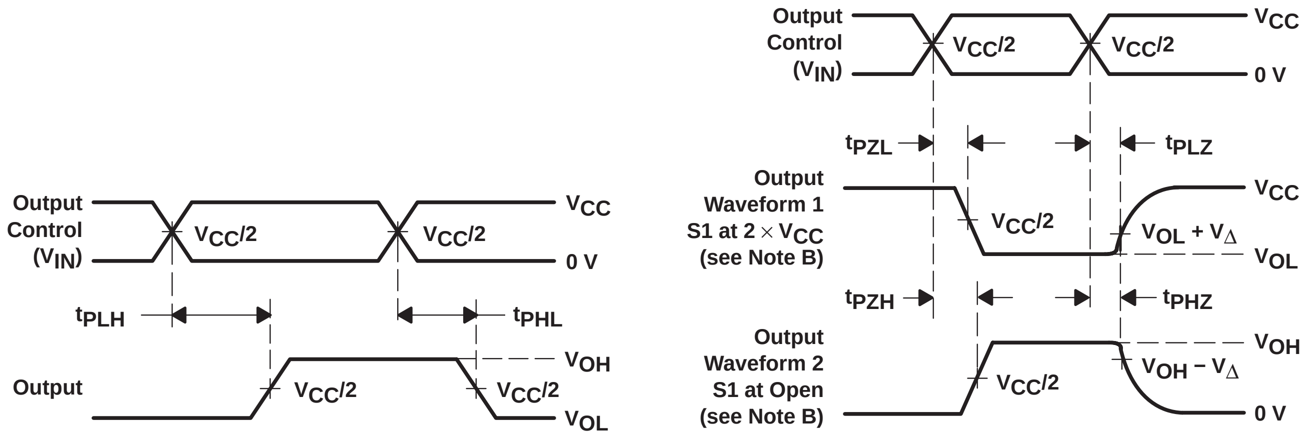
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.15		0.25	ns
$t_{pd(s)}$	S	A	1	10.5	1	8	ns
t_{en}	S	B	1	10	1	8	ns
	$\overline{OE}$	A or B	1	8.5	1	8	
t_{dis}	S	B	1	7.5	1	8.5	ns
	$\overline{OE}$	A or B	1	6.5	1	8	

[†] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
Output Control (V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

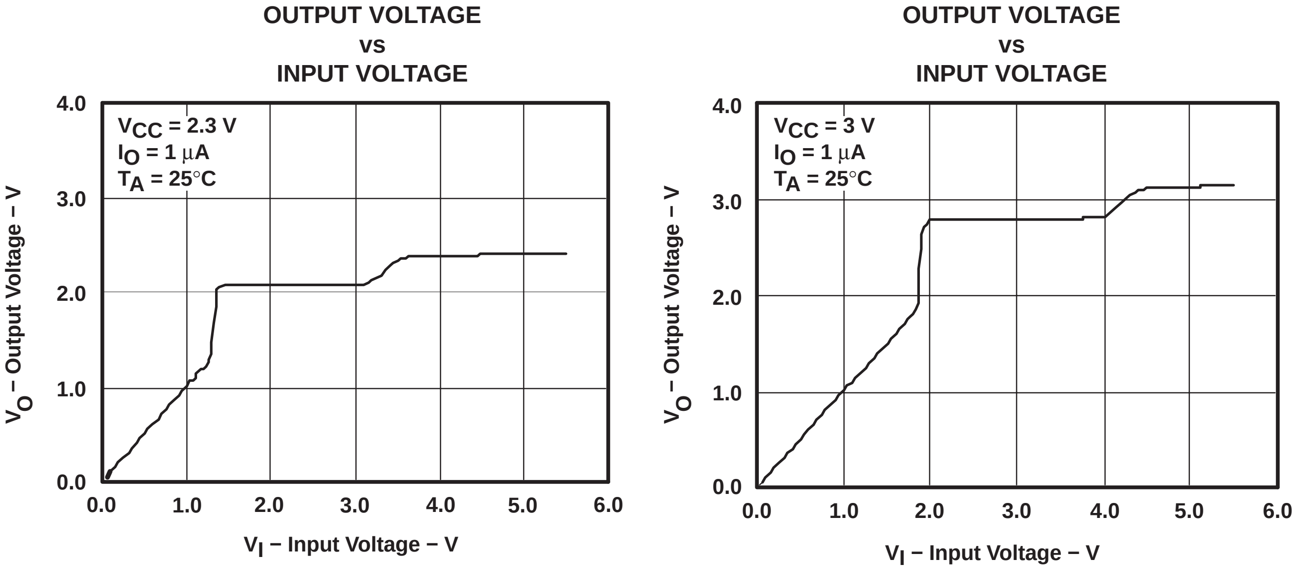
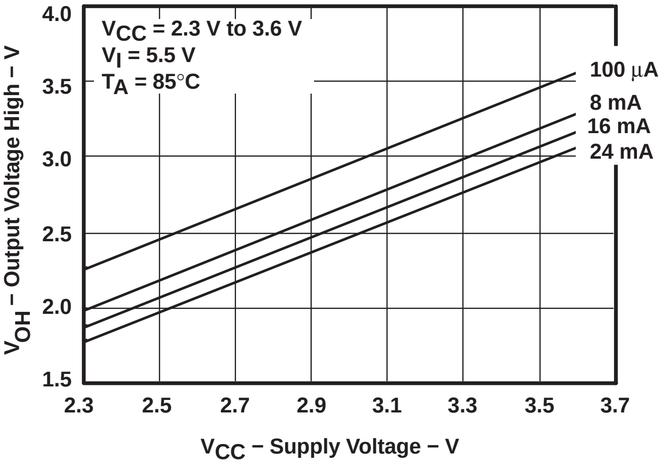


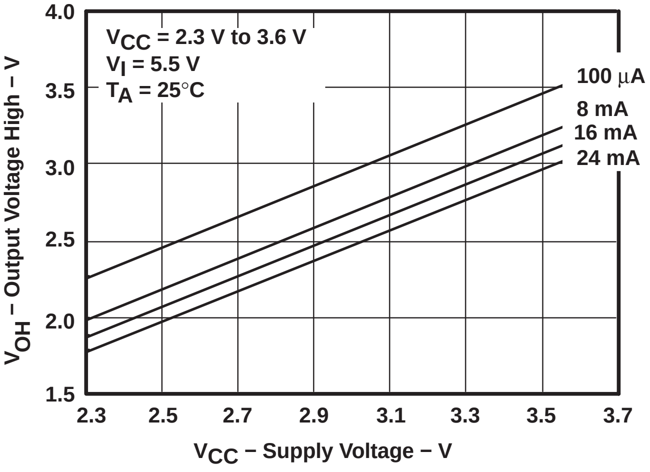
Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE



OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE



OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE

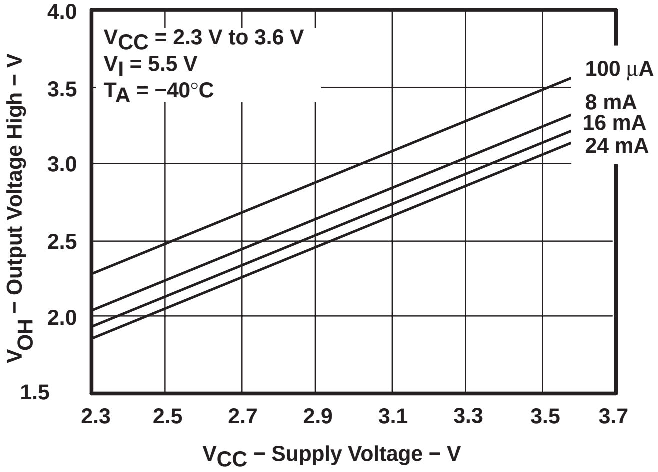


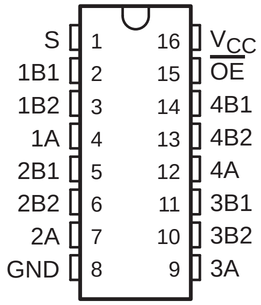
Figure 4. V_{OH} Values

SN74CB3T3257
4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS149 − OCTOBER 2003

- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation On All Data I/O Ports**
  - **5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}**
- **5-V Tolerant I/Os With Device Powered-Up or Powered-Down**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 5 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 20 μA Max)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, USB Interface, Memory Interleaving, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

DGV OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CB3T3257 is a high-speed TTL-compatible FET multiplexer/demultiplexer with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3257 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TSSOP − PW	Tube	SN74CB3T3257PW	KS257
		Tape and reel	SN74CB3T3257PWR	
	TVSOP − DGV	Tape and reel	SN74CB3T3257DGVR	KS257

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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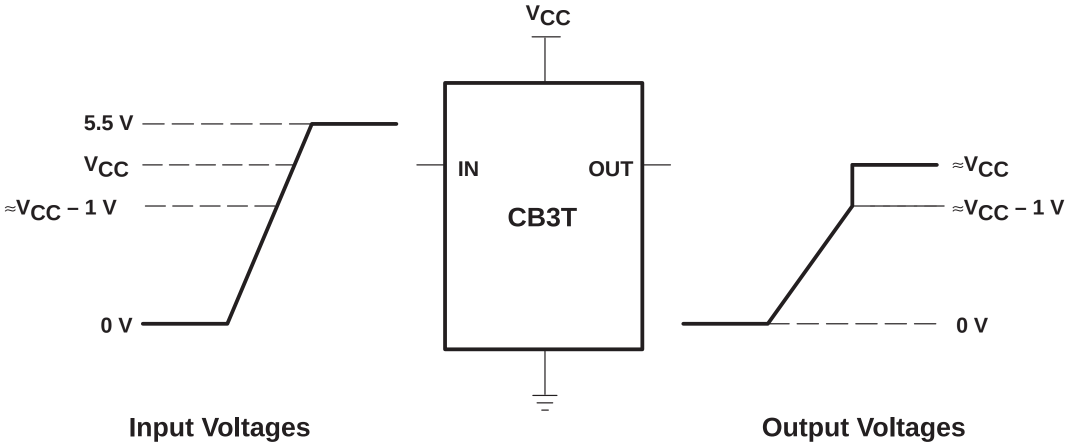
description/ordering information (continued)



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} − 1 V, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage-Translation Characteristics

The SN74CB3T3257 is a 4-bit 1-of-2 multiplexer/demultiplexer with a single output-enable ($\overline{OE}$) input. The select (S) input controls the data path of the multiplexer/demultiplexer. When $\overline{OE}$ is low, the multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

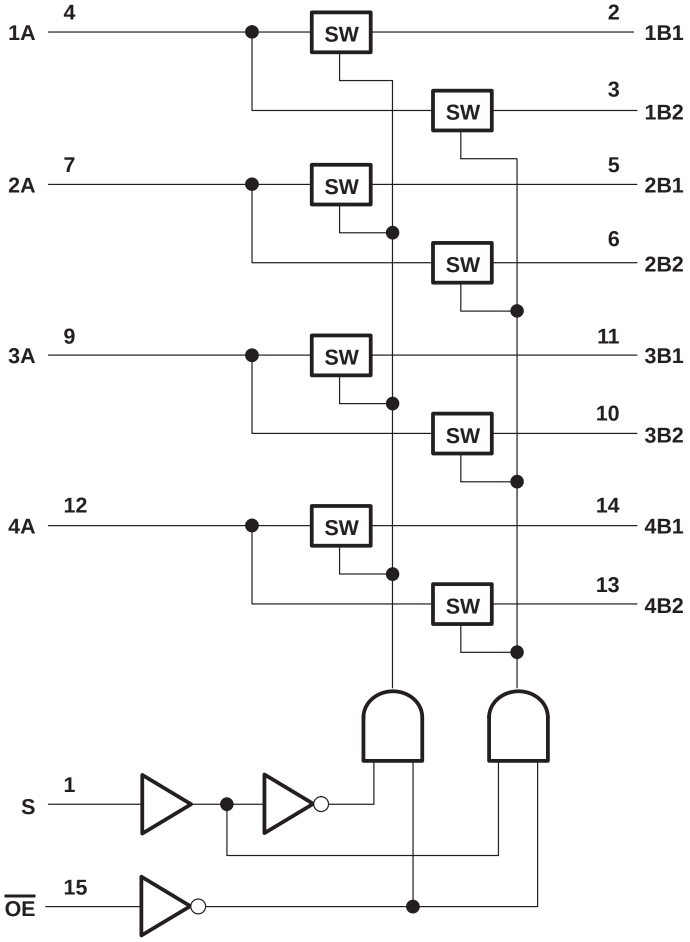
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

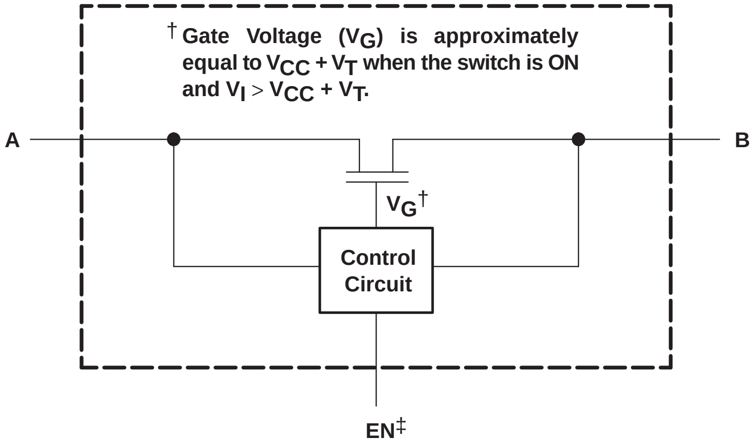
FUNCTION TABLE
(each multiplexer/demultiplexer)

INPUTS		INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S		
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect

logic diagram (positive logic)


1A
4
SW
2
1B1
SW
3
1B2
2A
7
SW
5
2B1
SW
6
2B2
3A
9
SW
11
3B1
SW
10
3B2
4A
12
SW
14
4B1
SW
13
4B2
S
1
OE
15

simplified schematic, each FET switch (SW)


† Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
A
B
V_G†
Control Circuit
EN‡

‡ EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DGV package	120°C/W
	PW package	108°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = −18 mA				−1.2	V
V_{OH}		See Figures 3 and 4					
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 3.6 V to 5.5 V or GND				±10	µA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} − 0.7 V to 5.5 V			±20	µA
			V_I = 0.7 V to V_{CC} − 0.7 V			−40	
			V_I = 0 to 0.7 V			±5	
I_{OZ}[‡]		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND				±10	µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0,				10	µA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND			20	µA
			V_I = 5.5 V			20	
ΔI_{CC}[§]	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				300	µA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND			3		pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND			7		pF
	B port				5		
$C_{io(ON)}$	A port	V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V		6		pF
			$V_{I/O}$ = GND		16		
	B port		$V_{I/O}$ = 5.5 V or 3.3 V		4		
			$V_{I/O}$ = GND		16		
r_{on}[¶]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA		5	8	Ω
			I_O = 16 mA		5	8	
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA		5	7	
			I_O = 32 mA		5	7	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

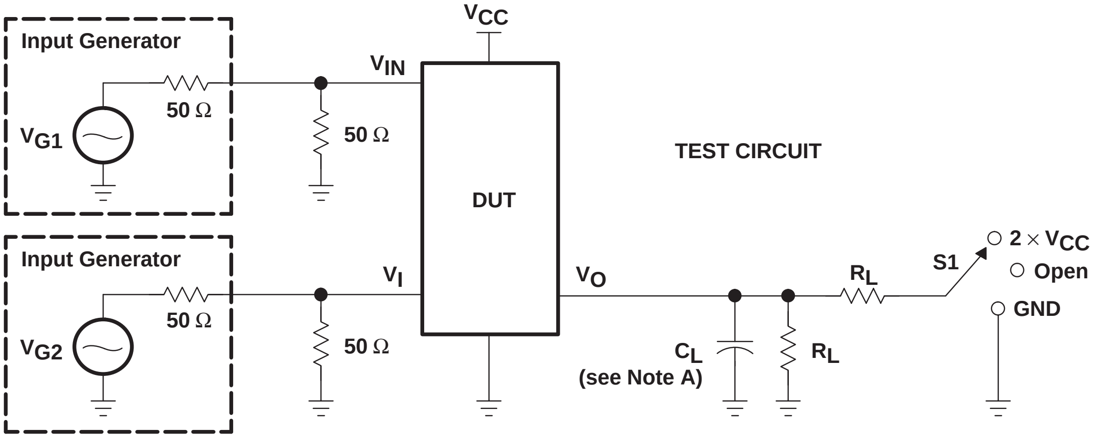
[¶] Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

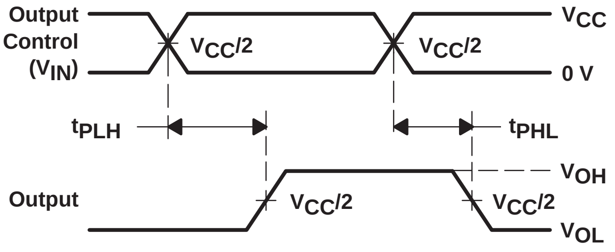
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.15		0.25	ns
$t_{pd(s)}$	S	A	1	9.5	1	7	ns
t_{en}	S	B	1	9	1	7.5	ns
	$\overline{OE}$	A or B	1	9	1	7.5	
t_{dis}	S	B	1	7	1	7.5	ns
	$\overline{OE}$	A or B	1	6	1	8	

[†] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

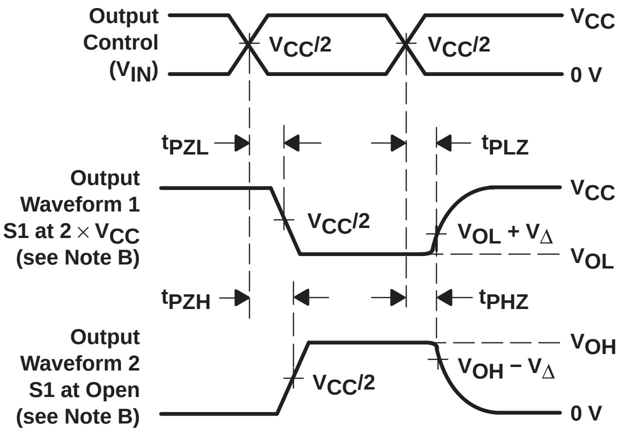
PARAMETER MEASUREMENT INFORMATION


V_{CC}
Input Generator
V_{IN}
50 Ω
V_{G1}
50 Ω
TEST CIRCUIT
DUT
Input Generator
V_I
V_O
R_L
S1
2 × V_{CC}
Open
GND
50 Ω
V_{G2}
50 Ω
C_L
(see Note A)
R_L

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V


Output
Control
(V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)


Output
Control
(V_{IN})
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 2 × V_{CC}
(see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

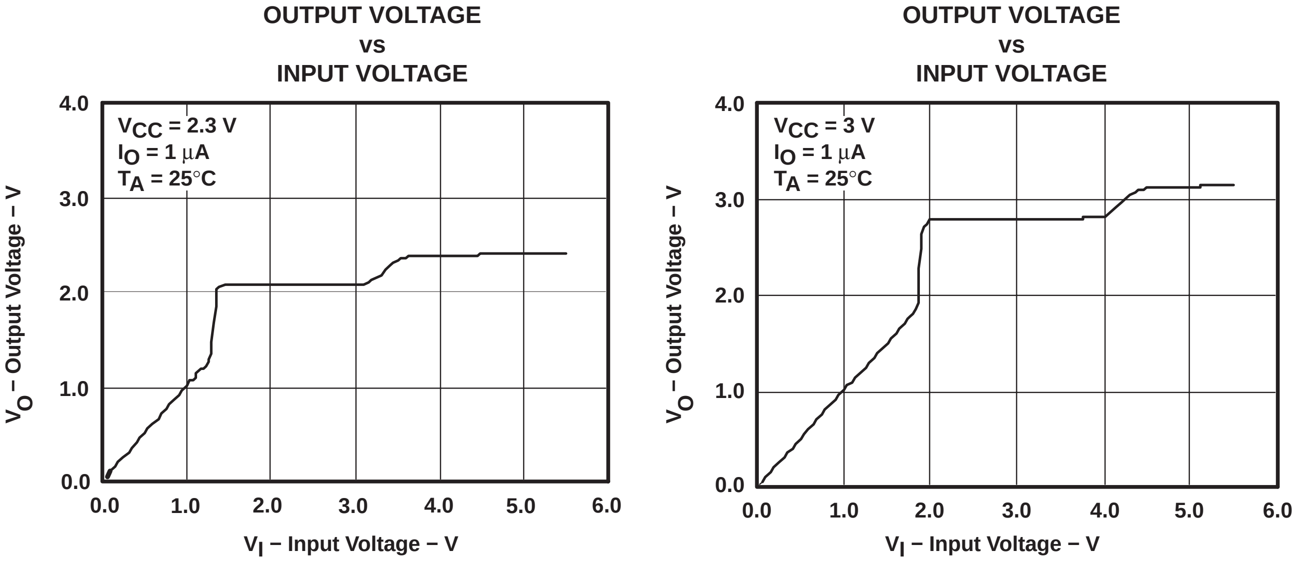


Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS (continued)

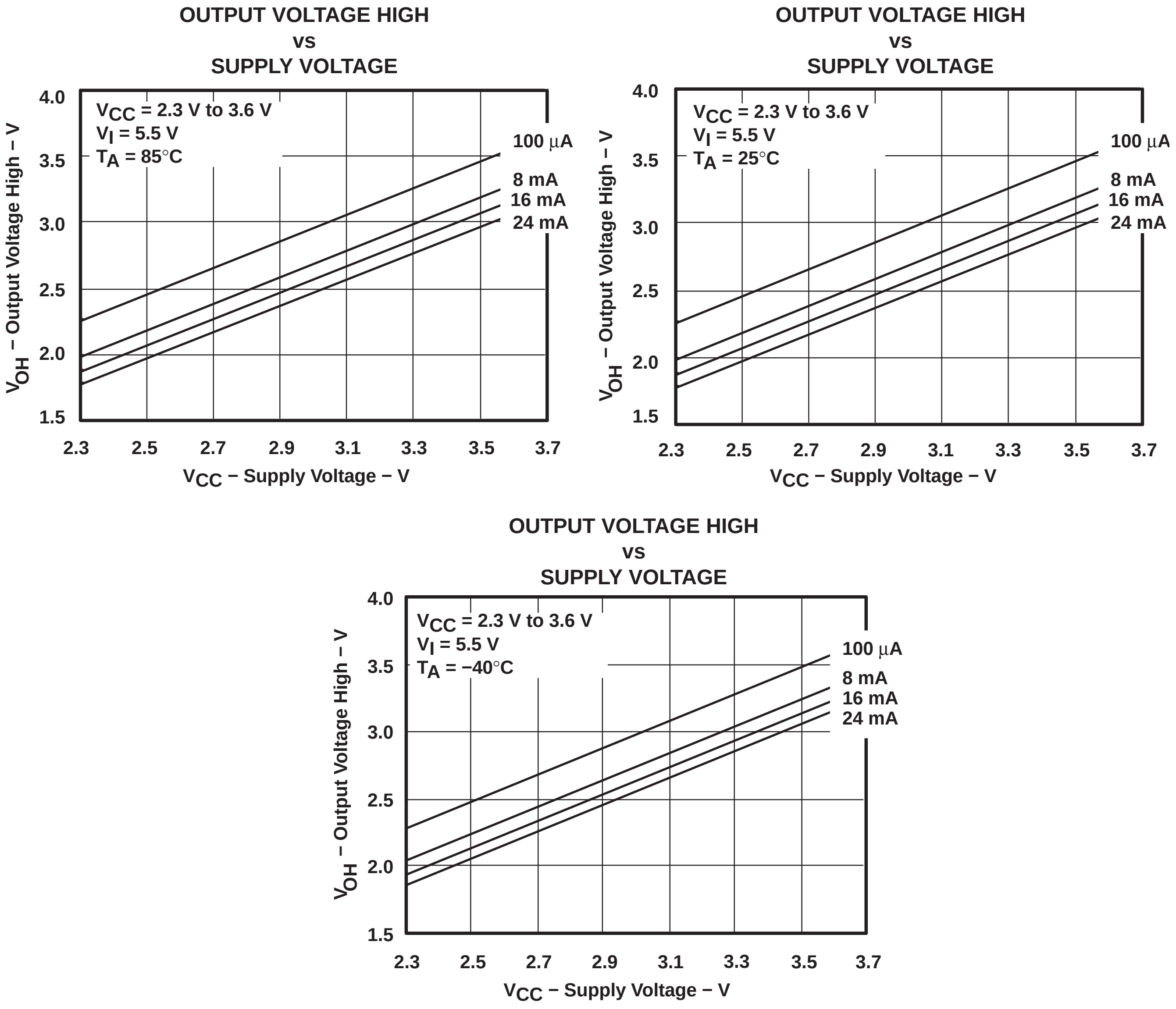


Figure 4. V_{OH} Values

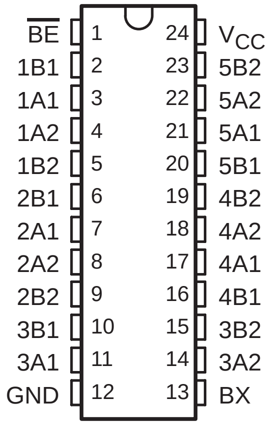
SN74CB3T3383
10-BIT FET BUS-EXCHANGE SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER

SCDS158 − OCTOBER 2003

- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation On All Data I/O Ports**
  - **5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}**
- **5-V-Tolerant I/Os With Device Powered-Up or Powered-Down**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics**
- **Low Input/Output Capacitance Minimizes Loading**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, Memory Interleaving, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

PRODUCT PREVIEW

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CB3T3383DW	
		Tape and reel	SN74CB3T3383DWR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CB3T3383DBQR	
	TSSOP − PW	Tape and reel	SN74CB3T3383PWR	
	TVSOP − DGV	Tape and reel	SN74CB3T3383DGVR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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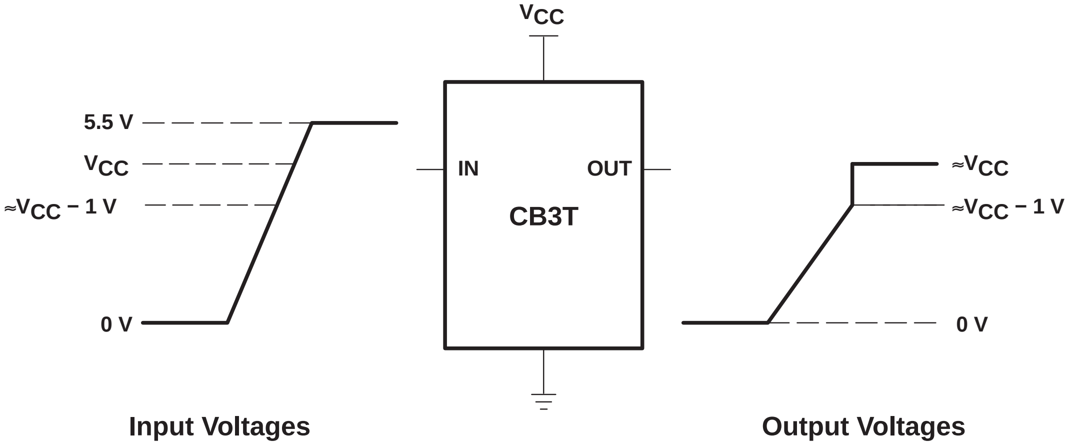
description/ordering information (continued)

The SN74CB3T3383 is a high-speed TTL-compatible FET bus-exchange switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3383 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} − 1 V, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage Translation Characteristics

The SN74CB3T3383 is organized as a 10-bit bus switch or as a 5-bit bus-exchange with enable ($\overline{BE}$) input.When used as a 5-bit bus-exchange, the device provides data exchanging between four signal ports. When $\overline{BE}$ is low, the bus-exchange switch is ON, and the select input (BX) controls the data path. When $\overline{BE}$ is high, the bus-exchange switch is OFF, and a high-impedance state exists between the A and B ports.

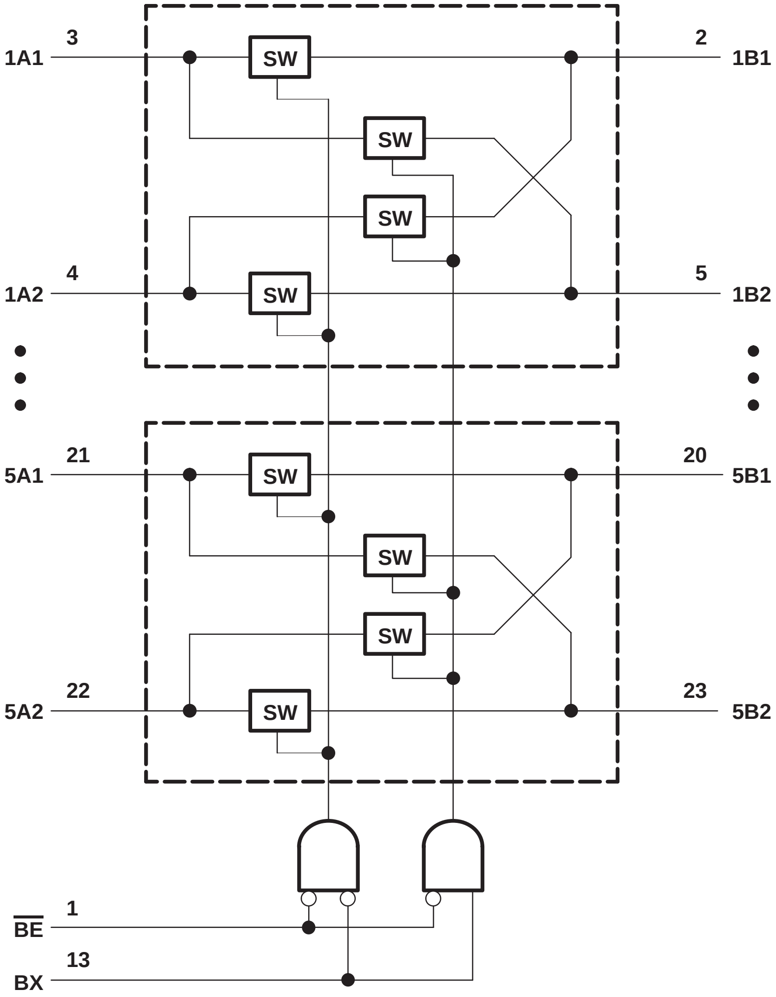
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{BE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each 5-bit switch)

INPUTS		INPUTS/OUTPUTS		FUNCTION
$\overline{\text{BE}}$	BX	A1	A2	
L	L	B1	B2	A1 port = B1 port A2 port = B2 port
L	H	B2	B1	A1 port = B2 port A2 port = B1 port
H	X	Z	Z	Disconnect

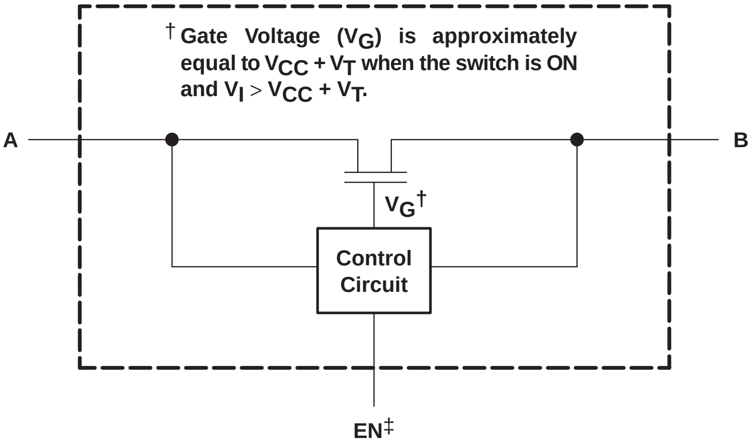
logic diagram (positive logic)


1A1
3
SW
2
1B1
SW
SW
1A2
4
SW
5
1B2
5A1
21
SW
20
5B1
SW
SW
5A2
22
SW
23
5B2
$\overline{\text{BE}}$
1
BX
13

PRODUCT PREVIEW

PRODUCT PREVIEW

simplified schematic, each FET switch (SW)


† Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
A
B
V_G†
Control Circuit
EN‡

‡ EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} (see Note 1)	−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DBQ package	61°C/W
DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = −18 mA					V
V_{OH}		See Figures 3 and 4					
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 3.6 V to 5.5 V or GND					μA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} − 0.7 V to 5.5 V				μA
			V_I = 0.7 V to V_{CC} − 0.7 V				
			V_I = 0 to 0.7 V				
I_{OZ}[‡]		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND					μA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0,					μA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND				μA
			V_I = 5.5 V				
ΔI_{CC}[§]	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND					μA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND					pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND					pF
$C_{io(ON)}$		V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V				pF
			$V_{I/O}$ = GND				
r_{on}[¶]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA				Ω
			I_O = 16 mA				
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA				
			I_O = 32 mA				

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

PRODUCT PREVIEW

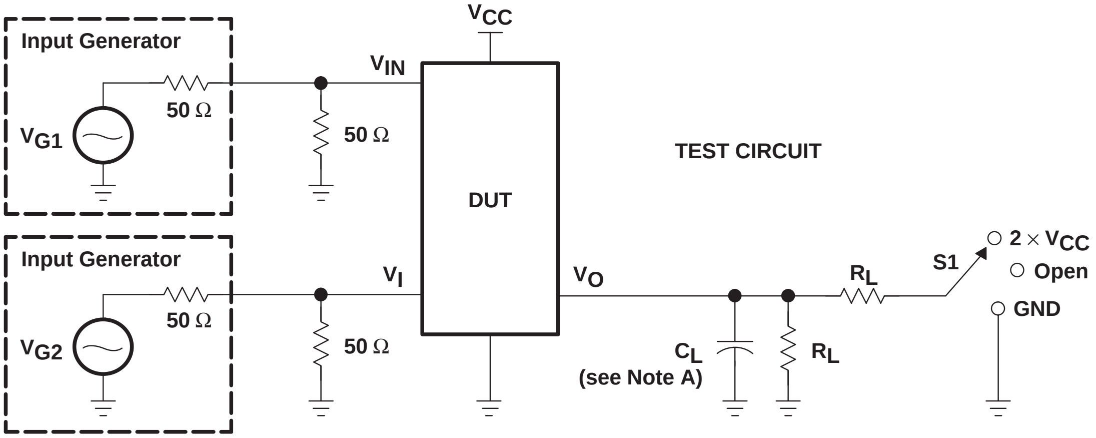
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A					ns
$t_{pd(s)}$	BX	A or B					
t_{en}	$\overline{BE}$	A or B					ns
t_{dis}	$\overline{BE}$	A or B					ns

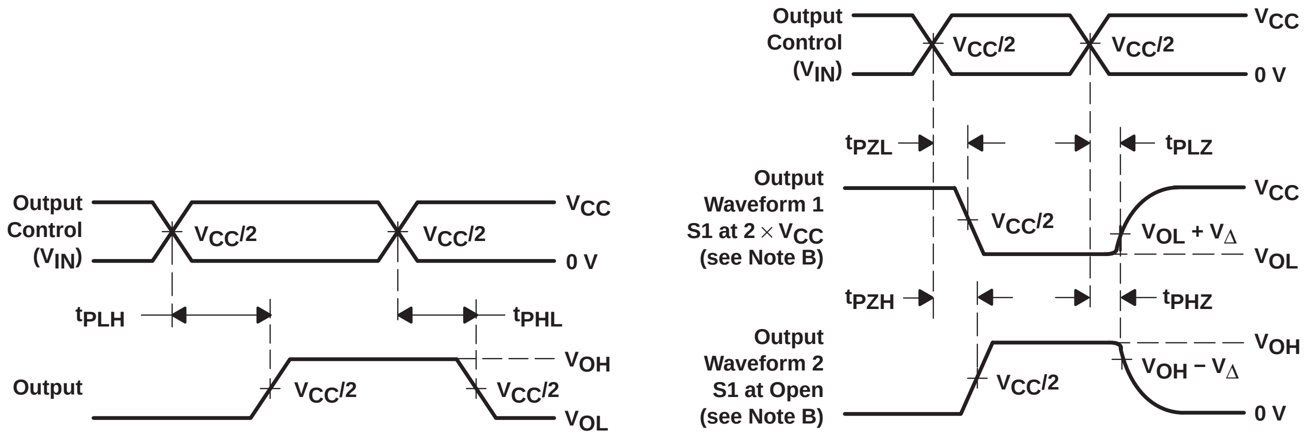
[†] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION


V_{CC}
Input Generator
V_{IN}
50 Ω
V_{G1}
50 Ω
TEST CIRCUIT
DUT
Input Generator
V_I
V_O
R_L
S1
2 × V_{CC}
Open
GND
50 Ω
V_{G2}
50 Ω
C_L
(see Note A)
R_L

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V


Output Control (V_{IN})
V_{CC}/2
V_{CC}/2
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
V_{CC}/2
V_{CC}/2
V_{OH}
V_{OL}
Output Control (V_{IN})
V_{CC}/2
V_{CC}/2
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
V_{CC}/2
V_{CC}
V_{OL} + V_Δ
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
V_{CC}/2
V_{OH}
V_{OH} − V_Δ
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

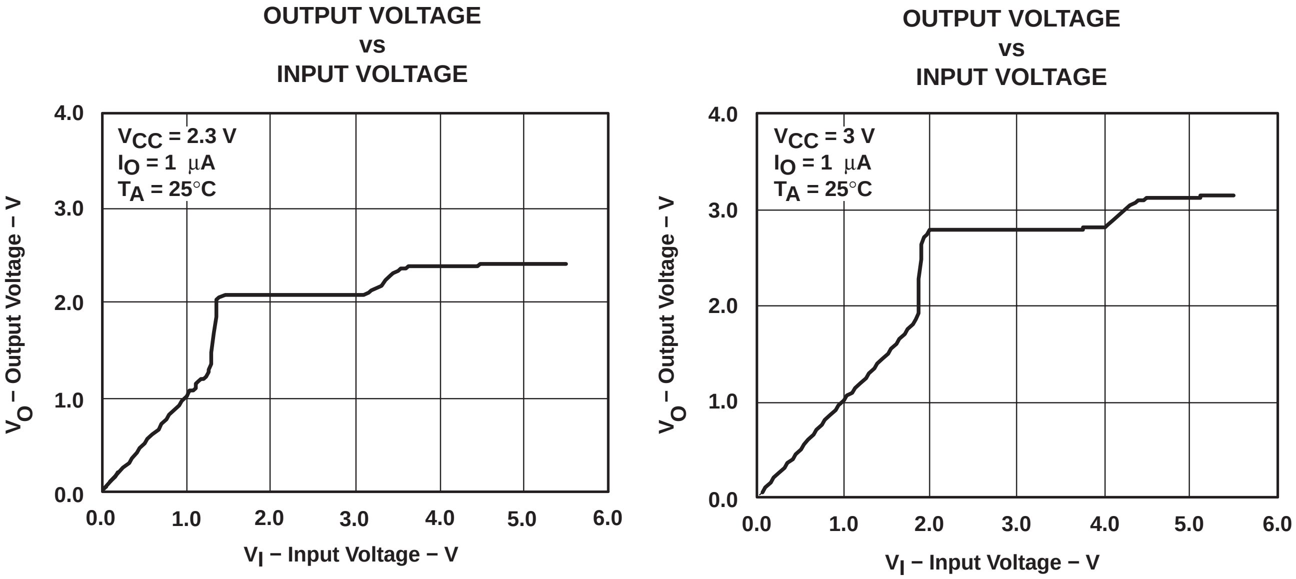


Figure 3. Data Output Voltage vs Data Input Voltage

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

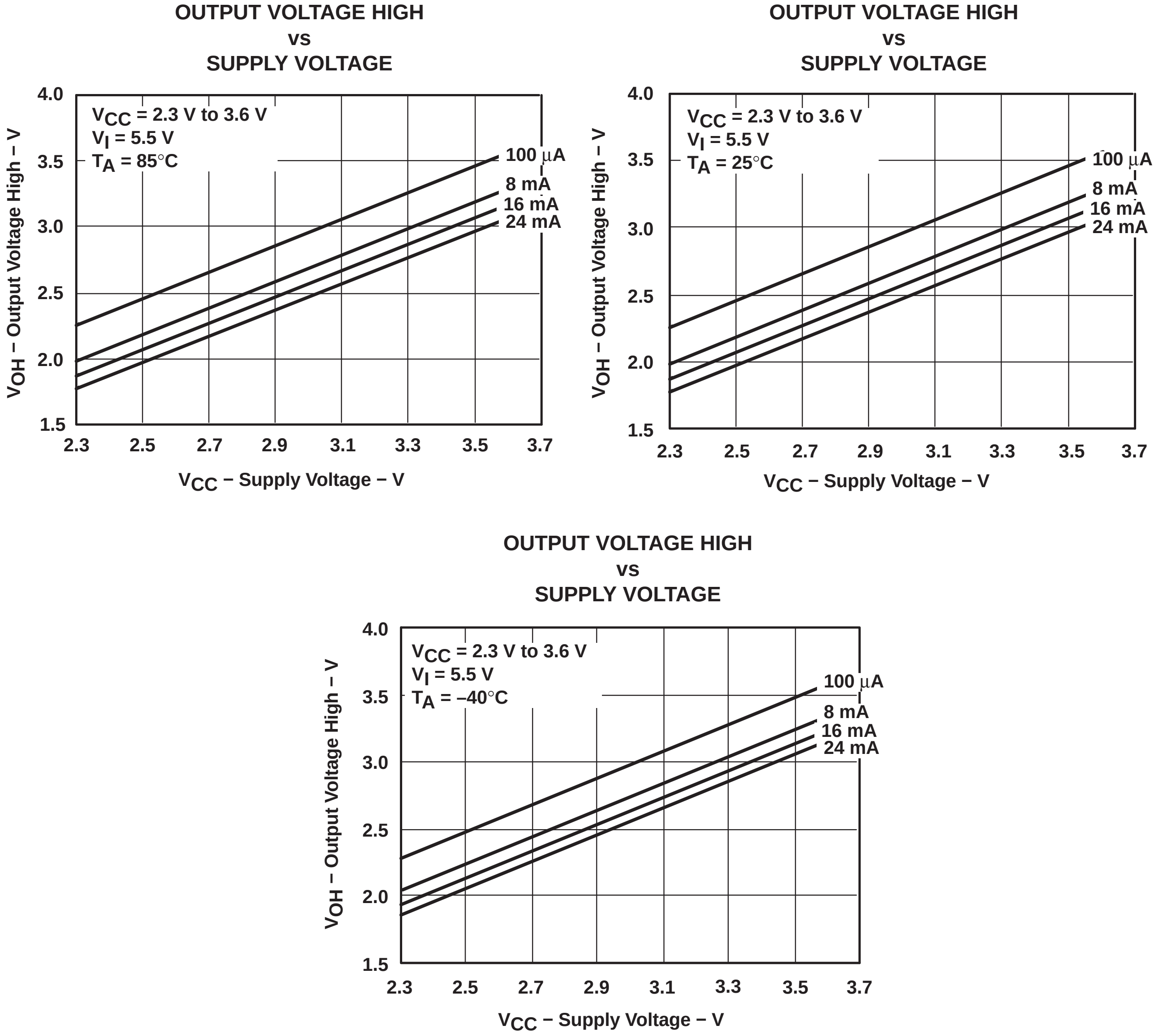


Figure 4. V_{OH} Values

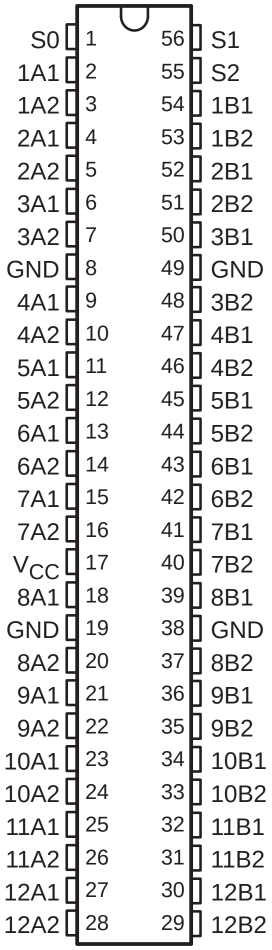
PRODUCT PREVIEW

SN74CB3T16212
24-BIT FET BUS-EXCHANGE SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER

SCDS157 − OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation On All Data I/O Ports**
  - **5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}**
- **5-V-Tolerant I/Os With Device Powered-Up or Powered-Down**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics**
- **Low Input/Output Capacitance Minimizes Loading**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, PCI Interface, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


S0 1 56 S1
1A1 2 55 S2
1A2 3 54 1B1
2A1 4 53 1B2
2A2 5 52 2B1
3A1 6 51 2B2
3A2 7 50 3B1
GND 8 49 GND
4A1 9 48 3B2
4A2 10 47 4B1
5A1 11 46 4B2
5A2 12 45 5B1
6A1 13 44 5B2
6A2 14 43 6B1
7A1 15 42 6B2
7A2 16 41 7B1
V_{CC} 17 40 7B2
8A1 18 39 8B1
GND 19 38 GND
8A2 20 37 8B2
9A1 21 36 9B1
9A2 22 35 9B2
10A1 23 34 10B1
10A2 24 33 10B2
11A1 25 32 11B1
11A2 26 31 11B2
12A1 27 30 12B1
12A2 28 29 12B2

PRODUCT PREVIEW

description/ordering information

The SN74CB3T16212 is a high-speed TTL-compatible FET bus-exchange switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T16212 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

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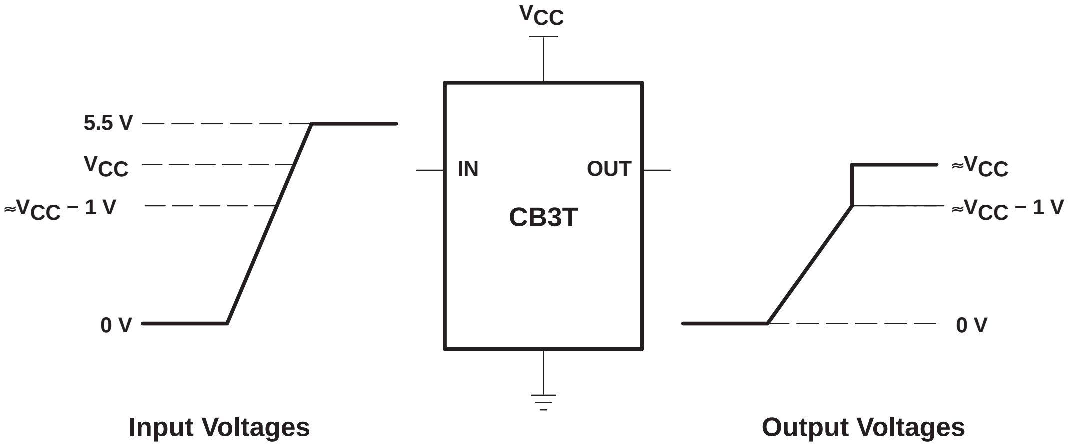
PRODUCT PREVIEW

description/ordering information (continued)



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} − 1 V, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage Translation Characteristics

The SN74CB3T16212 operates as a 24-bit bus switch or as a 12-bit bus-exchange that provides data exchanging between four signal ports. The select (S0, S1, S2) inputs control the data path of the bus-exchange switch. When the bus-exchange switch is ON, the A port is connected to the B port, allowing bidirectional data flow between ports. When the bus-exchange switch is OFF, a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, each select input should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CB3T16212DL	
		Tape and reel	SN74CB3T16212DLR	
	TSSOP − DGG	Tube	SN74CB3T16212DGG	
		Tape and reel	SN74CB3T16212DGGR	
	TVSOP − DGV	Tape and reel	SN74CB3T16212DGVR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

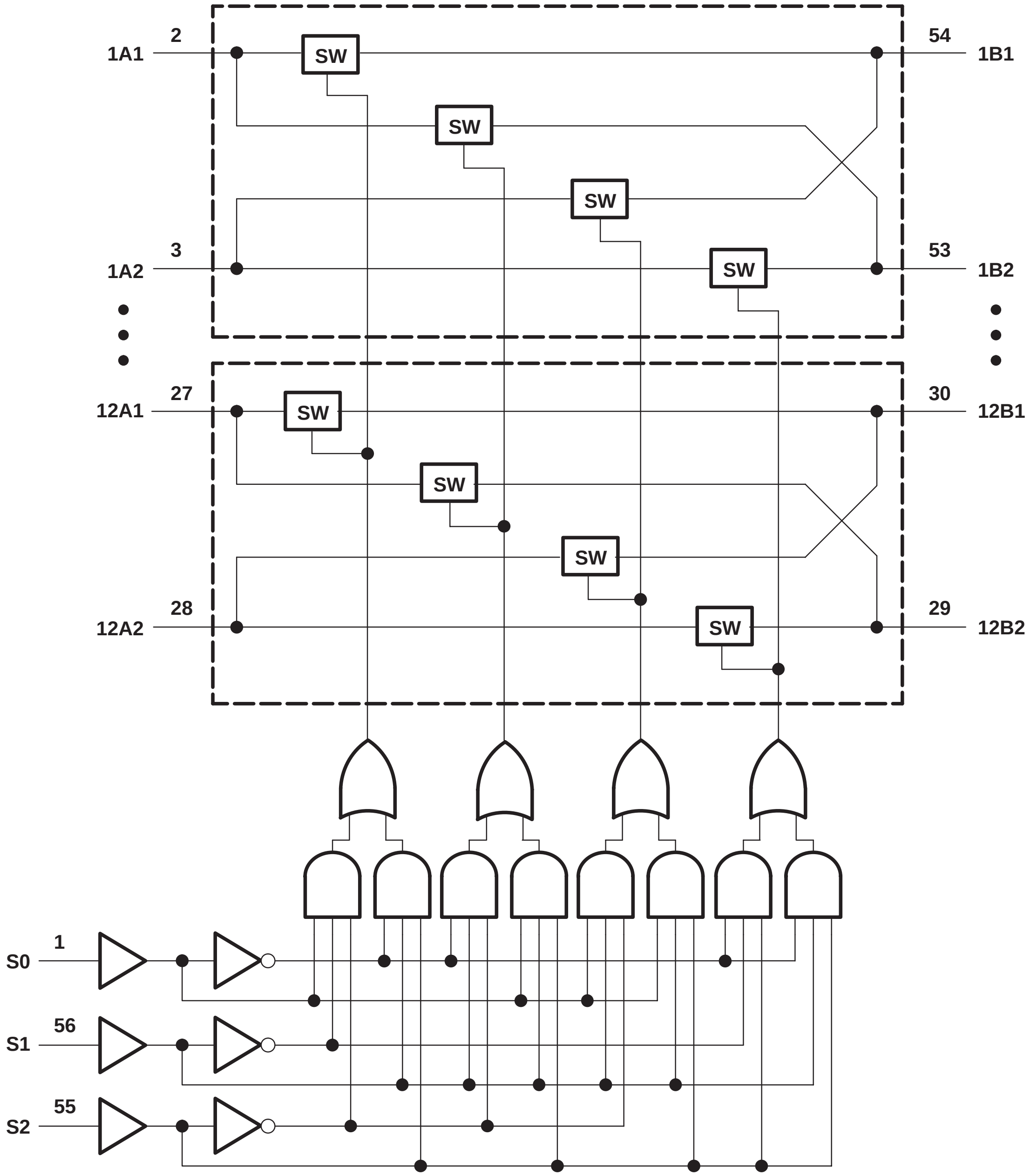
FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	**S1**	**S0**	**A1**	**A2**	
L	L	L	Z	Z	Disconnect
L	L	H	B1 port	Z	A1 port = B1 port
L	H	L	B2 port	Z	A1 port = B2 port
L	H	H	Z	B1 port	A2 port = B1 port
H	L	L	Z	B2 port	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1 port	B2 port	A1 port = B1 port A2 port = B2 port
H	H	H	B2 port	B1 port	A1 port = B2 port A2 port = B1 port

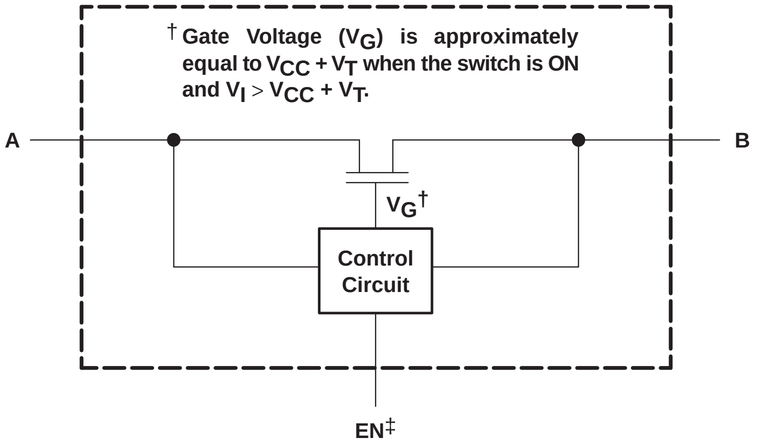
PRODUCT PREVIEW

PRODUCT PREVIEW

logic diagram (positive logic)


1A1
2
SW
54
1B1
SW
SW
1A2
3
SW
53
1B2
12A1
27
SW
30
12B1
SW
SW
12A2
28
SW
29
12B2
S0
1
S1
56
S2
55

simplified schematic, each FET switch (SW)


† Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
A
B
V_G†
Control Circuit
EN‡

‡ EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} (see Note 1)		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = −18 mA					V
V_{OH}		See Figures 3 and 4					
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 3.6 V to 5.5 V or GND					µA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} − 0.7 V to 5.5 V				µA
			V_I = 0.7 V to V_{CC} − 0.7 V				
			V_I = 0 to 0.7 V				
I_{OZ}‡		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND					µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0,					µA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND				µA
			V_I = 5.5 V				
ΔI_{CC}§	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND					µA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND					pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND					pF
	B port						
$C_{io(ON)}$	A port	V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V				pF
			$V_{I/O}$ = GND				
	B port		$V_{I/O}$ = 5.5 V or 3.3 V				
			$V_{I/O}$ = GND				
r_{on}¶		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA				Ω
			I_O = 16 mA				
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA				
			I_O = 32 mA				

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}†	A or B	B or A					ns
$t_{pd(s)}$	S	A					
t_{en}	S	B					ns
t_{dis}	S	B					ns

† The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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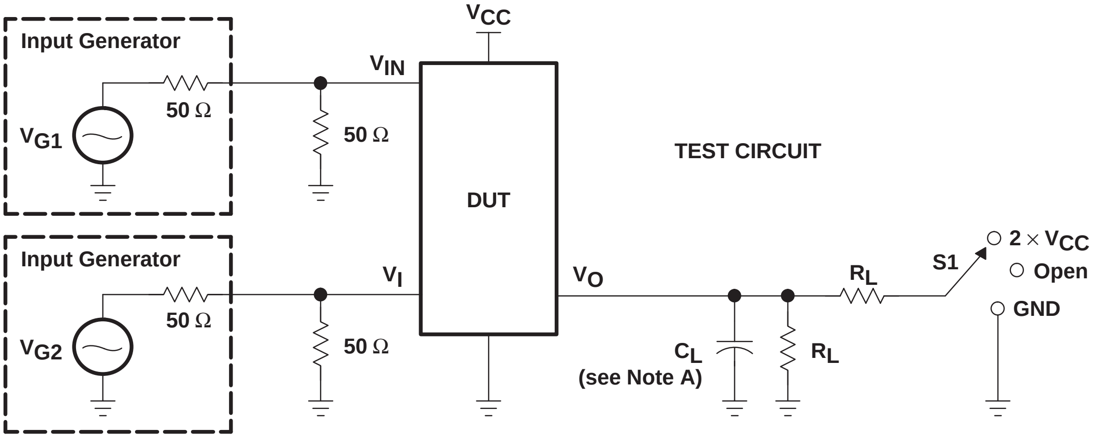
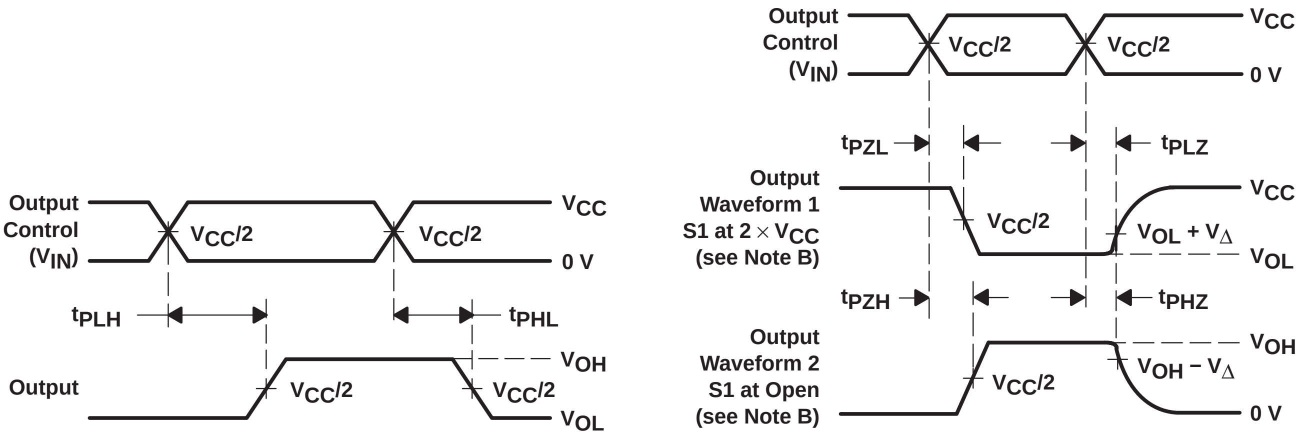
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION


VCC
Input Generator
VIN
50 Ω
VG1
50 Ω
TEST CIRCUIT
DUT
Input Generator
VI
VO
RL
S1
2 × VCC
Open
GND
VG2
50 Ω
50 Ω
CL
(see Note A)
RL

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V


Output Control (VIN)
VCC/2
VCC/2
VCC
0 V
tPLH
tPHL
Output
VCC/2
VCC/2
VOH
VOL
Output Control (VIN)
VCC/2
VCC/2
VCC
0 V
tPZL
tPLZ
Output Waveform 1 S1 at 2 × VCC (see Note B)
VCC/2
VOL + VΔ
VCC
VOL
tPZH
tPHZ
Output Waveform 2 S1 at Open (see Note B)
VCC/2
VOH − VΔ
VOH
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

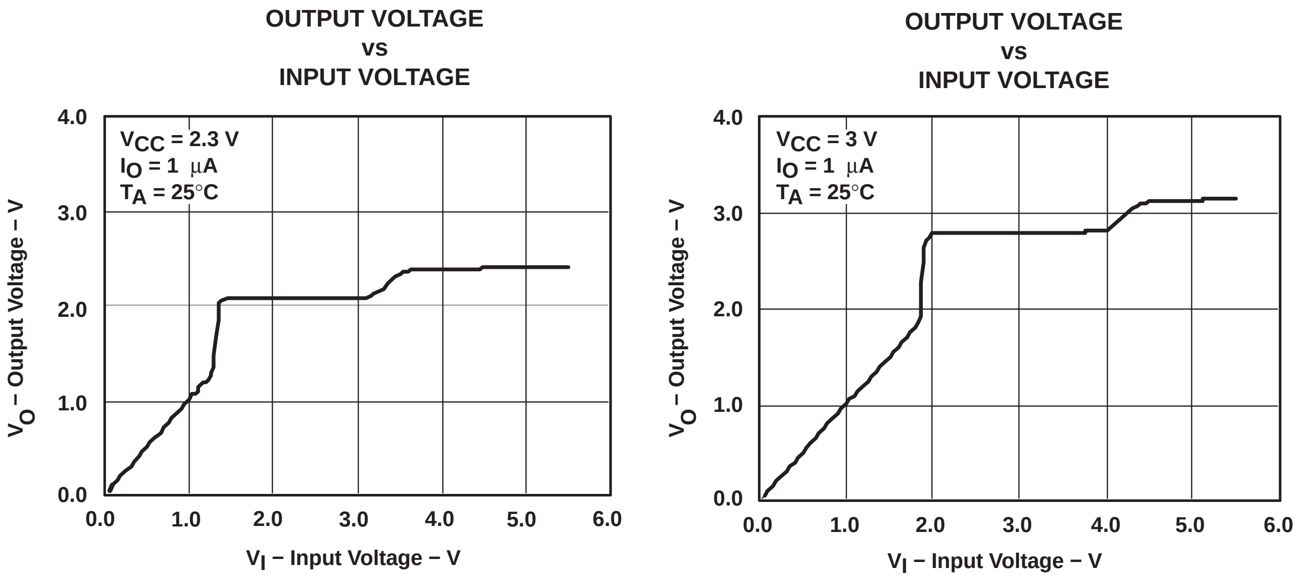


Figure 3. Data Output Voltage vs Data Input Voltage

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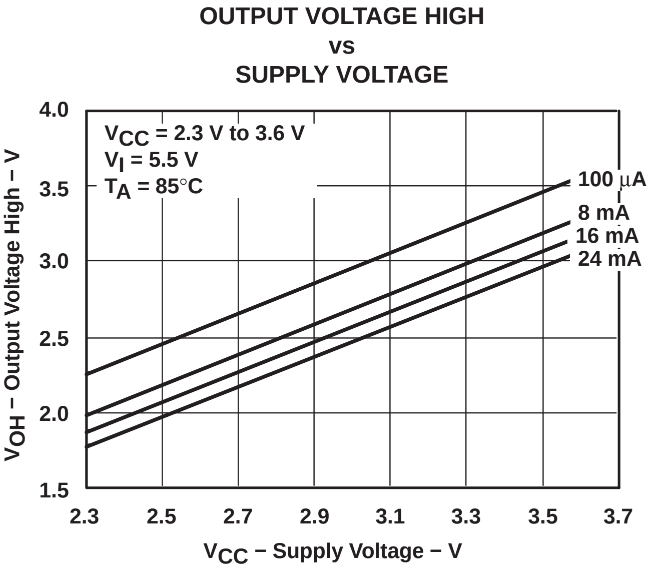
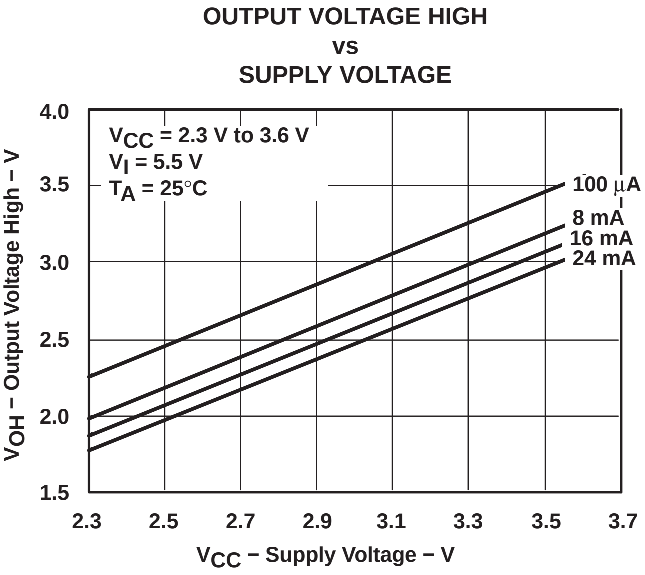
TYPICAL CHARACTERISTICS (continued)





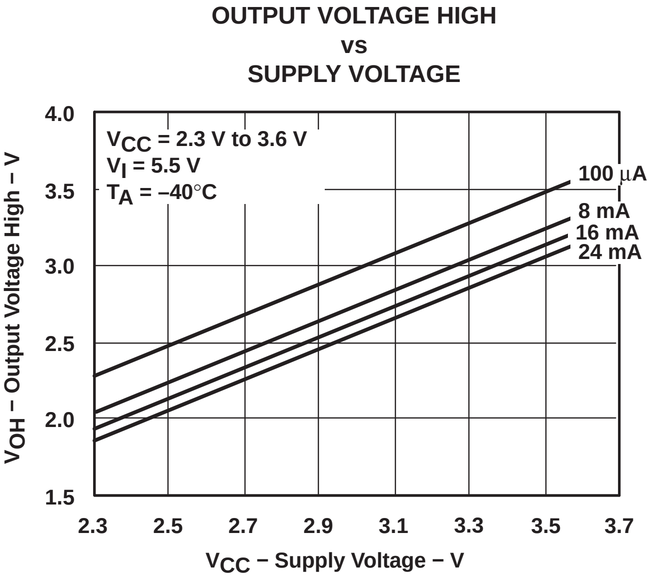


Figure 4. V_{OH} Values

PRODUCT PREVIEW

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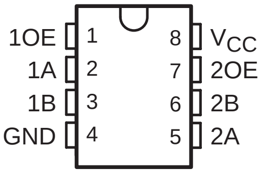
SN74CBT3305C
DUAL FET BUS SWITCH
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS125A − SEPTEMBER 2003 − REVISED OCTOBER 2003

- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 µA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: USB Interface, Bus Isolation, Low-Distortion Signal Gating**

D OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBT3305C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3305C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3305C is organized as two 1-bit bus switches with separate output-enable (1OE, 2OE) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When OE is high, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is low, the associated 1-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − D	Tube	SN74CBT3305CD	CU305C
		Tape and reel	SN74CBT3305CDR	
	TSSOP − PW	Tube	SN74CBT3305CPW	CU305C
		Tape and reel	SN74CBT3305CPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

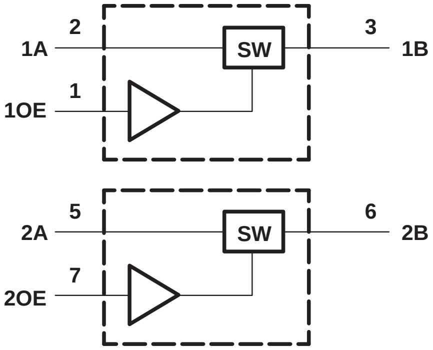
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

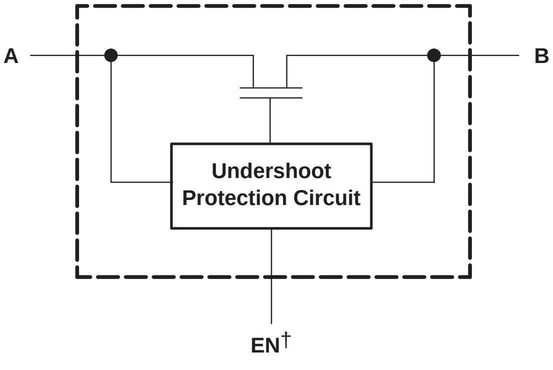
FUNCTION TABLE
(each bus switch)

INPUT OE	INPUT/OUTPUT A	FUNCTION
H	B	A port = B port
L	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): D package	97°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_{OZ}[‡]		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	μA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				3		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		12.5		pF
r_{on}[¶]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[#]	A or B	B or A		0.24		0.15	ns
t_{en}	OE	A or B		4.4	1.5	4.1	ns
t_{dis}	OE	A or B		5.1	1.5	4.8	ns

[#] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V, Switch OFF, V_{IN} = V_{CC} or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

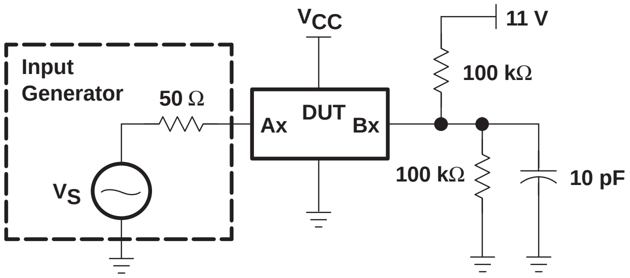

Input
Generator
V_S
50 Ω
V_{CC}
DUT
Ax
Bx
11 V
100 kΩ
100 kΩ
10 pF

Figure 1. Device Test Setup

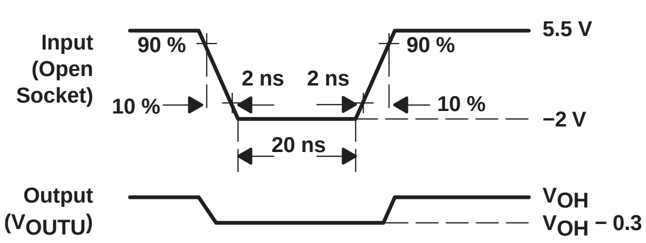
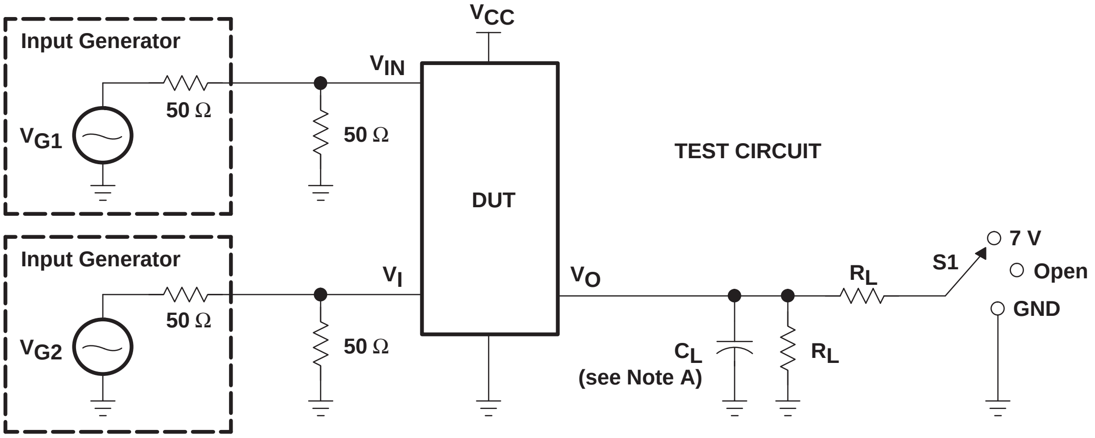
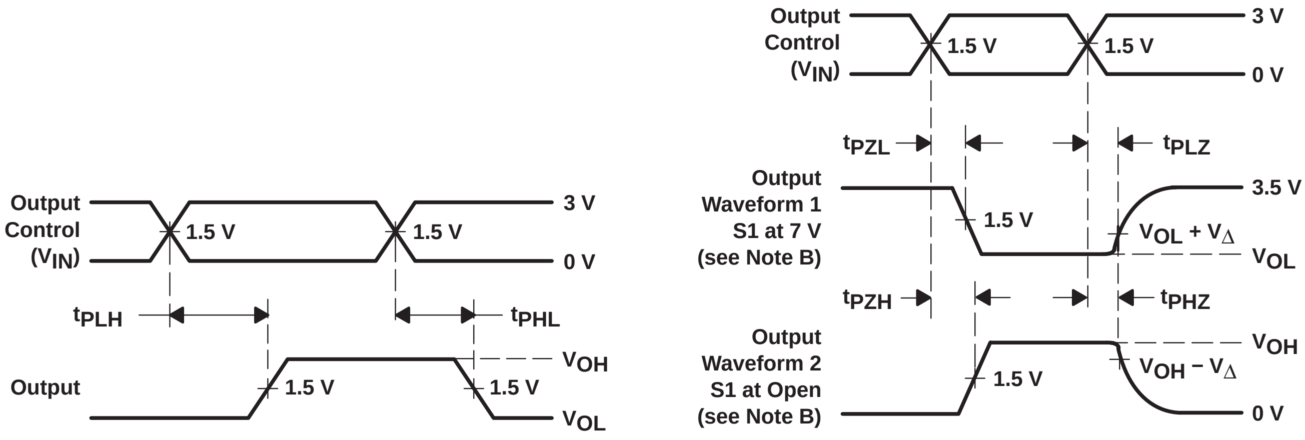

Input
(Open
Socket)
90 %
90 %
10 %
10 %
2 ns
2 ns
20 ns
5.5 V
−2 V
Output
(V_{OUTU})
V_{OH}
V_{OH} − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

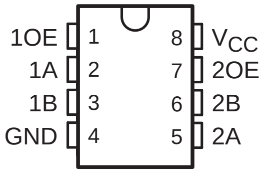
Figure 3. Test Circuit and Voltage Waveforms

SN74CBTD3305C
DUAL FET BUS SWITCH WITH LEVEL SHIFTING
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS126A − SEPTEMBER 2003 − REVISED OCTOBER 2003

- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Integrated Diode to V_{CC} Provides 5-V Input Down To 3.3-V Output Level Shift**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **V_{CC} Operating Range From 4.5 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: USB Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

D OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBTD3305C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. This device features an integrated diode in series with V_{CC} to provide level shifting for 5-V input down to 3.3-V output levels. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBTD3305C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBTD3305C is organized as two 1-bit bus switches with separate output-enable (1OE, 2OE) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When OE is high, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is low, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − D	Tube	SN74CBTD3305CD	CC305C
		Tape and reel	SN74CBTD3305CDR	
	TSSOP − PW	Tube	SN74CBTD3305CPW	CC305C
		Tape and reel	SN74CBTD3305CPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

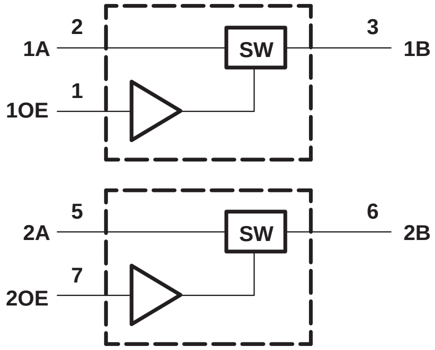
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

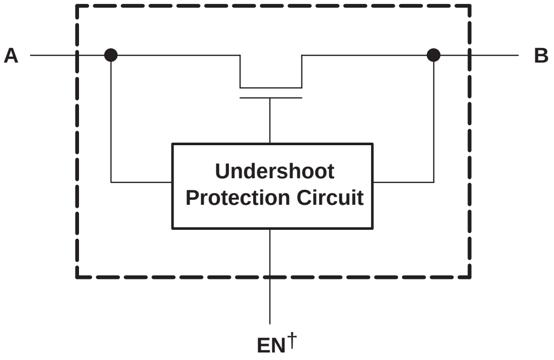
FUNCTION TABLE
(each bus switch)

INPUT OE	INPUT/OUTPUT A	FUNCTION
H	B	A port = B port
L	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . −0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$) . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$) . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . ±128 mA
Continuous current through V_{CC} or GND terminals . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5): D package . . . . 97°C/W
PW package . . . . 149°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 6 and 7)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTES:
6. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
7. In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
V_{OH}		See Figures 4 and 5						
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	µA
I_{OZ}[‡]		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	µA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			1.5	mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				3.5		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		12.5		pF
r_{on}[¶]		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	Ω
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		8	20	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	
t_{pd}[#]	A or B	B or A		0.15	ns
t_{en}	OE	A or B	1.5	4.7	ns
t_{dis}	OE	A or B	1.5	5.3	ns

[#] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V, Switch OFF, V_{IN} = V_{CC} or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

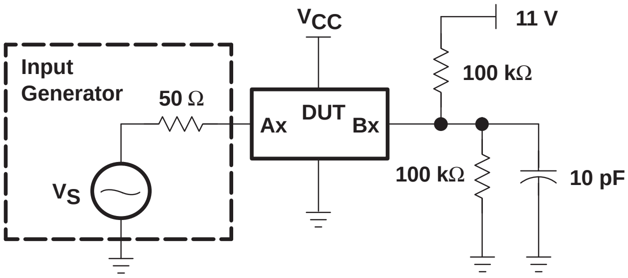

VCC
11 V
Input
Generator
50 Ω
DUT
Ax
Bx
100 kΩ
100 kΩ
10 pF
VS

Figure 1. Device Test Setup

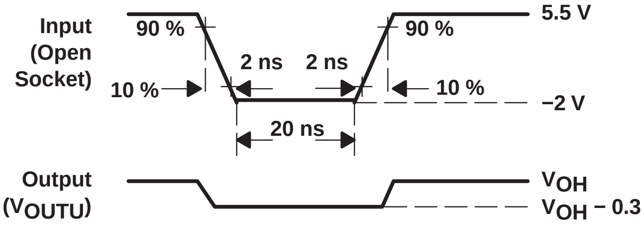
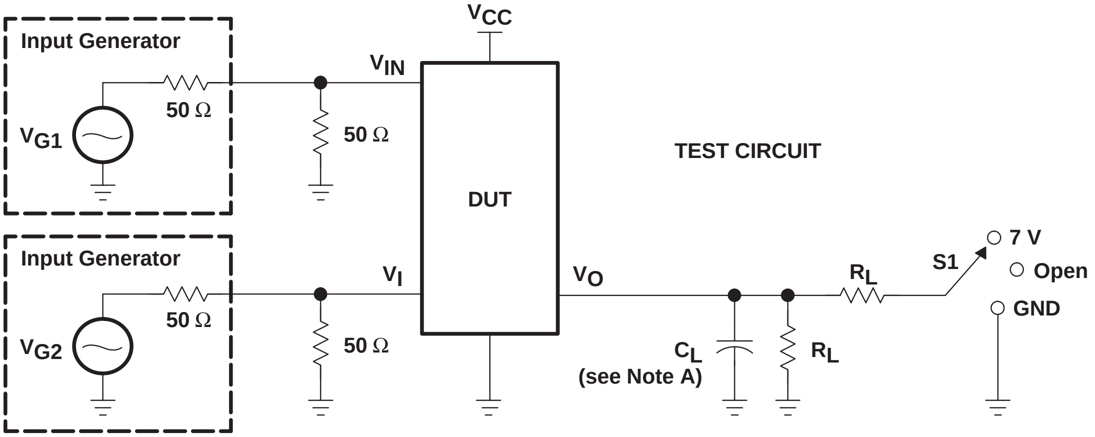
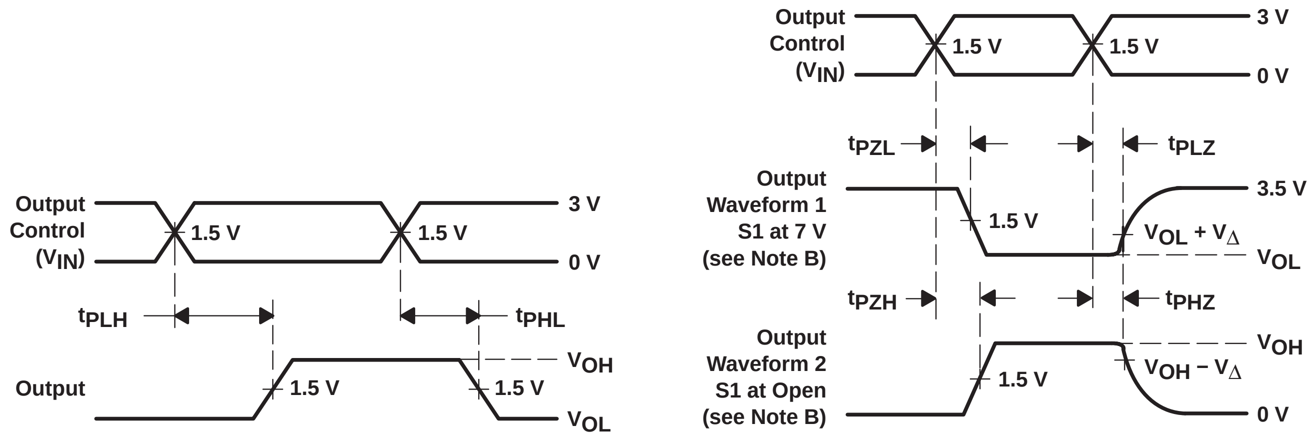

Input
(Open
Socket)
90 %
90 %
5.5 V
2 ns
2 ns
10 %
10 %
−2 V
20 ns
Output
(VOUTU)
VOH
VOH − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION FOR LEVEL SHIFTER


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V	Open	500 Ω	V_{CC} or GND	50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V	7 V	500 Ω	GND	50 pF	0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V	Open	500 Ω	V_{CC}	50 pF	0.3 V


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

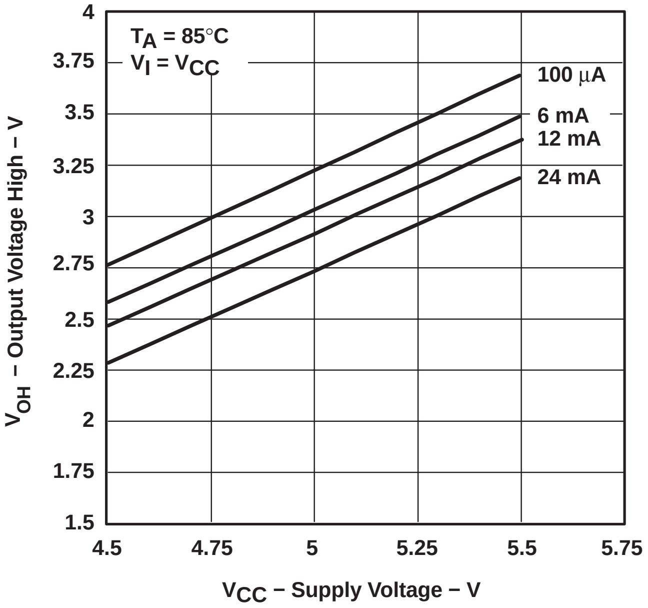
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

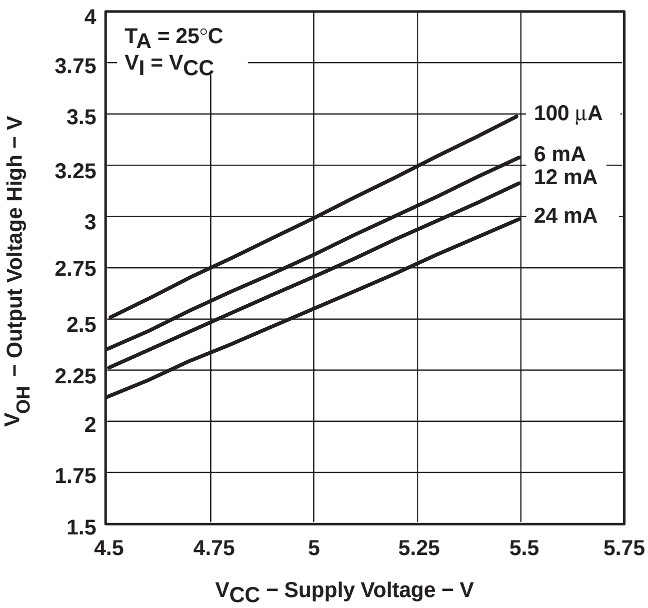
Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE



OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE



OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE

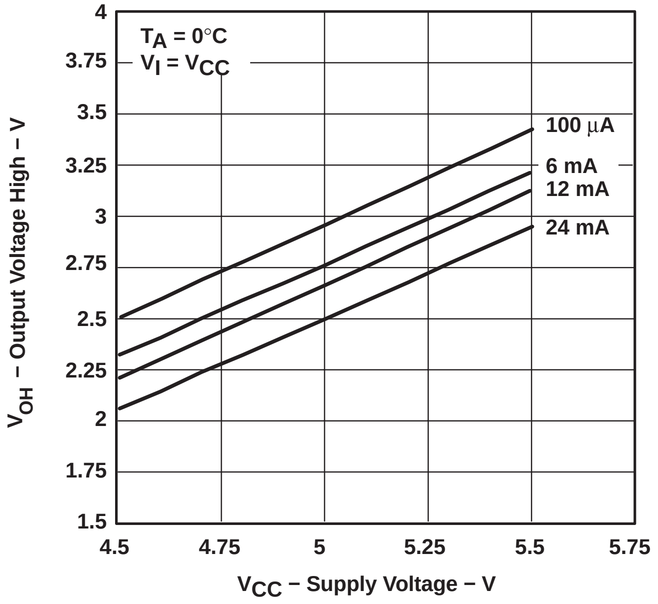


Figure 4. V_{OH} Values

TYPICAL CHARACTERISTICS (continued)

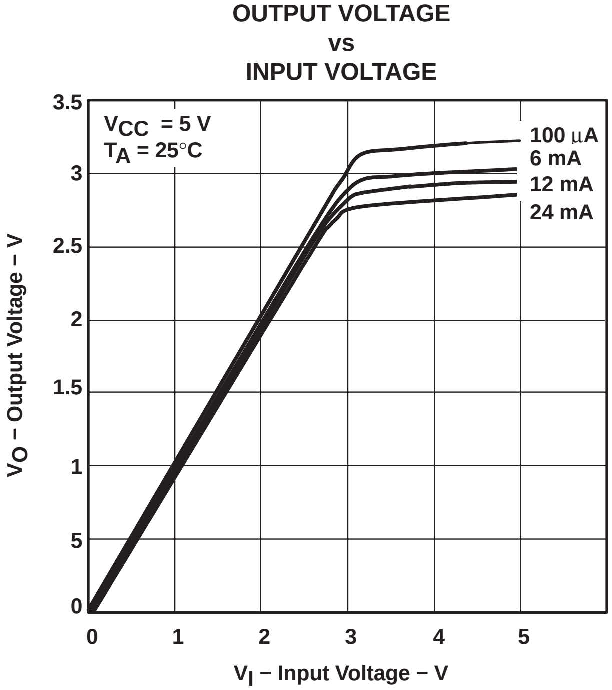


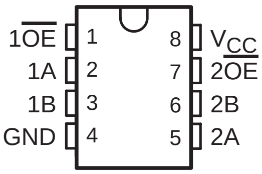
Figure 5. Data Output Voltage vs Data Input Voltage

SN74CBT3306C
DUAL FET BUS SWITCH
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS127A − SEPTEMBER 2003 − REVISED OCTOBER 2003

- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: USB Interface, Bus Isolation, Low-Distortion Signal Gating**

D OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBT3306C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3306C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3306C is organized as two 1-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When $\overline{OE}$ is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 1-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − D	Tube	SN74CBT3306CD	CU306C
		Tape and reel	SN74CBT3306CDR	
	TSSOP − PW	Tube	SN74CBT3306CPW	CU306C
		Tape and reel	SN74CBT3306CPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TEXAS INSTRUMENTS

description/ordering information (continued)

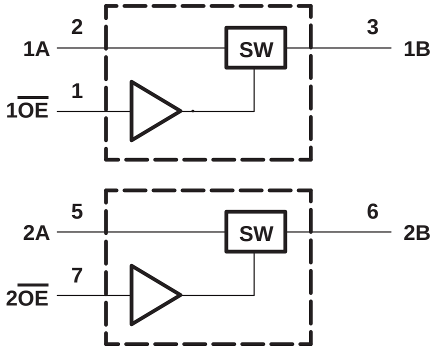
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

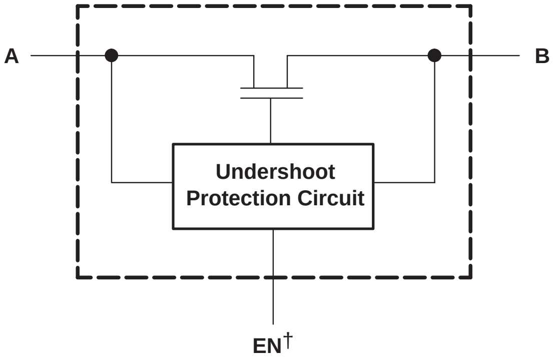
FUNCTION TABLE
(each bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): D package	97°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_{OZ}‡		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	μA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				3.5		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		12.5		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}#	A or B	B or A		0.24		0.15	ns
t_{en}	$\overline{OE}$	A or B		4.6	1.5	4.2	ns
t_{dis}	$\overline{OE}$	A or B		4.3	1.5	4.3	ns

# The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V,	Switch OFF,	V_{IN} = V_{CC} or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

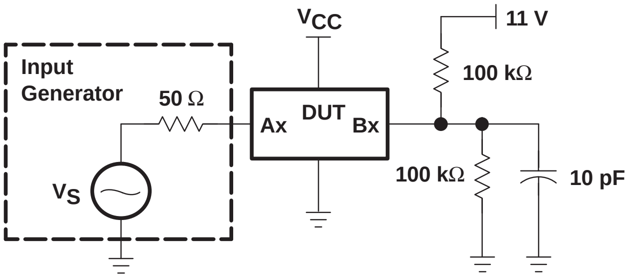

V_CC
11 V
Input
Generator
50 Ω
DUT
Ax
Bx
100 kΩ
100 kΩ
10 pF
V_S

Figure 1. Device Test Setup

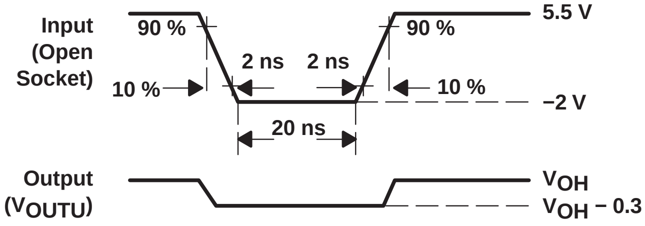
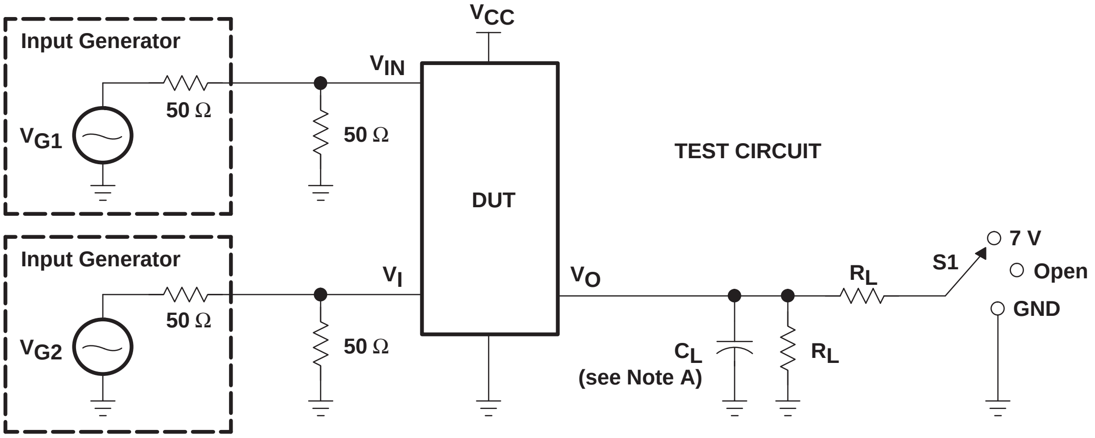
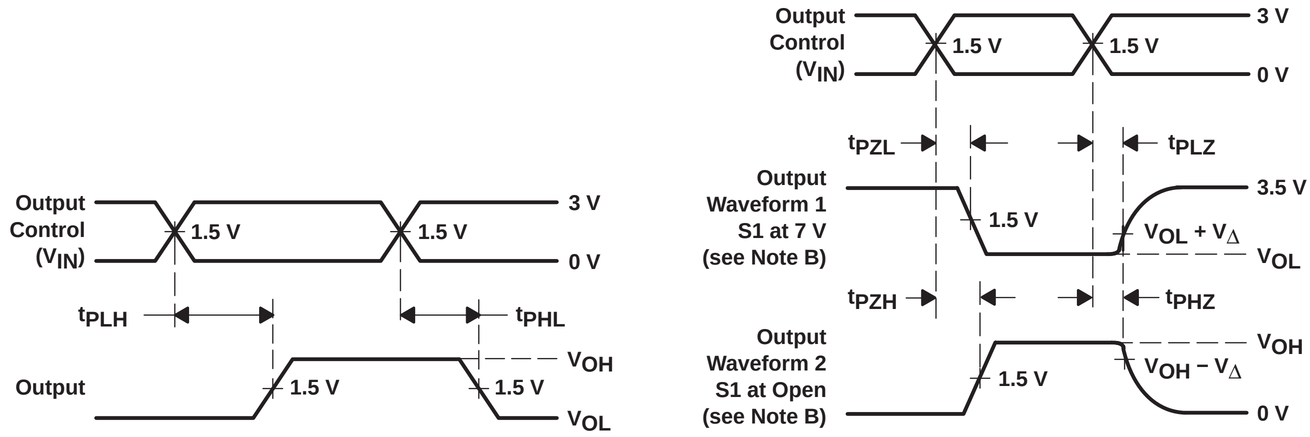

Input
(Open
Socket)
90 %
90 %
5.5 V
2 ns
2 ns
10 %
10 %
−2 V
20 ns
Output
(V_OUTU)
V_OH
V_OH − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

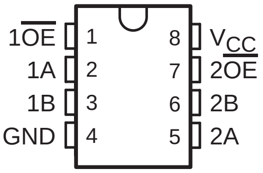
Figure 3. Test Circuit and Voltage Waveforms

SN74CBTD3306C
DUAL FET BUS SWITCH WITH LEVEL SHIFTING
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS128A − SEPTEMBER 2003 − REVISED OCTOBER 2003

- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Integrated Diode to V_{CC} Provides 5-V Input Down To 3.3-V Output Level Shift**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **V_{CC} Operating Range From 4.5 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: USB Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

D OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBTD3306C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. This device features an integrated diode in series with V_{CC} to provide level shifting for 5-V input down to 3.3-V output levels. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBTD3306C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBTD3306C is organized as two 1-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When $\overline{OE}$ is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − D	Tube	SN74CBTD3306CD	CC306C
		Tape and reel	SN74CBTD3306CDR	
	TSSOP − PW	Tube	SN74CBTD3306CPW	CC306C
		Tape and reel	SN74CBTD3306CPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

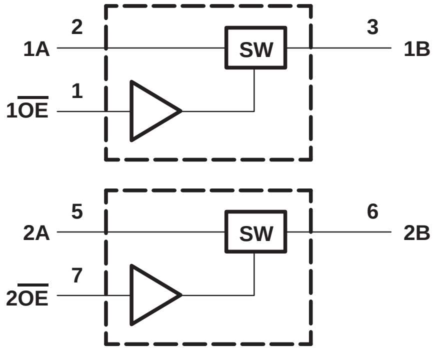
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

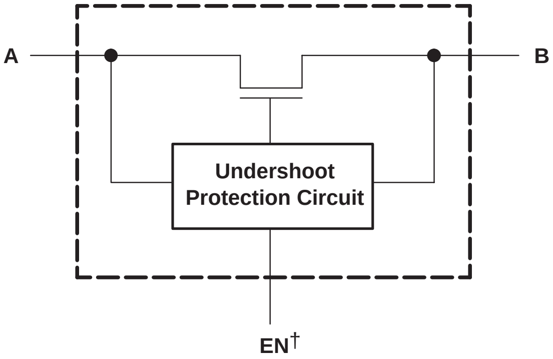
FUNCTION TABLE
(each bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): D package	97°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 6 and 7)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTES: 6. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
7. In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
V_{OH}		See Figures 4 and 5						
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_{OZ}[‡]		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			1.5	mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				3.5		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		12.5		pF
r_{on}[¶]		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	Ω
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		9	20	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	
t_{pd}[#]	A or B	B or A		0.15	ns
t_{en}	$\overline{OE}$	A or B	1.5	4.7	ns
t_{dis}	$\overline{OE}$	A or B	1.5	4.7	ns

[#] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V,	Switch OFF,	$V_{IN} = V_{CC}$ or GND	2	V_{OH}−0.3		V

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

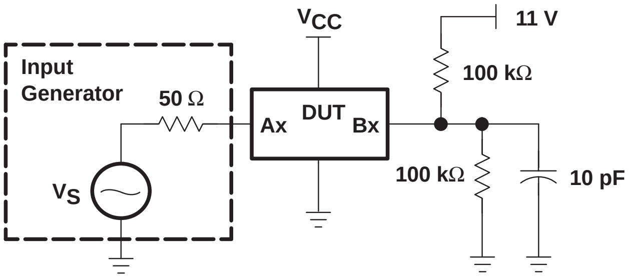

Input
Generator
50 Ω
V_S
V_{CC}
DUT
Ax
Bx
11 V
100 kΩ
100 kΩ
10 pF

Figure 1. Device Test Setup

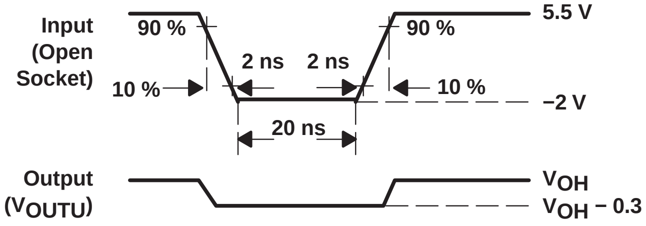
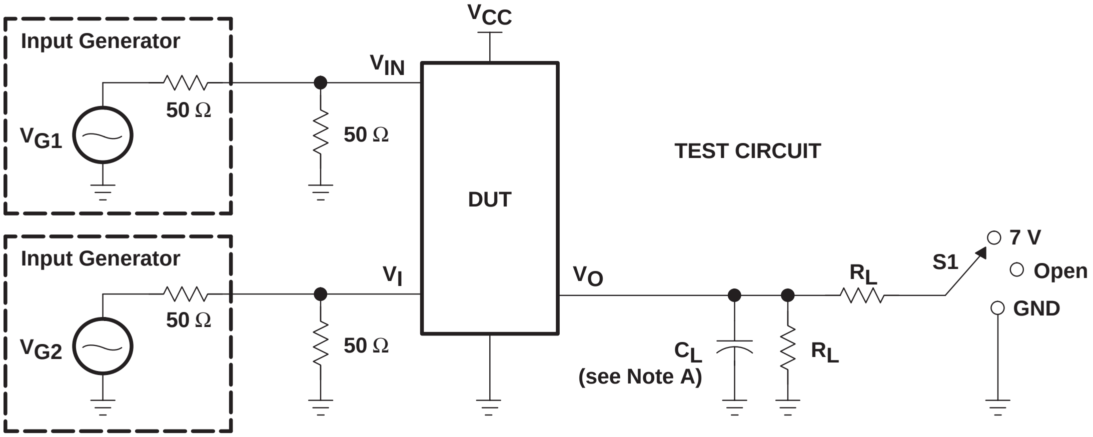
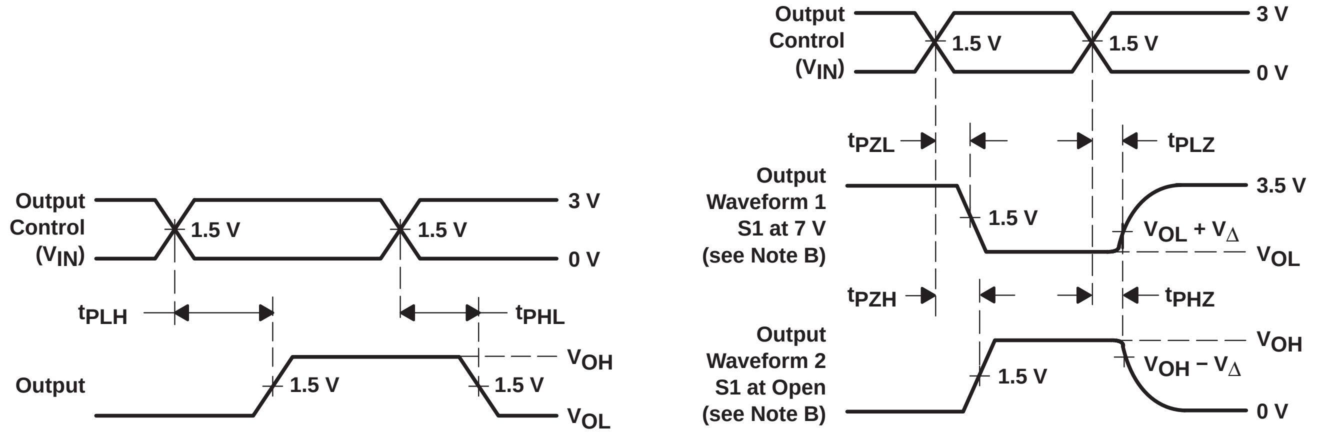

Input
(Open
Socket)
90 %
90 %
10 %
10 %
2 ns
2 ns
20 ns
5.5 V
−2 V
Output
(V_{OUTU})
V_{OH}
V_{OH} − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION FOR LEVEL SHIFTER


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V	Open	500 Ω	V_{CC} or GND	50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V	7 V	500 Ω	GND	50 pF	0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V	Open	500 Ω	V_{CC}	50 pF	0.3 V


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

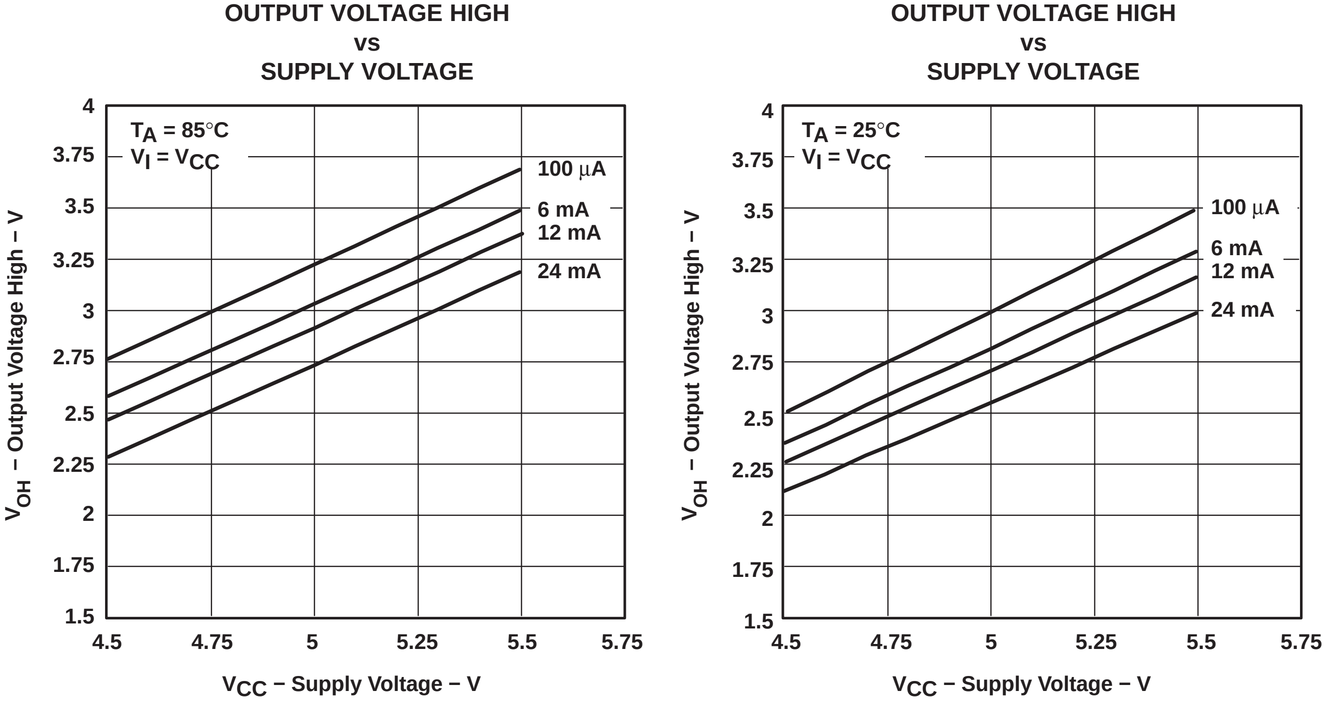
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



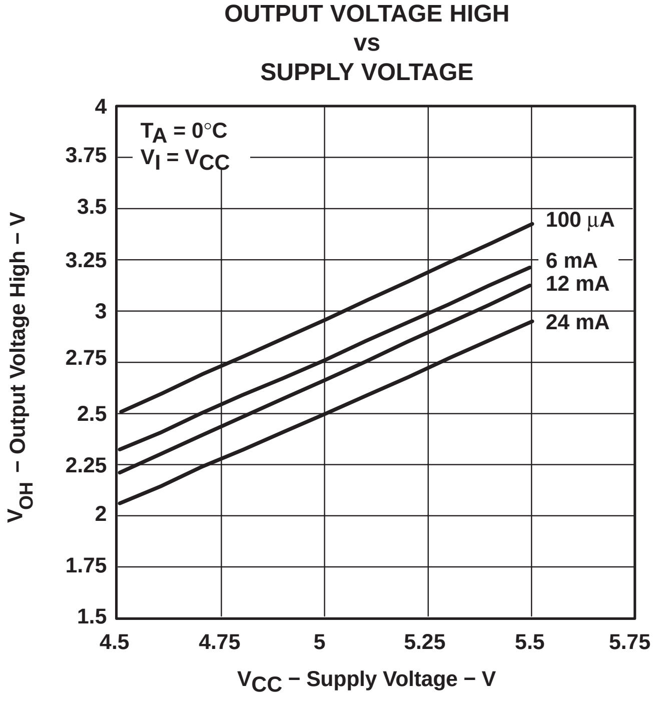


Figure 4. V_{OH} Values

TYPICAL CHARACTERISTICS (continued)

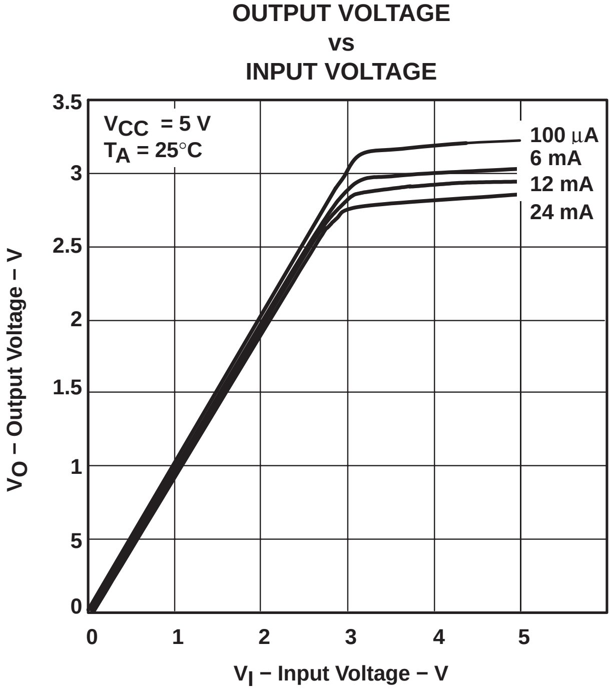


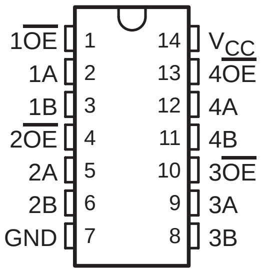
Figure 5. Data Output Voltage vs Data Input Voltage

SN74CBT3125C
QUADRUPLE FET BUS SWITCH
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS122A − JULY 2003 − REVISED OCTOBER 2003

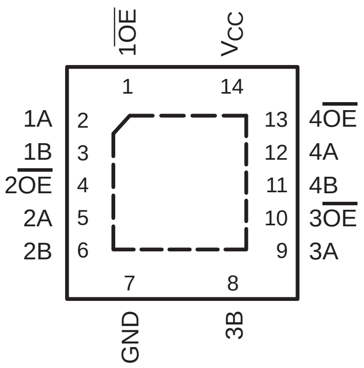
- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: USB Interface, Bus Isolation, Low-Distortion Signal Gating**

D, DB, DGV, OR PW PACKAGE
(TOP VIEW)



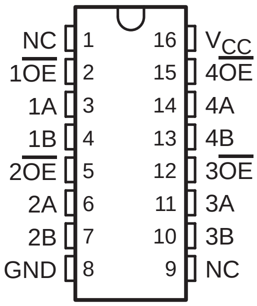
$1\overline{OE}$ 1
1A 2
1B 3
$2\overline{OE}$ 4
2A 5
2B 6
GND 7
8 3B
9 3A
10 $3\overline{OE}$
11 4B
12 4A
13 $4\overline{OE}$
14 V_{CC}

RGY PACKAGE
(TOP VIEW)



$1\overline{OE}$
V_{CC}
1
14
1A 2
1B 3
$2\overline{OE}$ 4
2A 5
2B 6
13 $4\overline{OE}$
12 4A
11 4B
10 $3\overline{OE}$
9 3A
7
8
GND
3B

DBQ PACKAGE
(TOP VIEW)



NC 1
$1\overline{OE}$ 2
1A 3
1B 4
$2\overline{OE}$ 5
2A 6
2B 7
GND 8
9 NC
10 3B
11 3A
12 $3\overline{OE}$
13 4B
14 4A
15 $4\overline{OE}$
16 V_{CC}

NC − No internal connection

description/ordering information

The SN74CBT3125C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3125C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3125C is organized as four 1-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$) inputs. It can be used as four 1-bit bus switches or as one 4-bit bus switch. When $\overline{OE}$ is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 1-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

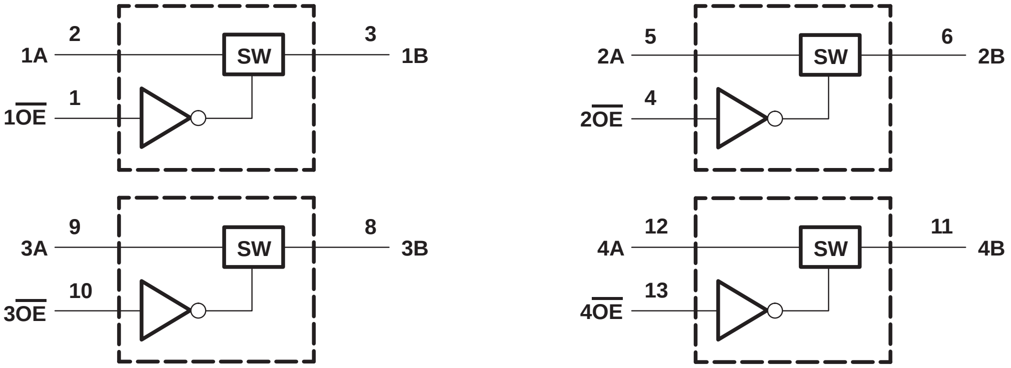
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBT3125CRGYR	CU125C
	SOIC − D	Tube	SN74CBT3125CD	CBT3125C
		Tape and reel	SN74CBT3125CDR	
	SSOP − DB	Tube	SN74CBT3125CDB	CU125C
		Tape and reel	SN74CBT3125CDBR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3125CDBQR	CU125C
	TSSOP − PW	Tube	SN74CBT3125CPW	CU125C
		Tape and reel	SN74CBT3125CPWR	
	TVSOP − DGV	Tape and reel	SN74CBT3125CDGVR	CU125C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each bus switch)

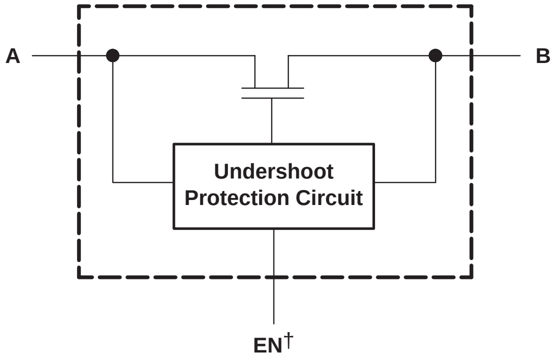
INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, PW, and RGY packages.

simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . −0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$) . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$) . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . ±128 mA
Continuous current through V_{CC} or GND terminals . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5): D package . . . . 86°C/W
(see Note 5): DB package . . . . 96°C/W
(see Note 5): DBQ package . . . . 90°C/W
(see Note 5): DGV package . . . . 127°C/W
(see Note 5): PW package . . . . 113°C/W
(see Note 6): RGY package . . . . 47°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_{OZ}[‡]		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	μA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				3		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		12.5		pF
r_{on}[¶]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[#]	A or B	B or A		0.24		0.15	ns
t_{en}	$\overline{OE}$	A or B		4.4	1.5	4	ns
t_{dis}	$\overline{OE}$	A or B		4.4	1.5	4.4	ns

[#] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V, Switch OFF, V_{IN} = V_{CC} or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

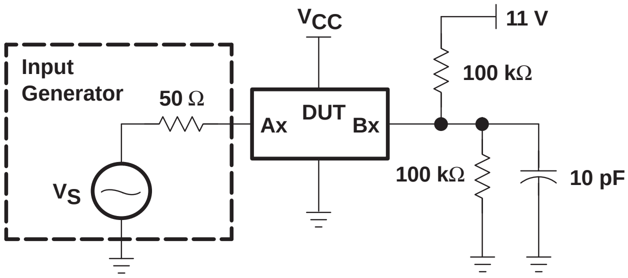

VCC
11 V
Input
Generator
50 Ω
DUT
Ax
Bx
100 kΩ
100 kΩ
10 pF
VS

Figure 1. Device Test Setup

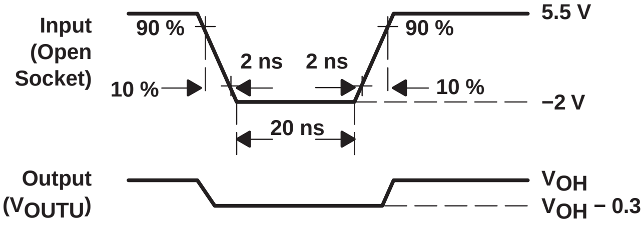
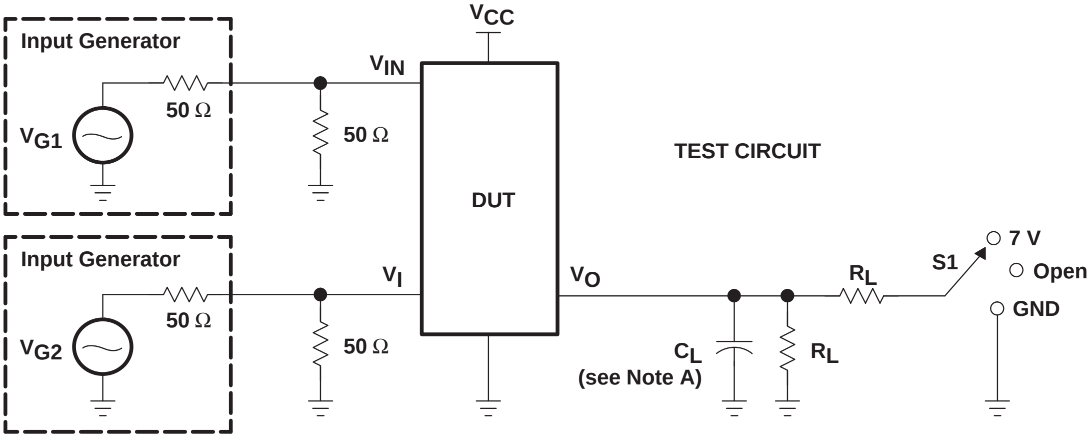
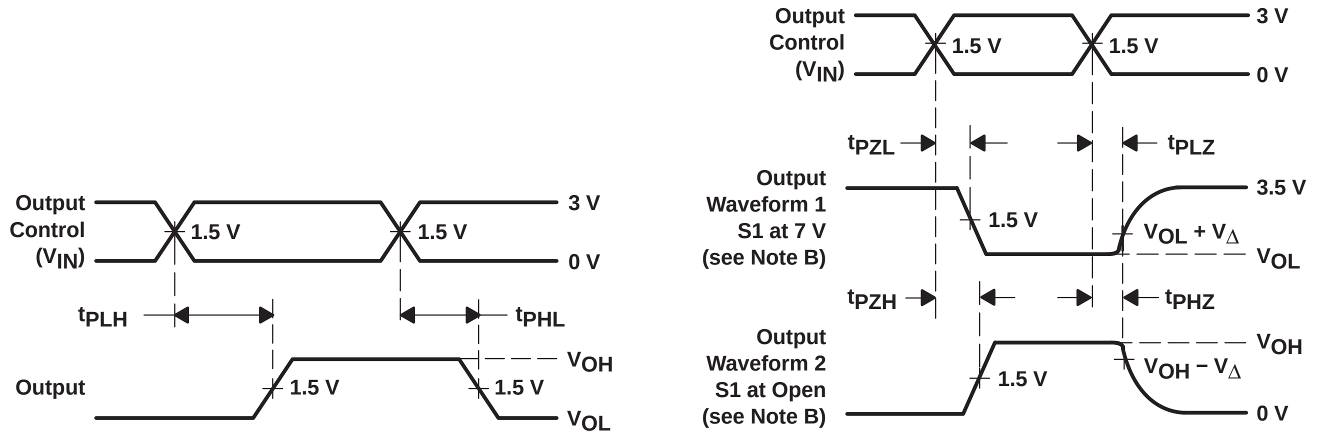

Input
(Open
Socket)
90 %
90 %
5.5 V
2 ns
2 ns
10 %
10 %
−2 V
20 ns
Output
(VOUTU)
VOH
VOH − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION


V_{CC}
Input Generator
V_{IN}
50 Ω
V_{G1}
50 Ω
DUT
TEST CIRCUIT
Input Generator
V_I
V_O
50 Ω
V_{G2}
50 Ω
R_L
S1
7 V
Open
GND
C_L
(see Note A)
R_L

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

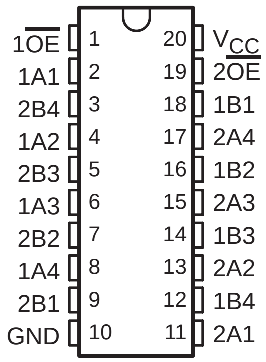
Figure 3. Test Circuit and Voltage Waveforms

SN74CBT3244C
8-BIT FET BUS SWITCH
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

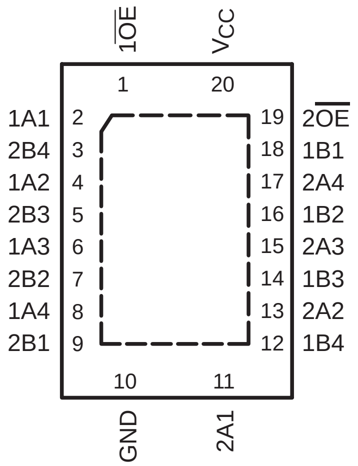
SCDS130A − SEPTEMBER 2003 − REVISED OCTOBER 2003

- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: USB Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBT3244C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3244C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3244C is organized as two 4-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. It can be used as two 4-bit bus switches or as one 8-bit bus switch. When $\overline{OE}$ is low, the associated 4-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 4-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

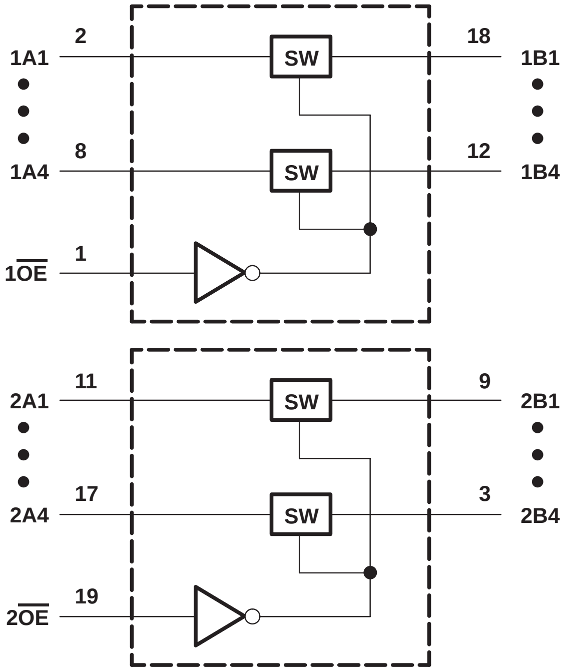
T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBT3244CRGYR	CU244C
	SOIC − DW	Tube	SN74CBT3244CDW	CBT3244C
		Tape and reel	SN74CBT3244CDWR	
	SSOP − DB	Tube	SN74CBT3244CDB	CU244C
		Tape and reel	SN74CBT3244CDBR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3244CDBQR	CBT3244C
	TSSOP − PW	Tube	SN74CBT3244CPW	CU244C
		Tape and reel	SN74CBT3244CPWR	
	TVSOP − DGV	Tape and reel	SN74CBT3244CDGVR	CU244C

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

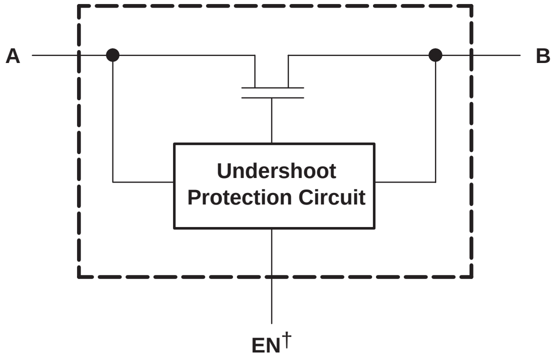
FUNCTION TABLE
(each 4-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)


1A1
2
SW
18
1B1
1A4
8
SW
12
1B4
1OE
1
2A1
11
SW
9
2B1
2A4
17
SW
3
2B4
2OE
19

simplified schematic, each FET switch (SW)


A
B
Undershoot
Protection Circuit
EN†

† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DB package	70°C/W
(see Note 5): DBQ package	68°C/W
(see Note 5): DGV package	92°C/W
(see Note 5): DW package	58°C/W
(see Note 5): PW package	83°C/W
(see Note 6): RGY package	37°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_{OZ}‡		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	μA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				4		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		14		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}#	A or B	B or A		0.24		0.15	ns
t_{en}	$\overline{OE}$	A or B		5.2	1.5	4.8	ns
t_{dis}	$\overline{OE}$	A or B		5.1	1.5	5.7	ns

# The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V, Switch OFF, V_{IN} = V_{CC} or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

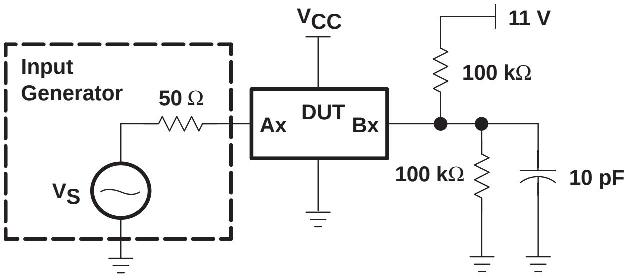

VCC
11 V
Input
Generator
50 Ω
100 kΩ
Ax
DUT
Bx
100 kΩ
10 pF
VS

Figure 1. Device Test Setup

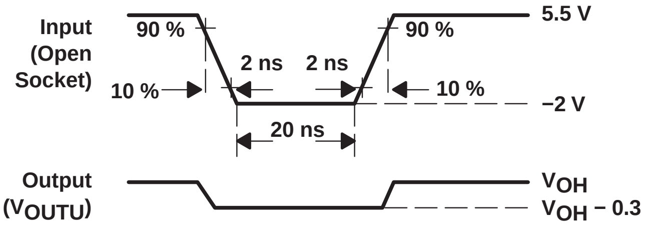
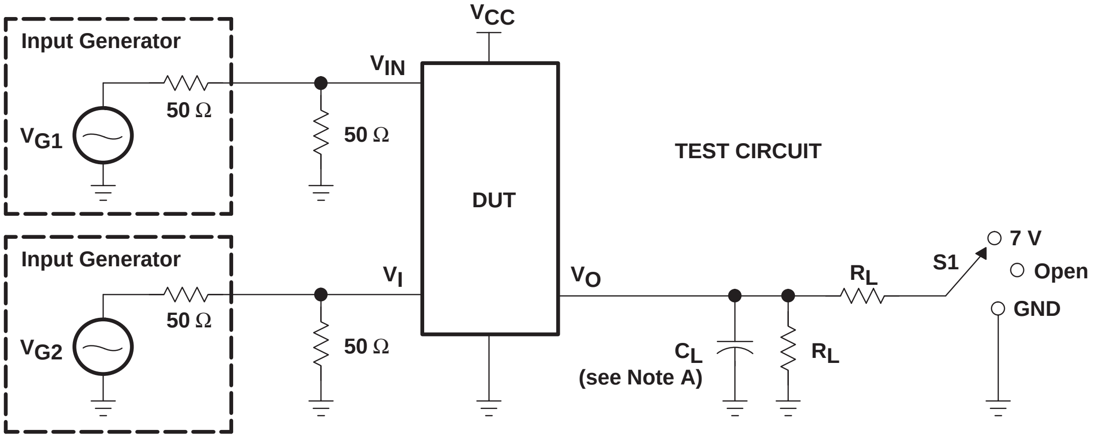
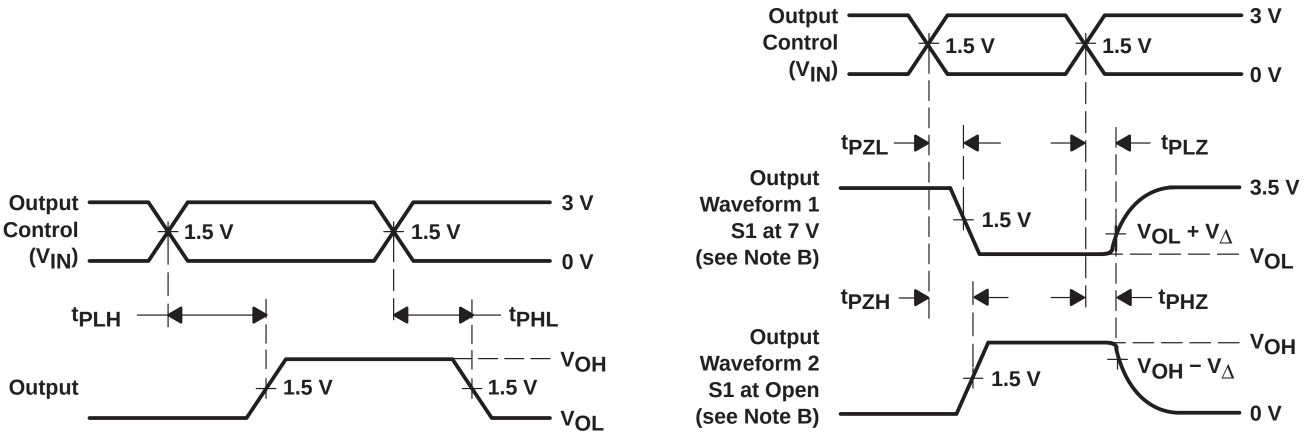

Input
(Open
Socket)
90 %
90 %
5.5 V
2 ns
2 ns
10 %
10 %
−2 V
20 ns
Output
(VOUTU)
VOH
VOH − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

SN74CBT3245C
8-BIT FET BUS SWITCH
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS131A − SEPTEMBER 2003 − REVISED OCTOBER 2003

- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
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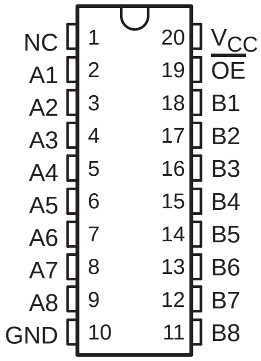
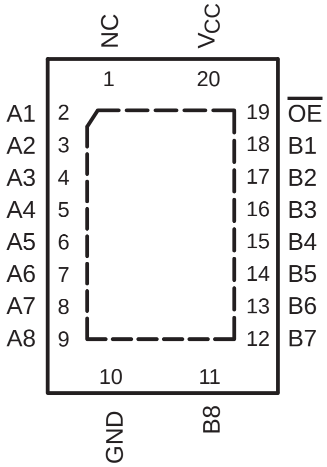
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: USB Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

RGY PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The SN74CBT3245C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3245C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3245C is organized as an 8-bit bus switch with a single output-enable ($\overline{\text{OE}}$) input. When $\overline{\text{OE}}$ is low, the bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{\text{OE}}$ is high, the bus switch is OFF, and the high-impedance state exists between the A and B ports.

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description/ordering information (continued)

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

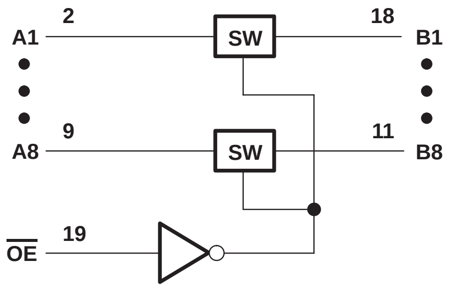
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBT3245CRGYR	CU245C
	SOIC − DW	Tube	SN74CBT3245CDW	CBT3245C
		Tape and reel	SN74CBT3245CDWR	
	SSOP − DB	Tube	SN74CBT3245CDB	CU245C
		Tape and reel	SN74CBT3245CDBR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3245CDBQR	CBT3245C
	TSSOP − PW	Tube	SN74CBT3245CPW	CU245C
		Tape and reel	SN74CBT3245CPWR	
	TVSOP − DGV	Tape and reel	SN74CBT3245CDGVR	CU245C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

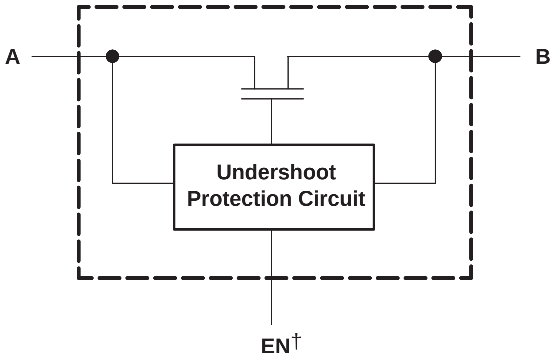
FUNCTION TABLE

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DB package	70°C/W
(see Note 5):	DBQ package	68°C/W
(see Note 5):	DGV package	92°C/W
(see Note 5):	DW package	58°C/W
(see Note 5):	PW package	83°C/W
(see Note 6):	RGY package	37°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_{OZ}‡		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	μA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				4		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		14		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}#	A or B	B or A		0.24		0.15	ns
t_{en}	$\overline{OE}$	A or B		5.1	1.5	4.7	ns
t_{dis}	$\overline{OE}$	A or B		4.9	1.5	5.3	ns

# The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V, Switch OFF, V_{IN} = V_{CC} or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

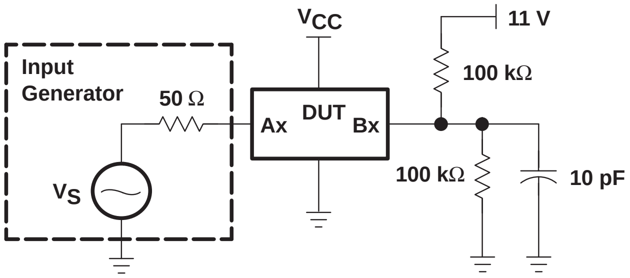

Input
Generator
50 Ω
V_S
V_{CC}
DUT
Ax
Bx
11 V
100 kΩ
100 kΩ
10 pF

Figure 1. Device Test Setup

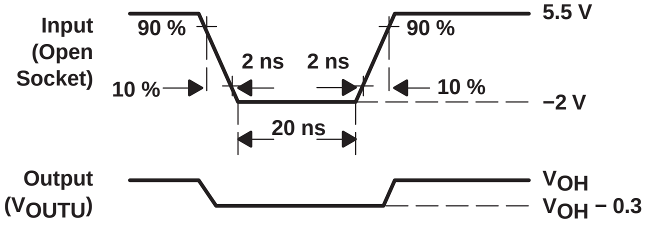
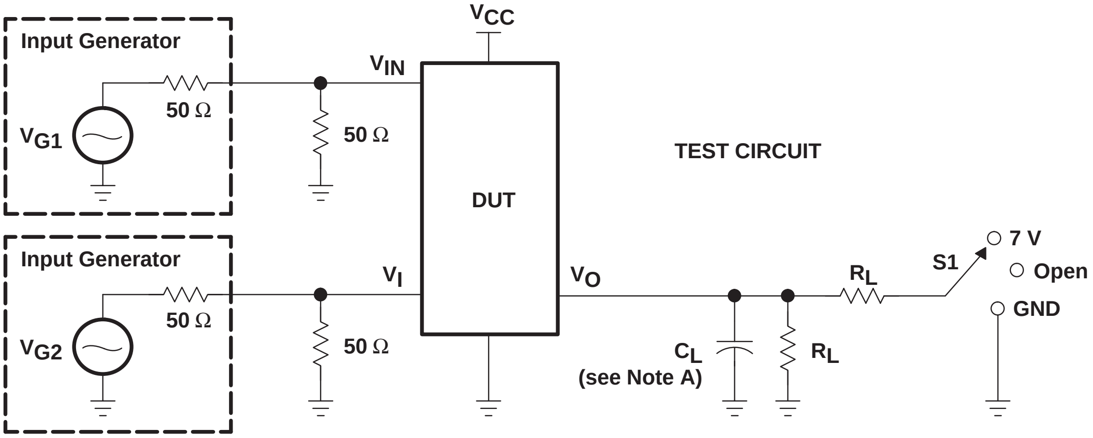
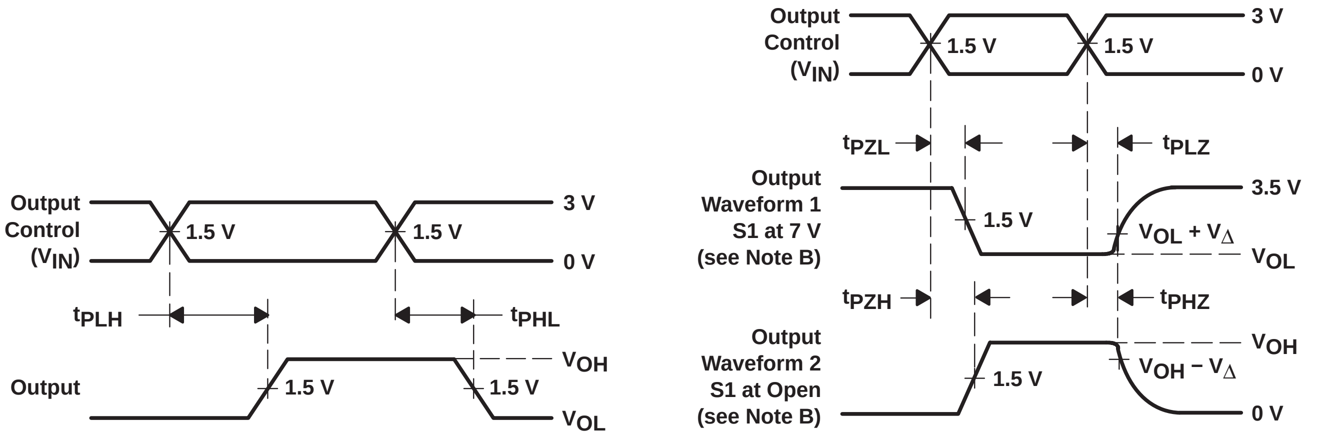

Input
(Open
Socket)
90 %
90 %
5.5 V
2 ns
2 ns
10 %
10 %
−2 V
20 ns
Output
(V_{OUTU})
V_{OH}
V_{OH} − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_{I}
50 Ω
V_{O}
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

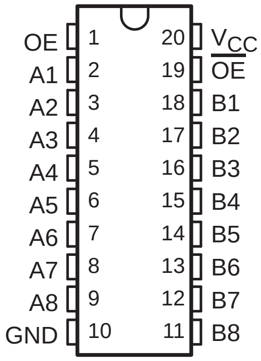
Figure 3. Test Circuit and Voltage Waveforms

SN74CBT3345C
8-BIT FET BUS SWITCH
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

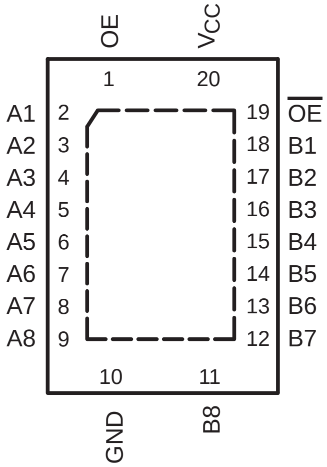
SCDS129A − SEPTEMBER 2003 − REVISED OCTOBER 2003

- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: USB Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBT3345C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3345C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3345C is organized as an 8-bit bus switch with two output-enable (OE, $\overline{\text{OE}}$) inputs. When OE is high or $\overline{\text{OE}}$ is low, the bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is low and $\overline{\text{OE}}$ is high, the bus switch is OFF and the high-impedance state exists between the A and B ports.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor, and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

ORDERING INFORMATION

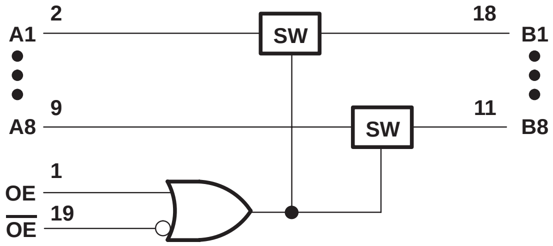
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBT3345CRGYR	CU345C
	SOIC − DW	Tube	SN74CBT3345CDW	CBT3345C
		Tape and reel	SN74CBT3345CDWR	
	SSOP − DB	Tube	SN74CBT3345CDB	CU345C
		Tape and reel	SN74CBT3345CDBR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3345CDBQR	CBT3345C
	TSSOP − PW	Tube	SN74CBT3345CPW	CU345C
		Tape and reel	SN74CBT3345CPWR	
	TVSOP − DGV	Tape and reel	SN74CBT3345CDGVR	CU345C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

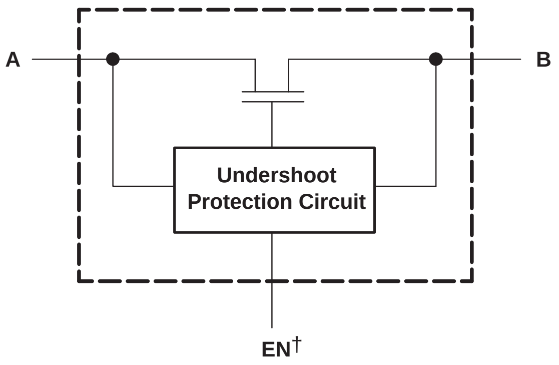
FUNCTION TABLE

INPUTS		INPUT/OUTPUT A	FUNCTION
OE	$\overline{OE}$		
H	X	B	A port = B port
X	L	B	A port = B port
L	H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DB package	70°C/W
(see Note 5): DBQ package	68°C/W
(see Note 5): DGV package	92°C/W
(see Note 5): DW package	58°C/W
(see Note 5): PW package	83°C/W
(see Note 6): RGY package	37°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	µA
I_{OZ}‡		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	µA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	µA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				4		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		14		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}#	A or B	B or A		0.24		0.15	ns
t_{en}	$\overline{\text{OE}}$ or OE	A or B		5.3	1.5	4.9	ns
t_{dis}	$\overline{\text{OE}}$ or OE	A or B		5.8	1.5	5.7	ns

# The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V,	Switch OFF,	V_{IN} = V_{CC} or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

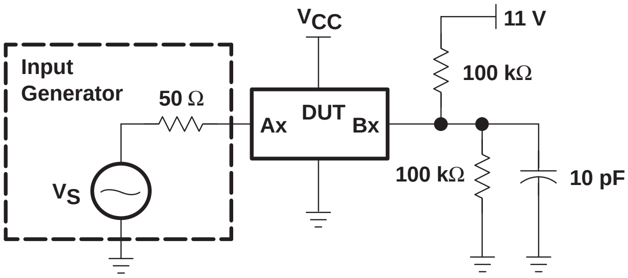

Input
Generator
50 Ω
V_S
V_{CC}
DUT
Ax
Bx
11 V
100 kΩ
100 kΩ
10 pF

Figure 1. Device Test Setup

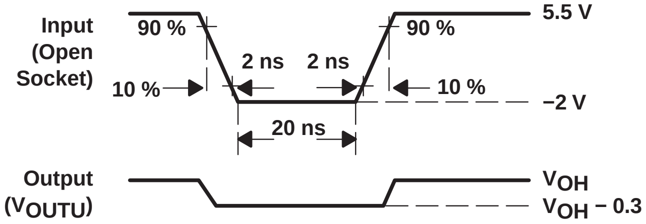
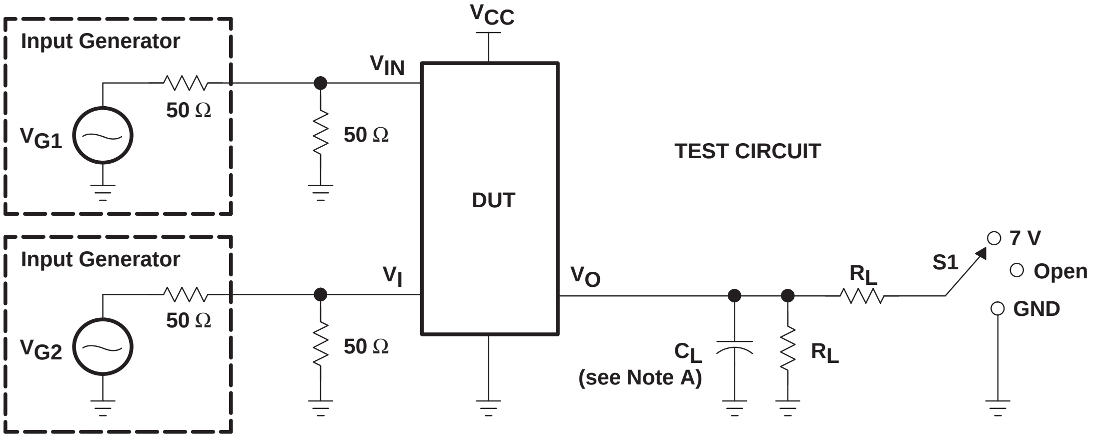
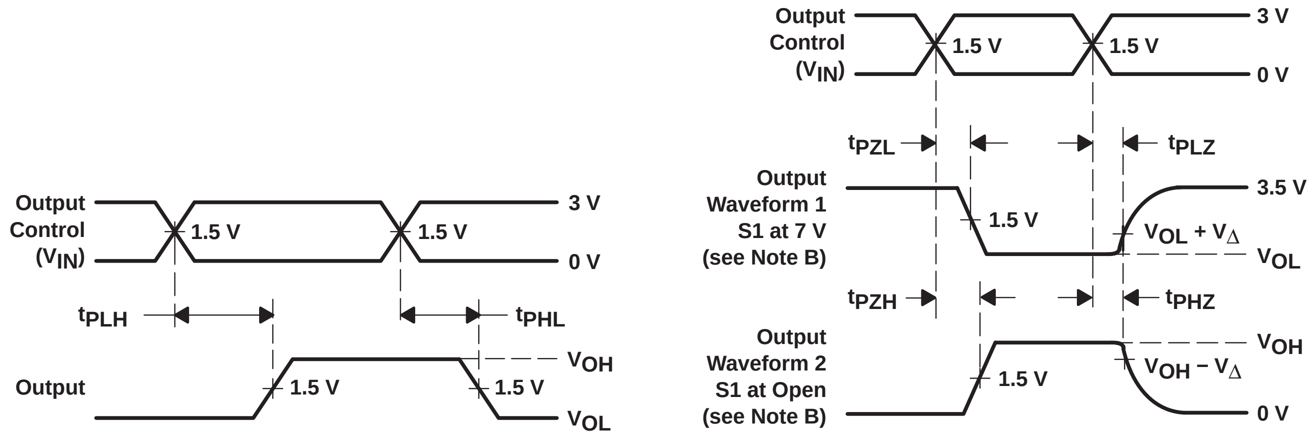

Input
(Open
Socket)
90 %
90 %
2 ns
2 ns
10 %
10 %
20 ns
5.5 V
−2 V
Output
(V_{OUTU})
V_{OH}
V_{OH} − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION


V_{CC}
Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
TEST CIRCUIT
DUT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
R_L
S1
7 V
Open
GND
C_L
(see Note A)
R_L

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

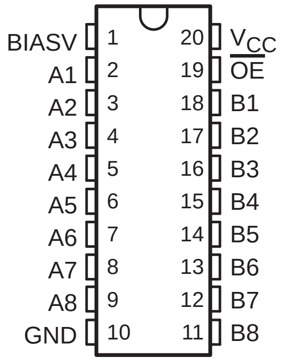
Figure 3. Test Circuit and Voltage Waveforms

SN74CBT6845C
8-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

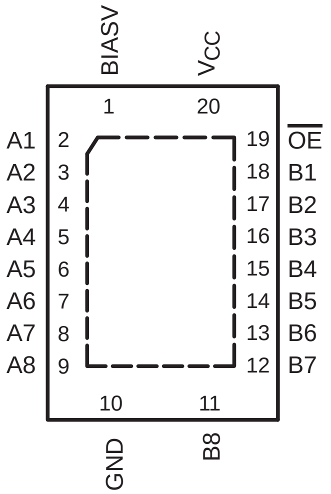
SCDS140 − OCTOBER 2003

- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot-Plugging**
- **Supports PCI Hot Plug**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 µA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBT6845C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT6845C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The SN74CBT6845C is an 8-bit bus switch with a single output-enable ($\overline{\text{OE}}$) input. When $\overline{\text{OE}}$ is low, the 8-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{\text{OE}}$ is high, the 8-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. The B port is precharged to BIASV through the equivalent of a 10-kΩ resistor when $\overline{\text{OE}}$ is high, or if the device is powered down (V_{CC} = 0 V).

During insertion (or removal) of a card into (or from) an active bus, the card's output voltage may be close to GND. When the connector pins make contact, the card's parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method will ensure that any glitch produced by insertion (or removal) of the card will not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

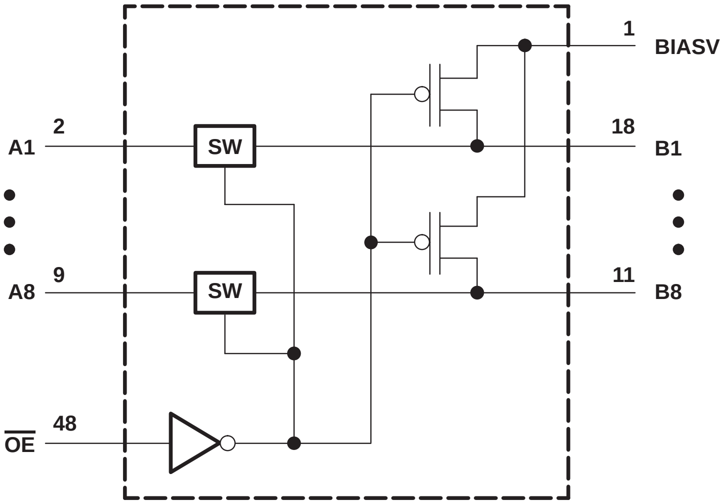
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBT6845CRGYR	CT6845C
	SOIC − DW	Tube	SN74CBT6845CDW	CBT6845C
		Tape and reel	SN74CBT6845CDWR	
	SSOP − DB	Tube	SN74CBT6845CDB	CT6845C
		Tape and reel	SN74CBT6845CDBR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT6845CDBQR	CBT6845C
	TSSOP − PW	Tube	SN74CBT6845CPW	CT6845C
		Tape and reel	SN74CBT6845CPWR	
	TVSOP − DGV	Tape and reel	SN74CBT6845CDGVR	CT6845C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

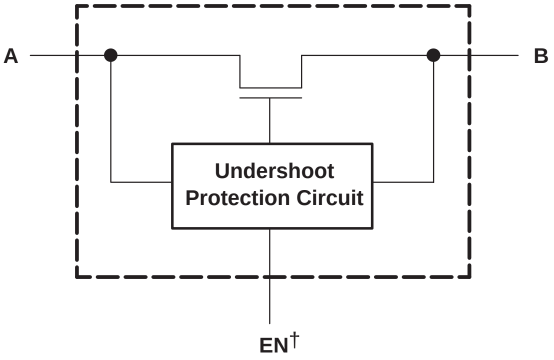
FUNCTION TABLE

INPUT $\overline{\text{OE}}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect B port = BIASV

logic diagram (positive logic)


1
BIASV
2
A1
SW
18
B1
9
A8
SW
11
B8
48
OE

simplified schematic, each FET switch (SW)


A
B
Undershoot
Protection Circuit
EN†

† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Bias supply voltage range, BIASV . . . . −0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . −0.5 V to 7 V
Control input clamp current, I_{IK} (V_{IN} < 0) . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O}$ < 0) . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . ±128 mA
Continuous current through V_{CC} or GND terminals . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DB package . . . . 70°C/W
(see Note 5): DBQ package . . . . 68°C/W
(see Note 5): DGV package . . . . 92°C/W
(see Note 5): DW package . . . . 58°C/W
(see Note 5): PW package . . . . 83°C/W
(see Note 6): RGY package . . . . 37°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIASV	Bias supply voltage	0	V_{CC}	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. BIASV is a supply voltage, not a control input.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
$V_{O(USP)}$‡		V_{CC} = BIASV = 5 V,	I_I = −10 mA, V_{IN} = V_{CC} or GND,	Switch OFF	3			V
V_O	B port	V_{CC} = 0 V,	BIASV = V_X,	I_O = 0	V_X −0.1		V_X	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_O	B port	V_{CC} = 4.5 V,	BIASV = 2.4 V, V_O = 0,	Switch OFF, V_{IN} = V_{CC} or GND		0.25		mA
I_{OZ}§		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	μA
ΔI_{CC}¶	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				4		pF
$C_{io(OFF)}$	A port	$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		13.5		pF
r_{on}#		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ $V_{O(USP)}$ = A-port undershoot static protection.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

¶ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

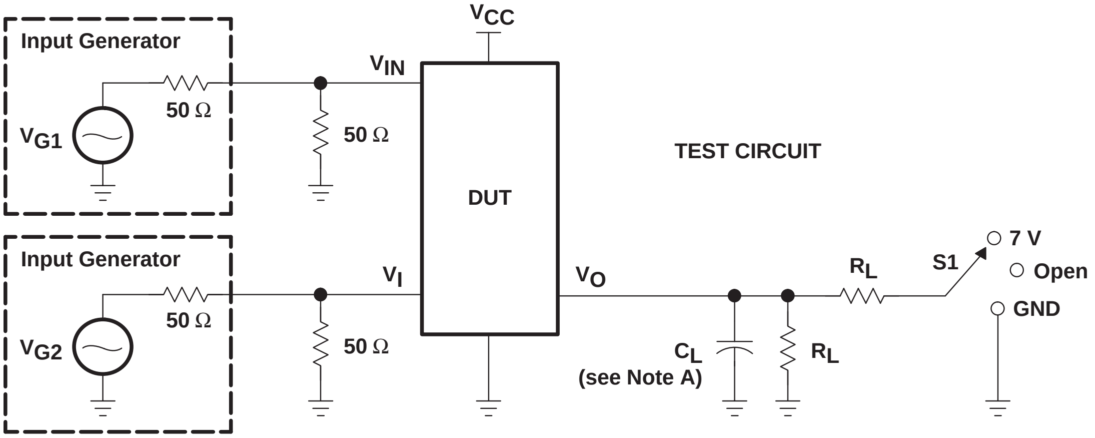
# Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

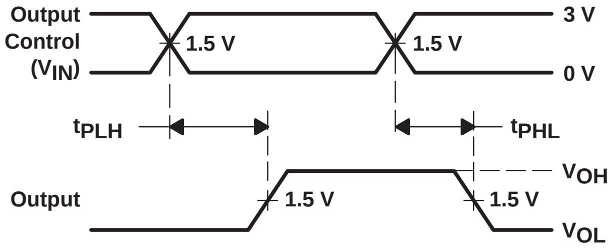
PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}‖		A or B	B or A		0.24		0.15	ns
t_{PZH}	BIASV = GND	$\overline{OE}$	A or B		5.2	1.5	4.8	ns
t_{PZL}	BIASV = 3 V				5.2	1.5	4.8	
t_{PHZ}	BIASV = GND	$\overline{OE}$	A or B		4.9	1.5	5.3	ns
t_{PLZ}	BIASV = 3 V				4.9	1.5	5.3	

‖ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

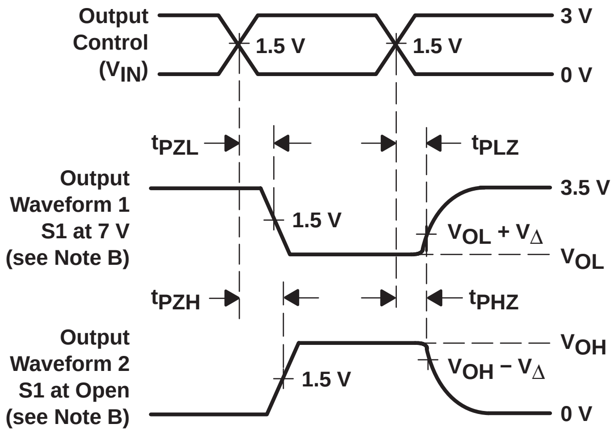
PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

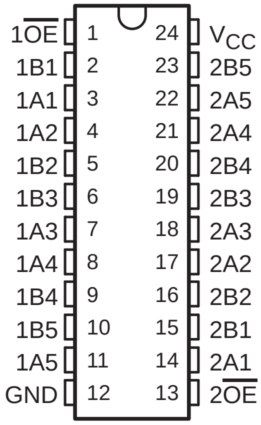
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Test Circuit and Voltage Waveforms

- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBT3384C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3384C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3384C is organized as two 5-bit bus switches with separate output-enable (1$\overline{OE}$, 2$\overline{OE}$) inputs. It can be used as two 5-bit bus switches or as one 10-bit bus switch. When $\overline{OE}$ is low, the associated 5-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 5-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

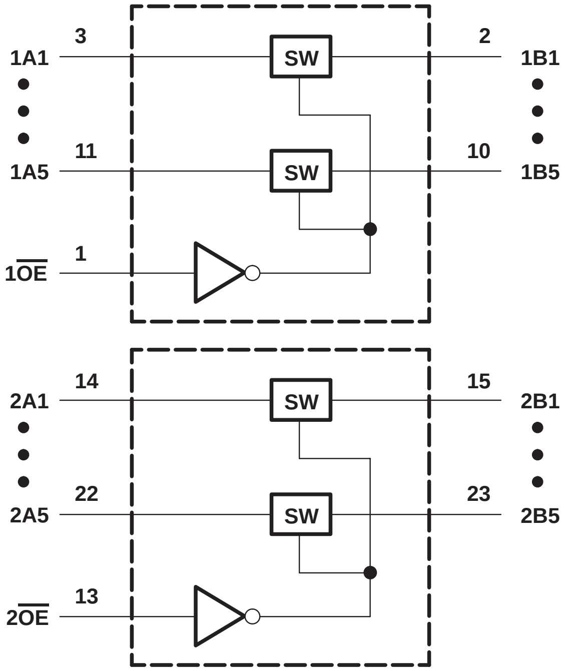
T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CBT3384CDW	CBT3384C
		Tape and reel	SN74CBT3384CDWR	
	SSOP − DB	Tube	SN74CBT3384CDB	CBT3384C
		Tape and reel	SN74CBT3384CDBR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3384CDBQR	CBT3384C
	TSSOP − PW	Tube	SN74CBT3384CPW	CU384C
		Tape and reel	SN74CBT3384CPWR	
	TVSOP − DGV	Tape and reel	SN74CBT3384CDGVR	CU384C

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

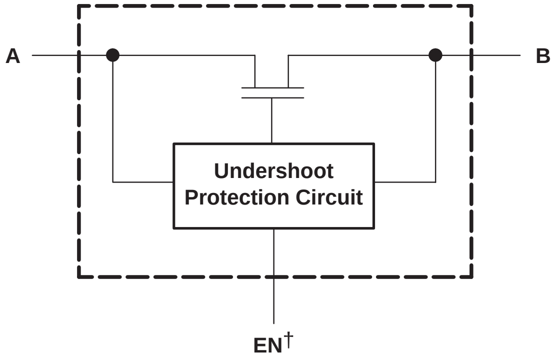
FUNCTION TABLE
(each 5-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)


1A1
3
SW
2
1B1
1A5
11
SW
10
1B5
1OE
1
2A1
14
SW
15
2B1
2A5
22
SW
23
2B5
2OE
13

simplified schematic, each FET switch (SW)


A
B
Undershoot
Protection Circuit
EN†

† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DB package	63°C/W
	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	µA
I_{OZ}[‡]		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	µA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	µA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				3.5		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		12.5		pF
r_{on}[¶]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[#]	A or B	B or A		0.24		0.15	ns
t_{en}	$\overline{OE}$	A or B		5	1.5	4.2	ns
t_{dis}	$\overline{OE}$	A or B		5	1.5	4.5	ns

[#] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V, Switch OFF, $V_{IN} = V_{CC}$ or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

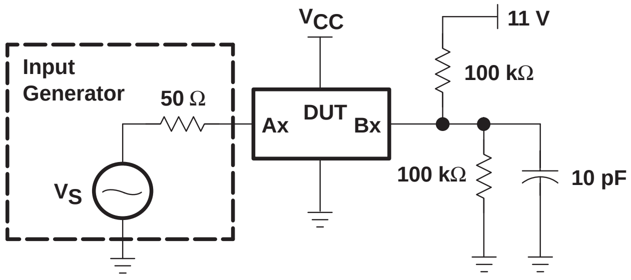

VCC
11 V
Input Generator
50 Ω
DUT
Ax
Bx
100 kΩ
100 kΩ
10 pF
VS

Figure 1. Device Test Setup

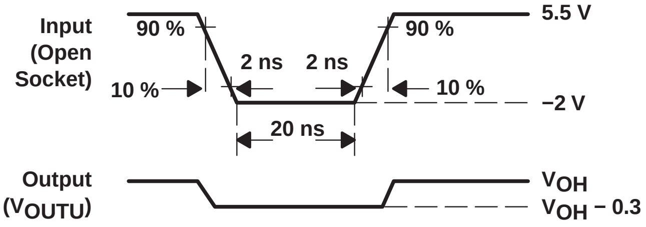
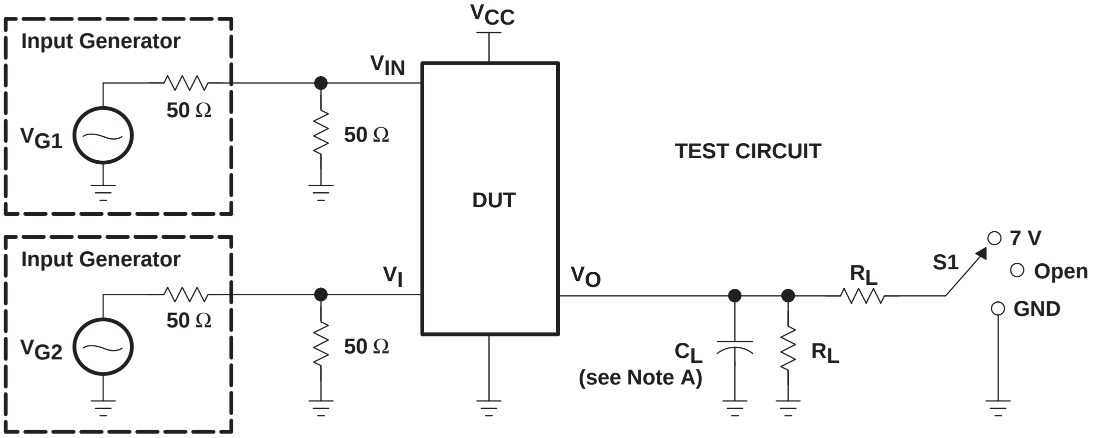
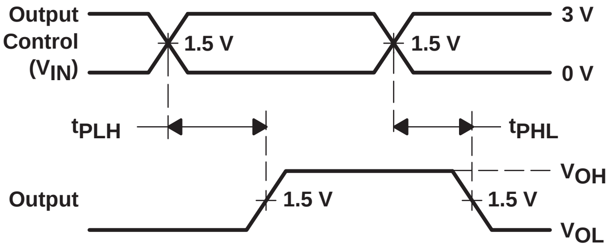

Input (Open Socket)
90 %
90 %
5.5 V
2 ns
2 ns
10 %
10 %
−2 V
20 ns
Output (VOUTU)
VOH
VOH − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

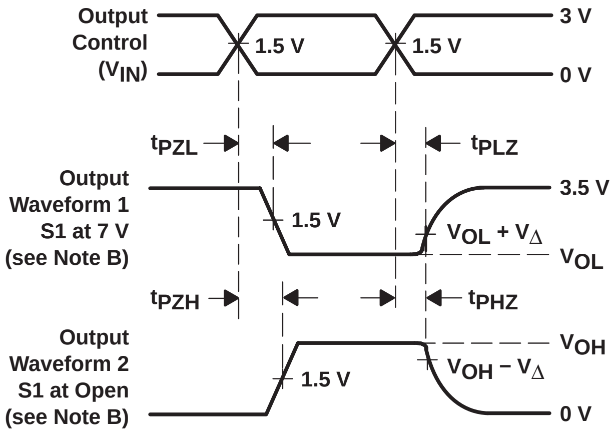
PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
Input Generator
V_{G2}
50 Ω
50 Ω
50 Ω
V_{CC}
V_{IN}
V_I
DUT
V_O
TEST CIRCUIT
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output
Control
(V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)


Output
Control
(V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

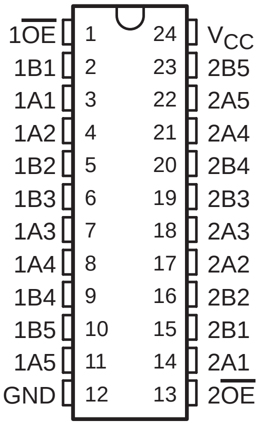
Figure 3. Test Circuit and Voltage Waveforms

SN74CBTD3384C
10-BIT FET BUS SWITCH WITH LEVEL SHIFTING
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS133A −SEPTEMBER 2003 − REVISED OCTOBER 2003

- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Integrated Diode to V_{CC} Provides 5-V Input Down To 3.3-V Output Level Shift**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **V_{CC} Operating Range From 4.5 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CBTD3384CDW	CBTD3384C
		Tape and reel	SN74CBTD3384CDWR	
	SSOP − DB	Tube	SN74CBTD3384CDB	CC384C
		Tape and reel	SN74CBTD3384CDBR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBTD3384CDBQR	CBTD3384C
	TSSOP − PW	Tube	SN74CBTD3384CPW	CC384C
		Tape and reel	SN74CBTD3384CPWR	
	TVSOP − DGV	Tape and reel	SN74CBTD3384CDGVR	CC384C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The SN74CBTD3384C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. This device features an integrated diode in series with V_{CC} to provide level shifting for 5-V input down to 3.3-V output levels. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBTD3384C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBTD3384C is organized as two 5-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. It can be used as two 5-bit bus switches or as one 10-bit bus switch. When $\overline{OE}$ is low, the associated 5-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 5-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

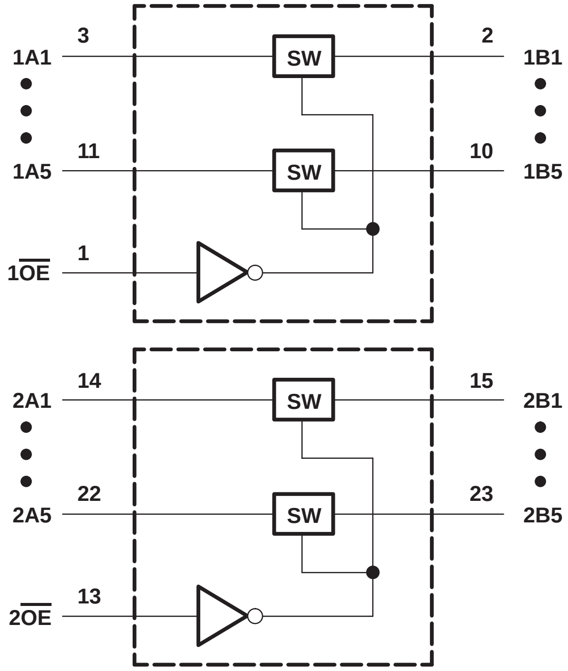
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

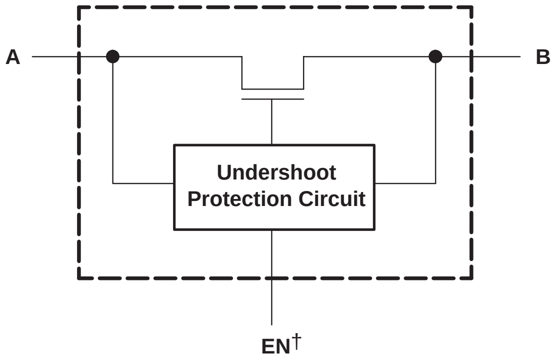
FUNCTION TABLE
(each 5-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DB package	63°C/W
	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 6 and 7)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTES: 6. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
7. In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
V_{OH}		See Figures 4 and 5						
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_{OZ}[‡]		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			1.5	mA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				3.5		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		12.5		pF
r_{on}[¶]		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	Ω
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		8	20	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	
t_{pd}[#]	A or B	B or A		0.15	ns
t_{en}	$\overline{OE}$	A or B	1.5	4.8	ns
t_{dis}	$\overline{OE}$	A or B	1.5	4.8	ns

[#] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V, Switch OFF, V_{IN} = V_{CC} or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

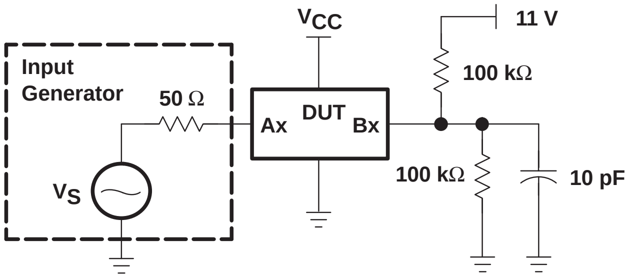

Input
Generator
50 Ω
V_S
V_{CC}
DUT
Ax
Bx
11 V
100 kΩ
100 kΩ
10 pF

Figure 1. Device Test Setup

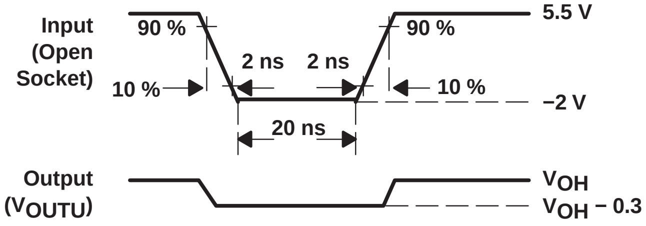
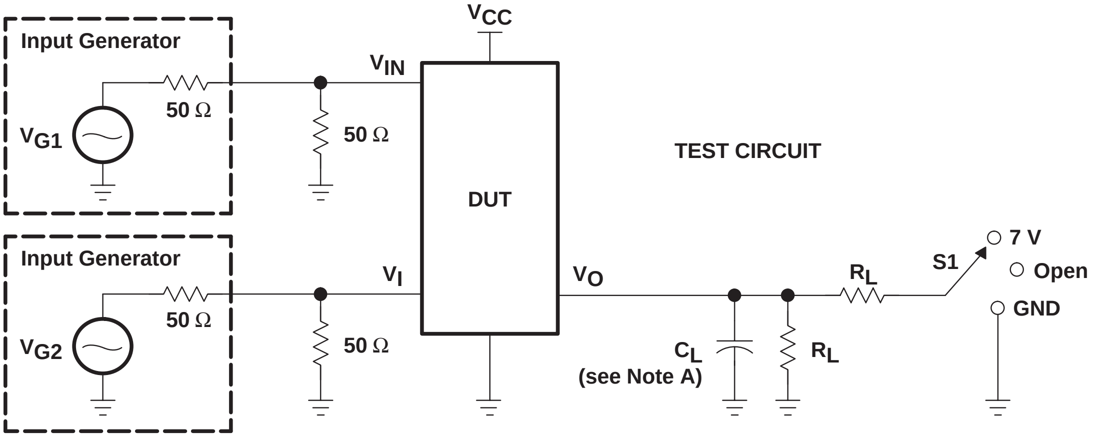
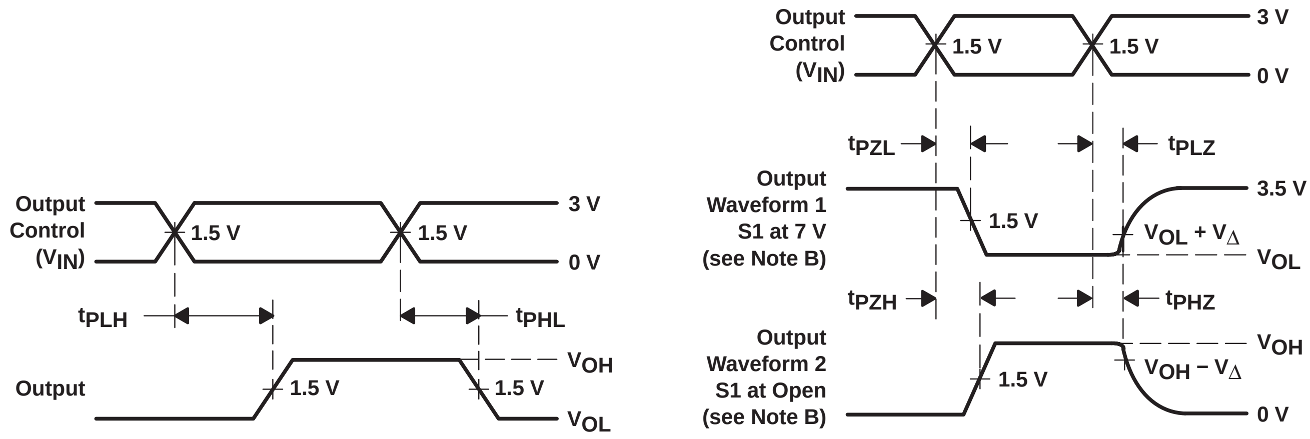

Input
(Open
Socket)
90 %
90 %
10 %
10 %
2 ns
2 ns
20 ns
5.5 V
−2 V
Output
(V_{OUTU})
V_{OH}
V_{OH} − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION FOR LEVEL SHIFTER


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V	Open	500 Ω	V_{CC} or GND	50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V	7 V	500 Ω	GND	50 pF	0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V	Open	500 Ω	V_{CC}	50 pF	0.3 V


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

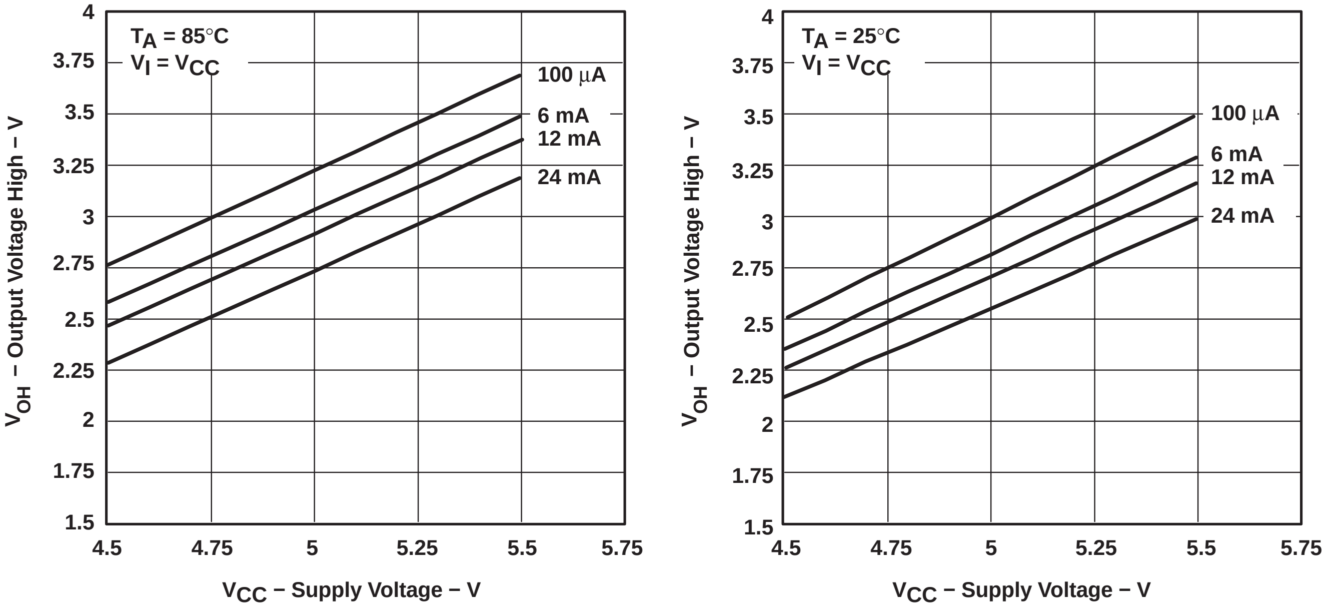
NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE HIGH vs SUPPLY VOLTAGE

OUTPUT VOLTAGE HIGH vs SUPPLY VOLTAGE



OUTPUT VOLTAGE HIGH vs SUPPLY VOLTAGE

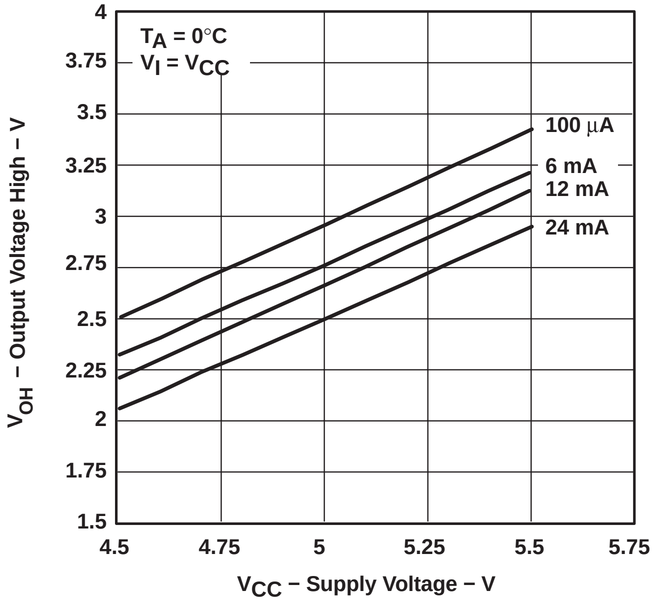


Figure 4. V_{OH} Values

TYPICAL CHARACTERISTICS (continued)

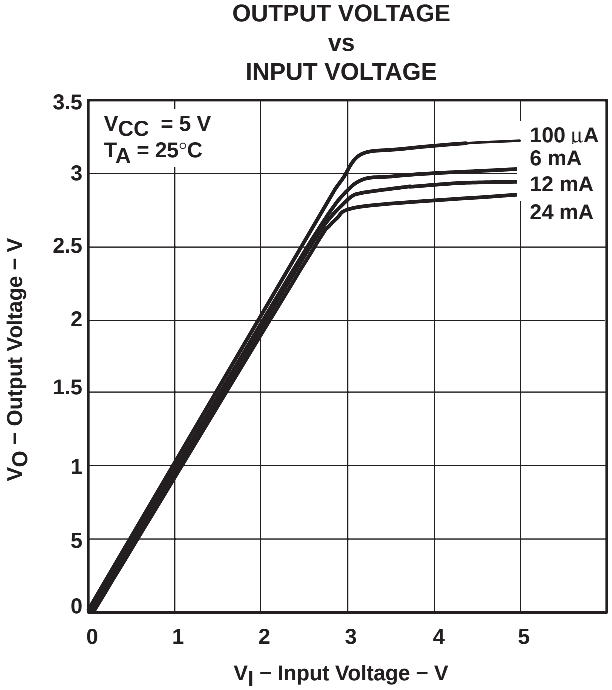


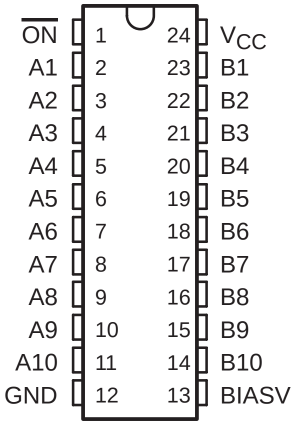
Figure 5. Data Output Voltage vs Data Input Voltage

SN74CBT6800C
10-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS138 − OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **Undershoot Protection for Off-Isolation on A and B Ports Up to −2 V**
- **B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot-Plugging**
- **Supports PCI Hot Plug**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 µA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBT6800C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT6800C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The SN74CBT6800C is a 10-bit bus switch with a single output-enable ($\overline{ON}$) input. When $\overline{ON}$ is low, the 10-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{ON}$ is high, the 10-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. The B port is precharged to BIASV through the equivalent of a 10-kΩ resistor when $\overline{ON}$ is high, or if the device is powered down (V_{CC} = 0 V).

During insertion (or removal) of a card into (or from) an active bus, the card's output voltage may be close to GND. When the connector pins make contact, the card's parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method will ensure that any glitch produced by insertion (or removal) of the card will not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{ON}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

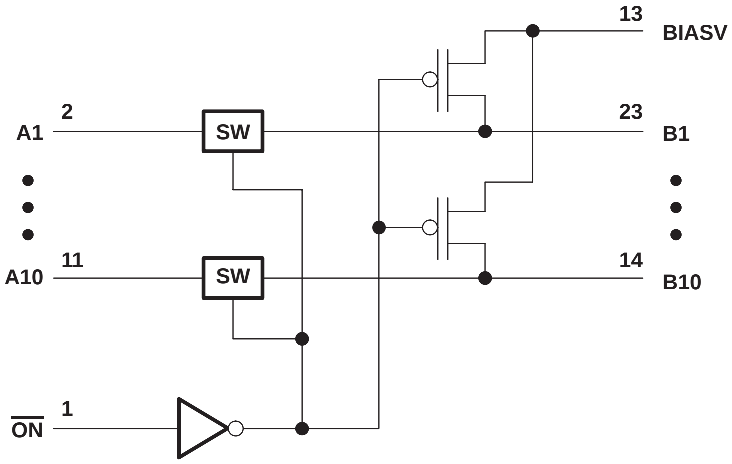
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CBT6800CDW	CBT6800C
		Tape and reel	SN74CBT6800CDWR	
	SSOP − DB	Tube	SN74CBT6800CDB	CT6800C
		Tape and reel	SN74CBT6800CDBR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT6800CDBQR	CBT6800C
	TSSOP − PW	Tube	SN74CBT6800CPW	CT6800C
		Tape and reel	SN74CBT6800CPWR	
	TVSOP − DGV	Tape and reel	SN74CBT6800CDGVR	CT6800C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

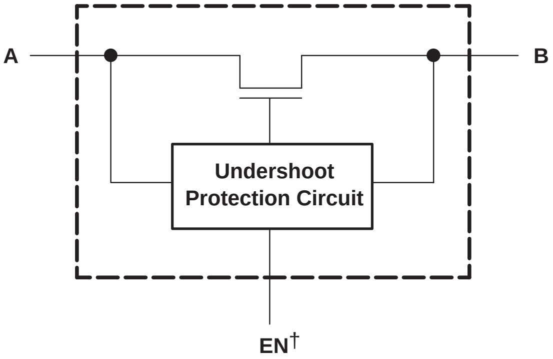
FUNCTION TABLE

INPUT $\overline{ON}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect B port = BIASV

logic diagram (positive logic)


13
BIASV
2
A1
SW
23
B1
11
A10
SW
14
B10
1
$\overline{\text{ON}}$

simplified schematic, each FET switch (SW)


A
B
Undershoot
Protection Circuit
EN†

† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Bias supply voltage range, BIASV		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DB package	63°C/W
	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

---

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIASV	Bias supply voltage	0	V_{CC}	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. BIASV is a supply voltage, not a control input.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
$V_{O(USP)}$[‡]		V_{CC} = BIASV = 5 V,	I_I = −10 mA, V_{IN} = V_{CC} or GND,	Switch OFF	3			V
V_O	B port	V_{CC} = 0 V,	BIASV = V_X,	I_O = 0	V_X−0.1		V_X	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_O	B port	V_{CC} = 4.5 V,	BIASV = 2.4 V, V_O= 0,	Switch OFF, V_{IN} = V_{CC} or GND		0.25		mA
I_{OZ}[§]		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	μA
ΔI_{CC}[¶]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				4		pF
$C_{io(OFF)}$	A port	$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		13.5		pF
r_{on}[#]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] $V_{O(USP)}$ = A-port undershoot static protection.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[¶] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

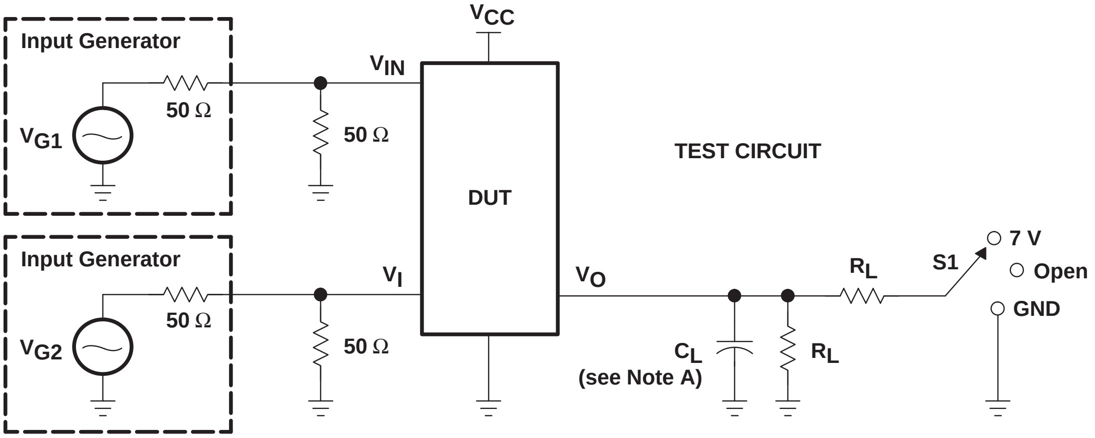
[#] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

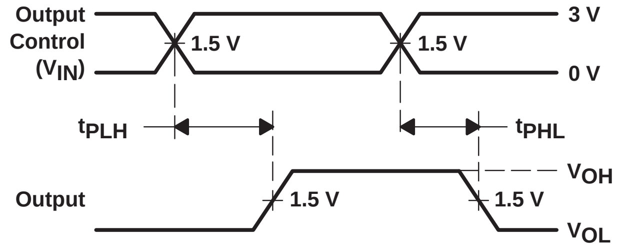
PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}[‖]		A or B	B or A		0.24		0.15	ns
t_{PZH}	BIASV = GND	$\overline{OE}$	A or B		6.2	1.5	5.9	ns
t_{PZL}	BIASV = 3 V				6.2	1.5	5.9	
t_{PHZ}	BIASV = GND	$\overline{OE}$	A or B		5.6	1.5	6.2	ns
t_{PLZ}	BIASV = 3 V				5.6	1.5	6.2	

[‖] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

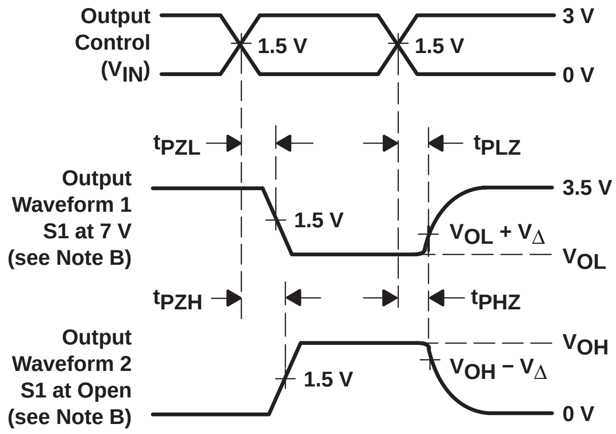
PARAMETER MEASUREMENT INFORMATION


V_{CC}
Input Generator
V_{IN}
50 Ω
V_{G1}
50 Ω
TEST CIRCUIT
DUT
Input Generator
V_I
V_O
R_L
S1
7 V
Open
GND
50 Ω
V_{G2}
50 Ω
C_L
(see Note A)
R_L

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V	Open	500 Ω	V_{CC} or GND	50 pF	
	4 V	Open	500 Ω	V_{CC} or GND	50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V	7 V	500 Ω	GND	50 pF	0.3 V
	4 V	7 V	500 Ω	GND	50 pF	0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V	Open	500 Ω	V_{CC}	50 pF	0.3 V
	4 V	Open	500 Ω	V_{CC}	50 pF	0.3 V


Output
Control
(V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)


Output
Control
(V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

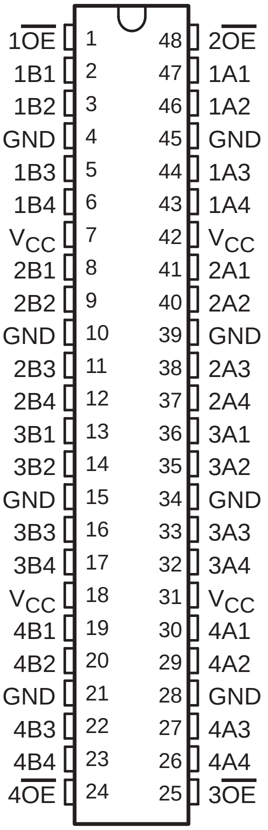
Figure 1. Test Circuit and Voltage Waveforms

SN74CBT16244C
16-BIT FET BUS SWITCH
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS134A − SEPTEMBER 2003 − REVISED OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 µA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


1$\overline{OE}$ 1 48 2$\overline{OE}$
1B1 2 47 1A1
1B2 3 46 1A2
GND 4 45 GND
1B3 5 44 1A3
1B4 6 43 1A4
V_{CC} 7 42 V_{CC}
2B1 8 41 2A1
2B2 9 40 2A2
GND 10 39 GND
2B3 11 38 2A3
2B4 12 37 2A4
3B1 13 36 3A1
3B2 14 35 3A2
GND 15 34 GND
3B3 16 33 3A3
3B4 17 32 3A4
V_{CC} 18 31 V_{CC}
4B1 19 30 4A1
4B2 20 29 4A2
GND 21 28 GND
4B3 22 27 4A3
4B4 23 26 4A4
4$\overline{OE}$ 24 25 3$\overline{OE}$

description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16244CDL	CBT16244C
		Tape and reel	SN74CBT16244CDLR	
	TSSOP − DGG	Tube	SN74CBT16244CDGG	CBT16244C
		Tape and reel	SN74CBT16244CDGGR	
	TVSOP − DGV	Tape and reel	SN74CBT16244CDGVR	CY244C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The SN74CBT16244C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16244C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT16244C is organized as four 4-bit bus switches with separate output-enable (1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$) inputs. It can be used as four 4-bit bus switches, two 8-bit bus switches, or as one 16-bit bus switch. When $\overline{OE}$ is low, the associated 4-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 4-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

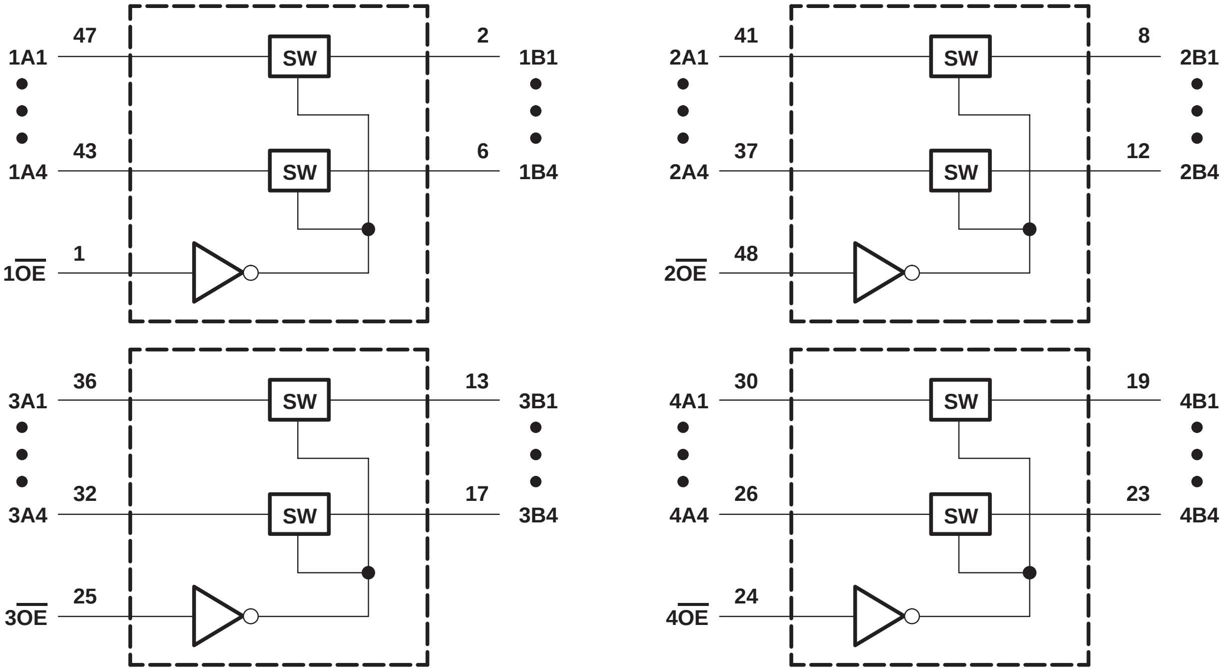
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

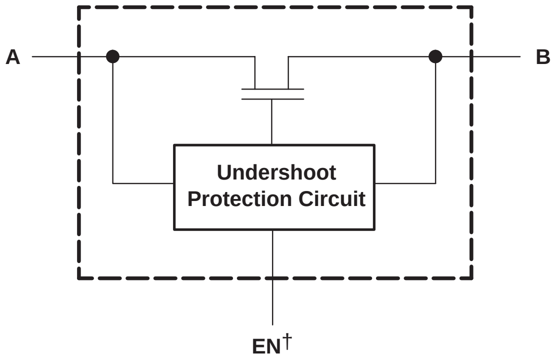
FUNCTION TABLE
(each 4-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . −0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . −0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$) . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$) . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . ±128 mA
Continuous current through V_{CC} or GND terminals . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DGG package . . . 70°C/W
DGV package . . . 58°C/W
DL package . . . 63°C/W
Storage temperature range, T_{stg} . . . −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	µA
I_{OZ}[‡]		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	µA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	µA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				3.5		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		14		pF
r_{on}[¶]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[#]	A or B	B or A		0.24		0.15	ns
t_{en}	$\overline{OE}$	A or B		5.1	1.5	4.7	ns
t_{dis}	$\overline{OE}$	A or B		5.2	1.5	5.4	ns

[#] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V, Switch OFF, V_{IN} = V_{CC} or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

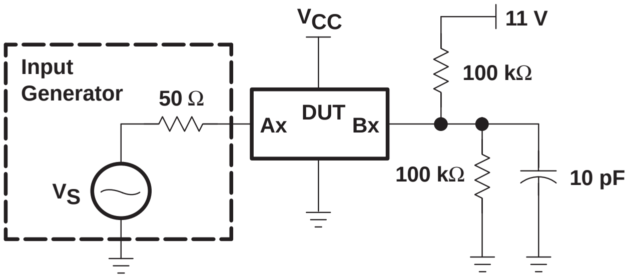

VCC
11 V
Input
Generator
50 Ω
DUT
Ax
Bx
100 kΩ
100 kΩ
10 pF
VS

Figure 1. Device Test Setup

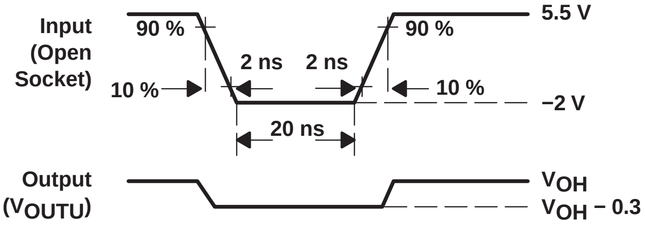
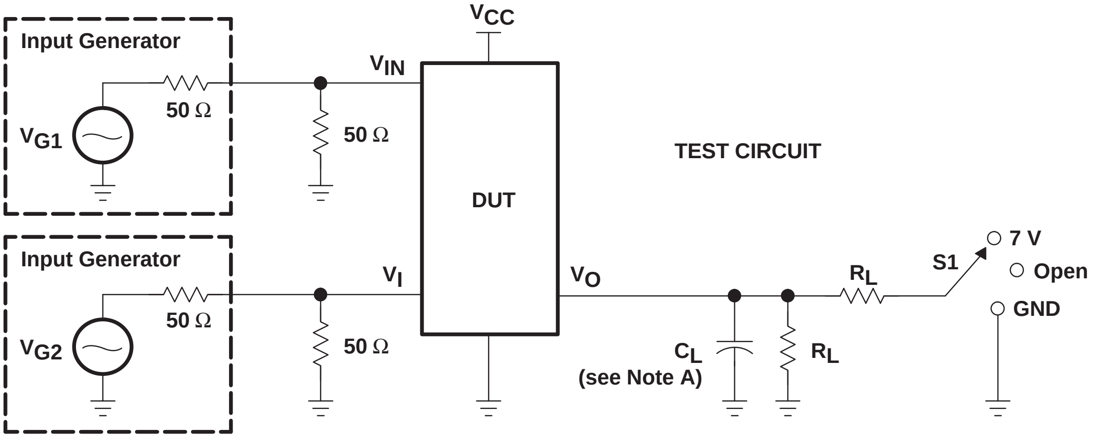
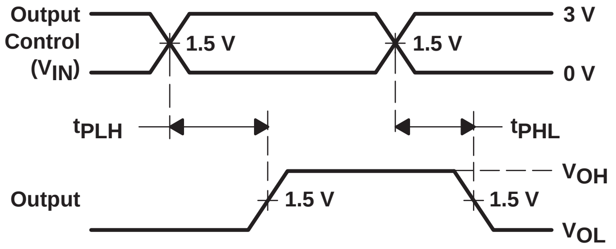

Input
(Open
Socket)
90 %
90 %
5.5 V
2 ns
2 ns
10 %
10 %
−2 V
20 ns
Output
(VOUTU)
VOH
VOH − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

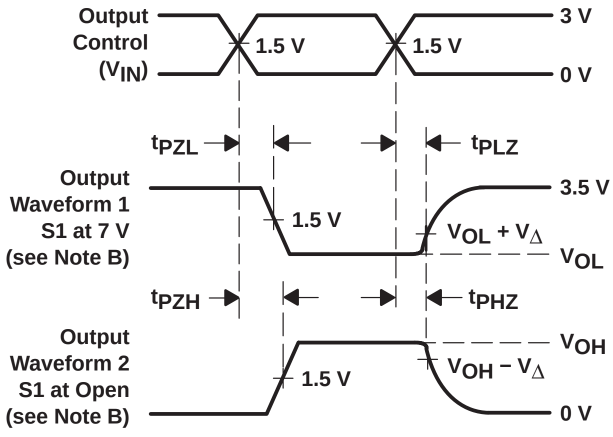
PARAMETER MEASUREMENT INFORMATION


VCC
Input Generator
VIN
50 Ω
VG1
50 Ω
TEST CIRCUIT
DUT
Input Generator
VI
VO
RL
S1
7 V
Open
GND
VG2
50 Ω
50 Ω
CL
(see Note A)
RL

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output
Control
(VIN)
1.5 V
1.5 V
3 V
0 V
tPLH
tPHL
VOH
Output
1.5 V
1.5 V
VOL

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)


Output
Control
(VIN)
1.5 V
1.5 V
3 V
0 V
tPZL
tPLZ
Output
Waveform 1
S1 at 7 V
(see Note B)
3.5 V
1.5 V
VOL + VΔ
VOL
tPZH
tPHZ
Output
Waveform 2
S1 at Open
(see Note B)
VOH
1.5 V
VOH − VΔ
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

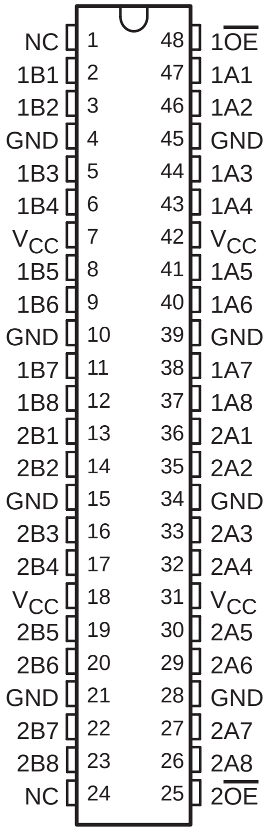
Figure 3. Test Circuit and Voltage Waveforms

SN74CBT16245C
16-BIT FET BUS SWITCH
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS139 − OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **Undershoot Protection for Off-Isolation on A and B Ports Up to −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1 48 1$\overline{OE}$
1B1 2 47 1A1
1B2 3 46 1A2
GND 4 45 GND
1B3 5 44 1A3
1B4 6 43 1A4
V_{CC} 7 42 V_{CC}
1B5 8 41 1A5
1B6 9 40 1A6
GND 10 39 GND
1B7 11 38 1A7
1B8 12 37 1A8
2B1 13 36 2A1
2B2 14 35 2A2
GND 15 34 GND
2B3 16 33 2A3
2B4 17 32 2A4
V_{CC} 18 31 V_{CC}
2B5 19 30 2A5
2B6 20 29 2A6
GND 21 28 GND
2B7 22 27 2A7
2B8 23 26 2A8
NC 24 25 2$\overline{OE}$

NC − No internal connection

description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16245CDL	CBT16245C
		Tape and reel	SN74CBT16245CDLR	
	TSSOP − DGG	Tube	SN74CBT16245CDGG	CBT16245C
		Tape and reel	SN74CBT16245CDGGR	
	TVSOP − DGV	Tape and reel	SN74CBT16245CDGVR	CY245C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TEXAS INSTRUMENTS

description/ordering information (continued)

The SN74CBT16245C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16245C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT16245C is organized as two 8-bit bus switches with separate output-enable (1$\overline{\text{OE}}$, 2$\overline{\text{OE}}$) inputs. It can be used as two 8-bit bus switches or as one 16-bit bus switch. When $\overline{\text{OE}}$ is low, the associated 8-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{\text{OE}}$ is high, the associated 8-bit bus switch is OFF and the high-impedance state exists between the A and B ports.

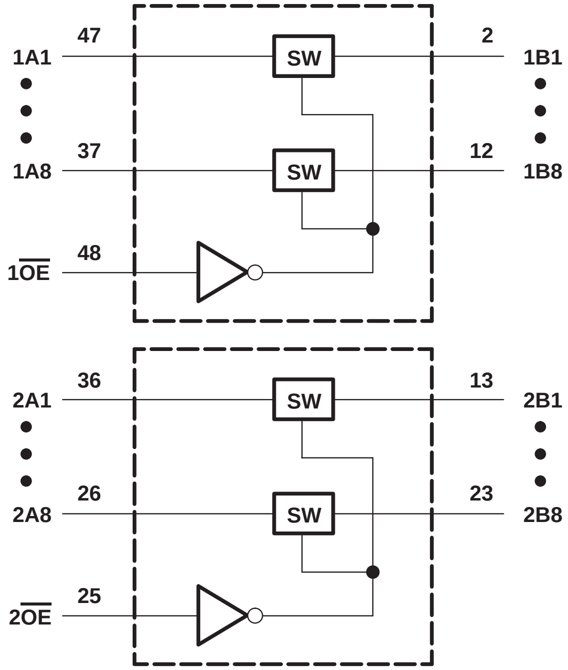
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

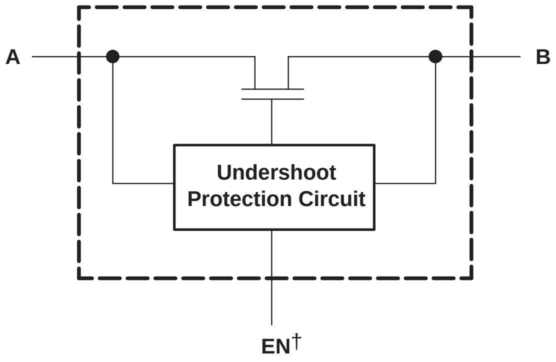
FUNCTION TABLE
(each 8-bit bus switch)

INPUT $\overline{\text{OE}}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



[†] EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V_{CC}		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} (V_{IN} < 0)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O}$ < 0)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

[‡] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	µA
I_{OZ}‡		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	µA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	µA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				3.5		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		14		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}#	A or B	B or A		0.24		0.15	ns
t_{en}	$\overline{OE}$	A or B		5.4	1.5	5	ns
t_{dis}	$\overline{OE}$	A or B		5.6	1.5	5.6	ns

# The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V,	Switch OFF,	V_{IN} = V_{CC} or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

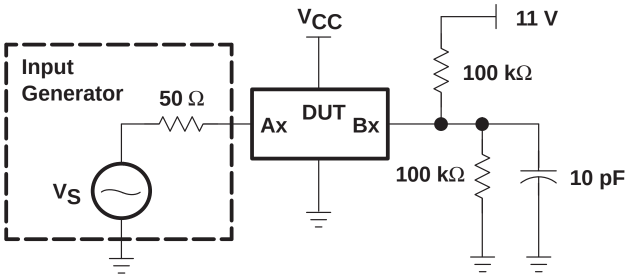

VCC
11 V
Input Generator
50 Ω
Ax
DUT
Bx
100 kΩ
100 kΩ
10 pF
VS

Figure 1. Device Test Setup

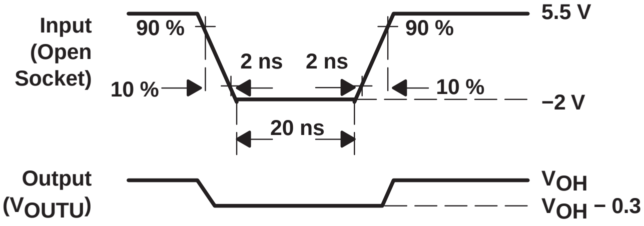
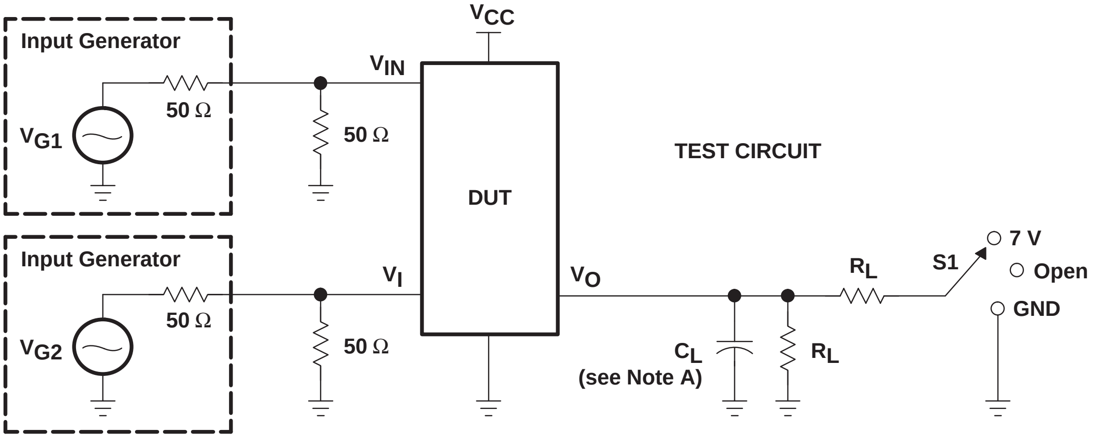
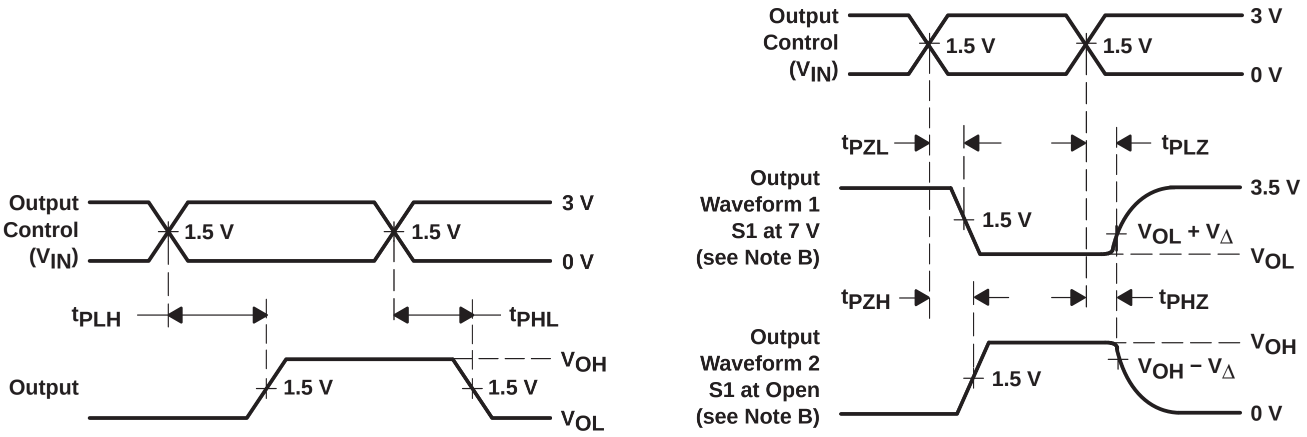

Input (Open Socket)
90 %
90 %
5.5 V
2 ns
2 ns
10 %
10 %
−2 V
20 ns
Output (VOUTU)
VOH
VOH − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION


V_{CC}
Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
$V_{OH} − V_\Delta$
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

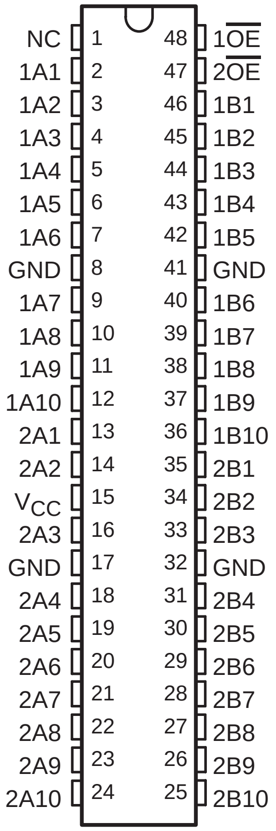
Figure 3. Test Circuit and Voltage Waveforms

SN74CBT16210C
20-BIT FET BUS SWITCH
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS115C − JANUARY 2003 − REVISED OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1 48 1$\overline{OE}$
1A1 2 47 2$\overline{OE}$
1A2 3 46 1B1
1A3 4 45 1B2
1A4 5 44 1B3
1A5 6 43 1B4
1A6 7 42 1B5
GND 8 41 GND
1A7 9 40 1B6
1A8 10 39 1B7
1A9 11 38 1B8
1A10 12 37 1B9
2A1 13 36 1B10
2A2 14 35 2B1
V_{CC} 15 34 2B2
2A3 16 33 2B3
GND 17 32 GND
2A4 18 31 2B4
2A5 19 30 2B5
2A6 20 29 2B6
2A7 21 28 2B7
2A8 22 27 2B8
2A9 23 26 2B9
2A10 24 25 2B10

NC − No internal connection

description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16210CDL	CBT16210C
		Tape and reel	SN74CBT16210CDLR	
	TSSOP − DGG	Tube	SN74CBT16210CDGG	CBT16210C
		Tape and reel	SN74CBT16210CDGGR	
	TVSOP − DGV	Tape and reel	SN74CBT16210CDGVR	CY210C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TEXAS INSTRUMENTS

description/ordering information (continued)

The SN74CBT16210C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16210C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT16210C is organized as two 10-bit bus switches with separate output-enable (1$\overline{OE}$, 2$\overline{OE}$) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When $\overline{OE}$ is low, the associated 10-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 10-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

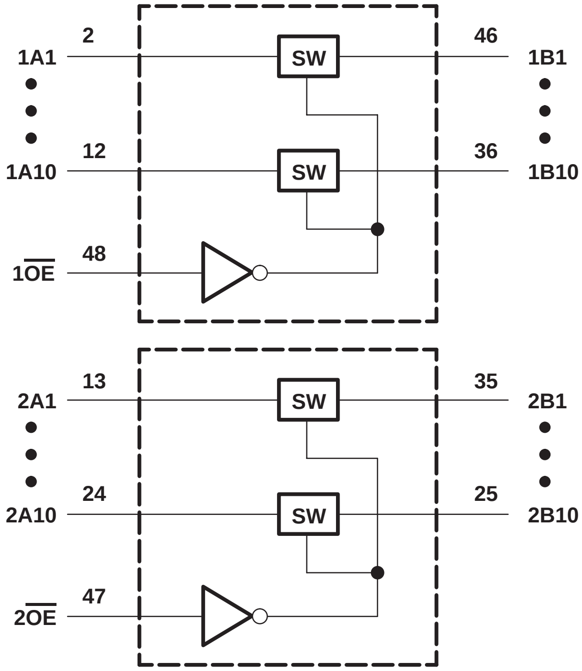
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

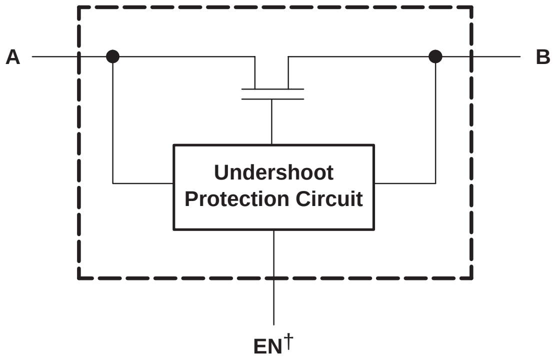
FUNCTION TABLE
(each 10-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_{OZ}[‡]		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	μA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				4.5		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		14.5		pF
r_{on}[¶]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[#]	A or B	B or A		0.24		0.15	ns
t_{en}	$\overline{OE}$	A or B		6.5	1.5	6	ns
t_{dis}	$\overline{OE}$	A or B		6.5	1.5	6	ns

[#] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V, Switch OFF, V_{IN} = V_{CC} or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

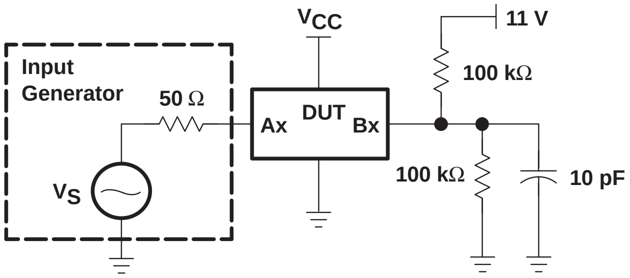

Input
Generator
50 Ω
V_S
V_{CC}
Ax
DUT
Bx
11 V
100 kΩ
100 kΩ
10 pF

Figure 1. Device Test Setup

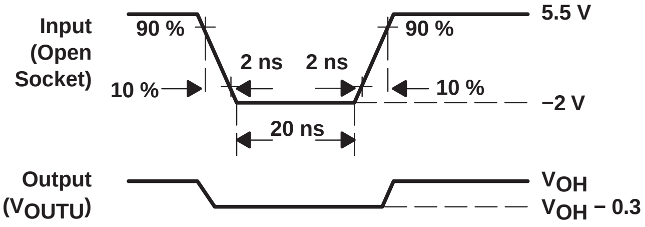
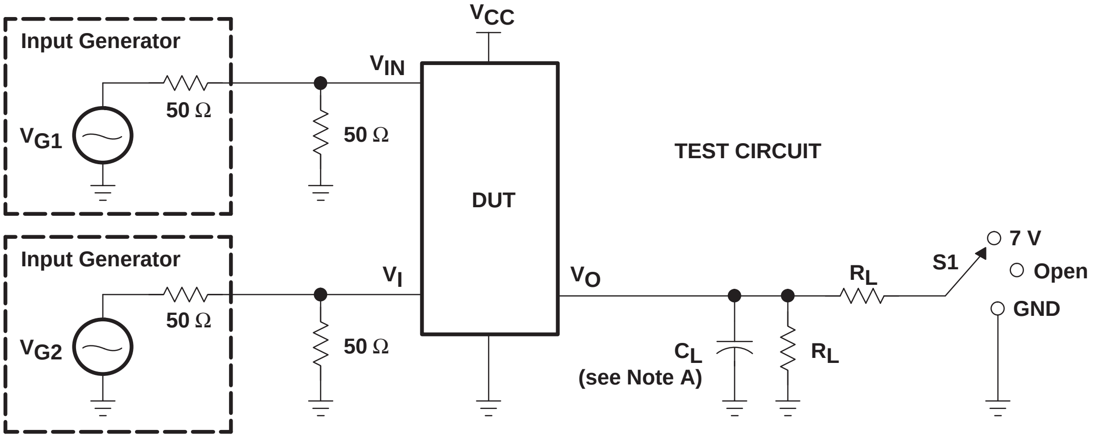
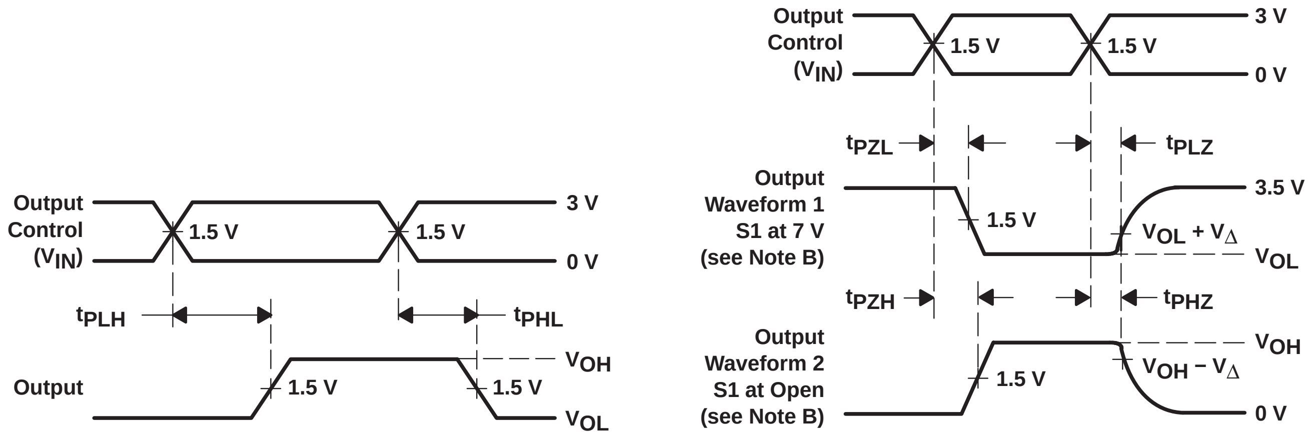

Input
(Open
Socket)
90 %
10 %
2 ns
2 ns
90 %
10 %
20 ns
5.5 V
−2 V
Output
(V_{OUTU})
V_{OH}
V_{OH} − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

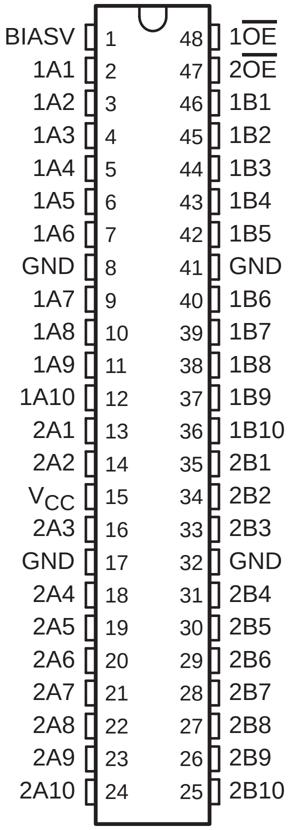
Figure 3. Test Circuit and Voltage Waveforms

SN74CBT16800C
20-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS117C − JANUARY 2003 − REVISED OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot-Plugging**
- **Supports PCI Hot Plug**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


BIASV 1 48 1$\overline{OE}$
1A1 2 47 2$\overline{OE}$
1A2 3 46 1B1
1A3 4 45 1B2
1A4 5 44 1B3
1A5 6 43 1B4
1A6 7 42 1B5
GND 8 41 GND
1A7 9 40 1B6
1A8 10 39 1B7
1A9 11 38 1B8
1A10 12 37 1B9
2A1 13 36 1B10
2A2 14 35 2B1
V_{CC} 15 34 2B2
2A3 16 33 2B3
GND 17 32 GND
2A4 18 31 2B4
2A5 19 30 2B5
2A6 20 29 2B6
2A7 21 28 2B7
2A8 22 27 2B8
2A9 23 26 2B9
2A10 24 25 2B10

description/ordering information

The SN74CBT16800C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16800C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description/ordering information (continued)

The SN74CBT16800C is organized as two 10-bit bus switches with separate output-enable (1$\overline{\text{OE}}$, 2$\overline{\text{OE}}$) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When $\overline{\text{OE}}$ is low, the associated 10-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{\text{OE}}$ is high, the associated 10-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. The B port is precharged to BIASV through the equivalent of a 10-kΩ resistor when $\overline{\text{OE}}$ is high, or if the device is powered down (V_{CC} = 0 V).

During insertion (or removal) of a card into (or from) an active bus, the card’s output voltage may be close to GND. When the connector pins make contact, the card’s parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method will ensure that any glitch produced by insertion (or removal) of the card will not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

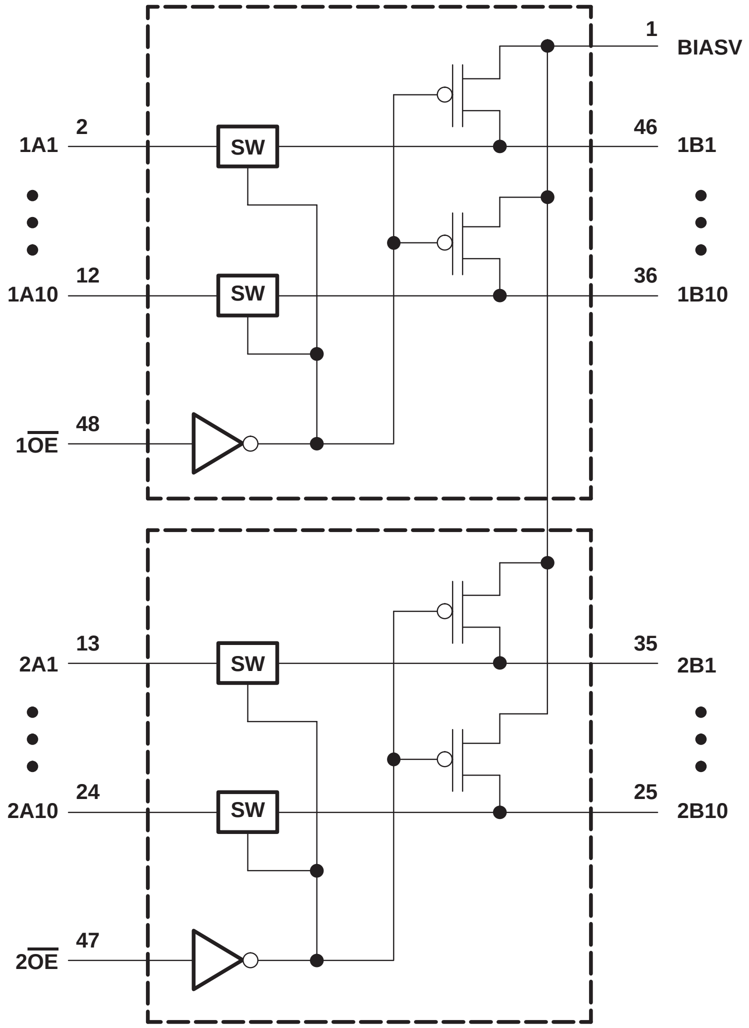
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16800CDL	CBT16800C
		Tape and reel	SN74CBT16800CDLR	
	TSSOP − DGG	Tube	SN74CBT16800CDGG	CBT16800C
		Tape and reel	SN74CBT16800CDGGR	
	TVSOP − DGV	Tape and reel	SN74CBT16800CDGVR	CY800C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

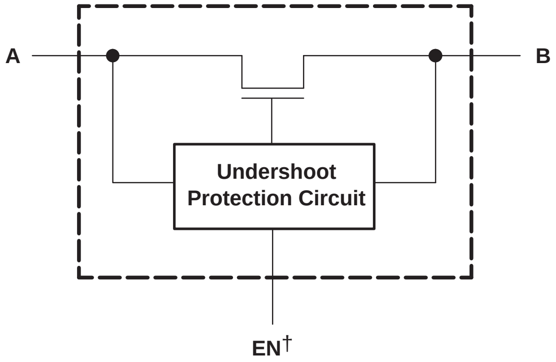
FUNCTION TABLE
(each 10-bit bus switch)

INPUT $\overline{\text{OE}}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect B port = BIASV

logic diagram (positive logic)


1
BIASV
1A1
2
SW
46
1B1
1A10
12
SW
36
1B10
1OE
48
2A1
13
SW
35
2B1
2A10
24
SW
25
2B10
2OE
47

simplified schematic, each FET switch (SW)


A
B
Undershoot Protection Circuit
EN†

† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Bias supply voltage range, BIASV		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIASV	Bias supply voltage	0	V_{CC}	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. BIASV is a supply voltage, not a control input.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
$V_{O(USP)}$‡		V_{CC} = BIASV = 5 V,	I_I = −10 mA, V_{IN} = V_{CC} or GND,	Switch OFF	3			V
V_O	B port	V_{CC} = 0 V,	BIASV = V_X,	I_O = 0	V_X−0.1		V_X	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_O	B port	V_{CC} = 4.5 V,	BIASV = 2.4 V, V_O = 0,	Switch OFF, V_{IN} = V_{CC} or GND		0.25		mA
I_{OZ}§		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	μA
ΔI_{CC}¶	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				4.5		pF
$C_{io(OFF)}$	A port	$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		15.5		pF
r_{on}#		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ $V_{O(USP)}$ = A-port undershoot static protection.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

¶ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

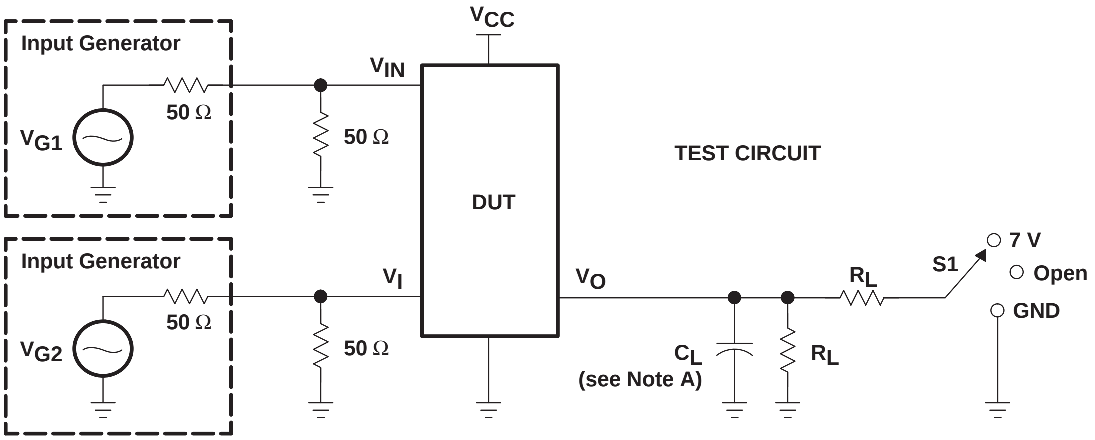
# Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

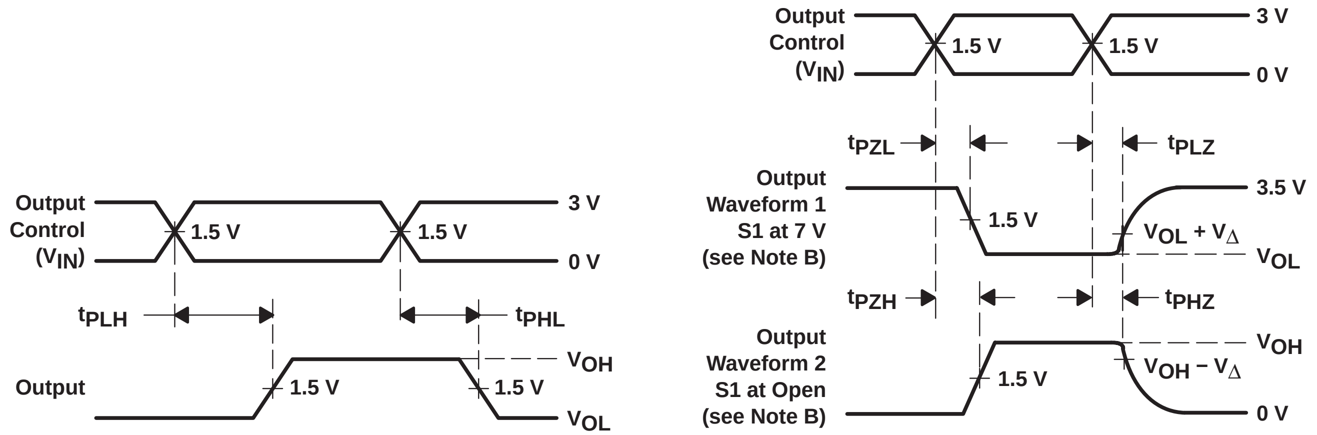
PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}‖		A or B	B or A		0.24		0.15	ns
t_{PZH}	BIASV = GND	$\overline{OE}$	A or B		6.5	1.5	6	ns
t_{PZL}	BIASV = 3 V				6.5	1.5	6	
t_{PHZ}	BIASV = GND	$\overline{OE}$	A or B		6.5	1.5	6	ns
t_{PLZ}	BIASV = 3 V				6.5	1.5	6	

‖ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION


Input Generator
VG1
50 Ω
VIN
50 Ω
VCC
DUT
TEST CIRCUIT
Input Generator
VG2
50 Ω
VI
50 Ω
VO
CL
(see Note A)
RL
RL
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output Control (VIN)
3 V
1.5 V
1.5 V
0 V
tPLH
tPHL
Output
VOH
1.5 V
1.5 V
VOL
Output Control (VIN)
3 V
1.5 V
1.5 V
0 V
tPZL
tPLZ
Output Waveform 1 S1 at 7 V (see Note B)
3.5 V
1.5 V
VOL + VΔ
VOL
tPZH
tPHZ
Output Waveform 2 S1 at Open (see Note B)
VOH
1.5 V
VOH − VΔ
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

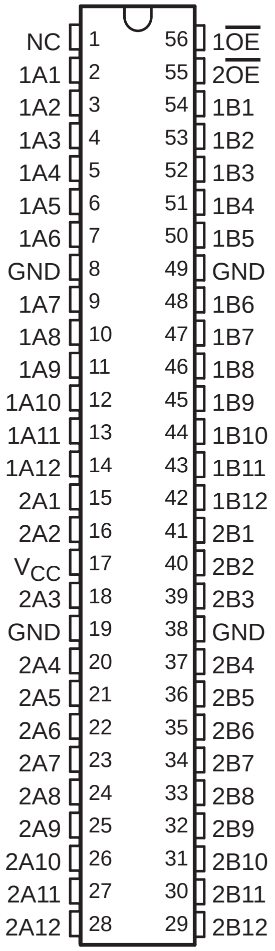
Figure 1. Test Circuit and Voltage Waveforms

SN74CBT16211C
24-BIT FET BUS SWITCH
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS116C − JANUARY 2003 − REVISED OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1 56 1$\overline{OE}$
1A1 2 55 2$\overline{OE}$
1A2 3 54 1B1
1A3 4 53 1B2
1A4 5 52 1B3
1A5 6 51 1B4
1A6 7 50 1B5
GND 8 49 GND
1A7 9 48 1B6
1A8 10 47 1B7
1A9 11 46 1B8
1A10 12 45 1B9
1A11 13 44 1B10
1A12 14 43 1B11
2A1 15 42 1B12
2A2 16 41 2B1
V_{CC} 17 40 2B2
2A3 18 39 2B3
GND 19 38 GND
2A4 20 37 2B4
2A5 21 36 2B5
2A6 22 35 2B6
2A7 23 34 2B7
2A8 24 33 2B8
2A9 25 32 2B9
2A10 26 31 2B10
2A11 27 30 2B11
2A12 28 29 2B12

NC − No internal connection

description/ordering information

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16211CDL	CBT16211C
		Tape and reel	SN74CBT16211CDLR	
	TSSOP − DGG	Tube	SN74CBT16211CDGG	CBT16211C
		Tape and reel	SN74CBT16211CDGGR	
	TVSOP − DGV	Tape and reel	SN74CBT16211CDGVR	CY211C

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The SN74CBT16211C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16211C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT16211C is organized as two 12-bit bus switches with separate output-enable (1$\overline{OE}$, 2$\overline{OE}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When $\overline{OE}$ is low, the associated 12-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 12-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

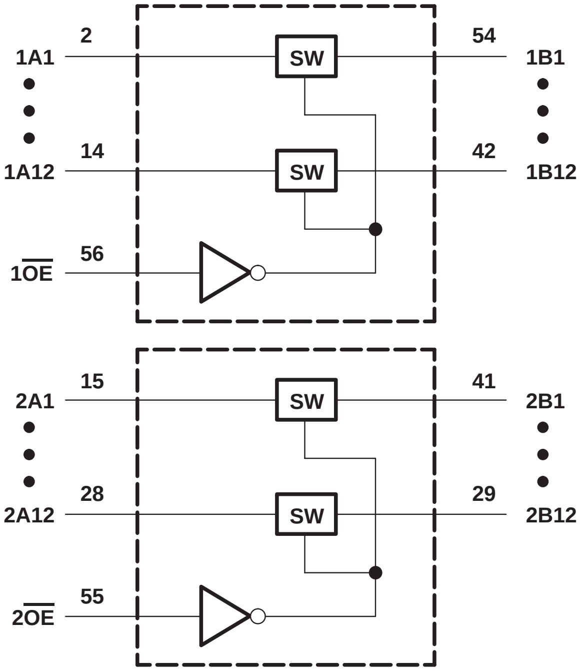
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

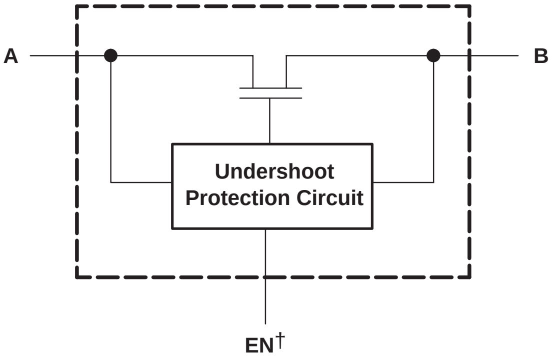
FUNCTION TABLE
(each 12-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DGG package	64°C/W
DGV package	48°C/W
DL package	56°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, $V_{IN} = V_{CC}$ or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	$V_{IN} = V_{CC}$ or GND				±1	μA
I_{OZ}‡		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, $V_{IN} = V_{CC}$ or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, $V_{IN} = V_{CC}$ or GND,	Switch ON or OFF			3	μA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				4.5		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	$V_{IN} = V_{CC}$ or GND		5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	$V_{IN} = V_{CC}$ or GND		14.5		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}#	A or B	B or A		0.24		0.15	ns
t_{en}	$\overline{OE}$	A or B		6.5	1.5	6	ns
t_{dis}	$\overline{OE}$	A or B		6.5	1.5	6	ns

# The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V, Switch OFF, V_{IN} = V_{CC} or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

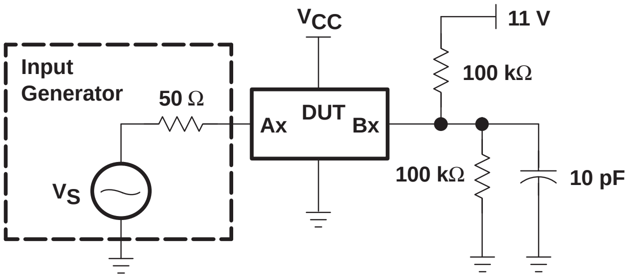

VCC
11 V
Input Generator
50 Ω
DUT
Ax
Bx
100 kΩ
100 kΩ
10 pF
VS

Figure 1. Device Test Setup

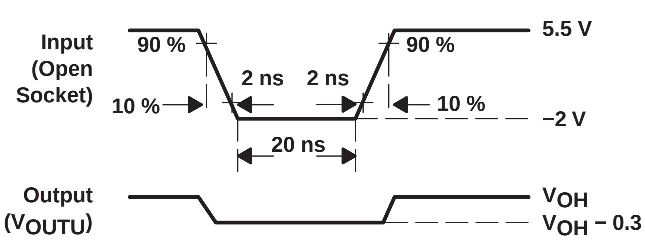
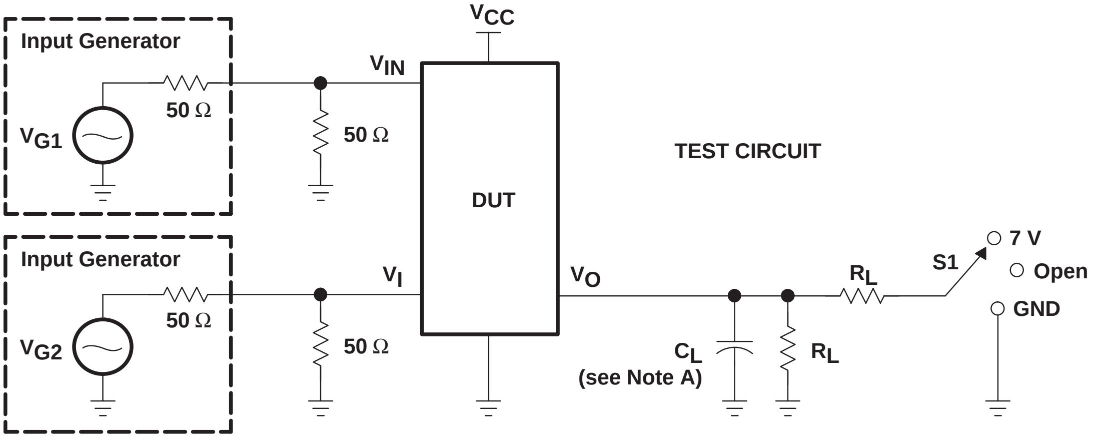
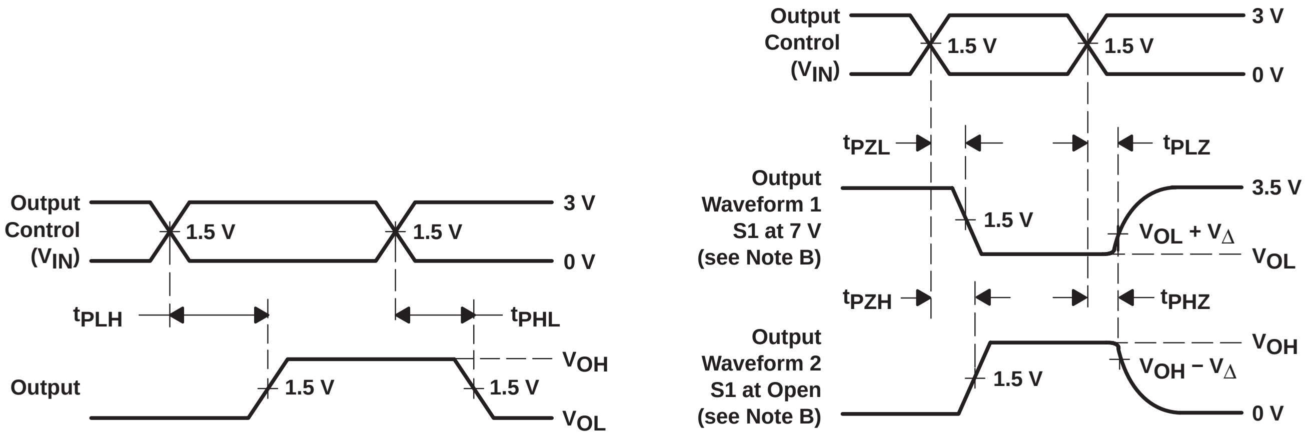

Input (Open Socket)
90 %
90 %
5.5 V
2 ns
2 ns
10 %
10 %
−2 V
20 ns
Output (VOUTU)
VOH
VOH − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION


VCC
Input Generator
VIN
VG1
50 Ω
50 Ω
TEST CIRCUIT
DUT
Input Generator
VI
VO
RL
S1
7 V
Open
GND
VG2
50 Ω
50 Ω
CL
(see Note A)
RL

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output Control (VIN)
3 V
1.5 V
1.5 V
0 V
tPLH
tPHL
VOH
Output
1.5 V
1.5 V
VOL
Output Control (VIN)
3 V
1.5 V
1.5 V
0 V
tPZL
tPLZ
Output Waveform 1 S1 at 7 V (see Note B)
3.5 V
1.5 V
VOL + VΔ
VOL
tPZH
tPHZ
Output Waveform 2 S1 at Open (see Note B)
VOH
1.5 V
VOH − VΔ
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

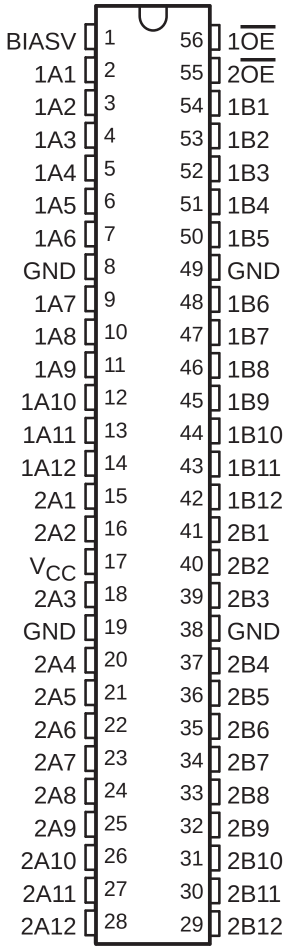
Figure 3. Test Circuit and Voltage Waveforms

SN74CBT16811C
24-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS 5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS118C − JANUARY 2003 − REVISED OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot-Plugging**
- **Supports PCI Hot Plug**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DGG, DGV, OR DL PACKAGE (TOP VIEW)


BIASV 1 56 $1\overline{OE}$
1A1 2 55 $2\overline{OE}$
1A2 3 54 1B1
1A3 4 53 1B2
1A4 5 52 1B3
1A5 6 51 1B4
1A6 7 50 1B5
GND 8 49 GND
1A7 9 48 1B6
1A8 10 47 1B7
1A9 11 46 1B8
1A10 12 45 1B9
1A11 13 44 1B10
1A12 14 43 1B11
2A1 15 42 1B12
2A2 16 41 2B1
V_{CC} 17 40 2B2
2A3 18 39 2B3
GND 19 38 GND
2A4 20 37 2B4
2A5 21 36 2B5
2A6 22 35 2B6
2A7 23 34 2B7
2A8 24 33 2B8
2A9 25 32 2B9
2A10 26 31 2B10
2A11 27 30 2B11
2A12 28 29 2B12

description/ordering information

The SN74CBT16811C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16811C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The SN74CBT16811C is organized as two 12-bit bus switches with separate output-enable (1$\overline{OE}$, 2$\overline{OE}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When $\overline{OE}$ is low, the associated 12-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 12-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. The B port is precharged to BIASV through the equivalent of a 10-kΩ resistor when $\overline{OE}$ is high, or if the device is powered down (V_{CC} = 0 V).

During insertion (or removal) of a card into (or from) an active bus, the card's output voltage may be close to GND. When the connector pins make contact, the card's parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method will ensure that any glitch produced by insertion (or removal) of the card will not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

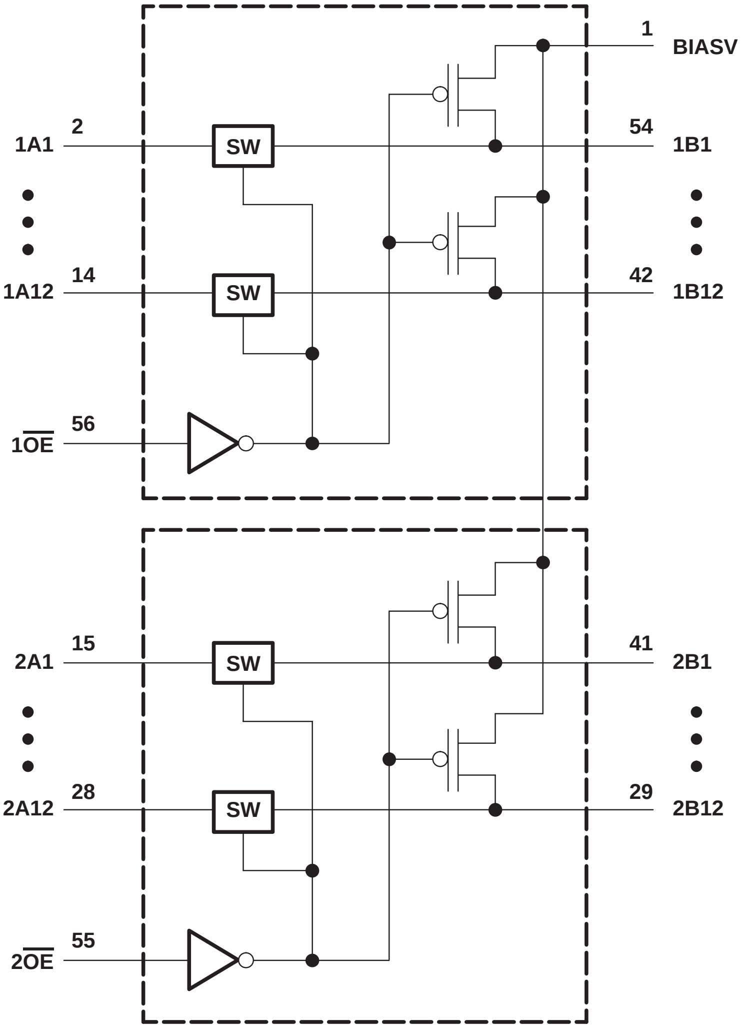
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16811CDL	CBT16811C
		Tape and reel	SN74CBT16811CDLR	
	TSSOP − DGG	Tube	SN74CBT16811CDGG	CBT16811C
		Tape and reel	SN74CBT16811CDGGR	
	TVSOP − DGV	Tape and reel	SN74CBT16811CDGVR	CY811C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

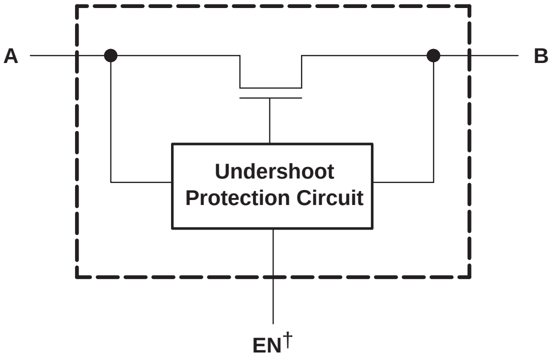
FUNCTION TABLE
(each 12-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect B port = BIASV

logic diagram (positive logic)


1
BIASV
1A1
2
SW
54
1B1
1A12
14
SW
42
1B12
1OE
56
2A1
15
SW
41
2B1
2A12
28
SW
29
2B12
2OE
55

simplified schematic, each FET switch (SW)


A
B
Undershoot Protection Circuit
EN†

---

† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}		−0.5 V to 7 V
Bias supply voltage range, BIASV		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIASV	Bias supply voltage	0	V_{CC}	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. BIASV is a supply voltage, not a control input.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
$V_{O(USP)}$‡		V_{CC} = BIASV = 5 V,	I_I = −10 mA, V_{IN} = V_{CC} or GND,	Switch OFF	3			V
V_O	B port	V_{CC} = 0 V,	BIASV = V_X,	I_O = 0	V_X−0.1		V_X	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	µA
I_O	B port	V_{CC} = 4.5 V,	BIASV = 2.4 V, V_O = 0,	Switch OFF, V_{IN} = V_{CC} or GND		0.25		mA
I_{OZ}§		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	µA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	µA
ΔI_{CC}¶	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				4.5		pF
$C_{io(OFF)}$	A port	$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		15.5		pF
$r_{on}$$^{\#}$		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ $V_{O(USP)}$ = A-port undershoot static protection.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

¶ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

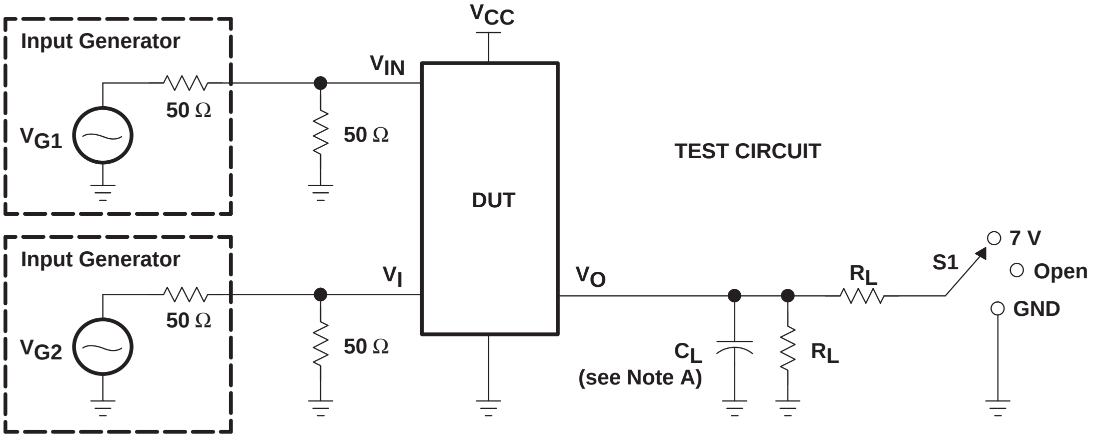
# Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

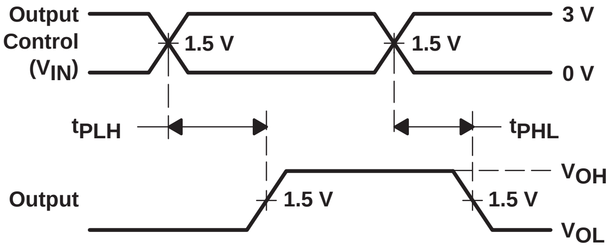
PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
$t_{pd}$$^{||}$		A or B	B or A		0.24		0.15	ns
t_{PZH}	BIASV = GND	$\overline{OE}$	A or B		6.5	1.5	6	ns
t_{PZL}	BIASV = 3 V				6.5	1.5	6	
t_{PHZ}	BIASV = GND	$\overline{OE}$	A or B		6.5	1.5	6	ns
t_{PLZ}	BIASV = 3 V				6.5	1.5	6	

‖ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

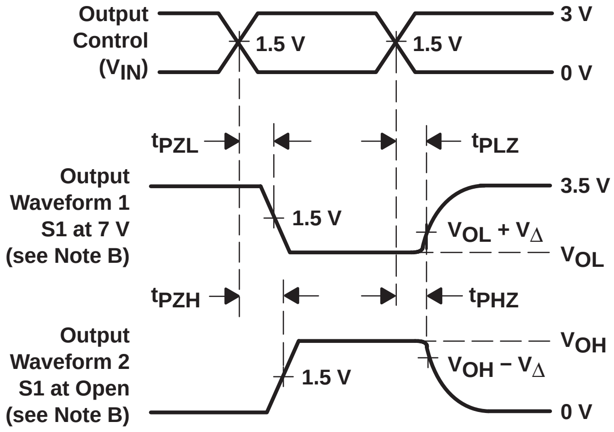
PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
50 Ω
V_{IN}
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
50 Ω
V_I
V_O
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output
Control
(V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)


Output
Control
(V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

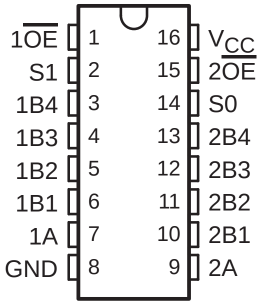
Figure 1. Test Circuit and Voltage Waveforms

SN74CBT3253C
DUAL 1-OF-4 FET MULTIPLEXER/DEMULTIPLEXER 5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

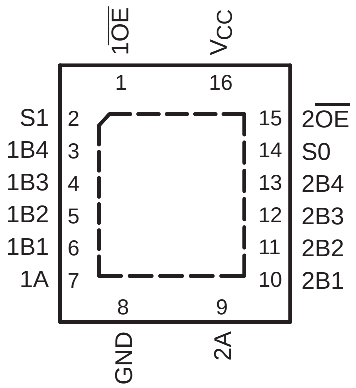
SCDS123A − JULY 2003 − REVISED OCTOBER 2003

- **SN74CBT3253C Functionally Identical to Industry-Standard ’3253 Function**
- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 µA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports I^{2}C Bus Expansion**
- **Supports Both Digital and Analog Applications: USB Interface, Bus Isolation, Low-Distortion Signal Gating**

D, DB, DBQ, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBT3253C is a high-speed TTL-compatible FET multiplexer/demultiplexer with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3253C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3253C is organized as two 1-of-4 multiplexer/demultiplexers with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When $\overline{OE}$ is low, the associated multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\mathrm{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

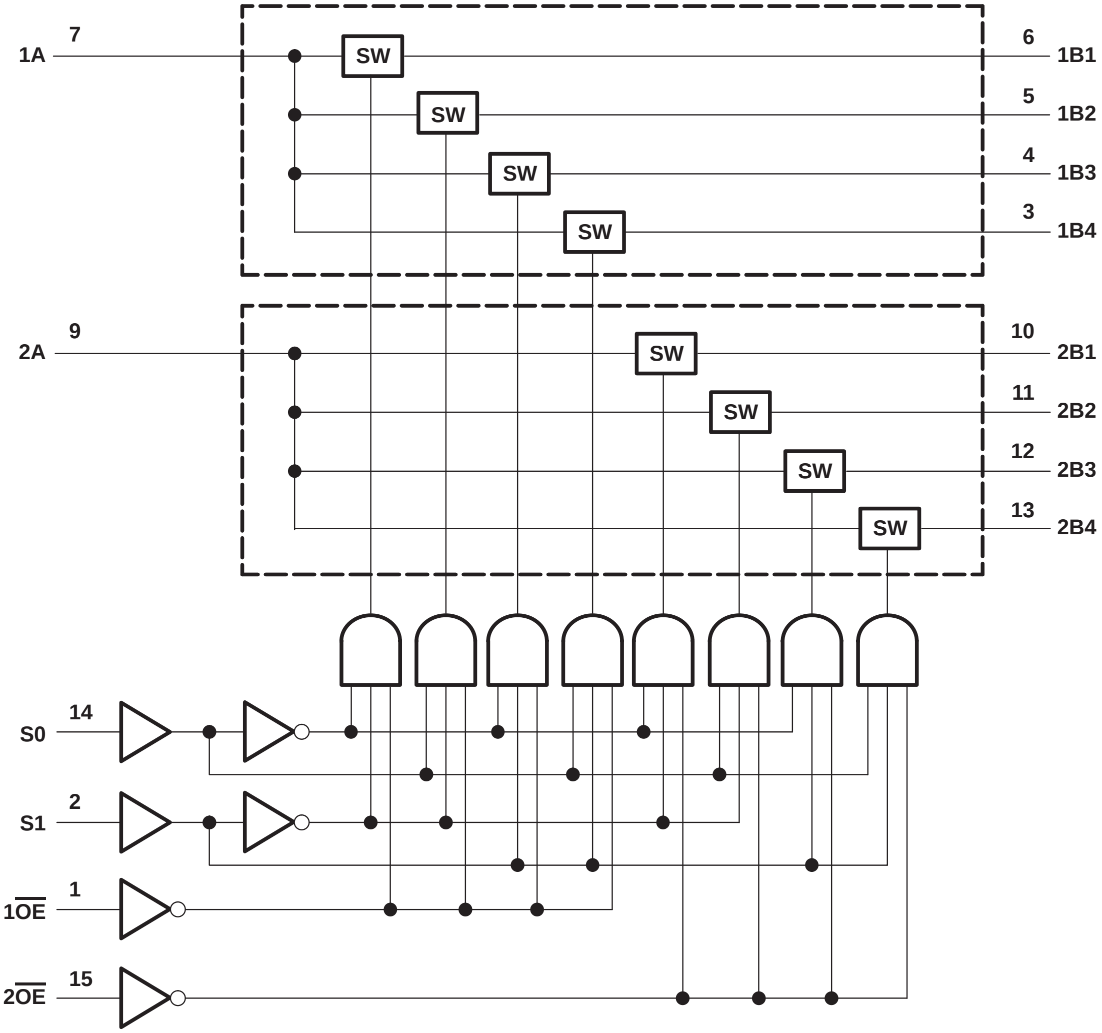
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBT3253CRGYR	CU253C
	SOIC − D	Tube	SN74CBT3253CD	CBT3253C
		Tape and reel	SN74CBT3253CDR	
	SSOP − DB	Tube	SN74CBT3253CDB	CU253C
		Tape and reel	SN74CBT3253CDBR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3253CDBQR	CBT3253C
	TSSOP − PW	Tube	SN74CBT3253CPW	CU253C
		Tape and reel	SN74CBT3253CPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

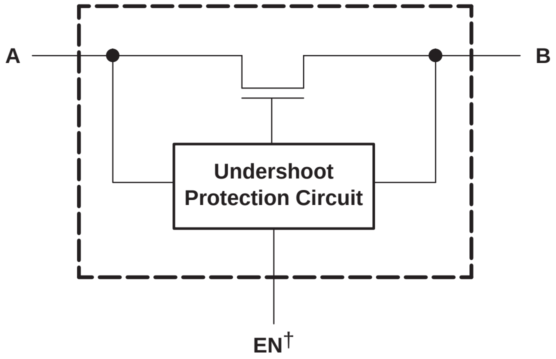
FUNCTION TABLE
(each multiplexer/demultiplexer)

INPUTS			INPUT/OUTPUT A	FUNCTION
$\overline{\mathrm{OE}}$	S1	S0		
L	L	L	B1	A port = B1 port
L	L	H	B2	A port = B2 port
L	H	L	B3	A port = B3 port
L	H	H	B4	A port = B4 port
H	X	X	Z	Disconnect

logic diagram (positive logic)


1A
7
SW
SW
SW
SW
6
1B1
5
1B2
4
1B3
3
1B4
2A
9
SW
SW
SW
SW
10
2B1
11
2B2
12
2B3
13
2B4
S0
14
S1
2
1OE
1
2OE
15

simplified schematic, each FET switch (SW)


A
B
Undershoot
Protection Circuit
EN†

† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)		−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)		−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)		±128 mA
Continuous current through V_{CC} or GND terminals		±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	D package	73°C/W
(see Note 5):	DB package	82°C/W
(see Note 5):	DBQ package	90°C/W
(see Note 5):	PW package	108°C/W
(see Note 6):	RGY package	39°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_{OZ}‡		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	μA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				3.5		pF
$C_{io(OFF)}$	A port	$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		14		pF
	B port					5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		22		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}#	A or B	B or A		0.24		0.15	ns
$t_{pd(s)}$	S	A		5.9	1.5	5.4	ns
t_{en}	S	B		6.2	1.5	5.8	ns
	$\overline{OE}$	A or B		5.7	1.5	5.3	
t_{dis}	S	B		6.2	1.5	5.8	ns
	$\overline{OE}$	A or B		5.7	1.5	5.3	

[#] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP[†]	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V, Switch OFF, $V_{IN} = V_{CC}$ or GND	2	V_{OH}−0.3		V

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

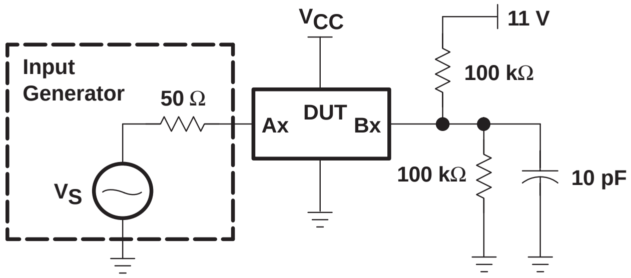

VCC
11 V
Input Generator
50 Ω
Ax
DUT
Bx
100 kΩ
100 kΩ
10 pF
VS

Figure 1. Device Test Setup

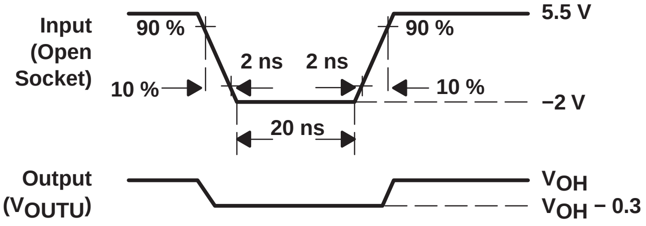
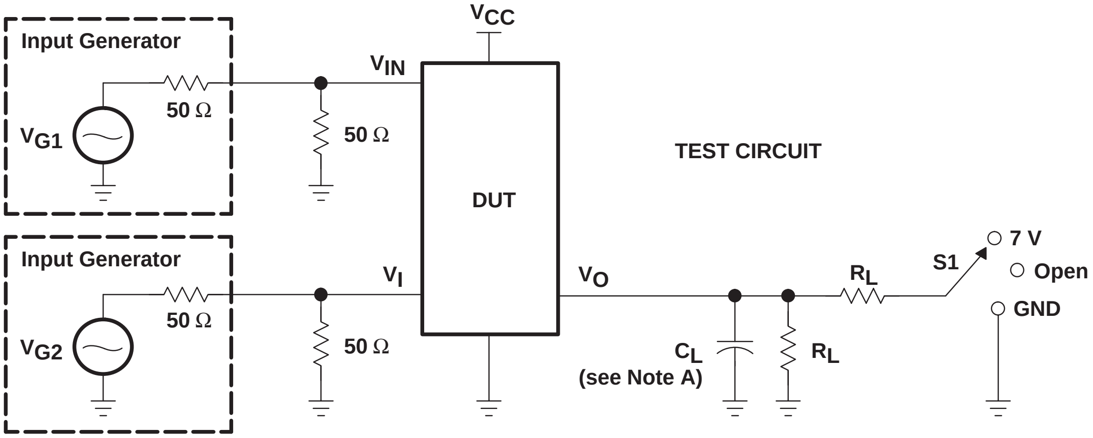
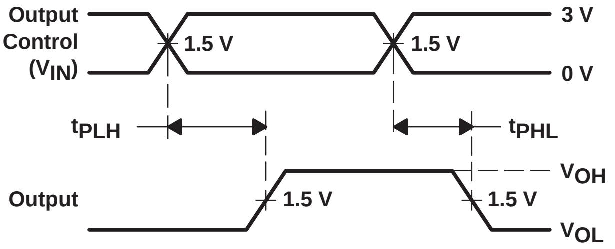

Input (Open Socket)
90 %
90 %
5.5 V
2 ns
2 ns
10 %
10 %
−2 V
20 ns
Output (VOUTU)
VOH
VOH − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

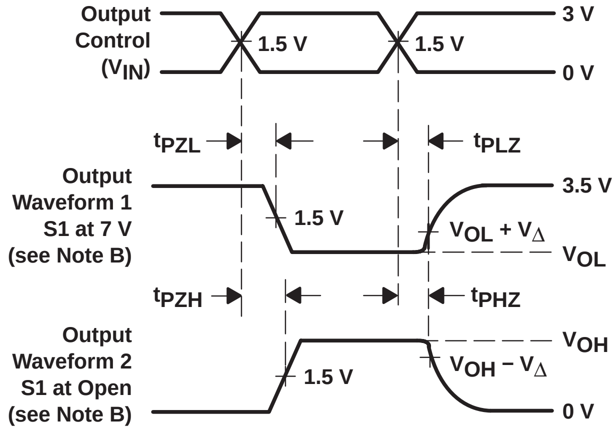
PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
50 Ω
V_{CC}
V_{IN}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
50 Ω
V_I
V_O
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output
Control
(V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)


Output
Control
(V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

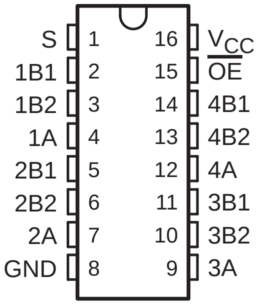
Figure 3. Test Circuit and Voltage Waveforms

SN74CBT3257C
4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

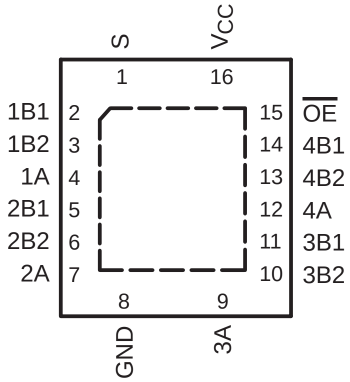
SCDS137 − OCTOBER 2003

- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports I^2C Bus Expansion**
- **Supports Both Digital and Analog Applications: USB Interface, Bus Isolation, Low-Distortion Signal Gating**

D, DB, DBQ, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBT3257CRGYR	CU257C
	SOIC − D	Tube	SN74CBT3257CD	CBT3257C
		Tape and reel	SN74CBT3257CDR	
	SSOP − DB	Tape and reel	SN74CBT3257CDBR	CU257C
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3257CDBQR	CU257C
	TSSOP − PW	Tube	SN74CBT3257CPW	CU257C
		Tape and reel	SN74CBT3257CPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The SN74CBT3257C is a high-speed TTL-compatible FET multiplexer/demultiplexer with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3257C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3257C is a 4-bit 1-of-2 multiplexer/demultiplexer with a single output-enable ($\overline{OE}$) input. The select (S) input controls the data path of the multiplexer/demultiplexer. When $\overline{OE}$ is low, the multiplexer/demultiplexer is enabled and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the multiplexer/demultiplexer is disabled and a high-impedance state exists between the A and B ports.

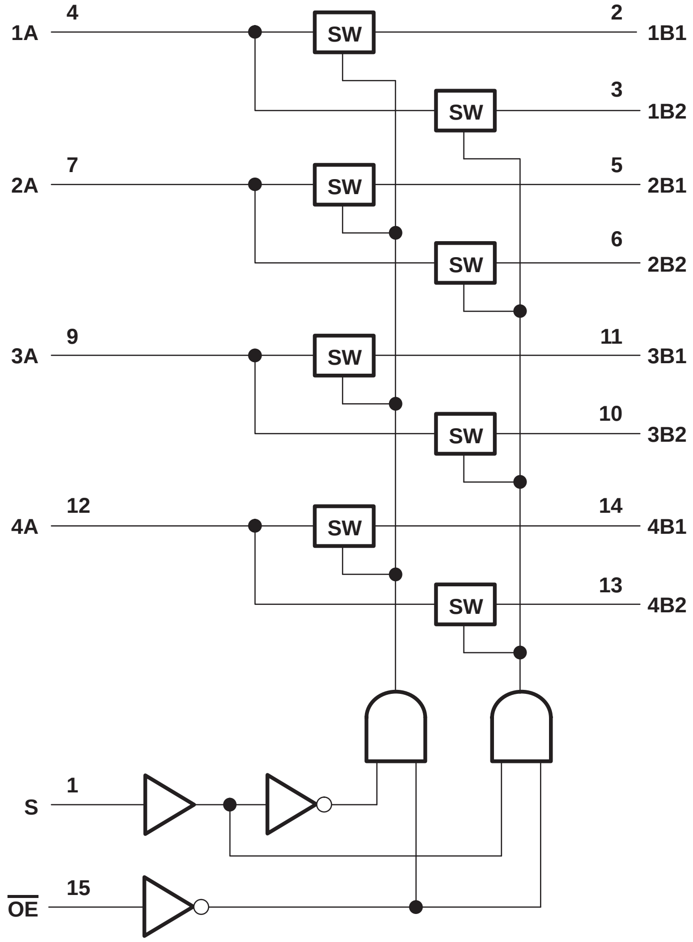
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

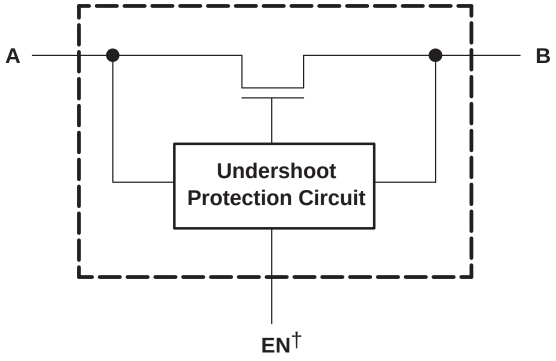
FUNCTION TABLE

INPUTS		INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S1		
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect

logic diagram (positive logic)


1A
4
SW
2
1B1
SW
3
1B2
2A
7
SW
5
2B1
SW
6
2B2
3A
9
SW
11
3B1
SW
10
3B2
4A
12
SW
14
4B1
SW
13
4B2
S
1
OE
15

simplified schematic, each FET switch (SW)


A
B
Undershoot
Protection Circuit
EN†

† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): D package	73°C/W
(see Note 5): DB package	82°C/W
(see Note 5): DBQ package	90°C/W
(see Note 5): PW package	108°C/W
(see Note 6): RGY package	39°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_{OZ}‡		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	μA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				3.5		pF
$C_{io(OFF)}$	A port	$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		8.5		pF
	B port					5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		16.5		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}#	A or B	B or A		0.24		0.15	ns
$t_{pd(s)}$	S	A		6	1.5	5.6	ns
t_{en}	S	B		6.3	1.5	5.8	ns
	$\overline{OE}$	A or B		6.3	1.5	5.8	
t_{dis}	S	B		6.5	1.5	6	ns
	$\overline{OE}$	A or B		5.9	1.5	5.9	

# The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V, Switch OFF, $V_{IN} = V_{CC}$ or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

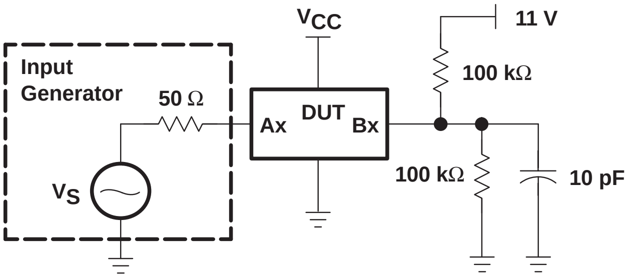

VCC
11 V
Input
Generator
50 Ω
Ax
DUT
Bx
100 kΩ
100 kΩ
10 pF
VS

Figure 1. Device Test Setup

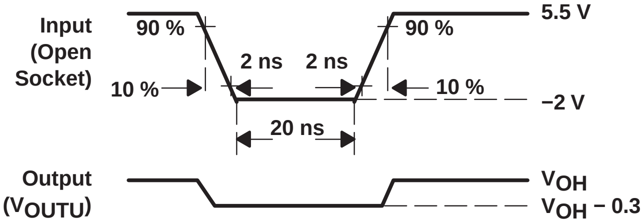
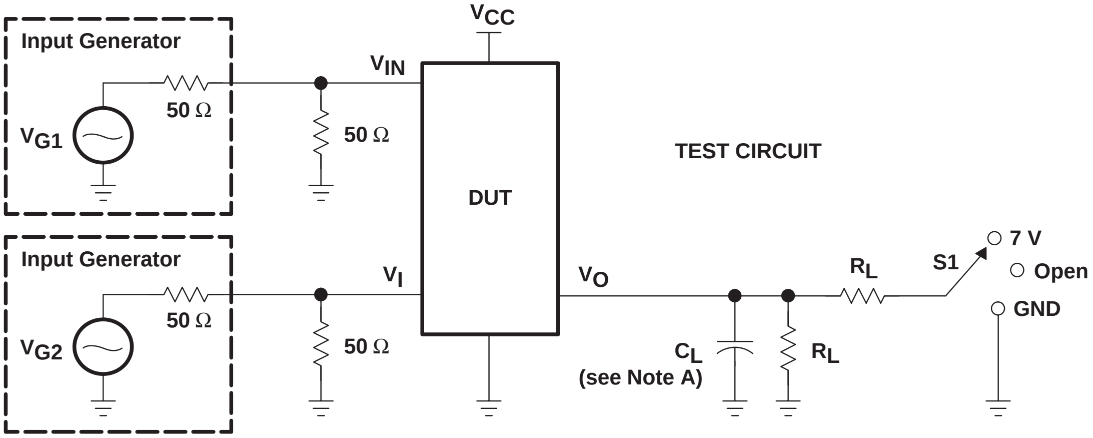
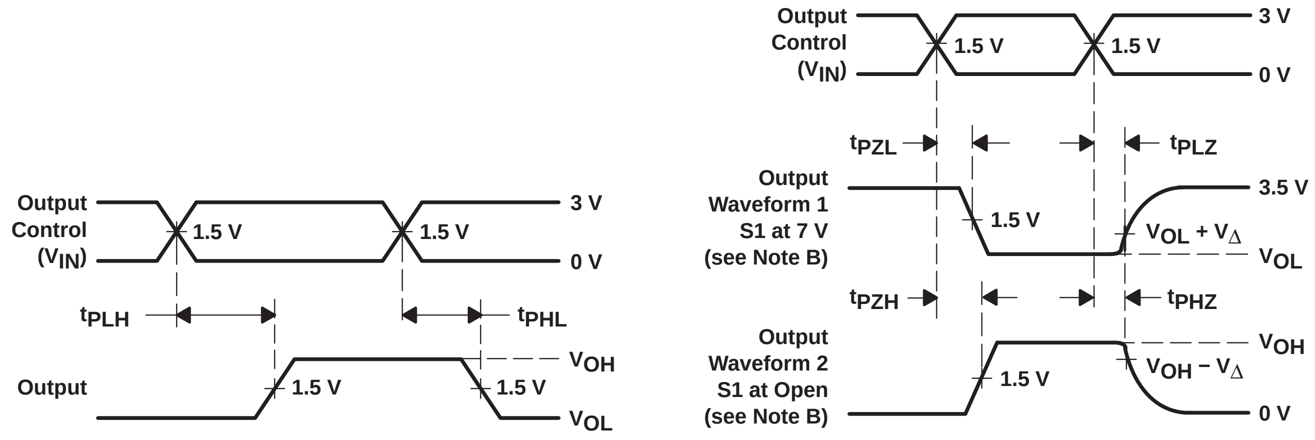

Input
(Open
Socket)
90 %
90 %
5.5 V
2 ns
2 ns
10 %
10 %
−2 V
20 ns
Output
(VOUTU)
VOH
VOH − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION


VCC
Input Generator
VG1
50 Ω
VIN
50 Ω
Input Generator
VG2
50 Ω
VI
50 Ω
DUT
TEST CIRCUIT
VO
CL
(see Note A)
RL
RL
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output Control (VIN)
1.5 V
1.5 V
3 V
0 V
tPLH
tPHL
Output
1.5 V
1.5 V
VOH
VOL
Output Control (VIN)
1.5 V
1.5 V
3 V
0 V
tPZL
tPLZ
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
VOL + VΔ
VOL
tPZH
tPHZ
Output Waveform 2 S1 at Open (see Note B)
1.5 V
VOH
VOH − VΔ
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

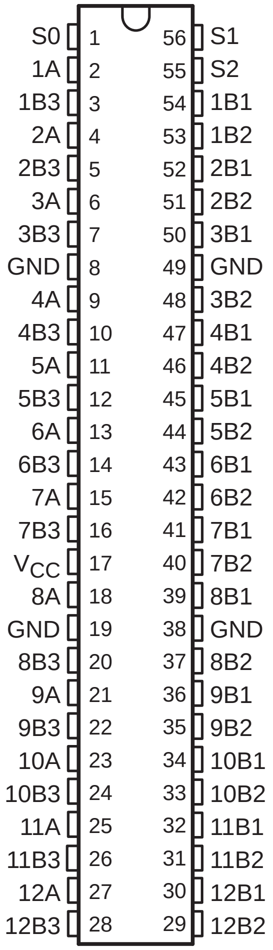
Figure 3. Test Circuit and Voltage Waveforms

SN74CBT16214C
12-BIT 1-OF-3 FET MULTIPLEXER/DEMULTIPLEXER 5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS121B − JUNE 2003 − REVISED OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics ($r_{on} = 3\ \Omega$ Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption ($I_{CC} = 3\ \mu A$ Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Bus Isolation, Low-Distortion Signal Gating**

DGG OR DL PACKAGE
(TOP VIEW)


S0 1 56 S1
1A 2 55 S2
1B3 3 54 1B1
2A 4 53 1B2
2B3 5 52 2B1
3A 6 51 2B2
3B3 7 50 3B1
GND 8 49 GND
4A 9 48 3B2
4B3 10 47 4B1
5A 11 46 4B2
5B3 12 45 5B1
6A 13 44 5B2
6B3 14 43 6B1
7A 15 42 6B2
7B3 16 41 7B1
VCC 17 40 7B2
8A 18 39 8B1
GND 19 38 GND
8B3 20 37 8B2
9A 21 36 9B1
9B3 22 35 9B2
10A 23 34 10B1
10B3 24 33 10B2
11A 25 32 11B1
11B3 26 31 11B2
12A 27 30 12B1
12B3 28 29 12B2

description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16214CDL	CBT16214C
		Tape and reel	SN74CBT16214CDLR	
	TSSOP − DGG	Tube	SN74CBT16214CDGG	CBT16214C
		Tape and reel	SN74CBT16214CDGGR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The SN74CBT16214C is a high-speed TTL-compatible FET multiplexer/demultiplexer with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16214C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT16214C is a 12-bit 1-of-3 multiplexer/demultiplexer. The select (S0, S1, S2) inputs control the data path of each multiplexer/demultiplexer. When the multiplexer/demultiplexer is enabled, the A port is connected to the B port, allowing bidirectional data flow between ports. When the multiplexer/demultiplexer is disabled, a high-impedance state exists between the A and B ports.

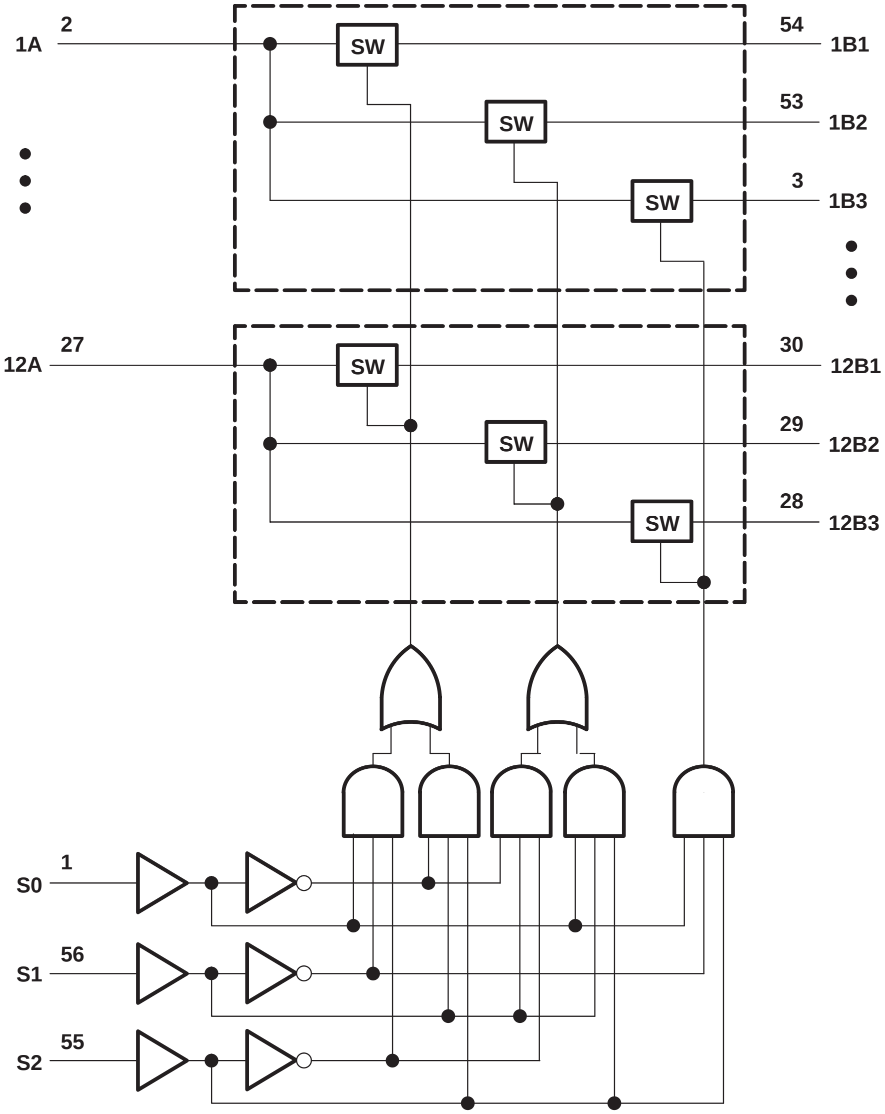
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, each select input should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

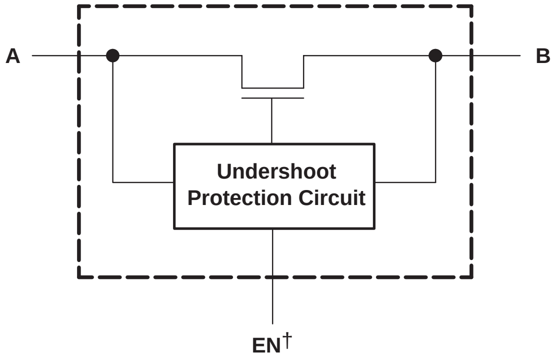
FUNCTION TABLE

INPUTS			INPUT/OUTPUT A	FUNCTION
S2	S1	S0		
L	L	L	Z	Disconnect
L	L	H	B1	A port = B1 port
L	H	L	B2	A port = B2 port
L	H	H	Z	Disconnect
H	L	L	Z	Disconnect
H	L	H	B3	A port = B3 port
H	H	L	B1	A port = B1 port
H	H	H	B2	A port = B2 port

logic diagram (positive logic)


1A
2
SW
54
1B1
SW
53
1B2
SW
3
1B3
12A
27
SW
30
12B1
SW
29
12B2
SW
28
12B3
S0
1
S1
56
S2
55

simplified schematic, each FET switch (SW)


A
B
Undershoot Protection Circuit
EN†

† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . −0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$) . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$) . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . ±128 mA
Continuous current through V_{CC} or GND terminals . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DGG package . . . . 64°C/W
DL package . . . . 56°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_{OZ}‡		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	μA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				3.5		pF
$C_{io(OFF)}$	A port	$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		10		pF
	B port					5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		18		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}#	A or B	B or A		0.24		0.15	ns
$t_{pd(s)}$	S	A		6.7	1.5	6.3	ns
t_{en}	S	B		7.2	1.5	6.6	ns
t_{dis}	S	B		7.5	1.5	7.3	ns

# The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V,	Switch OFF,	V_{IN} = V_{CC} or GND	2	V_{OH}−0.3		V

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

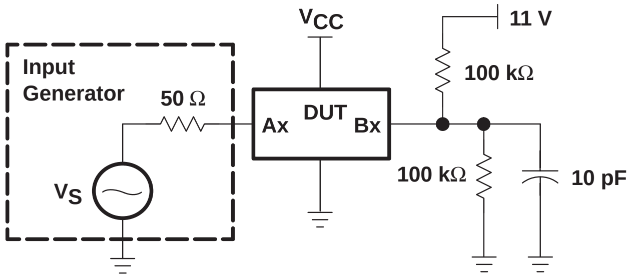

VCC
11 V
Input
Generator
50 Ω
DUT
Ax
Bx
100 kΩ
100 kΩ
10 pF
VS

Figure 1. Device Test Setup

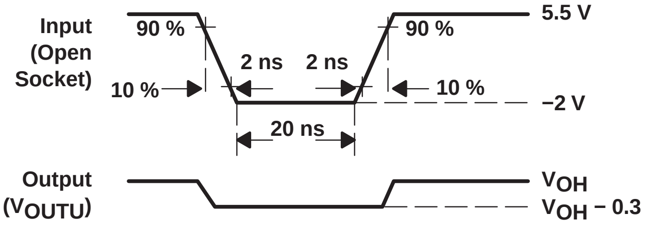
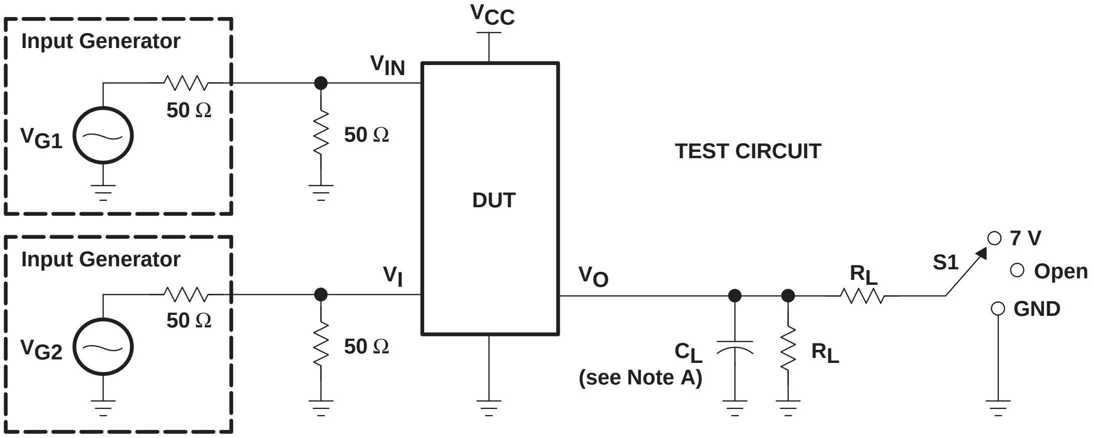
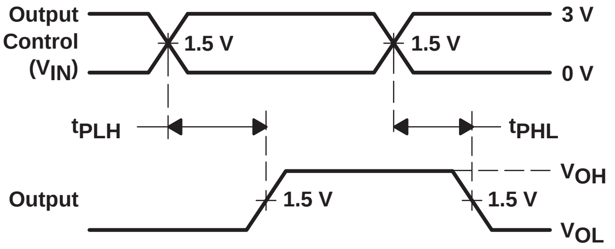

Input
(Open
Socket)
90 %
90 %
5.5 V
2 ns
2 ns
10 %
10 %
−2 V
20 ns
Output
(VOUTU)
VOH
VOH − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

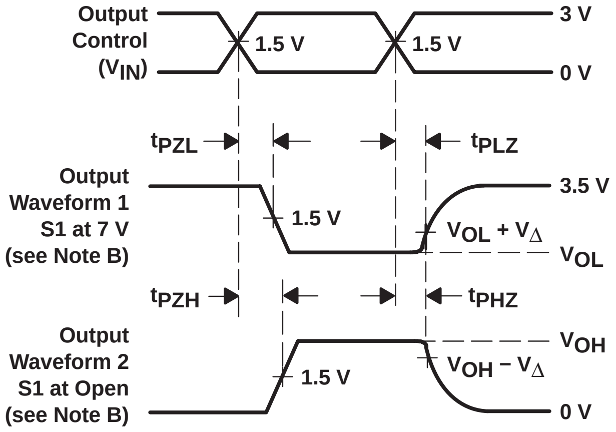
PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

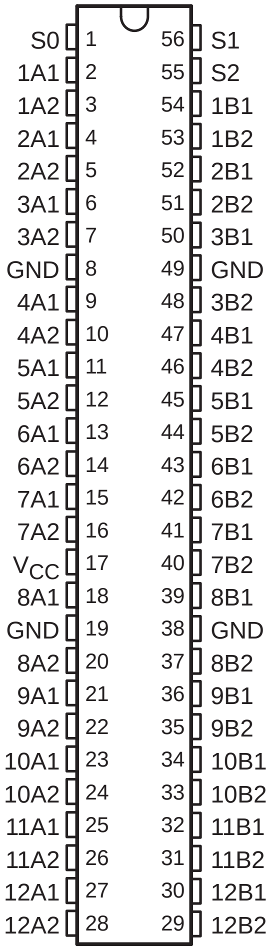
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

- **Member of the Texas Instruments Widebus™ Family**
- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 8 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 5 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


S0 1 56 S1
1A1 2 55 S2
1A2 3 54 1B1
2A1 4 53 1B2
2A2 5 52 2B1
3A1 6 51 2B2
3A2 7 50 3B1
GND 8 49 GND
4A1 9 48 3B2
4A2 10 47 4B1
5A1 11 46 4B2
5A2 12 45 5B1
6A1 13 44 5B2
6A2 14 43 6B1
7A1 15 42 6B2
7A2 16 41 7B1
VCC 17 40 7B2
8A1 18 39 8B1
GND 19 38 GND
8A2 20 37 8B2
9A1 21 36 9B1
9A2 22 35 9B2
10A1 23 34 10B1
10A2 24 33 10B2
11A1 25 32 11B1
11A2 26 31 11B2
12A1 27 30 12B1
12A2 28 29 12B2

description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16212CDL	CBT16212C
		Tape and reel	SN74CBT16212CDLR	
	TSSOP − DGG	Tube	SN74CBT16212CDGG	CBT16212C
		Tape and reel	SN74CBT16212CDGGR	
	TVSOP − DGV	Tape and reel	SN74CBT16212CDGVR	CY212C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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description/ordering information (continued)

The SN74CBT16212C is a high-speed TTL-compatible FET bus-exchange switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16212C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT16212C operates as a 24-bit bus switch, or as a 12-bit bus-exchange that provides data exchanging between four signal ports. The select (S0, S1, S2) inputs control the data path of the bus-exchange switch. When the bus-exchange switch is ON, the A port is connected to the B port, allowing bidirectional data flow between ports. When the bus-exchange switch is disabled, a high-impedance state exists between the A and B ports.

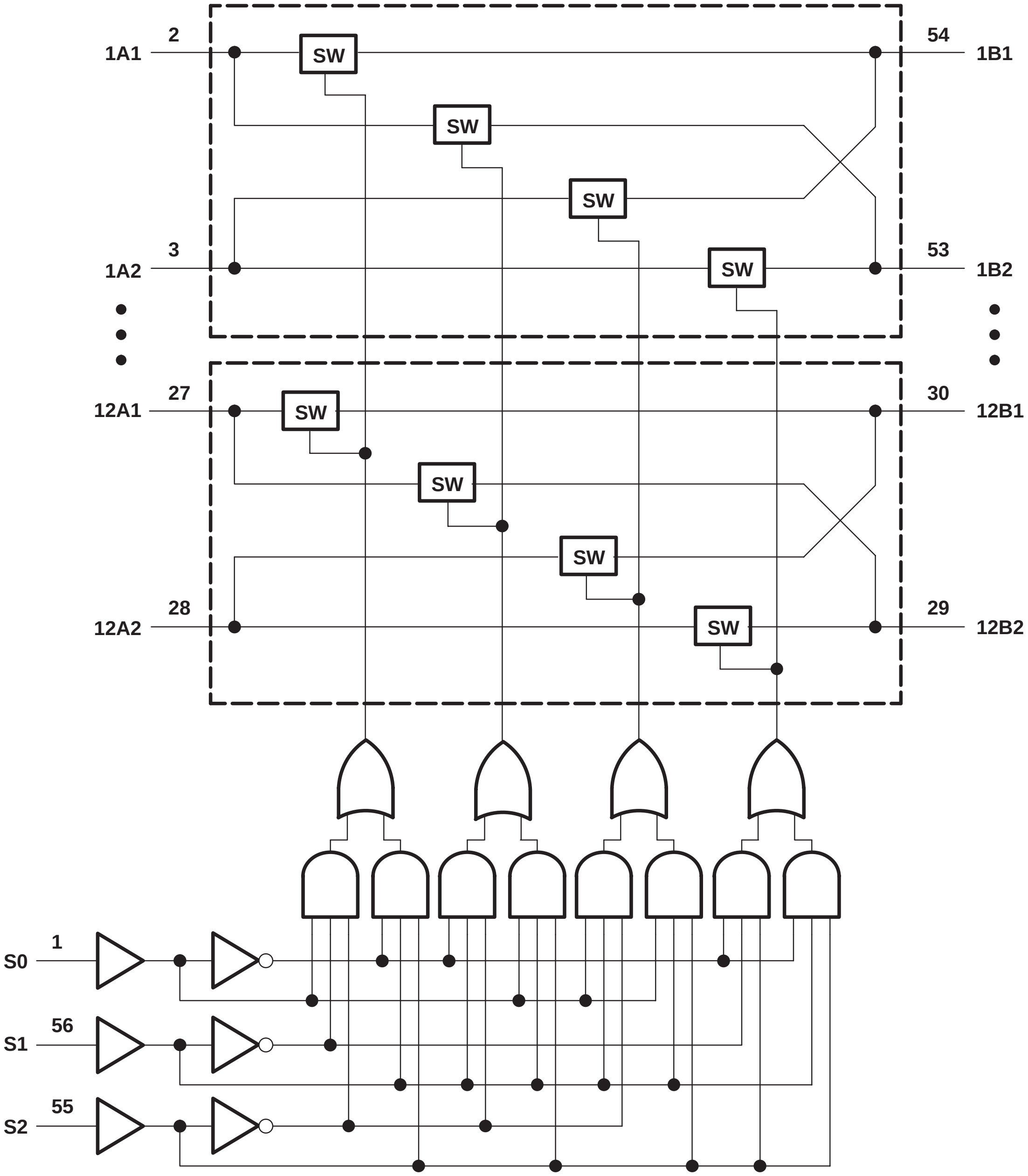
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, each select input should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

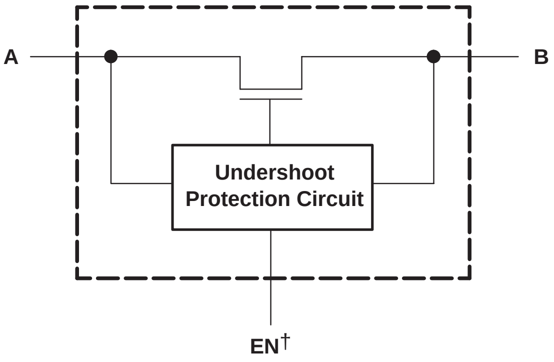
FUNCTION TABLE
(each 12-bit bus-exchange)

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	S1	S0	A1	A2	
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 port = B1 port
L	H	L	B2	Z	A1 port = B2 port
L	H	H	Z	B1	A2 port = B1 port
H	L	L	Z	B2	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 port = B1 port A2 port = B2 port
H	H	H	B2	B1	A1 port = B2 port A2 port = B1 port

logic diagram (positive logic)


1A1
2
SW
54
1B1
SW
SW
1A2
3
SW
53
1B2
12A1
27
SW
30
12B1
SW
SW
12A2
28
SW
29
12B2
S0
1
S1
56
S2
55

simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	−0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	−50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	−50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DGG package	64°C/W
DGV package	48°C/W
DL package	56°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_{OZ}[‡]		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			5	μA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				3.5		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		8		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		19		pF
r_{on}[¶]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	
				I_O = 30 mA		3	6	
			V_I = 2.4 V,	I_O = −15 mA		5	10	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[#]	A or B	B or A		0.24		0.15	ns
$t_{pd(s)}$	S	A		6.6	1.5	5.9	ns
t_{en}	S	B		7	1.5	6.8	ns
t_{dis}	S	B		7.4	1.5	7.2	ns

[#] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V,	Switch OFF,	$V_{IN} = V_{CC}$ or GND	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

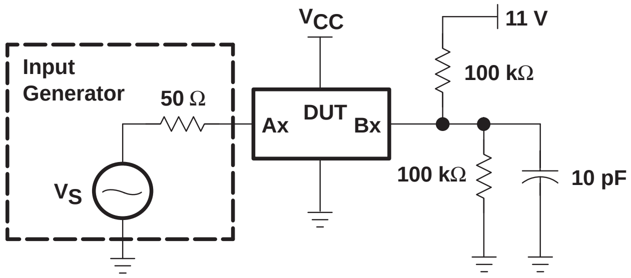

VCC
11 V
Input Generator
50 Ω
DUT
Ax
Bx
100 kΩ
100 kΩ
10 pF
VS

Figure 1. Device Test Setup

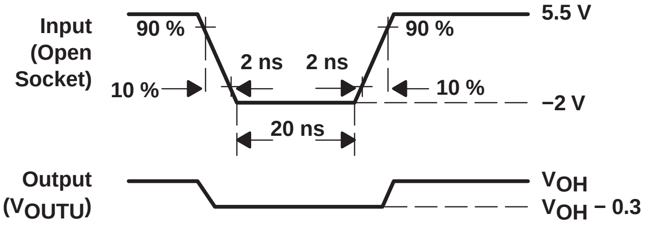
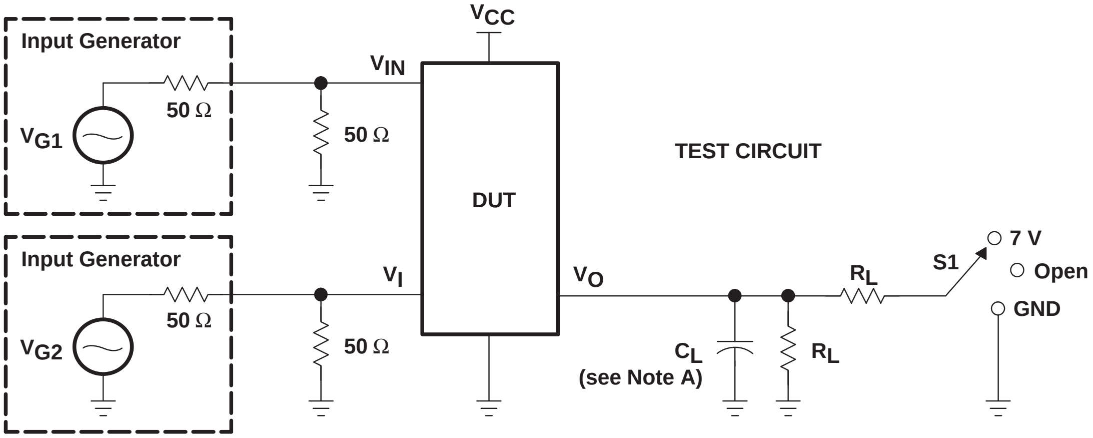
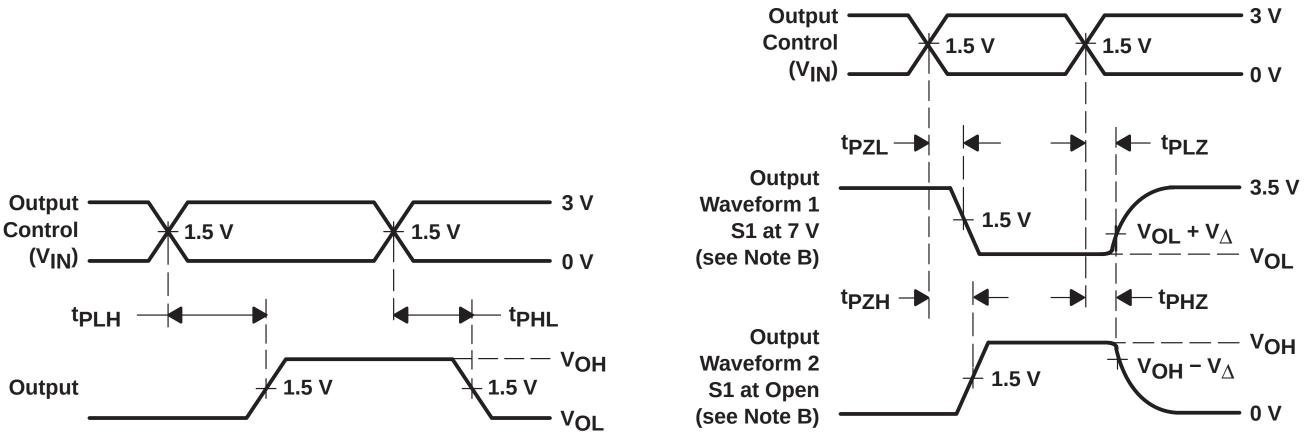

Input (Open Socket)
90 %
90 %
5.5 V
2 ns
2 ns
10 %
10 %
−2 V
20 ns
Output (VOUTU)
VOH
VOH − 0.3

Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION


Input Generator
V_{G1}
50 Ω
V_{IN}
50 Ω
V_{CC}
DUT
TEST CIRCUIT
Input Generator
V_{G2}
50 Ω
V_I
50 Ω
V_O
C_L
(see Note A)
R_L
R_L
S1
7 V
Open
GND

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V


Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
Output Control (V_{IN})
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
$V_{OH} - V_\Delta$
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

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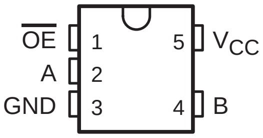
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

DBV OR DCK PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBT1G125 features a single high-speed line switch. The switch is disabled when the output-enable ($\overline{OE}$) input is high.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	SOT (SOT-23) − DBV	Reel of 3000	SN74CBT1G125DBVR	S25_
		Reel of 250	SN74CBT1G125DBVT	
	SOT (SC-70) − DCK	Reel of 3000	SN74CBT1G125DCKR	SM_
		Reel of 250	SN74CBT1G125DCKT	

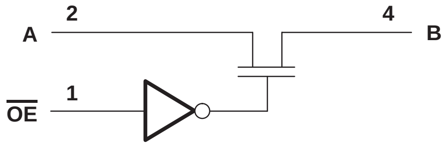
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DBV package	206°C/W
	DCK package	252°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP[‡]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA					−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND					±1	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND				1	μA
C_i	Control input	V_I = 3 V or 0					3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}				4		pF
r_{on}[§]		V_{CC} = 4 V,	TYP at V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA			5	7	
				I_I = 30 mA			5	7	
			V_I = 2.4 V,	I_I = 15 mA			10	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

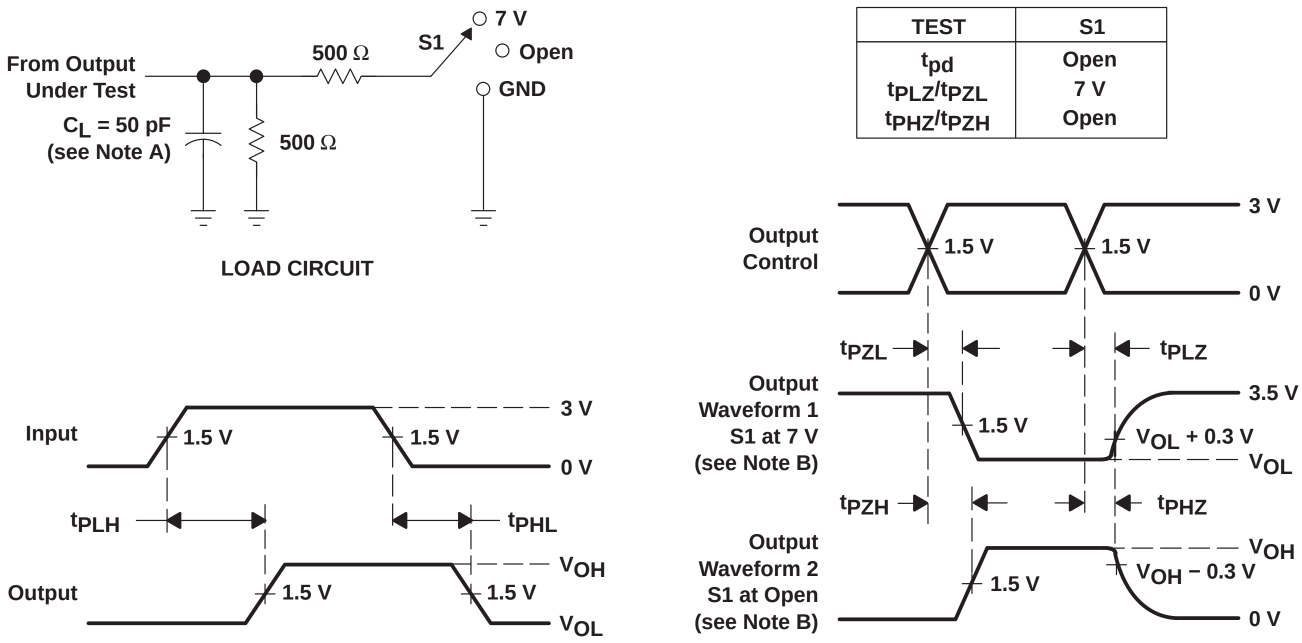
[§] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		5.5	1.6	4.9	ns
t_{dis}	$\overline{OE}$	A or B		4.5	1	4.2	ns

[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND
Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

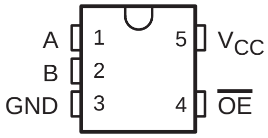
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**

DBV OR DCK PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBT1G384 features a single high-speed line switch. The switch is disabled when the output-enable ($\overline{OE}$) input is high.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[‡]
−40°C to 85°C	SOT (SOT-23) − DBV	Reel of 3000	SN74CBT1G384DBVR	S8D_
		Reel of 250	SN74CBT1G384DBVT	
	SOT (SC-70) − DCK	Reel of 3000	SN74CBT1G384DCKR	S8_
		Reel of 250	SN74CBT1G384DCKT	

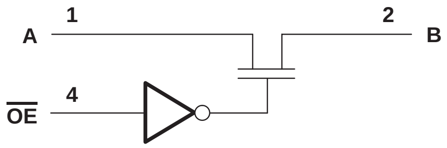
[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

[‡] The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DBV package	206°C/W
	DCK package	252°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA					−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND					±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND				1	µA
C_i	Control input	V_I = 3 V or 0					3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}				4		pF
r_{on}§		V_{CC} = 4 V,	TYP at V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA			5	7	
				I_I = 30 mA			5	7	
			V_I = 2.4 V,	I_I = 15 mA			10	15	

‡ All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

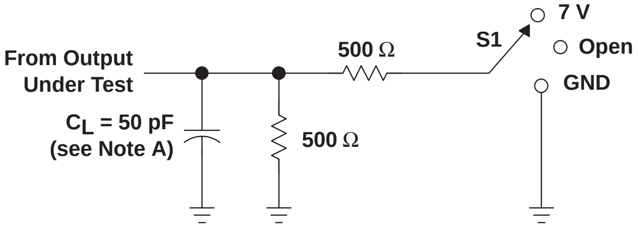
§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		5.5	1.6	4.9	ns
t_{dis}	$\overline{OE}$	A or B		4.5	1	4.2	ns

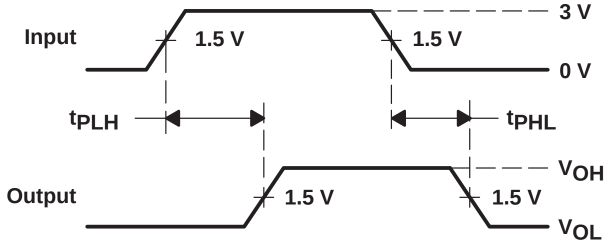
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

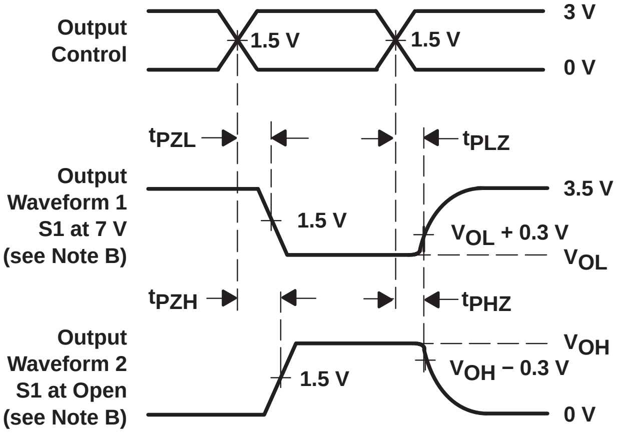

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The output is measured with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

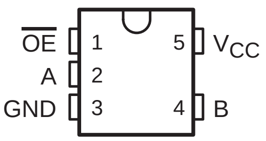
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTD1G125
SINGLE FET BUS SWITCH
WITH LEVEL SHIFTING

SCDS063K − JULY 1998 − REVISED JANUARY 2003

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

DBV OR DCK PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBTD1G125 features a single high-speed line switch. The switch is disabled when the output-enable ($\overline{OE}$) input is high. A diode to V_{CC} is integrated on the chip to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	SOT (SOT-23) − DBV	Reel of 3000	SN74CBTD1G125DBVR	P25_
		Reel of 250	SN74CBTD1G125DBVT	
	SOT (SC-70) − DCK	Reel of 3000	SN74CBTD1G125DCKR	PM_
		Reel of 250	SN74CBTD1G125DCKT	

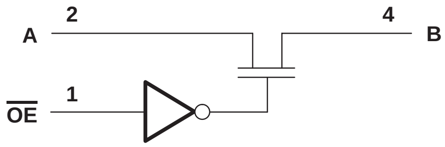
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DBV package	206°C/W
	DCK package	252°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}		See Figure 2						
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1.5	mA
ΔI_{CC}§	Control input	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control input	V_I = 3 V or 0				2		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			3.5		pF
r_{on}¶		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		35	50	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

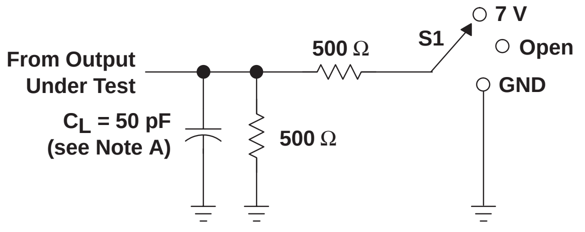
¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}[†]	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B	2	5.9	ns
t_{dis}	$\overline{OE}$	A or B	1	4.7	ns

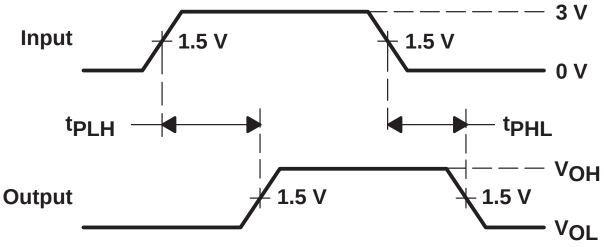
[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

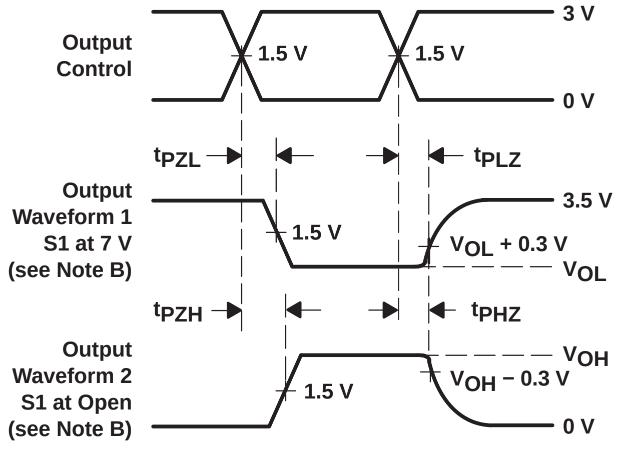

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

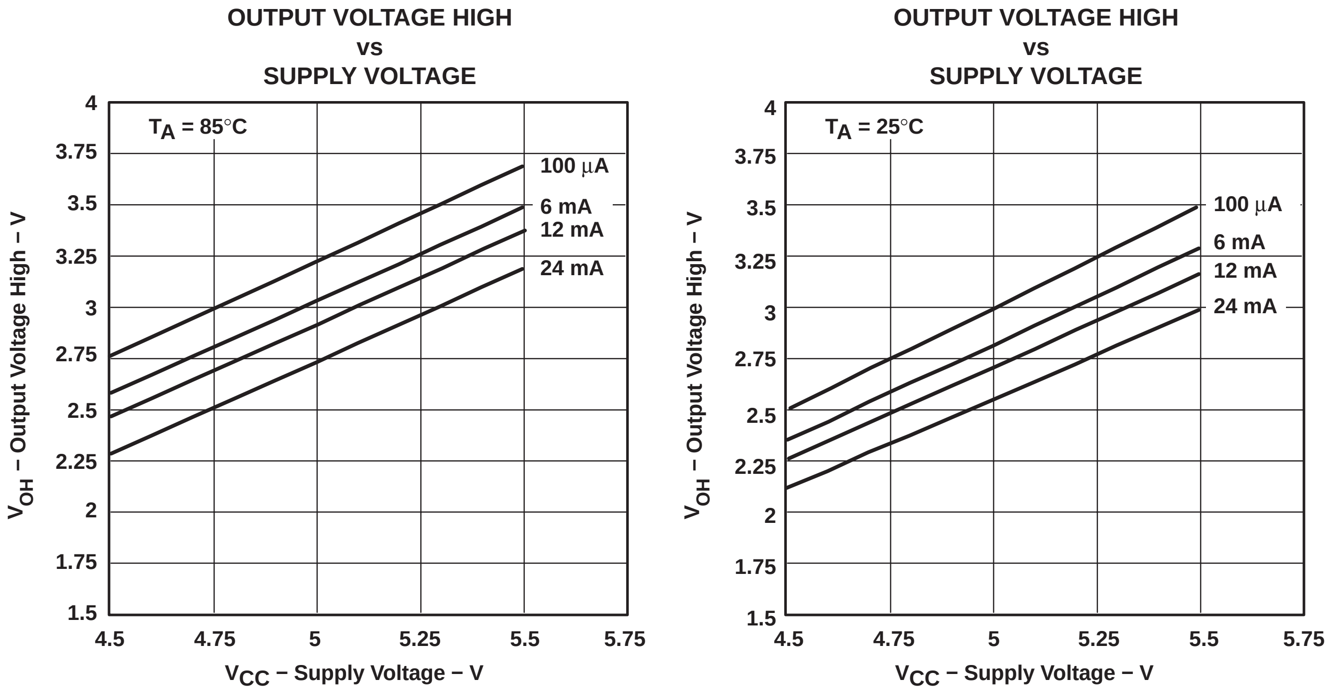

Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



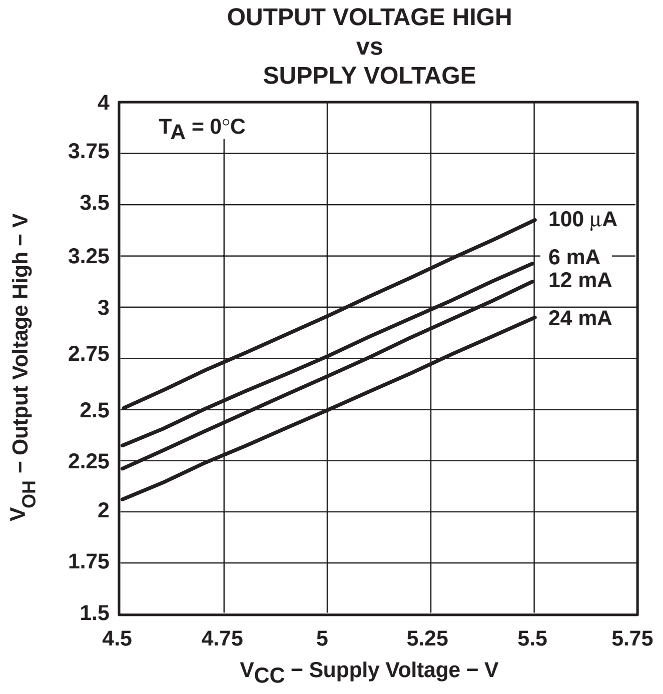


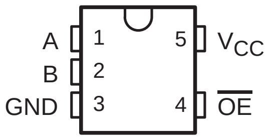
Figure 2. V_{OH} Values

SN74CBTD1G384
SINGLE FET BUS SWITCH
WITH LEVEL SHIFTING

SCDS066J − JULY 1998 − REVISED JANUARY 2003

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DBV OR DCK PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBTD1G384 features a single high-speed line switch. The switch is disabled when the output-enable ($\overline{\text{OE}}$) input is high. A diode to V_{CC} is integrated on the chip to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	SOT (SOT-23) − DBV	Reel of 3000	SN74CBTD1G384DBVR	P8D_
		Reel of 250	SN74CBTD1G384DBVT	
	SOT (SC-70) − DCK	Reel of 3000	SN74CBTD1G384DCKR	P8_
		Reel of 250	SN74CBTD1G384DCKT	

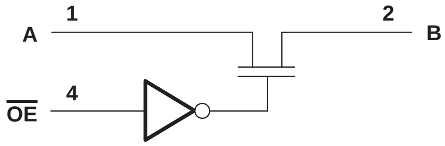
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[‡]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}		See Figure 2						
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1.5	mA
ΔI_{CC}[§]	Control input	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control input	V_I = 3 V or 0				2		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			3.5		pF
r_{on}[¶]		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		35	50	

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

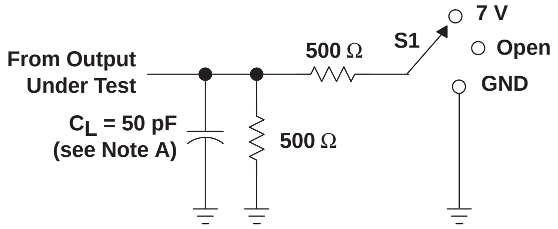
[¶] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}†	A or B	B or A		0.25	ns
t_{en}	$\overline{\text{OE}}$	A or B	2	5.9	ns
t_{dis}	$\overline{\text{OE}}$	A or B	1	4.7	ns

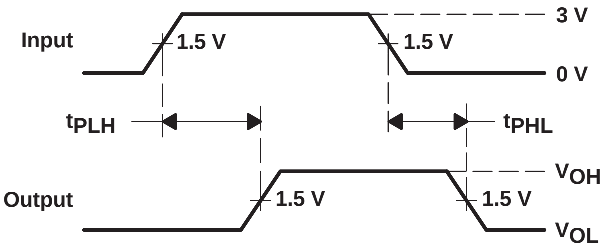
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

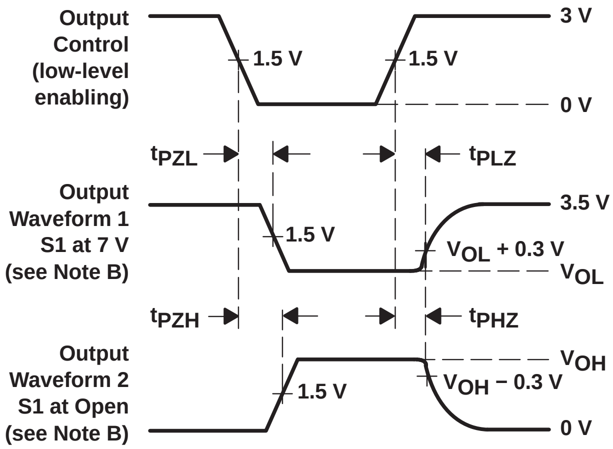

From Output Under Test
C_L = 50 pF (see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

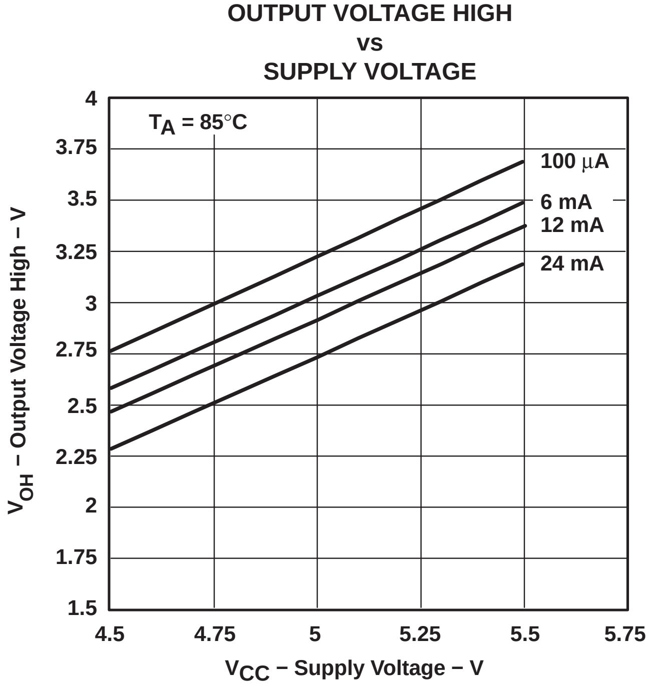

Output Control (low-level enabling)
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

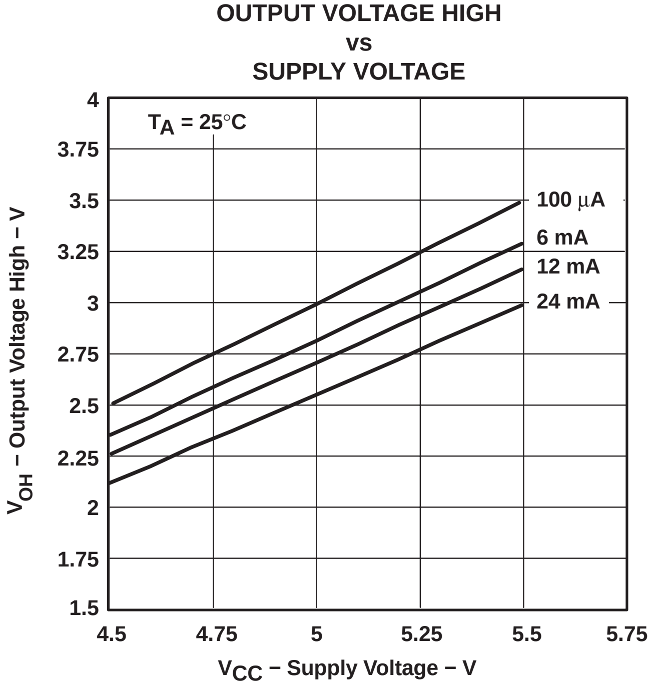
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The output is measured with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS





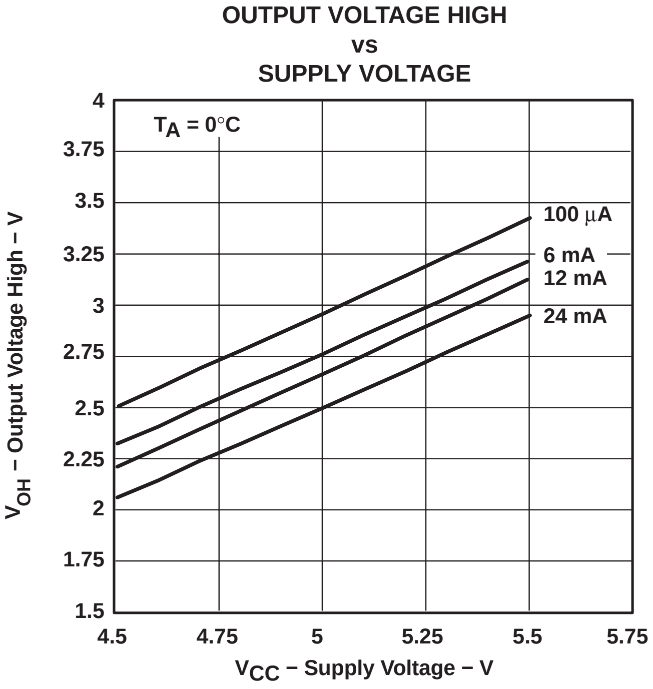
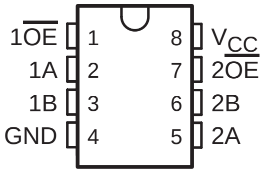


Figure 2. V_{OH} Values

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

**D OR PW PACKAGE
(TOP VIEW)**



description

The SN74CBT3306 dual FET bus switch features independent line switches. Each switch is disabled when the associated output-enable ($\overline{\mathrm{OE}}$) input is high.

ORDERING INFORMATION

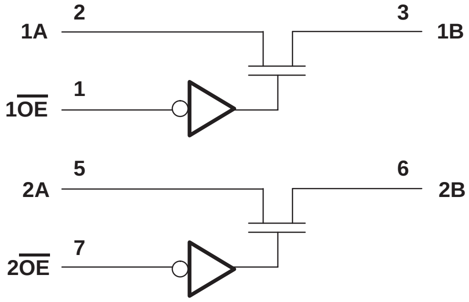
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − D	Tube	SN74CBT3306D	CU306
		Tape and reel	SN74CBT3306DR	
	TSSOP − PW	Tape and reel	SN74CBT3306PWR	CU306

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE
(each bus switch)**

INPUT $\overline{\mathrm{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_K ($V_{I/O}$ < 0)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	D package	97°C/W
	PW package	149°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			4		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

‡ All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

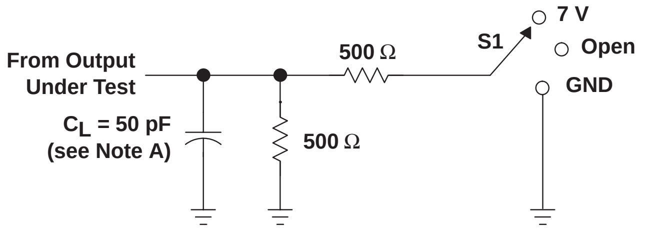
¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		5.6	1.8	5	ns
t_{dis}	$\overline{OE}$	A or B		4.6	1	4.3	ns

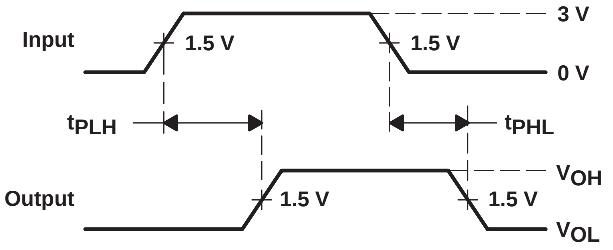
[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

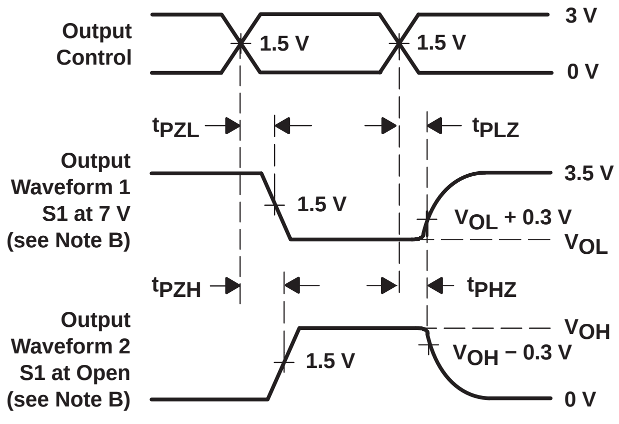

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

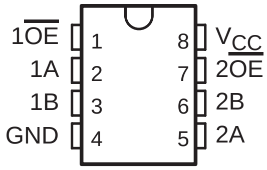
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTD3306
DUAL FET BUS SWITCH WITH LEVEL SHIFTING

SCDS030K − JANUARY 1996 − REVISED JULY 2002

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Designed to Be Used in Level-Shifting Applications**

D OR PW PACKAGE (TOP VIEW)



description/ordering information

The SN74CBTD3306 features two independent line switches. Each switch is disabled when the associated output-enable ($\overline{OE}$) input is high. A diode to V_{CC} is integrated on the chip to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

ORDERING INFORMATION

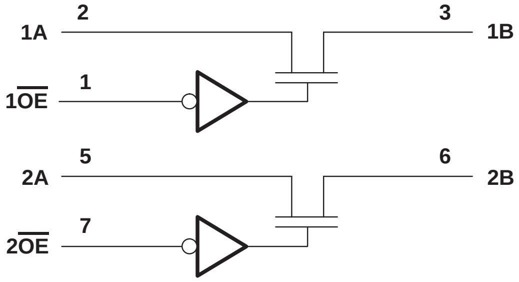
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − D	Tube	SN74CBTD3306D	CC306
		Tape and reel	SN74CBTD3306DR	
	TSSOP − PW	Tape and reel	SN74CBTD3306PWR	CC306

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	D package	97°C/W
	PW package	149°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}		See Figure 2						
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	$V_I = V_{CC}$ or GND			1.5	mA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE} = V_{CC}$			4		pF
r_{on}¶		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		35	50	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

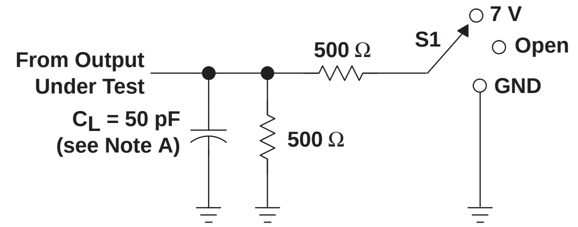
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}†	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B	2.1	5.4	ns
t_{dis}	$\overline{OE}$	A or B	1	4.7	ns

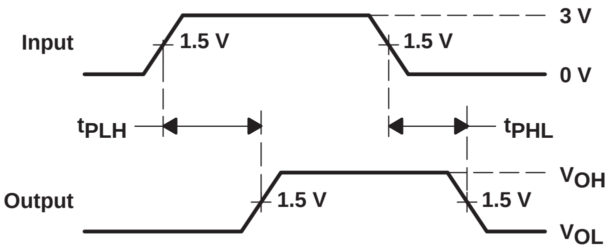
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

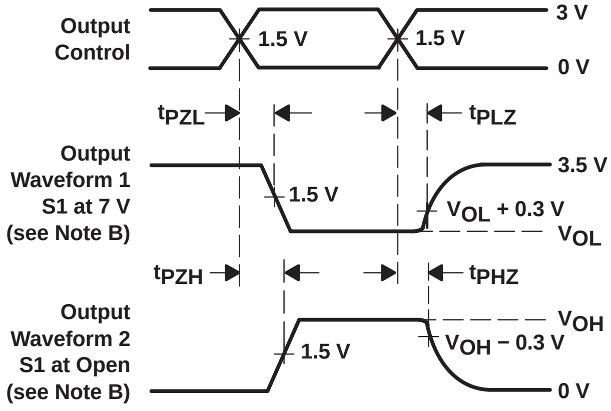

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

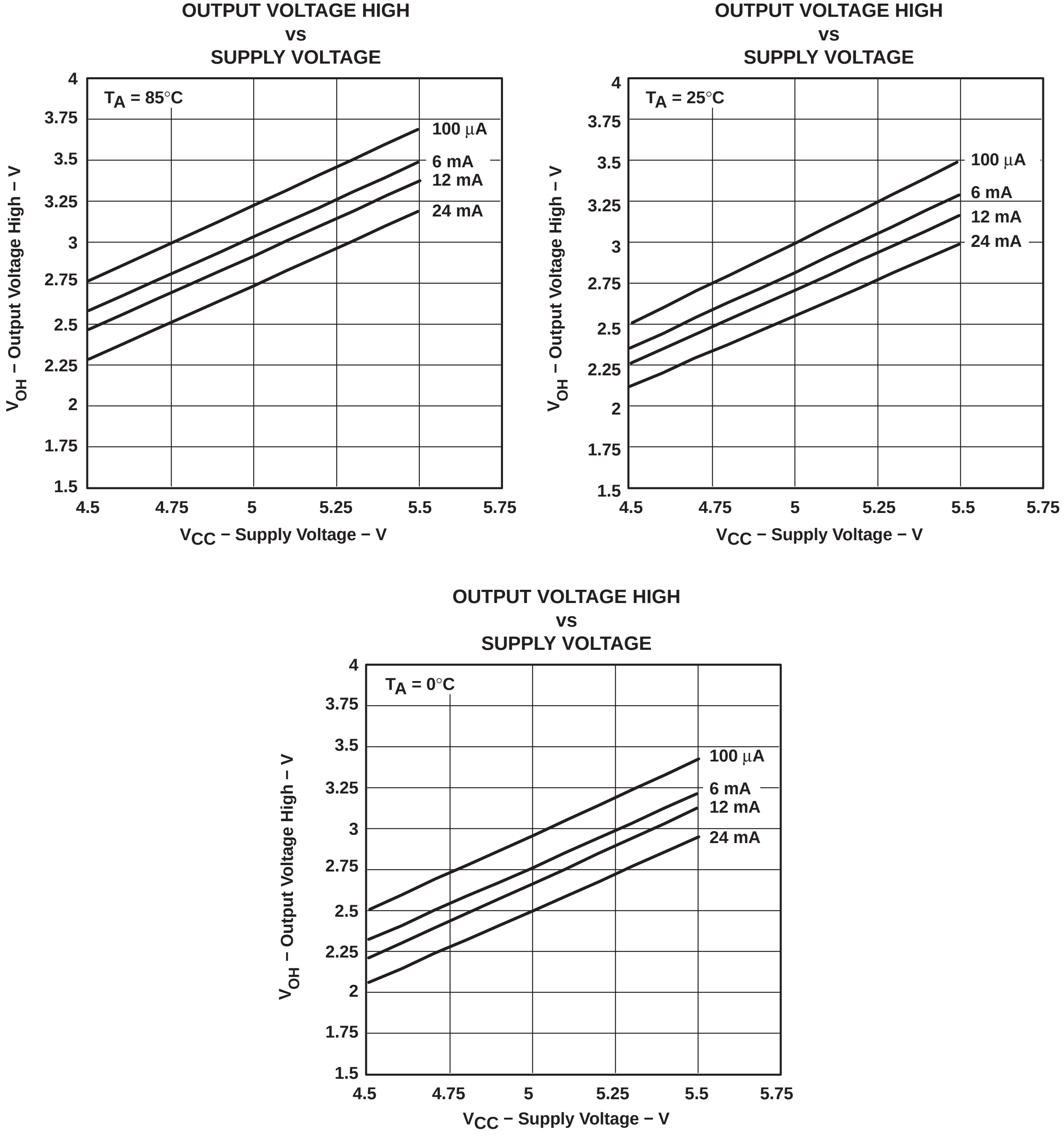


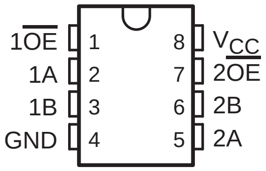
Figure 2. V_{OH} Values

SN74CBTS3306
DUAL FET BUS SWITCH
WITH SCHOTTKY DIODE CLAMPING

SCDS029H − JANUARY 1996 − REVISED NOVEMBER 2001

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

D OR PW PACKAGE
(TOP VIEW)



description

The SN74CBTS3306 features independent line switches with Schottky diodes on the I/Os to clamp undershoot. Each switch is disabled when the associated output-enable ($\overline{\text{OE}}$) input is high.

ORDERING INFORMATION

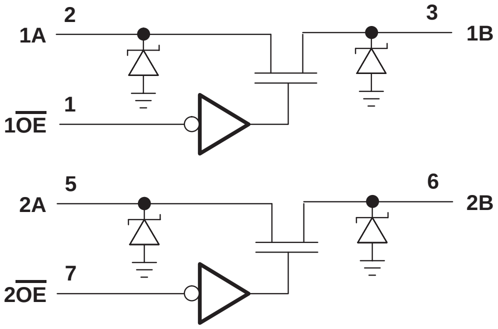
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − D	Tube	SN74CBTS3306D	CR306
		Tape and reel	SN74CBTS3306DR	
	TSSOP − PW	Tape and reel	SN74CBTS3306PWR	CR306

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each bus switch)

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	D package	97°C/W
	PW package	149°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[‡]	MAX	UNIT
V_{IK}	A or B inputs	V_{CC} = 4.5 V,	I_I = −18 mA				−0.7	V
	Control inputs						−1.2	
I_I	I_{IL}	V_{CC} = 5.5 V,	V_I = GND				−1	µA
	I_{IH}	V_{CC} = 5.5 V,	V_I = 5.5 V				150	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6		pF
r_{on}[¶]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

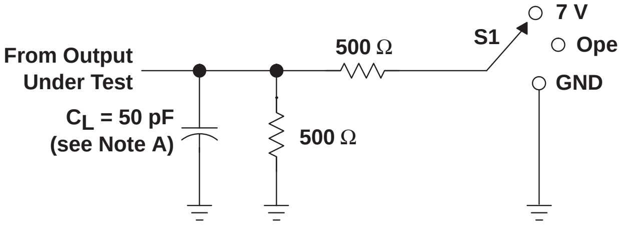
[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
[¶] Measured by the voltage drop between the A and B pin at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) pins.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		5.6	1.8	5	ns
t_{dis}	$\overline{OE}$	A or B		4.6	1	4.3	ns

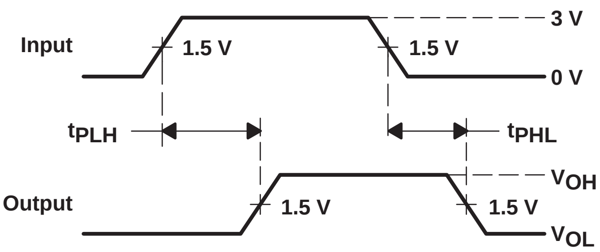
[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

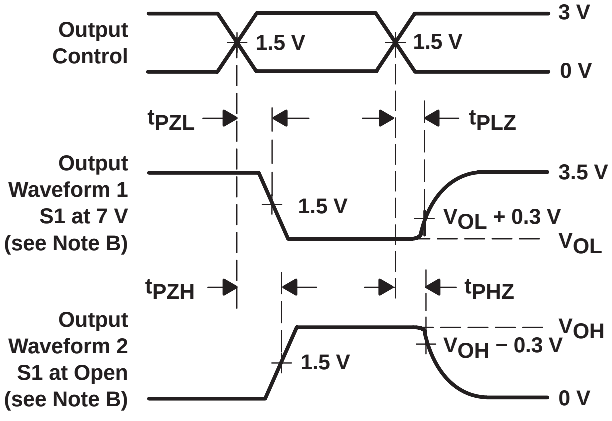

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	0pen


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

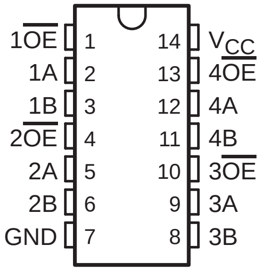
Figure 1. Load Circuit and Voltage Waveforms

SN74CBT3125
QUADRUPLE FET BUS SWITCH

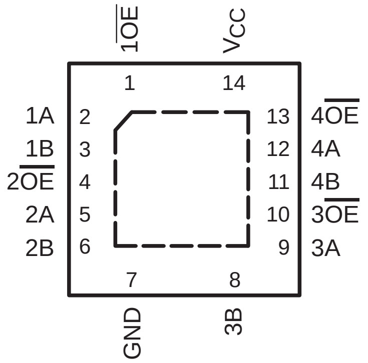
SCDS021I − MAY 1995 − REVISED SEPTEMBER 2002

- **Standard ’125-Type Pinout (D, DB, DGV, and PW Packages)**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

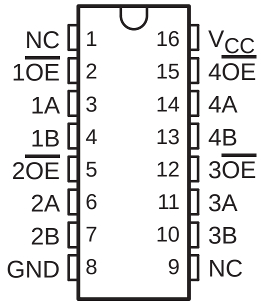
D, DB, DGV, OR PW PACKAGE
(TOP VIEW)


1$\overline{\text{OE}}$ 1 14 V_{CC}
1A 2 13 4$\overline{\text{OE}}$
1B 3 12 4A
2$\overline{\text{OE}}$ 4 11 4B
2A 5 10 3$\overline{\text{OE}}$
2B 6 9 3A
GND 7 8 3B

RGY PACKAGE
(TOP VIEW)


1$\overline{\text{OE}}$
V_{CC}
1 14
1A 2 13 4$\overline{\text{OE}}$
1B 3 12 4A
2$\overline{\text{OE}}$ 4 11 4B
2A 5 10 3$\overline{\text{OE}}$
2B 6 9 3A
7 8
GND
3B

DBQ PACKAGE
(TOP VIEW)


NC 1 16 V_{CC}
1$\overline{\text{OE}}$ 2 15 4$\overline{\text{OE}}$
1A 3 14 4A
1B 4 13 4B
2$\overline{\text{OE}}$ 5 12 3$\overline{\text{OE}}$
2A 6 11 3A
2B 7 10 3B
GND 8 9 NC

NC − No internal connection

description/ordering information

The SN74CBT3125 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable ($\overline{\text{OE}}$) input is high.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBT3125RGYR	CU125
	SOIC − D	Tube	SN74CBT3125D	CBT3125
		Tape and reel	SN74CBT3125DR	
	SSOP − DB	Tape and reel	SN74CBT3125DBR	CU125
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3125DBQR	CU125
	TSSOP − PW	Tape and reel	SN74CBT3125PWR	CU125
	TVSOP − DGV	Tape and reel	SN74CBT3125DGVR	CU125

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each bus switch)

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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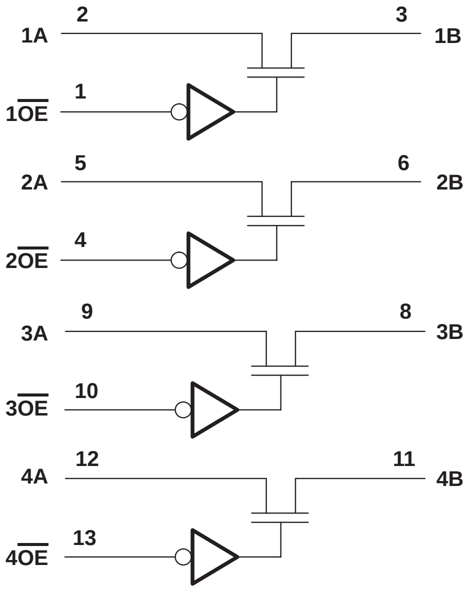
logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, PW, and RGY packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_K ($V_{I/O} < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): DBQ package	90°C/W
(see Note 2): DGV package	127°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			4		pF
r_{on}[§]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		16	22	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

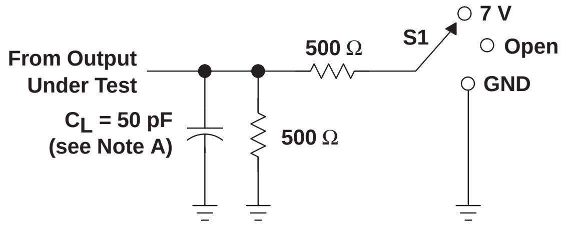
[§] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		6	1.6	5.4	ns
t_{dis}	$\overline{OE}$	A or B		5.1	1	4.7	ns

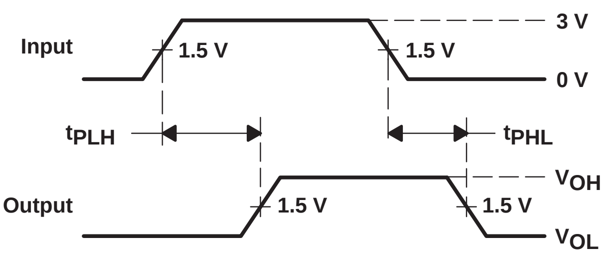
[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

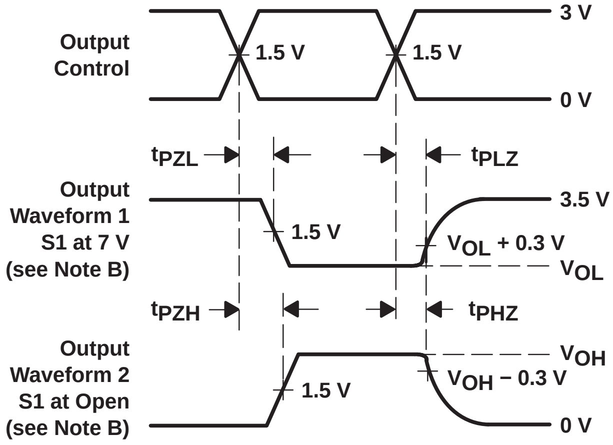

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

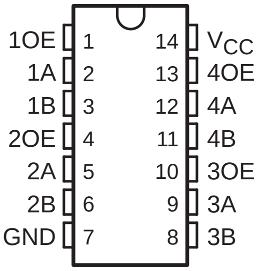
Figure 1. Load Circuit and Voltage Waveforms

SN74CBT3126
QUADRUPLE FET BUS SWITCH

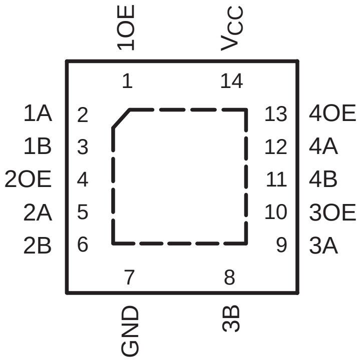
SCDS020K − MAY 1995 − REVISED OCTOBER 2003

- **Standard ’126-Type Pinout (D, DB, DGV, and PW Packages)**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

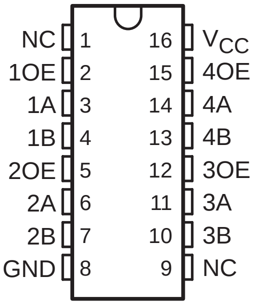
D, DB, DGV, OR PW PACKAGE (TOP VIEW)


1OE 1
1A 2
1B 3
2OE 4
2A 5
2B 6
GND 7
14 VCC
13 4OE
12 4A
11 4B
10 3OE
9 3A
8 3B

RGY PACKAGE (TOP VIEW)


1OE
VCC
1
14
1A 2
1B 3
2OE 4
2A 5
2B 6
13 4OE
12 4A
11 4B
10 3OE
9 3A
7
8
GND
3B

DBQ PACKAGE (TOP VIEW)


NC 1
1OE 2
1A 3
1B 4
2OE 5
2A 6
2B 7
GND 8
16 VCC
15 4OE
14 4A
13 4B
12 3OE
11 3A
10 3B
9 NC

NC − No internal connection

description/ordering information

The SN74CBT3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBT3126RGYR	CU126
	SOIC − D	Tube	SN74CBT3126D	CBT3126
		Tape and reel	SN74CBT3126DR	
	SSOP − DB	Tape and reel	SN74CBT3126DBR	CU126
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3126DBQR	CU126
	TSSOP − PW	Tube	SN74CBT3126PW	CU126
		Tape and reel	SN74CBT3126PWR	
	TVSOP − DGV	Tape and reel	SN74CBT3126DGVR	CU126

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each bus switch)

INPUT OE	FUNCTION
L	Disconnect
H	A = B

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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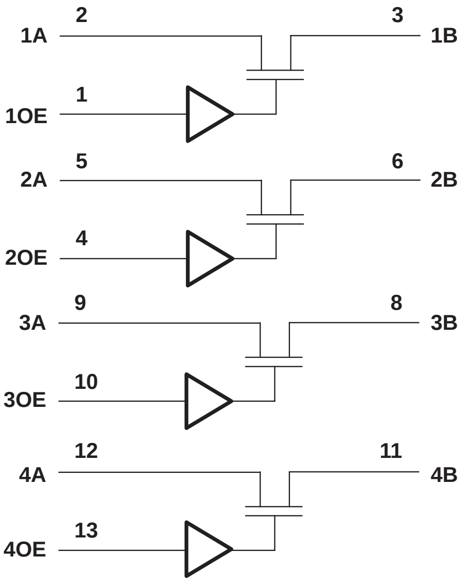
logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, PW, and RGY packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_K ($V_{I/O} < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): DBQ package	90°C/W
(see Note 2): DGV package	127°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA					−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND					±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND				3	µA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND				2.5	mA
C_i	Control inputs	V_I = 3 V or 0					3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	OE = GND				4		pF
r_{on}[§]		V_{CC} = 4 V,	TYP at V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA		16	22	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA			5	7	
				I_I = 30 mA			5	7	
			V_I = 2.4 V,	I_I = 15 mA			10	15	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

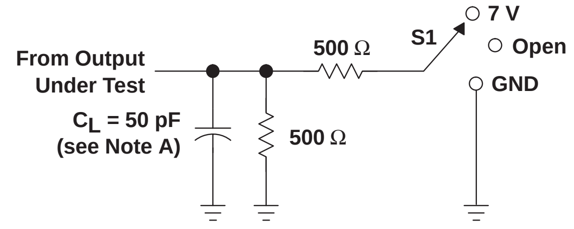
[§] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A		0.35		0.25	ns
t_{en}	OE	A or B		5.4	1.6	5.1	ns
t_{dis}	OE	A or B		5	1	4.5	ns

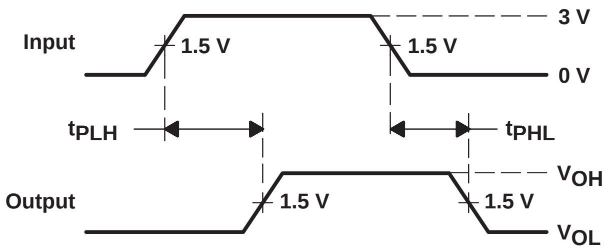
[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

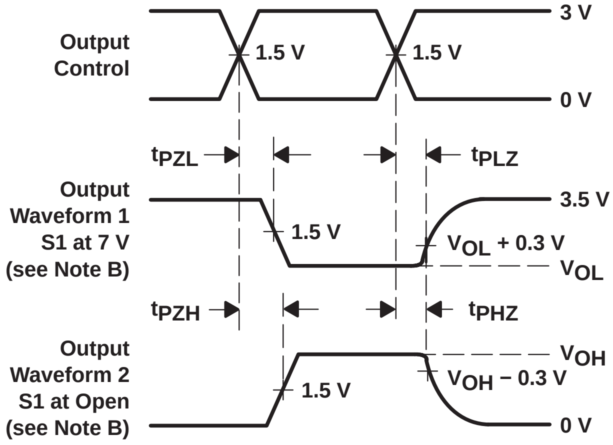

From Output Under Test
500 Ω
S1
7 V
Open
GND
C_L = 50 pF (see Note A)
500 Ω

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

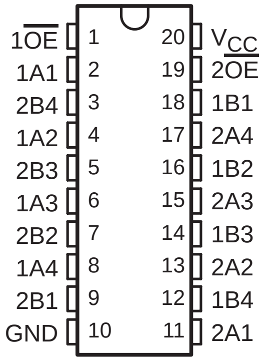
Figure 1. Load Circuit and Voltage Waveforms

SN74CBT3244
OCTAL FET BUS SWITCH

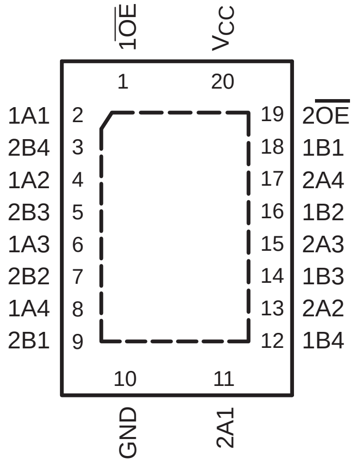
SCDS001N − NOVEMBER 1992 − REVISED SEPTEMBER 2003

- **Standard ’244-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

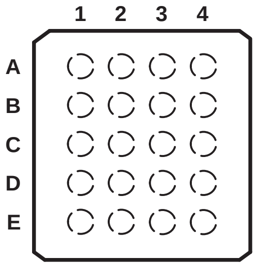
DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)


$1\overline{OE}$ 1
1A1 2
2B4 3
1A2 4
2B3 5
1A3 6
2B2 7
1A4 8
2B1 9
GND 10
20 V_{CC}
19 $2\overline{OE}$
18 1B1
17 2A4
16 1B2
15 2A3
14 1B3
13 2A2
12 1B4
11 2A1

RGY PACKAGE
(TOP VIEW)


$1\overline{OE}$
V_{CC}
1
20
1A1 2
2B4 3
1A2 4
2B3 5
1A3 6
2B2 7
1A4 8
2B1 9
19 $2\overline{OE}$
18 1B1
17 2A4
16 1B2
15 2A3
14 1B3
13 2A2
12 1B4
10
11
GND
2A1

GQN OR ZQN PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4
A	1A1	$1\overline{OE}$	V_{CC}	$2\overline{OE}$
B	1A2	2A4	2B4	1B1
C	1A3	2B3	2A3	1B2
D	1A4	2A2	2B2	1B3
E	GND	2B1	2A1	1B4

description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBT3244RGYR	CU244
	SOIC − DW	Tube	SN74CBT3244DW	CBT3244
		Tape and reel	SN74CBT3244DWR	
	SSOP − DB	Tape and reel	SN74CBT3244DBR	CU244
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3244DBQR	CBT3244
	TSSOP − PW	Tube	SN74CBT3244PW	CU244
		Tape and reel	SN74CBT3244PWR	
	TVSOP − DGV	Tape and reel	SN74CBT3244DGVR	CU244
	VFBGA − GQN	Tape and reel	SN74CBT3244GQNR	CU244
	VFBGA − ZQN (Pb-free)		SN74CBT3244ZQNR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TEXAS INSTRUMENTS

description/ordering information (continued)

The SN74CBT3244 provides eight bits of high-speed TTL-compatible bus switching. The SOIC, SSOP, TSSOP, and TVSOP packages provide a standard ’244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

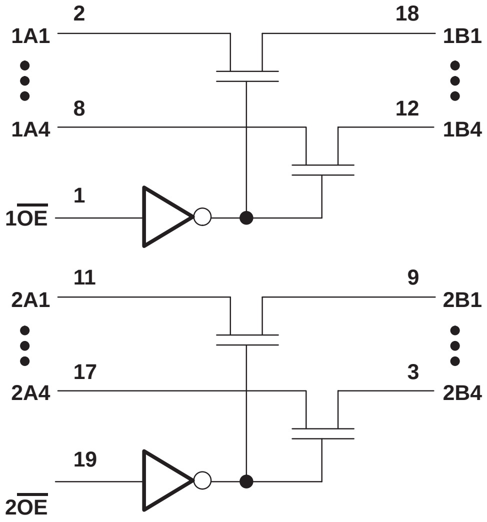
The device is organized as two 4-bit low-impedance switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on, and data can flow from port A to port B, or vice versa. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each 4-bit bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



Pin numbers shown are for the DB, DBQ, DGV, DW, RGY, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V
Continuous channel current . . . . 128 mA
Clamp current, I_K ($V_{I/O}$ < 0) . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . 70°C/W
(see Note 2): DBQ package . . . . 68°C/W
(see Note 2): DGV package . . . . 92°C/W
(see Note 2): DW package . . . . 58°C/W
(see Note 2): GQN/ZQN package . . . . 78°C/W
(see Note 2): PW package . . . . 83°C/W
(see Note 3): RGY package . . . . 37°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			50	µA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6		pF
r_{on}¶		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

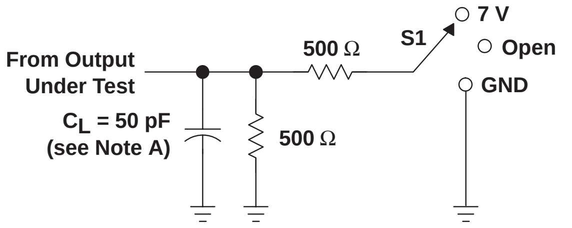
¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}†	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	8.9	ns
t_{dis}	$\overline{OE}$	A or B	1	7.4	ns

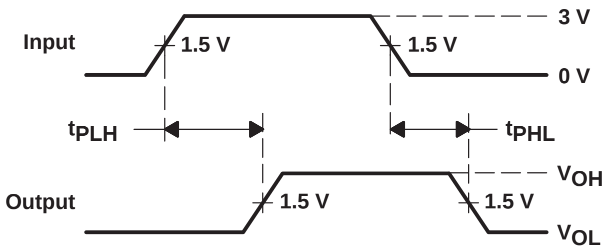
† This propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

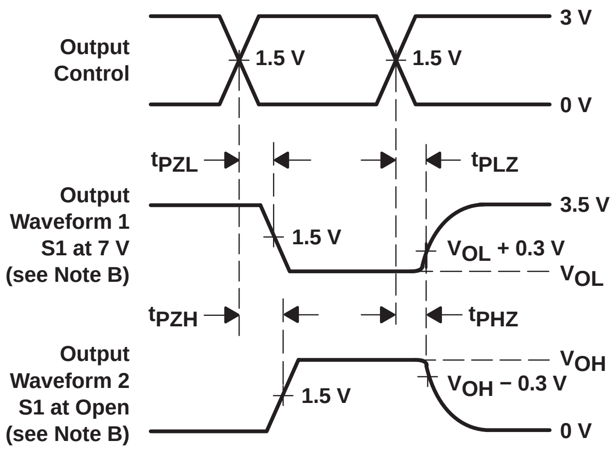

From Output Under Test
C_L = 50 pF (see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

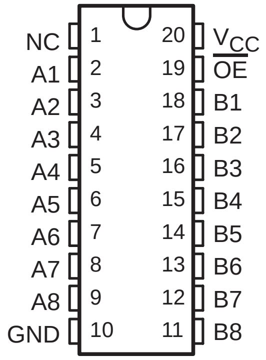
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

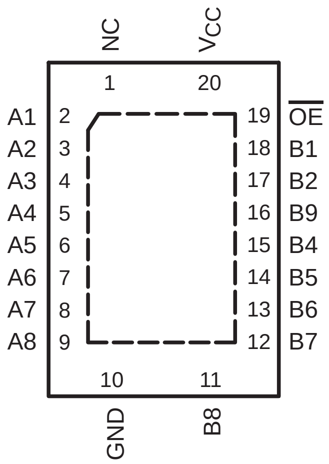
- **Standard ’245-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)


NC 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
GND 10
20 V_{CC}
19 $\overline{OE}$
18 B1
17 B2
16 B3
15 B4
14 B5
13 B6
12 B7
11 B8

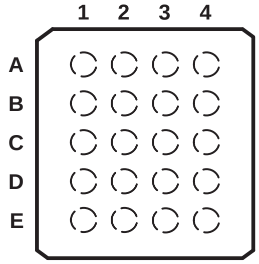
NC − No internal connection

RGY PACKAGE
(TOP VIEW)


NC
V_{CC}
1
20
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
19 $\overline{OE}$
18 B1
17 B2
16 B9
15 B4
14 B5
13 B6
12 B7
10
11
GND
B8

NC − No internal connection

GQN OR ZQN PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4
A	A1	NC	V_{CC}	$\overline{OE}$
B	A3	B2	A2	B1
C	A5	A4	B4	B3
D	A7	B6	A6	B5
E	GND	A8	B8	B7

NC − No internal connection

description/ordering information

The SN74CBT3245A provides eight bits of high-speed TTL-compatible bus switching. The SOIC, SSOP, TSSOP, and TVSOP packages provide a standard ’245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 8-bit switch. When the output-enable ($\overline{OE}$) input is low, the switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

ORDERING INFORMATION

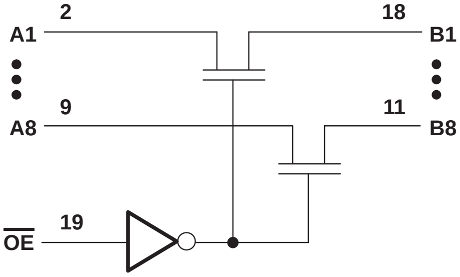
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBT3245ARGYR	CU245A
	SOIC − DW	Tube	SN74CBT3245ADW	CBT3245A
		Tape and reel	SN74CBT3245ADWR	
	SSOP − DB	Tape and reel	SN74CBT3245ADBR	CU245A
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3245ADBQR	CBT3245A
	TSSOP − PW	Tube	SN74CBT3245APW	CU245A
		Tape and reel	SN74CBT3245APWR	
	TVSOP − DGV	Tape and reel	SN74CBT3245ADGVR	CU245A
	VFBGA − GQN	Tape and reel	SN74CBT3245AGQNR	CU245A
	VFBGA − ZQN (Pb-free)		SN74CBT3245AZQNR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



Pin numbers shown are for the DB, DBQ, DGV, DW, PW, and RGY packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	70°C/W
(see Note 2): DBQ package	68°C/W
(see Note 2): DGV package	92°C/W
(see Note 2): DW package	58°C/W
(see Note 2): GQN/ZQN package	78°C/W
(see Note 2): PW package	83°C/W
(see Note 3): RGY package	37°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[‡]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			50	µA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control inputs	V_I = 3 V or 0				4		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			4		pF
r_{on}[¶]		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

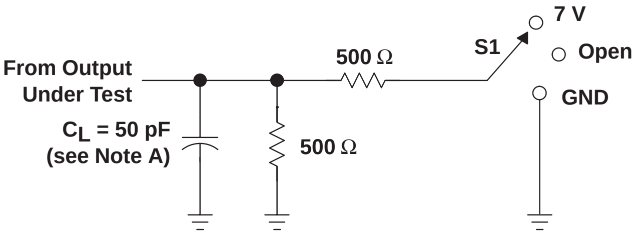
[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		6.4	1.9	5.9	ns
t_{dis}	$\overline{OE}$	A or B		5.7	2.1	6	ns

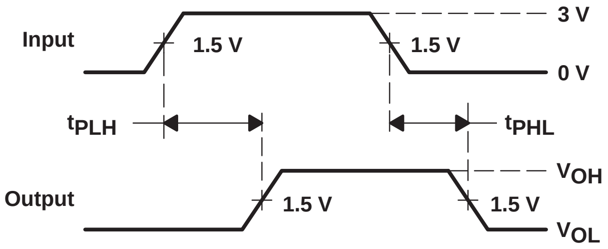
[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

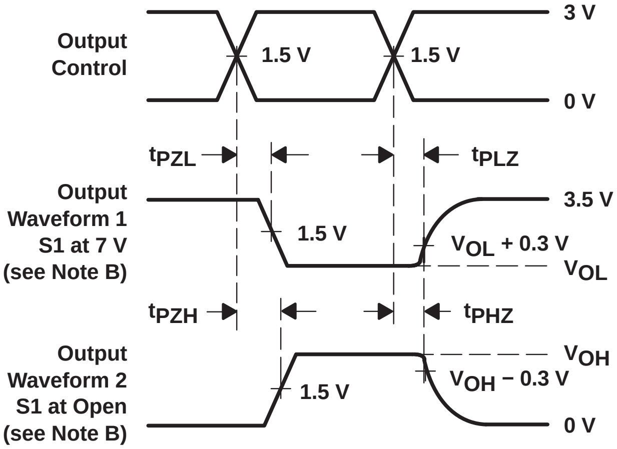

7 V
S1
Open
GND
500 Ω
From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

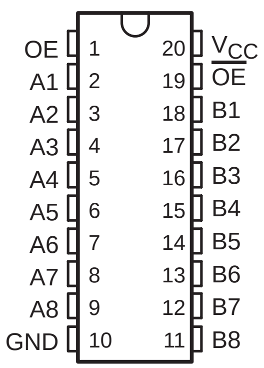
Figure 1. Load Circuit and Voltage Waveforms

SN74CBT3345
8-BIT FET BUS SWITCH

SCDS027H − MAY 1995 − REVISED JUNE 2002

- **Standard ’245-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3345 provides eight bits of high-speed TTL-compatible bus switching in a standard ’245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 8-bit switch bank with dual output-enable (OE and $\overline{\text{OE}}$) inputs. When $\overline{\text{OE}}$ is low or OE is high, the switch is on, and port A is connected to port B. When $\overline{\text{OE}}$ is high and OE is low, the switch is open, and the high-impedance state exists between the two ports.

ORDERING INFORMATION

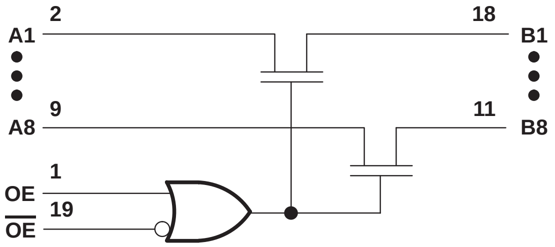
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CBT3345DW	CBT3345
		Tape and reel	SN74CBT3345DWR	
	SSOP − DB	Tape and reel	SN74CBT3345DBR	CU345
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3345DBQR	CBT3345
	TSSOP − PW	Tape and reel	SN74CBT3345PWR	CU345
	TVSOP − DGV	Tape and reel	SN74CBT3345DGVR	CU345

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		FUNCTION
OE	$\overline{OE}$	
H	X	A port = B port
X	L	A port = B port
L	H	Disconnect

logic diagram (positive logic)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	70°C
	DBQ package	68°C
	DGV package	92°C
	DW package	58°C
	PW package	83°C
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I	All inputs	V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			50	µA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC} or OE = GND			6		pF
r_{on}¶		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

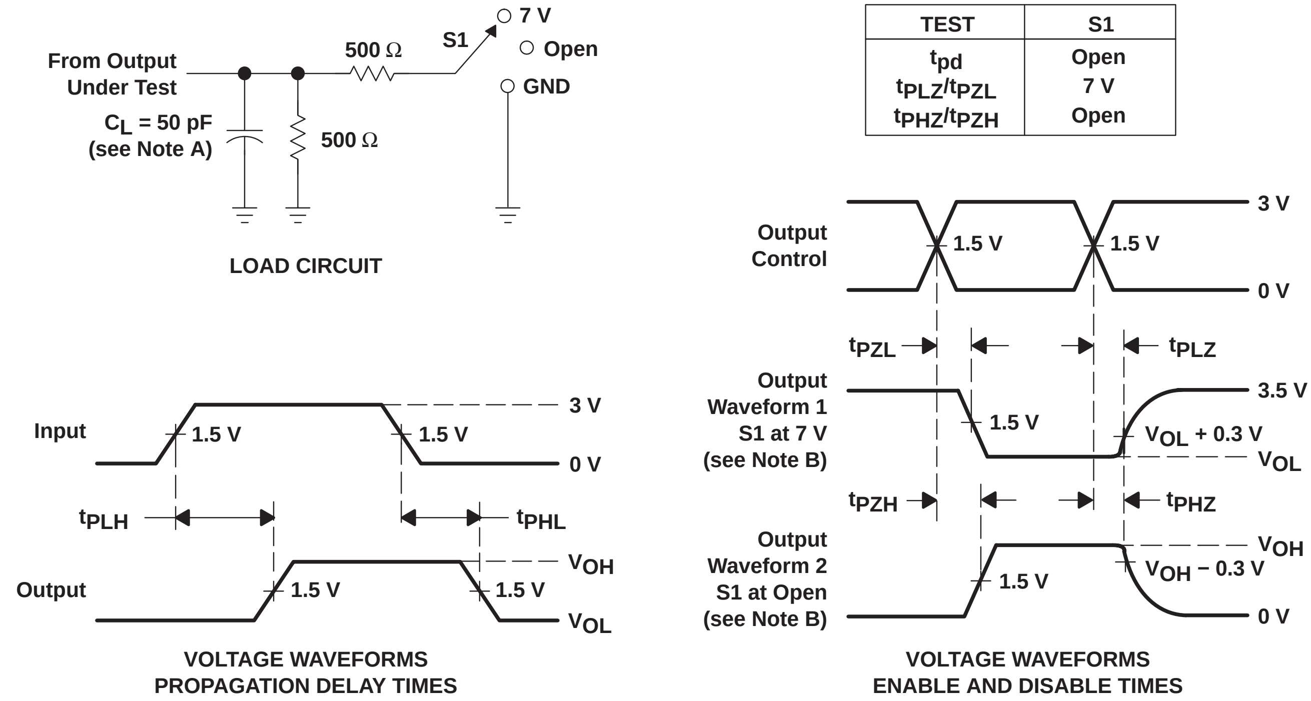
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	
t_{pd}[†]	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$ or OE	A or B	1	9.1	ns
t_{dis}	$\overline{OE}$ or OE	A or B	1	8.7	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION


From Output Under Test
C_L = 50 pF (see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND
LOAD CIRCUIT
Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES
Output Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

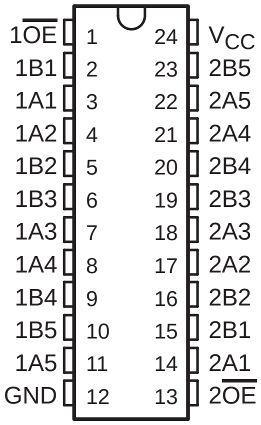
Figure 1. Load Circuit and Voltage Waveforms

SN74CBT3384A
10-BIT FET BUS SWITCH

SCDS004K − NOVEMBER 1992 − REVISED OCTOBER 2000

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)



description

The SN74CBT3384A provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as two 5-bit switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CBT3384ADW	CBT3384A
		Tape and reel	SN74CBT3384ADWR	
	SSOP − DB	Tape and reel	SN74CBT3384ADBR	CU384A
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3384ADBQR	CBT3384A
	TSSOP − PW	Tape and reel	SN74CBT3384APWR	CU384A
	TVSOP − DGV	Tape and reel	SN74CBT3384ADGVR	CU384A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 5-bit bus switch)

INPUTS		INPUTS/OUTPUTS	
$\overline{1OE}$	$\overline{2OE}$	1B1−1B5	2B1−2B5
L	L	1A1−1A5	2A1−2A5
L	H	1A1−1A5	Z
H	L	Z	2A1−2A5
H	H	Z	Z

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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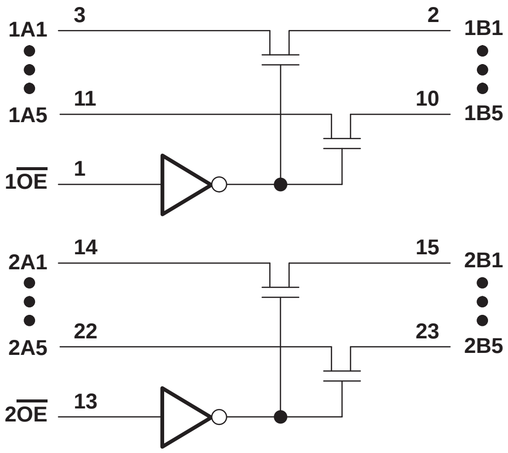
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	63°C/W
	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	$V_I = V_{CC}$ or GND			3	µA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				4		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE} = V_{CC}$			4.5		pF
r_{on}[§]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

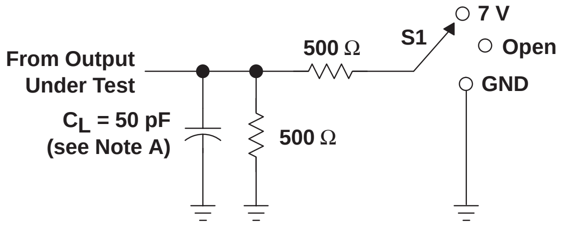
[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		6.2	1.9	5.7	ns
t_{dis}	$\overline{OE}$	A or B		5.5	2.1	5.2	ns

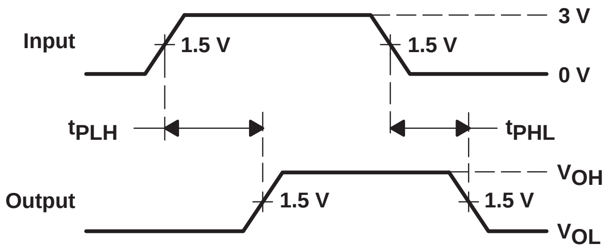
[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

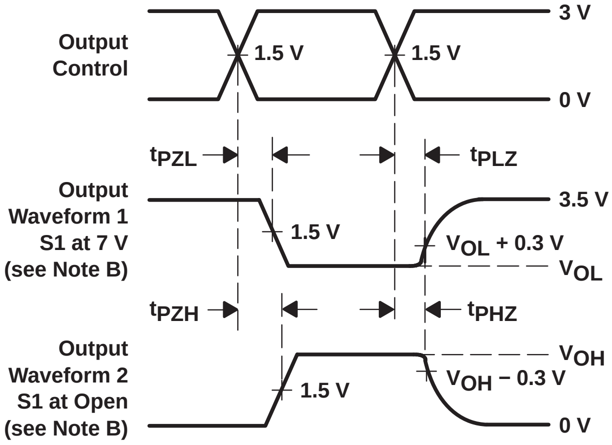

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

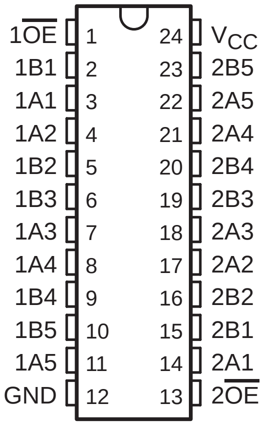
Figure 1. Load Circuit and Voltage Waveforms

SN54CBTD3384, SN74CBTD3384
10-BIT FET BUS SWITCHES
WITH LEVEL SHIFTING

SCDS025Q − MAY 1995 − REVISED JULY 2002

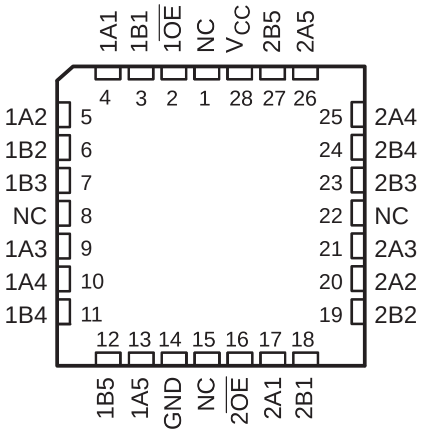
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Designed to Be Used in Level-Shifting Applications**

SN54CBTD3384 . . . JT OR W PACKAGE
SN74CBTD3384 . . . DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



1OE 1
1B1 2
1A1 3
1A2 4
1B2 5
1B3 6
1A3 7
1A4 8
1B4 9
1B5 10
1A5 11
GND 12
24 VCC
23 2B5
22 2A5
21 2A4
20 2B4
19 2B3
18 2A3
17 2A2
16 2B2
15 2B1
14 2A1
13 2OE

SN54CBTD3384 . . . FK PACKAGE
(TOP VIEW)



1A1
1B1
1OE
NC
VCC
2B5
2A5
4 3 2 1 28 27 26
1A2 5
1B2 6
1B3 7
NC 8
1A3 9
1A4 10
1B4 11
25 2A4
24 2B4
23 2B3
22 NC
21 2A3
20 2A2
19 2B2
12 13 14 15 16 17 18
1B5
1A5
GND
NC
2OE
2A1
2B1

NC − No internal connection

description/ordering information

The ’CBTD3384 devices provide ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switches allows connections to be made without adding propagation delay. A diode to V_{CC} is integrated on the die to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

These devices are organized as two 5-bit switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CBTD3384DW	CBTD3384
		Tape and reel	SN74CBTD3384DWR	
	SSOP − DB	Tape and reel	SN74CBTD3384DBR	CC384
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBTD3384DBQR	CBTD3384
	TSSOP − PW	Tape and reel	SN74CBTD3384PWR	CC384
	TVSOP − DGV	Tape and reel	SN74CBTD3384DGVR	CC384
−55°C to 125°C	CDIP − JT	Tube	SNJ54CBTD3384JT	SNJ54CBTD3384JT
	CFP − W	Tube	SNJ54CBTD3384W	SNJ54CBTD3384W
	LCCC − FK	Tube	SNJ54CBTD3384FK	SNJ54CBTD3384FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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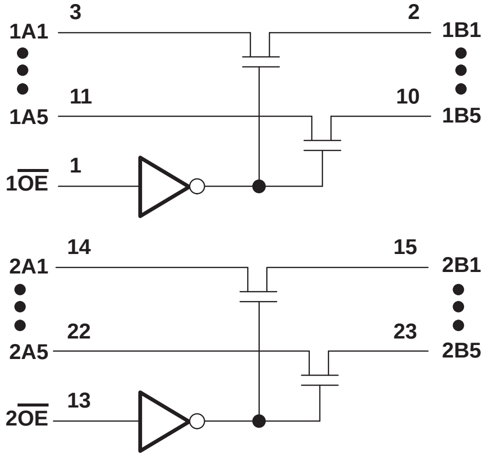
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

FUNCTION TABLE
(each 5-bit bus switch)

INPUTS		INPUTS/OUTPUTS	
$1\overline{OE}$	**$2\overline{OE}$**	**1B1−1B5**	**2B1−2B5**
L	L	1A1−1A5	2A1−2A5
L	H	1A1−1A5	Z
H	L	Z	2A1−2A5
H	H	Z	Z

logic diagram (positive logic)



Pin numbers shown are for the DB, DBQ, DGV, DW, JT, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V
Continuous channel current . . . . 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . 63°C/W
DBQ package . . . . 61°C/W
DGV package . . . . 86°C/W
DW package . . . . 46°C/W
PW package . . . . 88°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54CBTD3384		SN74CBTD3384		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level control input voltage	2		2		V
V_{IL}	Low-level control input voltage		0.8		0.8	V
T_A	Operating free-air temperature	−55	125	−40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54CBTD3384			SN74CBTD3384			UNIT
					MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA					−1.2			−1.2	V
V_{OH}		See Figure 2									
I_I		V_{CC} = 5.5 V, V_I = 5.5 V or GND					±1			±1	µA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND					1.5			1.5	mA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					2.5			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3			3		pF
$C_{io(OFF)}$		V_O = 3 V or 0, $\overline{OE}$ = V_{CC}				3.5			3.5		pF
r_{on}[§]		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5			5	7	Ω
				I_I = 30 mA		5			5	7	
			V_I = 2.4 V,	I_I = 15 mA		35			35	50	

[†] Typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

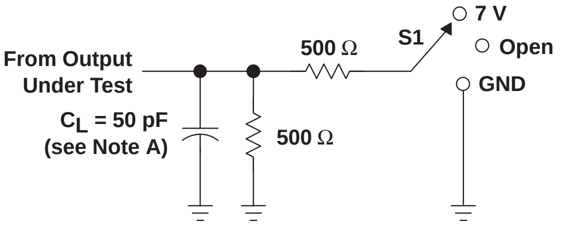
[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBTD3384		SN74CBTD3384		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A		0.25		0.25	ns
t_{en}	$\overline{OE}$	A or B	2.2	9.7	2.3	7	ns
t_{dis}	$\overline{OE}$	A or B	1.5	8.6	1.7	5.3	ns

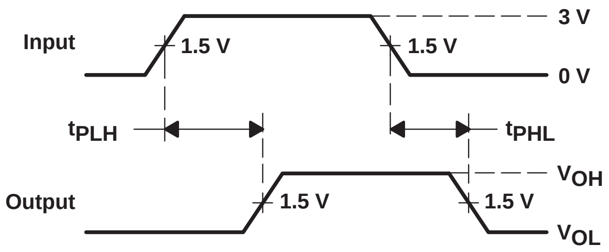
[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

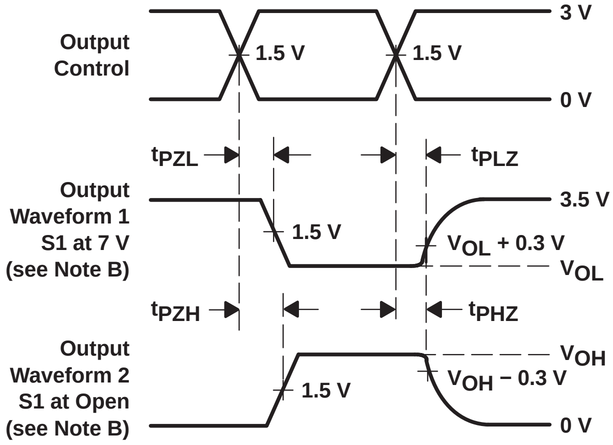

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
V_{OL} + 0.3 V
3.5 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH} − 0.3 V
V_{OH}
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

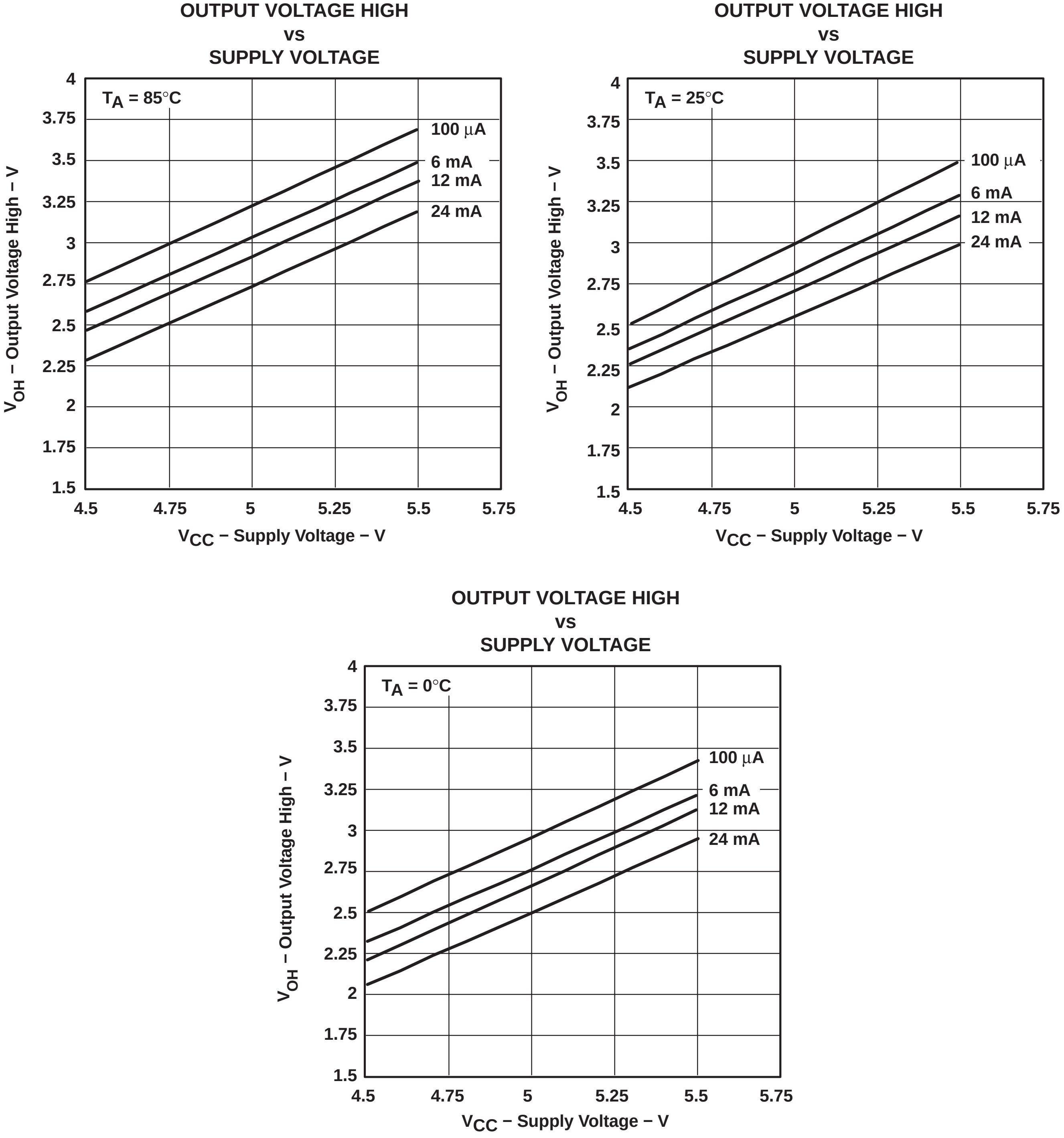


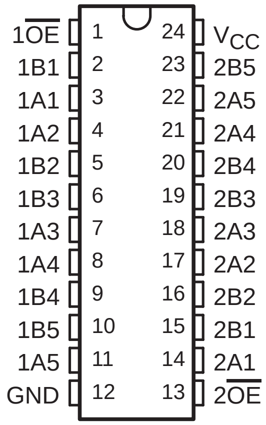
Figure 2. V_{OH} Values

SN74CBTS3384
10-BIT FET BUS SWITCH WITH SCHOTTKY DIODE CLAMPING

SCDS024M − MAY 1995 − REVISED JULY 2003

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBTS3384 provides ten bits of high-speed TTL-compatible bus switching with Schottky diodes on the I/Os to clamp undershoot. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as two 5-bit bus switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CBTS3384DW	CBTS3384
		Tape and reel	SN74CBTS3384DWR	
	SSOP − DB	Tape and reel	SN74CBTS3384DBR	CR384
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBTS3384DBQR	CBTS3384
	TSSOP − PW	Tube	SN74CBTS3384PW	CR384
		Tape and reel	SN74CBTS3384PWR	
	TVSOP − DGV	Tape and reel	SN74CBTS3384DGVR	CR384

---

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 5-bit bus switch)

INPUTS		INPUTS/OUTPUTS	
$1\overline{OE}$	$2\overline{OE}$	1B1−1B5	2B1−2B5
L	L	1A1−1A5	2A1−2A5
L	H	1A1−1A5	Z
H	L	Z	2A1−2A5
H	H	Z	Z

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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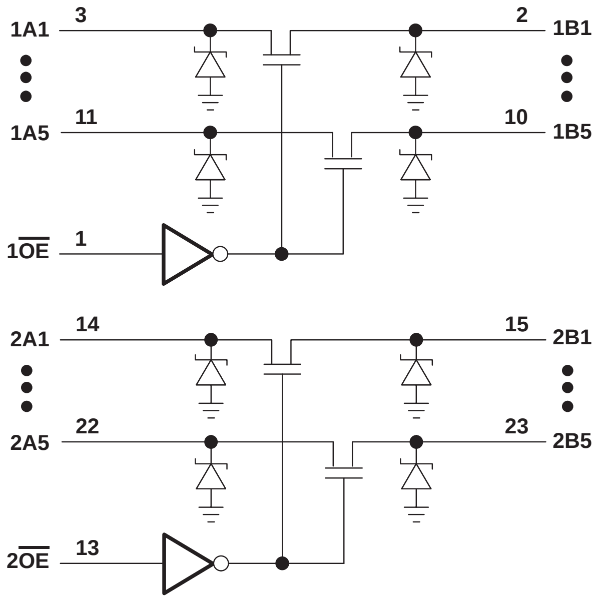
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	63°C/W
	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	A or B inputs	V_{CC} = 4.5 V,	I_I = −18 mA				−0.6	V
	Control inputs						−1.2	
I_I	I_{IL}	V_{CC} = 5.5 V,	V_I = GND				−1	μA
	I_{IH}	V_{CC} = 5.5 V,	V_I = 5.5 V				150	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	$V_I = V_{CC}$ or GND			3	μA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				6		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE} = V_{CC}$			6.5		pF
r_{on}§		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

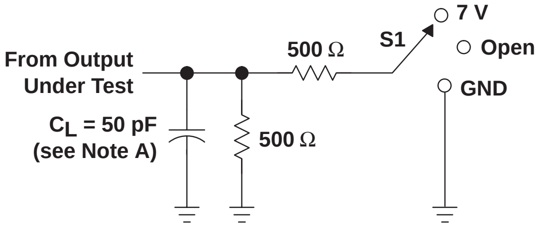
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		6.2	1.9	5.7	ns
t_{dis}	$\overline{OE}$	A or B		5.5	2.1	5.2	ns

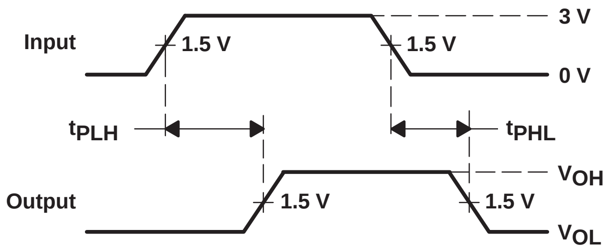
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

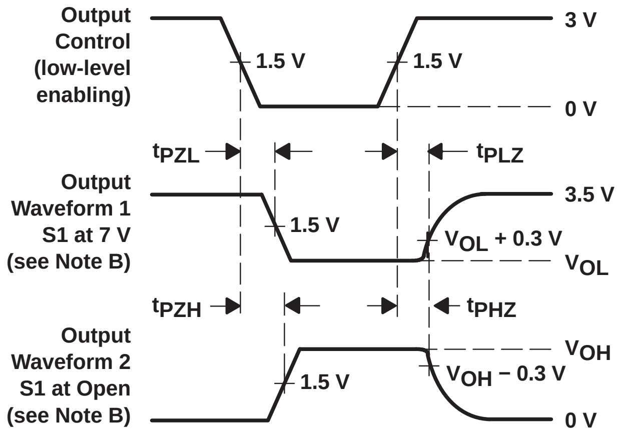

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
(low-level
enabling)
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

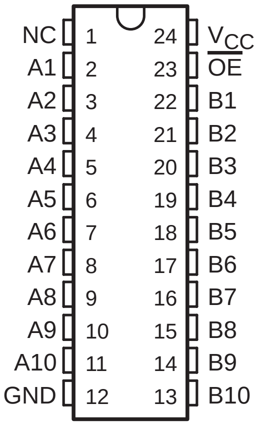
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

description

The SN74CBT3861 provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 10-bit switch with a single output-enable ($\overline{OE}$) input. When $\overline{OE}$ is low, the switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

ORDERING INFORMATION

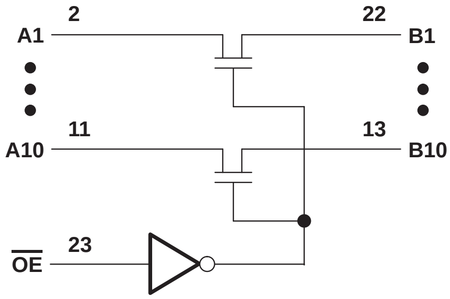
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CBT3861DW	CBT3861
		Tape and reel	SN74CBT3861DWR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3861DBQR	CBT3861
	TSSOP − PW	Tape and reel	SN74CBT3861PWR	CU861
	TVSOP − DGV	Tape and reel	SN74CBT3861DGVR	CU861

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[‡]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5		pF
r_{on}[¶]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	22	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

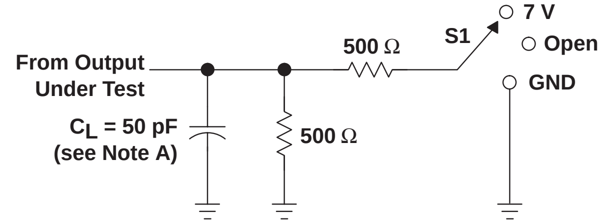
[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}†	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		8.1	3.8	7.5	ns
t_{dis}	$\overline{OE}$	A or B		6.3	3.4	6.6	ns

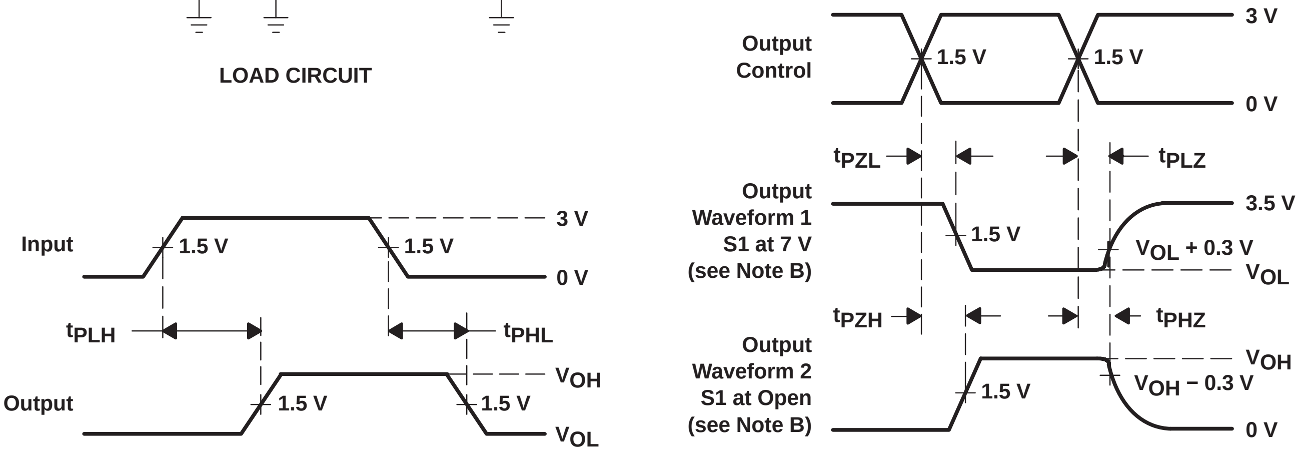
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION


From Output Under Test
C_L = 50 pF (see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}
Output Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

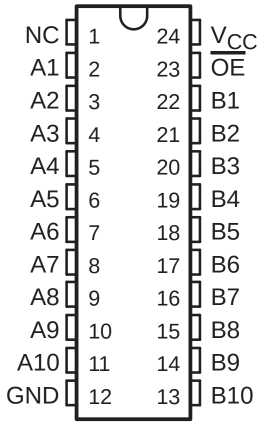
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTD3861
10-BIT FET BUS SWITCH
WITH LEVEL SHIFTING

SCDS084G − JULY 1998 − REVISED JULY 2002

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Designed to Be Used in Level-Shifting Applications**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The SN74CBTD3861 provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. A diode to V_{CC} is integrated on the die to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

The device is organized as one 10-bit switch with a single output-enable ($\overline{\text{OE}}$) input. When $\overline{\text{OE}}$ is low, the switch is on, and port A is connected to port B. When $\overline{\text{OE}}$ is high, the switch is open, and the high-impedance state exists between the two ports.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CBTD3861DW	CBTD3861
		Tape and reel	SN74CBTD3861DWR	
	SSOP − DB	Tape and reel	SN74CBTD3861DBR	CC861
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBTD3861DBQR	CBTD3861
	TSSOP − PW	Tape and reel	SN74CBTD3861PWR	CC861
	TVSOP − DGV	Tape and reel	SN74CBTD3861DGVR	CC861

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

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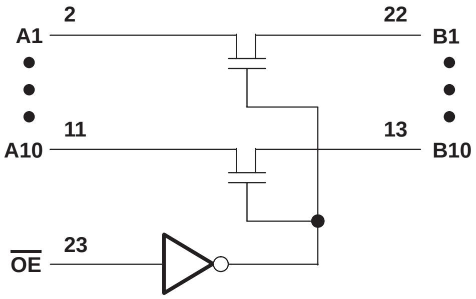
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	63°C/W
	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}		See Figure 2						
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1.5	mA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				2.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			4		pF
r_{on}§		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		20	50	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

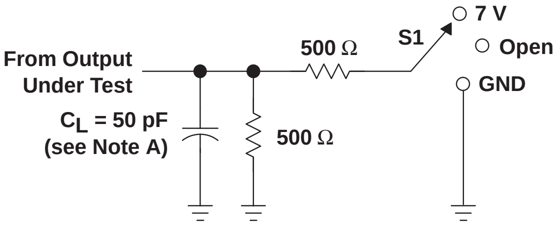
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}¶	A or B	B or A		0.35	ns
t_{en}	$\overline{OE}$	A or B	2.6	10	ns
t_{dis}	$\overline{OE}$	A or B	1	6	ns

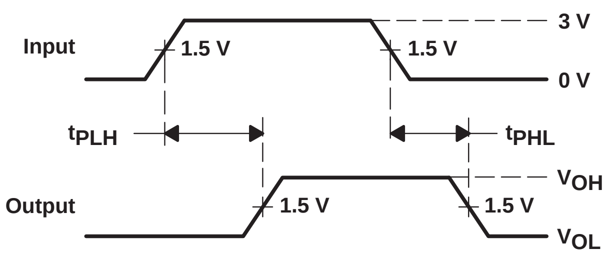
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

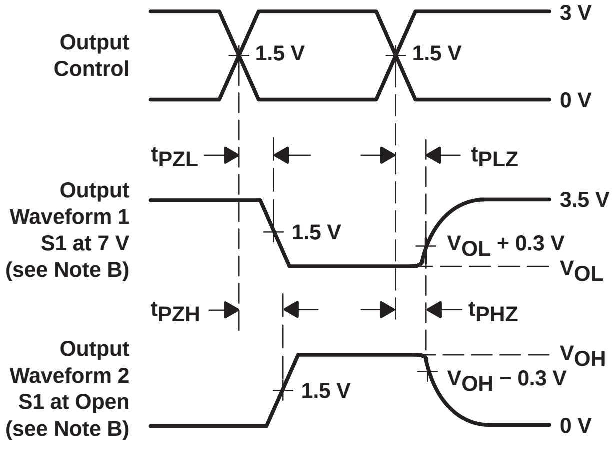

From Output
Under Test
500 Ω
S1
7 V
Open
GND
C_L = 50 pF
(see Note A)
500 Ω

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

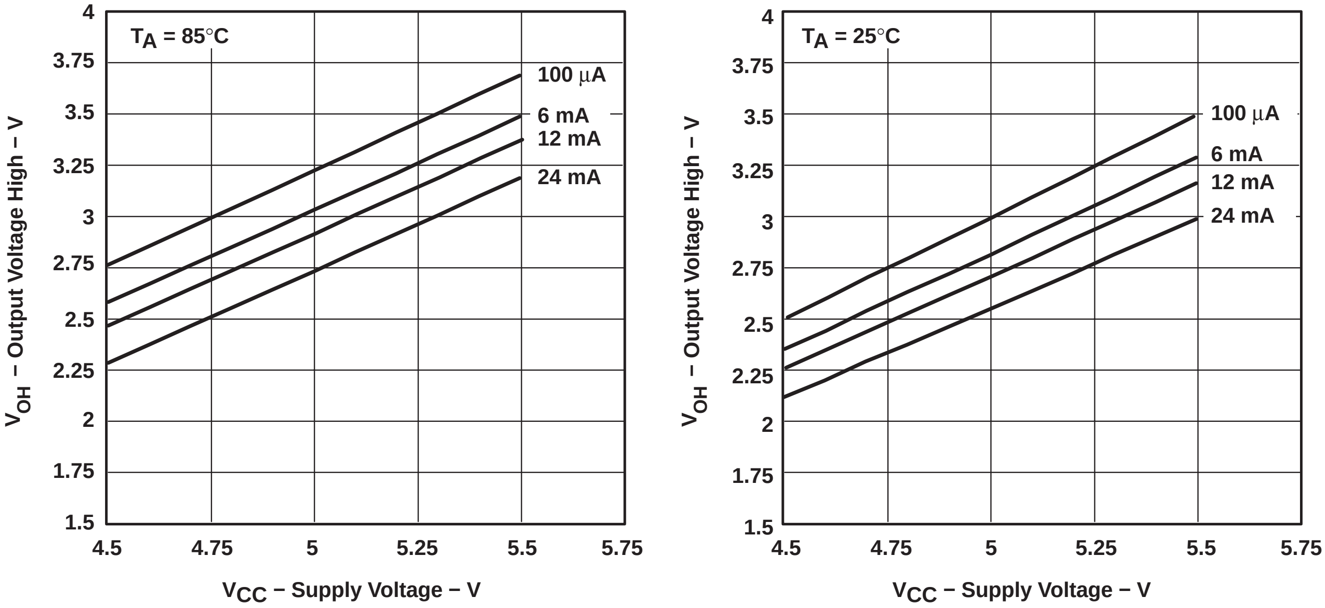

Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS


OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE

OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE

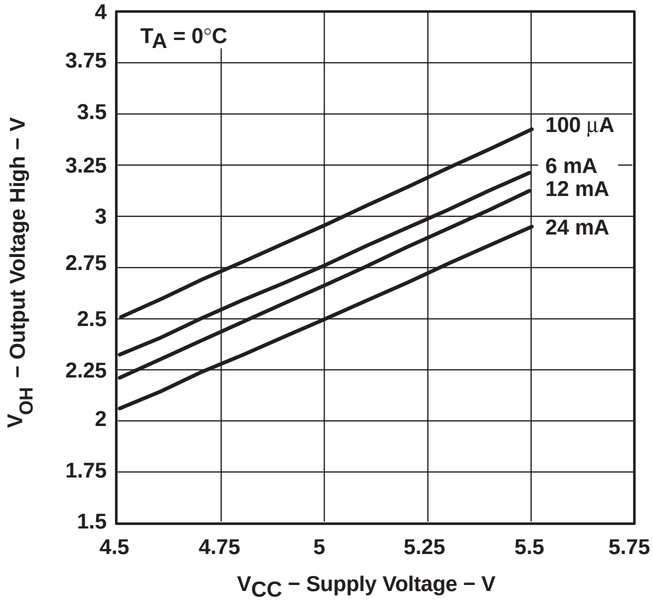

OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE

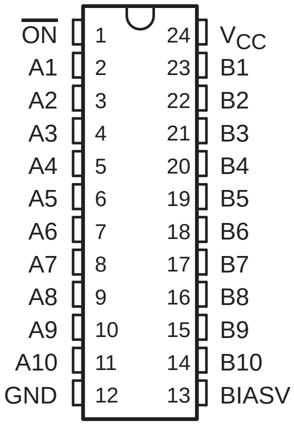
Figure 2. V_{OH} Values

SN74CBT6800A
10-BIT FET BUS SWITCH
WITH PRECHARGED OUTPUTS

SCDS005N − MARCH 1993 − REVISED MARCH 2001

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT6800A provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The SN74CBT6800A is organized as one 10-bit switch with a single enable ($\overline{\text{ON}}$) input. When $\overline{\text{ON}}$ is low, the switch is on, and port A is connected to port B. When $\overline{\text{ON}}$ is high, the switch between port A and port B is open. When $\overline{\text{ON}}$ is high or V_{CC} is 0 V, B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CBT6800ADW	CBT6800A
		Tape and reel	SN74CBT6800ADWR	
	SSOP − DB	Tape and reel	SN74CBT6800ADBR	CT6800A
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT6800ADBQR	CBT6800A
	TSSOP − PW	Tape and reel	SN74CBT6800APWR	CT6800A
	TVSOP − DGV	Tape and reel	SN74CBT6800ADGVR	CT6800A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT $\overline{\text{ON}}$	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV

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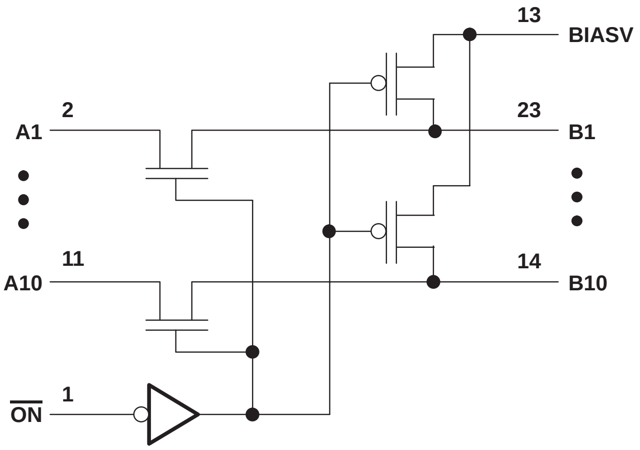
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Bias voltage range, BIASV		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	63°C/W
	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIASV	Supply voltage	1.3	V_{CC}	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	μA
I_O		V_{CC} = 4.5 V,	BIASV = 2.4 V,	V_O= 0	0.25			mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			50	μA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{o(OFF)}$		V_O = 3 V or 0,	Switch off			4.5		pF
r_{on}[§]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		11	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		3	7	
				I_I = 30 mA		3	7	
			V_I = 2.4 V,	I_I = 15 mA		6	15	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

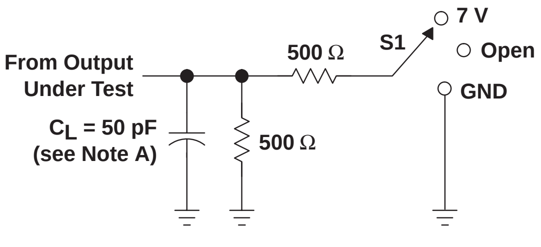
[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}[¶]		A or B	B or A		0.35		0.25	ns
t_{PZH}	BIASV = GND	$\overline{ON}$	A or B		6	2	5.1	ns
t_{PZL}	BIASV = 3 V				6	2	5.6	
t_{PHZ}	BIASV = GND	$\overline{ON}$	A or B		5.5	1	5	ns
t_{PLZ}	BIASV = 3 V				5.5	2	5.9	

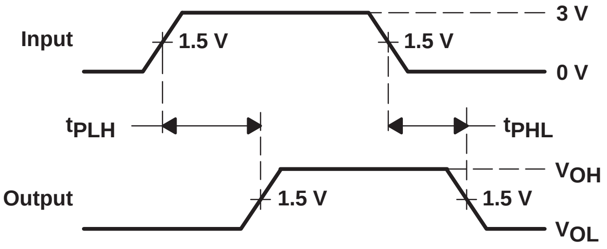
[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

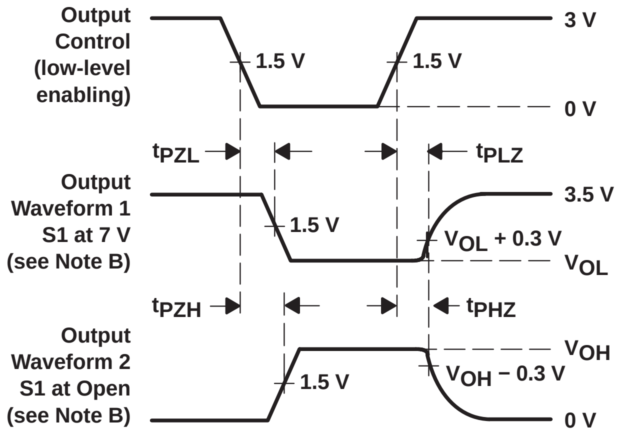

From Output
Under Test
500 Ω
S1
7 V
Open
GND
C_L = 50 pF
(see Note A)
500 Ω

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
(low-level
enabling)
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

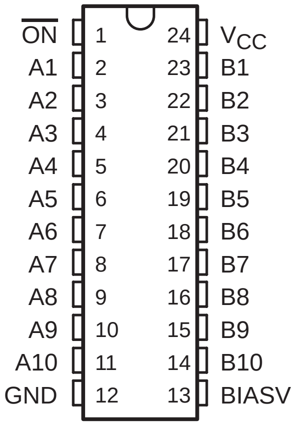
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTK6800
10-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS AND ACTIVE-CLAMP UNDERSHOOT-PROTECTION CIRCUIT

SCDS107B − APRIL 2000 − REVISED OCTOBER 2000

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion**
- **Active-Clamp Undershoot-Protection Circuit on the I/Os Clamps Undershoots Down to −2 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **− 2000-V Human-Body Model (A114-A)**
  - **− 200-V Machine Model (A115-A)**
  - **− 1000-V Charged-Device Model (C101)**

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBTK6800 device provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The A and B ports have an active-clamp undershoot-protection circuit. When there is an undershoot, the active-clamp circuit is enabled and current from V_{CC} is supplied to clamp the output, preventing the pass transistor from turning on.

The SN74CBTK6800 is organized as one 10-bit switch with a single enable ($\overline{\text{ON}}$) input. When $\overline{\text{ON}}$ is low, the switch is on, and port A is connected to port B. When $\overline{\text{ON}}$ is high, the switch between port A and port B is open. When $\overline{\text{ON}}$ is high or V_{CC} is 0 V, B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CBTK6800DW	CBTK6800
		Tape and reel	SN74CBTK6800DWR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBTK6800DBQR	CBTK6800
	TSSOP − PW	Tape and reel	SN74CBTK6800PWR	BK6800
	TVSOP − DGV	Tape and reel	SN74CBTK6800DGVR	BK6800

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT $\overline{\text{ON}}$	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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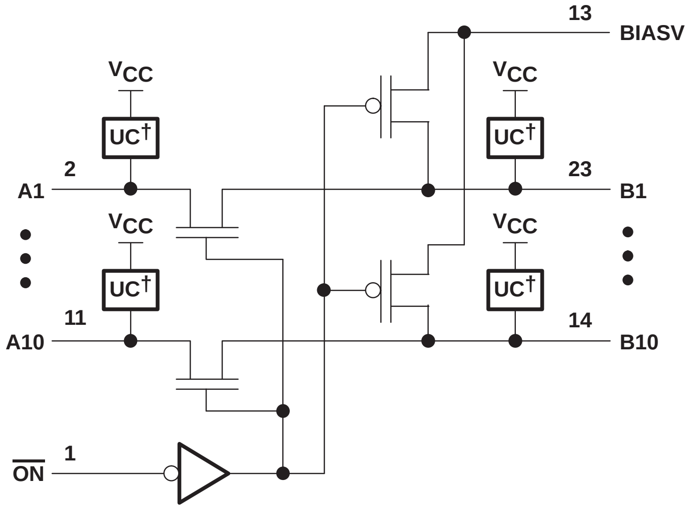
logic diagram (positive logic)



† Undershoot clamp

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}		−0.5 V to 7 V
Bias voltage range, BIASV		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIASV	Supply voltage	1.3	V_{CC}	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{IKU}		V_{CC} = 5.5 V,	0 mA ≥ I_I ≥ −50 mA,	$\overline{OE}$ = 5.5 V			−2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 5.5 V,	BIASV = Open			20	µA
I_O		V_{CC} = 4.5 V,	V_O= 0,	BIASV = 2.4 V	0.25			mA
I_{CC}		V_{CC} = 5.5 V,	V_I = V_{CC} or GND,	I_O = 0			20	µA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{o(OFF)}$		V_O = 3 V or 0,	Switch off			8.5		pF
r_{on}§		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		11	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		3	7	
				I_I = 30 mA		3	7	
			V_I = 2.4 V,	I_I = 15 mA		6	15	

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL-voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A			0.35		0.25	ns
t_{PZH}	$\overline{ON}$	A or B	BIASV = GND		6	2	5.1	ns
t_{PZL}			BIASV = 3 V		6	2	5.6	
t_{PHZ}	$\overline{ON}$	A or B	BIASV = GND		5.5	1	5	ns
t_{PLZ}			BIASV = 3 V		5.5	2	5.9	

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	See Figures 1 and 2, and Table 1	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

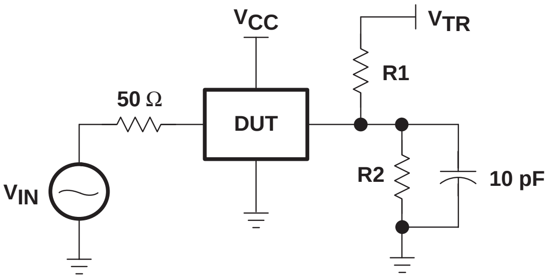


Figure 1. Device Test Setup

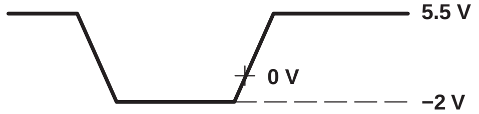


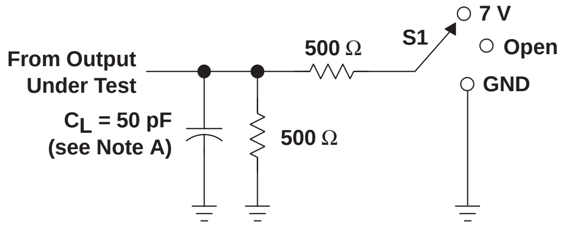
Figure 2. Transient Input Voltage Waveform

Table 1. Device Test Conditions

PARAMETER	VALUE	UNIT
B port under test‡	See Figure 1	
V_{IN}	See Figure 2	V
t_w	20	ns
t_r	2	ns
t_f	2	ns
R1 = R2	100	kΩ
V_{TR}	11	V
V_{CC}	5.5	V
BIASV	Open	

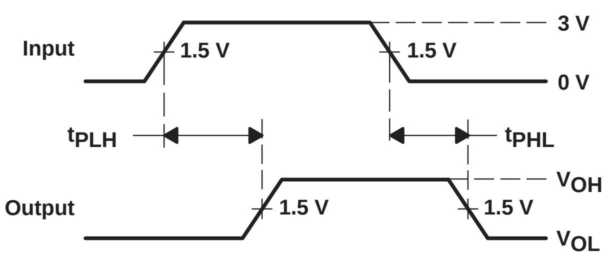
‡ Other B-port outputs are open.

PARAMETER MEASUREMENT INFORMATION

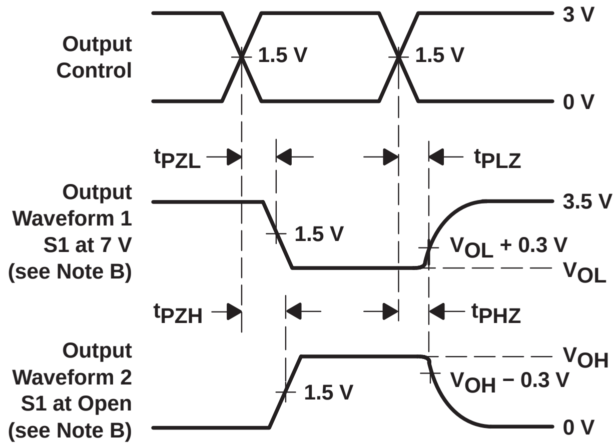

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

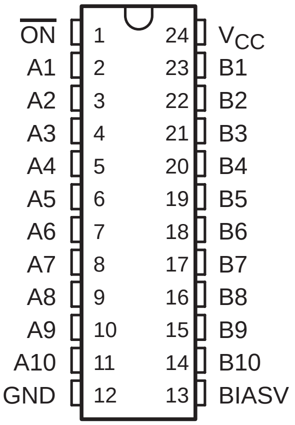
Figure 3. Load Circuit and Voltage Waveforms

SN74CBTS6800
10-BIT FET BUS SWITCH
WITH PRECHARGED OUTPUTS AND SCHOTTKY DIODE CLAMPING

SCDS102C − JUNE 1999 − REVISED OCTOBER 2000

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion**
- **Schottky Diodes on the I/Os to Clamp Undershoots up to −2 V**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBTS6800 provides ten bits of high-speed TTL-compatible bus switching with Schottky diodes on the I/Os to clamp undershoots.

The low on-state resistance of the switch allows bidirectional connections to be made, while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The SN74CBTS6800 is organized as one 10-bit switch with a single enable ($\overline{\text{ON}}$) input. When $\overline{\text{ON}}$ is low, the switch is on, and port A is connected to port B. When $\overline{\text{ON}}$ is high, the switch between port A and port B is open. When $\overline{\text{ON}}$ is high or V_{CC} is 0 V, B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CBTS6800DW	CBTS6800
		Tape and reel	SN74CBTS6800DWR	
	SSOP − DB	Tape and reel	SN74CBTS6800DBR	CS6800
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBTS6800DBQR	CBTS6800
	TSSOP − PW	Tape and reel	SN74CBTS6800PWR	CS6800
	TVSOP − DGV	Tape and reel	SN74CBTS6800DGVR	CS6800

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

$\overline{\text{ON}}$	B1−B10	FUNCTION
L	A1−A10	Connect
H	BIASV	Precharge

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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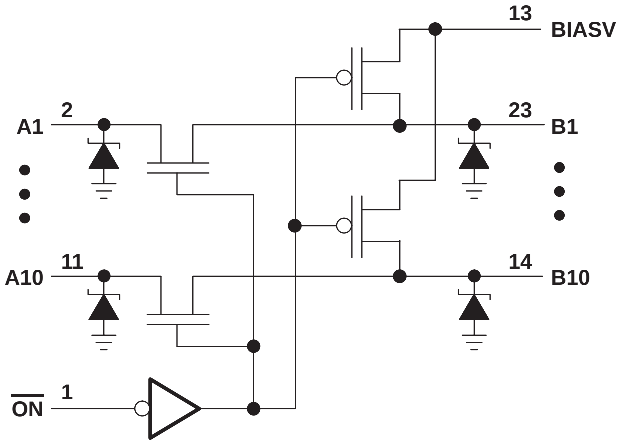
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Bias voltage range, BIASV		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	63°C/W
	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

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† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIASV	Supply voltage	1.3	V_{CC}	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	A or B inputs	V_{CC} = 4.5 V,	I_I = −18 mA				−0.7	V
	Control inputs						−1.2	
I_{IL}		V_{CC} = 5.5 V,	V_I = GND				−5	µA
I_{IH}		V_{CC} = 5.5 V,	V_I = 5.5 V				150	µA
I_O		V_{CC} = 4.5 V,	BIASV = 2.4 V,	V_O= 0	0.25			mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{ON}$ = V_{CC}			4.5		pF
r_{on}[§]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		11	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		3	7	
				I_I = 30 mA		3	7	
			V_I = 2.4 V,	I_I = 15 mA		6	15	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

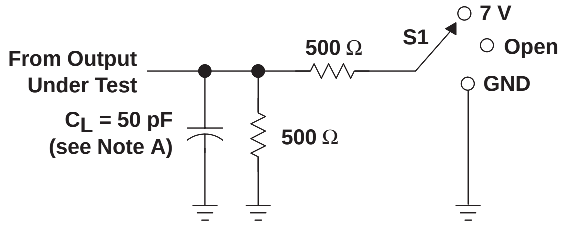
[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A			0.35		0.25	ns
t_{PZH}	$\overline{ON}$	A or B	BIASV = GND		6	2	5.1	ns
t_{PZL}			BIASV = 3 V		6	2	5.6	
t_{PHZ}	$\overline{ON}$	A or B	BIASV = GND		5.5	1	5	ns
t_{PLZ}			BIASV = 3 V		5.5	2	5.9	

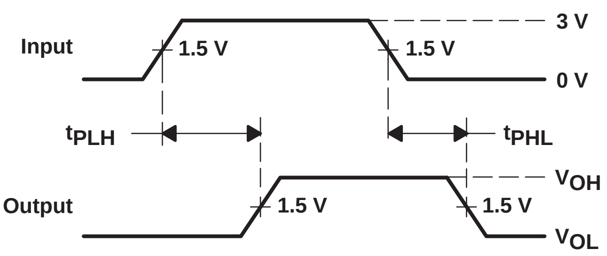
[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

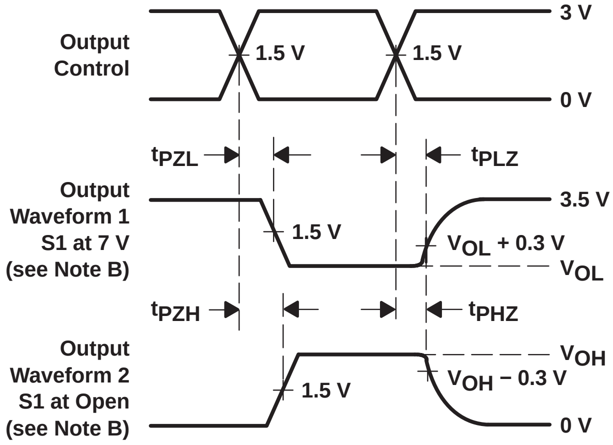

From Output
Under Test
CL = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
tPLH
tPHL
Output
1.5 V
1.5 V
VOH
VOL

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
tPZL
tPLZ
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
VOL + 0.3 V
VOL
tPZH
tPHZ
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
VOH
VOH − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SN54CBT16244, SN74CBT16244
16-BIT FET BUS SWITCHES

SCDS031I − MAY 1996 − REVISED OCTOBER 2000

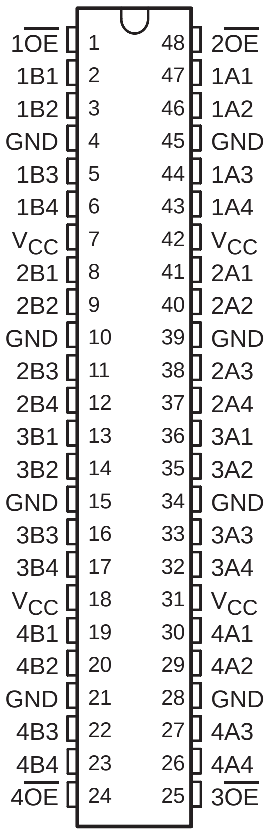
- **Members of Texas Instruments' Widebus™ Family**
- **Standard '16244-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

description

The 'CBT16244 devices provide 16 bits of high-speed TTL-compatible bus switching in a standard '16244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

These devices are organized as four 4-bit low-impedance switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on, and data can flow from port A to port B, or vice versa. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

SN54CBT16244 . . . WD PACKAGE
SN74CBT16244 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)


1OE 1 48 2OE
1B1 2 47 1A1
1B2 3 46 1A2
GND 4 45 GND
1B3 5 44 1A3
1B4 6 43 1A4
VCC 7 42 VCC
2B1 8 41 2A1
2B2 9 40 2A2
GND 10 39 GND
2B3 11 38 2A3
2B4 12 37 2A4
3B1 13 36 3A1
3B2 14 35 3A2
GND 15 34 GND
3B3 16 33 3A3
3B4 17 32 3A4
VCC 18 31 VCC
4B1 19 30 4A1
4B2 20 29 4A2
GND 21 28 GND
4B3 22 27 4A3
4B4 23 26 4A4
4OE 24 25 3OE

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16244DL	CBT16244
		Tape and reel	SN74CBT16244DLR	
	TSSOP − DGG	Tape and reel	SN74CBT16244DGGR	CBT16244
	TVSOP − DGV	Tape and reel	SN74CBT16244DGVR	CY244
−55°C to 125°C	CFP − WD	Tube	SNJ54CBT16244WD	SNJ54CBT16244WD

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 4-bit bus switch)

INPUT $\overline{OE}$	OUTPUTS A, B
L	A port = B port
H	Disconnect

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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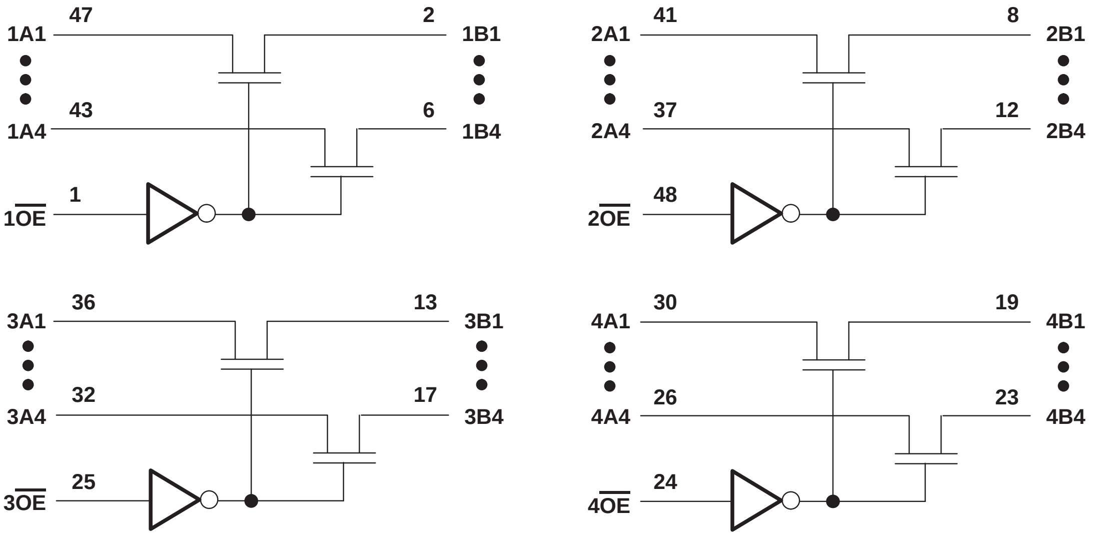
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54CBT16244		SN74CBT16244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4	5.5	4	5.5	V
V_{IH}	High-level control input voltage	2		2		V
V_{IL}	Low-level control input voltage		0.8		0.8	V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54CBT16244			SN74CBT16244			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2			−1.2	V
I_I		V_{CC} = 0	V_I = 5.5 V				10			10	μA
		V_{CC} = 5.5 V	V_I = 5.5 V or GND				±1			±1	
I_{CC}		V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,				3.2			3	μA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				2.5			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				2.5			2.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			4.5			4.5		pF
r_{on}§		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA			20			20	Ω
		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA		5	10		5	7	
			V_I = 0,	I_I = 30 mA		5	10		5	7	
			V_I = 2.4 V,	I_I = 15 mA		8	14		8	12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

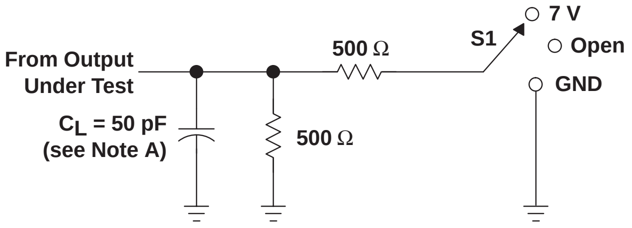
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBT16244				SN74CBT16244				UNIT
			V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A				0.8*		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		10.3	1	9.2		5.5	1	5.1	ns
t_{dis}	$\overline{OE}$	A or B		9.7	1	8.2		5.2	1	5.4	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

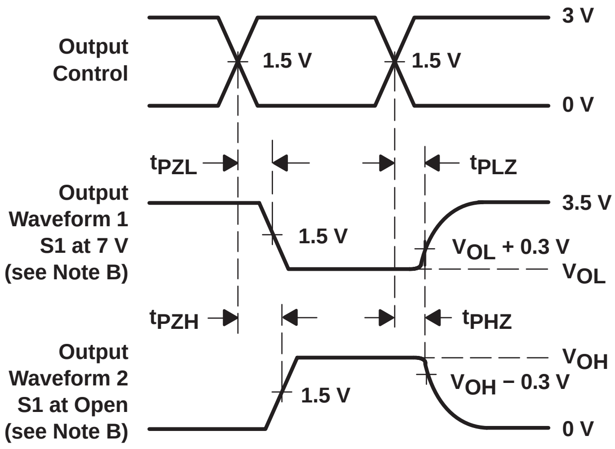
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

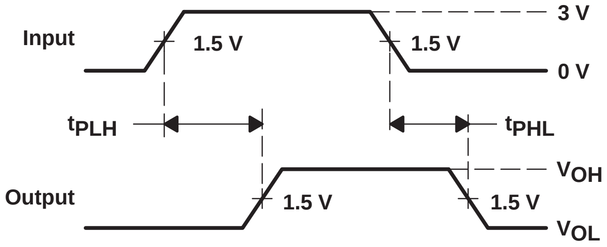
PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

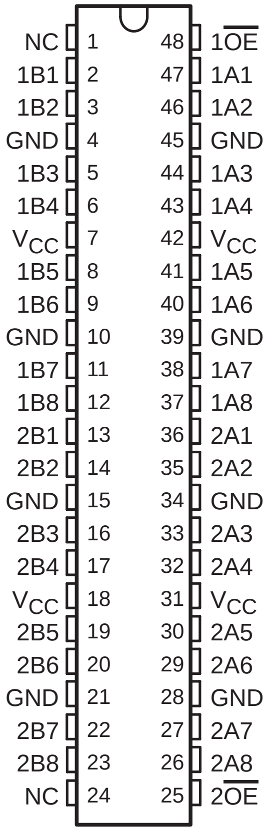
Figure 1. Load Circuit and Voltage Waveforms

SN74CBT16245
16-BIT FET BUS SWITCH

SCDS070C − JULY 1998 − REVISED OCTOBER 2000

- **Member of Texas Instruments' Widebus™ Family**
- **Standard '16245-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1 48 $1\overline{OE}$
1B1 2 47 1A1
1B2 3 46 1A2
GND 4 45 GND
1B3 5 44 1A3
1B4 6 43 1A4
V_{CC} 7 42 V_{CC}
1B5 8 41 1A5
1B6 9 40 1A6
GND 10 39 GND
1B7 11 38 1A7
1B8 12 37 1A8
2B1 13 36 2A1
2B2 14 35 2A2
GND 15 34 GND
2B3 16 33 2A3
2B4 17 32 2A4
V_{CC} 18 31 V_{CC}
2B5 19 30 2A5
2B6 20 29 2A6
GND 21 28 GND
2B7 22 27 2A7
2B8 23 26 2A8
NC 24 25 $2\overline{OE}$

NC − No internal connection

description

The SN74CBT16245 device provides 16 bits of high-speed TTL-compatible bus switching in a standard '16245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as two 8-bit low-impedance switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on, and data can flow from the A port to the B port, or vice versa. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16245DL	CBT16245
		Tape and reel	SN74CBT16245DLR	
	TSSOP − DGG	Tape and reel	SN74CBT16245DGGR	CBT16245
	TVSOP − DGV	Tape and reel	SN74CBT16245DGVR	CY245

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 8-bit bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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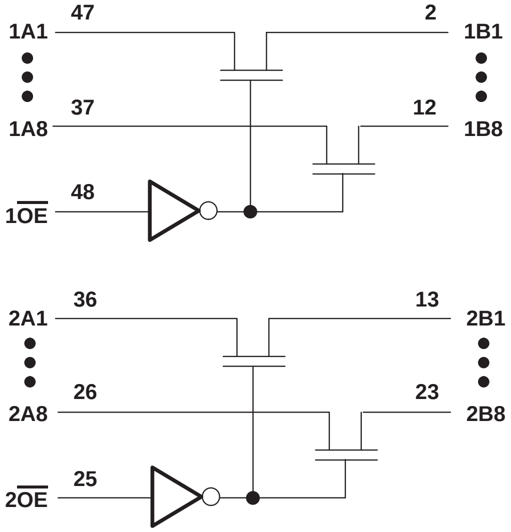
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	µA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			4.5		pF
r_{on}§		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		8	12	

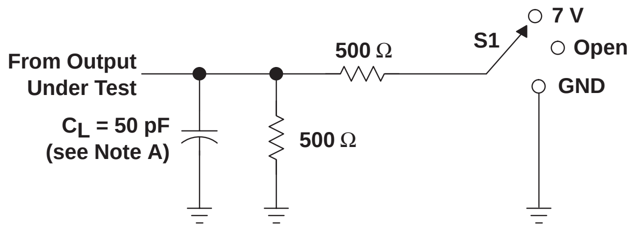
† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		6.1	1.2	5.6	ns
t_{dis}	$\overline{OE}$	A or B		7.5	3.9	7.7	ns

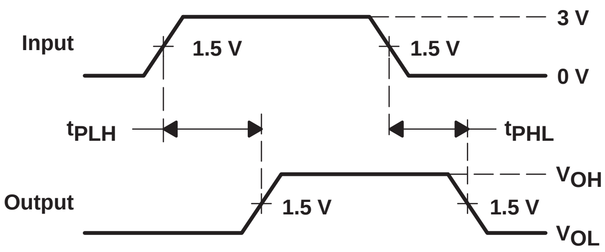
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

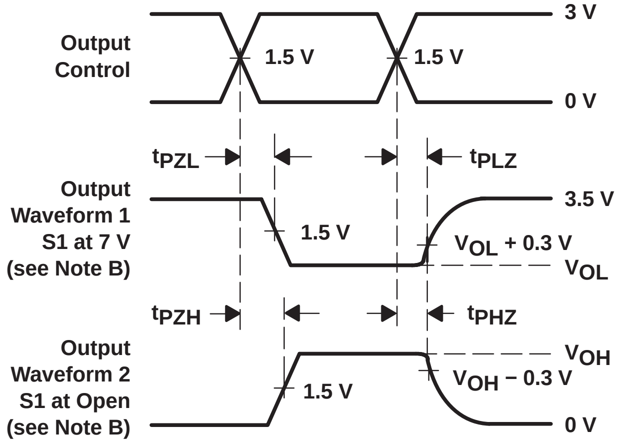

From Output
Under Test
C$_L$ = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t$_{PLH}$
t$_{PHL}$
Output
1.5 V
1.5 V
V$_{OH}$
V$_{OL}$

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t$_{PZL}$
t$_{PLZ}$
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V$_{OL}$ + 0.3 V
V$_{OL}$
t$_{PZH}$
t$_{PHZ}$
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V$_{OH}$
V$_{OH}$ − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

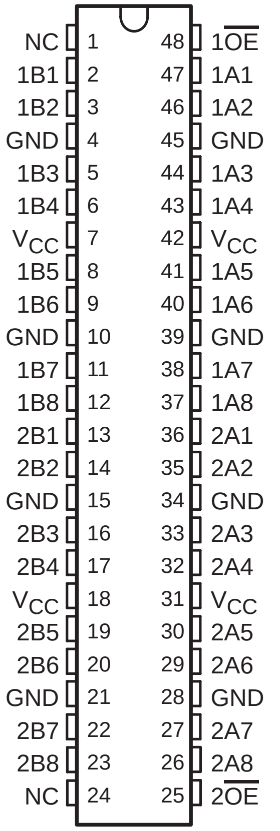
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTK16245
16-BIT FET BUS SWITCH
WITH ACTIVE-CLAMP UNDERSHOOT-PROTECTION CIRCUIT

SCDS105D − APRIL 2000 − REVISED NOVEMBER 2001

- **Member of the Texas Instruments Widebus™ Family**
- **Standard ’16245-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Active-Clamp Undershoot-Protection Circuit on the I/Os Clamps Undershoots up to −2 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1 48 1$\overline{\text{OE}}$
1B1 2 47 1A1
1B2 3 46 1A2
GND 4 45 GND
1B3 5 44 1A3
1B4 6 43 1A4
V_{CC} 7 42 V_{CC}
1B5 8 41 1A5
1B6 9 40 1A6
GND 10 39 GND
1B7 11 38 1A7
1B8 12 37 1A8
2B1 13 36 2A1
2B2 14 35 2A2
GND 15 34 GND
2B3 16 33 2A3
2B4 17 32 2A4
V_{CC} 18 31 V_{CC}
2B5 19 30 2A5
2B6 20 29 2A6
GND 21 28 GND
2B7 22 27 2A7
2B8 23 26 2A8
NC 24 25 2$\overline{\text{OE}}$

NC − No internal connection

description

The SN74CBTK16245 device provides 16 bits of high-speed TTL-compatible bus switching in a standard ’16245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The A and B ports have an active-clamp undershoot-protection circuit. When there is an undershoot, the active-clamp circuit is enabled, and current from V_{CC} is supplied to clamp the output, preventing the pass transistor from turning on.

The device is organized as two 8-bit low-impedance switches with separate output-enable ($\overline{\text{OE}}$) inputs. When $\overline{\text{OE}}$ is low, the switch is on, and data can flow from the A port to the B port, or vice versa. When $\overline{\text{OE}}$ is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBTK16245DL	CBTK16245
		Tape and reel	SN74CBTK16245DLR	
	TSSOP − DGG	Tape and reel	SN74CBTK16245DGGR	CBTK16245
	TVSOP − DGV	Tape and reel	SN74CBTK16245DGVR	CP245

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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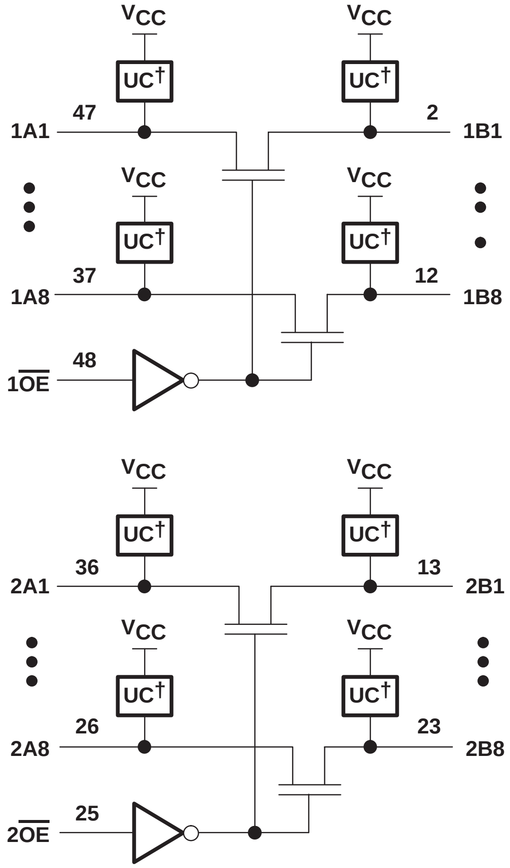
FUNCTION TABLE
(each 8-bit bus switch)

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)


VCC
UC†
1A1
47
2
1B1
1A8
37
12
1B8
1$\overline{\text{OE}}$
48
2A1
36
13
2B1
2A8
26
23
2B8
2$\overline{\text{OE}}$
25

† Undershoot clamp

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{IKU}		V_{CC} = 5.5 V,	0 mA ≥ I_I ≥ −50 mA,	$\overline{OE}$ = 5.5 V			−2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 5.5 V				20	μA
I_{CC}		V_{CC} = 5.5 V,	V_I = V_{CC} or GND,	I_O = 0			3	μA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5.5		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		8	12	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL-voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		7.4	1.6	4.9	ns
t_{dis}	$\overline{OE}$	A or B		7.4	4.2	7.5	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP[‡]	MAX	UNIT
V_{OUTU}	See Figures 1 and 2, and Table 1	2	$V_{OH}-0.3$		V

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

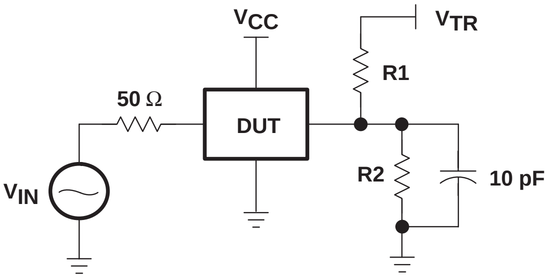


Figure 1. Device Test Setup

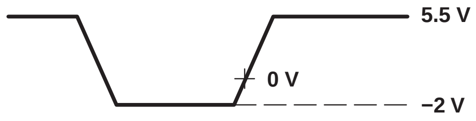


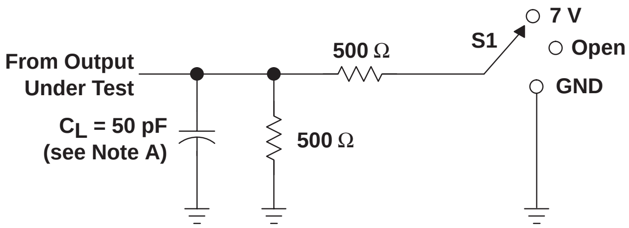
Figure 2. Transient Input Voltage Waveform

Table 1. Device Test Conditions

PARAMETER	VALUE	UNIT
B port under test[§]	See Figure 1	
V_{IN}	See Figure 2	V
t_w	20	ns
t_r	2	ns
t_f	2	ns
R1 = R2	100	kΩ
V_{TR}	11	V
V_{CC}	5.5	V

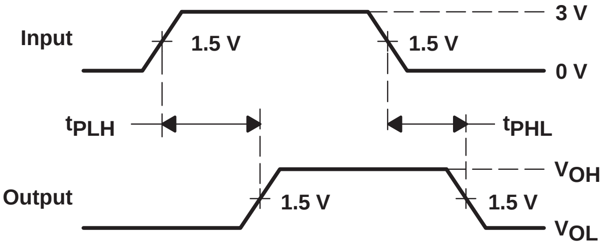
[§] Other B-port outputs are open.

PARAMETER MEASUREMENT INFORMATION

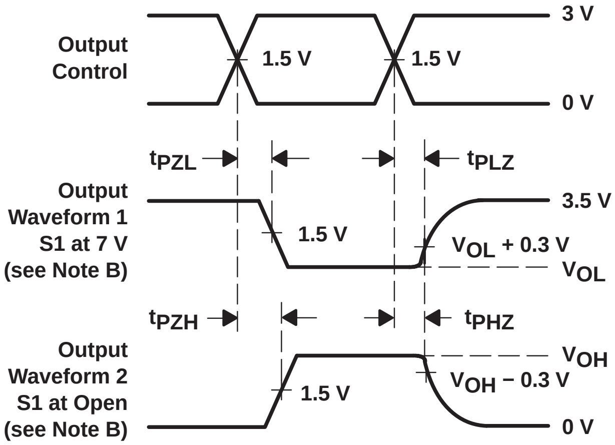

From Output
Under Test
500 Ω
S1
7 V
Open
GND
C_L = 50 pF
(see Note A)
500 Ω

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuit and Voltage Waveforms

SN74CBT16210
20-BIT FET BUS SWITCH

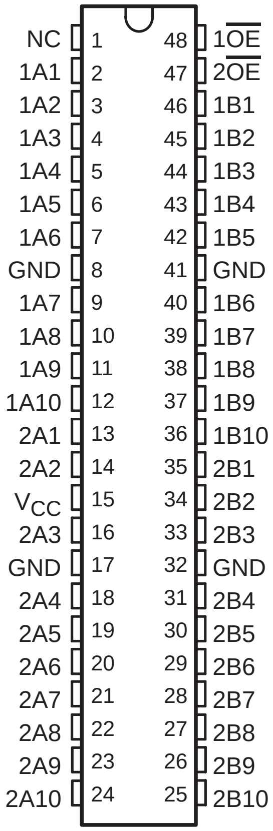
- **Member of Texas Instruments' Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

description

The SN74CBT16210 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as a dual 10-bit bus switch with separate output-enable ($\overline{\text{OE}}$) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When $\overline{\text{OE}}$ is low, the associated 10-bit bus switch is on, and port A is connected to port B. When $\overline{\text{OE}}$ is high, the switch is open, and the high-impedance state exists between the ports.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1 48 1OE
1A1 2 47 2OE
1A2 3 46 1B1
1A3 4 45 1B2
1A4 5 44 1B3
1A5 6 43 1B4
1A6 7 42 1B5
GND 8 41 GND
1A7 9 40 1B6
1A8 10 39 1B7
1A9 11 38 1B8
1A10 12 37 1B9
2A1 13 36 1B10
2A2 14 35 2B1
VCC 15 34 2B2
2A3 16 33 2B3
GND 17 32 GND
2A4 18 31 2B4
2A5 19 30 2B5
2A6 20 29 2B6
2A7 21 28 2B7
2A8 22 27 2B8
2A9 23 26 2B9
2A10 24 25 2B10

NC − No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16210DL	CBT16210
		Tape and reel	SN74CBT616210DLR	
	TSSOP − DGG	Tape and reel	SN74CBT16210DGGR	CBT16210
	TVSOP − DGV	Tape and reel	SN74CBT16210DGVR	CY210

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 10-bit bus switch)

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

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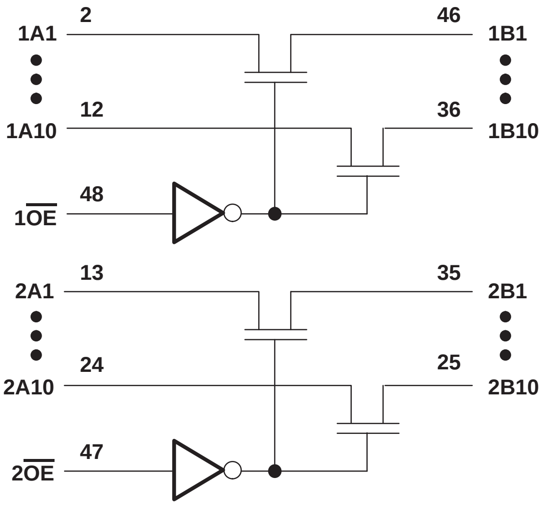
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V
Continuous channel current . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . 70°C/W
DGV package . . . . 58°C/W
DL package . . . . 63°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0 V,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				4.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5.5		pF
r_{on}§		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		8	12	

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

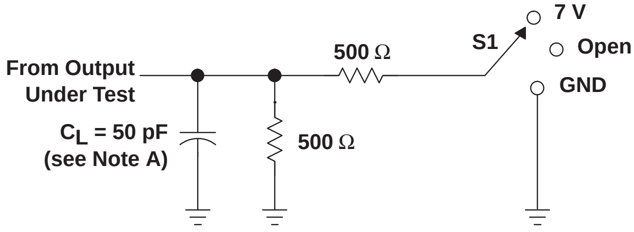
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		9.3	3.3	8.6	ns
t_{dis}	$\overline{OE}$	A or B		7.1	2.8	7.9	ns

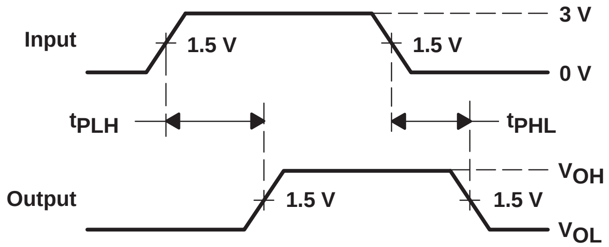
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

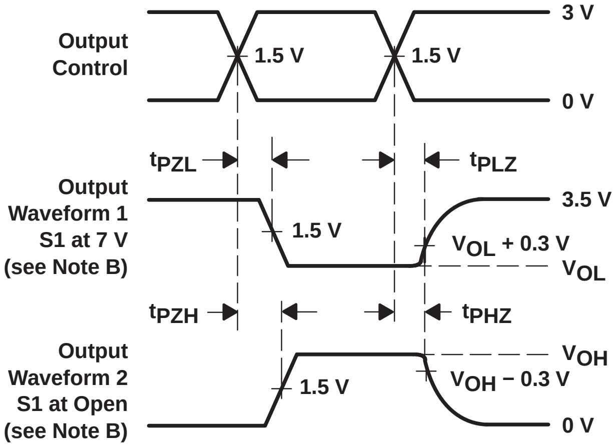

7 V
S1
Open
500 Ω
From Output
Under Test
GND
C_L = 50 pF
(see Note A)
500 Ω

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SN74CBTD16210
20-BIT FET BUS SWITCH
WITH LEVEL SHIFTING

SCDS049H − MARCH 1998 − REVISED JULY 2002

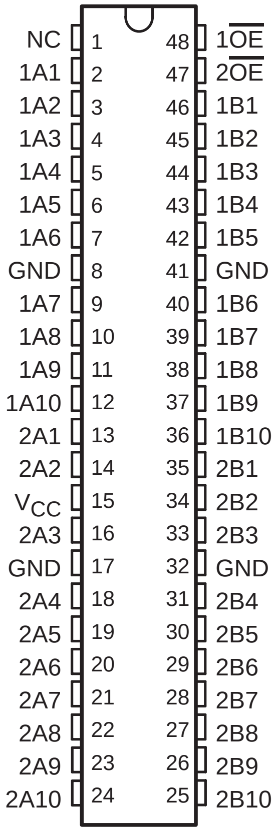
- **Member of Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Designed to Be Used in Level-Shifting Applications**

description/ordering information

The SN74CBTD16210 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. A diode to V_{CC} is integrated in the circuit to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

The device is organized as a dual 10-bit bus switch with separate output-enable ($\overline{OE}$) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When $\overline{OE}$ is low, the associated 10-bit bus switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the ports.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1
1A1 2
1A2 3
1A3 4
1A4 5
1A5 6
1A6 7
GND 8
1A7 9
1A8 10
1A9 11
1A10 12
2A1 13
2A2 14
VCC 15
2A3 16
GND 17
2A4 18
2A5 19
2A6 20
2A7 21
2A8 22
2A9 23
2A10 24
48 1OE
47 2OE
46 1B1
45 1B2
44 1B3
43 1B4
42 1B5
41 GND
40 1B6
39 1B7
38 1B8
37 1B9
36 1B10
35 2B1
34 2B2
33 2B3
32 GND
31 2B4
30 2B5
29 2B6
28 2B7
27 2B8
26 2B9
25 2B10

NC − No internal connection

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBTD16210DL	CBTD16210
		Tape and reel	SN74CBTD16210DLR	
	TSSOP − DGG	Tape and reel	SN74CBTD16210DGGR	CBTD16210
	TVSOP − DGV	Tape and reel	SN74CBTD16210DGVR	CYD210

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 10-bit bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Z

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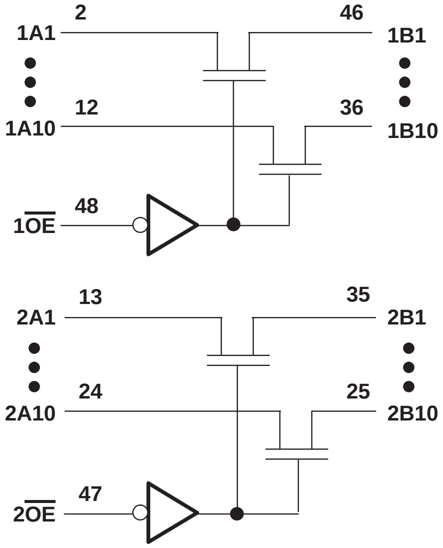
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V
Continuous channel current . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . 70°C/W
DGV package . . . . 58°C/W
DL package . . . . 63°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

---

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}		See Figure 2						
I_I		V_{CC} = 0 V,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1.5	mA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				4.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5.5		pF
r_{on}[§]		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		35	50	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

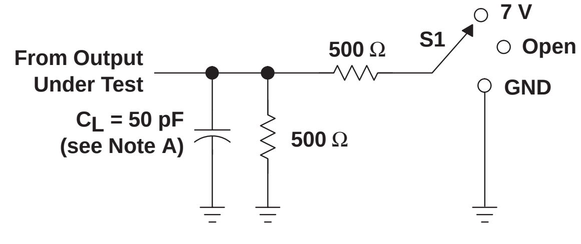
[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}[¶]	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B	1.5	9.8	ns
t_{dis}	$\overline{OE}$	A or B	1.5	8.9	ns

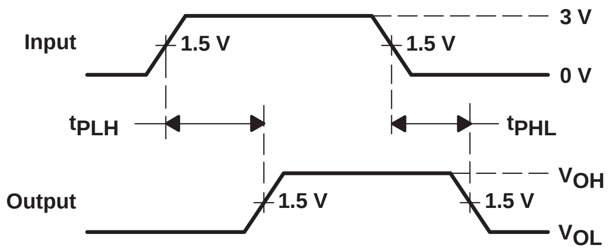
[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

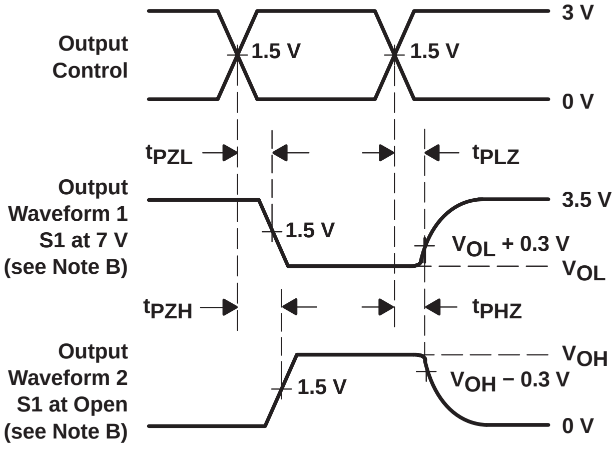

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

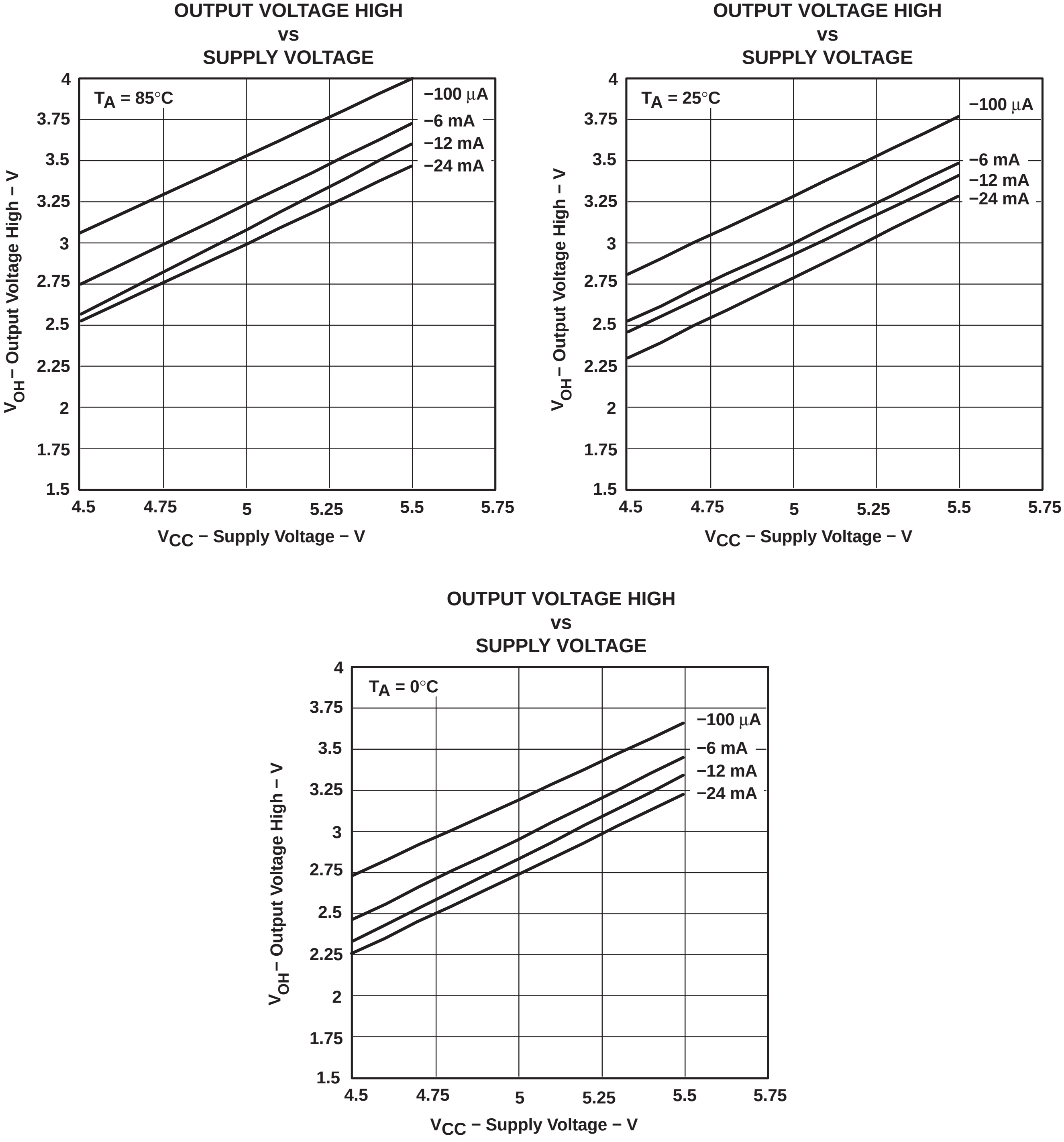

Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS


OUTPUT VOLTAGE HIGH vs SUPPLY VOLTAGE

OUTPUT VOLTAGE HIGH vs SUPPLY VOLTAGE

OUTPUT VOLTAGE HIGH vs SUPPLY VOLTAGE

Figure 2. V_{OH} Values

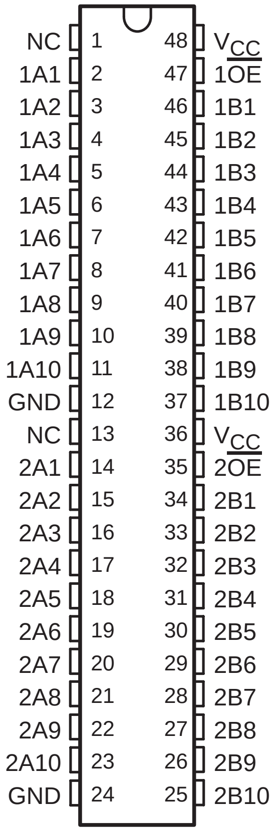
- **Member of Texas Instruments' Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

description

The SN74CBT16861 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one dual 10-bit switch with separate output-enable ($\overline{\text{OE}}$) input. When $\overline{\text{OE}}$ is low, the switch is on, and port A is connected to port B. When $\overline{\text{OE}}$ is high, the switch is open, and the high-impedance state exists between the two ports.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1 48 V_{CC}
1A1 2 47 $1\overline{OE}$
1A2 3 46 1B1
1A3 4 45 1B2
1A4 5 44 1B3
1A5 6 43 1B4
1A6 7 42 1B5
1A7 8 41 1B6
1A8 9 40 1B7
1A9 10 39 1B8
1A10 11 38 1B9
GND 12 37 1B10
NC 13 36 V_{CC}
2A1 14 35 $2\overline{OE}$
2A2 15 34 2B1
2A3 16 33 2B2
2A4 17 32 2B3
2A5 18 31 2B4
2A6 19 30 2B5
2A7 20 29 2B6
2A8 21 28 2B7
2A9 22 27 2B8
2A10 23 26 2B9
GND 24 25 2B10

NC − No internal connection

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16861DL	CBT16861
		Tape and reel	SN74CBT16861DLR	
	TSSOP − DGG	Tape and reel	SN74CBT16861DGGR	CBT16861
	TVSOP − DGV	Tape and reel	SN74CBT16861DGVR	CY861

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 10-bit bus switch)

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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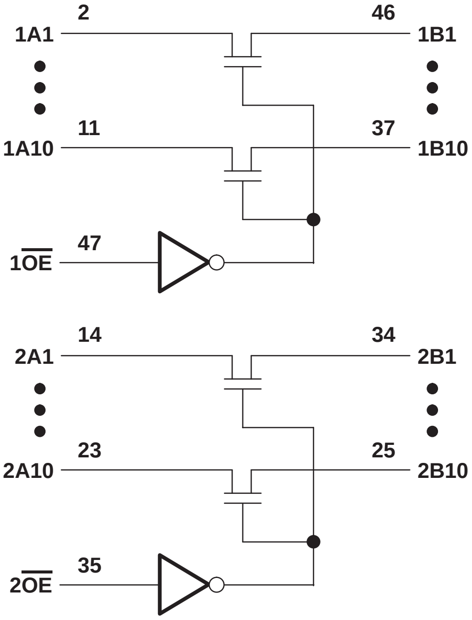
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	µA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5.5		pF
r_{on}§		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	22	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

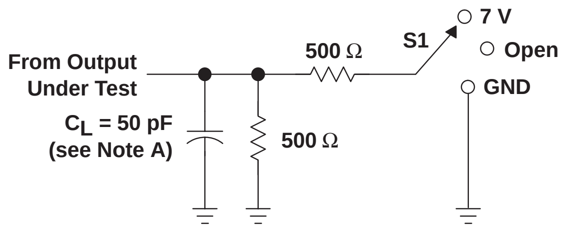
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B	2.7	6.3	1.7	6.5	ns
t_{dis}	$\overline{OE}$	A or B	1.5	8	1.8	7.1	ns

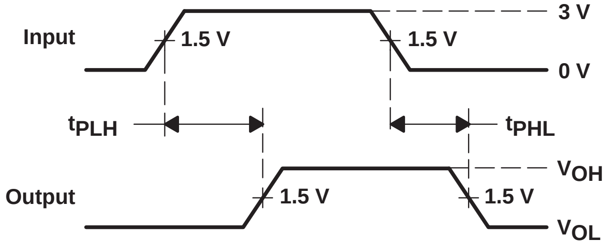
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

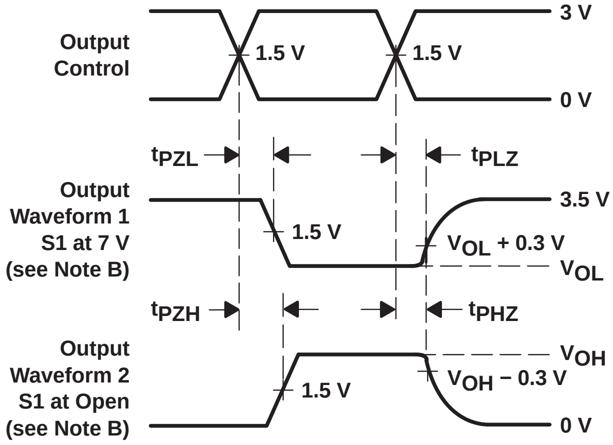

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

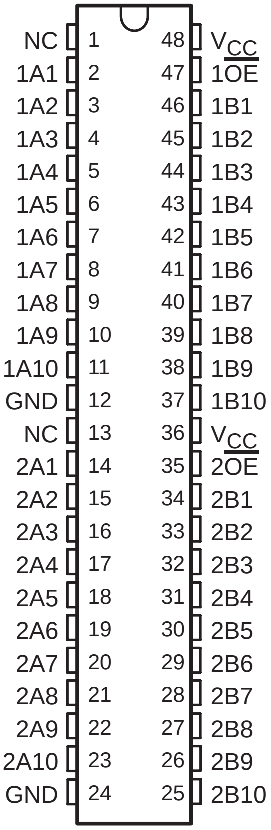
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTR16861
20-BIT FET BUS SWITCH

SCDS078D − JULY 1998 − REVISED NOVEMBER 2001

- **Member of the Texas Instruments Widebus™ Family**
- **25-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1 48 V_{CC}
1A1 2 47 $\overline{1OE}$
1A2 3 46 1B1
1A3 4 45 1B2
1A4 5 44 1B3
1A5 6 43 1B4
1A6 7 42 1B5
1A7 8 41 1B6
1A8 9 40 1B7
1A9 10 39 1B8
1A10 11 38 1B9
GND 12 37 1B10
NC 13 36 V_{CC}
2A1 14 35 $\overline{2OE}$
2A2 15 34 2B1
2A3 16 33 2B2
2A4 17 32 2B3
2A5 18 31 2B4
2A6 19 30 2B5
2A7 20 29 2B6
2A8 21 28 2B7
2A9 22 27 2B8
2A10 23 26 2B9
GND 24 25 2B10

NC − No internal connection

description

The SN74CBTR16861 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one dual 10-bit switch with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

The device has equivalent 25-Ω series resistors to reduce signal-reflection noise. This eliminates the need for external terminating resistors.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBTR16861DL	CBTR16861
		Tape and reel	SN74CBTR16861DLR	
	TSSOP − DGG	Tape and reel	SN74CBTR16861DGGR	CBTR16861
	TVSOP − DGV	Tape and reel	SN74CBTR16861DGVR	CZ861

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 10-bit bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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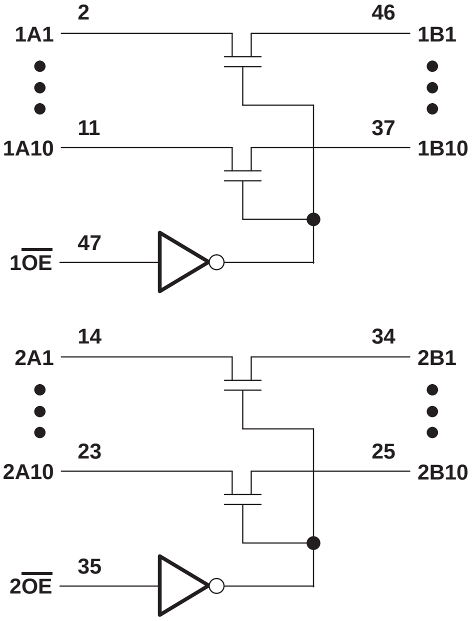
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V
Continuous channel current . . . . 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . 70°C/W
DGV package . . . . 58°C/W
DL package . . . . 63°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	µA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5		pF
r_{on}§		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA	20	37	50	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA	20	33	47	
				I_I = 30 mA	20	33	47	
			V_I = 2.4 V,	I_I = 15 mA	20	35	48	

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

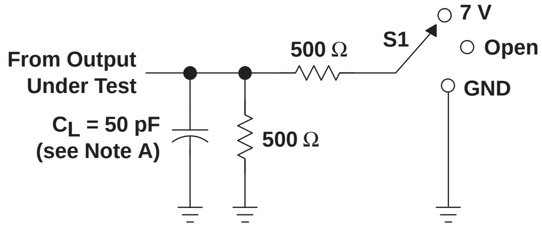
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		1.25		1.25	ns
t_{en}	$\overline{OE}$	A or B	3.1	9	2.7	8.6	ns
t_{dis}	$\overline{OE}$	A or B	2.7	6.3	2.3	6.9	ns

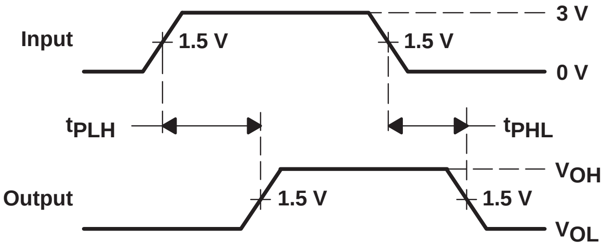
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

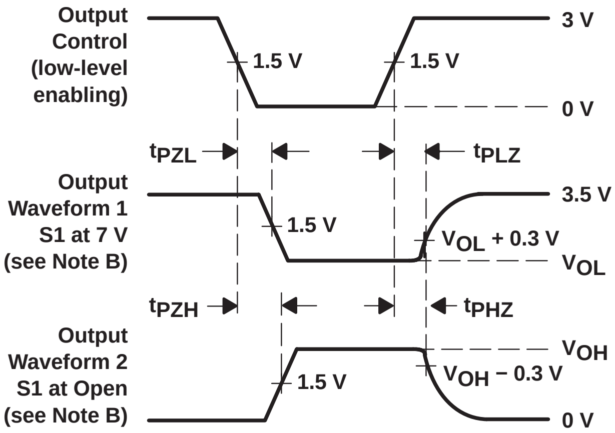

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
(low-level
enabling)
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

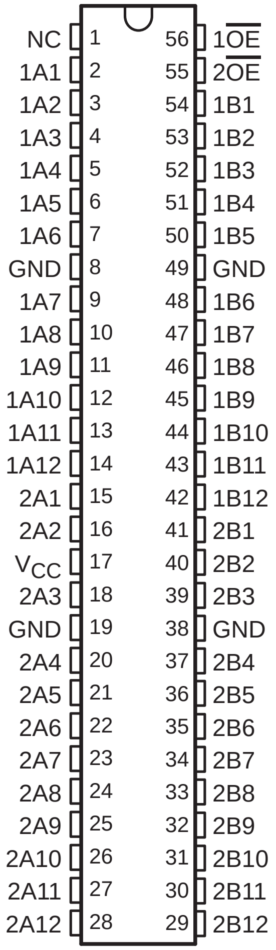
Figure 1. Load Circuit and Voltage Waveforms

SN74CBT16211A
24-BIT FET BUS SWITCH

SCDS028M − JULY 1995 − REVISED SEPTEMBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1 56 $1\overline{OE}$
1A1 2 55 $2\overline{OE}$
1A2 3 54 1B1
1A3 4 53 1B2
1A4 5 52 1B3
1A5 6 51 1B4
1A6 7 50 1B5
GND 8 49 GND
1A7 9 48 1B6
1A8 10 47 1B7
1A9 11 46 1B8
1A10 12 45 1B9
1A11 13 44 1B10
1A12 14 43 1B11
2A1 15 42 1B12
2A2 16 41 2B1
V_{CC} 17 40 2B2
2A3 18 39 2B3
GND 19 38 GND
2A4 20 37 2B4
2A5 21 36 2B5
2A6 22 35 2B6
2A7 23 34 2B7
2A8 24 33 2B8
2A9 25 32 2B9
2A10 26 31 2B10
2A11 27 30 2B11
2A12 28 29 2B12

NC − No internal connection

description/ordering information

The SN74CBT16211A provides 24 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a dual 12-bit bus switch or single 24-bit bus switch. When $1\overline{OE}$ is low, 1A is connected to 1B. When $2\overline{OE}$ is low, 2A is connected to 2B.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16211ADL	CBT16211A
		Tape and reel	SN74CBT16211ADLR	
	TSSOP − DGG	Tape and reel	SN74CBT16211ADGGR	CBT16211A
	TVSOP − DGV	Tape and reel	SN74CBT16211ADGVR	CY211A
	VFBGA − GQL	Tape and reel	SN74CBT16211AGQLR	CY211A
	VFBGA − ZQL (Pb-free)		SN74CBT16211AZQLR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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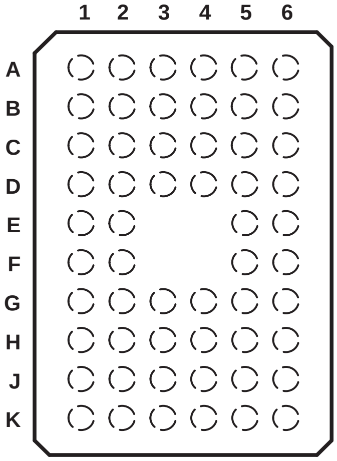
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

GQL OR ZQL PACKAGE
(TOP VIEW)


1
2
3
4
5
6
A
B
C
D
E
F
G
H
J
K

terminal assignments

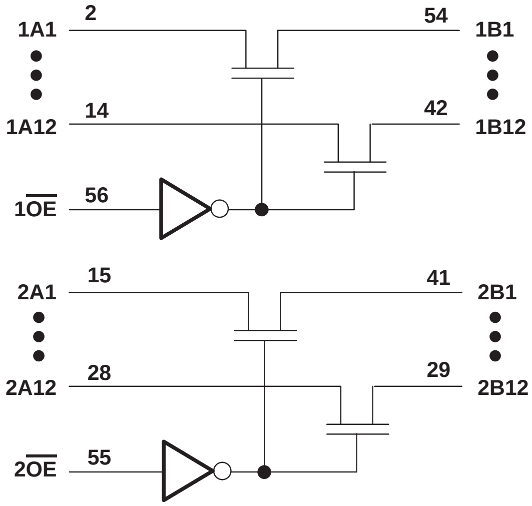
	1	2	3	4	5	6
A	1A2	1A1	NC	$1\overline{OE}$	$2\overline{OE}$	1B1
B	1A5	1A4	1A3	1B2	1B3	1B4
C	1A7	GND	1A6	1B5	GND	1B6
D	1A10	1A8	1A9	1B8	1B7	1B9
E	1A12	1A11			1B10	1B11
F	2A1	2A2			2B1	1B12
G	V_{CC}	GND	2A3	2B3	GND	2B2
H	2A4	2A5	2A6	2B6	2B5	2B4
J	2A7	2A8	2A9	2B9	2B8	2B7
K	2A10	2A11	2A12	2B12	2B11	2B10

NC − No internal connection

FUNCTION TABLE
(each 12-bit bus switch)

INPUTS		INPUTS/OUTPUTS	
$1\overline{OE}$	$2\overline{OE}$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

logic diagram (positive logic)


1A1
2
54
1B1
1A12
14
42
1B12
$1\overline{OE}$
56
2A1
15
41
2B1
2A12
28
29
2B12
$2\overline{OE}$
55

Pin numbers shown are for the DGG, DGV, and DL packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
	GQL/ZQL package	42°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0 V,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(off)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5.5		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		8	12	

‡ All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

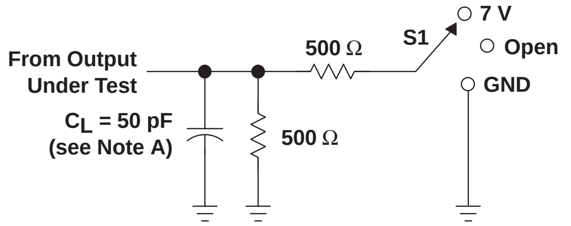
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}†	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		9.3	3.3	8.6	ns
t_{dis}	$\overline{OE}$	A or B		7.1	2.8	7.9	ns

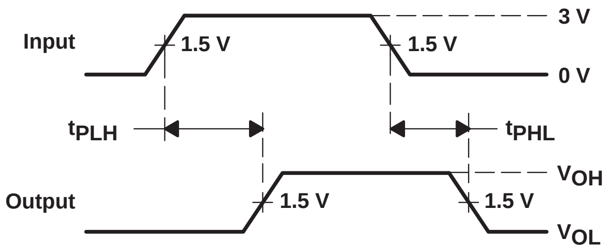
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

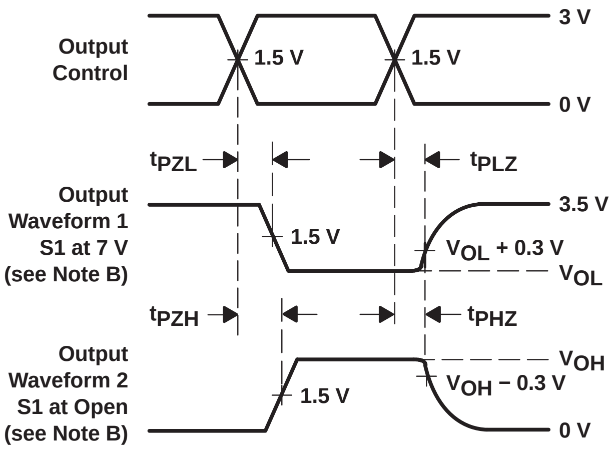

7 V
500 Ω
S1
Open
From Output Under Test
GND
C_L = 50 pF (see Note A)
500 Ω

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


3 V
Input
1.5 V
1.5 V
0 V
t_{PLH}
t_{PHL}
V_{OH}
Output
1.5 V
1.5 V
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


3 V
Output Control
1.5 V
1.5 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
3.5 V
1.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
V_{OH}
V_{OH} − 0.3 V
1.5 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

SN74CBTD16211
24-BIT FET BUS SWITCH
WITH LEVEL SHIFTING

SCDS048H − MARCH 1998 − REVISED JULY 2002

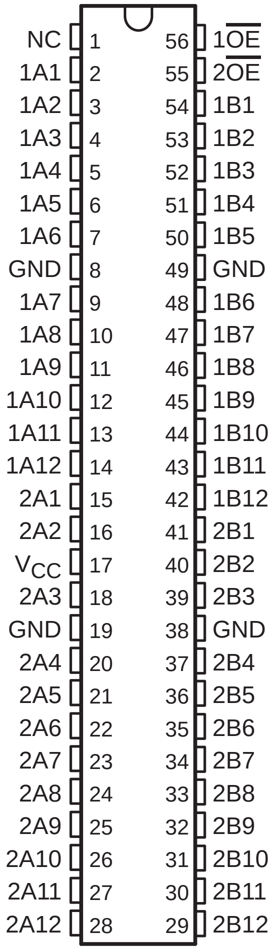
- **Member of Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Designed to Be Used in Level-Shifting Applications**

description/ordering information

The SN74CBTD16211 provides 24 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. A diode to V_{CC} is integrated in the circuit to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

The device is organized as a dual 12-bit bus switch with separate output-enable ($\overline{\text{OE}}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When $\overline{\text{OE}}$ is low, the associated 12-bit bus switch is on, and port A is connected to port B. When $\overline{\text{OE}}$ is high, the switch is open, and the high-impedance state exists between the ports.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1 56 1$\overline{\text{OE}}$
1A1 2 55 2$\overline{\text{OE}}$
1A2 3 54 1B1
1A3 4 53 1B2
1A4 5 52 1B3
1A5 6 51 1B4
1A6 7 50 1B5
GND 8 49 GND
1A7 9 48 1B6
1A8 10 47 1B7
1A9 11 46 1B8
1A10 12 45 1B9
1A11 13 44 1B10
1A12 14 43 1B11
2A1 15 42 1B12
2A2 16 41 2B1
V_{CC} 17 40 2B2
2A3 18 39 2B3
GND 19 38 GND
2A4 20 37 2B4
2A5 21 36 2B5
2A6 22 35 2B6
2A7 23 34 2B7
2A8 24 33 2B8
2A9 25 32 2B9
2A10 26 31 2B10
2A11 27 30 2B11
2A12 28 29 2B12

NC − No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBTD16211DL	CBTD16211
		Tape and reel	SN74CBTD16211DLR	
	TSSOP − DGG	Tape and reel	SN74CBTD16211DGGR	CBTD16211
	TVSOP − DGV	Tape and reel	SN74CBTD16211DGVR	CYD211

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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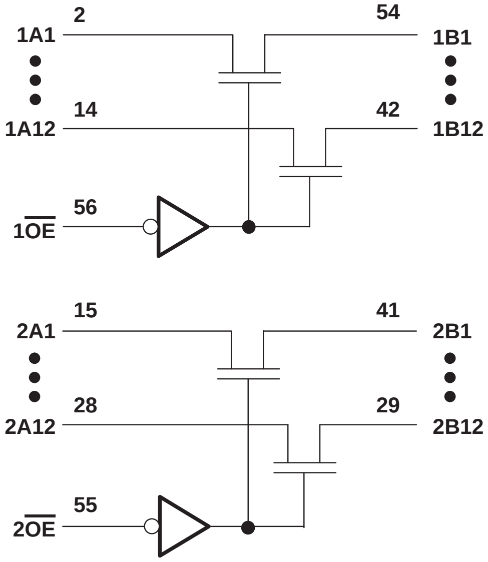
FUNCTION TABLE
(each 12-bit bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

---

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}		See Figure 2						
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1.5	mA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5.5		pF
r_{on}[§]		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		35	50	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

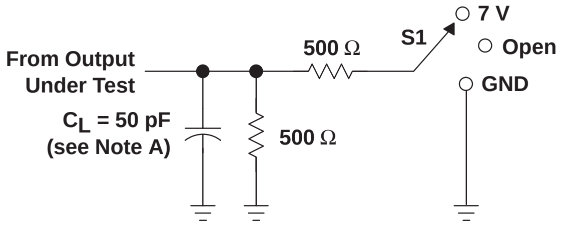
[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}[¶]	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B	1.5	9.8	ns
t_{dis}	$\overline{OE}$	A or B	1.5	8.9	ns

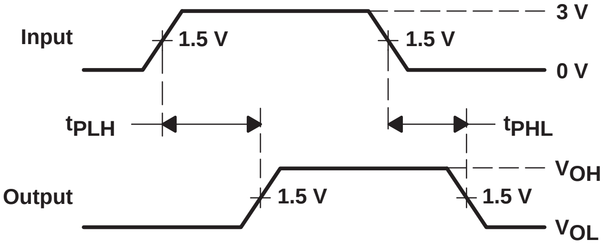
[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

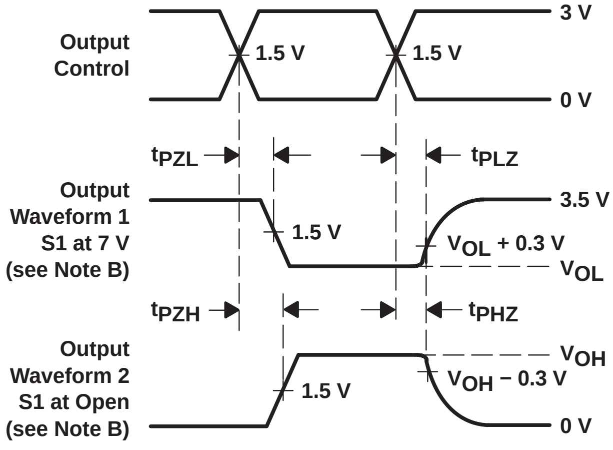

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

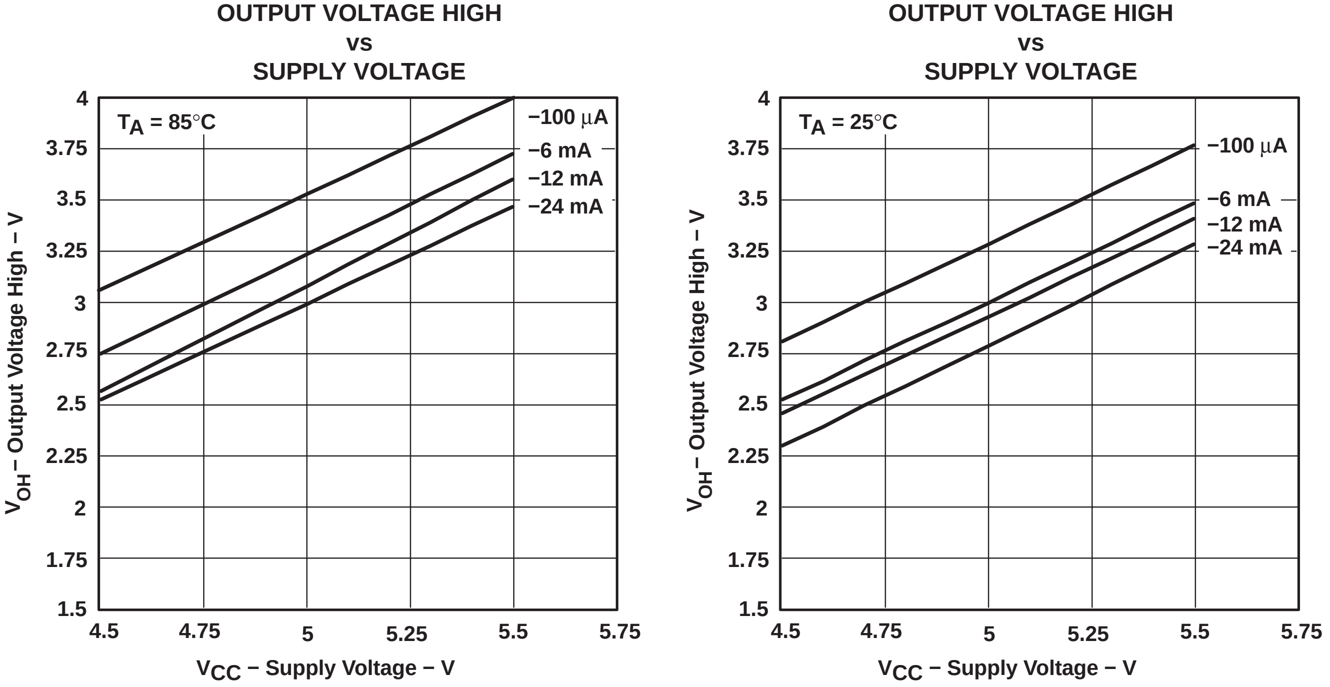

Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



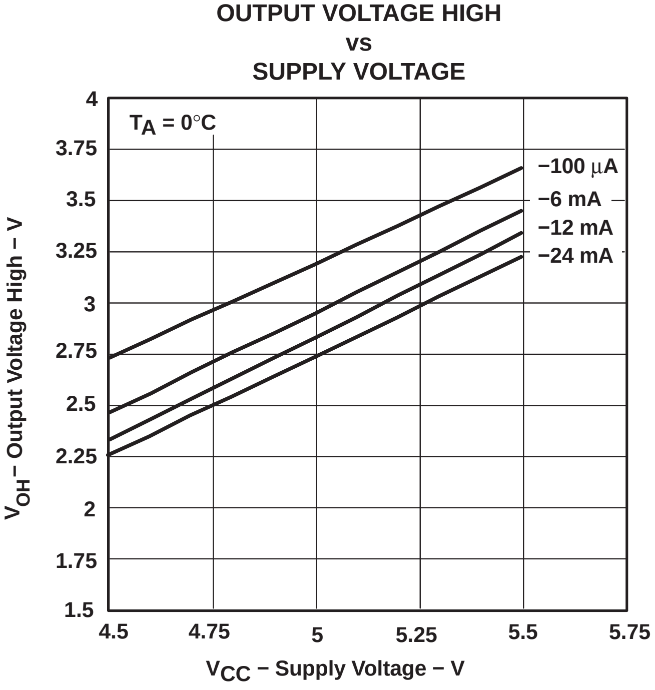


Figure 2. V_{OH} Values

SN74CBTH16211
24-BIT FET BUS SWITCH
WITH BUS HOLD

SCDS062C − JUNE 1998 − REVISED NOVEMBER 2001

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Bus Hold on Data Inputs/Outputs Eliminates the Need for External Pullup/Pulldown Resistors**

description

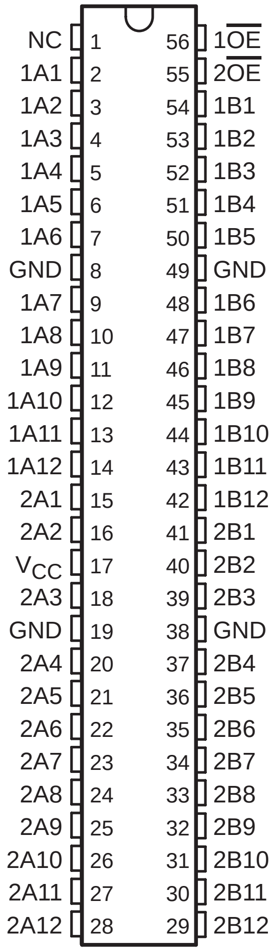
The SN74CBTH16211 provides 24 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 12-bit bus switches with separate output-enable ($\overline{\text{OE}}$) inputs. It can be used as two 12-bit bus switches or one 24-bit bus switch. When $\overline{\text{OE}}$ is low, the associated 12-bit bus switch is on, and the A port is connected to the B port. When $\overline{\text{OE}}$ is high, the switch is open, and a high-impedance state exists between the two ports.

Active bus-hold circuitry is provided to hold unused or floating A and B ports at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1 56 1OE
1A1 2 55 2OE
1A2 3 54 1B1
1A3 4 53 1B2
1A4 5 52 1B3
1A5 6 51 1B4
1A6 7 50 1B5
GND 8 49 GND
1A7 9 48 1B6
1A8 10 47 1B7
1A9 11 46 1B8
1A10 12 45 1B9
1A11 13 44 1B10
1A12 14 43 1B11
2A1 15 42 1B12
2A2 16 41 2B1
VCC 17 40 2B2
2A3 18 39 2B3
GND 19 38 GND
2A4 20 37 2B4
2A5 21 36 2B5
2A6 22 35 2B6
2A7 23 34 2B7
2A8 24 33 2B8
2A9 25 32 2B9
2A10 26 31 2B10
2A11 27 30 2B11
2A12 28 29 2B12

NC − No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBTH16211DL	CBTH16211
		Tape and reel	SN74CBTH16211DLR	
	TSSOP − DGG	Tape and reel	SN74CBTH16211DGGR	CBTH16211
	TVSOP − DGV	Tape and reel	SN74CBTH16211DGVR	CYH211

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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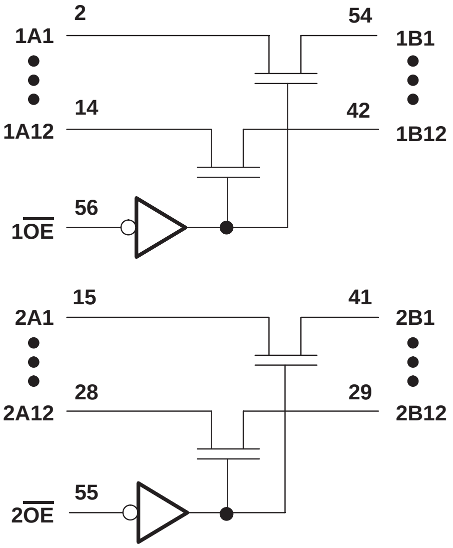
FUNCTION TABLE
(each bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V
Continuous channel current . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . 64°C/W
DGV package . . . . 48°C/W
DL package . . . . 56°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I	Control inputs	V_{CC} = 0 V,	V_I = 5.5 V				±10	µA
	All inputs	V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±10	
I_{BHL}[‡]		V_{CC} = 4.5 V,	V_I = 0.8 V		100			µA
I_{BHH}[§]		V_{CC} = 4.5 V,	V_I = 2 V		−100			µA
I_{BHLO}[¶]		V_{CC} = 5.5 V,	V_I = 0 to 5.5 V		500			µA
I_{BHHO}[#]		V_{CC} = 5.5 V,	V_I = 0 to 5.5 V		−500			µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}[‖]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
r_{on}[☆]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		8	12	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] The bus hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

[§] The bus hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

[¶] An external driver must source at least I_{BHLO} to switch this node from low to high.

[#] An external driver must sink at least I_{BHHO} to switch this node from high to low.

[‖] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

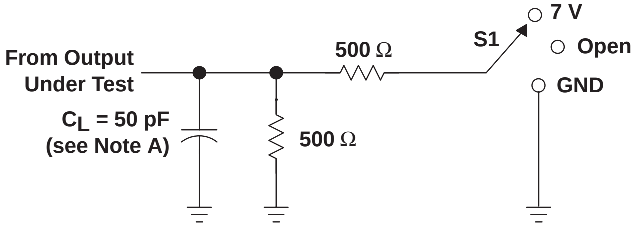
[☆] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[□]	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		9.9	1	9.6	ns
t_{dis}	$\overline{OE}$	A or B		9.5	1	8.3	ns

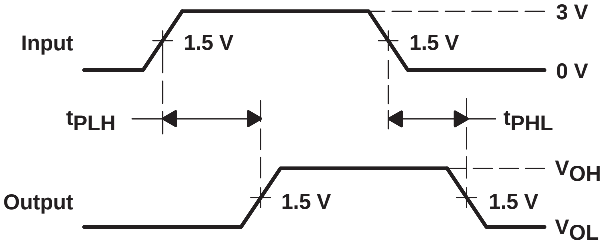
[□] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

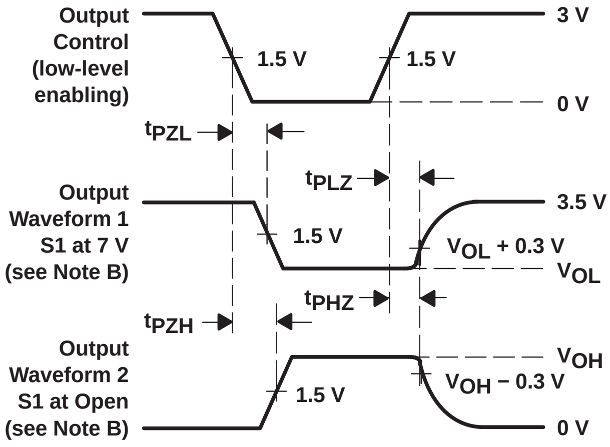

From Output Under Test
C_L = 50 pF (see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output Control (low-level enabling)
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PHZ}
t_{PZH}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SN74CBTS16211
24-BIT FET BUS SWITCH
WITH SCHOTTKY DIODE CLAMPING

SCDS050D − MARCH 1998 − REVISED OCTOBER 2000

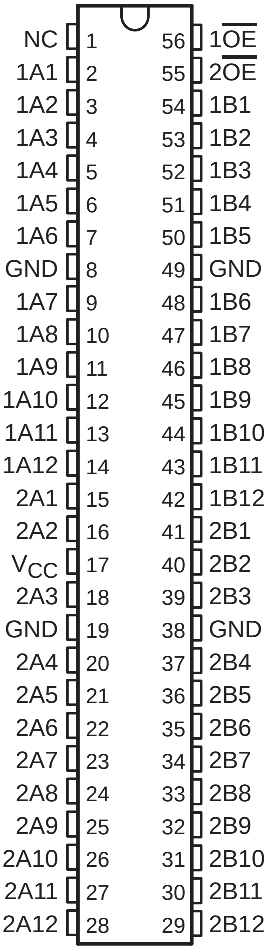
- **Member of Texas Instruments' Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**

description

The SN74CBTS16211 provides 24 bits of high-speed TTL-compatible bus switching with Schottky diodes on the I/Os to clamp undershoot. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device can operate as a dual 12-bit bus switch or as a single 24-bit bus switch. When $1\overline{OE}$ is low, 1A is connected to 1B. When $2\overline{OE}$ is low, 2A is connected to 2B.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1
1A1 2
1A2 3
1A3 4
1A4 5
1A5 6
1A6 7
GND 8
1A7 9
1A8 10
1A9 11
1A10 12
1A11 13
1A12 14
2A1 15
2A2 16
V_{CC} 17
2A3 18
GND 19
2A4 20
2A5 21
2A6 22
2A7 23
2A8 24
2A9 25
2A10 26
2A11 27
2A12 28
56 $1\overline{OE}$
55 $2\overline{OE}$
54 1B1
53 1B2
52 1B3
51 1B4
50 1B5
49 GND
48 1B6
47 1B7
46 1B8
45 1B9
44 1B10
43 1B11
42 1B12
41 2B1
40 2B2
39 2B3
38 GND
37 2B4
36 2B5
35 2B6
34 2B7
33 2B8
32 2B9
31 2B10
30 2B11
29 2B12

NC − No internal connection

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBTS16211DL	CBTS16211
		Tape and reel	SN74CBTS16211DLR	
	TSSOP − DGG	Tape and reel	SN74CBTS16211DGGR	CBTS16211
	TVSOP − DGV	Tape and reel	SN74CBTS16211DGVR	CYS211

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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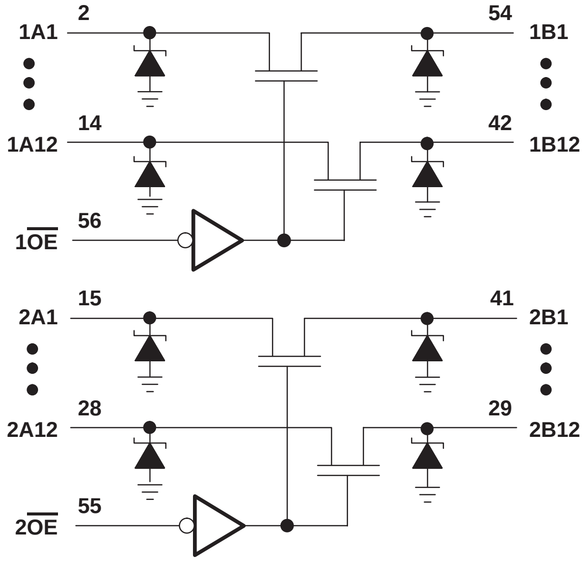
FUNCTION TABLE
(each 12-bit bus switch)

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	64°C/W
DGV package	48°C/W
DL package	56°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I	I_{IL}	V_{CC} = 5.5 V,	V_I = GND				−1	µA
	I_{IH}	V_{CC} = 5.5 V,	V_I = 5.5 V				150	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5.5		pF
r_{on}§		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		8	12	

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

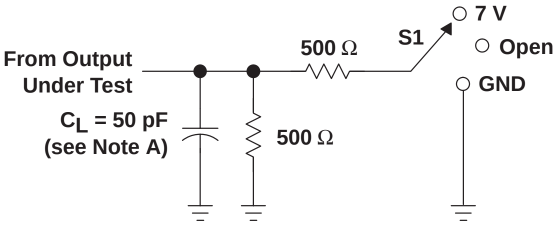
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		9.3	3.3	8.6	ns
t_{dis}	$\overline{OE}$	A or B		7.1	2.8	7.9	ns

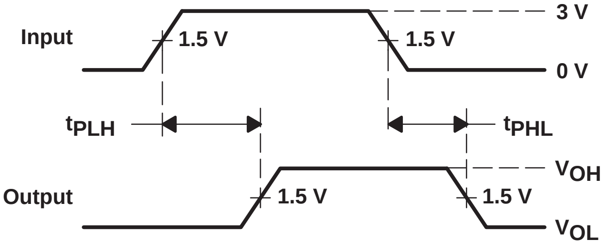
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

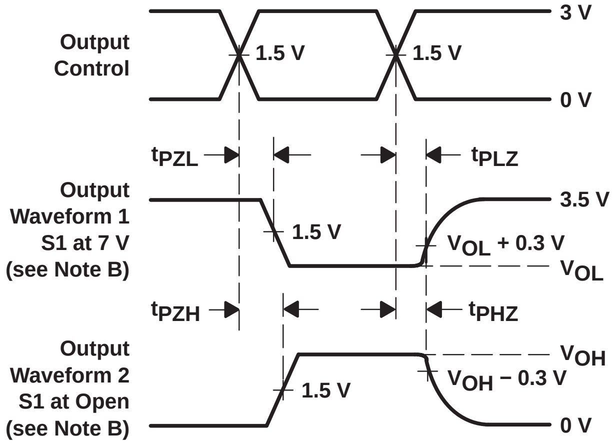

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments Widebus+™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Flow-Through Architecture Optimizes PCB Layout**

description/ordering information

The SN74CBT32245 provides 32 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as four 8-bit bus switches, two 16-bit bus switches, or one 32-bit bus switch. When output enable ($\overline{OE}$) is low, the switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch is open and the high-impedance state exists between the two ports.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	LFBGA − GKE	Tape and reel	SN74CBT32245GKER	BV245
	LFBGA − ZKE (Pb-free)		SN74CBT32245ZKER	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 8-bit bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

Widebus+ is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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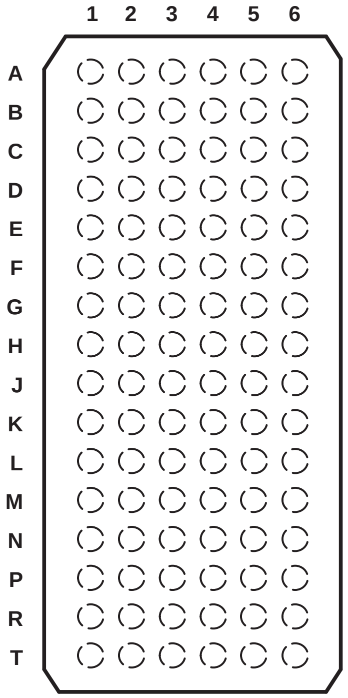
GKE OR ZKE PACKAGE
(TOP VIEW)

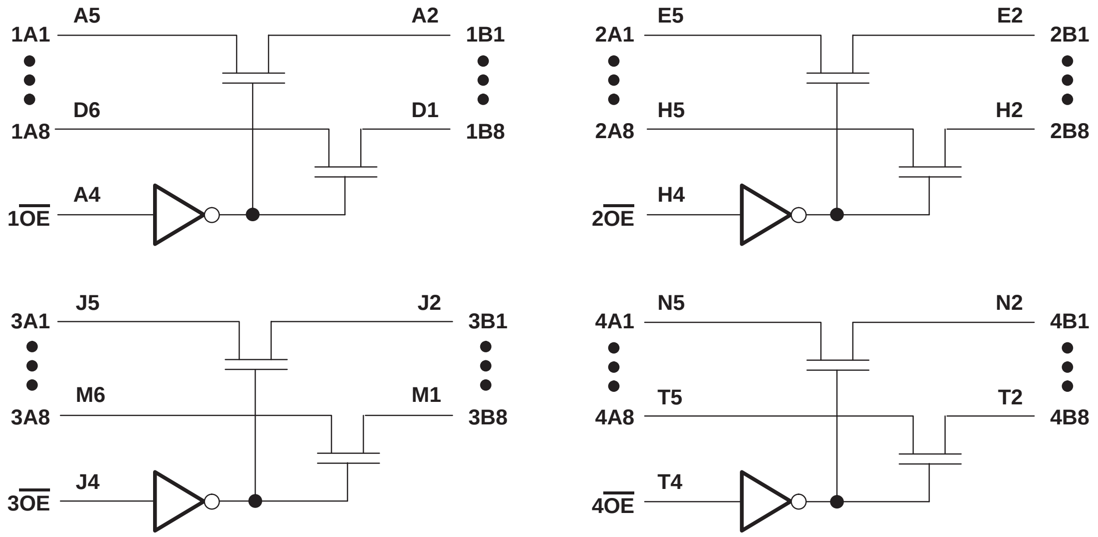

1
2
3
4
5
6
A
B
C
D
E
F
G
H
J
K
L
M
N
P
R
T

terminal assignments

	1	2	3	4	5	6
A	1B2	1B1	NC	1$\overline{\text{OE}}$	1A1	1A2
B	1B4	1B3	GND	GND	1A3	1A4
C	1B6	1B5	V_{CC}	V_{CC}	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
E	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	V_{CC}	V_{CC}	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
H	2B7	2B8	NC	2$\overline{\text{OE}}$	2A8	2A7
J	3B2	3B1	NC	3$\overline{\text{OE}}$	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	V_{CC}	V_{CC}	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
P	4B4	4B3	V_{CC}	V_{CC}	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
T	4B7	4B8	NC	4$\overline{\text{OE}}$	4A8	4A7

NC − No internal connection

logic diagram (positive logic)


1A1
A5
A2
1B1
1A8
D6
D1
1B8
1$\overline{\text{OE}}$
A4
2A1
E5
E2
2B1
2A8
H5
H2
2B8
2$\overline{\text{OE}}$
H4
3A1
J5
J2
3B1
3A8
M6
M1
3B8
3$\overline{\text{OE}}$
J4
4A1
N5
N2
4B1
4A8
T5
T2
4B8
4$\overline{\text{OE}}$
T4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): GKE/ZKE package	40°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			6	μA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			4.5		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		8	12	

‡ All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL-voltage level, rather than V_{CC} or GND.

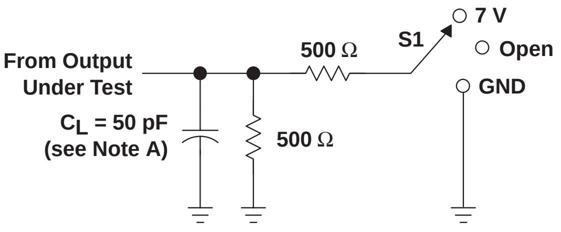
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}†	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		6.1	1.2	5.6	ns
t_{dis}	$\overline{OE}$	A or B		7.5	3.9	7.7	ns

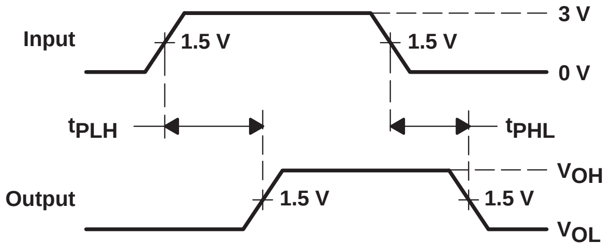
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

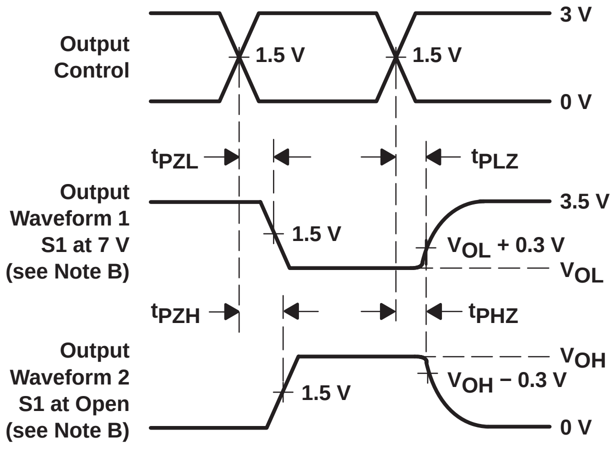

From Output Under Test
C_L = 50 pF (see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

SN74CBTK32245
32-BIT FET BUS SWITCH
WITH ACTIVE-CLAMP UNDERSHOOT-PROTECTION CIRCUIT

SCDS106E − APRIL 2000 − REVISED SEPTEMBER 2003

- **Member of the Texas Instruments Widebus+™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Active-Clamp Undershoot-Protection Circuit on the I/Os Clamps Undershoots Up To −2 V**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

description/ordering information

The SN74CBTK32245 provides 32 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The A and B ports have an active-clamp undershoot-protection circuit. When there is an undershoot, the active-clamp circuit is enabled and current from V_{CC} is supplied to clamp the output, preventing the pass transistor from turning on.

The device is organized as four 8-bit bus switches, two 16-bit bus switches, or one 32-bit bus switch. When the output-enable ($\overline{OE}$) input is low, the switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch is open and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	LFBGA − GKE	Tape and reel	SN74CBTK32245GKER	KT245
	LFBGA − ZKE (Pb-free)		SN74CBTK32245ZKER	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 8-bit bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

Widebus+ is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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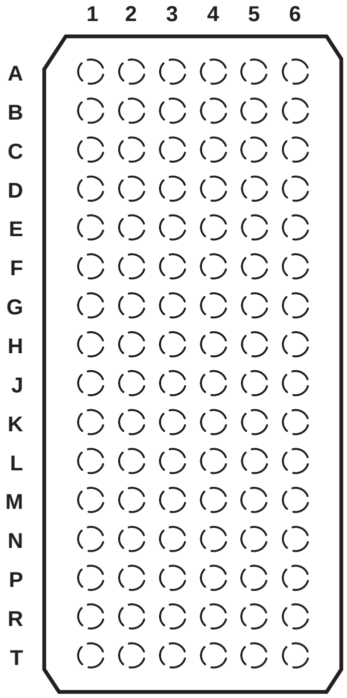
GKE OR ZKE PACKAGE
(TOP VIEW)

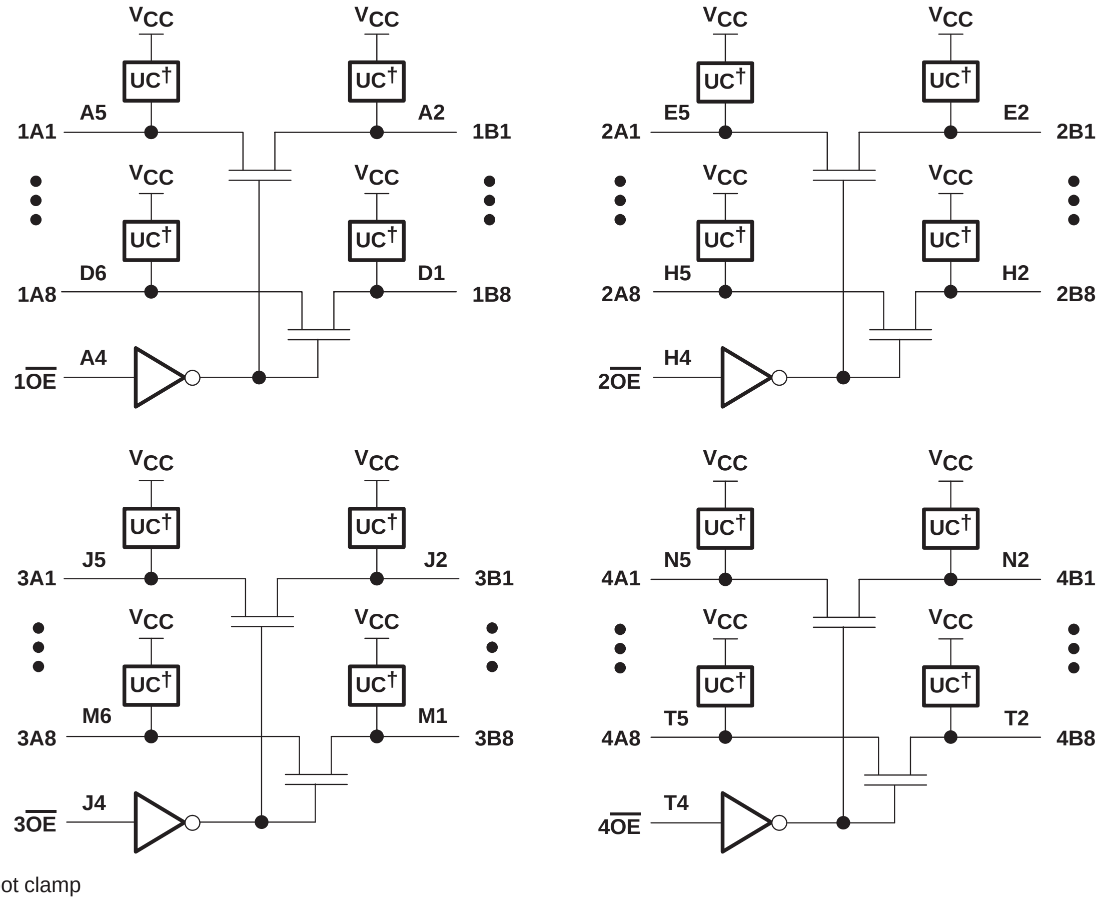


terminal assignments

	1	2	3	4	5	6
A	1B2	1B1	NC	1$\overline{\text{OE}}$	1A1	1A2
B	1B4	1B3	GND	GND	1A3	1A4
C	1B6	1B5	V_{CC}	V_{CC}	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
E	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	V_{CC}	V_{CC}	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
H	2B7	2B8	NC	2$\overline{\text{OE}}$	2A8	2A7
J	3B2	3B1	NC	3$\overline{\text{OE}}$	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	V_{CC}	V_{CC}	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
P	4B4	4B3	V_{CC}	V_{CC}	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
T	4B7	4B8	NC	4$\overline{\text{OE}}$	4A8	4A7

NC − No internal connection

logic diagram (positive logic)



† Undershoot clamp

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): GKE/ZKE package	40°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{IKU}		V_{CC} = 5.5 V,	0 mA ≥ I_I ≥ −50 mA,	$\overline{OE}$ = 5.5 V			−2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 5.5 V				20	µA
I_{CC}		V_{CC} = 5.5 V,	V_I = V_{CC} or GND,	I_O = 0			6	µA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5.5		pF
r_{on}[§]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		8	12	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL-voltage level, rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		7.4	1.6	4.9	ns
t_{dis}	$\overline{OE}$	A or B		7.4	4.2	7.5	ns

[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	See Figures 1 and 2, and Table 1	2	V_{OH}−0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

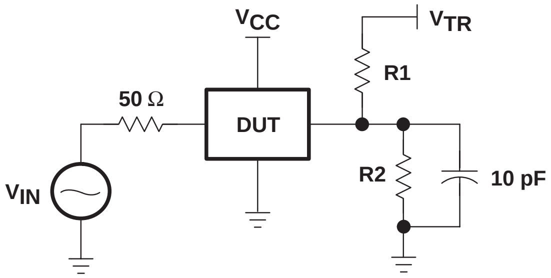


Figure 1. Device Test Setup

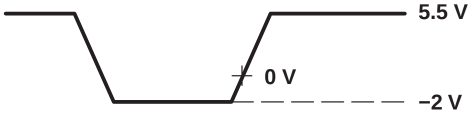


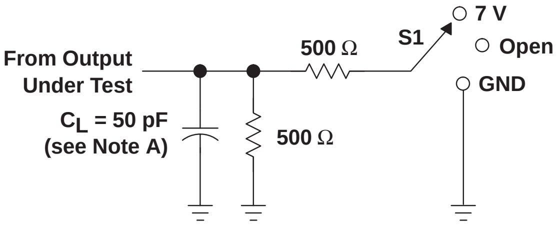
Figure 2. Transient Input Voltage Waveform

Table 1. Device Test Conditions

PARAMETER	VALUE	UNIT
B port under test‡	See Figure 1	
V_{IN}	See Figure 2	V
t_w	20	ns
t_r	2	ns
t_f	2	ns
R1 = R2	100	kΩ
V_{TR}	11	V
V_{CC}	5.5	V

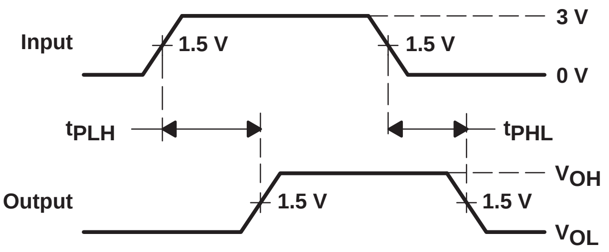
‡ Other B-port outputs are open

PARAMETER MEASUREMENT INFORMATION

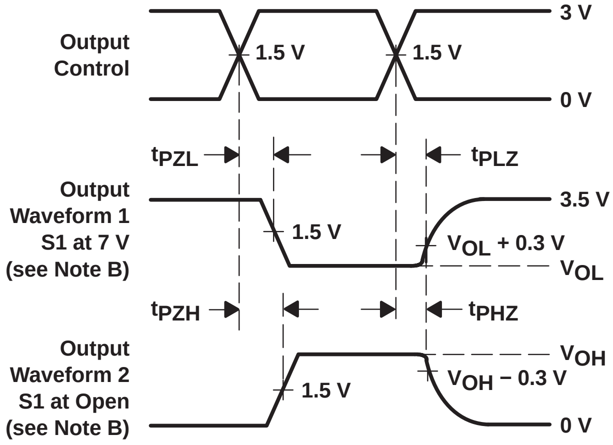

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

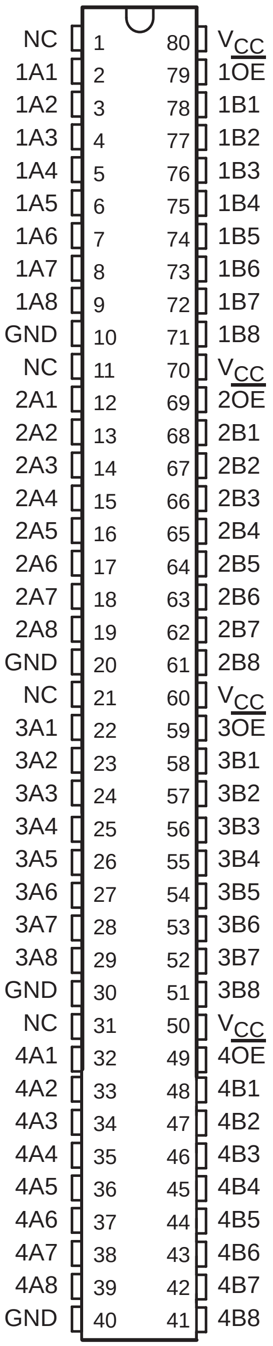
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

- **Member of Texas Instruments' Widebus+™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Flow-Through Architecture Optimizes PCB Layout**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DBB PACKAGE
(TOP VIEW)


NC 1
1A1 2
1A2 3
1A3 4
1A4 5
1A5 6
1A6 7
1A7 8
1A8 9
GND 10
NC 11
2A1 12
2A2 13
2A3 14
2A4 15
2A5 16
2A6 17
2A7 18
2A8 19
GND 20
NC 21
3A1 22
3A2 23
3A3 24
3A4 25
3A5 26
3A6 27
3A7 28
3A8 29
GND 30
NC 31
4A1 32
4A2 33
4A3 34
4A4 35
4A5 36
4A6 37
4A7 38
4A8 39
GND 40
80 V_{CC}
79 1$\overline{\text{OE}}$
78 1B1
77 1B2
76 1B3
75 1B4
74 1B5
73 1B6
72 1B7
71 1B8
70 V_{CC}
69 2$\overline{\text{OE}}$
68 2B1
67 2B2
66 2B3
65 2B4
64 2B5
63 2B6
62 2B7
61 2B8
60 V_{CC}
59 3$\overline{\text{OE}}$
58 3B1
57 3B2
56 3B3
55 3B4
54 3B5
53 3B6
52 3B7
51 3B8
50 V_{CC}
49 4$\overline{\text{OE}}$
48 4B1
47 4B2
46 4B3
45 4B4
44 4B5
43 4B6
42 4B7
41 4B8

NC − No internal connection

description

The SN74CBT34X245 provides 32 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as four 8-bit bus switches, two 16-bit bus switches, or one 32-bit bus switch. When output enable ($\overline{\text{OE}}$) is low, the switch is on, and port A is connected to port B. When $\overline{\text{OE}}$ is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Widebus+ is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION

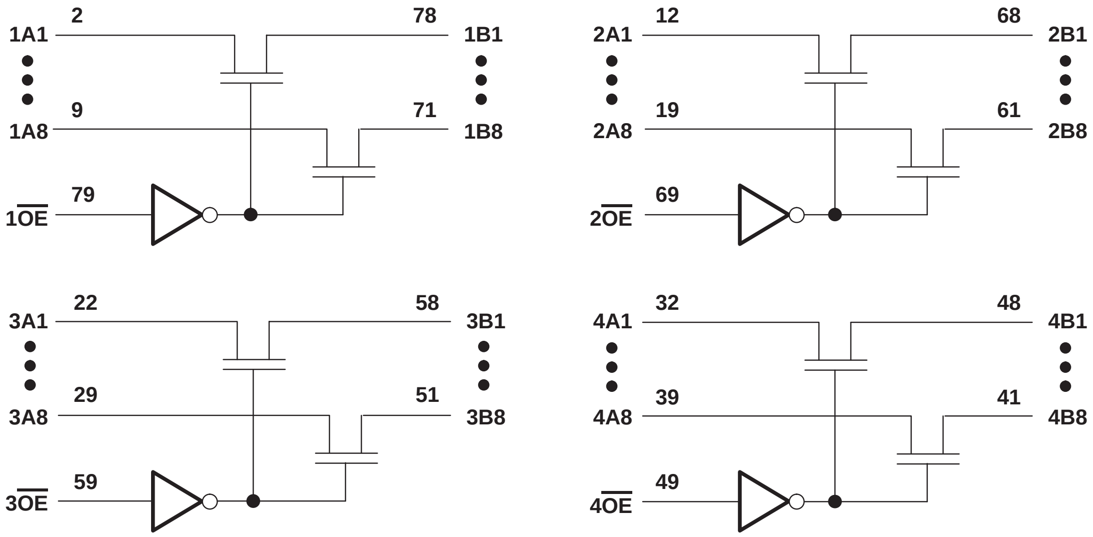
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TVSOP − DBB	Tape and reel	SN74CBT34X245DBBR	CBT34X245

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 8-bit bus switch)

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)


1A1
2
78
1B1
9
71
1A8
1B8
79
1$\overline{\text{OE}}$
2A1
12
68
2B1
19
61
2A8
2B8
69
2$\overline{\text{OE}}$
3A1
22
58
3B1
29
51
3A8
3B8
59
3$\overline{\text{OE}}$
4A1
32
48
4B1
39
41
4A8
4B8
49
4$\overline{\text{OE}}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2)	64°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 5.5 V				10	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			6	µA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5.5		pF
r_{on}[§]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		11	17	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		8	13	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

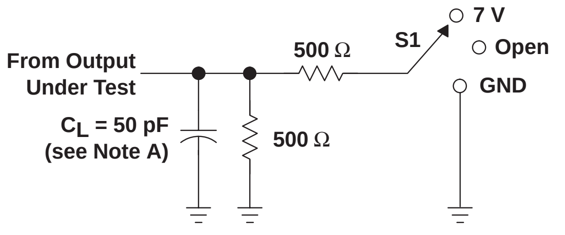
[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A				0.25	ns
t_{en}	$\overline{OE}$	A or B	2.2	6.5	1.9	6	ns
t_{dis}	$\overline{OE}$	A or B	1.9	6.2	2.2	6.7	ns

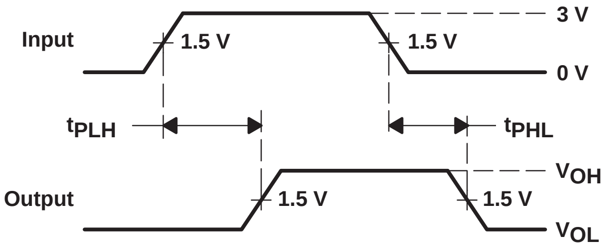
[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

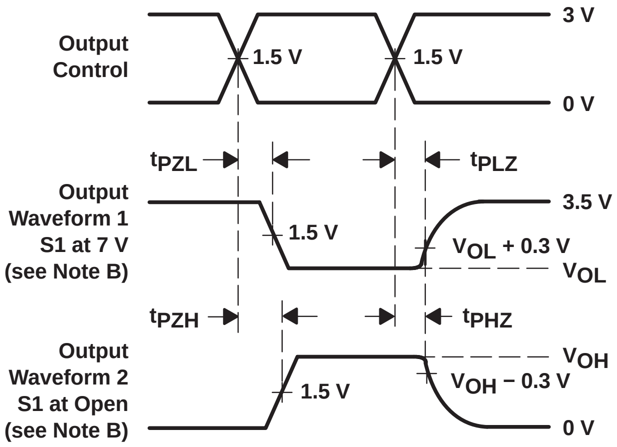

From Output Under Test
C_L = 50 pF (see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

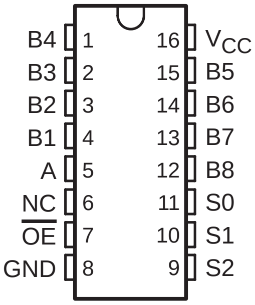
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

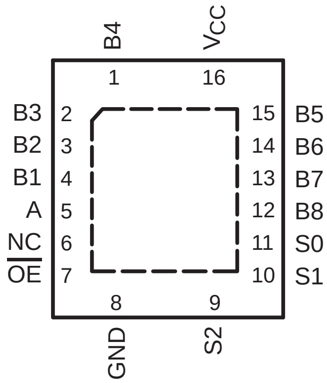
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

D, DB, DBQ, OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

RGY PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The SN74CBT3251 is a 1-of-8 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When output enable ($\overline{\text{OE}}$) is low, the SN74CBT3251 is enabled. S0, S1, and S2 select one of the B outputs for the A-input data.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBT3251RGYR	CU251
	SOIC − D	Tube	SN74CBT3251D	CBT3251
		Tape and reel	SN74CBT3251DR	
	SSOP − DB	Tape and reel	SN74CBT3251DBR	CU251
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3251DBQR	CU251
	TSSOP − PW	Tape and reel	SN74CBT3251PWR	CU251

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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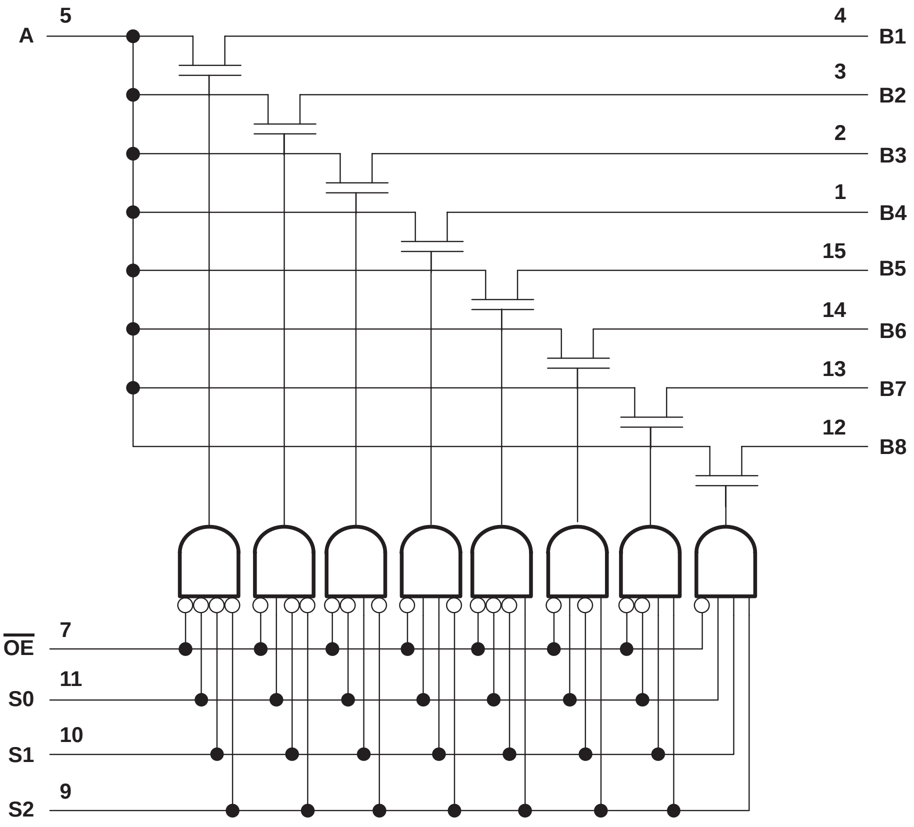
FUNCTION TABLE
(each multiplexer/demultiplexer)

INPUTS				FUNCTION
$\overline{OE}$	S2	S1	S0	
L	L	L	L	A port = B1 port
L	L	L	H	A port = B2 port
L	L	H	L	A port = B3 port
L	L	H	H	A port = B4 port
L	H	L	L	A port = B5 port
L	H	L	H	A port = B6 port
L	H	H	L	A port = B7 port
L	H	H	H	A port = B8 port
H	X	X	X	Disconnect

logic diagram (positive logic)


A
5
4
B1
3
B2
2
B3
1
B4
15
B5
14
B6
13
B7
12
B8
$\overline{OE}$
7
S0
11
S1
10
S2
9

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_K ($V_{I/O}$ < 0)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
(see Note 2): DB package	82°C/W
(see Note 2): DBQ package	90°C/W
(see Note 2): PW package	108°C/W
(see Note 3): RGY package	39°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[‡]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			17.5		pF
	B port					4		
r_{on}[¶]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

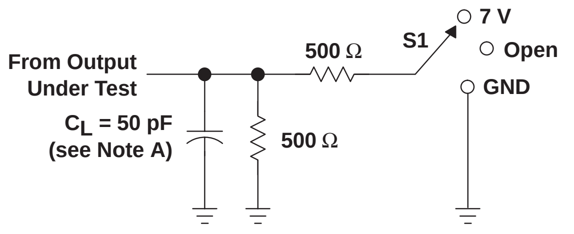
[¶] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.35		0.25	ns
t_{pd}	S	A		6	2	5.5	ns
t_{en}	S	B		6.4	1.5	5.6	ns
	$\overline{OE}$	A or B		6.4	1.6	5.8	
t_{dis}	S	B		6.8	1.9	6.4	ns
	$\overline{OE}$	A or B		6	2.3	6.2	

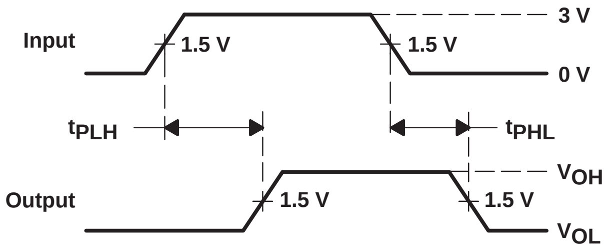
[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

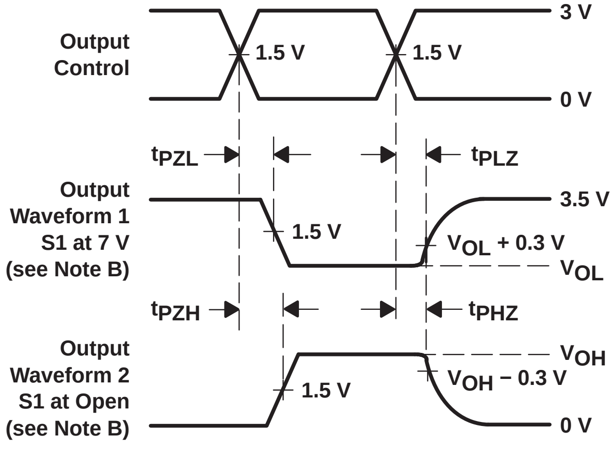

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

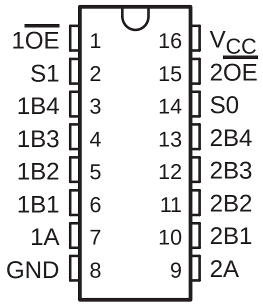
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

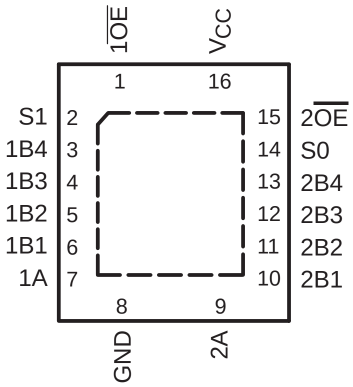
Figure 1. Load Circuit and Voltage Waveforms

- **TTL-Compatible Input Levels**

D, DB, DBQ, OR PW PACKAGE
(TOP VIEW)


1$\overline{OE}$ 1
S1 2
1B4 3
1B3 4
1B2 5
1B1 6
1A 7
GND 8
16 V_{CC}
15 2$\overline{OE}$
14 S0
13 2B4
12 2B3
11 2B2
10 2B1
9 2A

RGY PACKAGE
(TOP VIEW)


1$\overline{OE}$
V_{CC}
1
16
S1 2
1B4 3
1B3 4
1B2 5
1B1 6
1A 7
15 2$\overline{OE}$
14 S0
13 2B4
12 2B3
11 2B2
10 2B1
8
9
GND
2A

description/ordering information

The SN74CBT3253 is a dual 1-of-4 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

1$\overline{OE}$, 2$\overline{OE}$, S0, and S1 select the appropriate B output for the A-input data.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBT3253RGYR	CU253
	SOIC − D	Tube	SN74CBT3253D	CBT3253
		Tape and reel	SN74CBT3253DR	
	SSOP − DB	Tape and reel	SN74CBT3253DBR	CU253
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3253DBQR	CU253
	TSSOP − PW	Tape and reel	SN74CBT3253PWR	CU253

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				FUNCTION
1$\overline{OE}$	2$\overline{OE}$	S1	S0	
X	H	X	X	Disconnect 1A and 2A
H	X	X	X	Disconnect 1A and 2A
L	L	L	L	1A to 1B1 and 2A to 2B1
L	L	L	H	1A to 1B2 and 2A to 2B2
L	L	H	L	1A to 1B3 and 2A to 2B3
L	L	H	H	1A to 1B4 and 2A to 2B4

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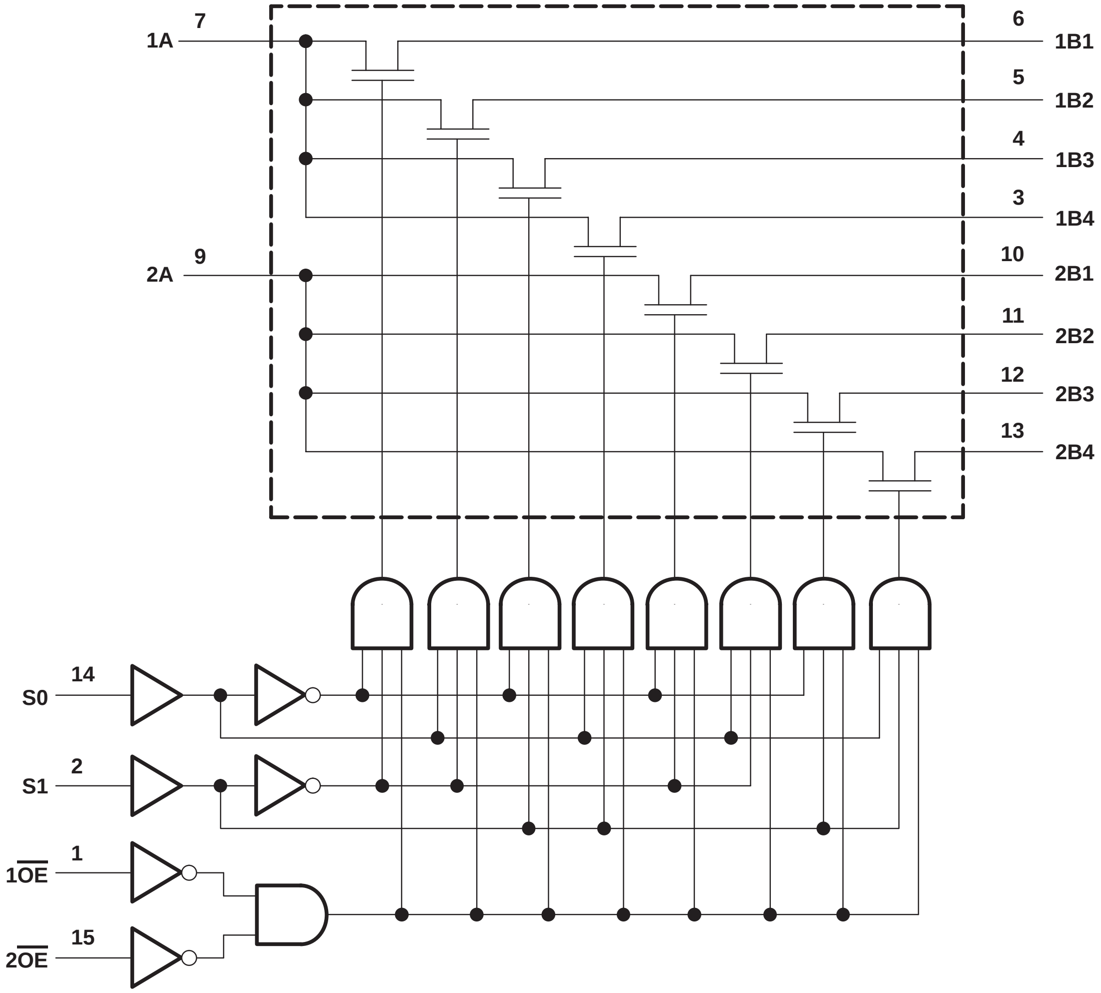
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_K ($V_{I/O} < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
(see Note 2): DB package	82°C/W
(see Note 2): DBQ package	90°C/W
(see Note 2): PW package	108°C/W
(see Note 3): RGY package	39°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5 V,	V_I = 5.5 V or GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			10		pF
	B port					4		
r_{on}§		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

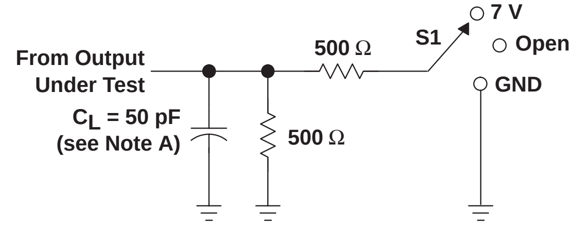
§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.35		0.25	ns
t_{pd}	S	A or B		6.6	1.6	6.2	ns
t_{en}	S	A or B		7.1	1.3	6.3	ns
	$\overline{OE}$			7.3	1.4	6.4	
t_{dis}	S	A or B		7.9	1.1	7.4	ns
	$\overline{OE}$			7.3	2.3	7	

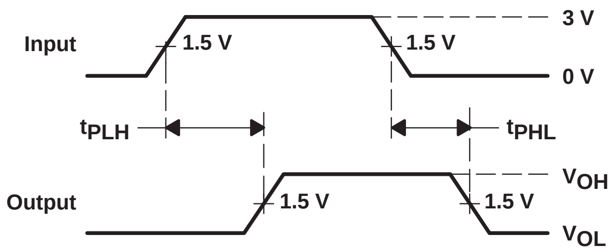
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

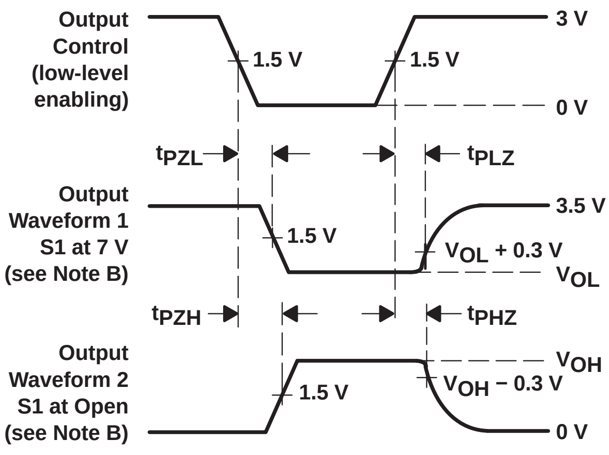

From Output Under Test
C_L = 50 pF (see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output Control (low-level enabling)
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PHL} and t_{PLH} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

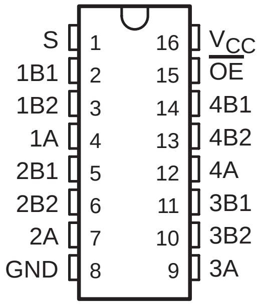
Figure 1. Load Circuit and Voltage Waveforms

SN74CBT3257
4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

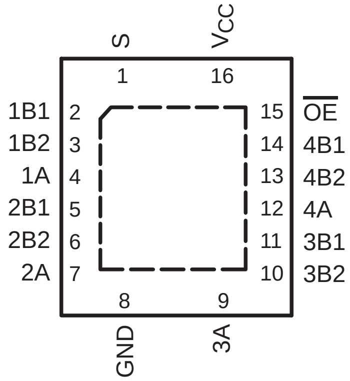
SCDS017L − MAY 1995 − REVISED SEPTEMBER 2002

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

D, DB, DBQ, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBT3257 is a 4-bit 1-of-2 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

Output-enable ($\overline{OE}$) and select-control (S) inputs select the appropriate B1 and B2 outputs for the A-input data.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBT3257RGYR	CU257
	SOIC − D	Tube	SN74CBT3257D	CBT3257
		Tape and reel	SN74CBT3257DR	
	SSOP − DB	Tape and reel	SN74CBT3257DBR	CU257
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3257DBQR	CU257
	TSSOP − PW	Tape and reel	SN74CBT3257PWR	CU257

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		FUNCTION
$\overline{OE}$	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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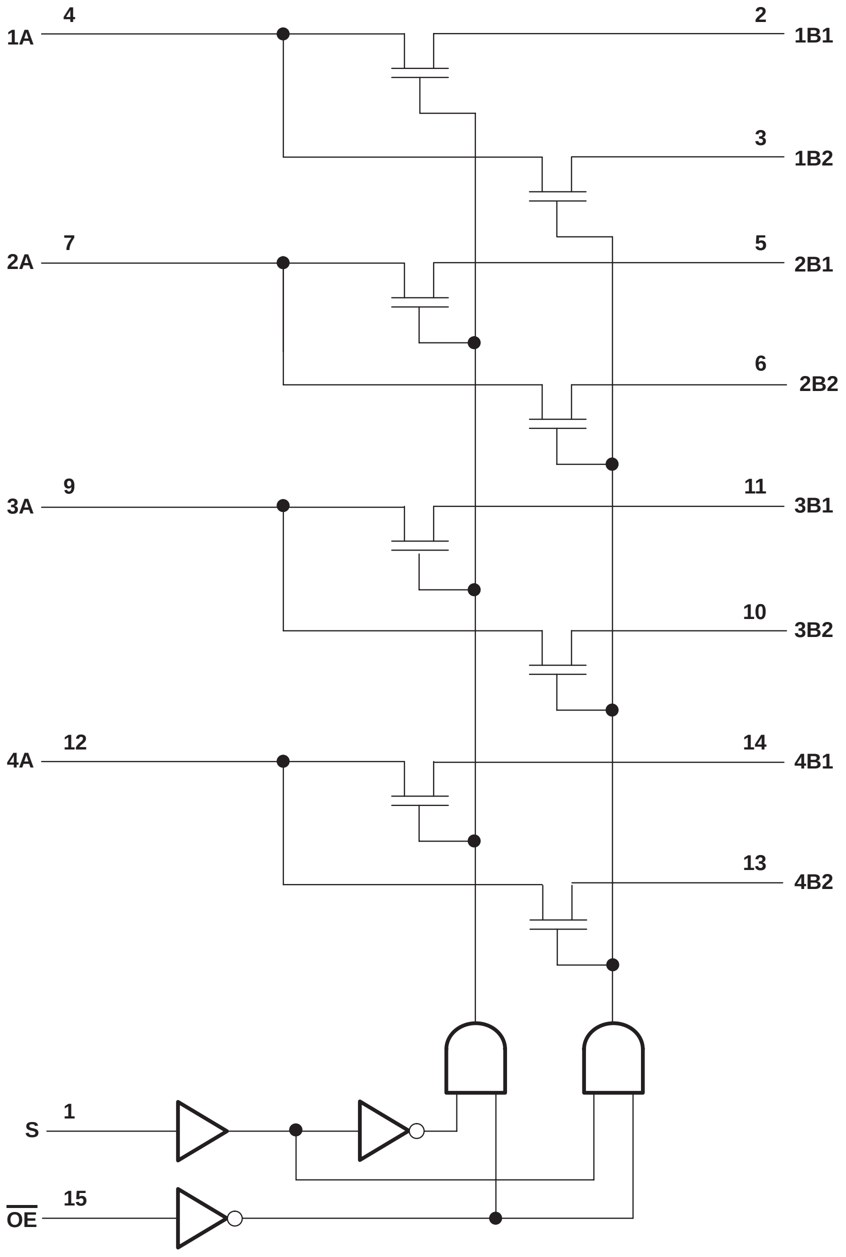
logic diagram (positive logic)


1A
4
2
1B1
3
1B2
2A
7
5
2B1
6
2B2
3A
9
11
3B1
10
3B2
4A
12
14
4B1
13
4B2
S
1
$\overline{\text{OE}}$
15

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_K ($V_{I/O} < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
(see Note 2): DB package	82°C/W
(see Note 2): DBQ package	90°C/W
(see Note 2): PW package	108°C/W
(see Note 3): RGY package	39°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6.5		pF
	B port					4		
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

‡ All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

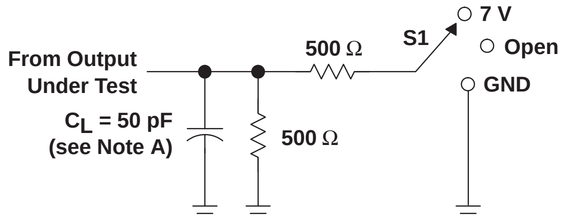
¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.35		0.25	ns
t_{pd}	S	A		5.5	1.6	5	ns
t_{en}	S	B		5.7	1.6	5.2	ns
	$\overline{OE}$	A or B		5.6	1.8	5.1	
t_{dis}	S	B		5.2	1	5	ns
	$\overline{OE}$	A or B		5.5	2.2	5.5	

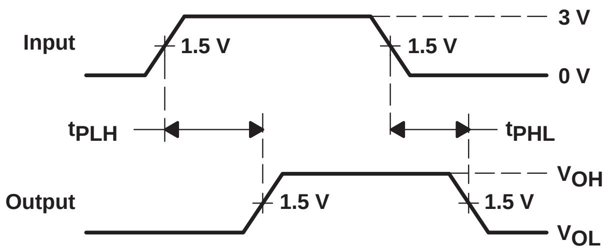
[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

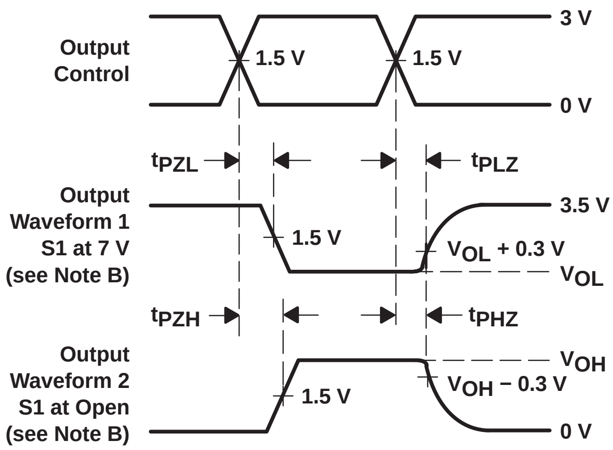

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

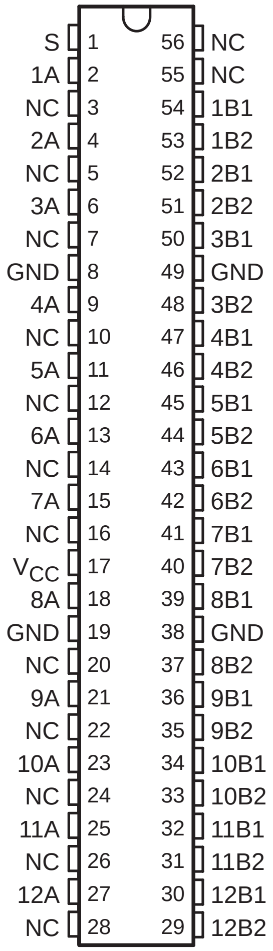
Figure 1. Load Circuit and Voltage Waveforms

SN74CBT16292
12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS053E − MARCH 1998 − REVISED OCTOBER 2000

- **Member of Texas Instruments’ Widebus™ Family**
- **4-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**
- **Make-Before-Break Feature**
- **Internal 500-Ω Pulldown Resistors to Ground**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


S 1 56 NC
1A 2 55 NC
NC 3 54 1B1
2A 4 53 1B2
NC 5 52 2B1
3A 6 51 2B2
NC 7 50 3B1
GND 8 49 GND
4A 9 48 3B2
NC 10 47 4B1
5A 11 46 4B2
NC 12 45 5B1
6A 13 44 5B2
NC 14 43 6B1
7A 15 42 6B2
NC 16 41 7B1
V_{CC} 17 40 7B2
8A 18 39 8B1
GND 19 38 GND
NC 20 37 8B2
9A 21 36 9B1
NC 22 35 9B2
10A 23 34 10B1
NC 24 33 10B2
11A 25 32 11B1
NC 26 31 11B2
12A 27 30 12B1
NC 28 29 12B2

NC − No internal connection

description

The SN74CBT16292 is a 12-bit 1-of-2 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1, and R_{INT} is connected to port B2. When S is high, port A is connected to port B2, and R_{INT} is connected to port B1.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16292DL	CBT16292
		Tape and reel	SN74CBT16292DLR	
	TSSOP − DGG	Tape and reel	SN74CBT16292DGGR	CBT16292
	TVSOP − DGV	Tape and reel	SN74CBT16292DGVR	CY292

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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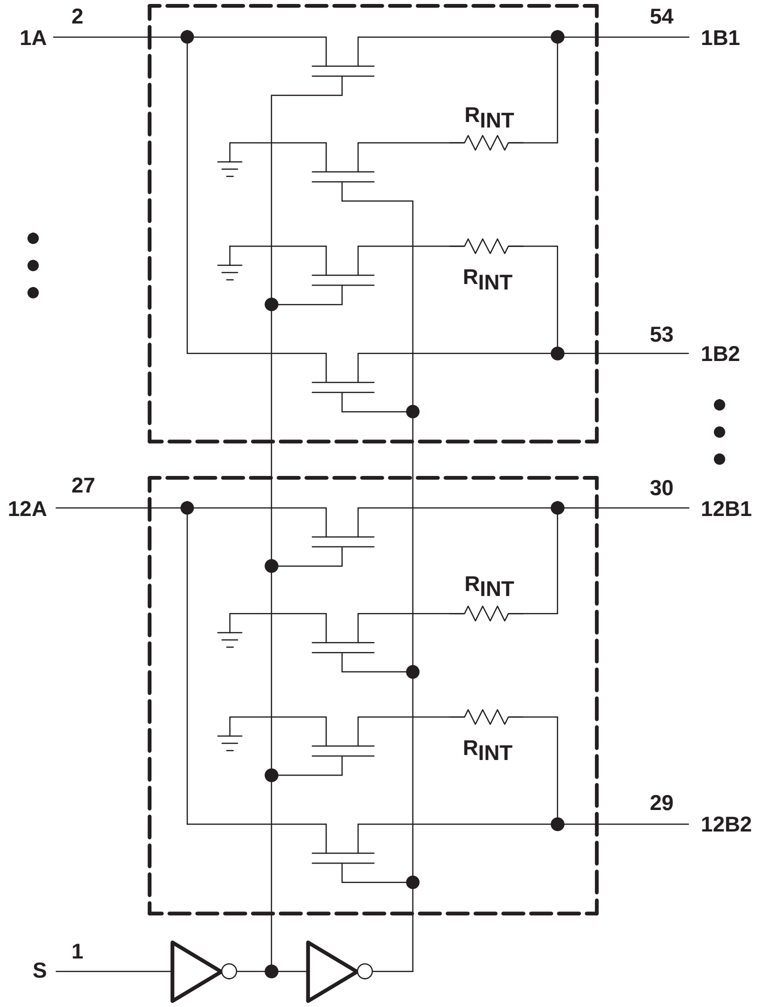
FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port R_{INT} = B2 port
H	A port = B2 port R_{INT} = B1 port

logic diagram (positive logic)


2
1A
54
1B1
RINT
RINT
53
1B2
27
12A
30
12B1
RINT
RINT
29
12B2
1
S

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[‡]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	$V_I = V_{CC}$ or GND				±5	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	$V_I = V_{CC}$ or GND			3	µA
ΔI_{CC}[§]	Control input	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control input	V_I = 3 V or 0				3		pF
C_{io}		V_{CC} = 0,	V_O = 3 V or 0			8		pF
r_{on}[¶]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		10	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		3	7	
				I_I = 30 mA		3	7	
			V_I = 2.4 V,	I_I = 15 mA		5	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.5		0.25	ns
t_{en}	S	A or B		6.8	1	6	ns
t_{dis}	S	A or B		7	1	6.3	ns

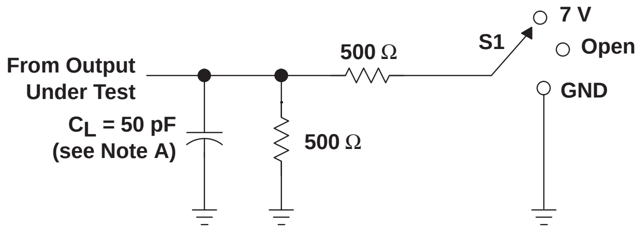
[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	DESCRIPTION	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
		MIN	MAX	MIN	MAX	
t_{mbb}[‡]	Make-before-break time	0	2	0	2	ns

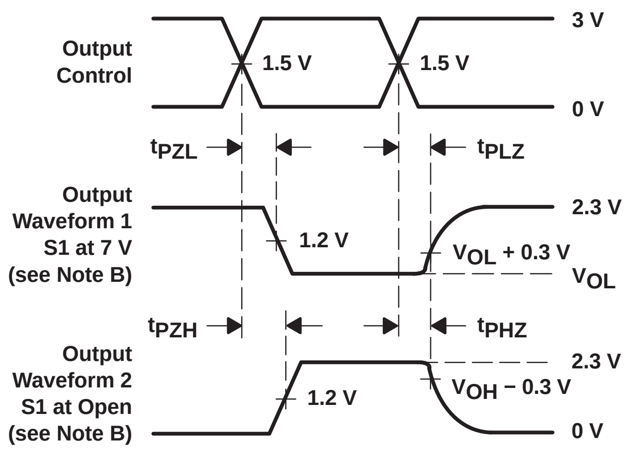
[‡] The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.

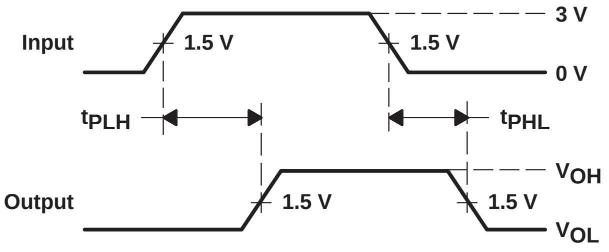
PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
CL = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PZL}/t_{PLZ}	7 V
t_{PZH}/t_{PHZ}	Open


Output
Control
1.5 V
1.5 V
3 V
0 V
tPZL
tPLZ
Output
Waveform 1
S1 at 7 V
(see Note B)
1.2 V
2.3 V
VOL + 0.3 V
VOL
tPZH
tPHZ
Output
Waveform 2
S1 at Open
(see Note B)
1.2 V
2.3 V
VOH − 0.3 V
0 V


Input
1.5 V
1.5 V
3 V
0 V
tPLH
tPHL
Output
1.5 V
1.5 V
VOH
VOL

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when connected to the internal 500-Ω pulldown resistor. Waveform 2 is for an output with internal conditions such that the output is high except when connected to the internal 500-Ω pulldown resistor.
- C. All pulse inputs and DC inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}. Z = R_{INT} = 500 Ω
- F. t_{PZL} and t_{PZH} are the same as t_{en}. Z = R_{INT} = 500 Ω
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

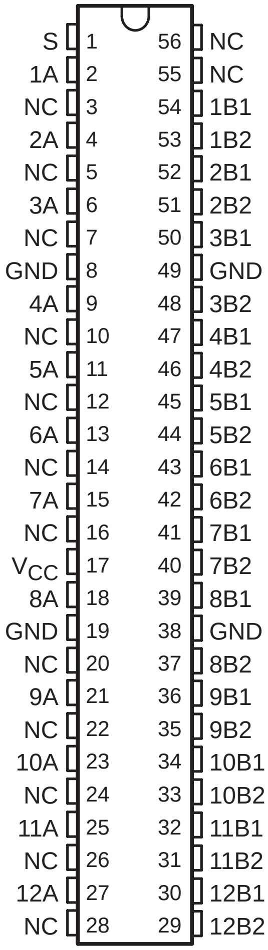
Figure 1. Load Circuit and Voltage Waveforms

SN74CBT162292
12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS052E − MARCH 1998 − REVISED OCTOBER 2000

- **Member of Texas Instruments' Widebus™ Family**
- **TTL-Compatible Control Input Levels**
- **Isolation Under Power-Off Conditions**
- **Make-Before-Break Feature**
- **Internal 500-Ω Pulldown Resistors to Ground**
- **A-Port Inputs/Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


S 1 56 NC
1A 2 55 NC
NC 3 54 1B1
2A 4 53 1B2
NC 5 52 2B1
3A 6 51 2B2
NC 7 50 3B1
GND 8 49 GND
4A 9 48 3B2
NC 10 47 4B1
5A 11 46 4B2
NC 12 45 5B1
6A 13 44 5B2
NC 14 43 6B1
7A 15 42 6B2
NC 16 41 7B1
VCC 17 40 7B2
8A 18 39 8B1
GND 19 38 GND
NC 20 37 8B2
9A 21 36 9B1
NC 22 35 9B2
10A 23 34 10B1
NC 24 33 10B2
11A 25 32 11B1
NC 26 31 11B2
12A 27 30 12B1
NC 28 29 12B2

NC − No internal connection

description

The SN74CBT162292 is a 12-bit 1-of-2 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1, and R_{INT} is connected to port B2. When S is high, port A is connected to port B2, and R_{INT} is connected to port B1.

The A-port inputs/outputs include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT162292DL	CBT162292
		Tape and reel	SN74CBT162292DLR	
	TSSOP − DGG	Tape and reel	SN74CBT162292DGGR	CBT162292
	TVSOP − DGV	Tape and reel	SN74CBT162292DGVR	CY2292

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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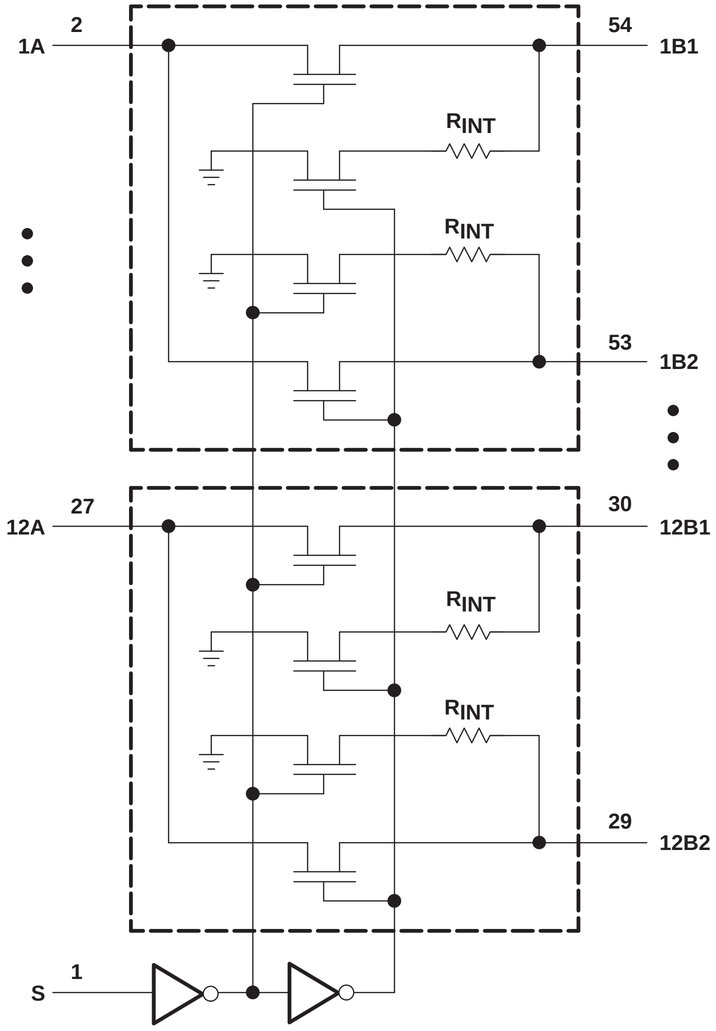
FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port R_{INT} = B2 port
H	A port = B2 port R_{INT} = B1 port

logic diagram (positive logic)


2
1A
54
1B1
RINT
RINT
53
1B2
27
12A
30
12B1
RINT
RINT
29
12B2
1
S

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±5	μA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 7 V				10	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}§	Control input	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control input	V_I = 3 V or 0				3.5		pF
C_{io}		V_{CC} = 0,	V_O = 3 V or 0			8		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		38	55	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 45 mA		39	63	
				I_I = 30 mA		37	55	
			V_I = 2.4 V,	I_I = 15 mA		37	55	

‡ All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF, (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		1.9		1.85	ns
t_{en}	S	A or B	1	10.7	1	9.5	ns
t_{dis}	S	A or B	1	10.9	1	9.7	ns

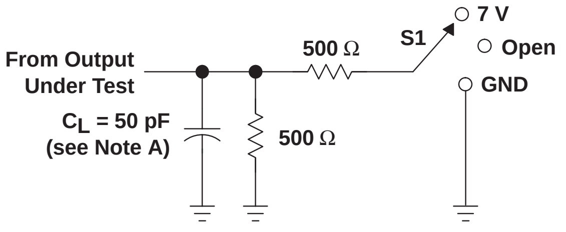
[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF, (unless otherwise noted) (see Figure 1)

PARAMETER	DESCRIPTION	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
		MIN	MAX	MIN	MAX	
t_{mbb}[‡]	Make-before-break time	0	2	0	2	ns

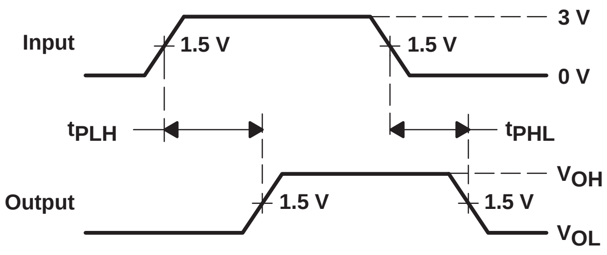
[‡] The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.

PARAMETER MEASUREMENT INFORMATION

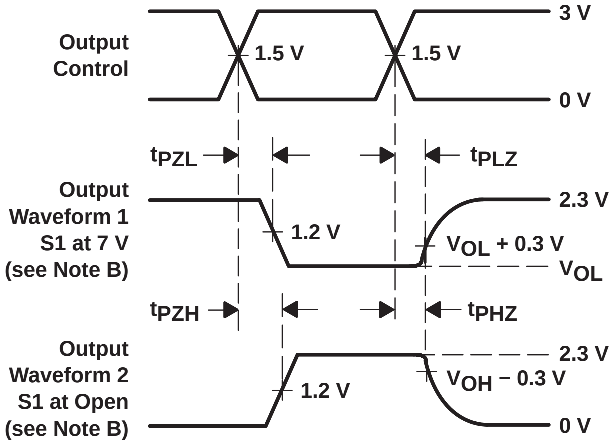

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PZL}/t_{PLZ}	7 V
t_{PZH}/t_{PHZ}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.2 V
2.3 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.2 V
2.3 V
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when connected to the internal 500-Ω pulldown resistor. Waveform 2 is for an output with internal conditions such that the output is high except when connected to the internal 500-Ω pulldown resistor.
- C. All pulse inputs and DC inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}. Z = R_{INT} = 500 Ω.
- F. t_{PZL} and t_{PZH} are the same as t_{en}. Z = R_{INT} = 500 Ω.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SN74CBT16214
12-BIT 1-OF-3 FET MULTIPLEXER/DEMULTIPLEXER

SCDS008L − MAY 1993 − REVISED NOVEMBER 2001

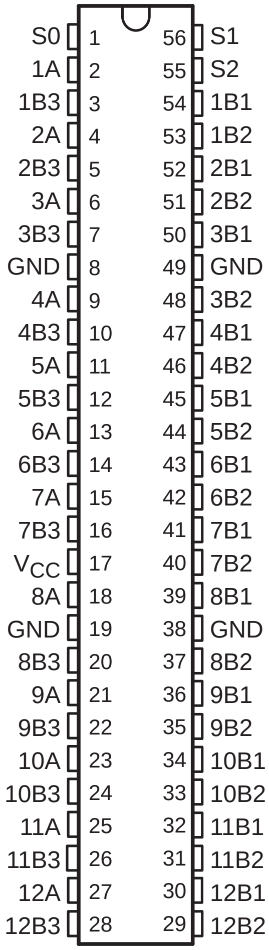
- **Member of the Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

description

The SN74CBT16214 provides 12 bits of high-speed TTL-compatible bus switching between three separate ports. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 12-bit bus-select switch via the data-select (S0−S2) terminals.

DGG OR DL PACKAGE
(TOP VIEW)


S0 1 56 S1
1A 2 55 S2
1B3 3 54 1B1
2A 4 53 1B2
2B3 5 52 2B1
3A 6 51 2B2
3B3 7 50 3B1
GND 8 49 GND
4A 9 48 3B2
4B3 10 47 4B1
5A 11 46 4B2
5B3 12 45 5B1
6A 13 44 5B2
6B3 14 43 6B1
7A 15 42 6B2
7B3 16 41 7B1
VCC 17 40 7B2
8A 18 39 8B1
GND 19 38 GND
8B3 20 37 8B2
9A 21 36 9B1
9B3 22 35 9B2
10A 23 34 10B1
10B3 24 33 10B2
11A 25 32 11B1
11B3 26 31 11B2
12A 27 30 12B1
12B3 28 29 12B2

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16214DL	CBT16214
		Tape and reel	SN74CBT16214DLR	
	TSSOP − DGG	Tape and reel	SN74CBT16214DGGR	CBT16214

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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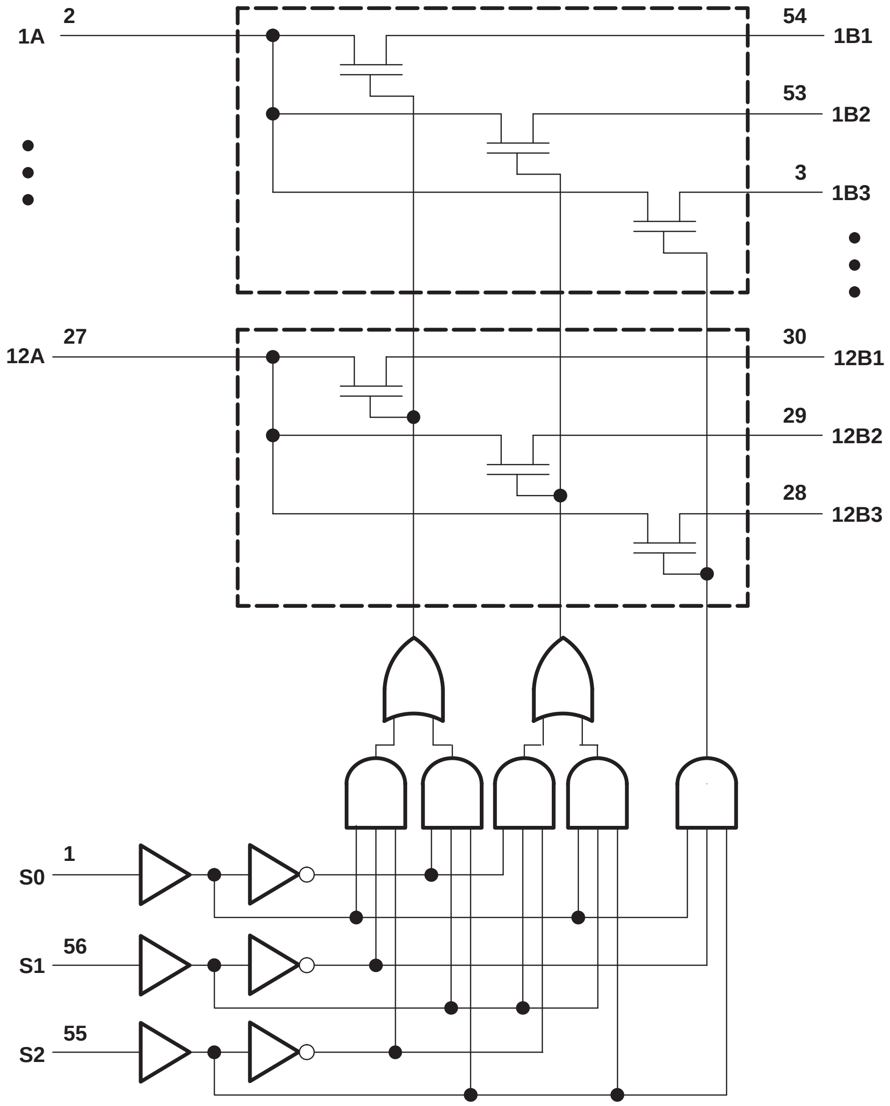
FUNCTION TABLE

INPUTS			INPUT/OUTPUT A	FUNCTION
S2	S1	S0		
L	L	L	Z	Disconnect
L	L	H	B1	A port = B1 port
L	H	L	B2	A port = B2 port
L	H	H	Z	Disconnect
H	L	L	Z	Disconnect
H	L	H	B3	A port = B3 port
H	H	L	B1	A port = B1 port
H	H	H	B2	A port = B2 port

logic diagram (positive logic)


2
1A
54
1B1
53
1B2
3
1B3
27
12A
30
12B1
29
12B2
28
12B3
1
S0
56
S1
55
S2

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	64°C
DL package	56°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				4		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	S_0, S_1, and S_2 = GND			7.5		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		4	7	
				I_I = 30 mA		4	7	
			V_I = 2.4 V,	I_I = 15 mA		6	12	

‡ All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

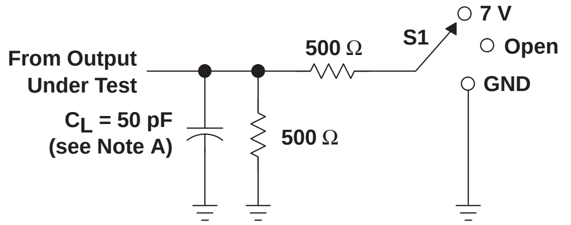
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd} †	A or B	B or A		0.35		0.25	ns
t_{pd}	S	B or A		15.3	5.5	13.9	ns
t_{en}	S	A or B		16	5.1	14.5	ns
t_{dis}	S	A or B		12.1	3.6	11.7	ns

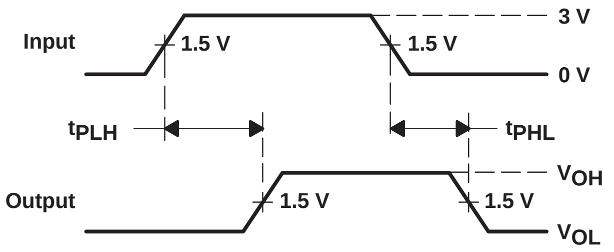
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

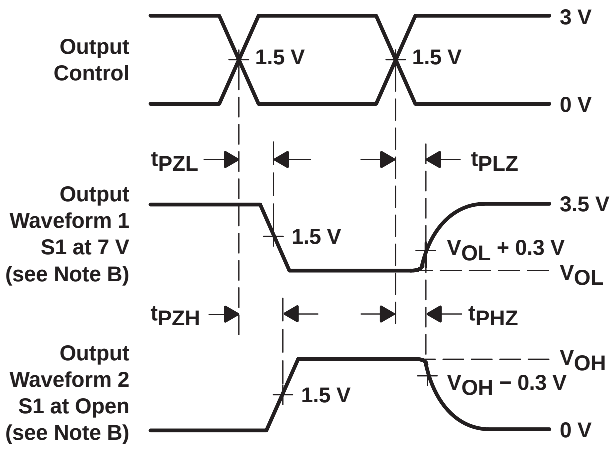

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SN74CBT16232
SYNCHRONOUS 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS009M − MAY 1995 − REVISED NOVEMBER 2001

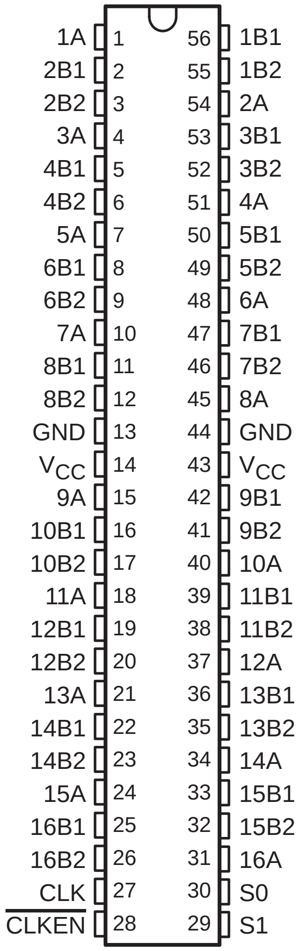
- **Member of the Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**

description

The SN74CBT16232 is a synchronous 16-bit 1-of-2 FET multiplexer/demultiplexer used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path.

Two select (S0 and S1) inputs control the data flow. A clock (CLK) and a clock enable ($\overline{\text{CLKEN}}$) synchronize the device operation. When $\overline{\text{CLKEN}}$ is high, the bus switch remains in the last clocked function.

DGG OR DL PACKAGE
(TOP VIEW)


1A 1 56 1B1
2B1 2 55 1B2
2B2 3 54 2A
3A 4 53 3B1
4B1 5 52 3B2
4B2 6 51 4A
5A 7 50 5B1
6B1 8 49 5B2
6B2 9 48 6A
7A 10 47 7B1
8B1 11 46 7B2
8B2 12 45 8A
GND 13 44 GND
V_{CC} 14 43 V_{CC}
9A 15 42 9B1
10B1 16 41 9B2
10B2 17 40 10A
11A 18 39 11B1
12B1 19 38 11B2
12B2 20 37 12A
13A 21 36 13B1
14B1 22 35 13B2
14B2 23 34 14A
15A 24 33 15B1
16B1 25 32 15B2
16B2 26 31 16A
CLK 27 30 S0
$\overline{\text{CLKEN}}$ 28 29 S1

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16232DL	CBT16232
		Tape and reel	SN74CBT16232DLR	
	TSSOP − DGG	Tape and reel	SN74CBT16232DGGR	CBT16232

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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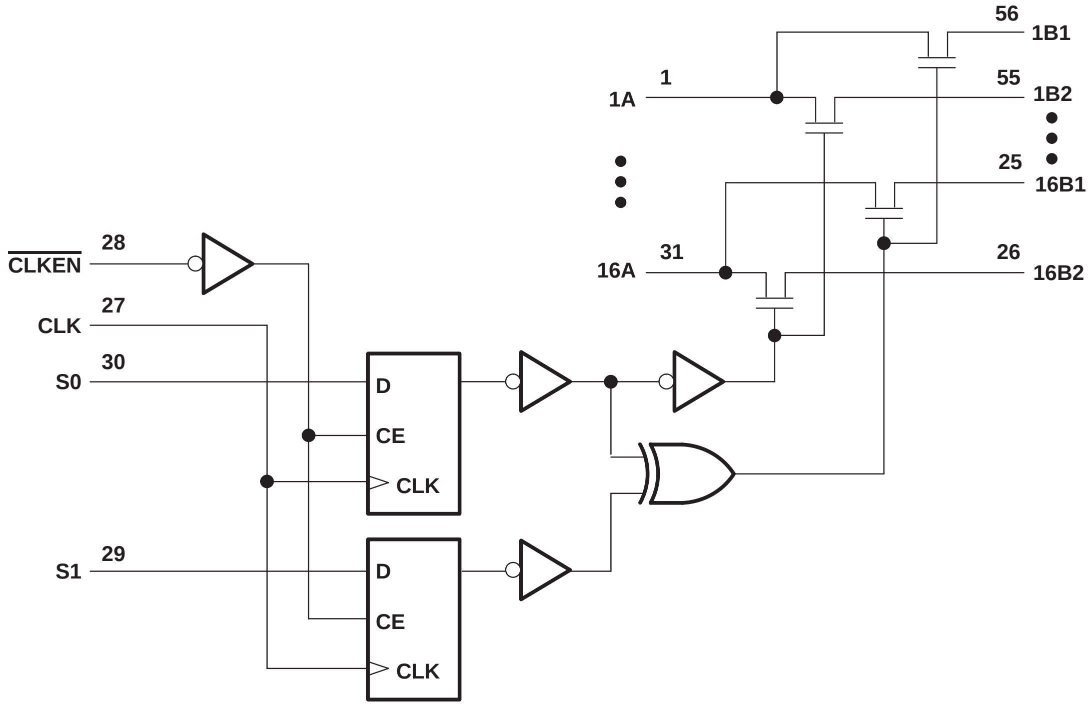
FUNCTION TABLE

INPUTS				FUNCTION
S1	S0	CLK	$\overline{\text{CLKEN}}$	
X	X	X	H	Last state
L	L	↑	L	Disconnect
L	H	↑	L	A = B1 and A = B2
H	L	↑	L	A = B1
H	H	↑	L	A = B2

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	64°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				4.5		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0,	$\overline{\text{CLKEN}}$ = 0,	S0 and S1 = GND		6.5		pF
	B port					4		
r_{on}§		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

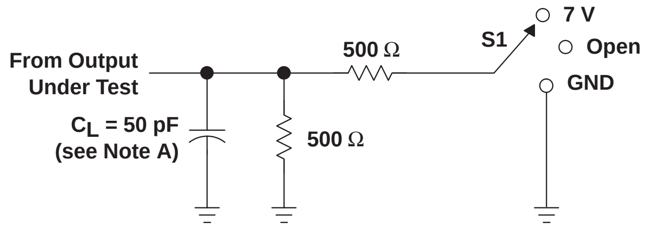
PARAMETER			V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150	MHz
t_w	Pulse duration	CLK high or low	3.3		3.3		ns
t_{su}	Setup time	S0, S1 before CLK↑	2.2		1.9		ns
		$\overline{\text{CLKEN}}$ before CLK↑	2.4		1.9		
t_h	Hold time	S0, S1 after CLK↑	0.5		1		ns
		$\overline{\text{CLKEN}}$ after CLK↑	1.9		1.8		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V MIN	V_{CC} = 4 V MAX	V_{CC} = 5 V ± 0.5 V MIN	V_{CC} = 5 V ± 0.5 V MAX	UNIT
f_{max}			150		150		MHz
t_{pd}[†]	A or B	B or A		0.35		0.25	ns
t_{pd}	CLK	A or B		6.1	2	5.8	ns
t_{en}	CLK	A, B1, B2		6.8	1.8	6.2	ns
		B1 and B2		8.5	3.1	7.9	
t_{dis}	CLK	A or B		5.8	1.9	6.2	ns

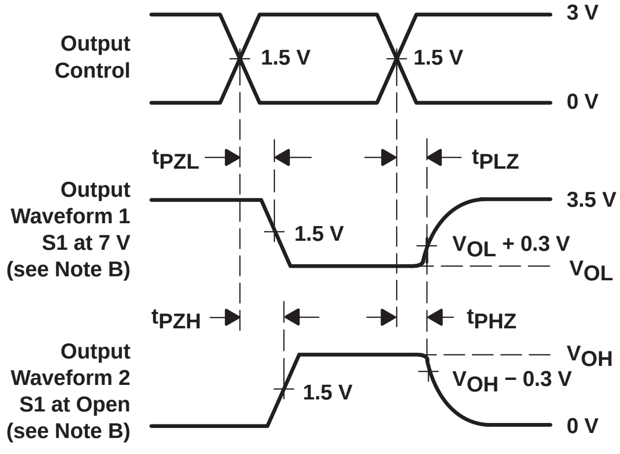
[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

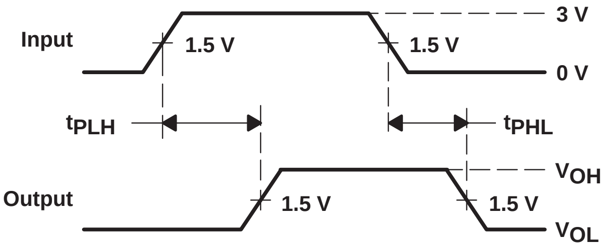
PARAMETER MEASUREMENT INFORMATION


From Output Under Test
C_L = 50 pF (see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Output Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SN74CBT16233
16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS010K − MAY 1995 − REVISED NOVEMBER 2001

- **Member of the Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

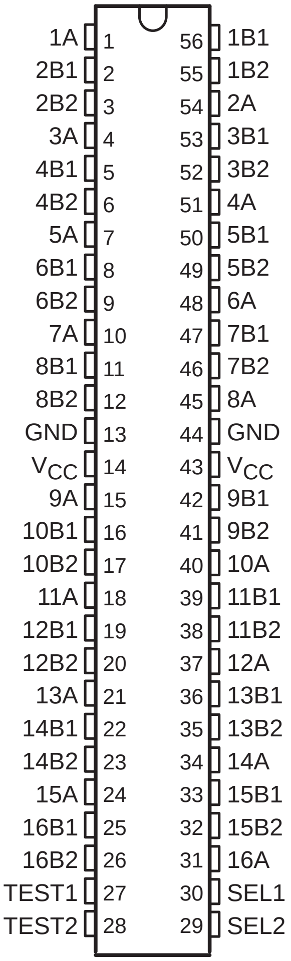
description

The SN74CBT16233 is a 16-bit 1-of-2 FET multiplexer/demultiplexer used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, where two different banks of memory need to be addressed simultaneously. The device can be used as two 8-bit to 16-bit multiplexers or as one 16-bit to 32-bit multiplexer.

Two select (SEL1 and SEL2) inputs control the data flow. When the TEST inputs are asserted, the A port is connected to both the B1 and the B2 ports. SEL1, SEL2, and the TEST inputs can be driven with a 5-V CMOS, a 5-V TTL, or a low-voltage TTL driver.

This device is designed so it does not have through current when switching directions.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



1A	1	56	1B1
2B1	2	55	1B2
2B2	3	54	2A
3A	4	53	3B1
4B1	5	52	3B2
4B2	6	51	4A
5A	7	50	5B1
6B1	8	49	5B2
6B2	9	48	6A
7A	10	47	7B1
8B1	11	46	7B2
8B2	12	45	8A
GND	13	44	GND
V_{CC}	14	43	V_{CC}
9A	15	42	9B1
10B1	16	41	9B2
10B2	17	40	10A
11A	18	39	11B1
12B1	19	38	11B2
12B2	20	37	12A
13A	21	36	13B1
14B1	22	35	13B2
14B2	23	34	14A
15A	24	33	15B1
16B1	25	32	15B2
16B2	26	31	16A
TEST1	27	30	SEL1
TEST2	28	29	SEL2

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16233DL	CBT16233
		Tape and reel	SN74CBT16233DLR	
	TSSOP − DGG	Tape and reel	SN74CBT16233DGGR	CBT16233
	TVSOP − DGV	Tape and reel	SN74CBT16233DGVR	CY233

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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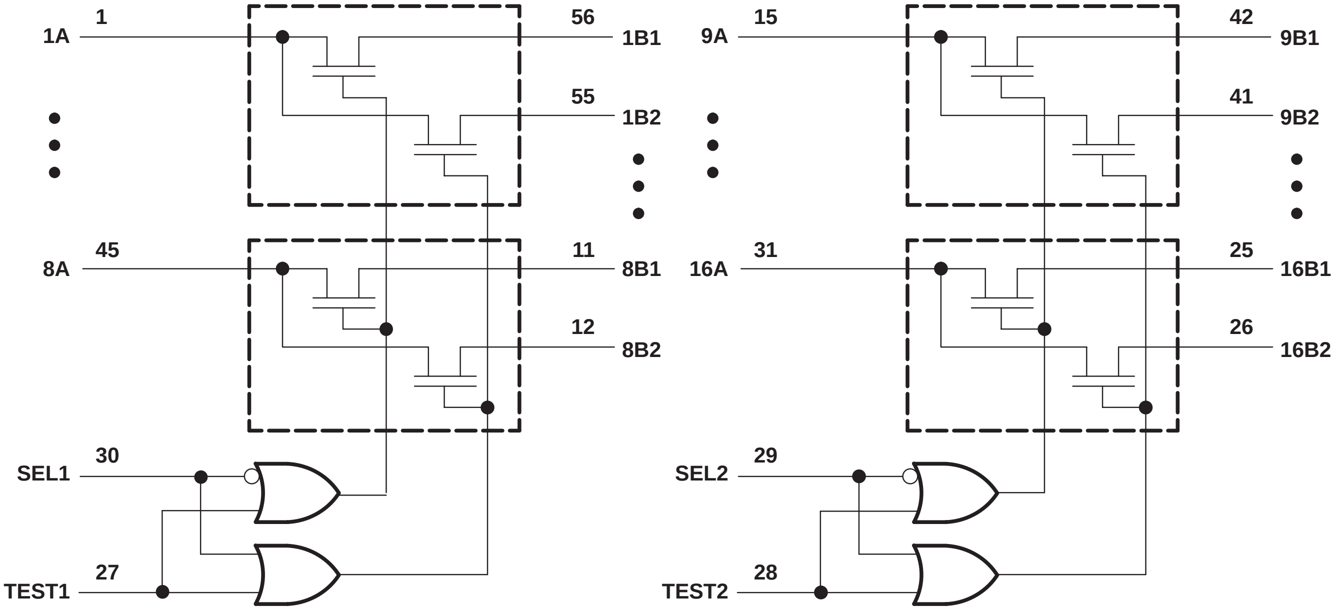
FUNCTION TABLE
(each multiplexer/demultiplexer)

INPUTS		FUNCTION
SEL	TEST	
L	L	A = B1
H	L	A = B2
X	H	A = B1 and A = B2

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to V_{CC} + 0.5 V
Continuous channel current		128 mA
Input clamp current, I_{IK} (V_I < 0)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.25 V				10	μA
		V_{CC} = 5.25 V,	V_I = 5.25 V or GND				±1	μA
I_{CC}		V_{CC} = 5.25 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.25 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				4.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0				4		pF
r_{on}§		V_{CC} = 4.75 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		7	12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

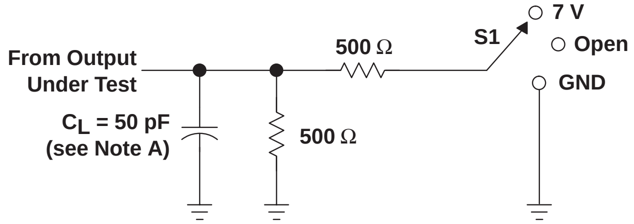
§ Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}¶	A or B	B or A		0.25	ns
t_{pd}	SEL	A	1.6	5.3	ns
t_{en}	TEST or SEL	B	1.3	5.2	ns
t_{dis}	TEST or SEL	B	1	5.3	ns

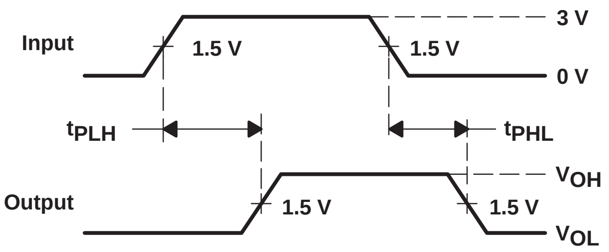
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

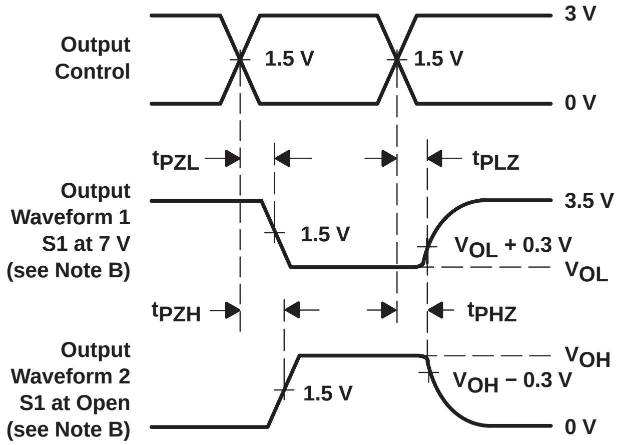

From Output Under Test
500 Ω
S1
7 V
Open
GND
C_L = 50 pF (see Note A)
500 Ω

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SN74CBT16390
16-BIT TO 32-BIT FET MULTIPLEXER/DEMULTIPLEXER BUS SWITCH

SCDS035E − OCTOBER 1997 − REVISED OCTOBER 2000

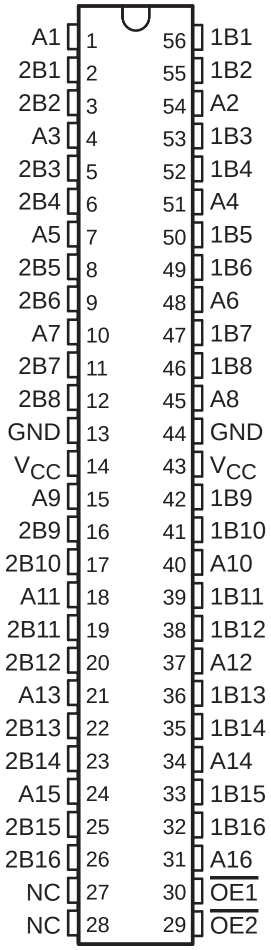
- **Member of Texas Instruments' Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

description

The SN74CBT16390 is a 16-bit to 32-bit switch used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, in which two different banks of memory must be addressed simultaneously. This device also can be used to connect or isolate the PCI bus to one or two slots simultaneously.

Two output enables ($\overline{\text{OE1}}$ and $\overline{\text{OE2}}$) control the data flow. When $\overline{\text{OE1}}$ is low, A port is connected to 1B port. When $\overline{\text{OE2}}$ is low, A port is connected to 2B port. When both $\overline{\text{OE1}}$ and $\overline{\text{OE2}}$ are low, the A port is connected to both 1B and 2B ports. The control inputs can be driven with a 5-V CMOS, 5-V TTL, or an LVTTL driver.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


A1 1 56 1B1
2B1 2 55 1B2
2B2 3 54 A2
A3 4 53 1B3
2B3 5 52 1B4
2B4 6 51 A4
A5 7 50 1B5
2B5 8 49 1B6
2B6 9 48 A6
A7 10 47 1B7
2B7 11 46 1B8
2B8 12 45 A8
GND 13 44 GND
V_{CC} 14 43 V_{CC}
A9 15 42 1B9
2B9 16 41 1B10
2B10 17 40 A10
A11 18 39 1B11
2B11 19 38 1B12
2B12 20 37 A12
A13 21 36 1B13
2B13 22 35 1B14
2B14 23 34 A14
A15 24 33 1B15
2B15 25 32 1B16
2B16 26 31 A16
NC 27 30 $\overline{\text{OE1}}$
NC 28 29 $\overline{\text{OE2}}$

NC − No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16390DL	CBT16390
		Tape and reel	SN74CBT16390DLR	
	TSSOP − DGG	Tape and reel	SN74CBT16390DGGR	CBT16390
	TVSOP − DGV	Tape and reel	SN74CBT16390DGVR	CY390

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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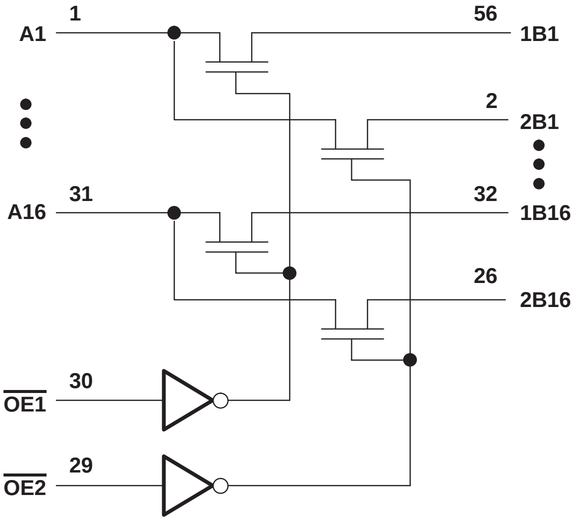
FUNCTION TABLE

INPUTS		FUNCTION
$\overline{\text{OE1}}$	$\overline{\text{OE2}}$	
L	L	A = 1B and A = 2B
L	H	A = 1B
H	L	A = 2B
H	H	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Continuous channel current	128 mA
Input clamp current, I_{IK} (V_I < 0)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	64°C/W
DGV package	48°C/W
DL package	56°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	µA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other input at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				5		pF
$C_{io(OFF)}$		V_O = 3 V or 0				5.5		pF
r_{on}[§]		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		7	12	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

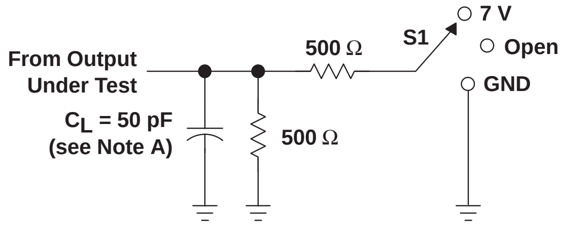
[§] Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}[¶]	A or B	B or A		0.25	ns
t_{en}	$\overline{\text{OE}}$	A or B	1.3	5.9	ns
t_{dis}	$\overline{\text{OE}}$	A or B	1	5.3	ns

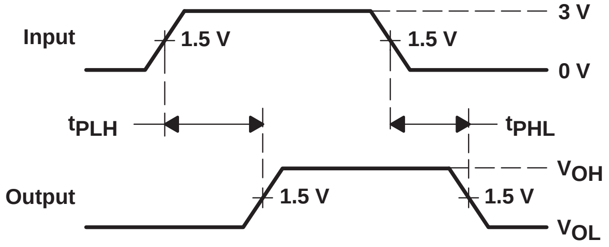
[¶] The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

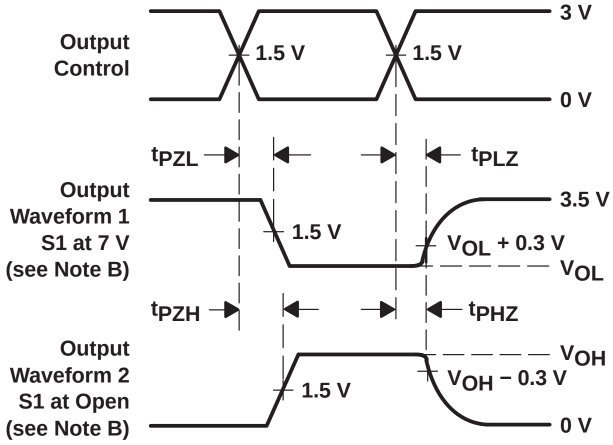

From Output
Under Test
CL = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
tPLH
tPHL
Output
1.5 V
1.5 V
VOH
VOL

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
tPZL
tPLZ
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
VOL + 0.3 V
VOL
tPZH
tPHZ
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
VOH
VOH − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
  Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SN54CBT3383, SN74CBT3383
10-BIT FET BUS-EXCHANGE SWITCHES

SCDS003M − NOVEMBER 1992 − REVISED NOVEMBER 2001

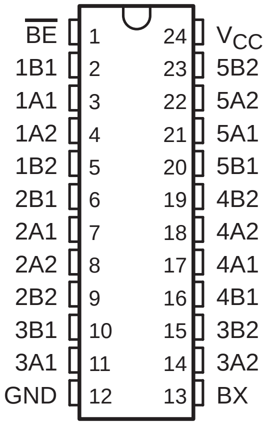
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

description

The ’CBT3383 devices provide ten bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The devices operate as a 10-bit bus switch or a 5-bit bus exchanger, which provides swapping of the A and B pairs of signals. The bus-exchange function is selected when BX is high. The switches are connected when $\overline{BE}$ is low.

SN54CBT3383 . . . JT OR W PACKAGE
SN74CBT3383 . . . DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74CBT3383DW	CBT3383
		Tape and reel	SN74CBT3383DWR	
	SSOP − DB	Tape and reel	SN74CBT3383DBR	CU383
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBT3383DBQR	CBT3383
	TSSOP − PW	Tape and reel	SN74CBT3833PWR	CU383
	TVSOP − DGV	Tape and reel	SN74CBT3833DGVR	CU383
−55°C to 125°C	CDIP − JT	Tube	SNJ54CBT3383JT	SNJ54CBT3383JT
	CFP − W	Tube	SNJ54CBT3383W	SNJ54CBT3383W

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{BE}$	BX	1A1−5A1	1A2−5A2
L	L	1B1−5B1	1B2−5B2
L	H	1B2−5B2	1B1−5B1
H	X	Z	Z

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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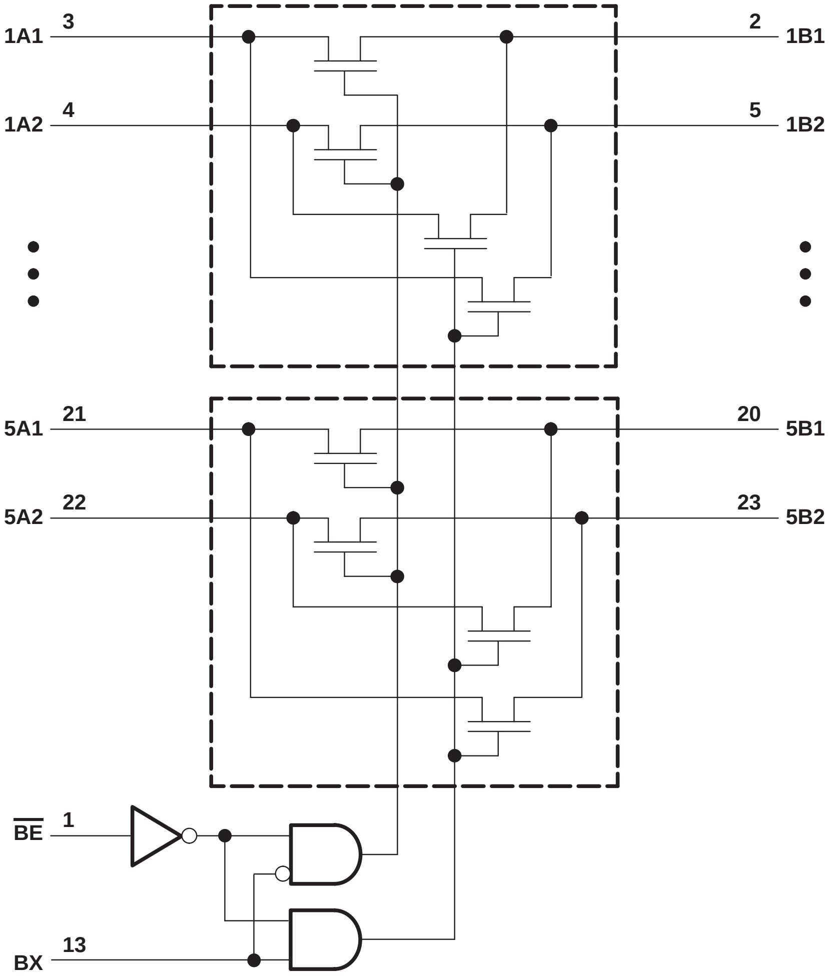
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	63°C/W
	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54CBT3383		SN74CBT3383		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level control input voltage	2		2		V
V_{IL}	Low-level control input voltage		0.8		0.8	V
T_A	Operating free-air temperature	−55	125	0	70	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54CBT3383			SN74CBT3383			UNIT
					MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA					−1.2			−1.2	V
I_I		V_{CC} = 5.5 V, V_I = 5.5 V or GND					±5			±1	µA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND					50			50	µA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					2.5			2.5	mA
C_i	Control inputs	V_I = 3 V or 0							3		pF
		V_I = 2.5 V					5				
$C_{io(OFF)}$		V_O = 3 V or 0, $\overline{BE}$ = V_{CC}							6		pF
		V_O = 2.5 V, $\overline{BE}$ = V_{CC}					6				
r_{on}[§]		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	9.2		5	7	Ω
				I_I = 30 mA					5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	17		10	15	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

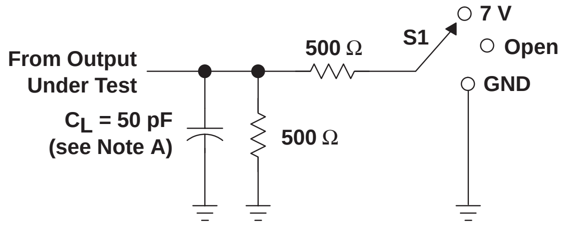
[§] Measured by the voltage drop between the input terminal and the output terminal at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBT3383		SN74CBT3383		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A		1.5		0.25	ns
t_{pd}	BX	A or B	1	10.2	1	9.2	ns
t_{en}	$\overline{BE}$	A or B	1	10.8	1	8.6	ns
t_{dis}	$\overline{BE}$	A or B	1	8.2	1	7.5	ns

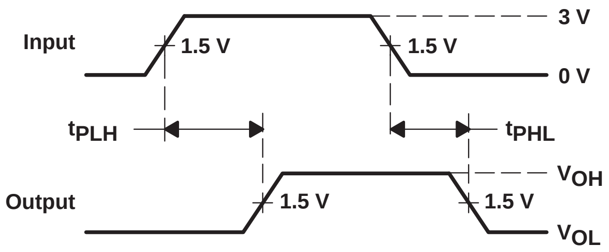
[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

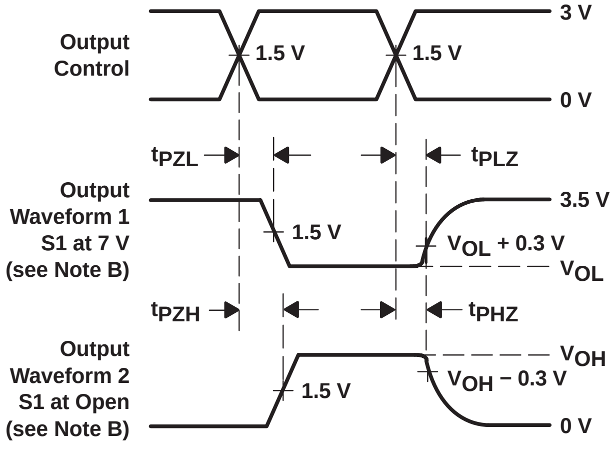

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SN54CBT16209, SN74CBT16209A
18-BIT FET BUS-EXCHANGE SWITCHES

SCDS006N − NOVEMBER 1992 − REVISED NOVEMBER 2001

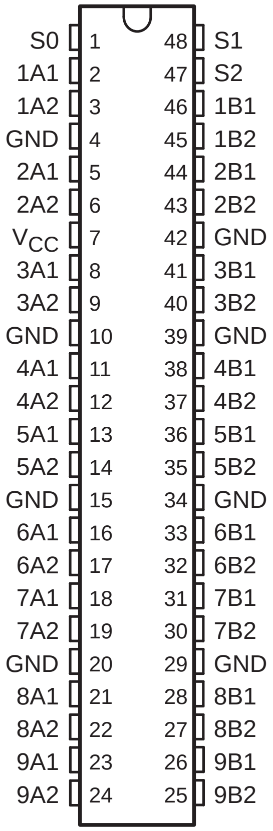
- **Members of the Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

description

The SN54CBT16209 and SN74CBT16209A devices provide 18 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switches allows connections to be made with minimal propagation delay.

The devices operate as an 18-bit bus switch or a 9-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0, S1, S2) terminals.

SN54CBT16209 . . . WD PACKAGE
SN74CBT16209A . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)


S0 1 48 S1
1A1 2 47 S2
1A2 3 46 1B1
GND 4 45 1B2
2A1 5 44 2B1
2A2 6 43 2B2
V$_{CC}$ 7 42 GND
3A1 8 41 3B1
3A2 9 40 3B2
GND 10 39 GND
4A1 11 38 4B1
4A2 12 37 4B2
5A1 13 36 5B1
5A2 14 35 5B2
GND 15 34 GND
6A1 16 33 6B1
6A2 17 32 6B2
7A1 18 31 7B1
7A2 19 30 7B2
GND 20 29 GND
8A1 21 28 8B1
8A2 22 27 8B2
9A1 23 26 9B1
9A2 24 25 9B2

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16209ADL	CBT16209A
		Tape and reel	SN74CBT616209ADLR	
	TSSOP − DGG	Tape and reel	SN74CBT16209ADGGR	CBT16209A
	TVSOP − DGV	Tape and reel	SN74CBT16209ADGVR	CY209A
−55°C to 125°C	CFP − WD	Tube	SNJ54CBT16209WD	SNJ54CBT16209WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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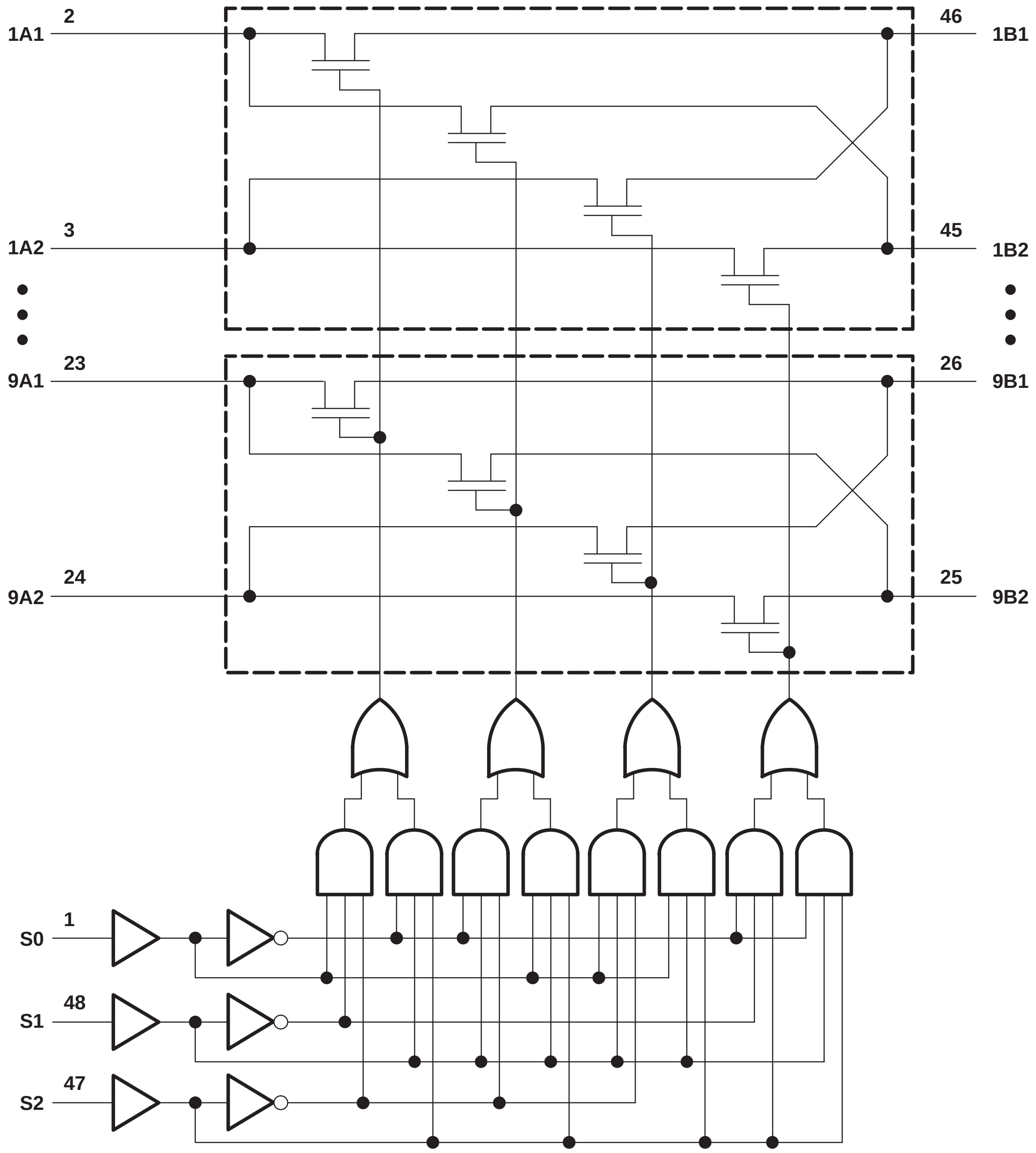
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	S1	S0	A1	A2	
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 port = B1 port
L	H	L	B2	Z	A1 port = B2 port
L	H	H	Z	B1	A2 port = B1 port
H	L	L	Z	B2	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 port = B1 port A2 port = B2 port
H	H	H	B2	B1	A1 port = B2 port A2 port = B1 port

logic diagram (positive logic)


1A1
2
46
1B1
1A2
3
45
1B2
9A1
23
26
9B1
9A2
24
25
9B2
S0
1
S1
48
S2
47

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54CBT16209		SN74CBT16209A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4	5.5	4	5.5	V
V_{IH}	High-level control input voltage	2		2		V
V_{IL}	Low-level control input voltage		0.8		0.8	V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	µA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				4		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	S0, S1, and S2 = GND			7.5		pF
r_{on}¶		V_{CC} = 4 V TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		4	8	
				I_I = 30 mA		4	8	
			V_I = 2.4 V,	I_I = 15 mA		6	15	

‡ All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

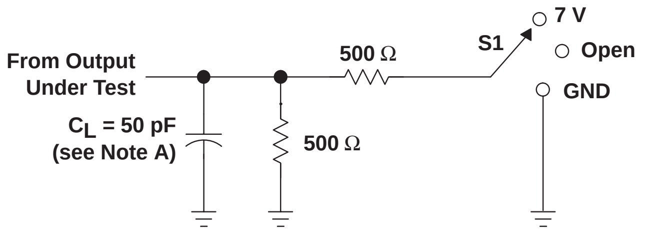
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBT16209				SN74CBT16209A				UNIT
			V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}†	A or B	B or A				0.8*		0.35		0.25	ns
t_{pd}	S	A or B		14	2	13.1		9.9	1.5	9	ns
t_{en}	S	A or B		16	1.7	15.3		10.3	1.5	9.8	ns
t_{dis}	S	A or B		14.5	1	13.2		9.3	1.5	8.8	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

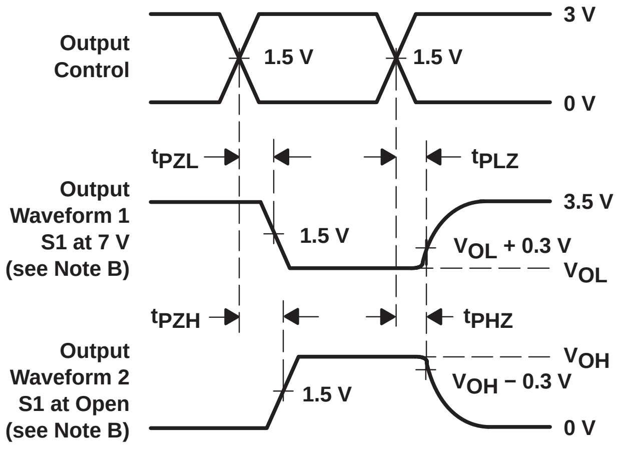
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

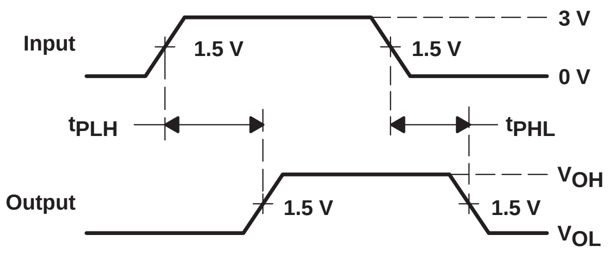
PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Output
Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 7 V
(see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at Open
(see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SN54CBT16212A, SN74CBT16212A
24-BIT FET BUS-EXCHANGE SWITCHES

SCDS007T − NOVEMBER 1992 − REVISED SEPTEMBER 2003

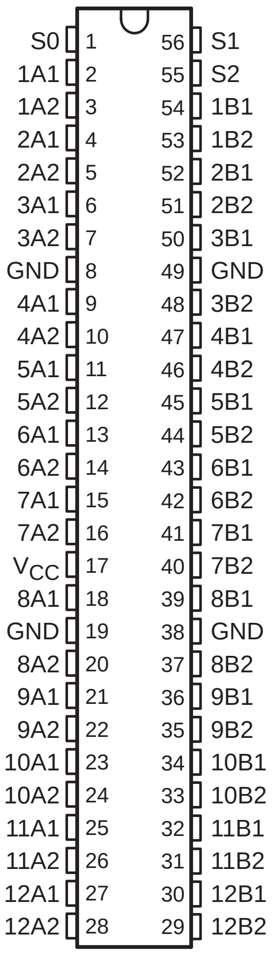
- **Members of the Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

description/ordering information

The ’CBT16212A devices provide 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

Each device operates as a 24-bit bus switch or a 12-bit bus exchanger that provides data exchanging between the four signal ports via the data-select (S0, S1, S2) terminals.

SN54CBT16212A . . . WD PACKAGE
SN74CBT16212A . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)


S0 1 56 S1
1A1 2 55 S2
1A2 3 54 1B1
2A1 4 53 1B2
2A2 5 52 2B1
3A1 6 51 2B2
3A2 7 50 3B1
GND 8 49 GND
4A1 9 48 3B2
4A2 10 47 4B1
5A1 11 46 4B2
5A2 12 45 5B1
6A1 13 44 5B2
6A2 14 43 6B1
7A1 15 42 6B2
7A2 16 41 7B1
VCC 17 40 7B2
8A1 18 39 8B1
GND 19 38 GND
8A2 20 37 8B2
9A1 21 36 9B1
9A2 22 35 9B2
10A1 23 34 10B1
10A2 24 33 10B2
11A1 25 32 11B1
11A2 26 31 11B2
12A1 27 30 12B1
12A2 28 29 12B2

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16212ADL	CBT16212A
		Tape and reel	SN74CBT16212ADLR	
	TSSOP − DGG	Tape and reel	SN74CBT16212ADGGR	CBT16212A
	TVSOP − DGV	Tape and reel	SN74CBT16212ADGVR	CY212A
	VFBGA − GQL	Tape and reel	SN74CBT16212AGQLR	CY212A
	VFBGA − ZQL (Pb-free)		SN74CBT16212AZQLR	
−55°C to 125°C	CFP − WD	Tube	SNJ54CBT16212AWD	SNJ54CBT16212AWD

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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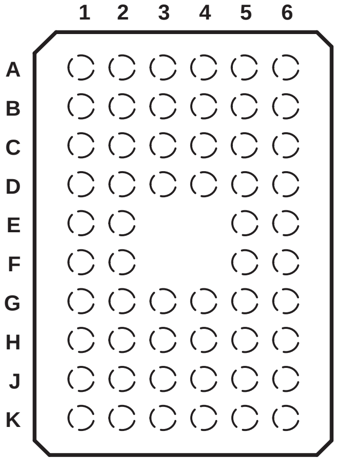
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**GQL OR ZQL PACKAGE
(TOP VIEW)**



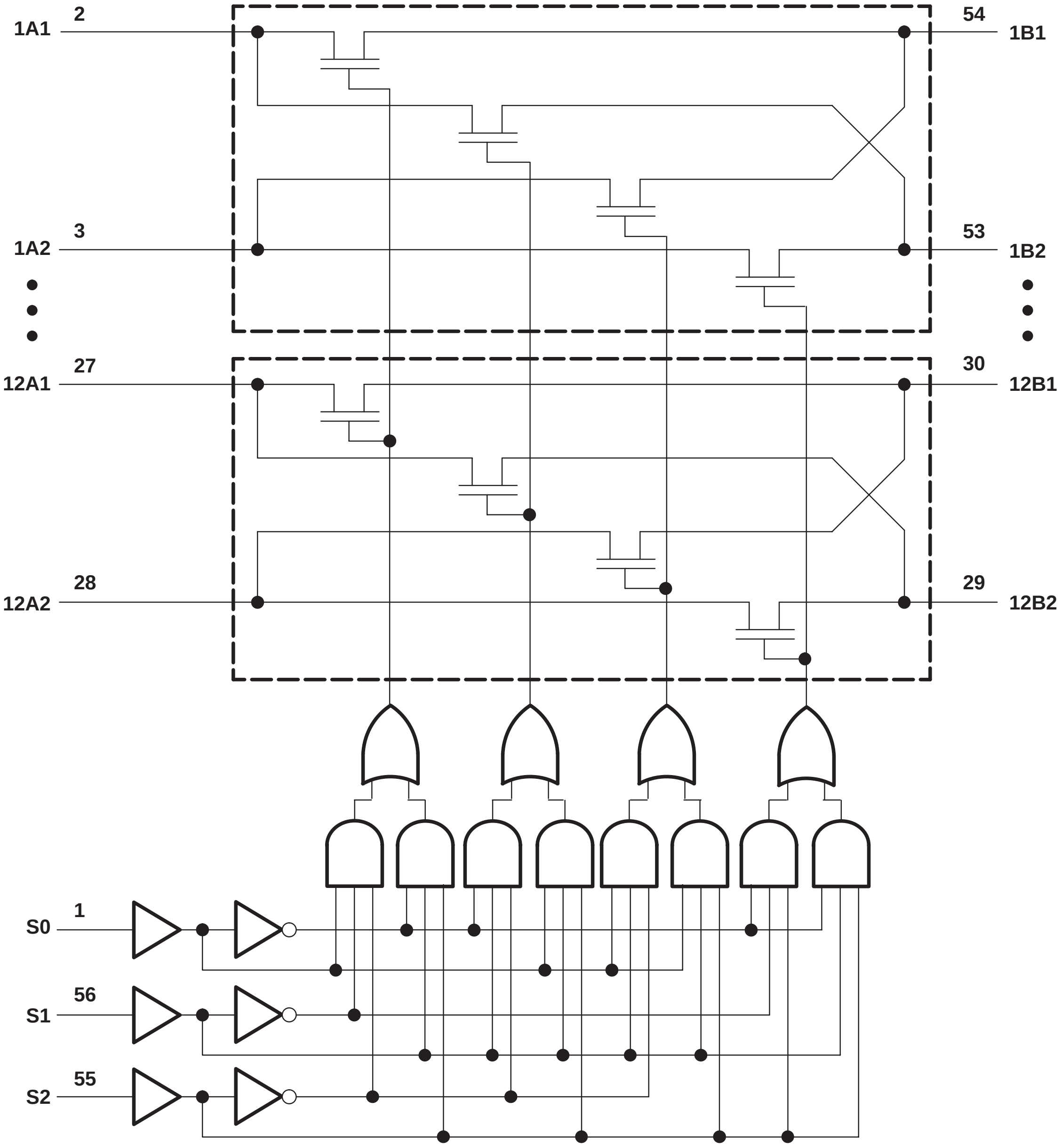
terminal assignments

	1	2	3	4	5	6
A	1A2	1A1	S0	S1	S2	1B1
B	3A1	2A2	2A1	1B2	2B1	2B2
C	4A1	GND	3A2	3B1	GND	3B2
D	5A2	4A2	5A1	4B2	4B1	5B1
E	6A2	6A1			5B2	6B1
F	7A1	7A2			7B1	6B2
G	V_{CC}	GND	8A1	8B1	GND	7B2
H	8A2	9A1	9A2	9B2	9B1	8B2
J	10A1	10A2	11A1	11B1	10B2	10B1
K	11A2	12A1	12A2	12B2	12B1	11B2

FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	S1	S0	A1	A2	
L	L	L	Z	Z	Disconnect
L	L	H	B1 port	Z	A1 port = B1 port
L	H	L	B2 port	Z	A1 port = B2 port
L	H	H	Z	B1 port	A2 port = B1 port
H	L	L	Z	B2 port	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1 port	B2 port	A1 port = B1 port A2 port = B2 port
H	H	H	B2 port	B1 port	A1 port = B2 port A2 port = B1 port

logic diagram (positive logic)


1A1
2
54
1B1
1A2
3
53
1B2
12A1
27
30
12B1
12A2
28
29
12B2
S0
1
S1
56
S2
55

Pin numbers shown are for the DGG, DGV, DL, and WD packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} (V_I < 0)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
	GQL/ZQL package	42°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54CBT16212A		SN74CBT16212A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4	5.5	4	5.5	V
V_{IH}	High-level control input voltage	2		2		V
V_{IL}	Low-level control input voltage		0.8		0.8	V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54CBT16212A			SN74CBT16212A			UNIT
					MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2			−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10			10	µA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1			±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0, V_I = V_{CC} or GND				3.2			3	µA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					2.5			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				2.5			2.5		pF
$C_{io(off)}$		V_O = 3 V or 0,	S0, S1, and S2 = GND			7.5			7.5		pF
r_{on}[¶]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V, I_I = 15 mA			14	20		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		4	10		4	7	
				I_I = 30 mA		4	10		4	7	
			V_I = 2.4 V, I_I = 15 mA			6	14		6	12	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

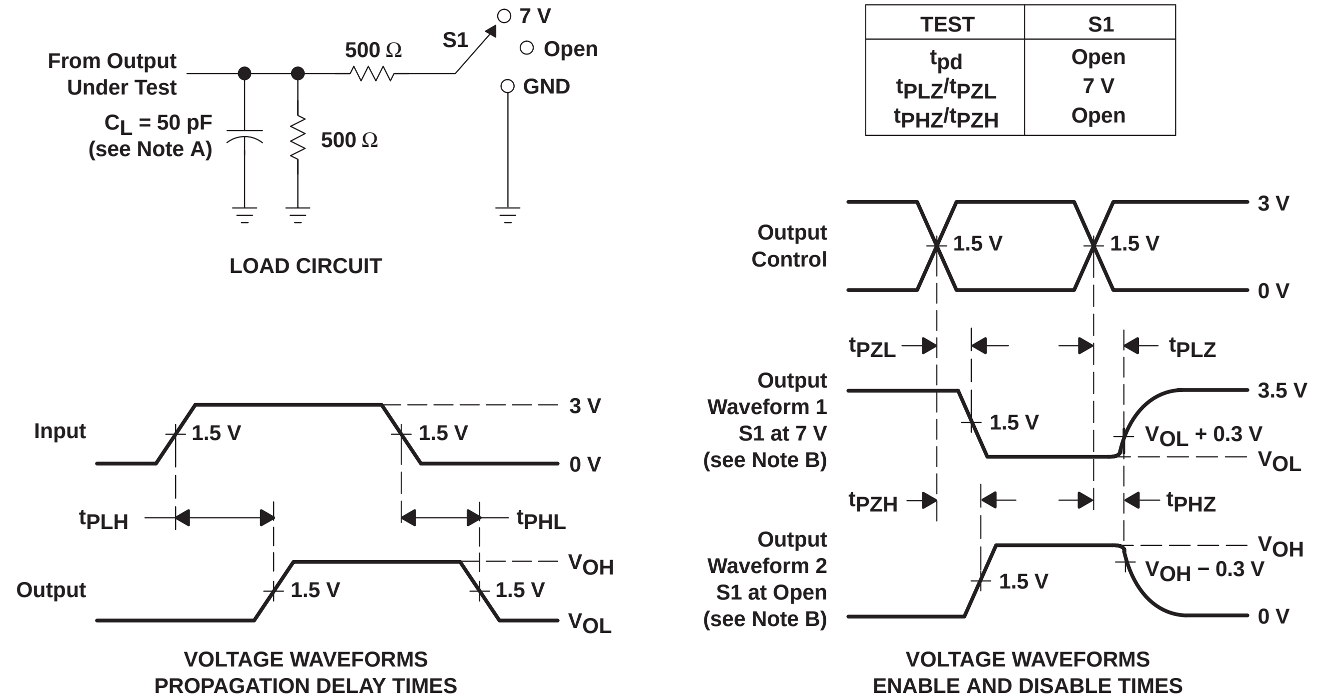
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBT16212A				SN74CBT16212A				UNIT
			V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}†	A or B	B or A				0.8*		0.35		0.25	ns
t_{pd}	S	A or B		14	1.5	13		10	1.5	9.1	ns
t_{en}	S	A or B		15	1.5	13.7		10.4	1.5	9.7	ns
t_{dis}	S	A or B		14.2	1.5	13.5		9.2	1.5	8.8	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION


From Output Under Test
500 Ω
S1
7 V
Open
GND
C_L = 50 pF (see Note A)
500 Ω
Output Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V
Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

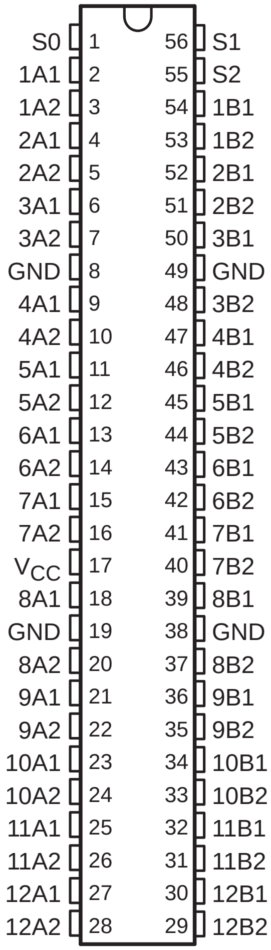
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTS16212
24-BIT FET BUS-EXCHANGE SWITCH WITH SCHOTTKY DIODE CLAMPING

SCDS036E − DECEMBER 1997 − REVISED NOVEMBER 2001

- **Member of the Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


S0 1 56 S1
1A1 2 55 S2
1A2 3 54 1B1
2A1 4 53 1B2
2A2 5 52 2B1
3A1 6 51 2B2
3A2 7 50 3B1
GND 8 49 GND
4A1 9 48 3B2
4A2 10 47 4B1
5A1 11 46 4B2
5A2 12 45 5B1
6A1 13 44 5B2
6A2 14 43 6B1
7A1 15 42 6B2
7A2 16 41 7B1
VCC 17 40 7B2
8A1 18 39 8B1
GND 19 38 GND
8A2 20 37 8B2
9A1 21 36 9B1
9A2 22 35 9B2
10A1 23 34 10B1
10A2 24 33 10B2
11A1 25 32 11B1
11A2 26 31 11B2
12A1 27 30 12B1
12A2 28 29 12B2

description

The SN74CBTS16212 provides 24 bits of high-speed TTL-compatible bus switching or exchanging with Schottky diodes on the I/Os to clamp undershoot. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 24-bit bus switch or as a 12-bit bus exchanger that provides data exchanging between the four signal ports via the data-select (S0−S2) terminals.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBTS16212DL	CBTS16212
		Tape and reel	SN74CBTS16212DLR	
	TSSOP − DGG	Tape and reel	SN74CBTS16212DGGR	CBTS16212
	TVSOP − DGV	Tape and reel	SN74CBTS16212DGVR	CYS212

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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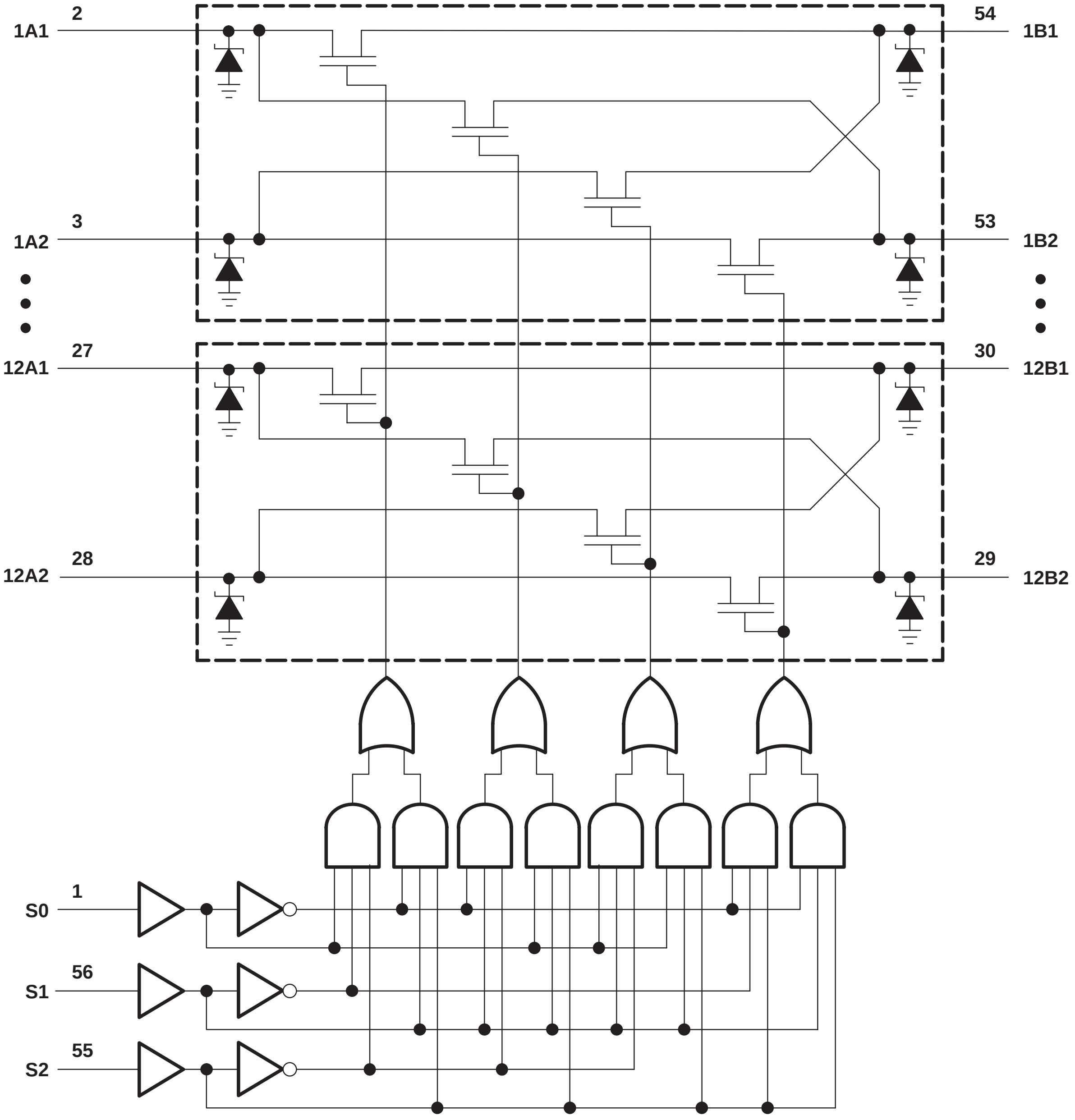
FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	**S1**	**S0**	**A1**	**A2**	
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 port = B1 port
L	H	L	B2	Z	A1 port = B2 port
L	H	H	Z	B1	A2 port = B1 port
H	L	L	Z	B2	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 port = B1 port A2 port = B2 port
H	H	H	B2	B1	A1 port = B2 port A2 port = B1 port

logic diagram (positive logic)


2
1A1
54
1B1
3
1A2
53
1B2
27
12A1
30
12B1
28
12A2
29
12B2
1
S0
56
S1
55
S2

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V
Continuous channel current . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . 64°C/W
DGV package . . . . 48°C/W
DL package . . . . 56°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I	I_{IL}	V_{CC} = 5.5 V,	V_I = GND				−1	μA
	I_{IH}	V_{CC} = 5.5 V,	V_I = 5.5 V				150	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				2.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	S0, S1, and S2 = GND			10.5		pF
r_{on}¶		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA			20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		4	7	
				I_I = 30 mA		4	7	
			V_I = 2.4 V,	I_I = 15 mA		6	12	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

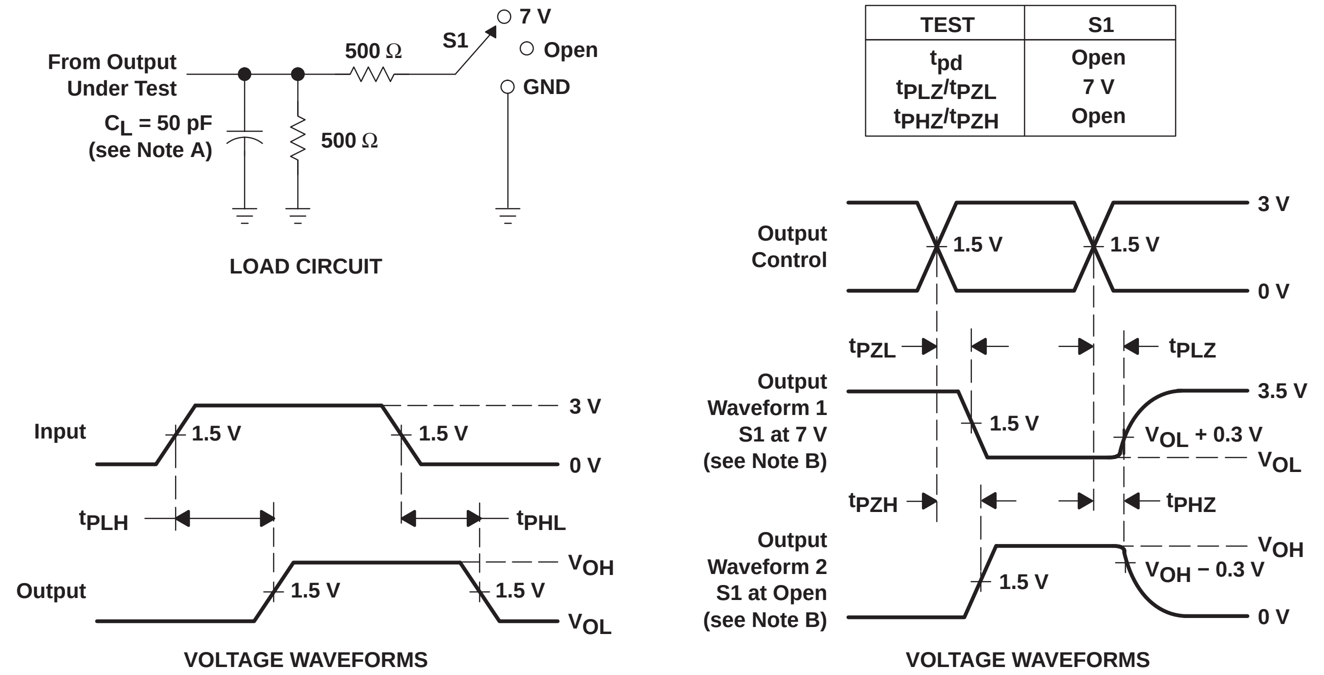
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.35		0.25	ns
t_{pd}	S	A or B		10	1.5	9.1	ns
t_{en}	S	A or B		10.4	1.5	9.7	ns
t_{dis}	S	A or B		9.2	1.5	8.8	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION


From Output Under Test
500 Ω
S1
7 V
Open
GND
C_L = 50 pF (see Note A)
500 Ω
Output Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
V_{OH}
V_{OH} − 0.3 V
1.5 V
0 V
Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SN74CBT16213
24-BIT FET BUS-EXCHANGE SWITCH

SCDS026I − MAY 1995 − REVISED NOVEMBER 2001

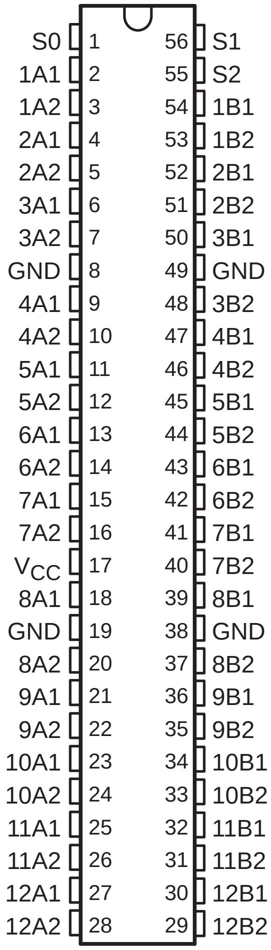
- **Member of the Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

description

The SN74CBT16213 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 24-bit bus switch or a 12-bit bus exchanger that provides data exchanging between the four signal ports via the data-select (S0−S2) terminals.

DGG OR DL PACKAGE
(TOP VIEW)


S0 1 56 S1
1A1 2 55 S2
1A2 3 54 1B1
2A1 4 53 1B2
2A2 5 52 2B1
3A1 6 51 2B2
3A2 7 50 3B1
GND 8 49 GND
4A1 9 48 3B2
4A2 10 47 4B1
5A1 11 46 4B2
5A2 12 45 5B1
6A1 13 44 5B2
6A2 14 43 6B1
7A1 15 42 6B2
7A2 16 41 7B1
VCC 17 40 7B2
8A1 18 39 8B1
GND 19 38 GND
8A2 20 37 8B2
9A1 21 36 9B1
9A2 22 35 9B2
10A1 23 34 10B1
10A2 24 33 10B2
11A1 25 32 11B1
11A2 26 31 11B2
12A1 27 30 12B1
12A2 28 29 12B2

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16213DL	CBT16213
		Tape and reel	SN74CBT16213DLR	
	TSSOP − DGG	Tape and reel	SN74CBT16213DGGR	CBT16213

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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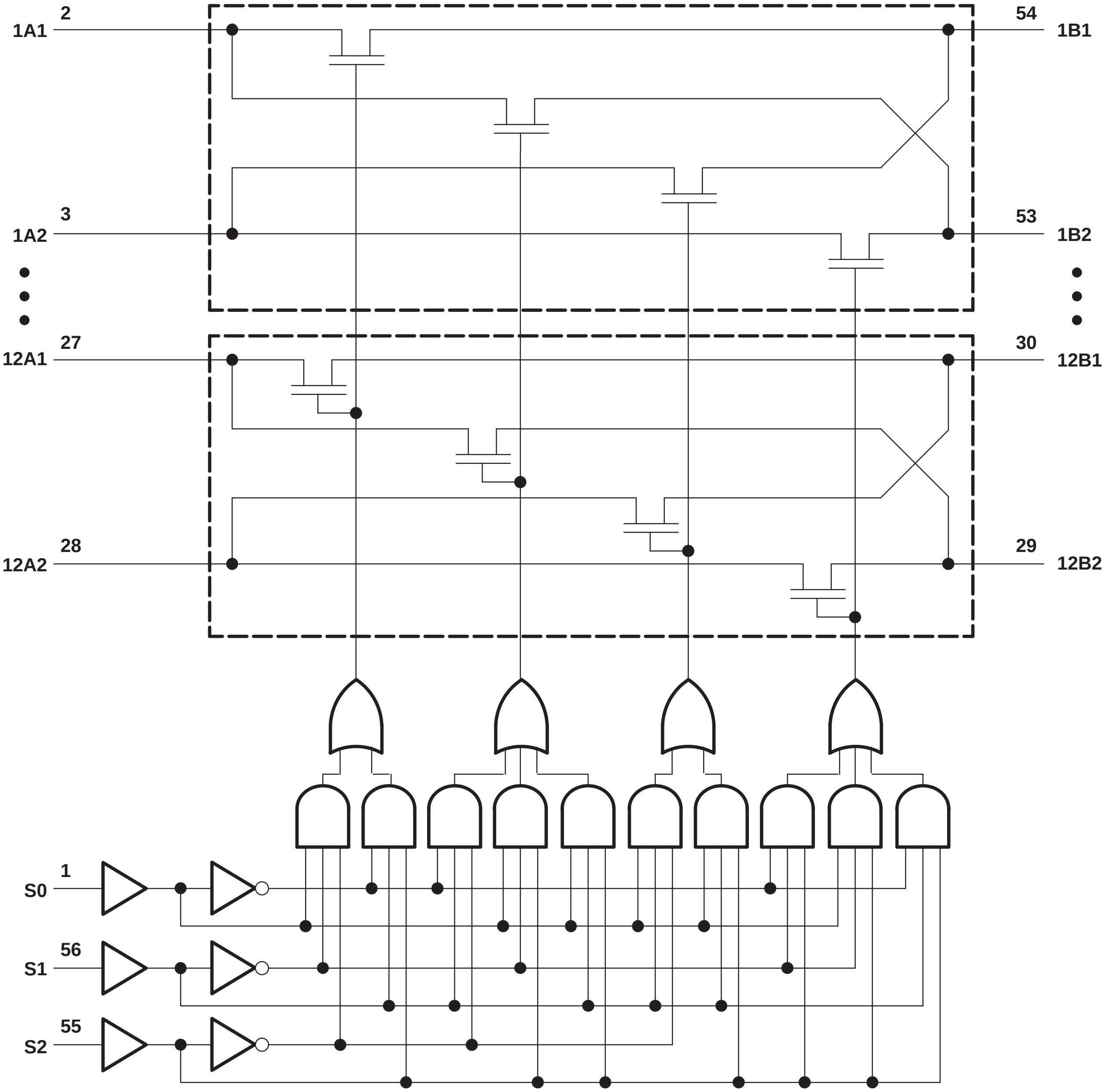
FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	**S1**	**S0**	**A1**	**A2**	
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 port = B1 port
L	H	L	B2	Z	A1 port = B2 port
L	H	H	Z	B1	A2 port = B1 port
H	L	L	Z	B2	A2 port = B2 port
H	L	H	A2 and B2	A1 and B2	A1 port = A2 port = B2 port
H	H	L	B1	B2	A1 port = B1 port A2 port = B2 port
H	H	H	B2	B1	A1 port = B2 port A2 port = B1 port

logic diagram (positive logic)


1A1
2
54
1B1
1A2
3
53
1B2
12A1
27
30
12B1
12A2
28
29
12B2
S0
1
S1
56
S2
55

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	64°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	µA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				4.5		pF
$C_{io(OFF)}$	B port	V_O = 3 V or 0,	S0, S1, and S2 = GND			8.5		pF
	A port					8		
r_{on}¶	A to B or B to A	V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		8	15	
	A1 to A2	V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		22	30	
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		10	14	
				I_I = 30 mA		10	14	
			V_I = 2.4 V,	I_I = 15 mA		16	22	

‡ All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

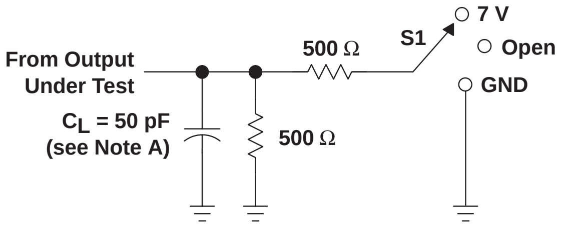
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}†	A or B	B or A		0.35		0.25	ns
	A1	A2		0.5		0.5	
t_{en}	S	A or B		12.4	3.2	11.1	ns
t_{dis}	S	A or B		12.4	2.3	11.9	ns
t_{en}	S0	A2 and B2		11.5	4	10.9	ns
t_{dis}	S0	A2 and B2		12.8	5.7	12	ns

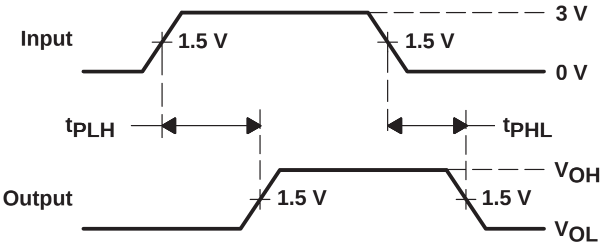
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

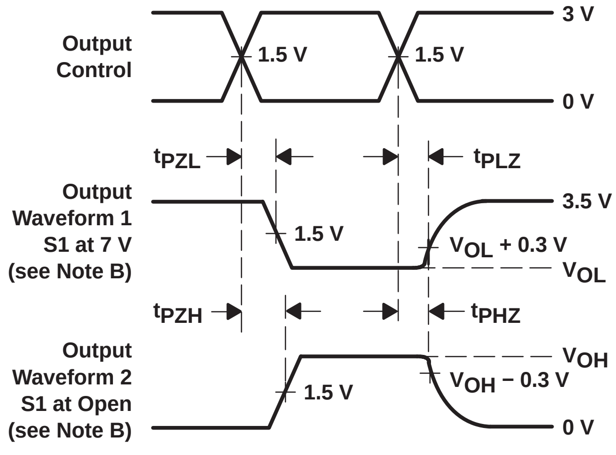

From Output Under Test
C_L = 50 pF (see Note A)
500 Ω
500 Ω
S1
7 V
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open


Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
Output
1.5 V
1.5 V
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B)
1.5 V
3.5 V
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at Open (see Note B)
1.5 V
V_{OH}
V_{OH} − 0.3 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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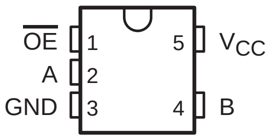
SN74CBTLV1G125
LOW-VOLTAGE SINGLE FET BUS SWITCH

SCDS057G − MARCH 1998 − REVISED OCTOBER 2003

- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**

DBV OR DCK PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBTLV1G125 features a single high-speed line switch. The switch is disabled when the output-enable ($\overline{\mathrm{OE}}$) input is high.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\mathrm{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	SOT (SOT-23) − DBV	Tape and reel	SN74CBTLV1G125DBVR	V25_
	SOT (SC-70) − DCK	Tape and reel	SN74CBTLV1G125DCKR	VM_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE

INPUT $\overline{\mathrm{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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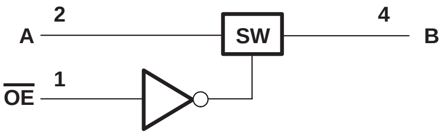
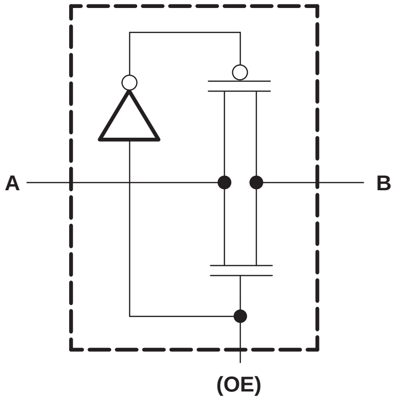
logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)		−0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DBV package	206°C/W
	DCK package	252°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	$V_I = V_{CC}$ or GND				±1	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	µA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	$V_I = V_{CC}$ or GND			10	µA
ΔI_{CC}‡	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	µA
C_i	Control inputs	V_I = 3 V or 0				2.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE} = V_{CC}$			7		pF
r_{on}§		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		7	10	Ω
				I_I = 24 mA		7	10	
			V_I = 1.7 V,	I_I = 15 mA		15	25	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

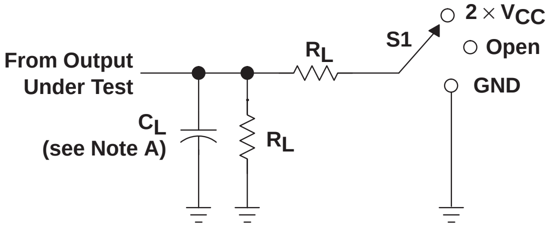
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	4	1	4	ns
t_{dis}	$\overline{OE}$	A or B	1	5	1	4.1	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

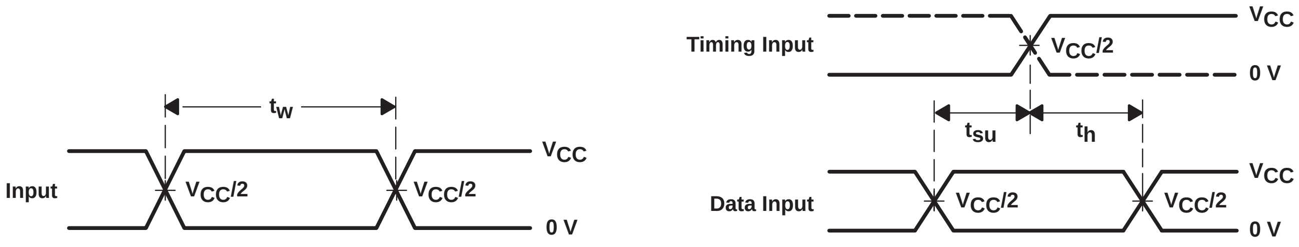
PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
R_L
S1
2 × V_{CC}
Open
GND
C_L
(see Note A)
R_L

LOAD CIRCUIT

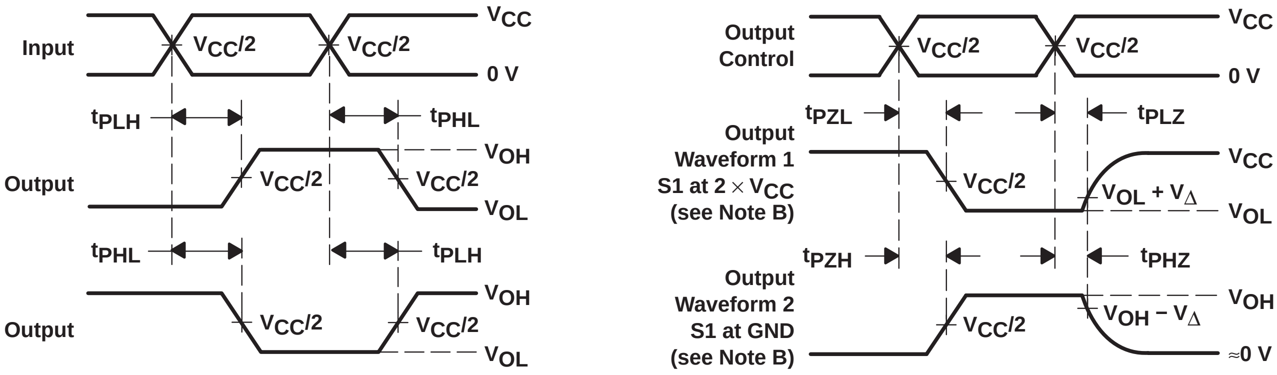
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
Timing Input
V_{CC}
$V_{CC}/2$
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
Output
Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 2 × V_{CC}
(see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at GND
(see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2$ ns, $t_f \le 2$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

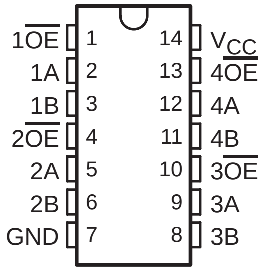
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTLV3125
LOW-VOLTAGE QUADRUPLE FET BUS SWITCH

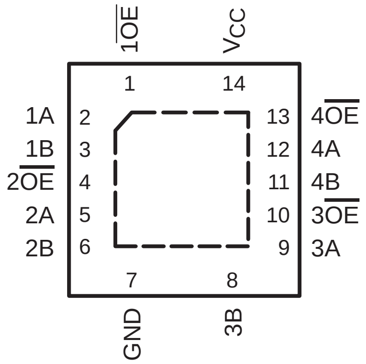
SCDS037J − DECEMBER 1997 − REVISED OCTOBER 2003

- **Standard ’125-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

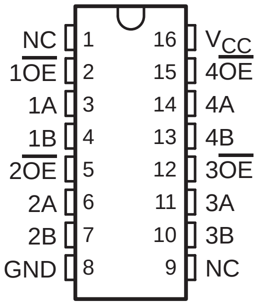
D, DGV, NS, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



DBQ PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The SN74CBTLV3125 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable ($\overline{\text{OE}}$) input is high.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBTLV3125RGYR	CL125
	SOIC − D	Tube	SN74CBTLV3125D	CBTLV3125
		Tape and reel	SN74CBTLV3125DR	
	SOP − NS	Tape and reel	SN74CBTLV3125NSR	CBTLV3125
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBTLV3125DBQR	CL125
	TSSOP − PW	Tape and reel	SN74CBTLV3125PWR	CL125
	TVSOP − DGV	Tape and reel	SN74CBTLV3125DGVR	CL125

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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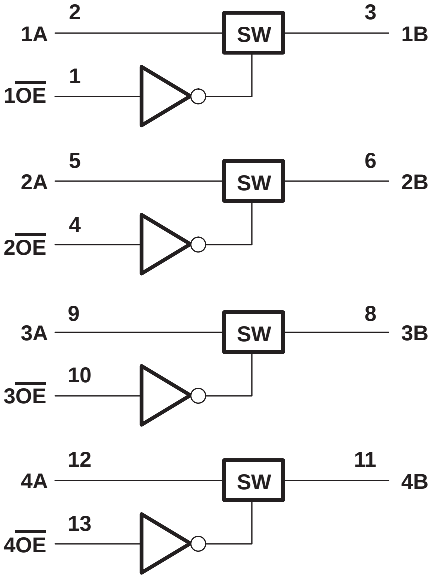
FUNCTION TABLE
(each bus switch)

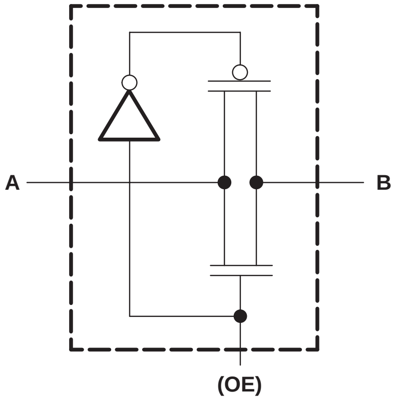
INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)


1A
2
SW
3
1B
1$\overline{OE}$
1
2A
5
SW
6
2B
2$\overline{OE}$
4
3A
9
SW
8
3B
3$\overline{OE}$
10
4A
12
SW
11
4B
4$\overline{OE}$
13

Pin numbers shown are for the D, DGV, NS, PW, and RGY packages.

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)		−0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0)		−50 mA
Package thermal impedance, θ_{JA}	(see Note 2): D package	86°C/W
	(see Note 2): DBQ package	90°C/W
	(see Note 2): DGV package	127°C/W
	(see Note 2): NS package	76°C/W
	(see Note 2): PW package	113°C/W
	(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	$V_I = V_{CC}$ or GND				±1	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	µA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	$V_I = V_{CC}$ or GND			10	µA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	µA
C_i	Control inputs	V_I = 3 V or 0				2.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE} = V_{CC}$			7		pF
r_{on}[§]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V,	I_I = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

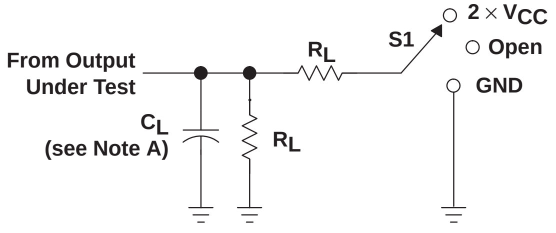
[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	2	4.6	2	4.4	ns
t_{dis}	$\overline{OE}$	A or B	1.1	3.9	1	4.2	ns

[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

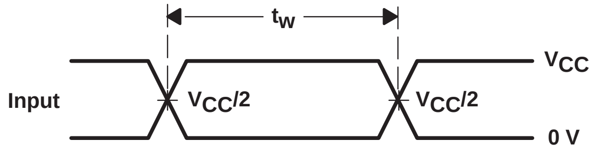
PARAMETER MEASUREMENT INFORMATION


From Output Under Test
C_L (see Note A)
R_L
R_L
S1
$2 \times V_{CC}$
Open
GND

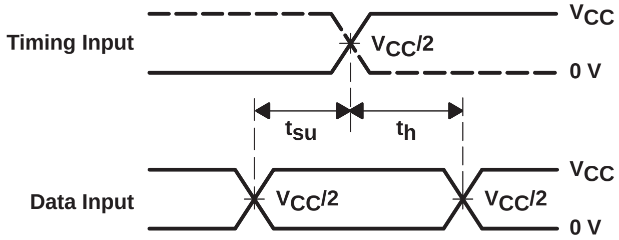
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

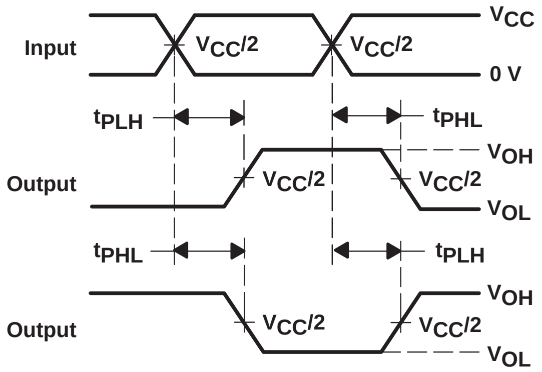
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

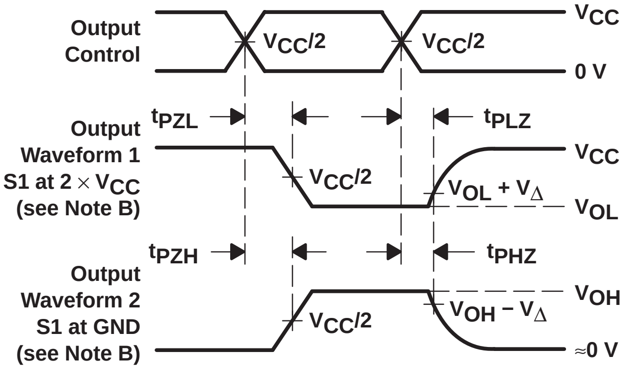
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
V_{CC}
$V_{CC}/2$
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at $2 \times V_{CC}$ (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

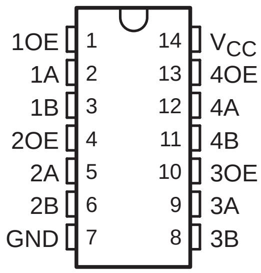
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTLV3126
LOW-VOLTAGE QUADRUPLE FET BUS SWITCH

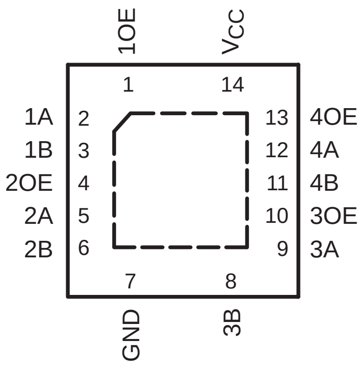
SCDS038I − DECEMBER 1997 − REVISED OCTOBER 2003

- **Standard ’126-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-up Performance Exceeds 100 mA per JESD 78, Class II**

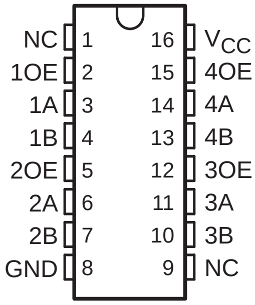
D, DGV, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



DBQ PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The SN74CBTLV3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBTLV3126RGYR	CL126
	SOIC − D	Tube	SN74CBTLV3126D	CBTLV3126
		Tape and reel	SN74CBTLV3126DR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBTLV3126DBQR	CL126
	TSSOP − PW	Tape and reel	SN74CBTLV3126PWR	CL126
	TVSOP − DGV	Tape and reel	SN74CBTLV3126DGVR	CL126

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each bus switch)

INPUT OE	FUNCTION
L	Disconnect
H	A port = B port

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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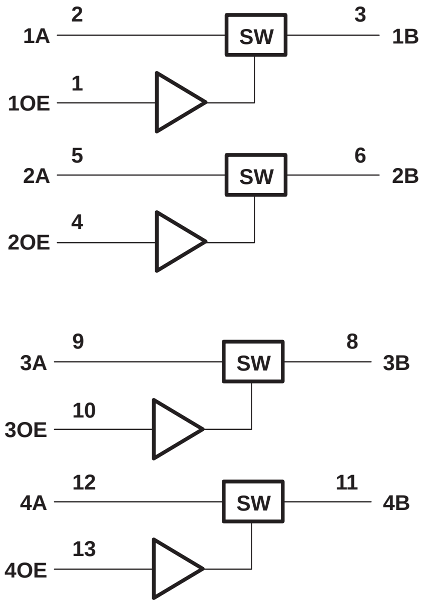
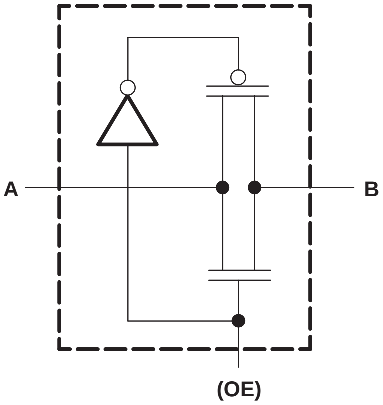
TEXAS INSTRUMENTS

logic diagram (positive logic)


2
1A
SW
3
1B
1
1OE
5
2A
SW
6
2B
4
2OE
9
3A
SW
8
3B
10
3OE
12
4A
SW
11
4B
13
4OE

Pin numbers shown are for the D, DGV, PW, and RGY packages.

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)		−0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0)		−50 mA
Package thermal impedance, θ_{JA}	(see Note 2): D package	86°C/W
	(see Note 2): DBQ package	90°C/W
	(see Note 2): DGV package	127°C/W
	(see Note 2): PW package	113°C/W
	(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	$V_I = V_{CC}$ or GND				±1	μA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	μA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	$V_I = V_{CC}$ or GND			10	μA
ΔI_{CC}§	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
C_i	Control inputs	V_I = 3 V or 0				2.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	OE = GND			7		pF
r_{on}¶		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V,	I_I = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

‡ All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

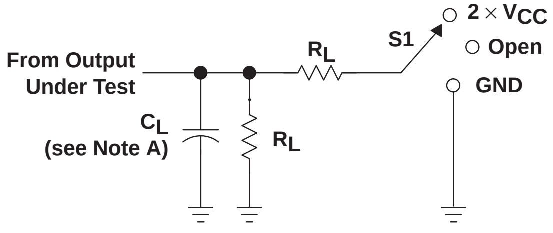
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.15		0.25	ns
t_{en}	OE	A or B	1.6	4.5	1.9	4.2	ns
t_{dis}	OE	A or B	1.3	4.7	1	4.8	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

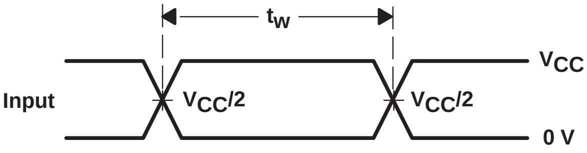
PARAMETER MEASUREMENT INFORMATION


From Output Under Test
C_L (see Note A)
R_L
R_L
S1
$2 \times V_{CC}$
Open
GND

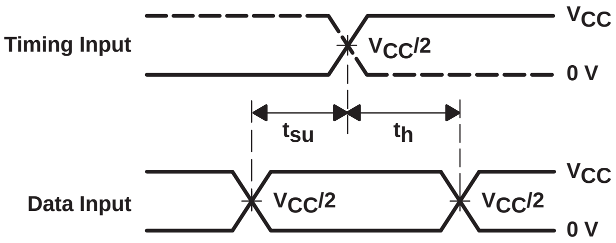
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

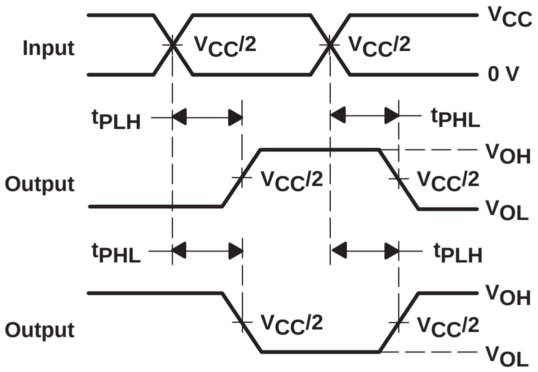
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

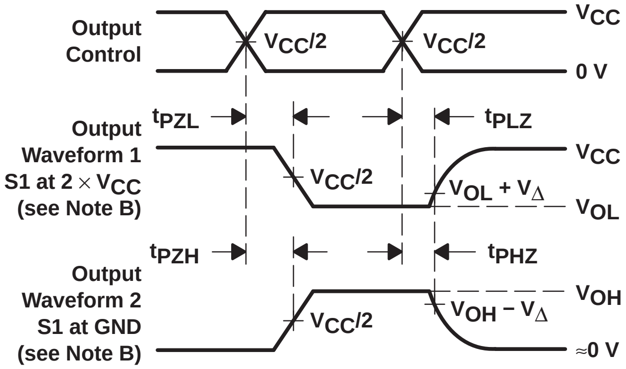
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
V_{CC}
$V_{CC}/2$
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at $2 \times V_{CC}$ (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

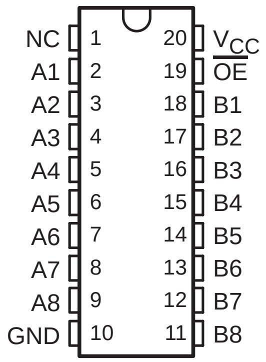
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTLV3245A
LOW-VOLTAGE OCTAL FET BUS SWITCH

SCDS034L − JULY 1997 − REVISED OCTOBER 2003

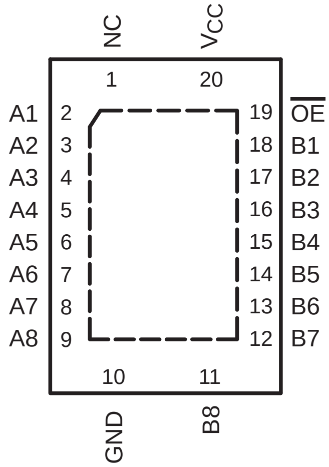
- **Standard ’245-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

RGY PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The SN74CBTLV3245A provides eight bits of high-speed bus switching in a standard ’245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 8-bit switch. When output enable ($\overline{OE}$) is low, the 8-bit bus switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBTLV3245ARGYR	CL245A
	SOIC − DW	Tube	SN74CBTLV3245ADW	CBTLV3245A
		Tape and reel	SN74CBTLV3245ADWR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBTLV3245ADBQR	CBTLV3245A
	TSSOP − PW	Tape and reel	SN74CBTLV3245APWR	CL245A
	TVSOP − DGV	Tape and reel	SN74CBTLV3245ADGVR	CL245A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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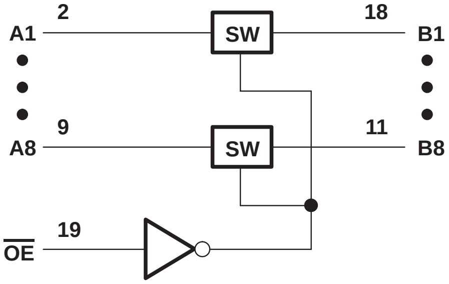
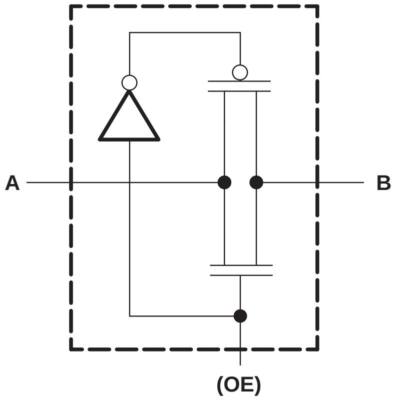
FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	−0.5 V to 4.6 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBQ package	68°C/W
(see Note 2): DGV package	92°C/W
(see Note 2): DW package	58°C/W
(see Note 2): PW package	83°C/W
(see Note 3): RGY package	37°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
	Data inputs						−0.8	
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±60	μA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				40	μA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			20	μA
ΔI_{CC}‡	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
C_i	Control inputs	V_I = 3 V or 0				4		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			9		pF
r_{on}§		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_O = 64 mA		5	8	Ω
				I_O = 24 mA		5	8	
			V_I = 1.7 V,	I_O = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_O = 64 mA		5	7	
				I_O = 24 mA		5	7	
			V_I = 2.4 V,	I_O = 15 mA		10	15	

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

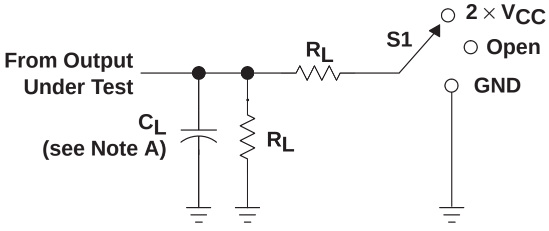
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	6	1	4.7	ns
t_{dis}	$\overline{OE}$	A or B	1	6.1	1	6.4	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

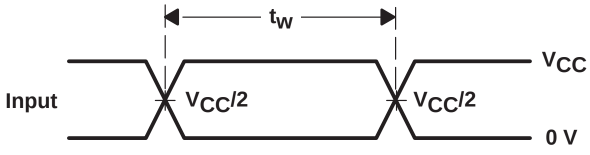
PARAMETER MEASUREMENT INFORMATION


From Output Under Test
C_L (see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

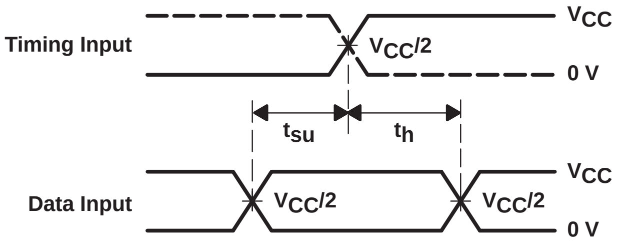
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

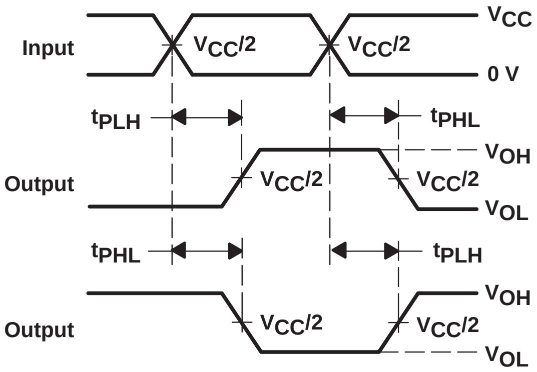
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

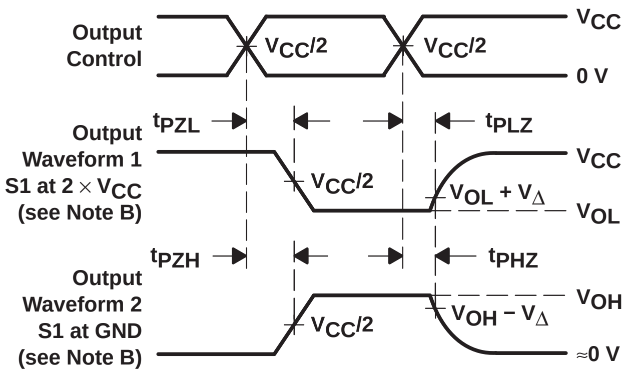
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
V_{CC}
$V_{CC}/2$
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

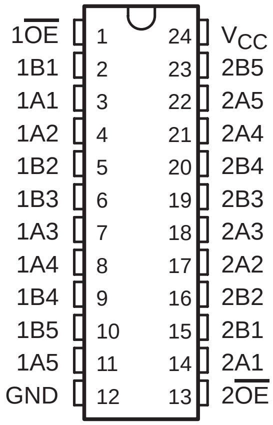
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2$ ns, $t_f \le 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBTLV3384 provides ten bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 5-bit bus switches with separate output-enable ($\overline{OE}$) inputs. It can be used as two 5-bit bus switches or one 10-bit bus switch. When $\overline{OE}$ is low, the associated 5-bit bus switch is on and A port is connected to B port. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QSOP − DBQ	Tape and reel	SN74CBTLV3384DBQR	CL384
	SOIC − DW	Tube	SN74CBTLV3384DW	CBTLV3384
		Tape and reel	SN74CBTLV3384DWR	
	TSSOP − PW	Tape and reel	SN74CBTLV3384PWR	CL384
	TVSOP − DGV	Tape and reel	SN74CBTLV3384DGVR	CL384

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 5-bit bus switch)

INPUTS		INPUTS/OUTPUTS	
$1\overline{OE}$	**$2\overline{OE}$**	**1B1−1B5**	**2B1−2B5**
L	L	1A1−1A5	2A1−2A5
L	H	1A1−1A5	Z
H	L	Z	2A1−2A5
H	H	Z	Z

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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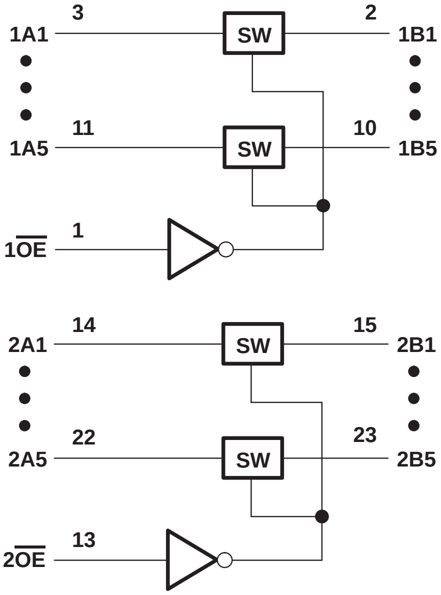
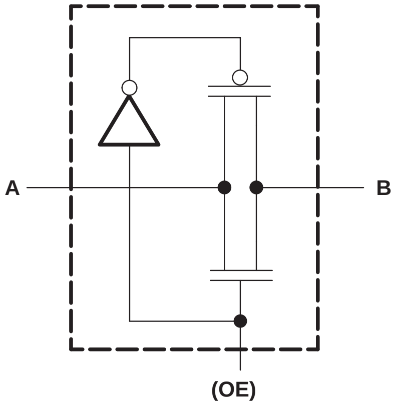
logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)		−0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	μA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	μA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			10	μA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
C_i	Control inputs	V_I = 3 V or 0				4.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			10		pF
r_{on}[§]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V,	I_I = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

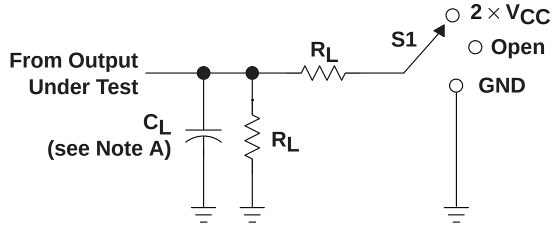
[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	5	1	4.3	ns
t_{dis}	$\overline{OE}$	A or B	1	5.5	1	5.5	ns

[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

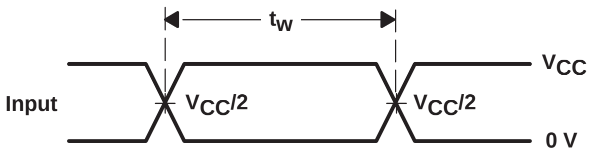
PARAMETER MEASUREMENT INFORMATION


From Output Under Test
C_L (see Note A)
R_L
R_L
S1
$2 \times V_{CC}$
Open
GND

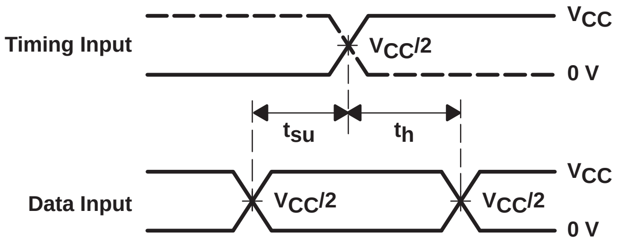
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

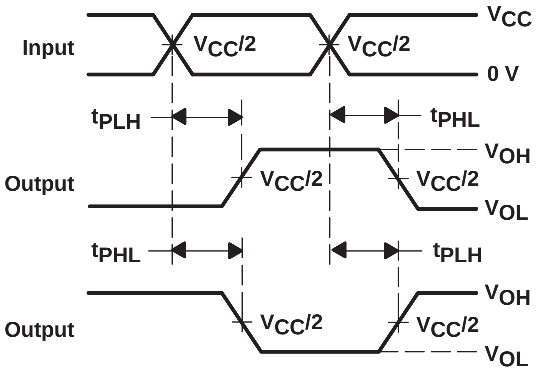
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

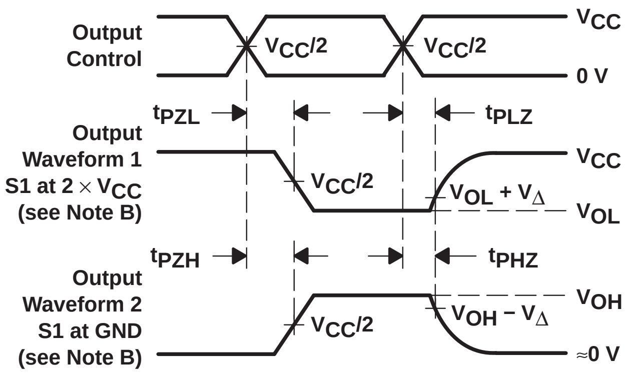
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
V_{CC}
$V_{CC}/2$
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at $2 \times V_{CC}$ (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2$ ns, $t_f \le 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

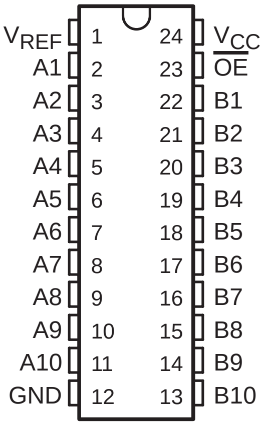
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTLV3857
LOW-VOLTAGE 10-BIT FET BUS SWITCH WITH INTERNAL PULLDOWN RESISTORS

SCDS085E − OCTOBER 1998 − REVISED OCTOBER 2003

- **Enable Signal Is SSTL_2 Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Designed for Use With 200 Mbit/s Double Data-Rate (DDR) SDRAM Applications**
- **Switch On-State Resistance Is Designed to Eliminate Series Resistor to DDR SDRAM**
- **Internal 10-kΩ Pulldown Resistors to Ground on B Port**
- **Internal 50-kΩ Pullup Resistor on Output-Enable Input**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

This 10-bit FET bus switch is designed for 3-V to 3.6-V V_{CC} operation and SSTL_2 output-enable ($\overline{\text{OE}}$) input levels.

When $\overline{\text{OE}}$ is low, the 10-bit bus switch is on, and port A is connected to port B. When $\overline{\text{OE}}$ is high, the switch is open, and the high-impedance state exists between the two ports. There are 10-kΩ pulldown resistors to ground on the B port.

The FET switch on-state resistance is designed to replace the series terminating resistor in the SSTL_2 data path.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QSOP − DBQ	Tape and reel	SN74CBTLV3857DBQR	CL857
	SOIC − DW	Tube	SN74CBTLV3857DW	CBTLV3857
		Tape and reel	SN74CBTLV3857DWR	
	TSSOP − PW	Tape and reel	SN74CBTLV3857PWR	CL857
	TVSOP − DGV	Tape and reel	SN74CBTLV3857DGVR	CL857

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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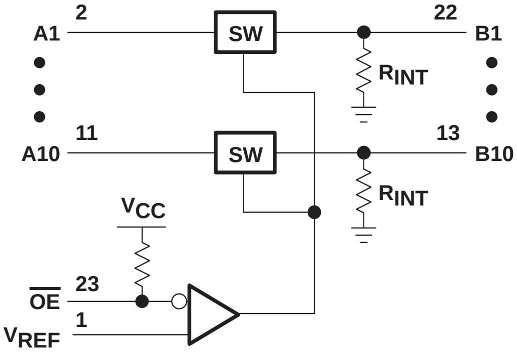
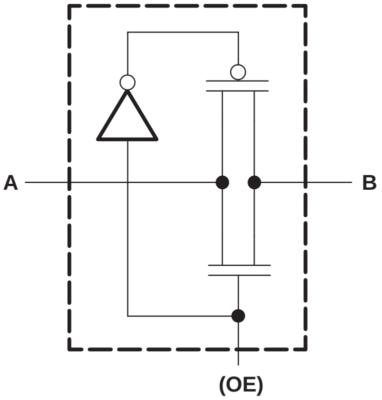
logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Input voltage range ($\overline{OE}$ only), V_I (see Note 1)		−0.5 V to V_{CC} + 0.5 V
Input voltage range (except $\overline{OE}$), V_I (see Note 1)		−0.5 V to 4.6 V
Continuous channel current		48 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{REF}	Reference voltage (0.38 × V_{CC})	1.15	1.25	1.35	V
V_{IH}	AC high-level control input voltage	V_{REF} + 350 mV			V
V_{IL}	AC low-level control input voltage			V_{REF} − 350 mV	V
V_{IH}	DC high-level control input voltage	V_{REF} + 180 mV			V
V_{IL}	DC low-level control input voltage			V_{REF} − 180 mV	V
T_A	Operating free-air temperature	−40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I	$\overline{OE}$	V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	mA
	A port						±5	µA
	B port						±1	mA
	V_{REF}						±5	µA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			25	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5		pF
r_{on}[‡]		V_{CC} = 3 V	V_I = 0,	I_I = 24 mA		5	8	Ω
			V_I = 0.9 V,	I_I = 24 mA		6	11	
			V_I = 1.25 V,	I_I = 24 mA		7	13	
			V_I = 1.6 V,	I_I = 24 mA		9	40	
r_{off}[‡]		V_{CC} = 0			1			MΩ
		V_{CC} = 3 V to 3.6 V,	V_I = 1.65 V,	$\overline{OE}$ = V_{CC}	1			

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

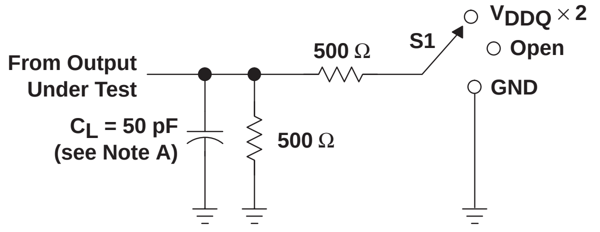
[‡] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. Resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	
t_{pd}[§]	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B	1.4	4.2	ns
t_{dis}	$\overline{OE}$	A or B	1.4	4.8	ns

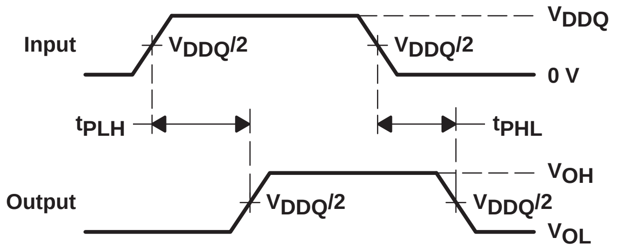
[§] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3 V ± 0.3 V AND V_{DDQ} = 2.5 ± 0.2 V

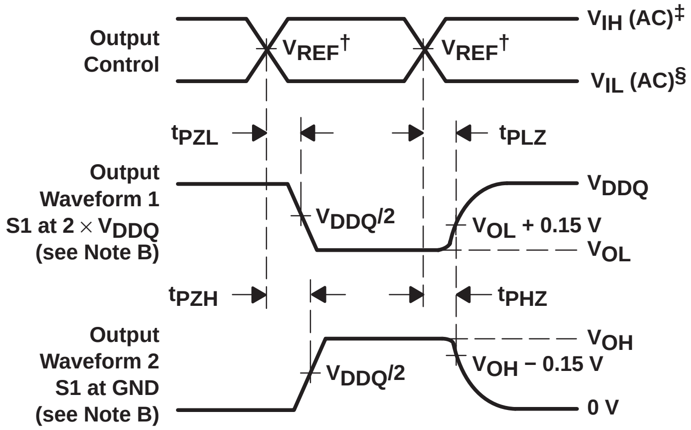

From Output
Under Test
C_L = 50 pF
(see Note A)
500 Ω
500 Ω
S1
$V_{DDQ} \times 2$
Open
GND

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$V_{DDQ} \times 2$
t_{PHZ}/t_{PZH}	GND


Input
$V_{DDQ}/2$
$V_{DDQ}/2$
V_{DDQ}
0 V
t_{PLH}
t_{PHL}
Output
$V_{DDQ}/2$
$V_{DDQ}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES


Output
Control
V_{REF}†
V_{REF}†
V_{IH} (AC)‡
V_{IL} (AC)§
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 2 × V_{DDQ}
(see Note B)
$V_{DDQ}/2$
V_{DDQ}
V_{OL} + 0.15 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at GND
(see Note B)
$V_{DDQ}/2$
V_{OH}
V_{OH} − 0.15 V
0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

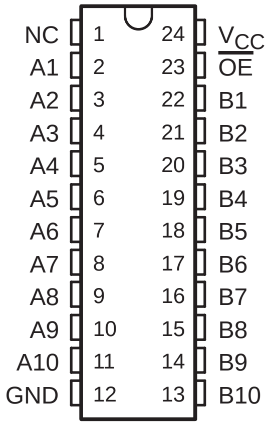
† $V_{REF} = 0.38 \times V_{CC}$
‡ $V_{IH}(AC) = V_{REF}$ + 350 mV
§ $V_{IL}(AC) = V_{REF}$ − 350 mV

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DBQ, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The SN74CBTLV3861 provides ten bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 10-bit bus switch. When output enable ($\overline{OE}$) is low, the 10-bit bus switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QSOP − DBQ	Tape and reel	SN74CBTLV3861DBQR	CL861
	SOIC − DW	Tube	SN74CBTLV3861DW	CBTLV3861
		Tape and reel	SN74CBTLV3861DWR	
	SOP − NS	Tape and reel	SN74CBTLV3861NSR	CBTLV3861
	TSSOP − PW	Tape and reel	SN74CBTLV3861PWR	CL861
	TVSOP − DGV	Tape and reel	SN74CBTLV3861DGVR	CL861

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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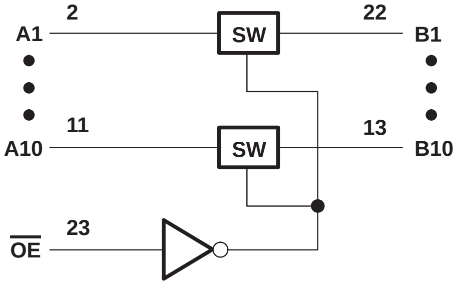
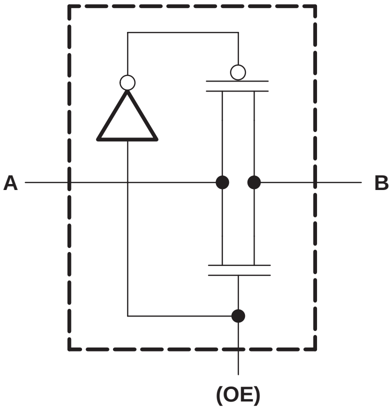
logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)		−0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	NS package	65°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	μA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	μA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			10	μA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5		pF
r_{on}[§]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V,	I_I = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

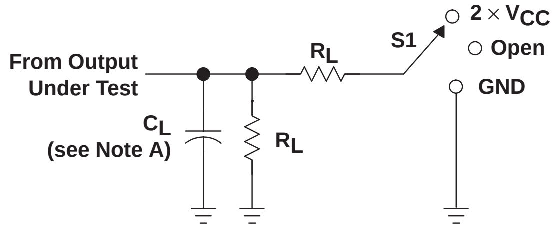
[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	2.1	5.5	2.1	4.9	ns
t_{dis}	$\overline{OE}$	A or B	1.7	5.5	2.5	5.8	ns

[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

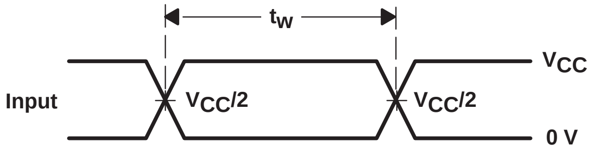
PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
C_L
(see Note A)
R_L
R_L
S1
$2 \times V_{CC}$
Open
GND

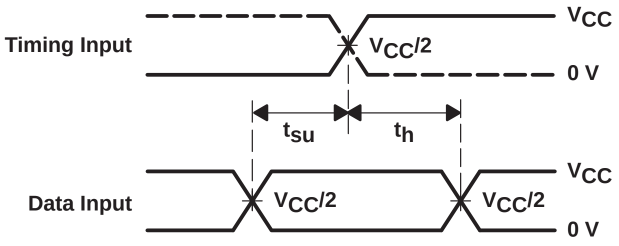
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

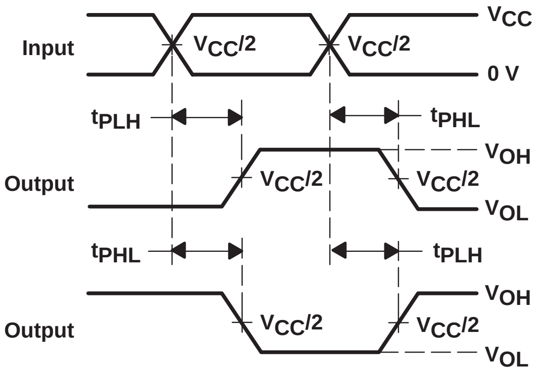
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

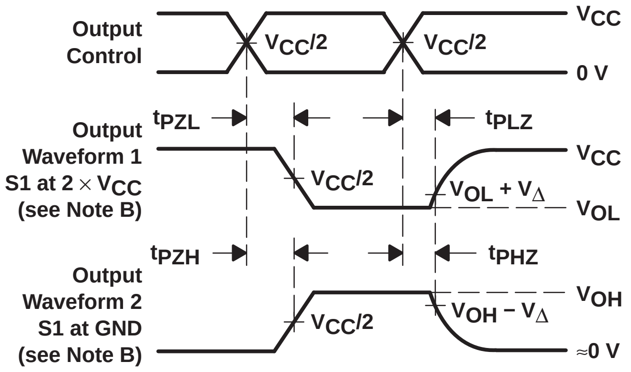
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
$V_{CC}/2$
V_{CC}
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output
Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at $2 \times V_{CC}$
(see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at GND
(see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

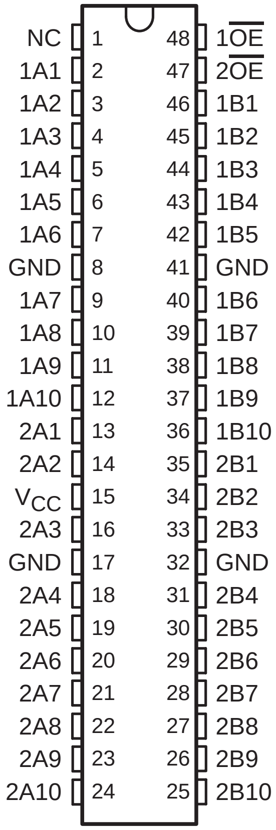
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTLV16210
LOW-VOLTAGE 20-BIT FET BUS SWITCH

SCDS042I − DECEMBER 1997 − REVISED OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1 48 1$\overline{\text{OE}}$
1A1 2 47 2$\overline{\text{OE}}$
1A2 3 46 1B1
1A3 4 45 1B2
1A4 5 44 1B3
1A5 6 43 1B4
1A6 7 42 1B5
GND 8 41 GND
1A7 9 40 1B6
1A8 10 39 1B7
1A9 11 38 1B8
1A10 12 37 1B9
2A1 13 36 1B10
2A2 14 35 2B1
V_{CC} 15 34 2B2
2A3 16 33 2B3
GND 17 32 GND
2A4 18 31 2B4
2A5 19 30 2B5
2A6 20 29 2B6
2A7 21 28 2B7
2A8 22 27 2B8
2A9 23 26 2B9
2A10 24 25 2B10

NC − No internal connection

description/ordering information

The SN74CBTLV16210 provides 20 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 10-bit bus switches with separate output-enable ($\overline{\text{OE}}$) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When $\overline{\text{OE}}$ is low, the associated 10-bit bus switch is on, and port A is connected to port B. When $\overline{\text{OE}}$ is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBTLV16210DL	CBTLV16210
		Tape and reel	SN74CBTLV16210DLR	
	TSSOP − DGG	Tape and reel	SN74CBTLV16210GR	CBTLV16210
	TVSOP − DGV	Tape and reel	SN74CBTLV16210VR	CN210

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 10-bit bus switch)

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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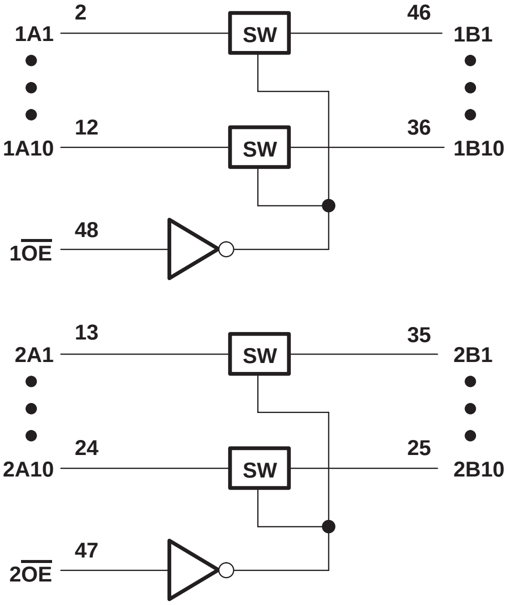
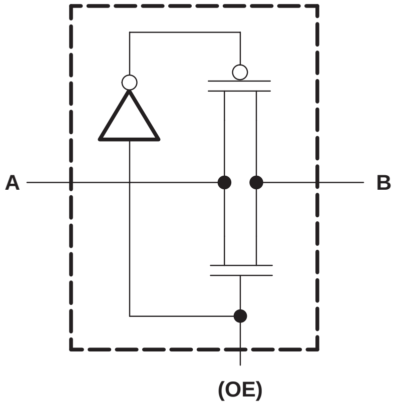
logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)		−0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	$V_I = V_{CC}$ or GND				±1	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	µA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	$V_I = V_{CC}$ or GND			10	µA
ΔI_{CC}‡	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	µA
C_i	Control inputs	V_I = 3 V or 0				4.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE} = V_{CC}$			6.5		pF
r_{on}§		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V,	I_I = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

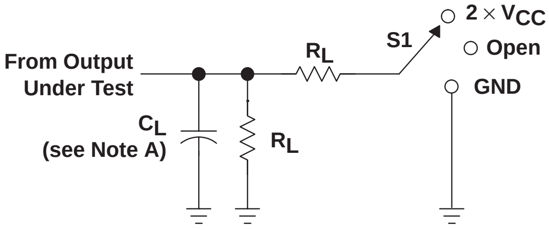
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	6.8	1	6	ns
t_{dis}	$\overline{OE}$	A or B	1	7.3	1	7.4	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

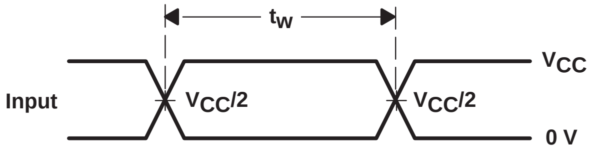
PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

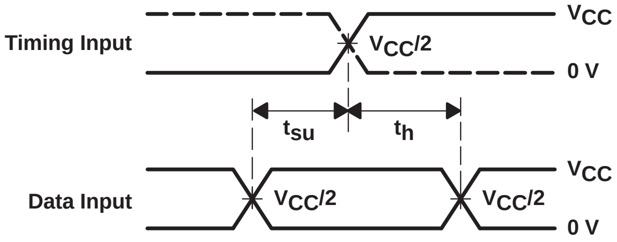
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

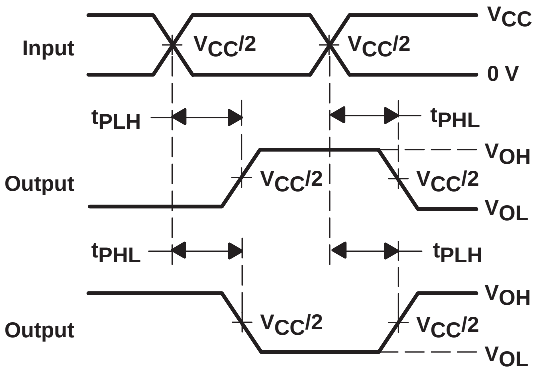
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

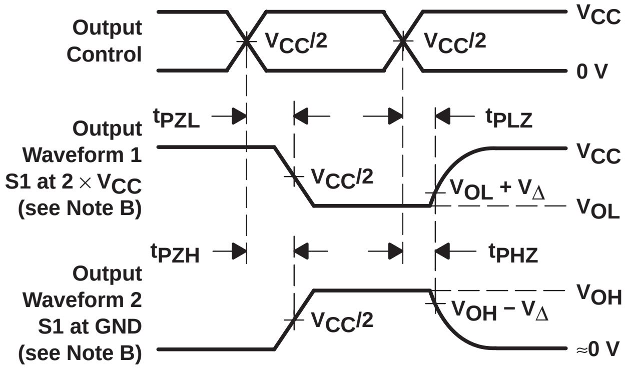
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
V_{CC}
$V_{CC}/2$
0 V
t_{su}
t_h
Data Input
V_{CC}
$V_{CC}/2$
$V_{CC}/2$
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
V_{CC}
$V_{CC}/2$
$V_{CC}/2$
0 V
t_{PLH}
t_{PHL}
Output
V_{OH}
$V_{CC}/2$
$V_{CC}/2$
V_{OL}
t_{PHL}
t_{PLH}
Output
V_{OH}
$V_{CC}/2$
$V_{CC}/2$
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output
Control
V_{CC}
$V_{CC}/2$
$V_{CC}/2$
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 2 × V_{CC}
(see Note B)
V_{CC}
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at GND
(see Note B)
V_{OH}
$V_{OH} - V_\Delta$
$V_{CC}/2$
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2$ ns, $t_f \le 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

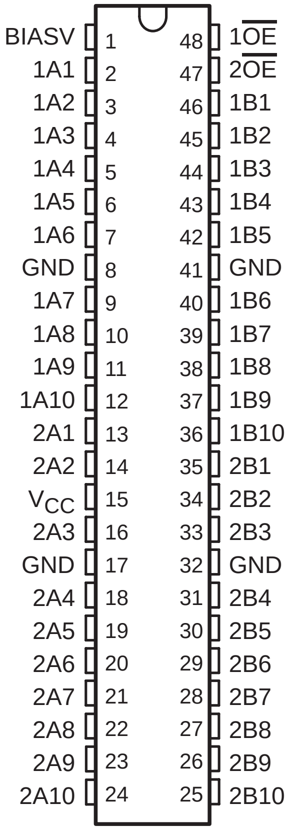
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTLV16800
LOW-VOLTAGE 20-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS

SCDS045J − DECEMBER 1997 − REVISED OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **B-Port Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


BIASV 1
1A1 2
1A2 3
1A3 4
1A4 5
1A5 6
1A6 7
GND 8
1A7 9
1A8 10
1A9 11
1A10 12
2A1 13
2A2 14
V_{CC} 15
2A3 16
GND 17
2A4 18
2A5 19
2A6 20
2A7 21
2A8 22
2A9 23
2A10 24
48 1$\overline{OE}$
47 2$\overline{OE}$
46 1B1
45 1B2
44 1B3
43 1B4
42 1B5
41 GND
40 1B6
39 1B7
38 1B8
37 1B9
36 1B10
35 2B1
34 2B2
33 2B3
32 GND
31 2B4
30 2B5
29 2B6
28 2B7
27 2B8
26 2B9
25 2B10

description/ordering information

The SN74CBTLV16800 provides 20 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The device is organized as dual 10-bit bus switches with separate output-enable ($\overline{OE}$) inputs. It can be used as two 10-bit bus switches or one 20-bit bus switch. When $\overline{OE}$ is low, the associated 10-bit bus switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, the high-impedance state exists between the two ports, and port B is precharged to BIASV through the equivalent of a 10-kΩ resistor.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBTLV16800DL	CBTLV16800
		Tape and reel	SN74CBTLV16800DLR	
−40°C to 85°C	TSSOP − DGG	Tape and reel	SN74CBTLV16800GR	CBTLV16800
	TVSOP − DGV	Tape and reel	SN74CBTLV16800VR	CN800

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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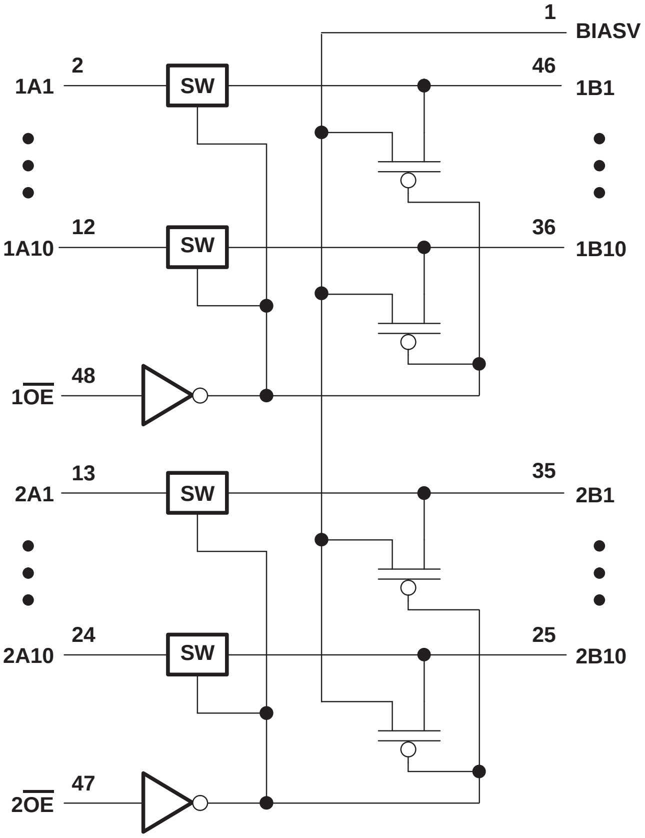
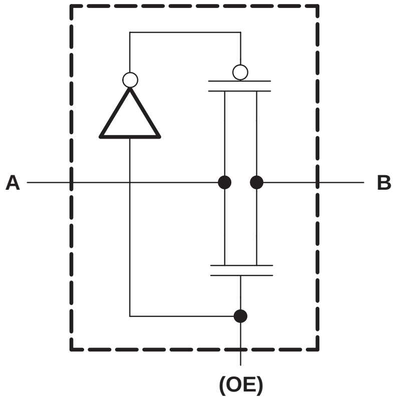
FUNCTION TABLE
(each 10-bit bus switch)

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV

logic diagram (positive logic)


1
BIASV
2
1A1
SW
46
1B1
12
1A10
SW
36
1B10
48
1$\overline{\text{OE}}$
13
2A1
SW
35
2B1
24
2A10
SW
25
2B10
47
2$\overline{\text{OE}}$

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Bias voltage range, BIASV		−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)		−0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
BIASV	Bias voltage		1.3	V_{CC}	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA					−1.2	V
I_I		V_{CC} = 3.6 V,	$V_I = V_{CC}$ or GND					±1	μA
I_{off}	A port	V_{CC} = 0,	V_I or V_O = 0 to 3.6 V					10	μA
I_O		V_{CC} = 3 V,	BIASV = 2.4 V,	V_O= 0,	$\overline{OE} = V_{CC}$		0.25		mA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	$V_I = V_{CC}$ or GND				10	μA
ΔI_{CC}§	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND				300	μA
C_i	Control inputs	V_I = 3 V or 0					4.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	Switch off,	BIASV = Open			6.5		pF
r_{on}¶		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA			5	9	Ω
				I_I = 24 mA			5	9	
			V_I = 1.7 V,	I_I = 15 mA			25	35	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA			5	7	
				I_I = 24 mA			5	7	
			V_I = 2.4 V,	I_I = 15 mA			8	15	

‡ All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

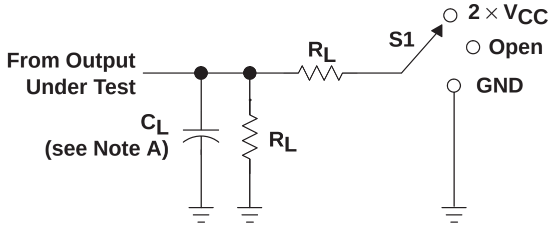
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V MIN	V_{CC} = 2.5 V ± 0.2 V MAX	V_{CC} = 3.3 V ± 0.3 V MIN	V_{CC} = 3.3 V ± 0.3 V MAX	UNIT
t_{pd}[†]		A or B	B or A		0.15		0.25	ns
t_{PZH}	BIASV = GND	$\overline{OE}$	A or B	2.9	7.7	2.2	5.5	ns
t_{PZL}	BIASV = 3 V			2.8	6.4	2.1	5.3	
t_{PHZ}	BIASV = GND	$\overline{OE}$	A or B	1.4	6.8	2.6	7.6	ns
t_{PLZ}	BIASV = 3 V			1.3	4.2	1.5	5.1	

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

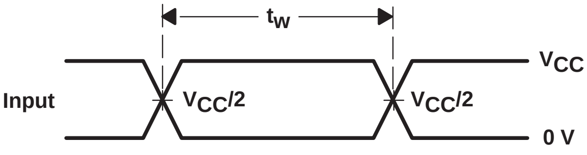
PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
C_L
(see Note A)
R_L
R_L
S1
$2 \times V_{CC}$
Open
GND

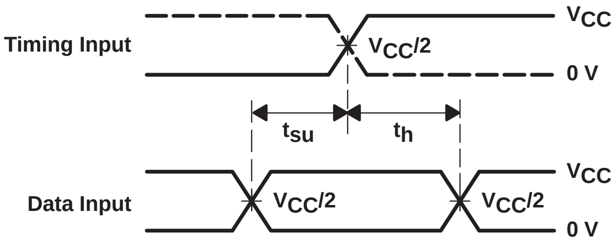
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

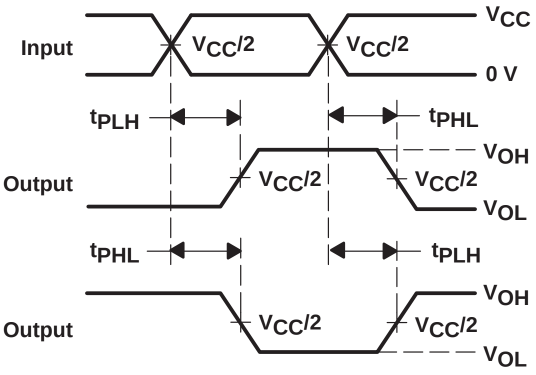
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

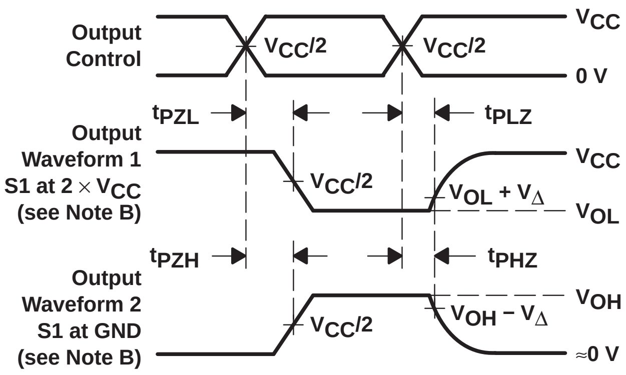
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
$V_{CC}/2$
V_{CC}
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output
Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at $2 \times V_{CC}$
(see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at GND
(see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

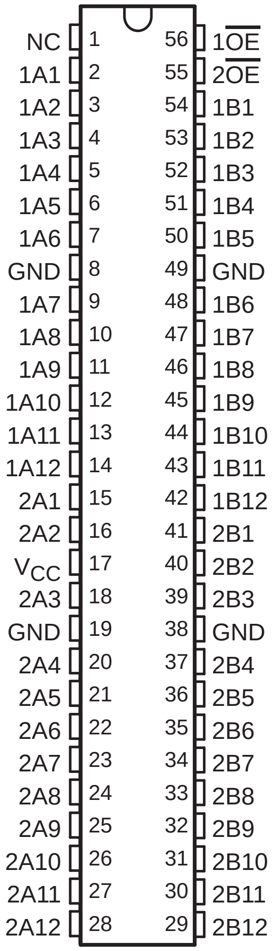
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTLV16211
LOW-VOLTAGE 24-BIT FET BUS SWITCH

SCDS043I − DECEMBER 1997 − REVISED OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **− 2000-V Human-Body Model (A114-A)**
  - **− 200-V Machine Model (A115-A)**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


NC 1
1A1 2
1A2 3
1A3 4
1A4 5
1A5 6
1A6 7
GND 8
1A7 9
1A8 10
1A9 11
1A10 12
1A11 13
1A12 14
2A1 15
2A2 16
V_{CC} 17
2A3 18
GND 19
2A4 20
2A5 21
2A6 22
2A7 23
2A8 24
2A9 25
2A10 26
2A11 27
2A12 28
56 $1\overline{\text{OE}}$
55 $2\overline{\text{OE}}$
54 1B1
53 1B2
52 1B3
51 1B4
50 1B5
49 GND
48 1B6
47 1B7
46 1B8
45 1B9
44 1B10
43 1B11
42 1B12
41 2B1
40 2B2
39 2B3
38 GND
37 2B4
36 2B5
35 2B6
34 2B7
33 2B8
32 2B9
31 2B10
30 2B11
29 2B12

NC − No internal connection

description/ordering information

The SN74CBTLV16211 provides 24 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 12-bit bus switches with separate output-enable ($\overline{\text{OE}}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When $\overline{\text{OE}}$ is low, the associated 12-bit bus switch is on, and port A is connected to port B. When $\overline{\text{OE}}$ is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBTLV16211DL	CBTLV16211
		Tape and reel	SN74CBTLV16211DLR	
	TSSOP − DGG	Tape and reel	SN74CBTLV16211GR	CBTLV16211
	TVSOP − DGV	Tape and reel	SN74CBTLV16211VR	CN211

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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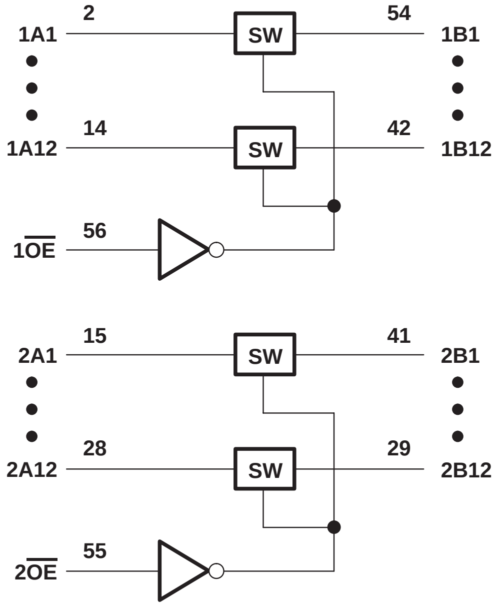
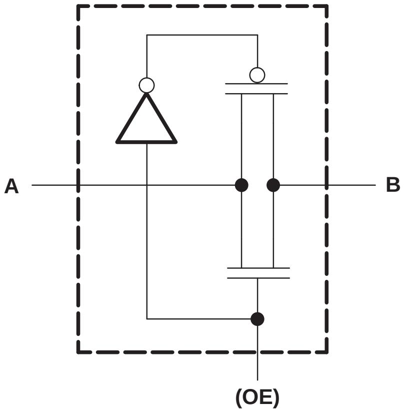
FUNCTION TABLE
(each 12-bit bus switch)

INPUT $\overline{\text{OE}}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)


1A1
2
54
1B1
SW
1A12
14
42
1B12
SW
1$\overline{\text{OE}}$
56
2A1
15
41
2B1
SW
2A12
28
29
2B12
SW
2$\overline{\text{OE}}$
55

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to 4.6 V
Continuous channel current . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . 64°C/W
DGV package . . . . 48°C/W
DL package . . . . 56°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	$V_I = V_{CC}$ or GND				±1	μA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	μA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	$V_I = V_{CC}$ or GND			10	μA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
C_i	Control inputs	V_I = 3.3 V or 0				4.5		pF
$C_{io(OFF)}$		V_O = 3.3 V or 0,	$\overline{\text{OE}} = V_{CC}$			6.5		pF
r_{on}[§]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V,	I_I = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

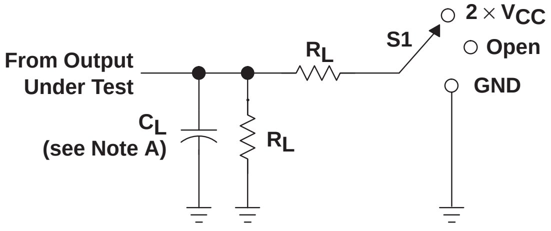
[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{\text{OE}}$	A or B	1	7	1	6.2	ns
t_{dis}	$\overline{\text{OE}}$	A or B	1	7.2	1	7.7	ns

[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

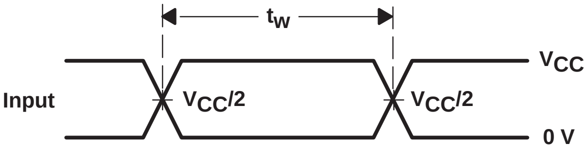
PARAMETER MEASUREMENT INFORMATION


From Output Under Test
C_L (see Note A)
R_L
R_L
S1
$2 \times V_{CC}$
Open
GND

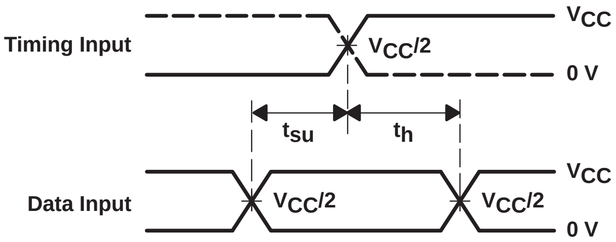
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

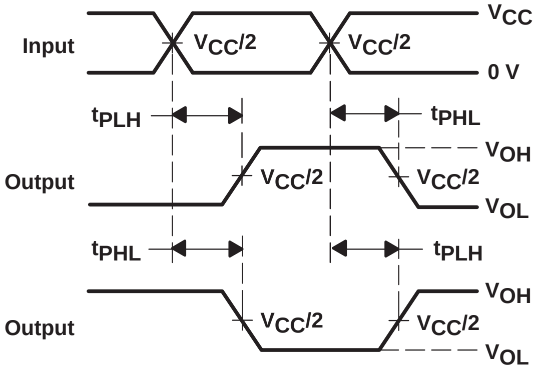
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

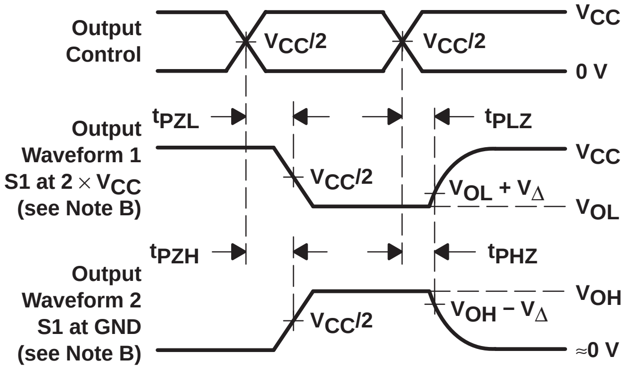
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
V_{CC}
$V_{CC}/2$
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at $2 \times V_{CC}$ (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2$ ns, $t_f \le 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

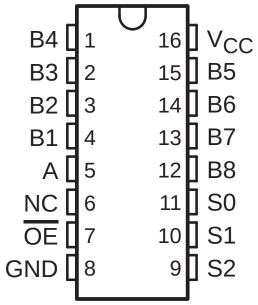
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTLV3251
LOW-VOLTAGE 1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER

SCDS054I − MARCH 1998 − REVISED OCTOBER 2003

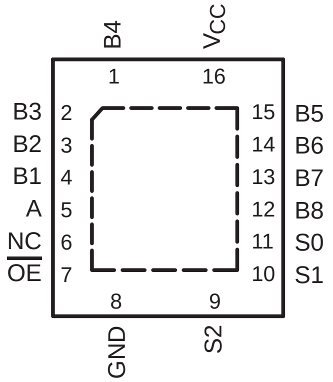
- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

D, DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

RGY PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The SN74CBTLV3251 device is a 1-of-8 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The select inputs (S0, S1, S2) control the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable ($\overline{OE}$) input is high.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBTLV3251RGYR	CL251
	SOIC − D	Tube	SN74CBTLV3251D	CBTLV3251
		Tape and reel	SN74CBTLV3251DR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBTLV3251DBQR	CL251
	TSSOP − PW	Tape and reel	SN74CBTLV3251PWR	CL251
	TVSOP − DGV	Tape and reel	SN74CBTLV3251DGVR	CL251

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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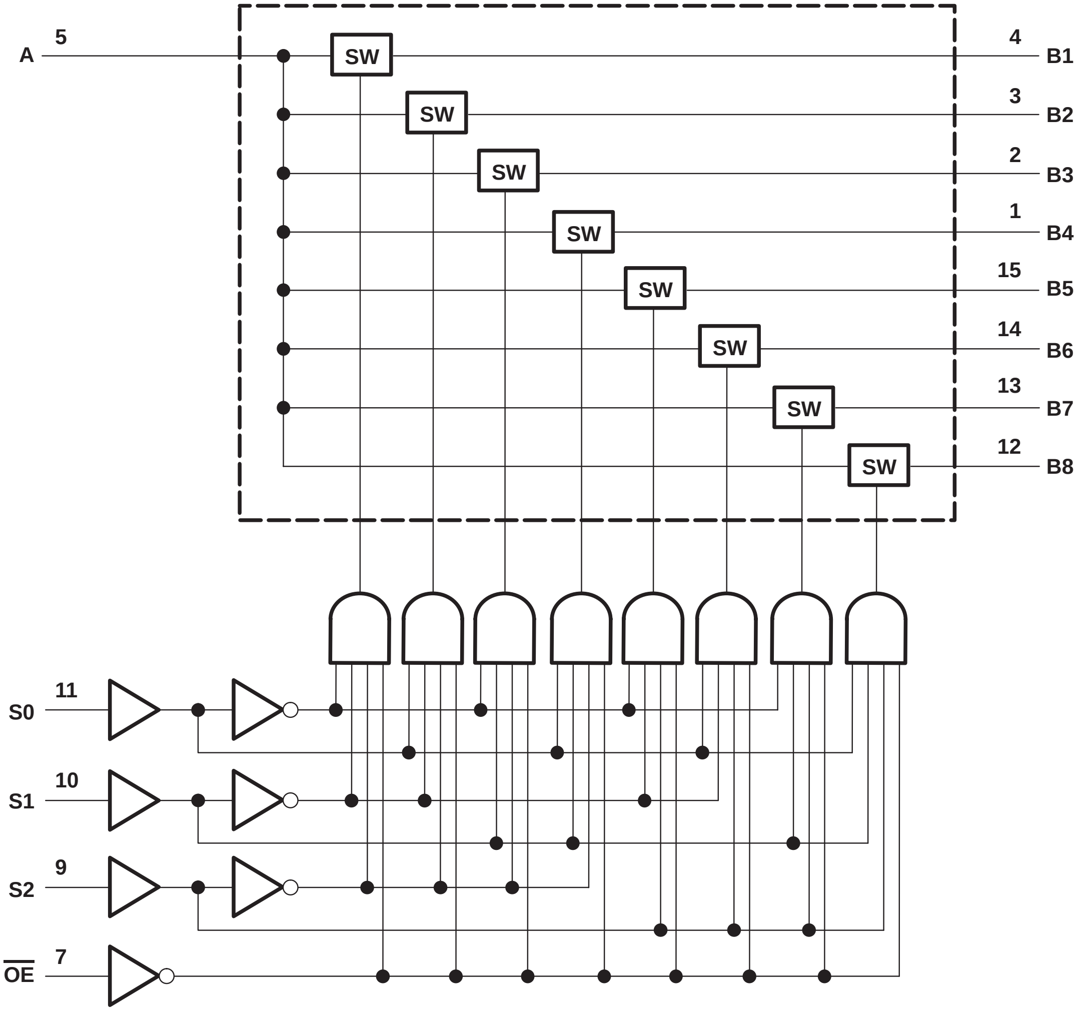
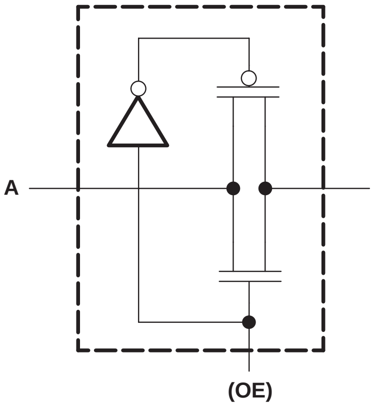
FUNCTION TABLE

INPUTS				FUNCTION
$\overline{OE}$	S2	S1	S0	
L	L	L	L	A port = B1 port
L	L	L	H	A port = B2 port
L	L	H	L	A port = B3 port
L	L	H	H	A port = B4 port
L	H	L	L	A port = B5 port
L	H	L	H	A port = B6 port
L	H	H	L	A port = B7 port
L	H	H	H	A port = B8 port
H	X	X	X	Disconnect

logic diagram (positive logic)


A
5
SW
SW
SW
SW
SW
SW
SW
SW
4
B1
3
B2
2
B3
1
B4
15
B5
14
B6
13
B7
12
B8
S0
11
S1
10
S2
9
$\overline{OE}$
7

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)		−0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_K ($V_{I/O}$ < 0)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	D package	73°C/W
(see Note 2):	DBQ package	90°C/W
(see Note 2):	DGV package	120°C/W
(see Note 2):	PW package	108°C/W
(see Note 3):	RGY package	39°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	μA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				20	μA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			10	μA
ΔI_{CC}‡	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			40.5		pF
	B port					6		
r_{on}§		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V,	I_I = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

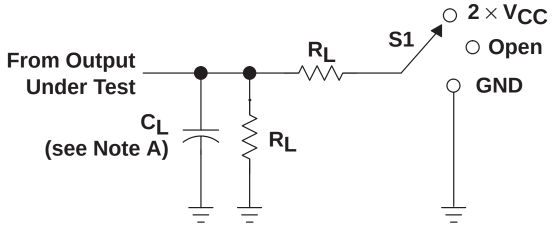
§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B¶	B or A		0.15		0.25	ns
	S	A	1	6.1	1	5.3	
t_{en}	S	B	1	4.1	1	3.6	ns
t_{dis}	S	B	1	3.5	1	3.3	ns
t_{en}	$\overline{OE}$	A or B	1	5.2	1	4.5	ns
t_{dis}	$\overline{OE}$	A or B	1	6.7	1	7.2	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

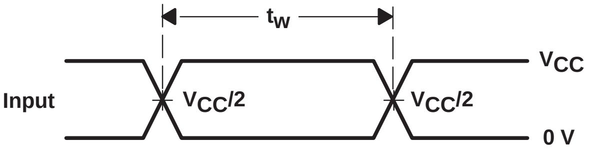
PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

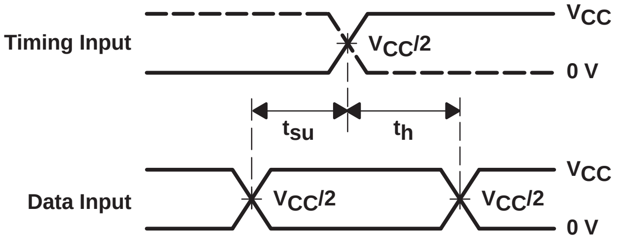
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

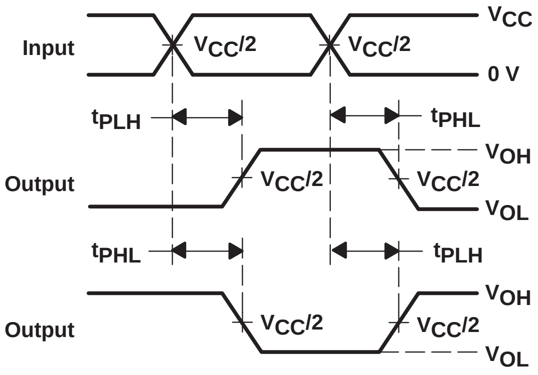
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

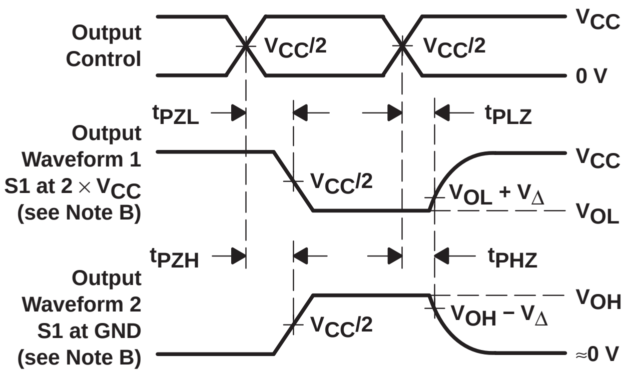
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
V_{CC}
$V_{CC}/2$
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output
Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 2 × V_{CC}
(see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at GND
(see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

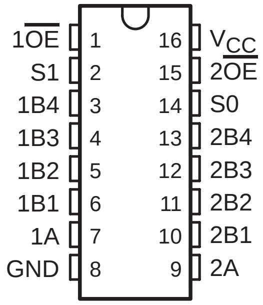
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTLV3253
LOW-VOLTAGE DUAL 1-OF-4 FET MULTIPLEXER/DEMULTIPLEXER

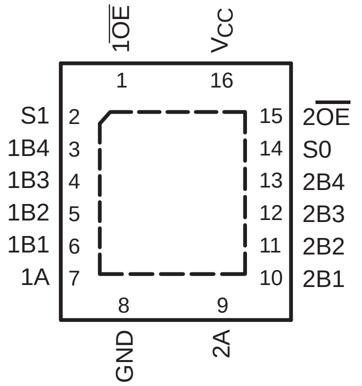
SCDS039H − DECEMBER 1997 − REVISED OCTOBER 2003

- **Functionally Equivalent to QS3253**
- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

D, DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBTLV3253 is a dual 1-of-4 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The select (S0, S1) inputs control the data flow. The FET multiplexers/demultiplexers are disabled when the associated output-enable ($\overline{OE}$) input is high.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBTLV3253RGYR	CL253
	SOIC − D	Tube	SN74CBTLV3253D	CBTLV3253
		Tape and reel	SN74CBTLV3253DR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBTLV3253DBQR	CL253
	TSSOP − PW	Tape and reel	SN74CBTLV3253PWR	CL253
	TVSOP − DGV	Tape and reel	SN74CBTLV3253DGVR	CL253

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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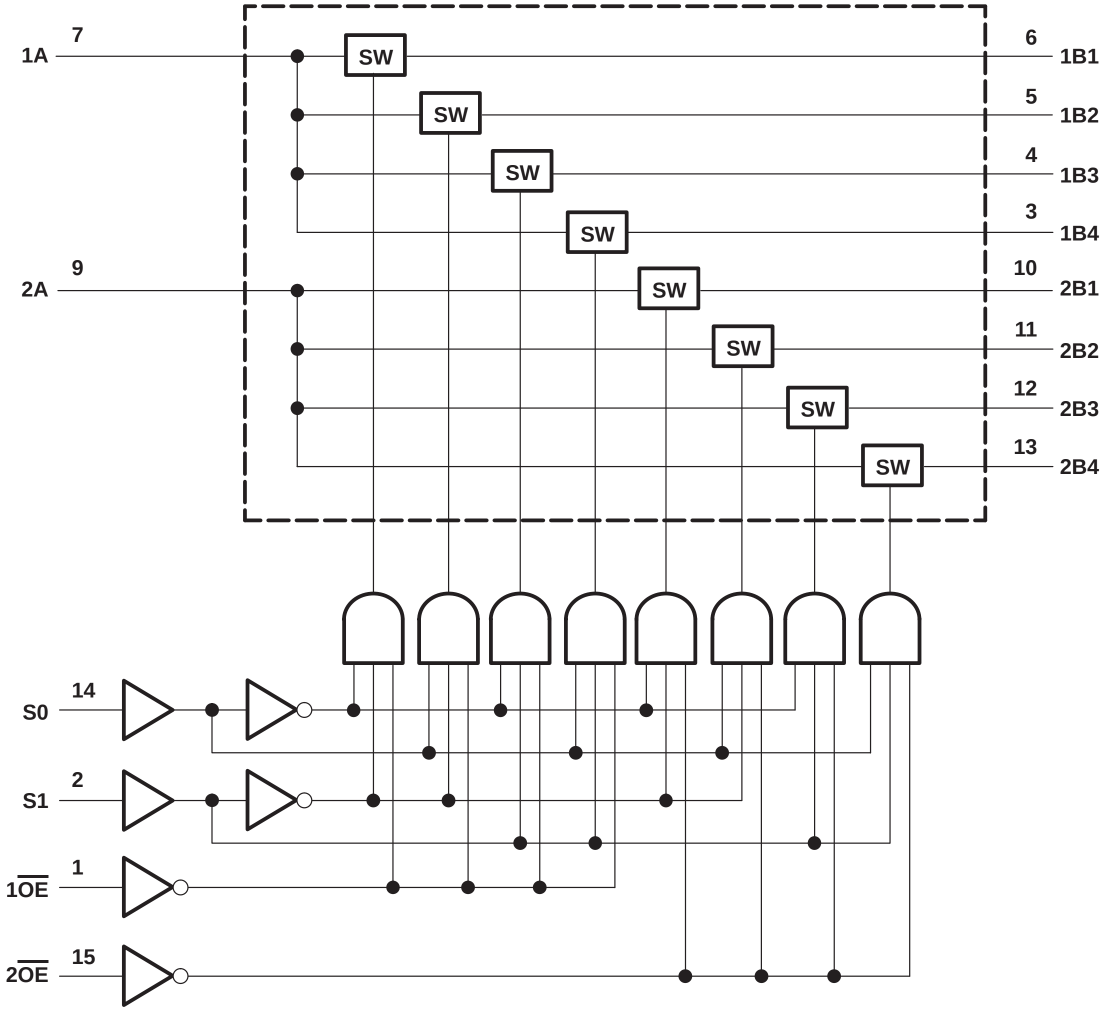
TEXAS INSTRUMENTS

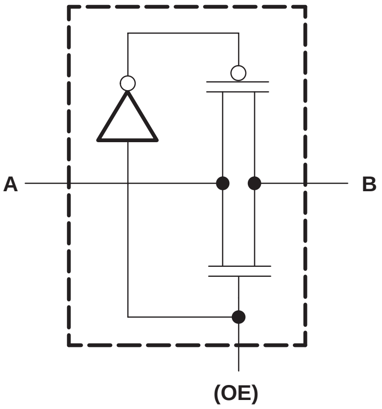
FUNCTION TABLE
(each multiplexer/demultiplexer)

INPUTS			FUNCTION
$\overline{OE}$	S1	S0	
L	L	L	A port = B1 port
L	L	H	A port = B2 port
L	H	L	A port = B3 port
L	H	H	A port = B4 port
H	X	X	Disconnect

logic diagram (positive logic)


1A
7
2A
9
SW
6
1B1
5
1B2
4
1B3
3
1B4
10
2B1
11
2B2
12
2B3
13
2B4
S0
14
S1
2
1OE
1
2OE
15

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to 4.6 V
Continuous channel current . . . . 128 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0) . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . 73°C/W
(see Note 2): DBQ package . . . . 90°C/W
(see Note 2): DGV package . . . . 120°C/W
(see Note 2): PW package . . . . 108°C/W
(see Note 3): RGY package . . . . 39°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				15	µA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			10	µA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	µA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			20.5		pF
	B port					5.5		
r_{on}[§]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V,	I_I = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

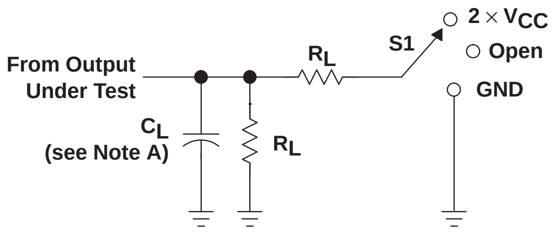
[§] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B[¶]	B or A		0.15		0.25	ns
	S	A or B	1	6.8	1	5.5	
t_{en}	S	A or B	1	4.3	1	4	ns
t_{dis}	S	A or B	1	5.1	1	5.5	ns
t_{en}	$\overline{OE}$	A or B	1	5	1	4.8	ns
t_{dis}	$\overline{OE}$	A or B	1	5.5	1	5.4	ns

[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

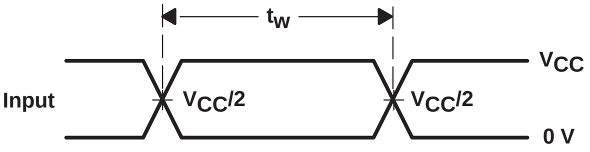
PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
C_L
(see Note A)
R_L
R_L
S1
$2 \times V_{CC}$
Open
GND

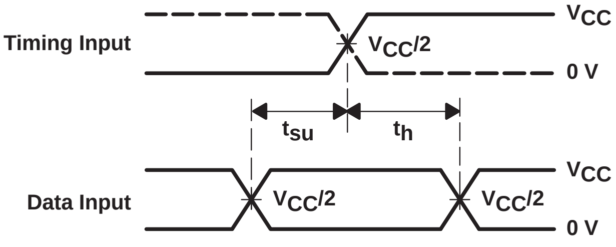
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

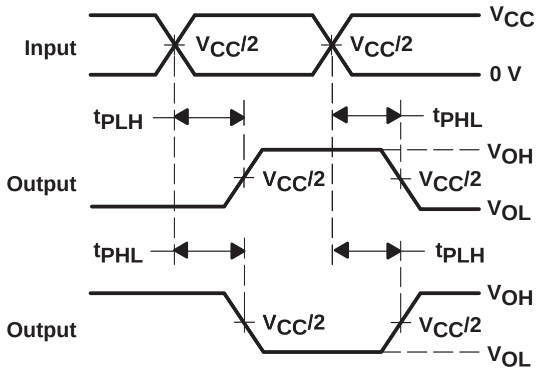
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

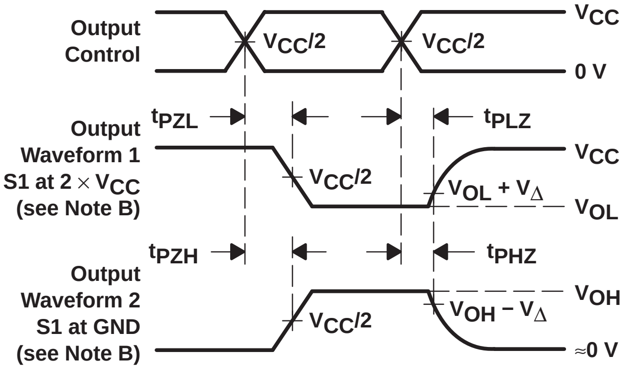
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
V_{CC}
$V_{CC}/2$
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output
Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at $2 \times V_{CC}$
(see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at GND
(see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2$ ns, $t_f \le 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

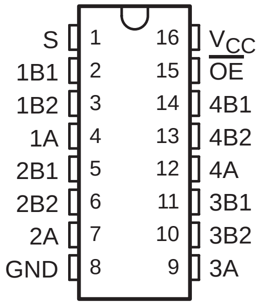
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTLV3257
LOW-VOLTAGE 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

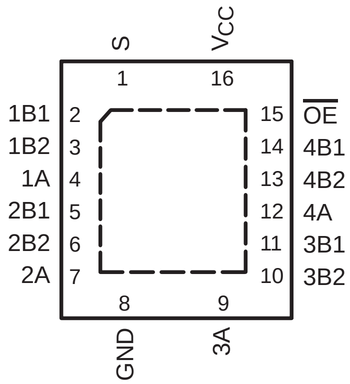
SCDS040I − DECEMBER 1997 − REVISED OCTOBER 2003

- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

D, DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBTLV3257 is a 4-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The select (S) input controls the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable ($\overline{OE}$) input is high.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	SN74CBTLV3257RGYR	CL257
	SOIC − D	Tube	SN74CBTLV3257D	CBTLV3257
		Tape and reel	SN74CBTLV3257DR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74CBTLV3257DBQR	CL257
	TSSOP − PW	Tape and reel	SN74CBTLV3257PWR	CL257
	TVSOP − DGV	Tape and reel	SN74CBTLV3257DGVR	CL257

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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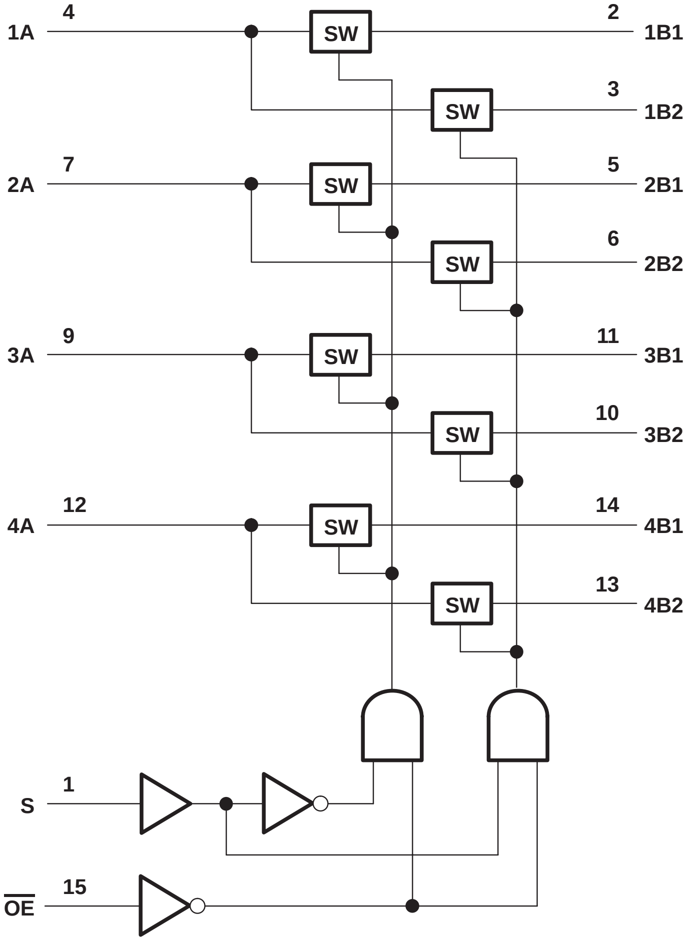
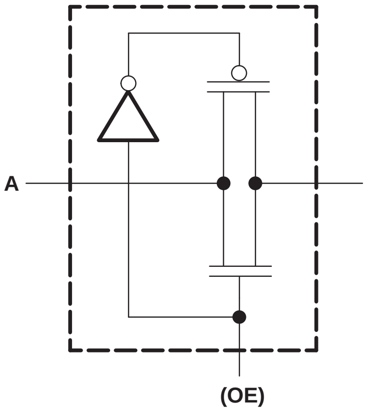
FUNCTION TABLE

INPUTS		FUNCTION
$\overline{OE}$	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

logic diagram (positive logic)


1A
4
SW
2
1B1
SW
3
1B2
2A
7
SW
5
2B1
SW
6
2B2
3A
9
SW
11
3B1
SW
10
3B2
4A
12
SW
14
4B1
SW
13
4B2
S
1
$\overline{OE}$
15

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	−0.5 V to 4.6 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
(see Note 2): DBQ package	90°C/W
(see Note 2): DGV package	120°C/W
(see Note 2): PW package	108°C/W
(see Note 3): RGY package	39°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	$V_I = V_{CC}$ or GND				±1	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				15	µA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	$V_I = V_{CC}$ or GND			10	µA
ΔI_{CC}‡	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	µA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0,	$\overline{OE} = V_{CC}$			10.5		pF
	B port					5.5		
r_{on}§		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V,	I_I = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

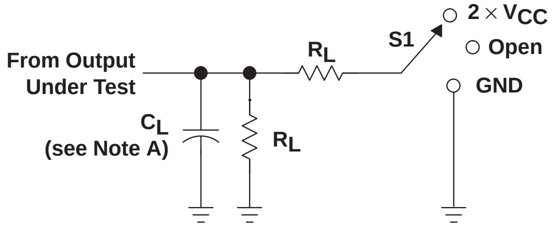
§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B¶	B or A		0.15		0.25	ns
	S	A or B	1.8	6.1	1.8	5.3	
t_{en}	S	A or B	1.7	6.1	1.7	5.3	ns
t_{dis}	S	A or B	1	4.8	1	4.5	ns
t_{en}	$\overline{OE}$	A or B	1.9	5.6	2	5	ns
t_{dis}	$\overline{OE}$	A or B	1	5.5	1.6	5.5	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

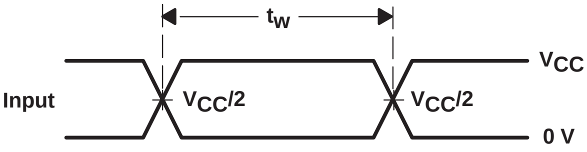
PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

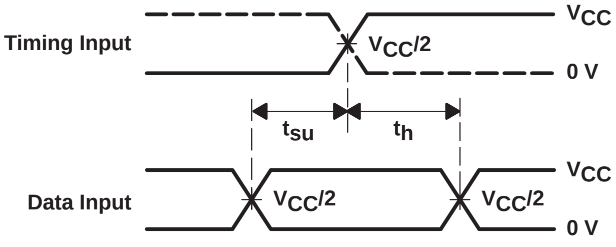
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

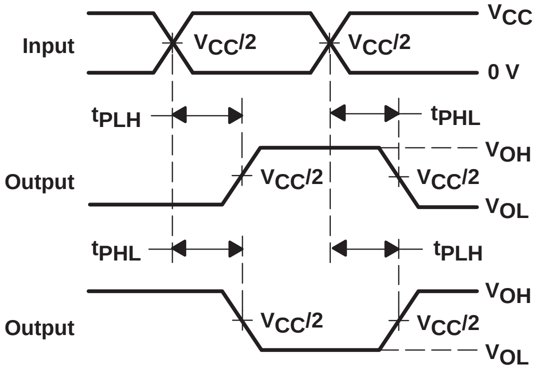
V_{CC}	C_L	R_L	V_Δ
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

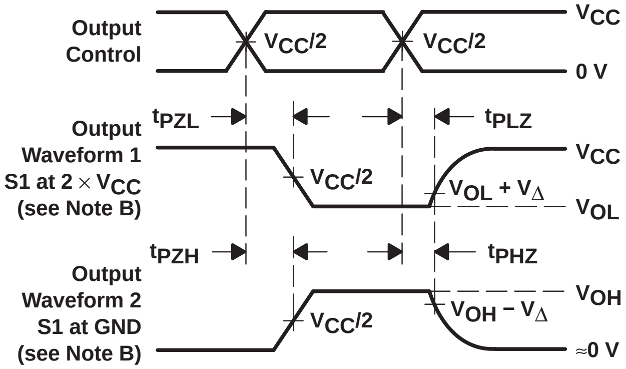
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
$V_{CC}/2$
V_{CC}
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output
Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 2 × V_{CC}
(see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at GND
(see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2$ ns, $t_f \le 2$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

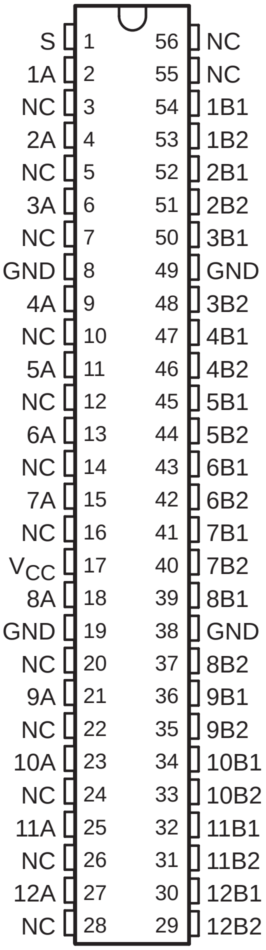
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTLV16292
LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS055K − MARCH 1998 − REVISED OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **4-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Make-Before-Break Feature**
- **Internal 500-Ω Pulldown Resistors to Ground**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


S 1 56 NC
1A 2 55 NC
NC 3 54 1B1
2A 4 53 1B2
NC 5 52 2B1
3A 6 51 2B2
NC 7 50 3B1
GND 8 49 GND
4A 9 48 3B2
NC 10 47 4B1
5A 11 46 4B2
NC 12 45 5B1
6A 13 44 5B2
NC 14 43 6B1
7A 15 42 6B2
NC 16 41 7B1
V_CC 17 40 7B2
8A 18 39 8B1
GND 19 38 GND
NC 20 37 8B2
9A 21 36 9B1
NC 22 35 9B2
10A 23 34 10B1
NC 24 33 10B2
11A 25 32 11B1
NC 26 31 11B2
12A 27 30 12B1
NC 28 29 12B2

NC − No internal connection

description/ordering information

The SN74CBTLV16292 is a 12-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1, and R_{INT} is connected to port B2. When S is high, port A is connected to port B2, and R_{INT} is connected to port B1.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBTLV16292DL	CBTLV16292
		Tape and reel	SN74CBTLV16292DLR	
	TSSOP − DGG	Tape and reel	SN74CBTLV16292GR	CBTLV16292
	TVSOP − DGV	Tape and reel	SN74CBTLV16292VR	CN292

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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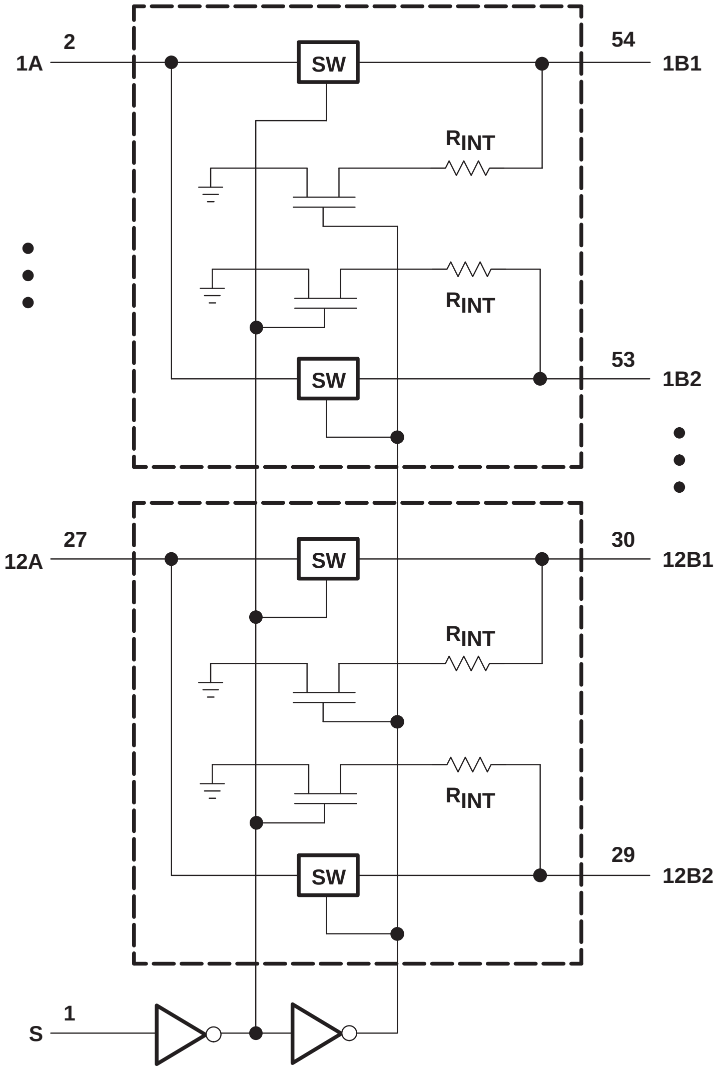
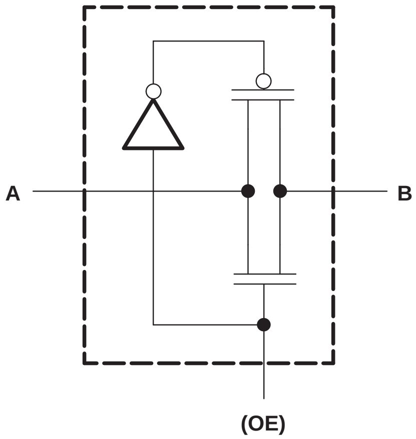
FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port R_{INT} = B2 port
H	A port = B2 port R_{INT} = B1 port

logic diagram (positive logic)


1A
2
54
1B1
SW
RINT
RINT
53
1B2
SW
27
12A
30
12B1
SW
RINT
RINT
29
12B2
SW
S
1

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)		−0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} (V_I < 0)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	µA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			10	µA
ΔI_{CC}[‡]	Control input	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	µA
C_i	Control input	V_I = 3.3 V or 0				3.5		pF
C_{io}	A or B port	V_O = 3.3 V or 0				22.5		pF
r_{on}[§]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V,	I_I = 15 mA		11	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		3	7	
				I_I = 24 mA		3	7	
			V_I = 2.4 V,	I_I = 15 mA		7	15	

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A		0.15		0.25	ns
t_{pd}[#]	S	A	2.5	7.1	2.5	6.7	ns
t_{en}	S	B	1	5.6	1	5	ns
t_{dis}	S	B	1	5	1	4.5	ns

[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

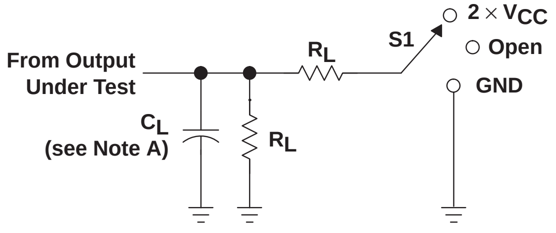
[#] This propagation delay was measured by observing the change of voltage on the A output introduced by static levels equal to 3-V or 0 for 3.3 V ± 0.3 V or V_{CC} or 0 for 2.5 V ± 0.2 V on B1 and B2 to achieve the desired transition.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	DESCRIPTION	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_{mbb}[‖]	Make-before-break time	0	2	0	2	ns

[‖] The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.

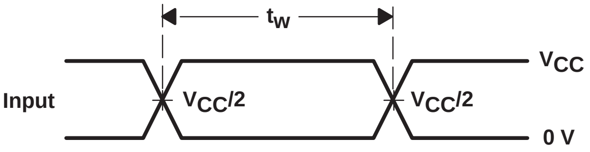
PARAMETER MEASUREMENT INFORMATION


2 × V_{CC}
S1
Open
GND
From Output Under Test
R_L
C_L (see Note A)
R_L

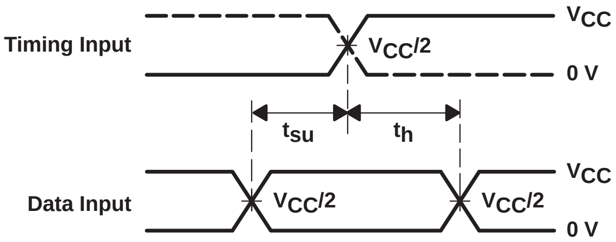
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

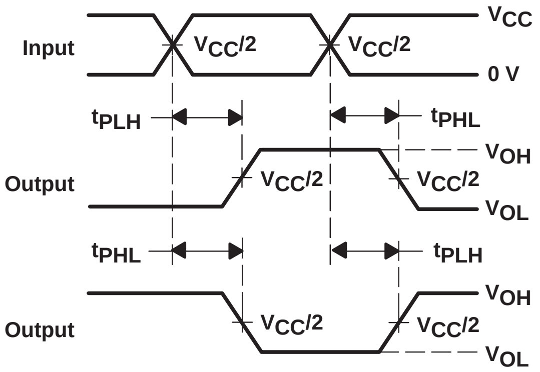
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

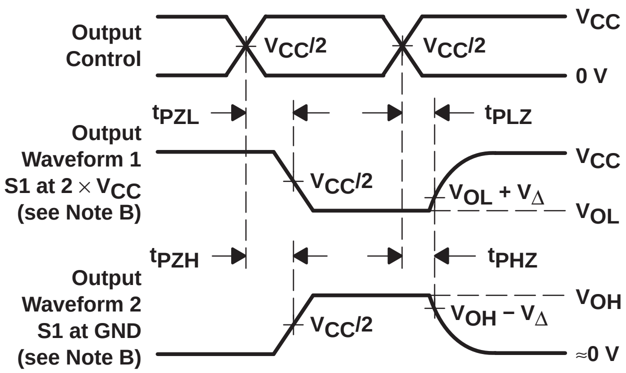
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
$V_{CC}/2$
V_{CC}
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2$ ns, $t_f \le 2$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

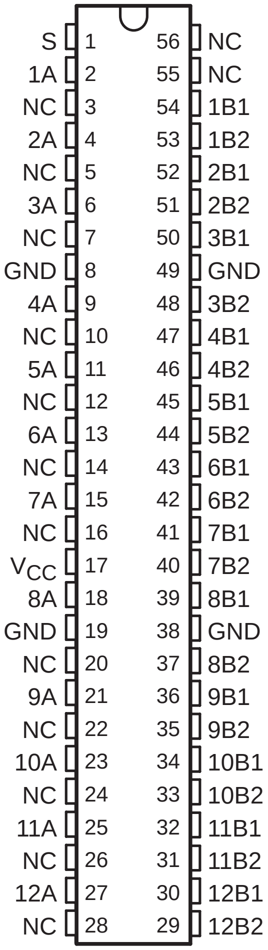
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTLVR16292
LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS056H − MARCH 1998 − REVISED OCTOBER 2003

- **Member of the Texas Instruments Widebus™ Family**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Make-Before-Break Feature**
- **Internal 500-Ω Pulldown Resistors to Ground**
- **Input/Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


S 1 56 NC
1A 2 55 NC
NC 3 54 1B1
2A 4 53 1B2
NC 5 52 2B1
3A 6 51 2B2
NC 7 50 3B1
GND 8 49 GND
4A 9 48 3B2
NC 10 47 4B1
5A 11 46 4B2
NC 12 45 5B1
6A 13 44 5B2
NC 14 43 6B1
7A 15 42 6B2
NC 16 41 7B1
VCC 17 40 7B2
8A 18 39 8B1
GND 19 38 GND
NC 20 37 8B2
9A 21 36 9B1
NC 22 35 9B2
10A 23 34 10B1
NC 24 33 10B2
11A 25 32 11B1
NC 26 31 11B2
12A 27 30 12B1
NC 28 29 12B2

NC − No internal connection

description/ordering information

The SN74CBTLVR16292 is a 12-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1, and R_{INT} is connected to port B2. When S is high, port A is connected to port B2, and R_{INT} is connected to port B1.

The input/output ports include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBTLVR16292L	CBTLVR16292
		Tape and reel	SN74CBTLVR16292LR	
	TSSOP − DGG	Tape and reel	SN74CBTLVR16292GR	CBTLVR16292
	TVSOP − DGV	Tape and reel	SN74CBTLVR16292VR	CE292

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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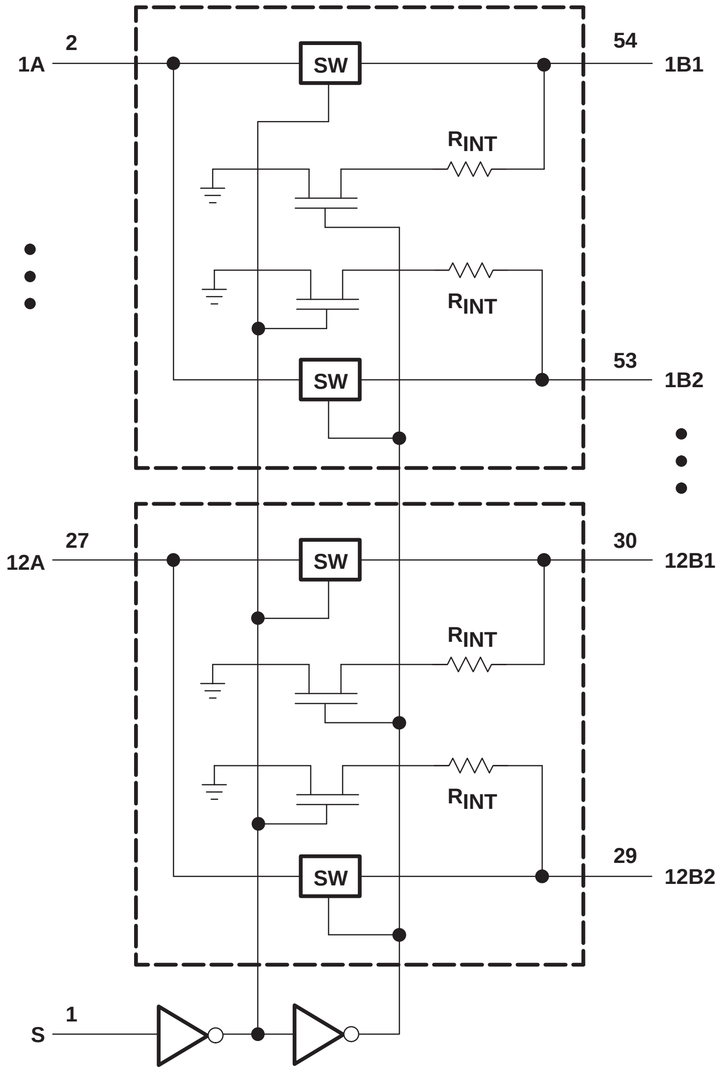
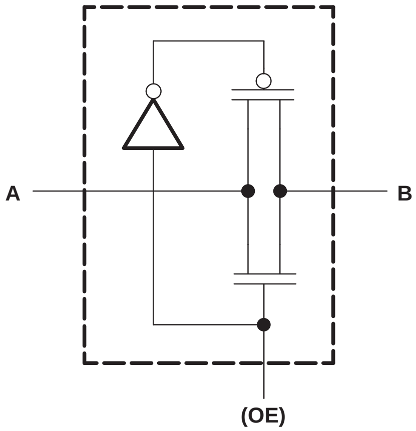
FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port R_{INT} = B2 port
H	A port = B2 port R_{INT} = B1 port

logic diagram (positive logic)


1A
2
SW
54
1B1
RINT
RINT
53
1B2
SW
12A
27
SW
30
12B1
RINT
RINT
29
12B2
SW
S
1

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)		−0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} (V_I < 0)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	μA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	μA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			10	μA
ΔI_{CC}[‡]	Control input	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
C_i	Control input	V_I = 3.3 V or 0				3.5		pF
C_{io}	A or B port	V_O = 3.3 V or 0				23		pF
r_{on}[§]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		30	47	Ω
				I_I = 24 mA		30	47	
			V_I = 1.7 V,	I_I = 15 mA		36	80	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		30	42	
				I_I = 24 mA		30	42	
			V_I = 2.4 V,	I_I = 15 mA		32	47	

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
[‡] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A		0.15		0.25	ns
t_{pd}[#]	S	A	3.2	8.5	3.2	8	ns
t_{en}	S	B	1	6.5	1	5.8	ns
t_{dis}	S	B	1	5.3	1	4.6	ns

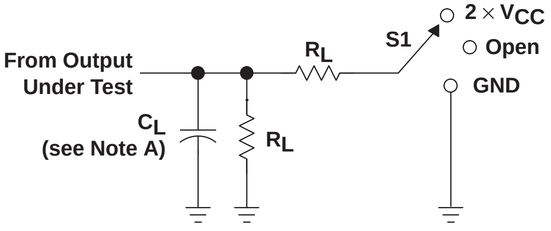
[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
[#] This propagation delay was measured by observing the change of voltage on the A output introduced by static levels equal to 3-V or 0 for 3.3 V ± 0.3 V or V_{CC} or 0 for 2.5 V ± 0.2 V on B1 and B2 to achieve the desired transition.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	DESCRIPTION	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_{mbb}[||]	Make-before-break time	0	2	0	2	ns

[||] The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.

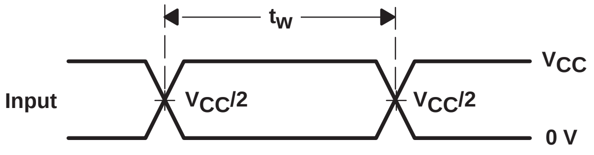
PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
C_L
(see Note A)
R_L
R_L
S1
2 × V_{CC}
Open
GND

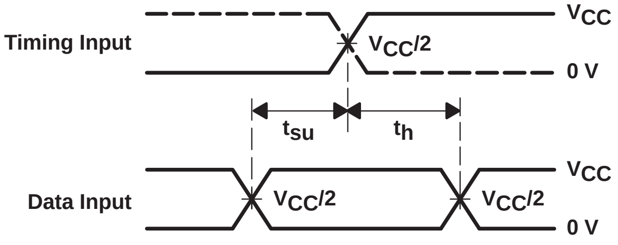
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

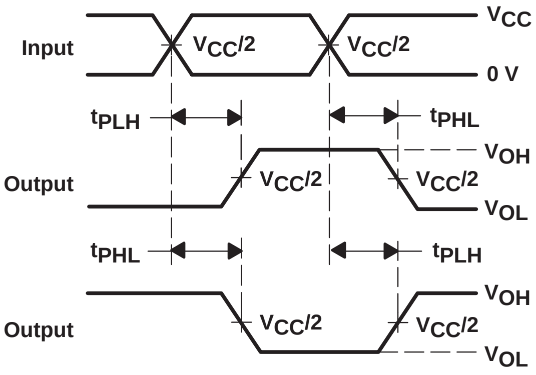
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

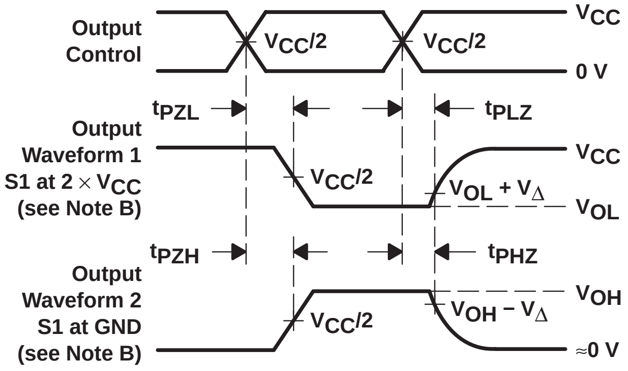
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
$V_{CC}/2$
V_{CC}
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output
Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at 2 × V_{CC}
(see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at GND
(see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

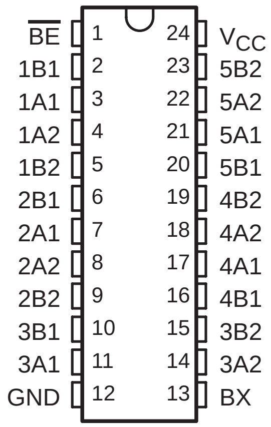
Figure 1. Load Circuit and Voltage Waveforms

SN74CBTLV3383
LOW-VOLTAGE 10-BIT FET BUS-EXCHANGE SWITCH

SCDS047G − MARCH 1998 − REVISED OCTOBER 2003

- **5-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBTLV3383 provides ten bits of high-speed bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 10-bit bus switch or as a 5-bit bus exchanger, which provides swapping of the A and B pairs of signals. The bus-exchange function is selected when BX is high, and $\overline{BE}$ is low.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QSOP − DBQ	Tape and reel	SN74CBTLV3383DBQR	CL383
	SOIC − DW	Tube	SN74CBTLV3383DW	CBTLV3383
		Tape and reel	SN74CBTLV3383DWR	
	TSSOP − PW	Tape and reel	SN74CBTLV3383PWR	CL383
	TVSOP − DGV	Tape and reel	SN74CBTLV3383DGVR	CL383

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{BE}$	BX	1A1−5A1	1A2−5A2
L	L	1B1−5B1	1B2−5B2
L	H	1B2−5B2	1B1−5B1
H	X	Z	Z

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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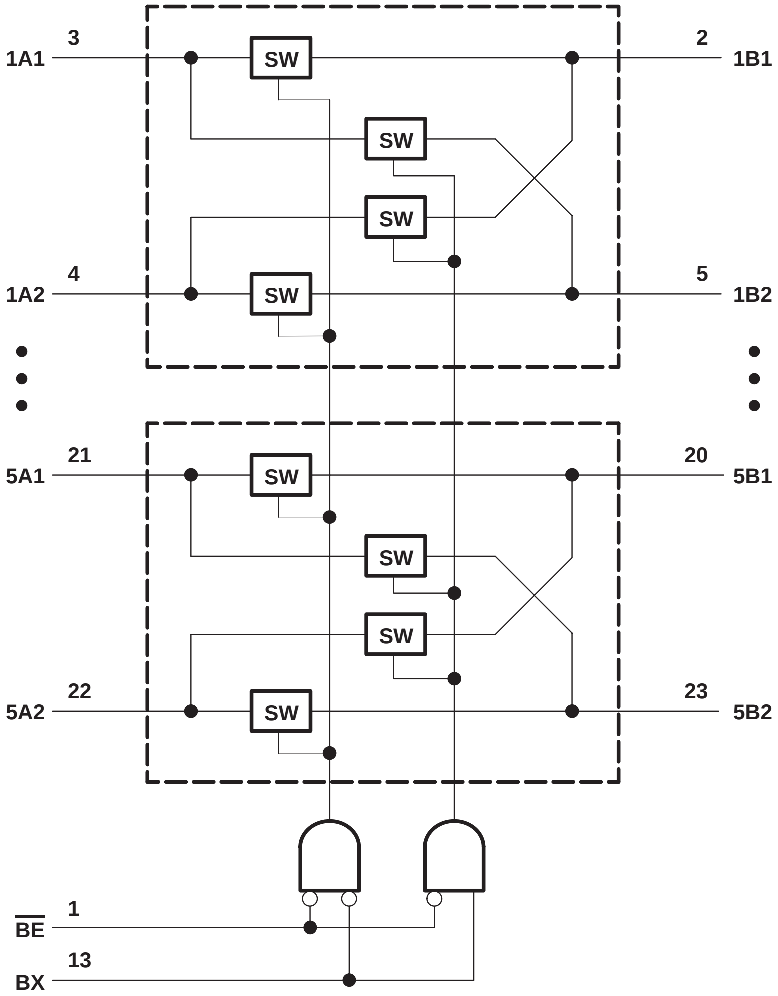
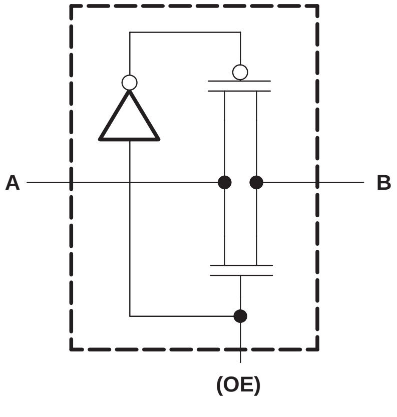
logic diagram (positive logic)


1A1
3
SW
2
1B1
SW
SW
1A2
4
SW
5
1B2
5A1
21
SW
20
5B1
SW
SW
5A2
22
SW
23
5B2
BE
1
BX
13

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)		−0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[‡]	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	μA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	μA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			10	μA
ΔI_{CC}[§]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{BE}$ = V_{CC}			13.5		pF
r_{on}[¶]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V,	I_I = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[§] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

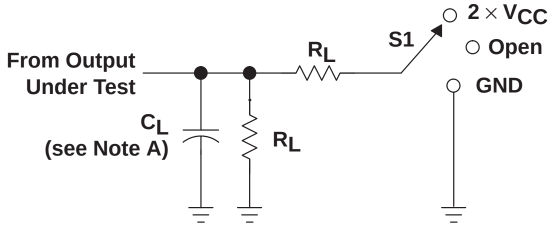
[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A		0.15		0.25	ns
t_{pd}	BX	A or B	1.5	5.8	1.5	4.7	ns
t_{en}	$\overline{BE}$	A or B	1.5	5.3	1.5	4.7	ns
t_{dis}	$\overline{BE}$	A or B	1	6	1	6	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

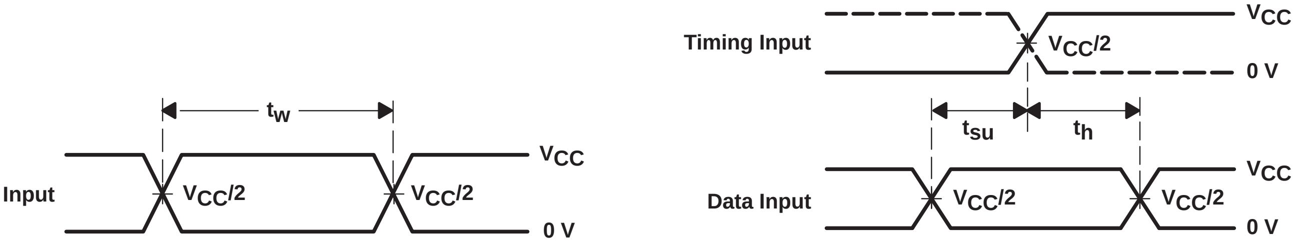
PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
R_L
S1
$2 \times V_{CC}$
Open
GND
C_L
(see Note A)
R_L

LOAD CIRCUIT

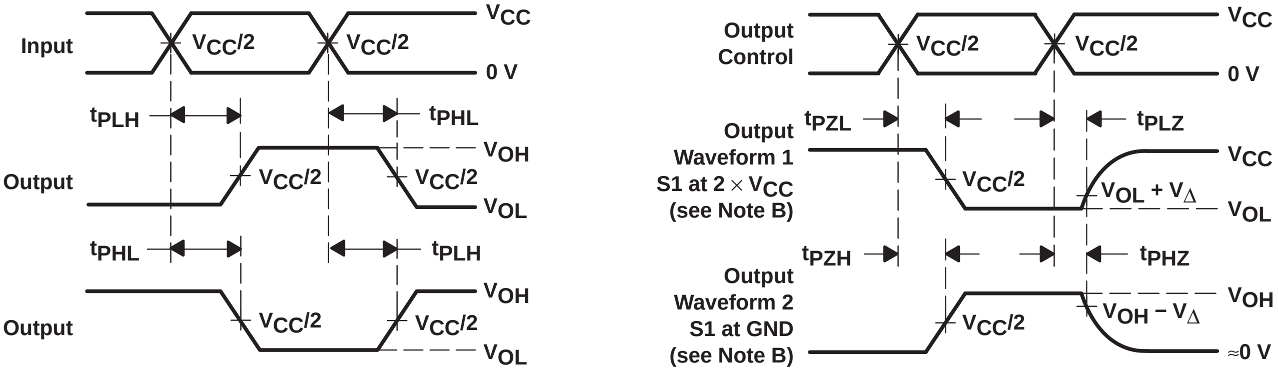
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
Timing Input
$V_{CC}/2$
V_{CC}
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
Output
Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at $2 \times V_{CC}$
(see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at GND
(see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2$ ns, $t_f \le 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments Widebus™ Family**
- **4-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Break-Before-Make Feature**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

description/ordering information

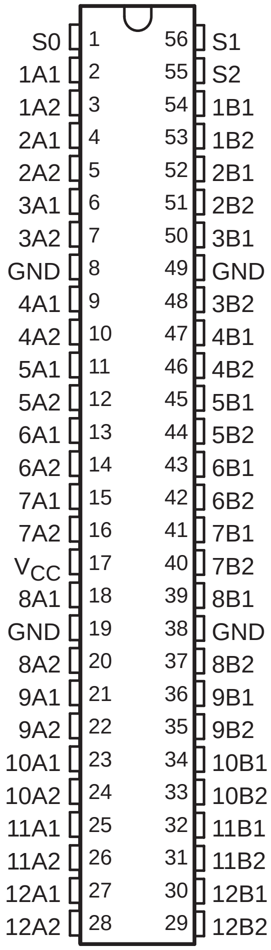
The SN74CBTLV16212 provides 24 bits of high-speed bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 24-bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0, S1, S2) terminals.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

The SN74CBTLV16212 is specified by the break-before-make feature to have no through current when switching between B ports.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)


S0 1 56 S1
1A1 2 55 S2
1A2 3 54 1B1
2A1 4 53 1B2
2A2 5 52 2B1
3A1 6 51 2B2
3A2 7 50 3B1
GND 8 49 GND
4A1 9 48 3B2
4A2 10 47 4B1
5A1 11 46 4B2
5A2 12 45 5B1
6A1 13 44 5B2
6A2 14 43 6B1
7A1 15 42 6B2
7A2 16 41 7B1
VCC 17 40 7B2
8A1 18 39 8B1
GND 19 38 GND
8A2 20 37 8B2
9A1 21 36 9B1
9A2 22 35 9B2
10A1 23 34 10B1
10A2 24 33 10B2
11A1 25 32 11B1
11A2 26 31 11B2
12A1 27 30 12B1
12A2 28 29 12B2

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBTLV16212DL	CBTLV16212
		Tape and reel	SN74CBTLV16212DLR	
	TSSOP − DGG	Tape and reel	SN74CBTLV16212GR	CBTLV16212
	TVSOP − DGV	Tape and reel	SN74CBTLV16212VR	CN212

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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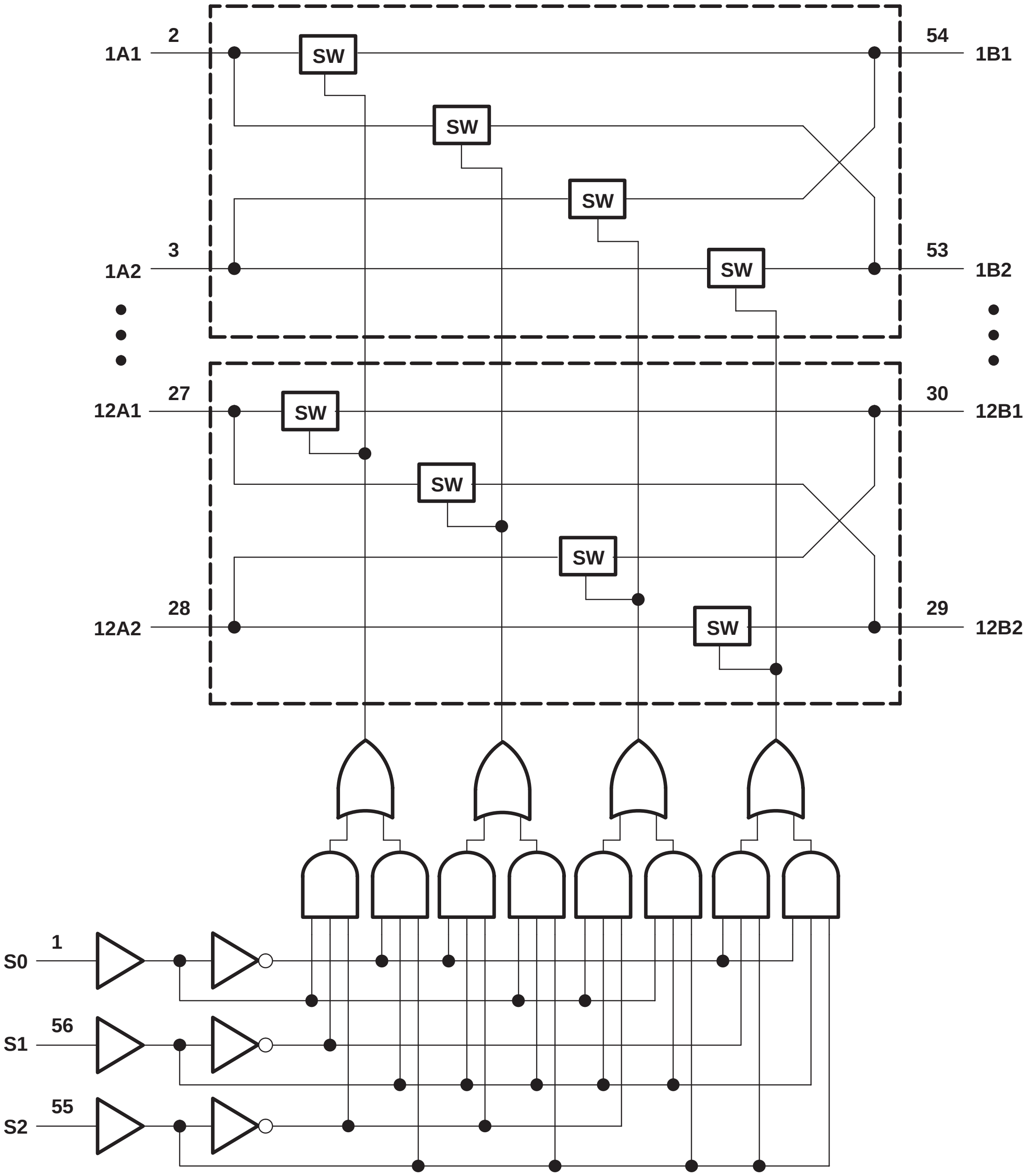
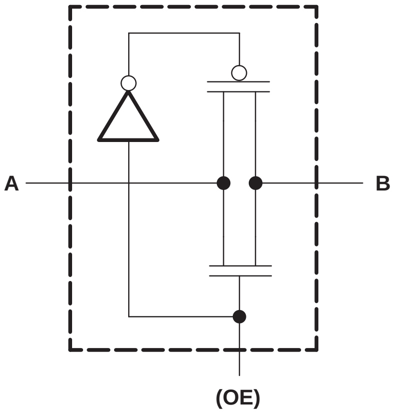
FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	**S1**	**S0**	**A1**	**A2**	
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 port = B1 port
L	H	L	B2	Z	A1 port = B2 port
L	H	H	Z	B1	A2 port = B1 port
H	L	L	Z	B2	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 port = B1 port A2 port = B2 port
H	H	H	B2	B1	A1 port = B2 port A2 port = B1 port

logic diagram (positive logic)


1A1
2
SW
54
1B1
SW
SW
1A2
3
SW
53
1B2
12A1
27
SW
30
12B1
SW
SW
12A2
28
SW
29
12B2
S0
1
S1
56
S2
55

simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)		−0.5 V to 4.6 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	$V_I = V_{CC}$ or GND				±1	μA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	μA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	$V_I = V_{CC}$ or GND			10	μA
ΔI_{CC}‡	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
C_i	Control inputs	V_I = 3 V or 0				5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	S_1, S_2, and S_3 = GND			8		pF
r_{on}§		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V,	I_I = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

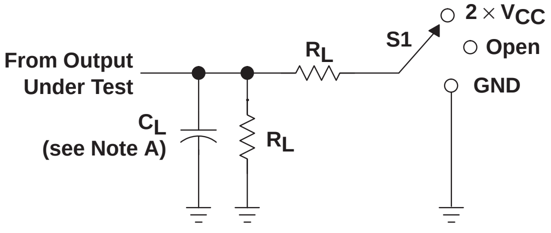
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.15		0.25	ns
t_{pd}	S	B or A	3	11.1	3	8.8	ns
t_{en}	S	A or B	3	10.9	3	8.6	ns
t_{dis}	S	A or B	1	8.7	2	8.8	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

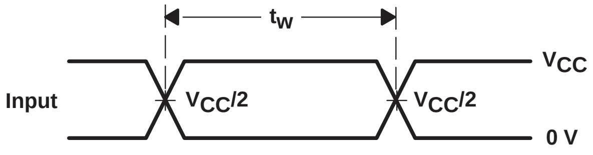
PARAMETER MEASUREMENT INFORMATION


From Output Under Test
R_L
S1
2 × V_{CC}
Open
GND
C_L (see Note A)
R_L

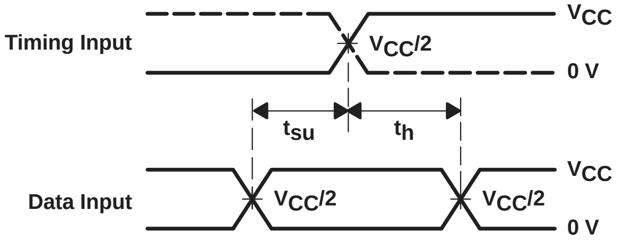
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

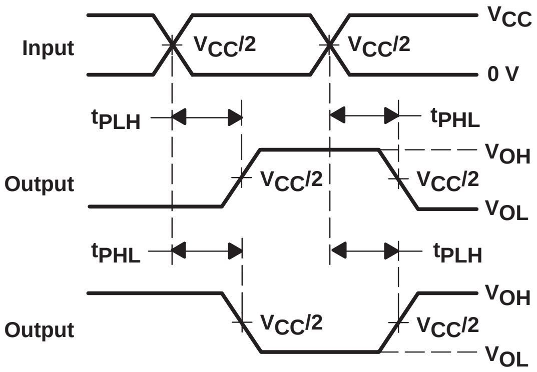
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V


t_w
Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

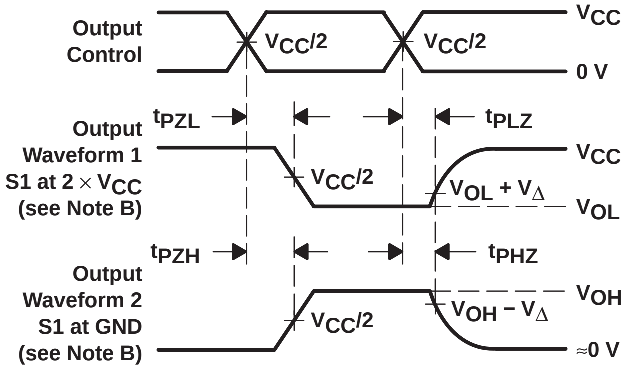
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
V_{CC}
$V_{CC}/2$
0 V
t_{su}
t_h
Data Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PLH}
t_{PHL}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
$V_{CC}/2$
$V_{CC}/2$
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output Control
$V_{CC}/2$
$V_{CC}/2$
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at 2 × V_{CC} (see Note B)
$V_{CC}/2$
$V_{OL} + V_\Delta$
V_{CC}
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
$V_{CC}/2$
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2$ ns, $t_f \le 2$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

Insert Tab Here

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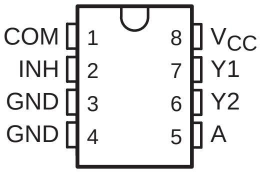
SN74AUC2G53
SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH OR 2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

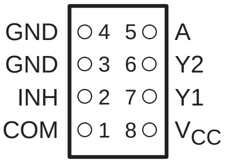
SCES484A − AUGUST 2003 − REVISED NOVEMBER 2003

- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **Operates at 0.8 V to 2.7 V**
- **Sub 1-V Operable**
- **Low Power Consumption, 10 μA at 2.7 V**
- **High On-Off Output Voltage Ratio**
- **High Degree of Linearity**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DCT OR DCU PACKAGE
(TOP VIEW)



YEP OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

This analog switch is operational at 0.8-V to 2.7-V V_{CC}, but is designed specifically for 1.1-V to 2.7-V V_{CC} operation.

The SN74AUC2G53 can handle both analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[‡]
−40°C to 85°C	NanoStar™ − WCSP (DSBGA) 0.23-mm Large Bump − YEP	Tape and reel	SN74AUC2G53YEPR	_ _ _U4_
	NanoFree™ − WCSP (DSBGA) 0.23-mm Large Bump − YZP (Pb-free)		SN74AUC2G53YZPR	
	SSOP − DCT	Tape and reel	SN74AUC2G53DCTR	U53_ _ _
	VSSOP − DCU	Tape and reel	SN74AUC2G53DCUR	U53_

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

[‡] DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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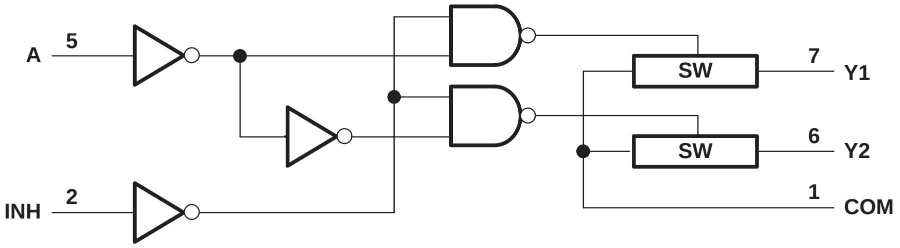
FUNCTION TABLE

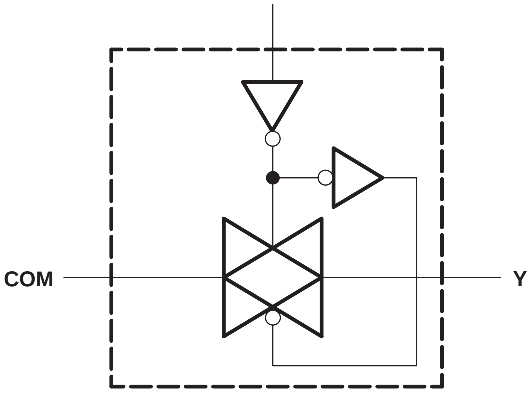
CONTROL INPUTS		ON CHANNEL
INH	**A**	
L	L	Y1
L	H	Y2
H	X	None

logic diagram (positive logic)



NOTE A: For simplicity, the test conditions shown in Figures 1 through 4 and 6 through 10 are for the demultiplexer configuration. Signals may be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

simplified schematic, each switch (SW)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)		−0.5 V to 3.6 V
Input voltage range, V_I (see Notes 1 and 2)		−0.5 V to 3.6 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1 and 2)		−0.5 V to V_{CC} + 0.5 V
Control input clamp current, I_{IK} ($V_I < 0$)		−50 mA
I/O port diode current, I_{IOK} ($V_{I/O} < 0$ or $V_{I/O} > V_{CC}$)		±50 mA
On-state switch current, I_T ($V_{I/O} = 0$ to V_{CC})		±50 mA
Continuous current through V_{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	DCT package	220°C/W
	DCU package	227°C/W
	YEP/YZP package	102°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	2.7	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.7		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_I	Control input voltage		0	3.6	V
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 0.8 V to 1.6 V		20	ns/V
		V_{CC} = 1.65 V to 1.95 V		10	
		V_{CC} = 2.3 V to 2.7 V		3.5	
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
r_{on}	On-state switch resistance		$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ (see Figures 1 and 2)	I_S = 4 mA	1.1 V			40	Ω
					1.65 V		12.5	20	
				I_S = 8 mA	2.3 V		6	15	
$r_{on(p)}$	Peak on resistance		$V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$ (see Figures 1 and 2)	I_S = 4 mA	1.1 V		131	180	Ω
					1.65 V		32	80	
				I_S = 8 mA	2.3 V		15	20	
Δr_{on}	Difference of on-state resistance between switches		$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figures 1 and 2)	I_S = 4 mA	1.1 V			4	Ω
					1.65 V			1	
				I_S = 8 mA	2.3 V			1	
$I_{S(off)}$	Off-state switch leakage current		$V_I = V_{CC}$ and V_O = GND, or V_I = GND and $V_O = V_{CC}$, $V_{INH} = V_{IH}$ (see Figure 3)		2.7 V			±1	μA
								±0.1†	
$I_{S(on)}$	On-state switch leakage current		$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$, V_O = Open (see Figure 4)		2.7 V			±1	μA
								±0.1†	
I_I	Control input current		$V_C = V_{CC}$ or GND		2.7 V			±5	μA
I_{CC}	Supply current		$V_C = V_{CC}$ or GND		2.7 V			10	μA
C_{ic}	Control input capacitance				2.5 V		2		pF
$C_{io(off)}$	Switch input/output capacitance	Y			2.5 V		3		pF
		COM					4.5		
$C_{io(on)}$	Switch input/output capacitance				2.5 V		9		pF

† T_A = 25°C

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V		V_{CC} = 1.5 V ± 0.1 V		V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}‡	COM or Y	Y or COM	0.3		0.3		0.3			0.2		0.1	ns
t_{en}	INH	COM or Y	9.2	0.5	3.5	0.5	2.2	0.5	1	1.9	0.5	1.8	ns
t_{dis}			8.1	0.5	4.2	0.5	3.2	0.5	1.9	3.4	0.5	2.6	
t_{en}	A	COM or Y	9.2	0.5	3.6	0.5	2.3	0.5	1.1	1.9	0.5	1.6	ns
t_{dis}			10	0.5	3.6	0.5	2.3	0.5	1.1	2	0.5	1.6	

‡ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

switching characteristics over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}[†]	COM or Y	Y or COM			0.4		0.2	ns
t_{en}	INH	COM or Y	0.5	1.6	3.1	0.5	2.2	ns
t_{dis}			0.5	2.2	3.4	0.5	2.2	ns
t_{en}	A	COM or Y	0.5	1.6	3	0.5	2.2	ns
t_{dis}			0.5	1.6	3	0.5	2.3	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

analog switch characteristics, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response[‡] (switch ON)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = sine wave (see Figure 6)	0.8 V	90	MHz
				1.1 V	101	
				1.4 V	110	
				1.65 V	122	
				2.3 V	198	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = sine wave (see Figure 6)	0.8 V	>500	
				1.1 V	>500	
				1.4 V	>500	
				1.65 V	>500	
				2.3 V	>500	
Crosstalk[§] (between switches)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	0.8 V	−59	dB
				1.1 V	−59	
				1.4 V	−59	
				1.65 V	−59	
				2.3 V	−60	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	0.8 V	−55	
				1.1 V	−55	
				1.4 V	−55	
				1.65 V	−55	
				2.3 V	−55	
Crosstalk (control input to signal output)	INH	COM or Y	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)	0.8 V	0.56	mV
				1.1 V	0.68	
				1.4 V	0.81	
				1.65 V	0.93	
				2.3 V	1.5	

[‡] Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads −3 dB.

[§] Adjust f_{in} voltage to obtain 0 dBm at input.

analog switch characteristics, T_A = 25°C (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Feed-through attenuation§ (switch OFF)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	0.8 V	−60	dB
				1.1 V	−60	
				1.4 V	−60	
				1.65 V	−60	
				2.3 V	−60	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	0.8 V	−59	
				1.1 V	−59	
				1.4 V	−59	
				1.65 V	−59	
				2.3 V	−59	
Sine-wave distortion	COM or Y	Y or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	0.8 V	6.19	%
				1.1 V	0.39	
				1.4 V	0.06	
				1.65 V	0.02	
				2.3 V	0.01	
			C_L = 50 pF, R_L = 10 kΩ, f_{in} = 10 kHz (sine wave) (see Figure 10)	0.8 V	3.55	
				1.1 V	0.38	
				1.4 V	0.04	
				1.65 V	0.02	
				2.3 V	0.02	

§ Adjust f_{in} voltage to obtain 0 dBm at input.

operating characteristics for INH input, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 0.8 V	V_{CC} = 1.2 V	V_{CC} = 1.5 V	V_{CC} = 1.8 V	V_{CC} = 2.5 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	3	3	3	3	3	pF

operating characteristics for A input, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 0.8 V	V_{CC} = 1.2 V	V_{CC} = 1.5 V	V_{CC} = 1.8 V	V_{CC} = 2.5 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	5.5	5.5	5.5	5.5	5.5	pF
		Outputs disabled		0.5	0.5	0.5	0.5	0.5	

PARAMETER MEASUREMENT INFORMATION

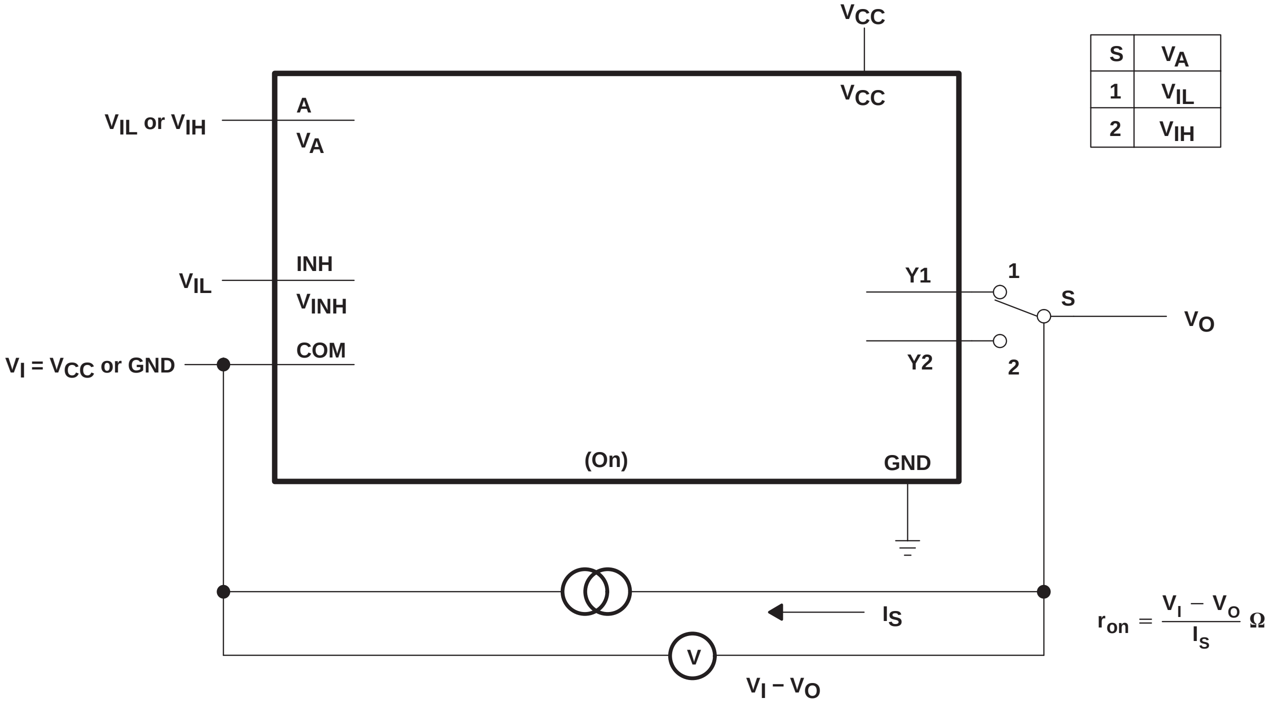

V_{CC}
V_{CC}
S | V_A
1 | V_{IL}
2 | V_{IH}
V_{IL} or V_{IH}
A
V_A
V_{IL}
INH
V_{INH}
$V_I = V_{CC}$ or GND
COM
Y1
1
S
V_O
Y2
2
(On)
GND
I_S
$r_{on} = \frac{V_I - V_O}{I_S}\ \Omega$
V
$V_I - V_O$

Figure 1. On-State Resistance Test Circuit

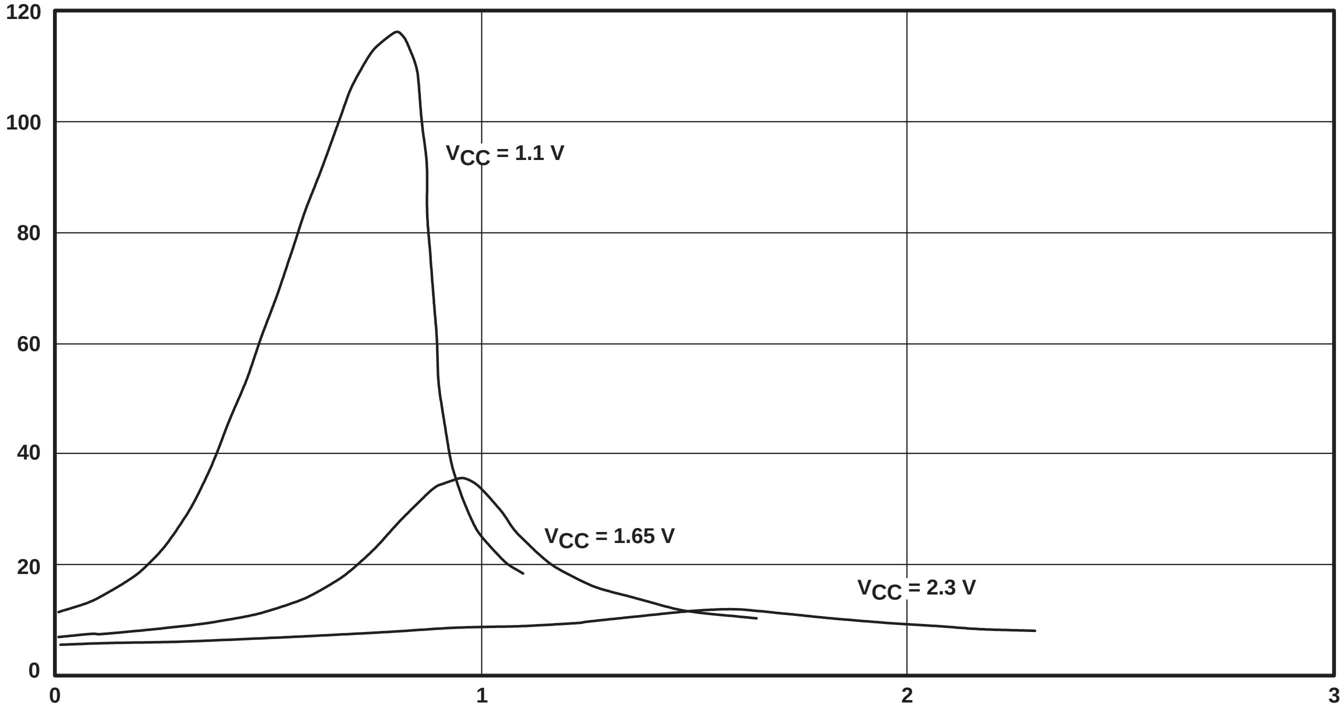
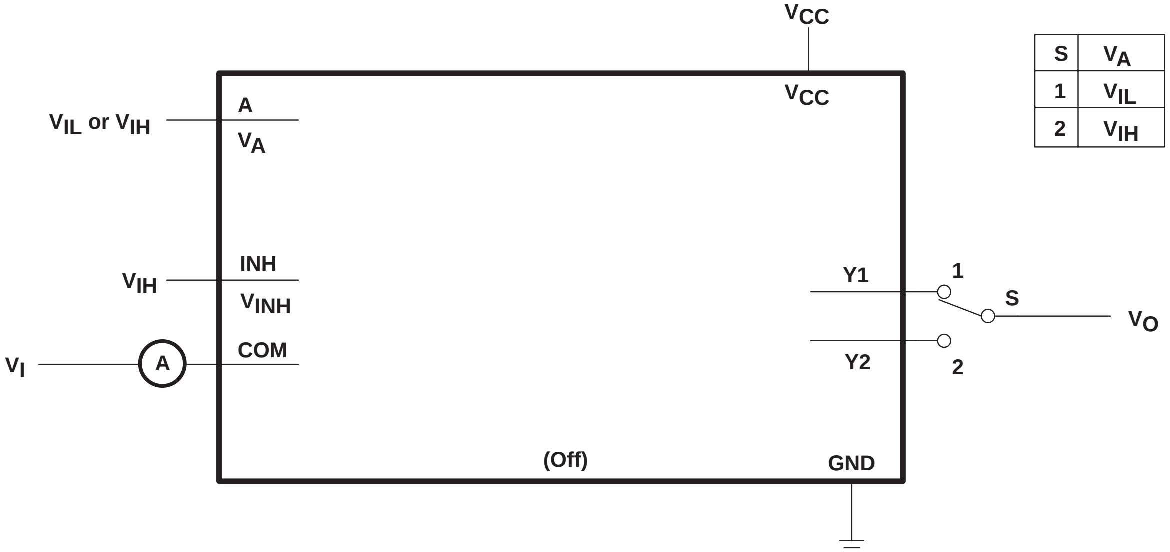


Figure 2. Typical r_{on} as a Function of Voltage (V_I) for V_I = 0 to V_{CC}

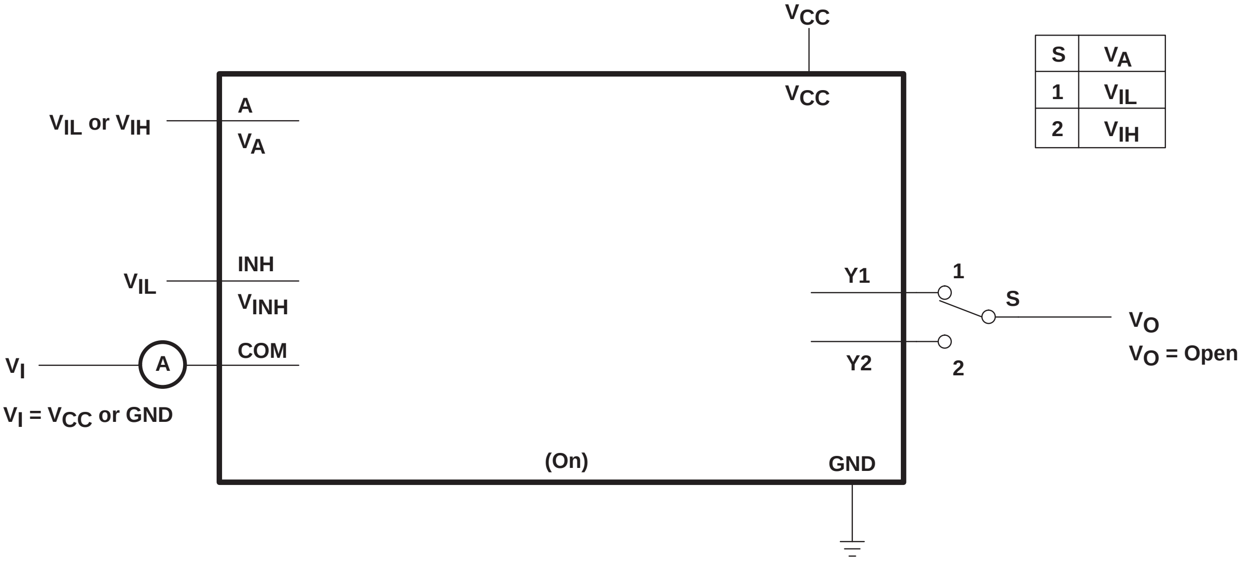
PARAMETER MEASUREMENT INFORMATION


V_{CC}
V_{CC}
V_{IL} or V_{IH}
A
V_A
V_{IH}
INH
V_{INH}
V_I
A
COM
Y1
1
S
V_O
Y2
2
(Off)
GND

S	V_A
1	V_{IL}
2	V_{IH}

Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

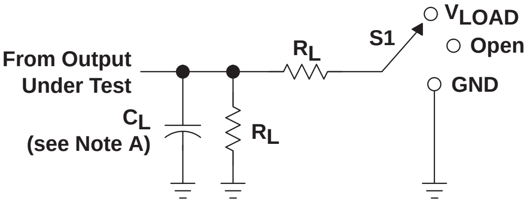
Figure 3. Off-State Switch Leakage-Current Test Circuit


V_{CC}
V_{CC}
V_{IL} or V_{IH}
A
V_A
V_{IL}
INH
V_{INH}
V_I
A
COM
V_I = V_{CC} or GND
Y1
1
S
V_O
V_O = Open
Y2
2
(On)
GND

S	V_A
1	V_{IL}
2	V_{IH}

Figure 4. On-State Switch Leakage-Current Test Circuit

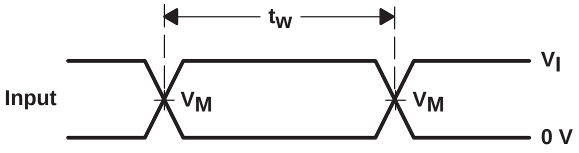
PARAMETER MEASUREMENT INFORMATION


From Output Under Test
R_L
S1
V_{LOAD}
Open
GND
C_L (see Note A)
R_L

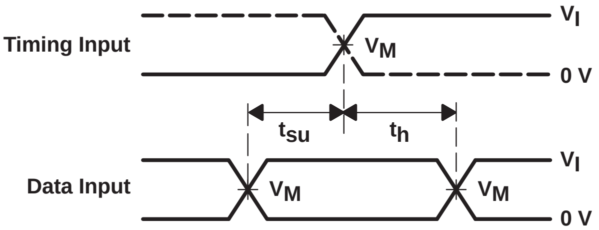
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

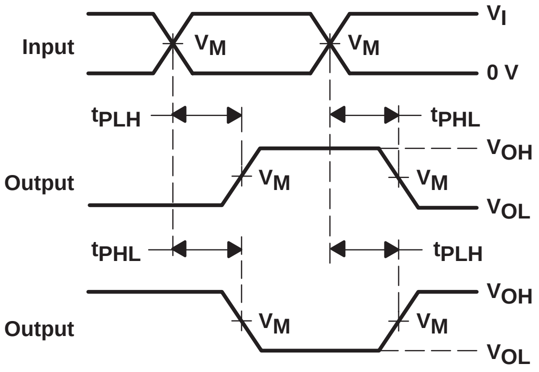
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
0.8 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.2 V ± 0.1 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.15 V
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V


t_w
Input
V_M
V_M
V_I
0 V

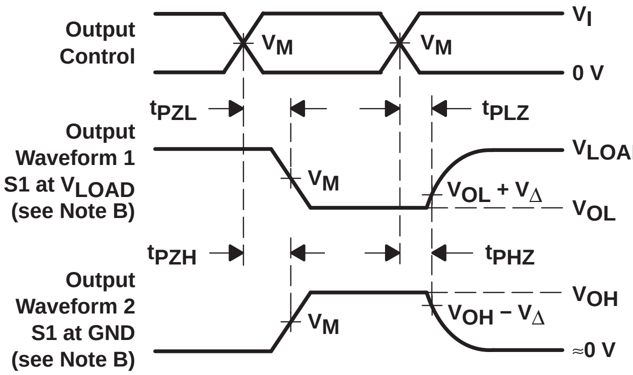
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
V_I
V_M
0 V
t_{su}
t_h
Data Input
V_M
V_M
V_I
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
V_M
V_M
V_I
0 V
t_{PLH}
t_{PHL}
Output
V_M
V_M
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
V_M
V_M
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

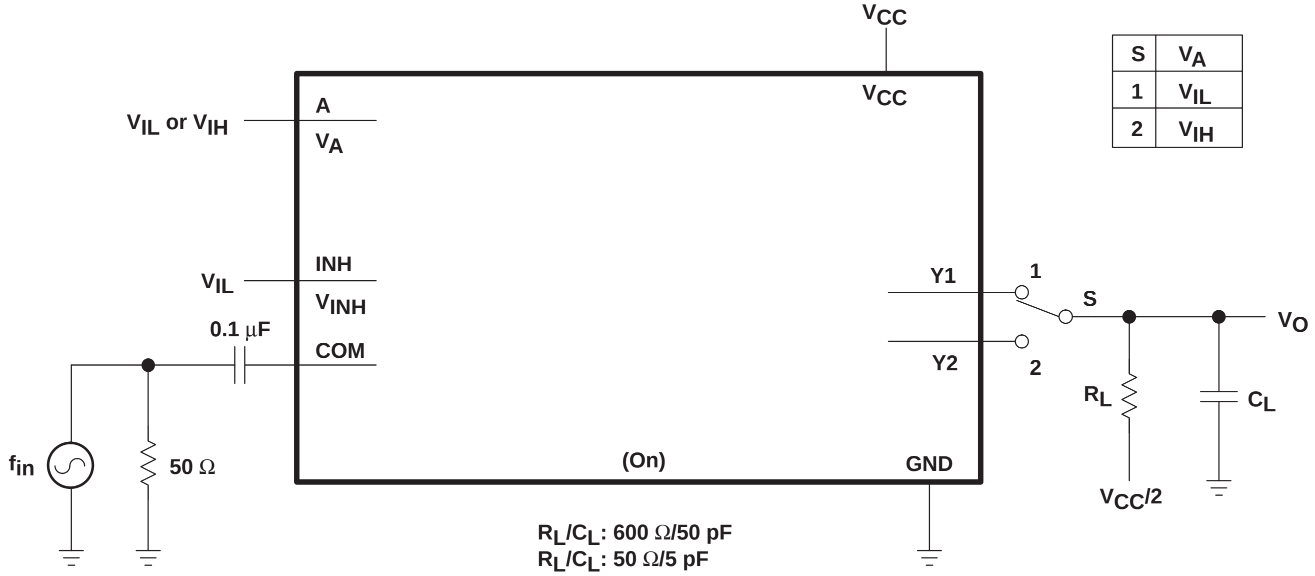

Output Control
V_M
V_M
V_I
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at V_{LOAD} (see Note B)
V_M
$V_{LOAD}/2$
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
V_M
V_{OH}
$V_{OH} - V_\Delta$
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

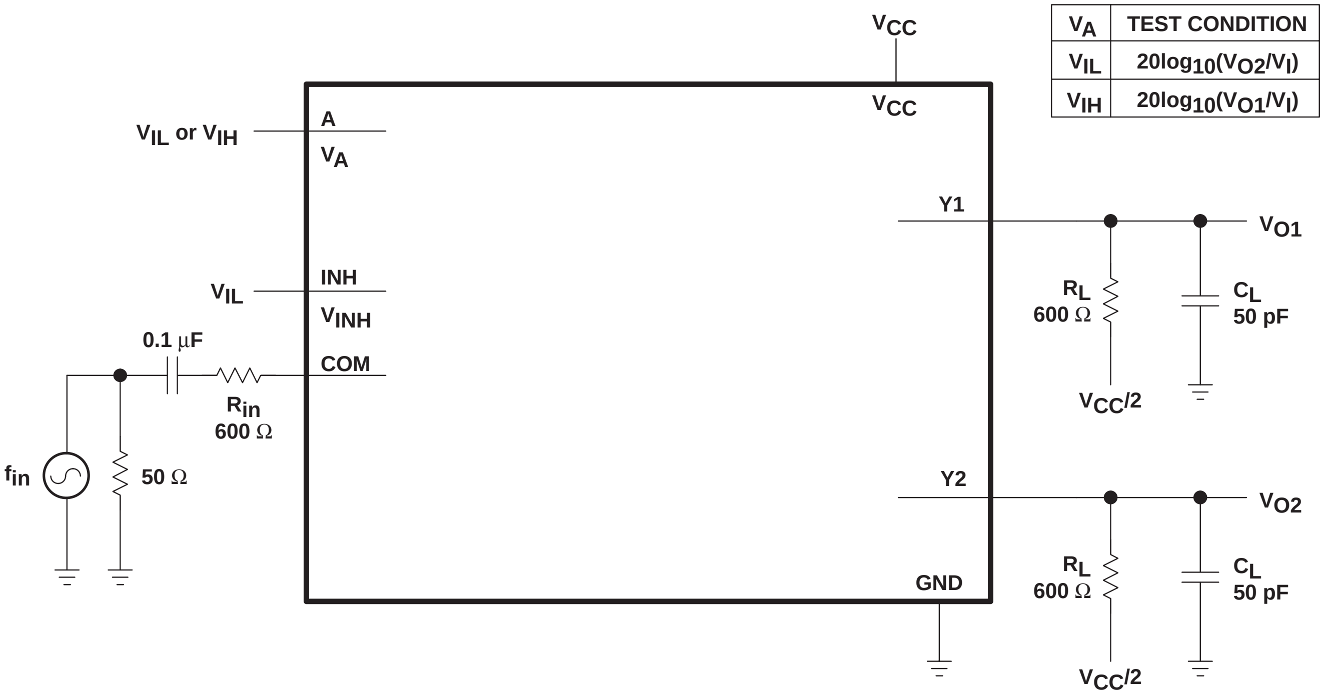
PARAMETER MEASUREMENT INFORMATION


V_{CC}
V_{CC}
V_{IL} or V_{IH}
A
V_A
V_{IL}
INH
V_{INH}
0.1 µF
COM
f_{in}
50 Ω
(On)
GND
Y1
Y2
1
2
S
V_O
R_L
C_L
$V_{CC}/2$

S	V_A
1	V_{IL}
2	V_{IH}

R_L/C_L: 600 Ω/50 pF
R_L/C_L: 50 Ω/5 pF

Figure 6. Frequency Response (Switch On)


V_{CC}
V_{CC}
V_{IL} or V_{IH}
A
V_A
V_{IL}
INH
V_{INH}
0.1 µF
COM
R_{in}
600 Ω
f_{in}
50 Ω
GND
Y1
V_{O1}
R_L
600 Ω
C_L
50 pF
$V_{CC}/2$
Y2
V_{O2}
R_L
600 Ω
C_L
50 pF
$V_{CC}/2$

V_A	TEST CONDITION
V_{IL}	$20\log_{10}(V_{O2}/V_I)$
V_{IH}	$20\log_{10}(V_{O1}/V_I)$

Figure 7. Crosstalk (Between Switches)

PARAMETER MEASUREMENT INFORMATION

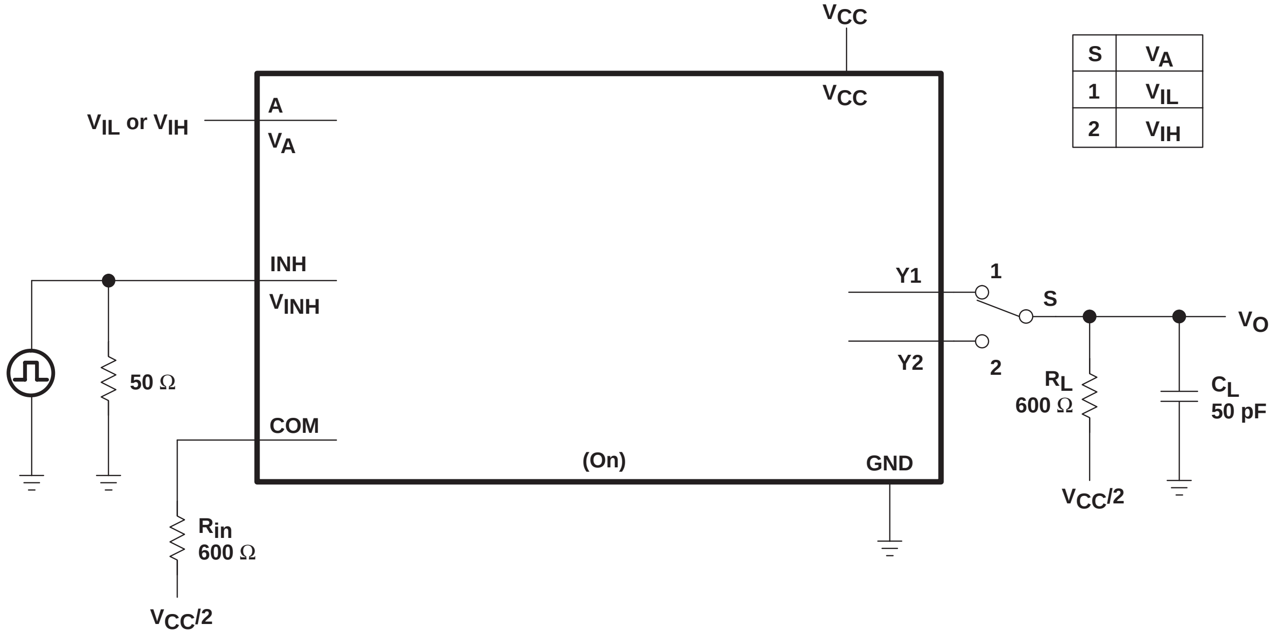
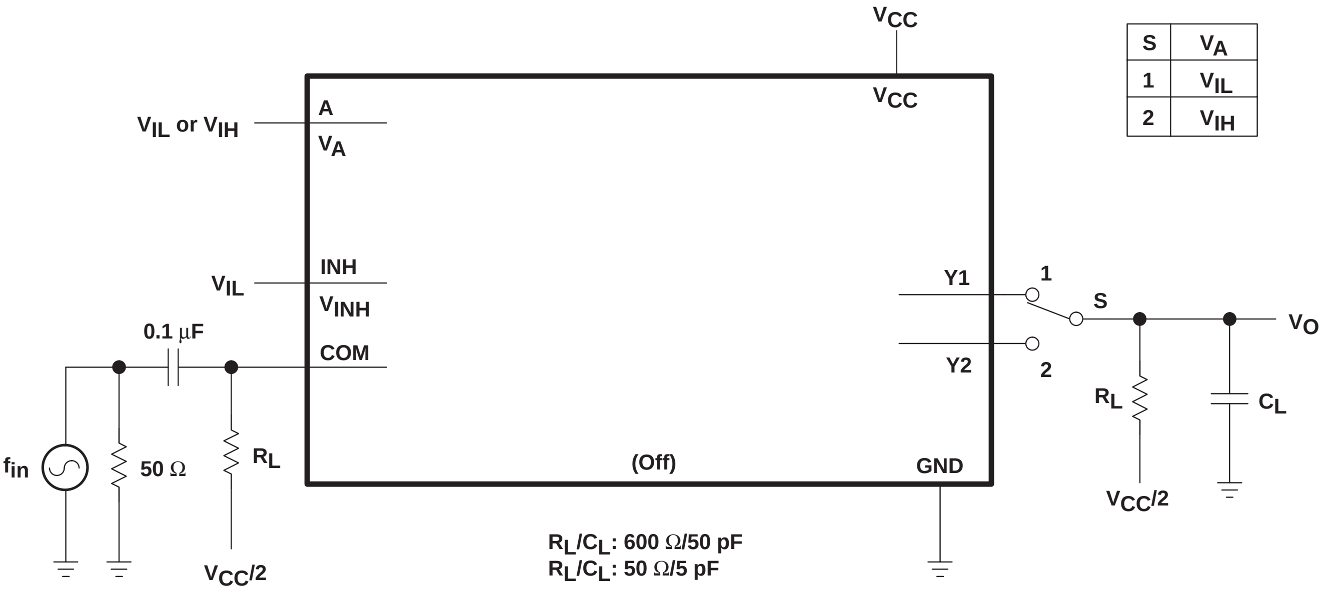

VCC
VCC
S | VA
1 | VIL
2 | VIH
VIL or VIH
A
VA
INH
VINH
50 Ω
COM
Rin
600 Ω
VCC/2
(On)
GND
Y1
Y2
1
2
S
VO
RL
600 Ω
VCC/2
CL
50 pF

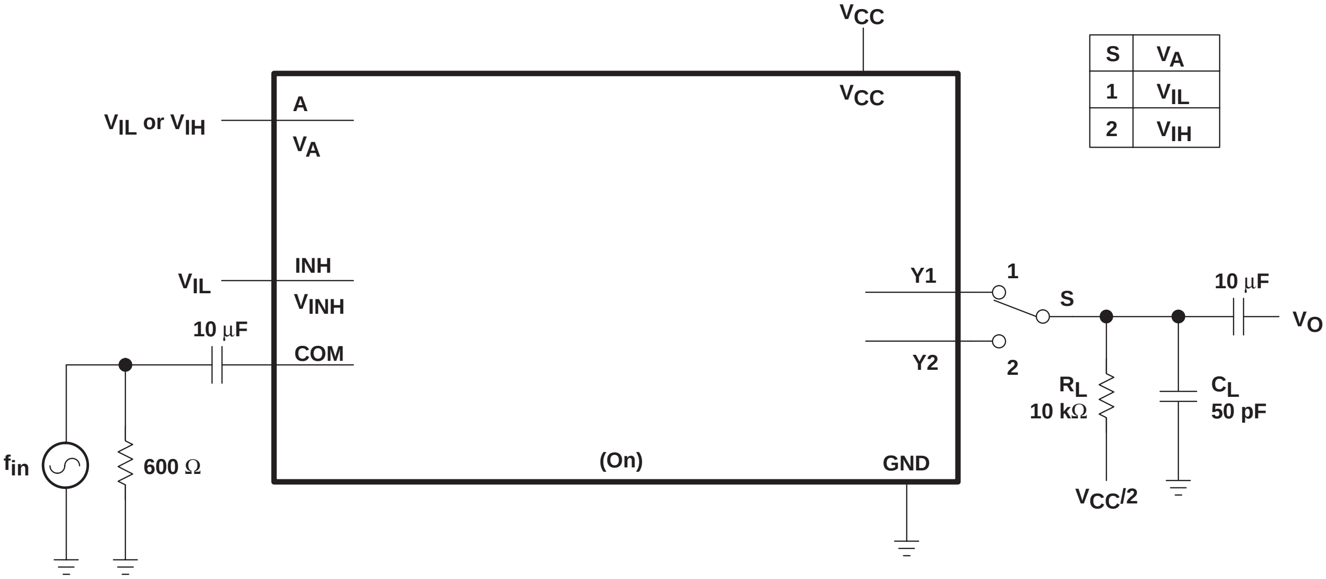
Figure 8. Crosstalk (Control Input, Switch Output)


VCC
VCC
S | VA
1 | VIL
2 | VIH
VIL or VIH
A
VA
VIL
INH
VINH
0.1 µF
COM
fin
50 Ω
RL
VCC/2
(Off)
GND
Y1
Y2
1
2
S
VO
RL
CL
VCC/2

R_L/C_L: 600 Ω/50 pF
R_L/C_L: 50 Ω/5 pF

Figure 9. Feedthrough (Switch Off)

PARAMETER MEASUREMENT INFORMATION


V_{CC}
V_{CC}
V_{IL} or V_{IH}
A
V_A
V_{IL}
INH
V_{INH}
10 μF
COM
f_{in}
600 Ω
(On)
GND
Y1
Y2
1
2
S
R_L
10 kΩ
$V_{CC}/2$
C_L
50 pF
10 μF
V_O

S	V_A
1	V_{IL}
2	V_{IH}

V_{CC} = 0.8 V, V_I = 0.7 V_{P-P}
V_{CC} = 1.1 V, V_I = 1 V_{P-P}
V_{CC} = 1.4 V, V_I = 1.2 V_{P-P}
V_{CC} = 1.65 V, V_I = 1.4 V_{P-P}
V_{CC} = 2.3 V, V_I = 2 V_{P-P}

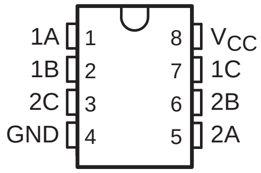
Figure 10. Sine-Wave Distortion

SN74AUC2G66
DUAL BILATERAL ANALOG SWITCH

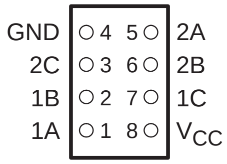
SCES507 − NOVEMBER 2003

- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **Operates at 0.8 V to 2.7 V**
- **Sub 1-V Operable**
- **Max t_{pd} of 0.5 ns at 1.8 V**
- **Low Power Consumption, 10 μA at 2.7 V**
- **High On-Off Output Voltage Ratio**
- **High Degree of Linearity**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DCT OR DCU PACKAGE
(TOP VIEW)



YEP OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

This dual analog switch is operational at 0.8-V to 2.7-V V_{CC}, but is designed specifically for 1.1-V to 2.7-V V_{CC} operation.

The SN74AUC2G66 can handle both analog and digital signals. It permits signals with amplitudes of up to 2.7-V (peak) to be transmitted in either direction.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	NanoStar™ − WCSP (DSBGA) 0.23-mm Large Bump − YEP	Tape and reel	SN74AUC2G66YEPR	_ _ _U6_
	NanoFree™ − WCSP (DSBGA) 0.23-mm Large Bump − YZP (Pb-free)	Tape and reel	SN74AUC2G66YZPR	
	SSOP − DCT	Tape and reel	SN74AUC2G66DCTR	U66_ _ _
	VSSOP − DCU	Tape and reel	SN74AUC2G66DCUR	U66_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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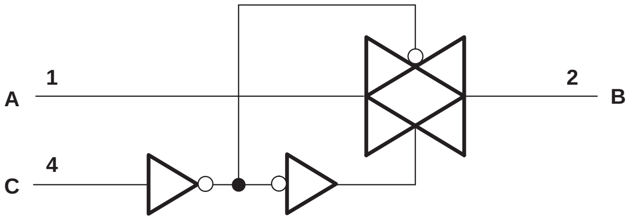
FUNCTION TABLE

CONTROL INPUT (C)	SWITCH
L	OFF
H	ON

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.5 V to 3.6 V
Input voltage range, V_I (see Notes 1 and 2)	−0.5 V to 3.6 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1 and 2)	−0.5 V to V_{CC} + 0.5 V
Control input clamp current, I_{IK} ($V_I < 0$)	−50 mA
I/O port diode current, I_{IOK} ($V_{I/O} < 0$ or $V_{I/O} > V_{CC}$)	±50 mA
On-state switch current, I_T ($V_{I/O} = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DCT package	220°C/W
DCU package	227°C/W
YEP/YZP package	102°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	2.7	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.7		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_I	Control input voltage		0	3.6	V
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 1.65 V†		20	ns/V
		V_{CC} = 1.65 V to 2.3 V‡		20	
		V_{CC} = 2.3 V to 2.7 V‡		20	
T_A	Operating free-air temperature		−40	85	°C

† The data was taken at C_L = 15 pF, R_L = 2 kΩ (see Figure 1).

‡ The data was taken at C_L = 30 pF, R_L = 500 Ω (see Figure 1).

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP§	MAX	UNIT
r_{on}	On-state switch resistance	V_I = V_{CC} or GND, V_C = V_{IH} (see Figures 1 and 2)	I_S = 4 mA	1.1 V		17	40	Ω
				1.65 V		7	20	
			I_S = 8 mA	2.3 V		4	15	
$r_{on(p)}$	Peak on resistance	V_I = V_{CC} to GND, V_C = V_{IH} (see Figures 1 and 2)	I_S = 4 mA	1.1 V		131	180	Ω
				1.65 V		32	80	
			I_S = 8 mA	2.3 V		15	20	
Δr_{on}	Difference of on-state resistance between switches	V_I = V_{CC} to GND, V_C = V_{IH} (see Figures 1 and 2)	I_S = 4 mA	1.1 V			3	Ω
				1.65 V			1	
			I_S = 8 mA	2.3 V			1	
$I_{S(off)}$	Off-state switch leakage current	V_I = V_{CC} and V_O = GND, or V_I = GND and V_O = V_{CC}, V_C = V_{IL} (see Figure 3)		2.7 V			±1	μA
							±0.1†	
$I_{S(on)}$	On-state switch leakage current	V_I = V_{CC} or GND, V_C = V_{IH}, V_O = Open (see Figure 4)		2.7 V			±1	μA
							±0.1†	
I_I	Control input current	V_I = V_{CC} or GND		0 to 2.7 V			±5	μA
I_{CC}	Supply current	V_I = V_{CC} or GND,	I_O = 0	0.8 V to 2.7 V			10	μA
C_{ic}	Control input capacitance			2.5 V		2.5		pF
$C_{io(off)}$	Switch input/output capacitance			2.5 V		3		pF
$C_{io(on)}$	Switch input/output capacitance			2.5 V		7		pF

§ T_A = 25°C

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V		V_{CC} = 1.5 V ± 0.1 V		V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A	1		0.6		0.5			0.5		0.4	ns
t_{en}	C	A or B	5	0.5	3	0.5	2.1	0.5	0.9	1.6	0.5	1.4	ns
t_{dis}	C	A or B	5.3	0.5	4	0.5	3	0.5	2.6	3.3	0.5	2.7	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

switching characteristics over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}[†]	A or B	B or A			0.7		0.7	ns
t_{en}	C	A or B	0.5	1.6	2.7	0.5	2.3	ns
t_{dis}	C	A or B	0.5	2.7	3.4	0.5	2	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

analog switch characteristics, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response[‡] (switch ON)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = sine wave (see Figure 6)	0.8 V	101	MHz
				1.1 V	150	
				1.4 V	175	
				1.65 V	250	
				2.3 V	400	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = sine wave (see Figure 6)	0.8 V	450	
				1.1 V	>500	
				1.4 V	>500	
				1.65 V	>500	
				2.3 V	>500	
Crosstalk[§] (between switches)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	0.8 V	−60	dB
				1.1 V	−60	
				1.4 V	−60	
				1.65 V	−60	
				2.3 V	−60	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	0.8 V	−65	
				1.1 V	−65	
				1.4 V	−65	
				1.65 V	−65	
				2.3 V	−65	

[‡] Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads −3 dB.
[§] Adjust f_{in} voltage to obtain 0 dBm at input.

analog switch characteristics, T_A = 25°C (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Crosstalk (control input to signal output)	C	A or B	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)	0.8 V	9	mV
				1.1 V	14	
				1.4 V	15	
				1.65 V	16	
				2.3 V	20	
Feed-through attenuation[‡] (switch OFF)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	0.8 V	−50	dB
				1.1 V	−50	
				1.4 V	−50	
				1.65 V	−50	
				2.3 V	−50	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	0.8 V	−60	
				1.1 V	−60	
				1.4 V	−60	
				1.65 V	−60	
				2.3 V	−60	
Sine-wave distortion	A or B	B or A	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	0.8 V	7	%
				1.1 V	0.256	
				1.4 V	0.04	
				1.65 V	0.03	
				2.3 V	0.01	
	A or B	B or A	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 10 kHz (sine wave) (see Figure 10)	0.8 V	3.7	
				1.1 V	0.4	
				1.4 V	0.04	
				1.65 V	0.02	
				2.3 V	0.02	

[‡] Adjust f_{in} voltage to obtain 0 dBm at input.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 0.8 V	V_{CC} = 1.2 V	V_{CC} = 1.5 V	V_{CC} = 1.8 V	V_{CC} = 2.5 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	2.5	2.5	2.5	2.5	2.5	pF

PARAMETER MEASUREMENT INFORMATION

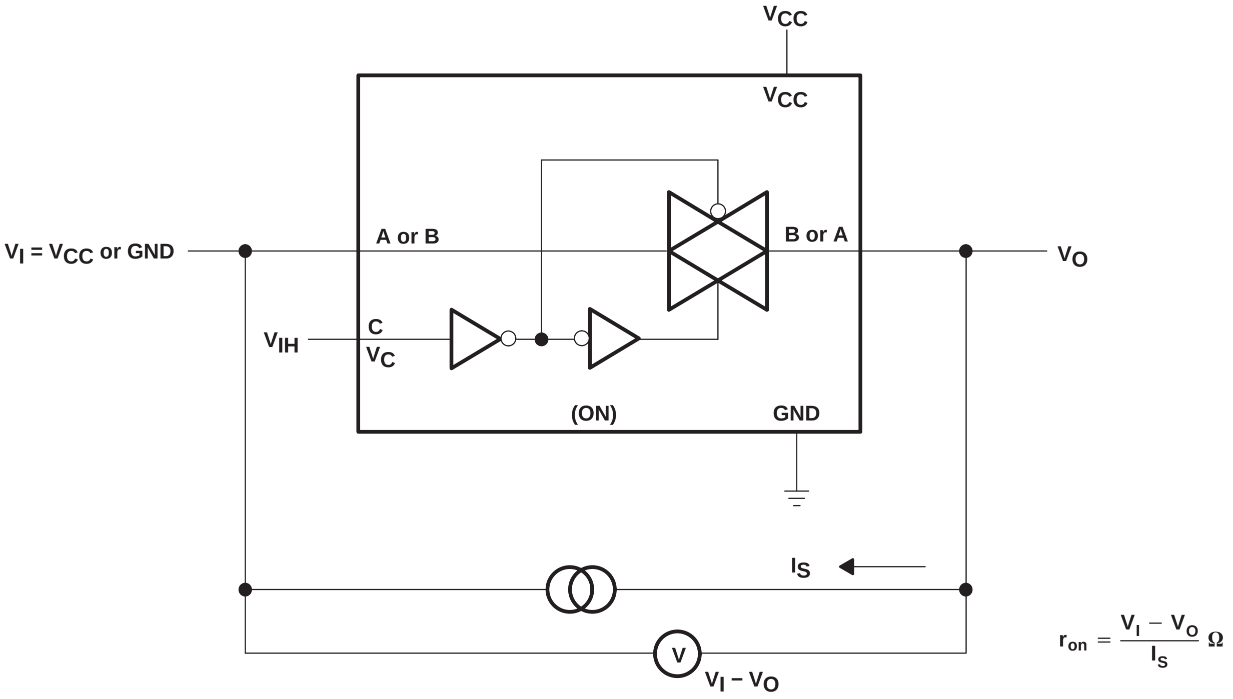

V_{CC}
V_{CC}
$V_I = V_{CC}$ or GND
A or B
B or A
V_O
V_{IH}
C
V_C
(ON)
GND
I_S
V
$V_I − V_O$
$r_{on} = \frac{V_I - V_O}{I_S}\ \Omega$

Figure 1. On-State Resistance Test Circuit

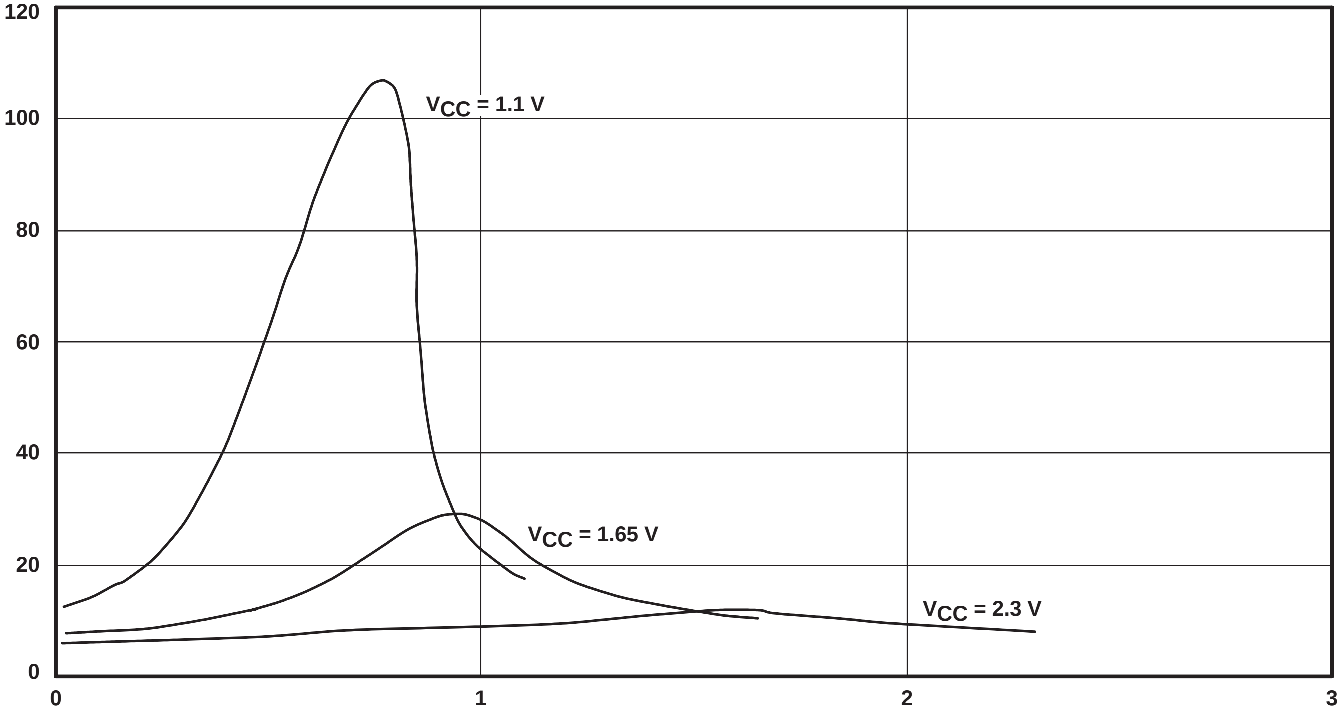


Figure 2. Typical r_{on} as a Function of Voltage (V_I) for V_I = 0 to V_{CC}

PARAMETER MEASUREMENT INFORMATION

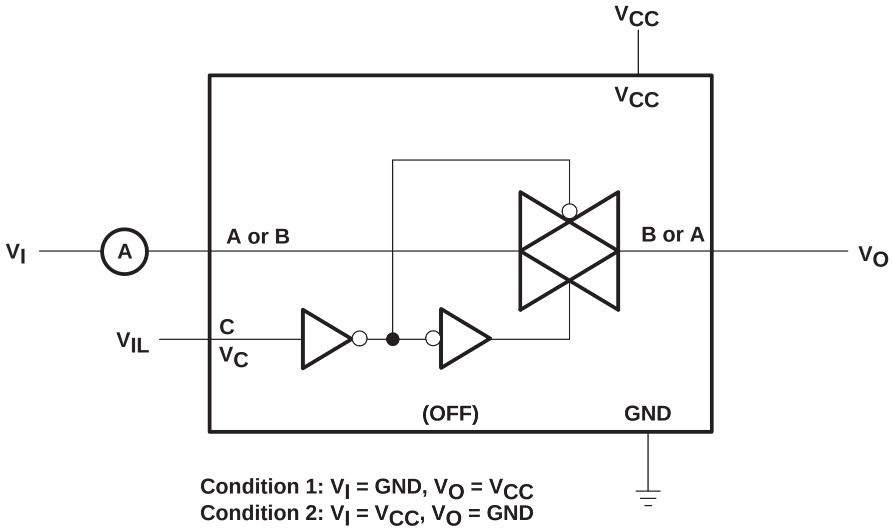

V_{CC}
V_{CC}
V_I
A
A or B
B or A
V_O
V_{IL}
C
V_C
(OFF)
GND
Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

Figure 3. Off-State Switch Leakage-Current Test Circuit

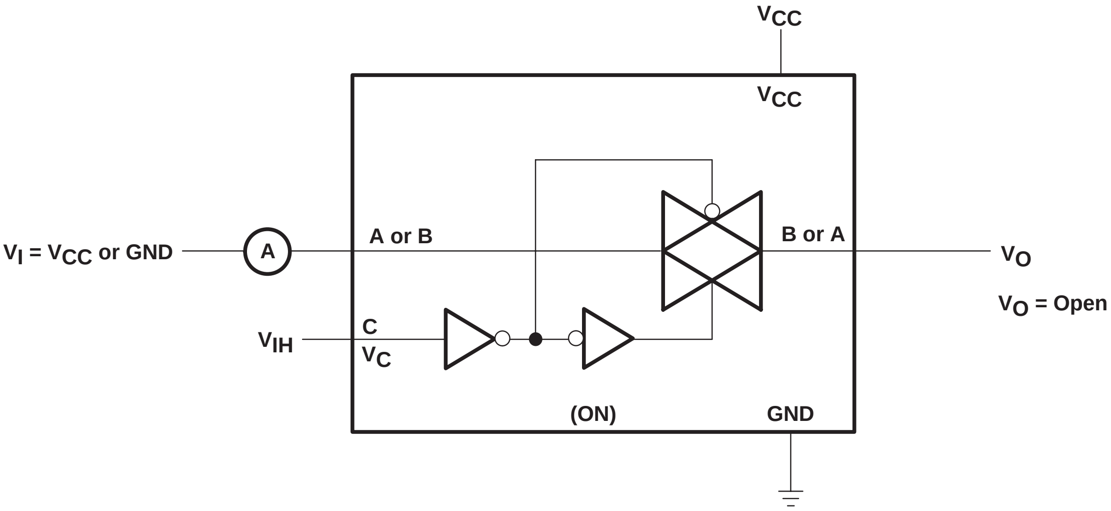
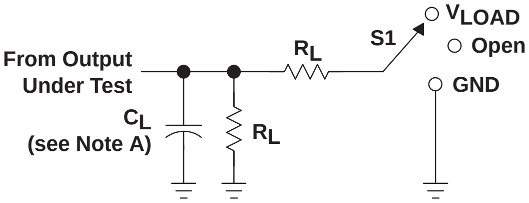

V_{CC}
V_{CC}
V_I = V_{CC} or GND
A
A or B
B or A
V_O
V_O = Open
V_{IH}
C
V_C
(ON)
GND

Figure 4. On-State Leakage-Current Test Circuit

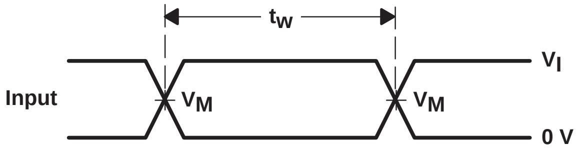
PARAMETER MEASUREMENT INFORMATION


From Output Under Test
C_L (see Note A)
R_L
R_L
S1
V_{LOAD}
Open
GND

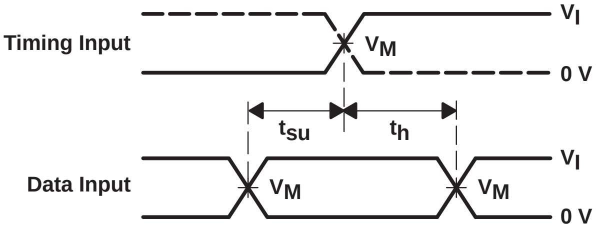
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

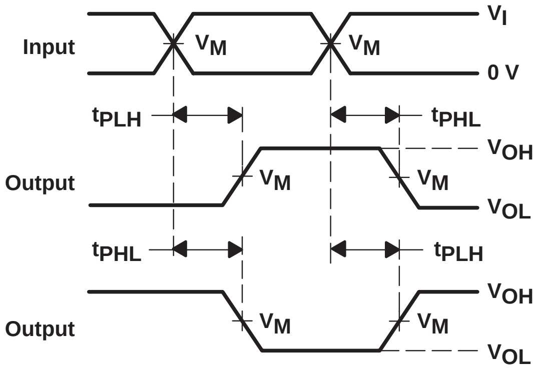
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
0.8 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.2 V ± 0.1 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.15 V
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V


t_w
Input
V_M
V_M
V_I
0 V

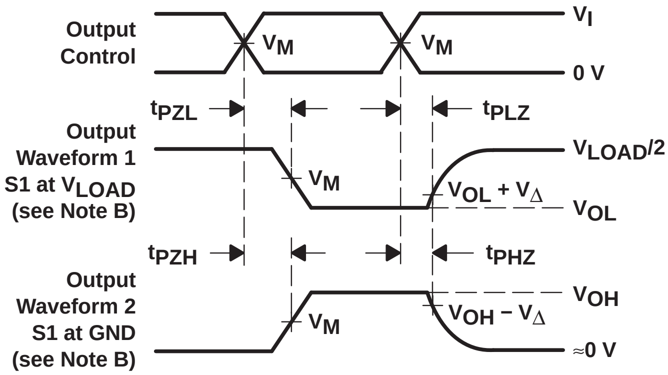
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
V_I
V_M
0 V
t_{su}
t_h
Data Input
V_I
V_M
V_M
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
V_I
V_M
V_M
0 V
t_{PLH}
t_{PHL}
Output
V_{OH}
V_M
V_M
V_{OL}
t_{PHL}
t_{PLH}
Output
V_{OH}
V_M
V_M
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output Control
V_I
V_M
V_M
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at V_{LOAD} (see Note B)
$V_{LOAD}/2$
V_M
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
V_{OH}
V_M
$V_{OH} - V_\Delta$
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

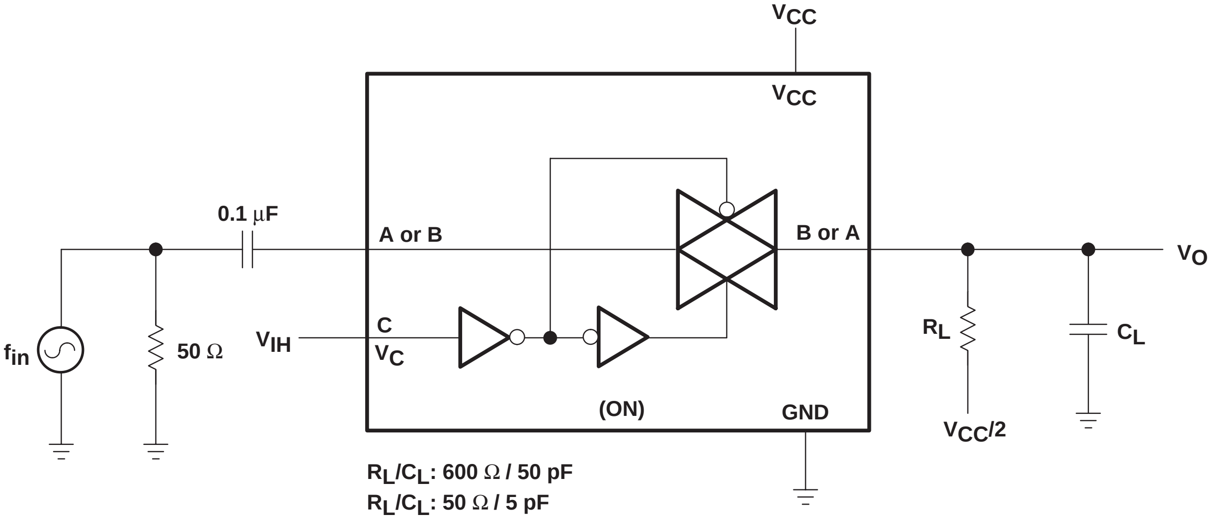

VCC
VCC
0.1 µF
A or B
B or A
VO
fin
50 Ω
VIH
C
VC
RL
CL
(ON)
GND
VCC/2
RL/CL: 600 Ω / 50 pF
RL/CL: 50 Ω / 5 pF

Figure 6. Frequency Response (Switch ON)

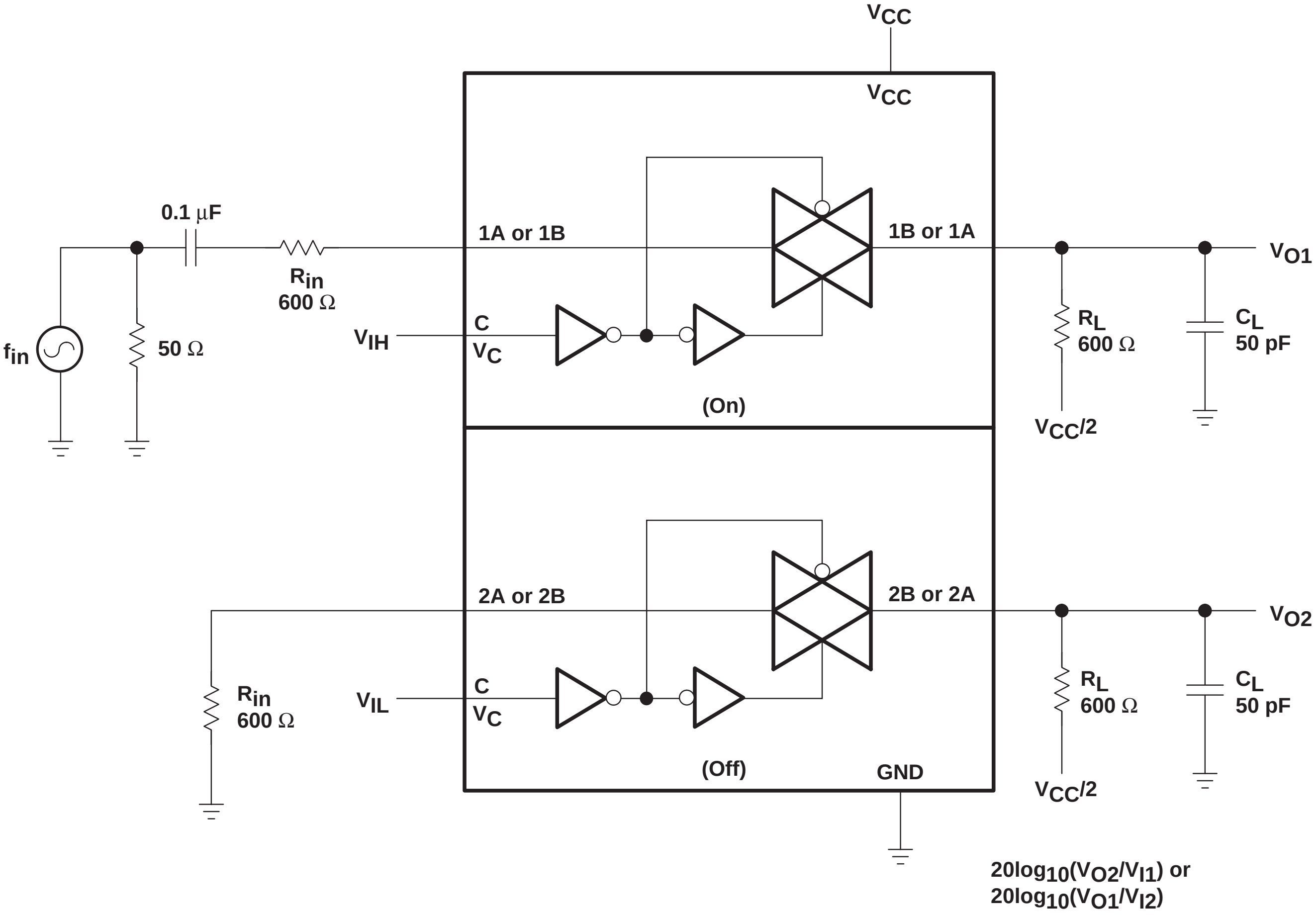

VCC
VCC
0.1 µF
Rin
600 Ω
1A or 1B
1B or 1A
VO1
fin
50 Ω
VIH
C
VC
RL
600 Ω
CL
50 pF
(On)
VCC/2
2A or 2B
2B or 2A
VO2
Rin
600 Ω
VIL
C
VC
RL
600 Ω
CL
50 pF
(Off)
GND
VCC/2
20log10(VO2/VI1) or
20log10(VO1/VI2)

Figure 7. Crosstalk (Between Switches)

PARAMETER MEASUREMENT INFORMATION

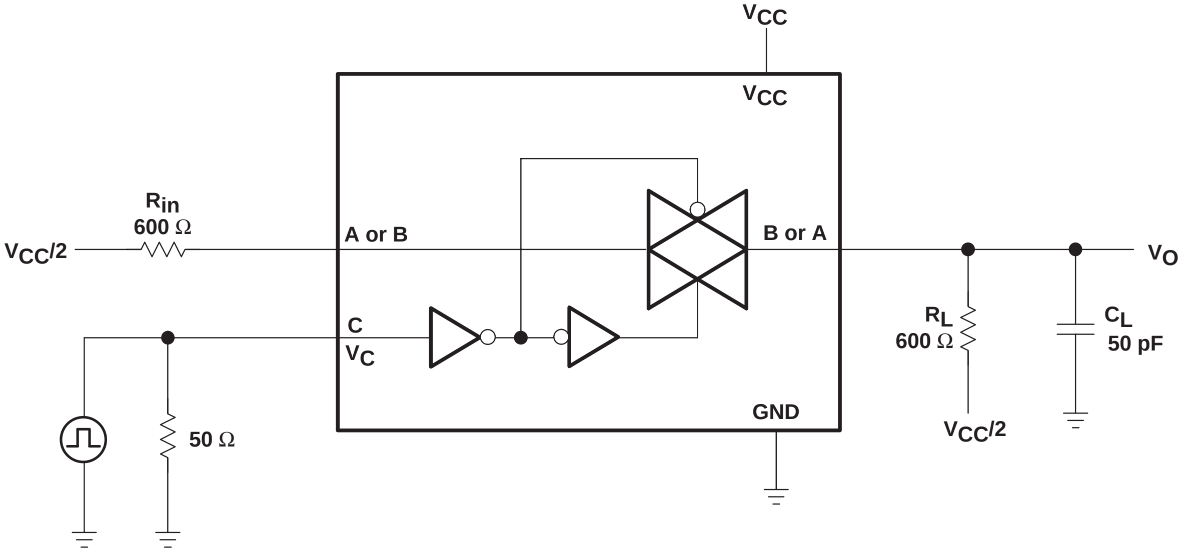
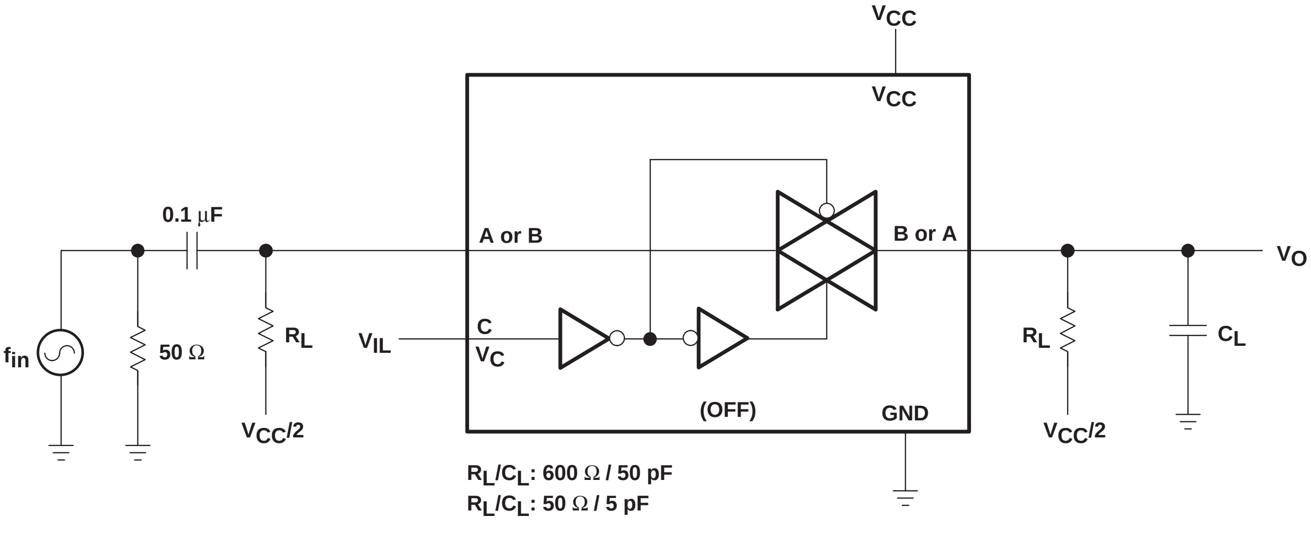

V_{CC}
V_{CC}
R_{in}
600 Ω
$V_{CC}/2$
A or B
B or A
V_O
C
V_C
R_L
600 Ω
C_L
50 pF
50 Ω
GND
$V_{CC}/2$

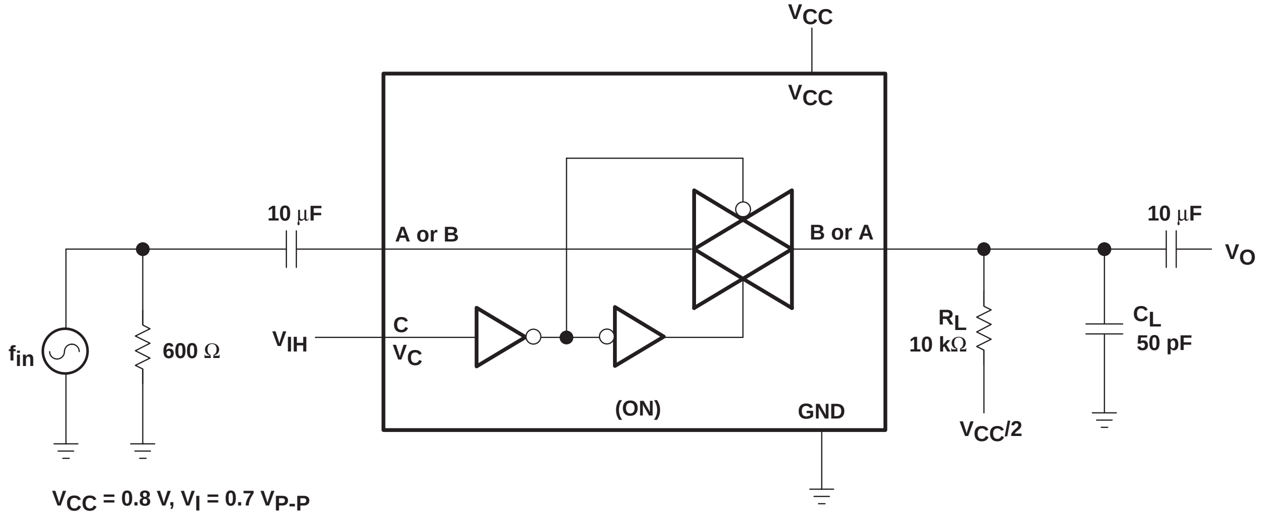
Figure 8. Crosstalk (Control Input − Switch Output)


V_{CC}
V_{CC}
0.1 µF
A or B
B or A
V_O
f_{in}
50 Ω
R_L
V_{IL}
C
V_C
R_L
C_L
(OFF)
GND
$V_{CC}/2$
$V_{CC}/2$

R_L/C_L: 600 Ω / 50 pF
R_L/C_L: 50 Ω / 5 pF

Figure 9. Feed Through, Switch Off

PARAMETER MEASUREMENT INFORMATION


V_{CC}
V_{CC}
10 μF
A or B
B or A
10 μF
V_O
f_{in}
600 Ω
V_{IH}
C
V_C
R_L
10 kΩ
C_L
50 pF
(ON)
GND
$V_{CC}/2$

V_{CC} = 0.8 V, V_I = 0.7 V_{P-P}
V_{CC} = 1.1 V, V_I = 1 V_{P-P}
V_{CC} = 1.4 V, V_I = 1.2 V_{P-P}
V_{CC} = 1.65 V, V_I = 1.4 V_{P-P}
V_{CC} = 2.3 V, V_I = 2 V_{P-P}

Figure 10. Sine-Wave Distortion

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TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS026C – Revised September 2003

CD4016B Types

CMOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

High-Voltage Types (20-Volt Rating)

■ CD4016B Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch on or off.

The CD4016 "B" Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

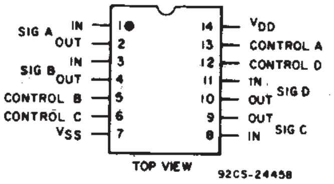
Features:

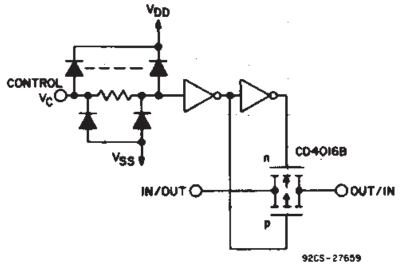
- **20-V digital or ± 10-V peak-to-peak switching**
- **280-Ω typical on-state resistance for 15-V operation**
- **Switch on-state resistance matched to within 10 Ω typ. over 15-V signal-input range**
- **High on/off output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ**
- **High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p}, $V_{DD}-V_{SS} \geqslant 10$ V, R_L = 10 kΩ**
- **Extremely low off-state switch leakage resulting in very low offset current and high effective off-state resistance: 100 pA typ. @ $V_{DD}-V_{SS}$=18 V, T_A=25°C**
- **Extremely high control input impedance (control circuit isolated from signal circuit: 10^{12} Ω typ.**
- **Low crosstalk between switches: –50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ**
- **Matched control-input to signal-output capacitance: Reduces output signal transients**
- **Frequency response, switch on = 40 MHz (typ.)**
- **100% tested for quiescent current at 20 V**
- **Maximum control input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V at 25°C**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

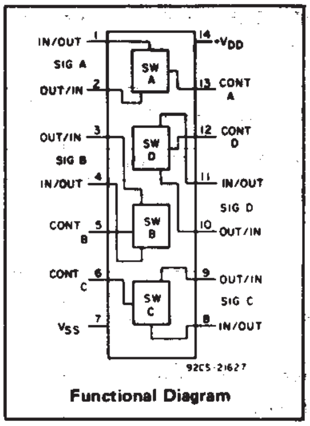
- **Analog signal switching/multiplexing**
  - **Signal gating**
  - **Squelch control**
  - **Chopper**
  - **Modulator**
  - **Demodulator**
  - **Commutating switch**
- **Digital signal switching/multiplexing**
- **CMOS logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**

Terminal Assignment





Schematic diagram - 1 of 4 identical sections.



Functional Diagram

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) .... –0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... –0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –55°C to +100°C 500mW
For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) .... –55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... –65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

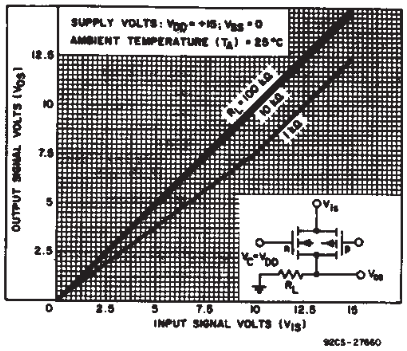


Fig. 1— Typ. on-state characteristics for 1 of 4 switches with V_{DD}=+15 V, V_{SS}=0 V.

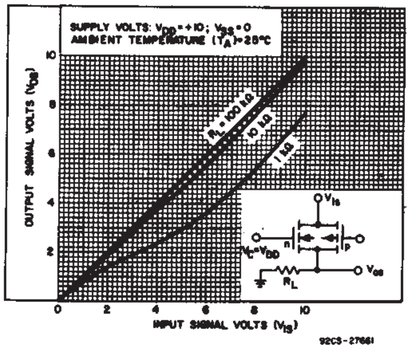


Fig. 2— Typ. on-state characteristics for 1 of 4 switches with V_{DD}=+10 V, V_{SS}=0 V.

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ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS
		V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25		
								Typ.	Max.	
Quiescent Device Current, I_{DD}		0,5	5	0.25	0.25	7.5	7.5	0.01	0.25	µA
		0,10	10	0.5	0.5	15	15	0.01	0.5	
		0,15	15	1	1	30	30	0.01	1	
		0,20	20	5	5	150	150	0.02	5	
Signal Inputs (V_{is}) and Output (V_{os})										
On-State Resistance, r_{on} Max.	$V_C = V_{DD}$ $R_L = 10k\Omega$ Returned to $\frac{V_{DD}-V_{SS}}{2}$ $V_{is}=V_{DD}$ or V_{SS}		10	600	610	840	960	–	660	Ω
	V_{is}=4.75 to 5.75 V		10	1870	1900	2380	2600	–	2000	
	$V_{is}=V_{DD}$ or V_{SS}		15	360	370	520	600	–	400	
	V_{is}=7.25 to 7.75 V		15	775	790	1080	1230	–	850	
ΔOn-State Resistance Between Any 2 Switches, Δr_{on}	$R_L = 10 k\Omega$, $V_C = V_{DD}$		5	–	–	–	–	15	–	Ω
			10	–	–	–	–	10	–	
			15	–	–	–	–	5	–	
Total Harmonic Distortion, THD	$V_C=V_{DD}$ = 5 V, V_{SS} = −5 V, $V_{is(p\text{-}p)}$ = 5 V (Sine wave centered on 0 V) R_L=10 kΩ, f_{is}=1 kHz sine wave			–	–	–	–	0.4	–	%
−3dB Cutoff Frequency (Switch on)	$V_C=V_{DD}$=5 V, V_{SS}=−5 V, $V_{is(p\text{-}p)}$ =5 V (Sine wave centered on 0 V) R_L = 1 kΩ,			–	–	–	–	40	–	MHz
−50dB Feed-through Frequency (Switch off)	$V_C=V_{SS}$= −5 V, $V_{is(p\text{-}p)}$=5 V (Sine wave centered on 0 V) R_L = 1 lkΩ			–	–	–	–	1.25	–	MHz
Input/Output Leakage Current (Switch off) I_{is} Max.	V_C = 0 V V_{is} = 18 V, V_{os} = 0 V; V_{is} = 0 V, V_{os} = 18 V		18	±0.1	±0.1	±1	±1	10^{-4}	±0.1	µA
−50 dB Crosstalk Frequency	$V_C(A) = V_{DD}$ = +5 V, $V_C(B) = V_{SS}$ = −5 V, $V_{is}(A)$ = 5 $V_{p\text{-}p}$, 50 Ω source R_L = 1 kΩ			–	–	–	–	0.9	–	MHz
Propagation Delay (Signal Input to Signal Output) t_{pd}	R_L = 200 kΩ $V_C = V_{DD}$, V_{SS} = GND, C_L = 50 pF V_{is} = Square Wave 0 to V_{DD} t_r, t_f = 20 ns		5	–	–	–	–	40	100	ns
			10	–	–	–	–	20	40	
			15	–	–	–	–	15	30	
Capacitance: Input, C_{is}	V_{DD} = +5 V $V_C = V_{SS}$ = −5 V			–	–	–	–	4	–	pF
Output, C_{os}				–	–	–	–	4	–	
Feedthrough, C_{ios}				–	–	–	–	0.2	–	

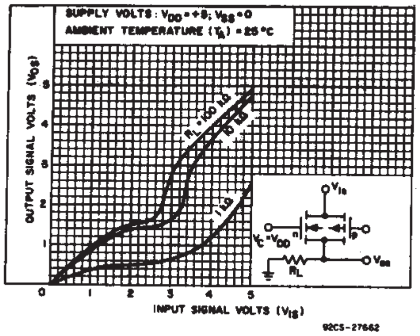


Fig. 3—Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = 0 V.

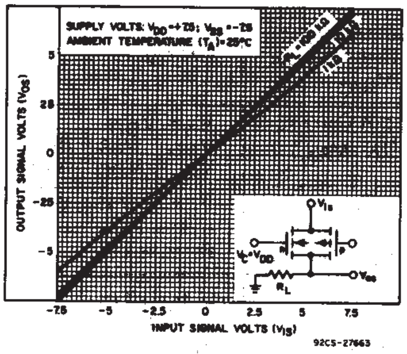


Fig. 4—Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +7.5 V, V_{SS} = −7.5 V.

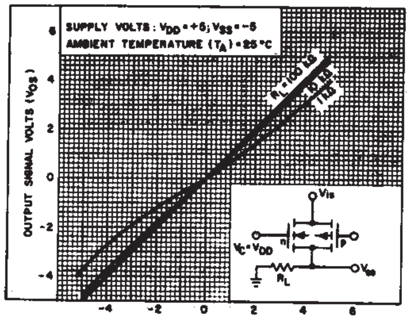


Fig. 5— Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = −5 V.

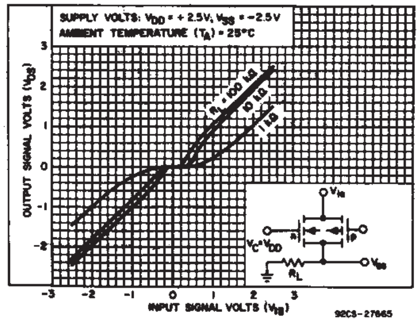


Fig. 6— Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +2.5 V, V_{SS} = −2.5 V.

ELECTRICAL CHARACTERISTICS (cont'd)

CHARACTERISTIC	TEST CONDITIONS		LIMITS AT INDICATED TEMPERATURES (°C)						UNITS
		V_{DD} (V)	−55	−40	+85	+125	+25 Typ.	+25 Max.	
Control (V_C)									
Control Input Low Voltage, V_{ILC} (Max.)	$\lvert I_{is}\rvert < 10\,\mu A$ $V_{is} = V_{SS}$, $V_{OS} = V_{DD}$ and $V_{is} = V_{DD}$, $V_{OS} = V_{SS}$	5,10, 15	0.9	0.9	0.4	0.4	–	0.7	V
Control Input High Voltage, V_{IHC}	See Fig. 10	5	3.5 (Min.)						V
		10	7 (Min.)						
		15	11 (Min.)						
Input Current, I_{IN} (Max.)	$V_{is} \leqslant V_{DD}$ $V_{DD} - V_{SS} = 18$ V $V_{CC} \leqslant V_{DD} - V_{SS}$	18	±0.1	±0.1	±1	±1	$\pm 10^{-5}$	±0.1	µA
Crosstalk (Control Input to Signal Output)	$V_C = 10$ V (Sq. Wave) t_r, $t_f = 20$ ns $R_L = 10$ kΩ	10	–	–	–	–	50	–	mV
Turn-On Propagation Delay	t_r, $t_f = 20$ ns $C_L = 50$ pF $R_L = 1$ kΩ	5	–	–	–	–	35	70	ns
		10	–	–	–	–	20	40	
		15	–	–	–	–	15	30	
Maximum Control Input Repetition Rate	$V_{is} = V_{DD}$, V_{SS} = GND, $R_L = 1$ kΩ to gnd, $C_L = 50$ pF, $V_C = 10$ V(Square wave centered on 5 V) t_r, $t_f = 20$ ns, $V_{os} = ½ V_{os}$ @ 1 kHz	10	–	–	–	–	10	–	MHz
Input Capacitance, C_{IN}			–	–	–	–	5	7.5	µF

V_{DD} (V)	Switch Input							Switch Output	
	V_{is} (V)	I_{is} (mA)						V_{os} (V)	
		−55°C	−40°C	25°C*	25°C▲	+85°C	+125°C	Min.	Max.
5	0	0.25	0.2	0.2	0.16	0.12	0.14	–	0.4
5	5	−0.25	−0.2	−0.2	−0.16	−0.12	−0.14	4.6	–
10	0	0.62	0.5	0.5	0.4	0.3	0.35	–	0.5
10	10	−0.62	−0.5	−0.5	−0.4	−0.3	−0.35	9.5	–
15	0	1.8	1.4	1.5	1.2	1	1.1	–	1.5
15	15	−1.8	−1.4	−1.5	−1.2	−1	−1.1	13.5	–

* Plastic package ▲ Ceramic package

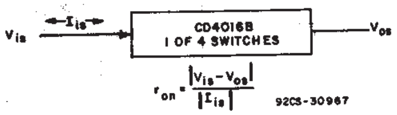


Fig. 10— Determination of r_{on} as a test condition for control input high voltage (V_{IHC}) specification.

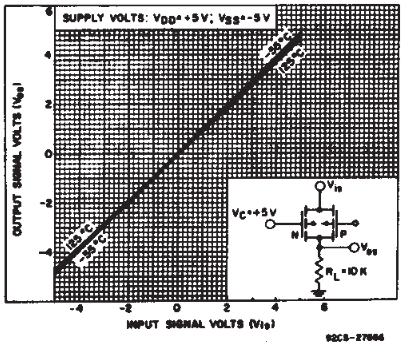


Fig. 7— Typ. on-state characteristics as a function of temp. for 1 of 4 switches with $V_{DD} = +5$ V, $V_{SS} = -5$ V.

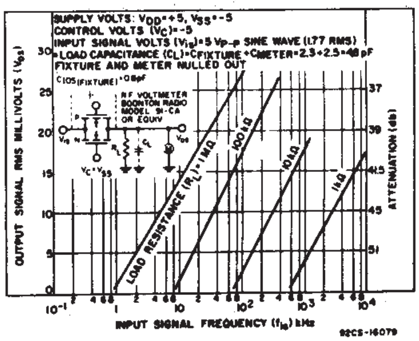


Fig. 8 – Typ. feedthru vs. frequency – switch off.

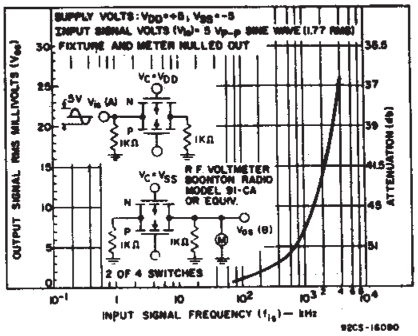


Fig. 9— Typical crosstalk between switch circuits in the same package.

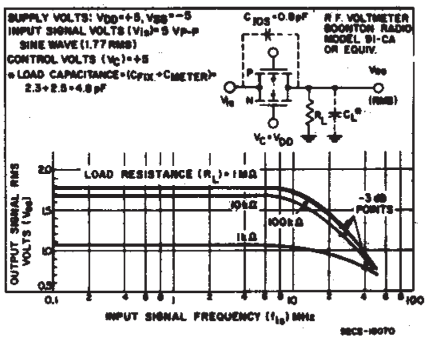


Fig. 11 – Typical frequency response – switch on.

TYPICAL ON-STATE RESISTANCE CHARACTERISTICS, $T_A = 25^oC$

CHARAC-TERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1kΩ		R_L = 10kΩ		R_L = 100kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)
r_{on}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
r_{on} (max.)	+15	0	300	+11	300	+9.3	320	+9.2
r_{on}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
r_{on} (max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
r_{on}	+ 5	0	860	+ 5	470	+ 5	450	+ 5
			600	0	580	0	800	0
r_{on} (max.)	+ 5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
r_{on}	+7.5	−7.5	200	+7.5	200	+7.5	180	+7.5
			200	−7.5	200	−7.5	180	−7.5
r_{on} (max.)	+7.5	−7.5	290	±0.25	280	±25	400	±0.25
r_{on}	+ 5	− 5	260	+ 5	250	+ 5	240	+ 5
			310	− 5	250	− 5	240	− 5
r_{on} (max.)	+ 5	− 5	600	±0.25	580	±0.25	760	±0.25
r_{on}	+2.5	−2.5	590	+2.5	450	+2.5	490	+2.5
			720	−2.5	520	−2.5	520	−2.5
r_{on} (max.)	+2.5	−2.5	232k	±0.25	300k	±0.25	870k	±0.25

* Variation from aperfect switch, r_{on} = 0 Ω.

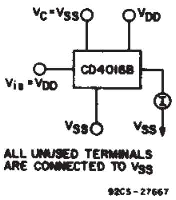

$V_C = V_{SS}$
V_{DD}
CD4016B
$V_{is} = V_{DD}$
I
V_{SS}
V_{SS}
ALL UNUSED TERMINALS ARE CONNECTED TO V_{SS}
92CS-27667

Fig. 12 – Off-state switch input or output leakage current test circuit.

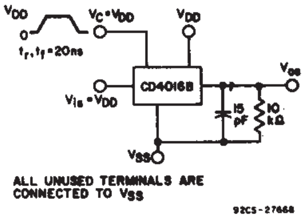
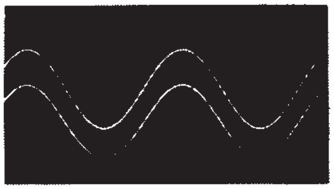

V_{DD}
0
$t_r, t_f = 20ns$
$V_C = V_{DD}$
V_{DD}
CD4016B
$V_{is} = V_{DD}$
V_{os}
15 pF
10 kΩ
V_{SS}
ALL UNUSED TERMINALS ARE CONNECTED TO V_{SS}
92CS-27668

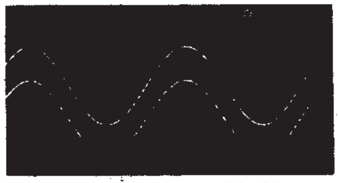
Fig. 13 – Test circuit for square-wave response.



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
$V_{DD} = V_C = +7.5V, V_{SS} = -7.5V, R_L = 10KΩ$
C_L = 15 pF
f_{IS} = 1 KHz V_{IS} = 5V p-p
DISTORTION = 0.2 %

92CS-27612

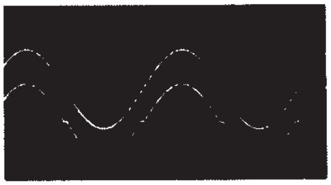
Fig. 14 – Typical sine wave response of V_{DD} = +7.5 V, V_{SS} = −7.5 V.



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
$V_{DD} = V_C = +5 V, V_{SS} = -5 V, R_L = 10KΩ$
C_L = 15 pF
f_{IS} = 1 KHz V_{IS} = 5 V p-p
DISTORTION = 0.4 %

92CS-27613

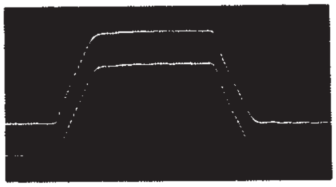
Fig. 15 – Typical sine wave response of V_{DD} = +5 V, V_{SS} = −5 V.



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV
$V_{DD} = V_C = +2.5V, V_{SS} = -2.5V, R_L = 10KΩ$
C_L = 15 pF
f_{IS} = 1 KHz V_{IS} = 5V p-p
DISTORTION = 3 %

92CS-27614

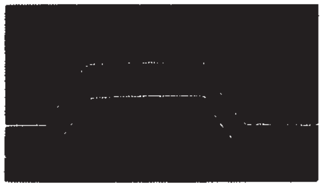
Fig. 16 – Typical sine wave response of V_{DD} = +2.5 V, V_{SS} = −2.5 V.



SCALE: X = 100 ns/DIV
Y = 5.0 V/DIV

92CS-27615

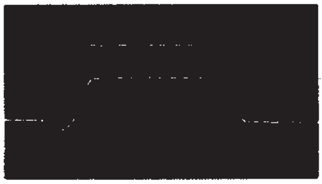
Fig. 17 – Typical square wave response at $V_{DD} = V_C$ = +15 V, V_{SS} = Gnd.



SCALE: X = 100 ns/DIV
Y = 5.0 V/DIV

92CS-27616

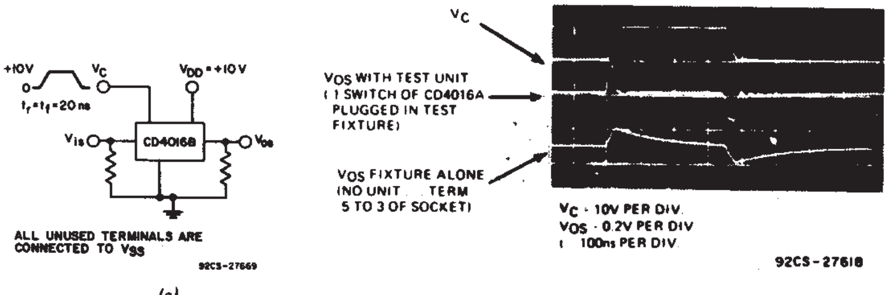
Fig. 18 – Typical square wave response at $V_{DD} = V_C$ = +10 V, V_{SS} = Gnd.



SCALE: X = 100 ns/DIV
Y = 2 V/DIV

92CS-27617

Fig. 19 – Typical square wave response at $V_{DD} = V_C$ = +5 V, V_{SS} = Gnd.


+10V
0
$t_r = t_f = 20$ ns
V_C
$V_{DD} = +10V$
V_{is}
CD4016B
V_{os}
ALL UNUSED TERMINALS ARE CONNECTED TO V_{SS}
92CS-27669
V_C
V_{OS} WITH TEST UNIT (1 SWITCH OF CD4016A PLUGGED IN TEST FIXTURE)
V_{OS} FIXTURE ALONE (NO UNIT TERM 5 TO 3 OF SOCKET)
V_C - 10V PER DIV.
V_{OS} - 0.2V PER DIV
t 100ns PER DIV
92CS-27618

(a) *(b)*

Fig.20 – Crosstalk-control input to signal output.

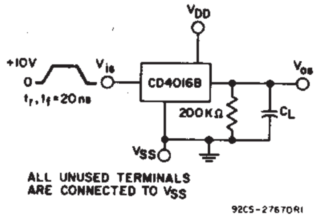

V_{DD}
+10V
0
$t_r, t_f = 20$ ns
V_{is}
CD4016B
V_{os}
200KΩ
C_L
V_{SS}
ALL UNUSED TERMINALS ARE CONNECTED TO V_{SS}
92CS-27670R1

Fig.21 – Propagation delay time signal input (V_{IS}) to signal output (V_{OS}).

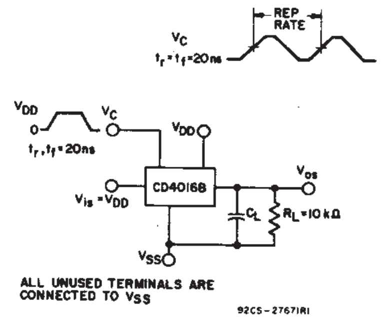
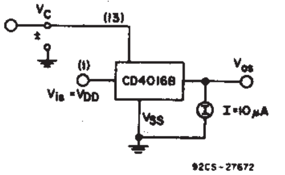

REP RATE
V_C
$t_r = t_f = 20$ ns
V_{DD}
0
V_C
$t_r, t_f = 20$ ns
V_{DD}
CD4016B
$V_{is} = V_{DD}$
V_{os}
C_L
$R_L = 10$ kΩ
V_{SS}
ALL UNUSED TERMINALS ARE CONNECTED TO V_{SS}
92CS-27671R1

Fig. 22 – Max. control-input repetition rate.


V_C
(13)
±
(1)
$V_{is} = V_{DD}$
CD4016B
V_{os}
V_{SS}
$I = 10\mu A$
92CS-27672

SWITCH THRESHOLD VOLTAGE IS DEFINED AS THE VOLTAGE APPLIED TO A TRANSMISSION GATE CONTROL WHICH CAUSES 10 µA OF TRANSMISSION GATE CURRENT.

Fig.23 – Switch threshold voltage.

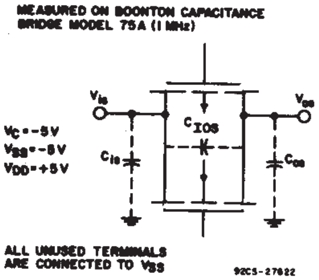

MEASURED ON BOONTON CAPACITANCE BRIDGE MODEL 75A (1 MHz)
V_{is}
V_{os}
C_{IOS}
$V_C = -5V$
$V_{SS} = -5V$
$V_{DD} = +5V$
C_{is}
C_{os}
ALL UNUSED TERMINALS ARE CONNECTED TO V_{SS}
92CS-27622

Fig.24 – Capacitance C_{IOS} and C_{OS}.

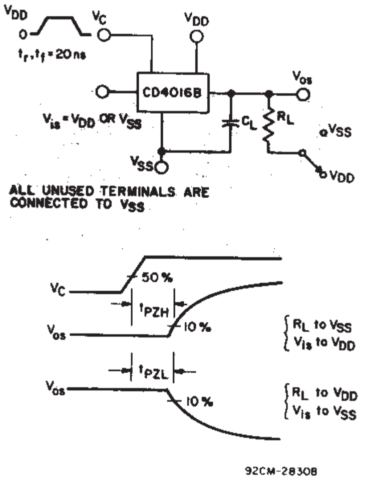
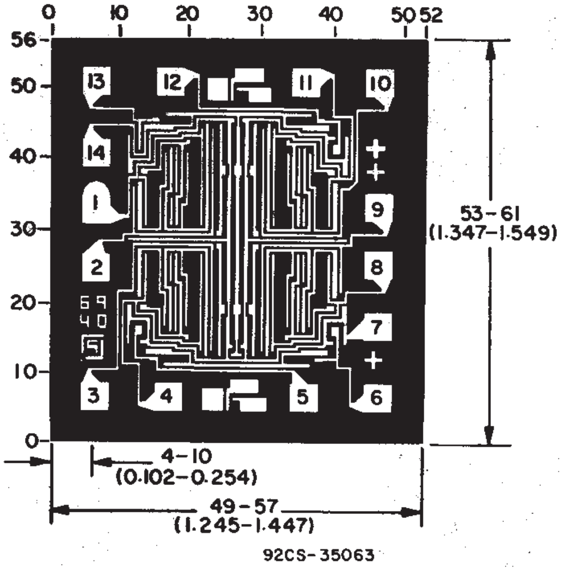

V_{DD}
0
V_C
$t_r, t_f = 20$ ns
V_{DD}
CD4016B
$V_{is} = V_{DD}$ OR V_{SS}
V_{os}
C_L
R_L
V_{SS}
V_{DD}
V_{SS}
ALL UNUSED TERMINALS ARE CONNECTED TO V_{SS}
V_C
50%
t_{PZH}
V_{os}
10%
R_L to V_{SS}
V_{is} to V_{DD}
t_{PZL}
V_{os}
10%
R_L to V_{DD}
V_{is} to V_{SS}
92CM-28308

Fig.25 – Turn-On propagation delay-control input.

Dimensions and pad layout for CD4016BH


0
10
20
30
40
50
52
56
50
40
30
20
10
0
13
12
11
10
14
1
9
2
8
7
3
4
5
6
53–61
(1.347–1.549)
4–10
(0.102–0.254)
49–57
(1.245–1.447)
92CS-35063

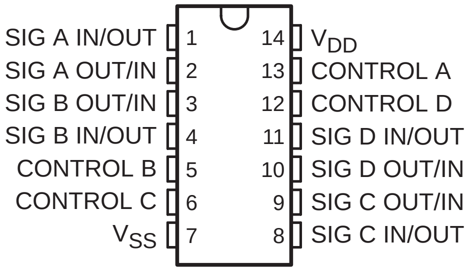
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CD4066B
CMOS QUAD BILATERAL SWITCH

SCHS051D − NOVEMBER 1998 − REVISED SEPTEMBER 2003

- **15-V Digital or ±7.5-V Peak-to-Peak Switching**
- **125-Ω Typical On-State Resistance for 15-V Operation**
- **Switch On-State Resistance Matched to Within 5 Ω Over 15-V Signal-Input Range**
- **On-State Resistance Flat Over Full Peak-to-Peak Signal Range**
- **High On/Off Output-Voltage Ratio: 80 dB Typical at f_{is} = 10 kHz, R_L = 1 kΩ**
- **High Degree of Linearity: <0.5% Distortion Typical at f_{is} = 1 kHz, V_{is} = 5 V p-p, $V_{DD} - V_{SS} \geq 10$ V, R_L = 10 kΩ**
- **Extremely Low Off-State Switch Leakage, Resulting in Very Low Offset Current and High Effective Off-State Resistance: 10 pA Typical at $V_{DD} - V_{SS}$ = 10 V, T_A = 25°C**
- **Extremely High Control Input Impedance (Control Circuit Isolated From Signal Circuit): 10^{12} Ω Typical**
- **Low Crosstalk Between Switches: −50 dB Typical at f_{is} = 8 MHz, R_L = 1 kΩ**
- **Matched Control-Input to Signal-Output Capacitance: Reduces Output Signal Transients**
- **Frequency Response, Switch On = 40 MHz Typical**
- **100% Tested for Quiescent Current at 20 V**
- **5-V, 10-V, and 15-V Parametric Ratings**
- **Meets All Requirements of JEDEC Tentative Standard No. 13-B, *Standard Specifications for Description of "B" Series CMOS Devices***
- **Applications:**
  - **Analog Signal Switching/Multiplexing: Signal Gating, Modulator, Squelch Control, Demodulator, Chopper, Commutating Switch**
  - **Digital Signal Switching/Multiplexing**
  - **Transmission-Gate Logic Implementation**
  - **Analog-to-Digital and Digital-to-Analog Conversion**
  - **Digital Control of Frequency, Impedance, Phase, and Analog-Signal Gain**

E, F, M, NS, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full signal-input range.

The CD4066B consists of four bilateral switches, each with independent controls. Both the p and the n devices in a given switch are biased on or off simultaneously by the control signal. As shown in Figure 1, the well of the n-channel device on each switch is tied to either the input (when the switch is on) or to V_{SS} (when the switch is off). This configuration eliminates the variation of the switch-transistor threshold voltage with input signal and, thus, keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage and more constant on-state impedance over the input-signal range. However, for sample-and-hold applications, the CD4016B is recommended.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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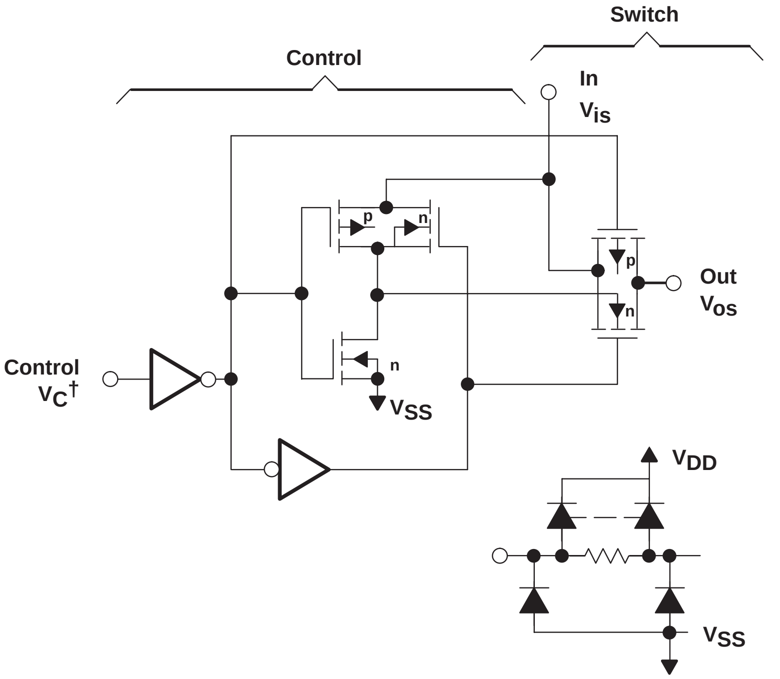
description/ordering information (continued)

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	CDIP − F	Tube of 25	CD4066BF3A	CD4066BF3A
	PDIP − E	Tube of 25	CD4066BE	CD4066BE
	SOIC − M	Tube of 50	CD4066BM	CD4066BM
		Reel of 2500	CD4066BM96	
		Reel of 250	CD4066BMT	
	SOP − NS	Reel of 2000	CD4066BNSR	CD4066B
	TSSOP − PW	Tube of 90	CD4066BPW	CM066B
		Reel of 2000	CD4066BPWR	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



[†] All control inputs are protected by the CMOS protection network.

NOTES: A. All p substrates are connected to V_{DD}.
B. Normal operation control-line biasing: switch on (logic 1), $V_C = V_{DD}$; switch off (logic 0), $V_C = V_{SS}$
C. Signal-level range: $V_{SS} \le V_{is} \le V_{DD}$

92CS-29113

Figure 1. Schematic Diagram of One-of-Four Identical Switches and Associated Control Circuitry

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

DC supply-voltage range, V_{DD} (voltages referenced to V_{SS} terminal) . . . . −0.5 V to 20 V
Input voltage range, V_{is} (all inputs) . . . . −0.5 V to V_{DD} + 0.5 V
DC input current, I_{IN} (any one input) . . . . ±10 mA
Package thermal impedance, θ_{JA} (see Note 1): E package . . . . 80°C/W
M package . . . . 86°C/W
NS package . . . . 76°C/W
PW package . . . . 113°C/W
Lead temperature (during soldering):
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max . . . . 265°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	3	18	V
T_A	Operating free-air temperature	−55	125	°C

electrical characteristics

PARAMETER		TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES						UNIT
			V_{IN} (V)	V_{DD} (V)	−55°C	−40°C	85°C	125°C	25°C		
									TYP	MAX	
I_{DD}	Quiescent device current		0, 5	5	0.25	0.25	7.5	7.5	0.01	0.25	µA
			0, 10	10	0.5	0.5	15	15	0.01	0.5	
			0, 15	15	1	1	30	30	0.01	1	
			0, 20	20	5	5	150	150	0.02	5	
Signal Inputs (V_{is}) and Outputs (V_{os})											
r_{on}	On-state resistance (max)	$V_C = V_{DD}$, R_L = 10 kΩ returned to $\frac{(V_{DD} - V_{SS})}{2}$, $V_{is} = V_{SS}$ to V_{DD}		5	800	850	1200	1300	470	1050	Ω
				10	310	330	500	550	180	400	
				15	200	210	300	320	125	240	
Δr_{on}	On-state resistance difference between any two switches	R_L = 10 kΩ, $V_C = V_{DD}$		5					15		Ω
				10					10		
				15					5		
THD	Total harmonic distortion	$V_C = V_{DD}$ = 5 V, V_{SS} = −5 V, $V_{is(p\text{-}p)}$ = 5 V (sine wave centered on 0 V), R_L = 10 kΩ, f_{is} = 1-kHz sine wave							0.4		%
	−3-dB cutoff frequency (switch on)	$V_C = V_{DD}$ = 5 V, V_{SS} = −5 V, $V_{is(p\text{-}p)}$ = 5 V (sine wave centered on 0 V), R_L = 1 kΩ							40		MHz
	−50-dB feedthrough frequency (switch off)	$V_C = V_{SS}$ = −5 V, $V_{is(p\text{-}p)}$ = 5 V (sine wave centered on 0 V), R_L = 1 kΩ							1		MHz
I_{is}	Input/output leakage current (switch off) (max)	V_C = 0 V, V_{is} = 18 V, V_{os} = 0 V; and V_C = 0 V, V_{is} = 0 V, V_{os} = 18 V		18	±0.1	±0.1	±1	±1	$\pm10^{-5}$	±0.1	µA
	−50-dB crosstalk frequency	$V_C(A) = V_{DD}$ = 5 V, $V_C(B) = V_{SS}$ = −5 V, $V_{is}(A)$ = 5 $V_{p\text{-}p}$, 50-Ω source, R_L = 1 kΩ							8		MHz
t_{pd}	Propagation delay (signal input to signal output)	R_L = 200 kΩ, $V_C = V_{DD}$, V_{SS} = GND, C_L = 50 pF, V_{is} = 10 V (square wave centered on 5 V), t_r, t_f = 20 ns		5					20	40	ns
				10					10	20	
				15					7	15	
C_{is}	Input capacitance	V_{DD} = 5 V, $V_C = V_{SS}$ = −5 V							8		pF
C_{os}	Output capacitance	V_{DD} = 5 V, $V_C = V_{SS}$ = −5 V							8		pF
C_{ios}	Feedthrough	V_{DD} = 5 V, $V_C = V_{SS}$ = −5 V							0.5		pF

electrical characteristics (continued)

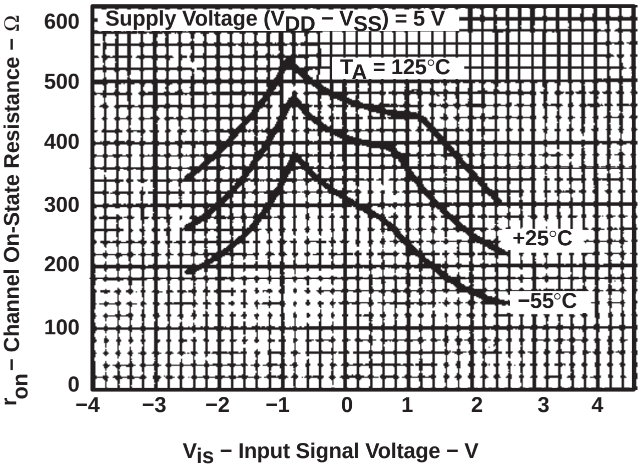
CHARACTERISTIC		TEST CONDITIONS	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES						UNIT
				−55°C	−40°C	85°C	125°C	25°C		
								TYP	MAX	
Control (V_C)										
V_{ILC}	Control input, low voltage (max)	$\lvert I_{is} \rvert$ < 10 µA, $V_{is} = V_{SS}$, $V_{OS} = V_{DD}$, and $V_{is} = V_{DD}$, $V_{OS} = V_{SS}$	5	1	1	1	1		1	V
			10	2	2	2	2		2	
			15	2	2	2	2		2	
V_{IHC}	Control input, high voltage	See Figure 6	5	3.5 (MIN)						V
			10	7 (MIN)						
			15	11 (MIN)						
I_{IN}	Input current (max)	$V_{is} \leq V_{DD}$, $V_{DD} - V_{SS}$ = 18 V, $V_{CC} \leq V_{DD} - V_{SS}$	18	±0.1	±0.1	±1	±1	$\pm 10^{-5}$	±0.1	µA
	Crosstalk (control input to signal output)	V_C = 10 V (square wave), t_r, t_f = 20 ns, R_L = 10 kΩ	10					50		mV
	Turn-on and turn-off propagation delay	$V_{IN} = V_{DD}$, t_r, t_f = 20 ns, C_L = 50 pF, R_L = 1 kΩ	5					35	70	ns
			10					20	40	
			15					15	30	
	Maximum control input repetition rate	$V_{is} = V_{DD}$, V_{SS} = GND, R_L = 1 kΩ to GND, C_L = 50 pF, V_C = 10 V (square wave centered on 5 V), t_r, t_f = 20 ns, V_{OS} = 1/2 V_{OS} at 1 kHz	5					6		MHz
			10					9		
			15					9.5		
C_I	Input capacitance							5	7.5	pF

switching characteristics

V_{DD} (V)	SWITCH INPUT						SWITCH OUTPUT, V_{OS} (V)	
	V_{is} (V)	I_{is} (mA)						
		−55°C	−40°C	25°C	85°C	125°C	MIN	MAX
5	0	0.64	0.61	0.51	0.42	0.36		0.4
5	5	−0.64	−0.61	−0.51	−0.42	−0.36	4.6	
10	0	1.6	1.5	1.3	1.1	0.9		0.5
10	10	−1.6	−1.5	−1.3	−1.1	−0.9	9.5	
15	0	4.2	4	3.4	2.8	2.4		1.5
15	15	−4.2	−4	−3.4	−2.8	−2.4	13.5	

TYPICAL CHARACTERISTICS

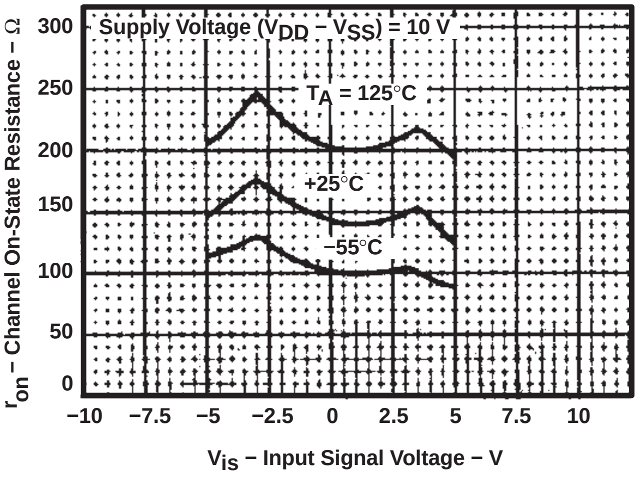
TYPICAL ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)



92CS-27326RI

Figure 2

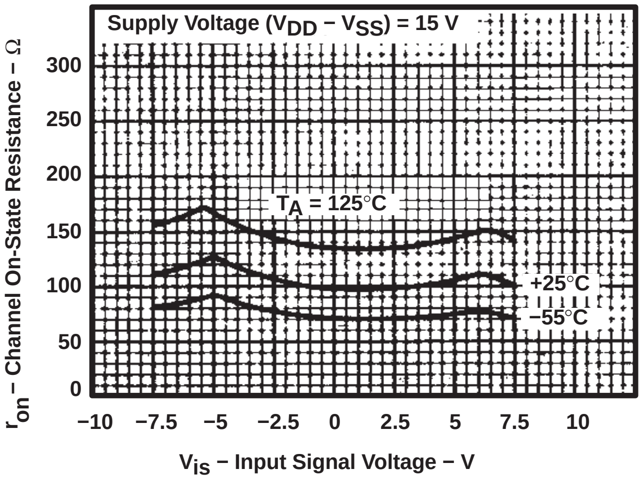
TYPICAL ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)



92CS-27327RI

Figure 3

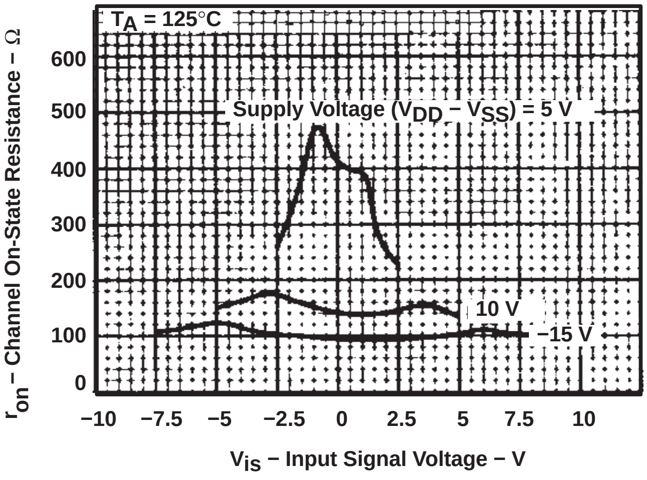
TYPICAL ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)



92CS-27329RI

Figure 4

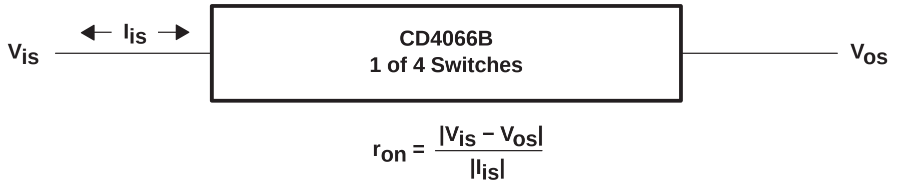
TYPICAL ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)



92CS-27330RI

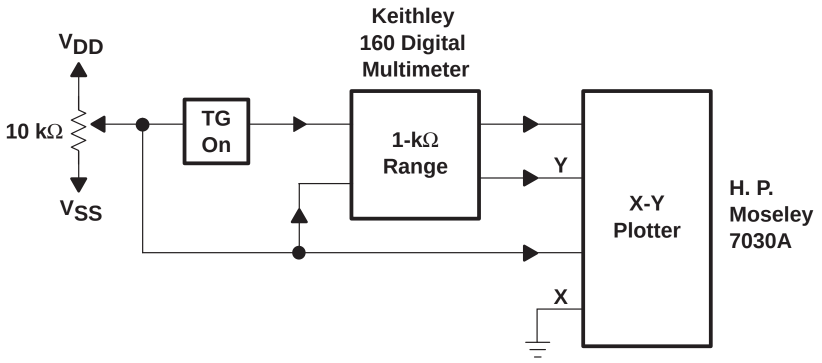
Figure 5

TYPICAL CHARACTERISTICS


I_{is}
V_{is}
CD4066B
1 of 4 Switches
V_{os}
$r_{on} = \frac{|V_{is} - V_{os}|}{|I_{is}|}$

92CS-30966

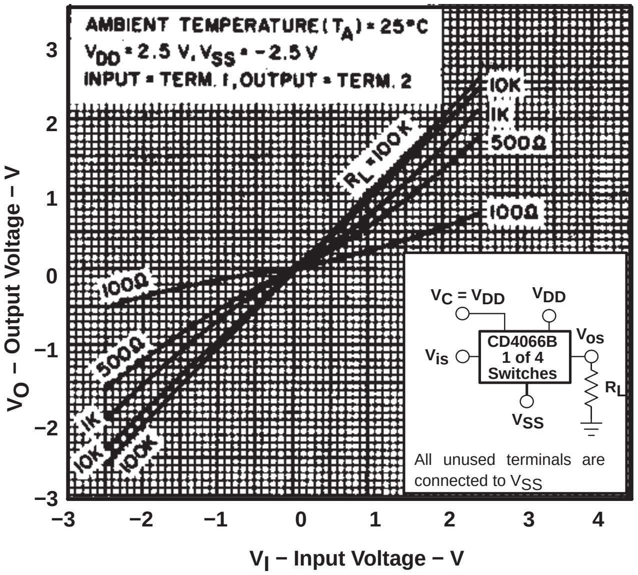
Figure 6. Determination of r_{on} as a Test Condition for Control-Input High-Voltage (V_{IHC}) Specification


Keithley
160 Digital
Multimeter
V_{DD}
10 kΩ
V_{SS}
TG
On
1-kΩ
Range
Y
X
X-Y
Plotter
H. P.
Moseley
7030A

92CS-22716

Figure 7. Channel On-State Resistance Measurement Circuit

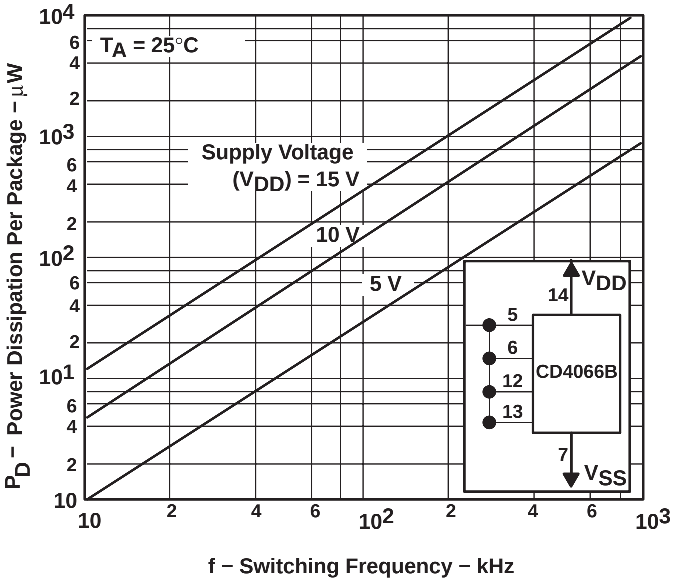
TYPICAL ON CHARACTERISTICS
FOR 1 OF 4 CHANNELS



92CS-30919

Figure 8

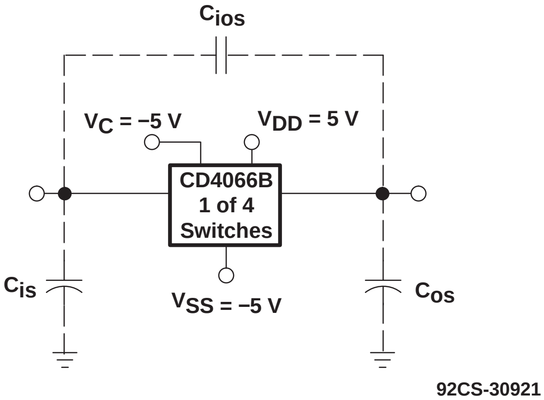
POWER DISSIPATION PER PACKAGE
vs
SWITCHING FREQUENCY



92C-30920

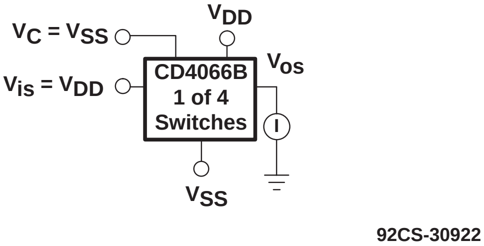
Figure 9

TYPICAL CHARACTERISTICS


C_{ios}
$V_C = -5$ V
$V_{DD} = 5$ V
CD4066B
1 of 4
Switches
C_{is}
$V_{SS} = -5$ V
C_{os}
92CS-30921

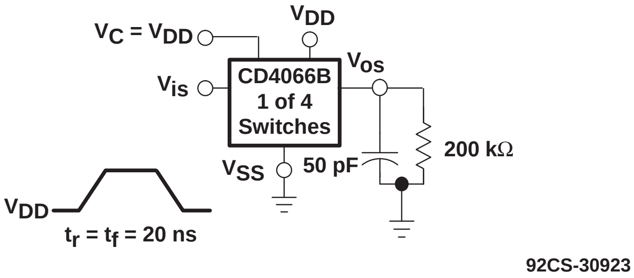
Measured on Boonton capacitance bridge, model 75a (1 MHz); test-fixture capacitance nulled out.

Figure 10. Typical On Characteristics for One of Four Channels


V_{DD}
$V_C = V_{SS}$
V_{os}
$V_{is} = V_{DD}$
CD4066B
1 of 4
Switches
I
V_{SS}
92CS-30922

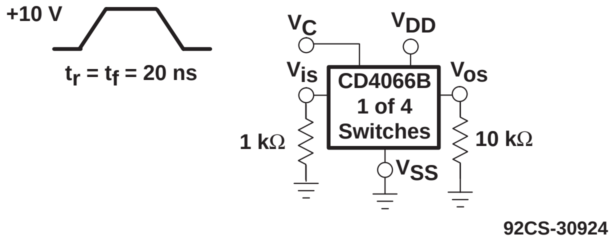
All unused terminals are connected to V_{SS}.

Figure 11. Off-Switch Input or Output Leakage


V_{DD}
$V_C = V_{DD}$
V_{os}
V_{is}
CD4066B
1 of 4
Switches
200 kΩ
V_{SS}
50 pF
V_{DD}
$t_r = t_f = 20$ ns
92CS-30923

All unused terminals are connected to V_{SS}.

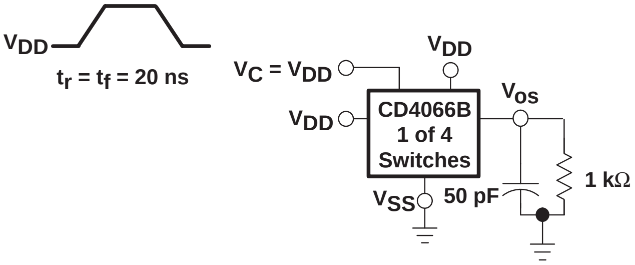
Figure 12. Propagation Delay Time Signal Input (V_{is}) to Signal Output (V_{os})


+10 V
$t_r = t_f = 20$ ns
V_C
V_{DD}
V_{is}
V_{os}
CD4066B
1 of 4
Switches
1 kΩ
10 kΩ
V_{SS}
92CS-30924

All unused terminals are connected to V_{SS}.

Figure 13. Crosstalk-Control Input to Signal Output

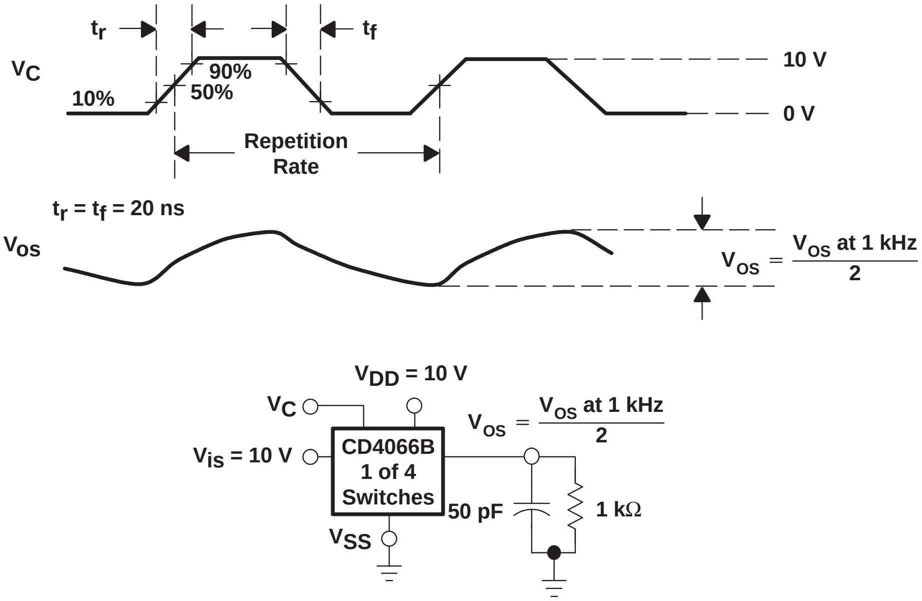
TYPICAL CHARACTERISTICS


VDD
tr = tf = 20 ns
VC = VDD
VDD
VDD
CD4066B
1 of 4
Switches
VOS
VSS
50 pF
1 kΩ

NOTES: A. All unused terminals are connected to V_{SS}.
B. Delay is measured at V_{OS} level of +10% from ground (turn-on) or on-state output level (turn-off).

92CS-30925

Figure 14. Propagation Delay, t_{PLH}, t_{PHL} Control-Signal Output

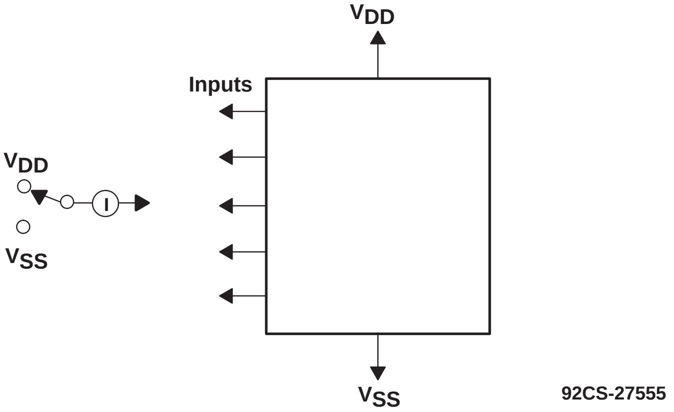

tr
tf
VC
90%
50%
10%
10 V
0 V
Repetition
Rate
tr = tf = 20 ns
VOS
VOS = VOS at 1 kHz / 2
VDD = 10 V
VC
Vis = 10 V
CD4066B
1 of 4
Switches
VOS = VOS at 1 kHz / 2
50 pF
1 kΩ
VSS

All unused terminals are connected to V_{SS}.

92CS-30925

Figure 15. Maximum Allowable Control-Input Repetition Rate

TYPICAL CHARACTERISTICS


VDD
Inputs
VDD
I
VSS
VSS
92CS-27555

Measure inputs sequentially to both V_{DD} and V_{SS}. Connect all unused inputs to either V_{DD} or V_{SS}. Measure control inputs only.

Figure 16. Input Leakage-Current Test Circuit

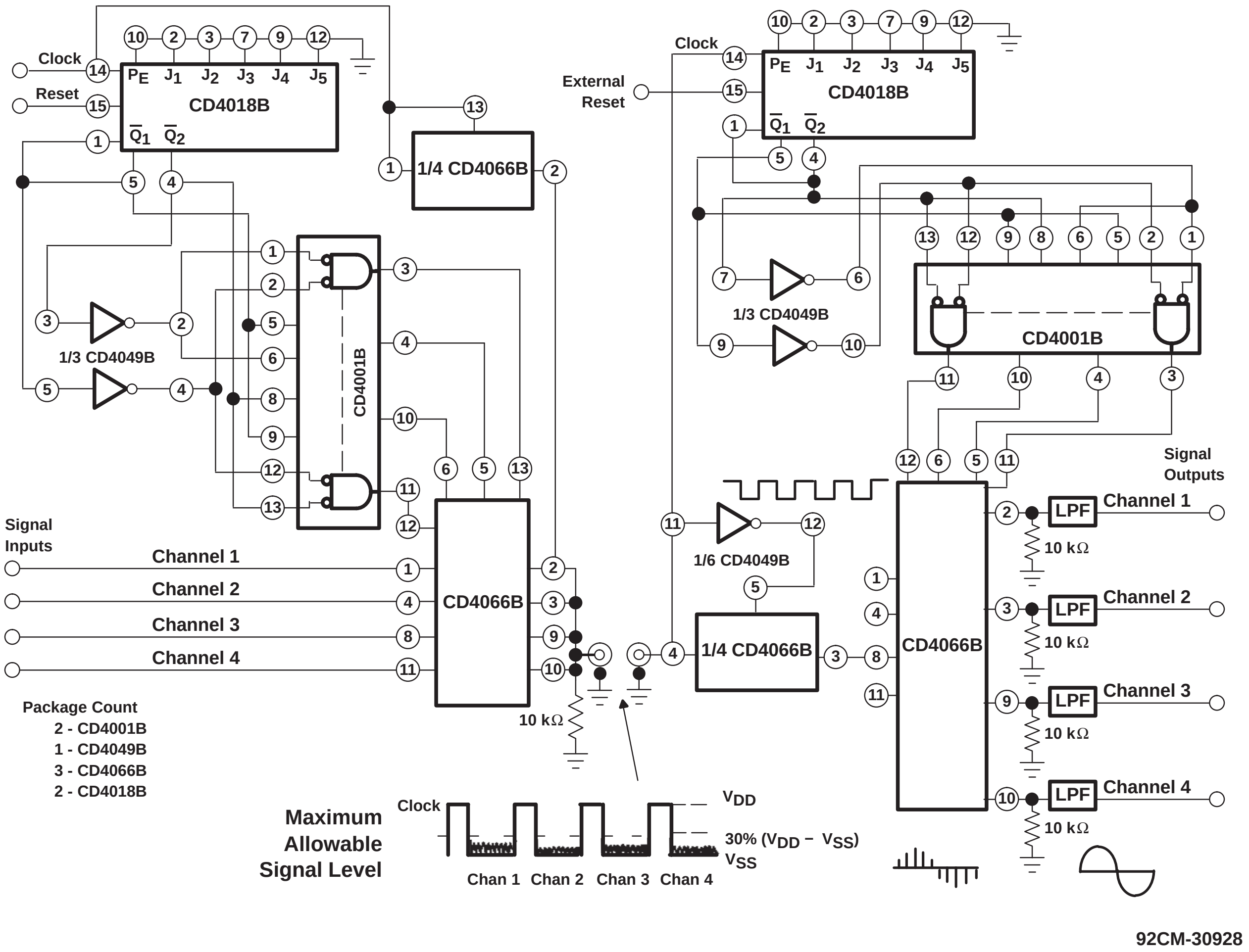
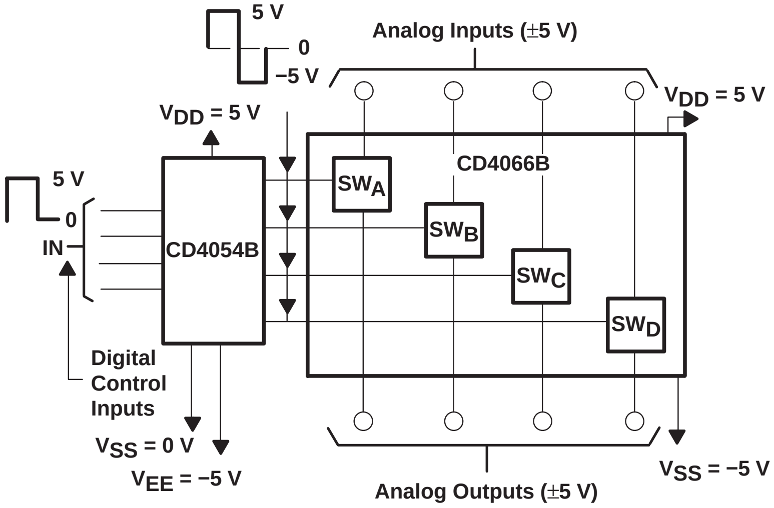

Clock
Reset
CD4018B
PE J1 J2 J3 J4 J5
Q̄1 Q̄2
1/4 CD4066B
CD4001B
1/3 CD4049B
1/3 CD4049B
Signal Inputs
Channel 1
Channel 2
Channel 3
Channel 4
CD4066B
10 kΩ
Package Count
2 - CD4001B
1 - CD4049B
3 - CD4066B
2 - CD4018B
Clock
External Reset
CD4018B
1/3 CD4049B
1/3 CD4049B
CD4001B
1/6 CD4049B
1/4 CD4066B
CD4066B
Signal Outputs
LPF
Channel 1
Channel 2
Channel 3
Channel 4
10 kΩ
Maximum Allowable Signal Level
Clock
VDD
30% (VDD − VSS)
VSS
Chan 1 Chan 2 Chan 3 Chan 4
92CM-30928

Figure 17. Four-Channel PAM Multiplex System Diagram

TYPICAL CHARACTERISTICS


5 V
0
−5 V
Analog Inputs (±5 V)
V_{DD} = 5 V
V_{DD} = 5 V
CD4066B
5 V
0
IN
CD4054B
SW_A
SW_B
SW_C
SW_D
Digital Control Inputs
V_{SS} = 0 V
V_{EE} = −5 V
Analog Outputs (±5 V)
V_{SS} = −5 V

92CS-30927

Figure 18. Bidirectional Signal Transmission Via Digital Control Logic

APPLICATION INFORMATION

In applications that employ separate power sources to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the four CD4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4066B.

In certain applications, the external load-resistor current can include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 V (calculated from r_{on} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.

TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS052B − Revised June 2003

CD4067B, CD4097B Types

CMOS Analog Multiplexers/Demultiplexers

High-Voltage Types (20-Volt Rating)

CD4067B – Single 16-Channel Multiplexer/Demultiplexer
CD4097B – Differential 8-Channel Multiplexer/Demultiplexer

■ CD4067B and CD4097B CMOS analog multiplexers/demultiplexers* are digitally controlled analog switches having low ON impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4067B is a 16-channel multiplexer with four binary control inputs, A,B,C,D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

The CD4097B is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches.

A logic "1" present at the inhibit input turns all channels off.

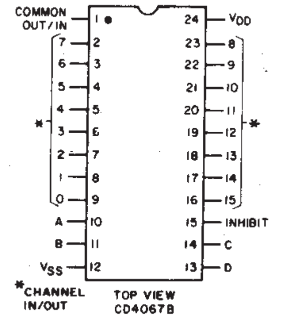
The CD4067B and CD4097B types are supplied in 24-lead hermetic dual-in-line ceramic packages (F3A suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead small-outline packages (M, M96, and NSR suffixes), and 24-lead thin shrink small-outline packages (P and PWR suffixes).

Features:

- Low ON resistance: 125 Ω (typ.) over 15 $V_{p\text{-}p}$ signal-input range for $V_{DD}-V_{SS}$=15 V
- High OFF resistance: channel leakage of ±10 pA (typ.) @ $V_{DD}-V_{SS}$=10 V
- Matched switch characteristics: R_{ON}=5 Ω (typ.) for $V_{DD}-V_{SS}$=15 V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 0.2 μW (typ.) @ $V_{DD}-V_{SS}$=10 V
- Binary address decoding on chip
- 5-V, 10-V, and 15-V parametric ratings
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative **Standard No. 13B,** "Standard Specifications for Description of 'B' Series CMOS Devices"

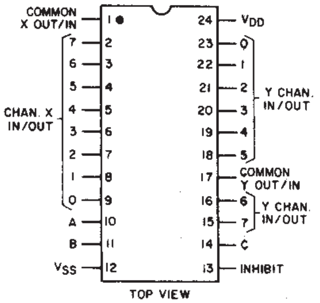
Applications:

- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating


COMMON OUT/IN
1
2
3
4
5
6
7
8
9
10
11
12
7
6
5
4
3
2
1
0
A
B
VSS
24
23
22
21
20
19
18
17
16
15
14
13
VDD
8
9
10
11
12
13
14
15
INHIBIT
C
D
*
*CHANNEL IN/OUT

TOP VIEW
CD4067B
TERMINAL ASSIGNMENT

92CS-24978


COMMON X OUT/IN
1
2
3
4
5
6
7
8
9
10
11
12
7
6
5
4
3
2
1
0
CHAN. X IN/OUT
A
B
VSS
24
23
22
21
20
19
18
17
16
15
14
13
VDD
0
1
2
3
4
5
Y CHAN. IN/OUT
COMMON Y OUT/IN
6
7
Y CHAN. IN/OUT
C
INHIBIT

TOP VIEW
CD4097B
TERMINAL ASSIGNMENT

92CS-24979

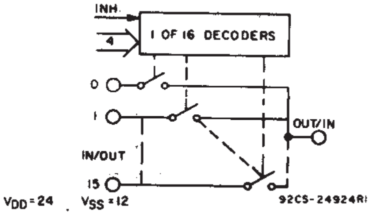

INH
4
1 OF 16 DECODERS
0
1
IN/OUT
15
OUT/IN
VDD=24
VSS=12
92CS-24924R1

Fig. 1 — CD4067 functional diagram.

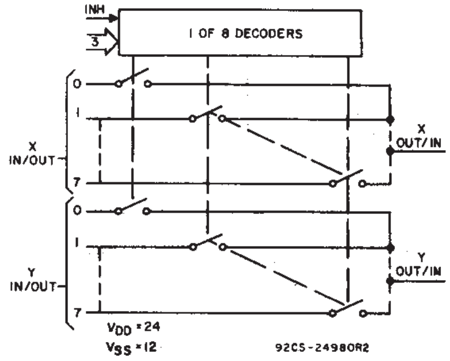

INH
3
1 OF 8 DECODERS
0
1
7
X IN/OUT
X OUT/IN
0
1
7
Y IN/OUT
Y OUT/IN
VDD=24
VSS=12
92CS-24980R2

Fig. 2—CD4097 functional diagram.

Recommended Operating Conditions at T_A = 25°C (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

Characteristic	Min.	Max.	Units
Supply-Voltage Range (T_A=Full Package-Temp. Range)	3	18	V
Multiplexer Switch Input Current Capability	–	25	mA
Output Load Resistance	100	–	Ω

NOTE:

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067; terminals 1 and 17 on the CD4097.

CD4067 TRUTH TABLE

A	B	C	D	Inh	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

CD4097 TRUTH TABLE

A	B	C	Inh	Selected Channel
X	X	X	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

---

*When these devices are used as demultiplexers, the channel in/out terminals are the outputs and the common out/in terminals are the inputs.

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ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							Units
	V_{is} (V)	V_{SS} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{OS})											
Quiescent Device Current, I_{DD} Max.			5	5	5	150	150	–	0.04	5	μA
			10	10	10	300	300	–	0.04	10	
			15	20	20	600	600	–	0.04	20	
			20	100	100	3000	3000	–	0.08	100	
ON-state Resistance $V_{SS} \leqslant V_{is} \leqslant V_{DD}$ r_{on} Max.		0	5	800	850	1200	1300	–	470	1050	Ω
		0	10	310	330	520	550	–	180	400	
		0	15	200	210	300	320	–	125	240	
Change in on-state Resistance (Between Any Two Channels) Δr_{on}		0	5	–	–	–	–	–	15	–	Ω
		0	10	–	–	–	–	–	10	–	
		0	15	–	–	–	–	–	5	–	
OFF Channel Leakage Current: Any Channel OFF Max. or All Channels OFF (Common OUT/IN) Max.		0	18	±100*		±1000*		–	±0.1	±100*	nA
Capacitance: Input, C_{is}		−5	5	–	–	–	–	–	5	–	pF
Output, C_{os} CD4067				–	–	–	–	–	55	–	
CD4097				–	–	–	–	–	35		
Feed-through, C_{ios}				–	–	–	–	–	0.2		
Propagation Delay Time (Signal Input to Output	V_{DD} ⎍	R_L = 200 KΩ C_L=50 pF t_r,t_f=20 ns	5	–	–	–	–	–	30	60	ns
			10	–	–	–	–	–	15	30	
			15	–	–	–	–	–	10	20	
CONTROL (ADDRESS or INHIBIT) V_C											
Input Low Voltage, V_{IL} Max.	=V_{DD} thru 1 KΩ	R_L=1 KΩ to V_{SS} I_{IS}<2 μA on all OFF Channels	5	1.5				–	–	1.5	V
			10	3				–	–	3	
			15	4				–	–	4	
Input High Voltage, V_{IH} Min.			5	3.5				3.5	–	–	
			10	7				7	–	–	
			15	11				11	–	–	

* Determined by minimum feasible leakage measurement for automatic testing.

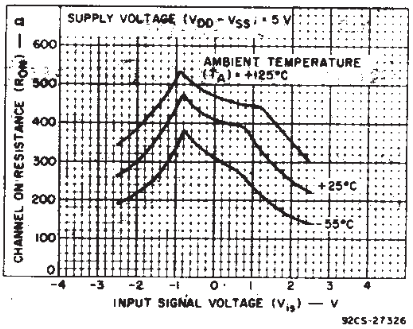


Fig. 3—Typical ON resistance vs. input signal voltage (all types).

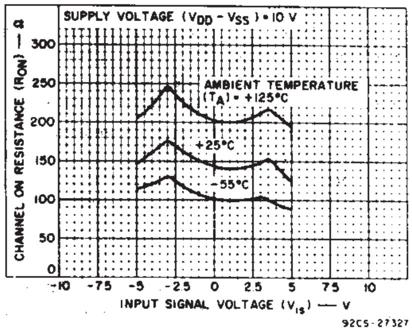


Fig. 4—Typical ON resistance vs. input signal voltage (all types).

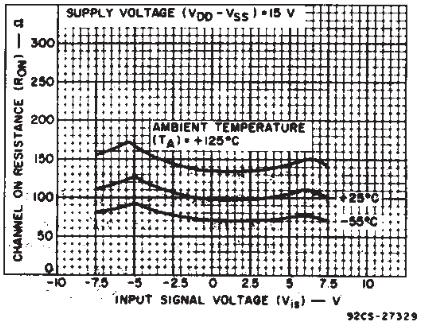


Fig. 5—Typical ON resistance vs. input signal voltage (all types).

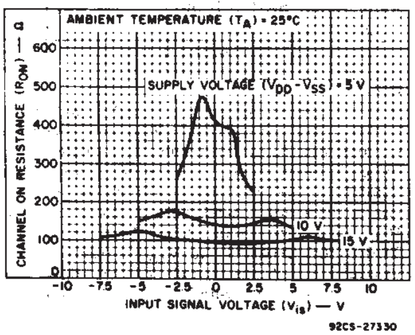


Fig. 6—Typical ON resistance vs. input signal voltage (all types).

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							Units
	V_{is} (V)	V_{SS} (V)	V_{DD} (V)	−55	−40	+85	+125	+25			
								Min.	Typ.	Max.	
Input Current, I_{IN} Max.	V_{IN} = 0, 18 V		18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA
Propagation Delay Time: Address or Inhibit-to-Signal OUT (Channel turning ON)	R_L=10 KΩ, C_L=50 pF, t_r,t_f=20 ns										ns
		0	5	–	–	–	–	–	325	650	
		0	10	–	–	–	–	–	135	270	
		0	15	–	–	–	–	–	95	190	
Address or Inhibit-to-Signal OUT (Channel turning OFF)	R_L=300 Ω, C_L=50 pF, t_r,t_f=20 ns										ns
		0	5	–	–	–	–	–	220	440	
		0	10	–	–	–	–	–	90	180	
		0	15	–	–	–	–	–	65	130	
Input Capacitance, C_{IN}	Any Address or Inhibit Input			–	–	–	–	–	5	7.5	pF

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) .... −0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −55°C to +100°C 500mW
For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) .... −55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... −65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

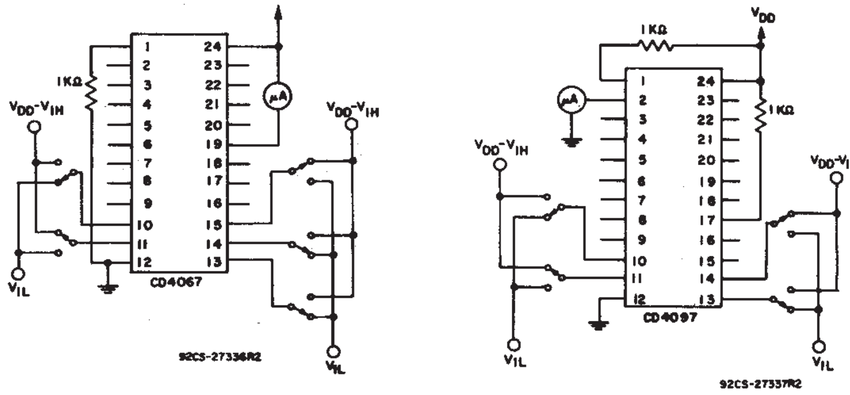

1KΩ
VDD-VIH
VIL
µA
CD4067
92CS-27336R2
1KΩ
VDD
CD4097
92CS-27337R2

Fig. 8—Input voltage—measure <2 µA on all OFF channels (e.g., channel 12).

TEST CIRCUITS

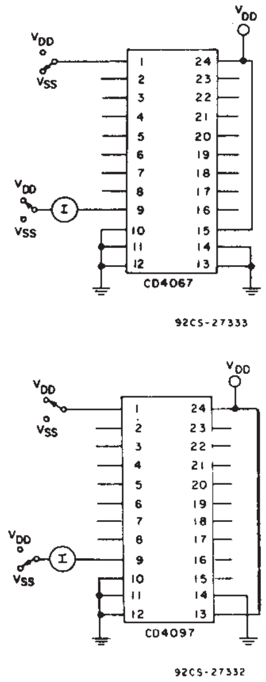

VDD
VSS
I
CD4067
92CS-27333
CD4097
92CS-27332

Fig. 7—OFF channel leakage current—any channel OFF.

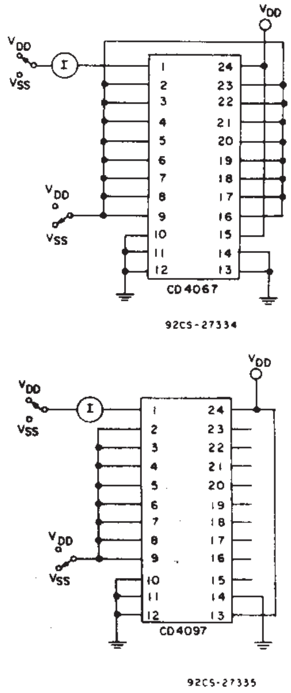

VDD
VSS
I
CD4067
92CS-27334
CD4097
92CS-27335

Fig. 9—OFF channel leakage current—all channels OFF.

ELECTRICAL CHARACTERISTICS (Cont'd)

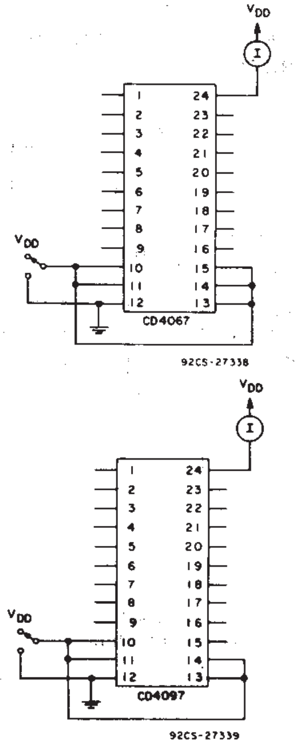
CHARACTERISTIC	TEST CONDITIONS					TYPICAL VALUES	UNITS
	V_{is} (V)	V_{DD} (V)	R_L (KΩ)				
Cutoff (−3-dB) Frequency Channel ON (Sine Wave Input)	5●	10	1	V_{os} at Common OUT/IN	CD4067	14	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -3$ dB				CD4097	20	
				V_{os} at Any Channel		60	
Total Harmonic Distortion, THD	2●	5	10			0.3	%
	3●	10				0.2	
	5●	15				0.12	
	f_{is} = 1 kHz sine wave						
−40-dB Feedthrough Frequency (All Channels OFF	5●	10	1	V_{os} at Common OUT/IN	CD4067	20	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -40$ dB				CD4097	12	
				V_{os} at Any Channel		8	
Signal Crosstalk (Frequency at −40 dB)	5●	10	1	Between Any 2 Channels▲		1	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -40$ dB			Between Sections CD4097 Only	Measured on Common	10	
					Measured on Any Channel	18	
Address-or-Inhibit-to-Signal Crosstalk	–	10	10*			75	mV (Peak)
	V_{SS}=0, t_r,t_f=20 ns, V_C=V_{DD}−V_{SS} (Square Wave)						

● Peak-to-peak voltage symmetrical about $\frac{V_{DD}-V_{SS}}{2}$.

▲ Worst case.

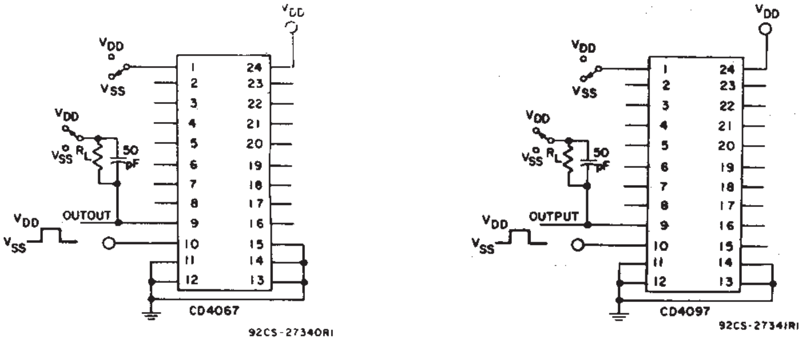
* Both ends of channel.

TEST CIRCUITS (Cont'd)



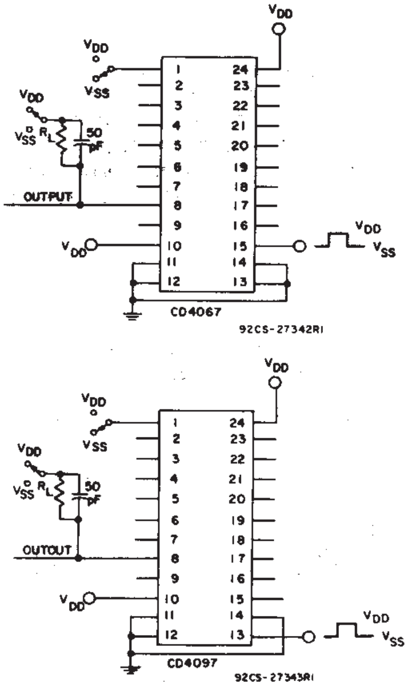
VDD
I
CD4067
92CS-27338
VDD
I
CD4097
92CS-27339

Fig. 10– Quiescent device current.



VDD
VSS
RL
50 pF
OUTPUT
CD4067
92CS-27340RI
CD4097
92CS-27341RI

Fig. 11– Turn-on and turn-off propagation delay–address select input to signal output (e.g. measured on channel 0).



VDD
VSS
RL
50 pF
OUTPUT
CD4067
92CS-27342RI
CD4097
92CS-27343RI

Fig. 12– Turn-on and turn-off propagation delay–inhibit input to signal output (e.g. measured on channel 1).

CD4067B, CD4097B Types

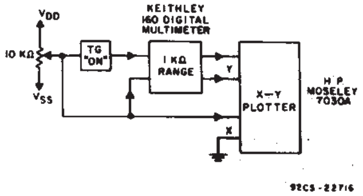

VDD
10 KΩ
VSS
TG "ON"
KEITHLEY 160 DIGITAL MULTIMETER
1 KΩ RANGE
Y
X
X—Y PLOTTER
H P MOSELEY 7030A
92CS-22716

Fig. 13— Channel ON resistance measurement circuit.

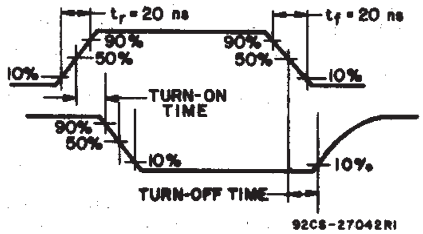

tr = 20 ns
tf = 20 ns
90%
50%
10%
90%
50%
10%
TURN-ON TIME
90%
50%
10%
10%
TURN-OFF TIME
92CS-27042R1

Fig. 14— Propagation delay waveform channel being turned ON (R_L = 10 K Ω, C_L = 50 pF).

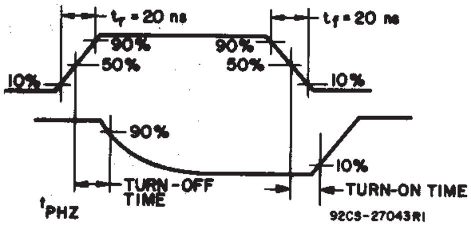

tr = 20 ns
tf = 20 ns
90%
50%
10%
90%
50%
10%
90%
10%
tPHZ
TURN-OFF TIME
TURN-ON TIME
92CS-27043R1

Fig. 15— Propagation delay waveform, channel being turned OFF (R_L = 300 Ω, C_L = 50 pF).

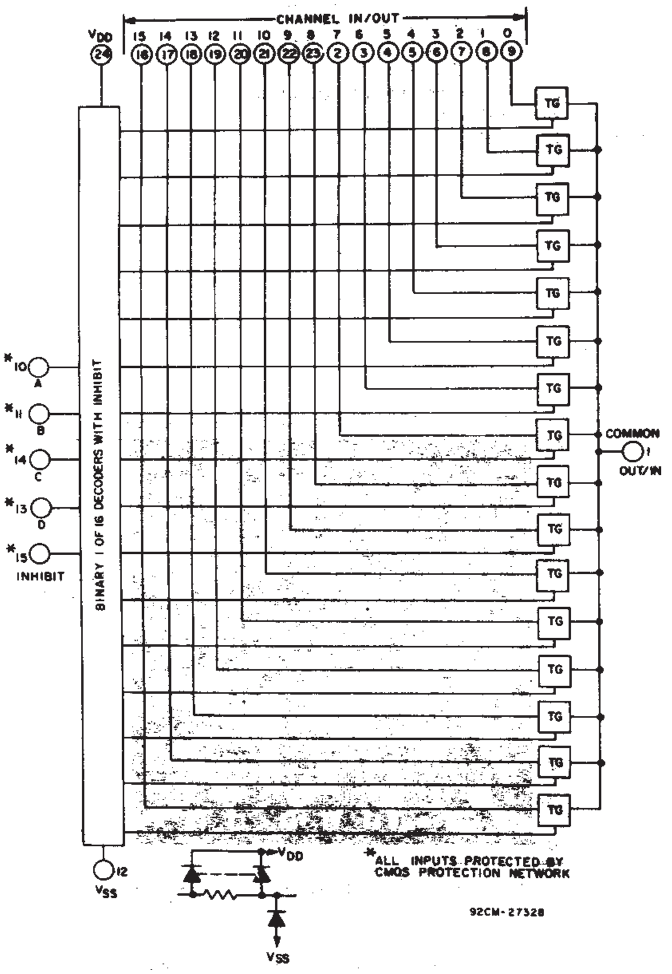

CHANNEL IN/OUT
VDD 24
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
16 17 18 19 20 21 22 23 2 3 4 5 6 7 8 9
TG
COMMON 1 OUT/IN
*10 A
*11 B
*14 C
*13 D
*15 INHIBIT
BINARY 1 OF 16 DECODERS WITH INHIBIT
12 VSS
VDD
VSS
*ALL INPUTS PROTECTED BY CMOS PROTECTION NETWORK
92CM-27328

Fig. 16—CD4067 logic diagram.

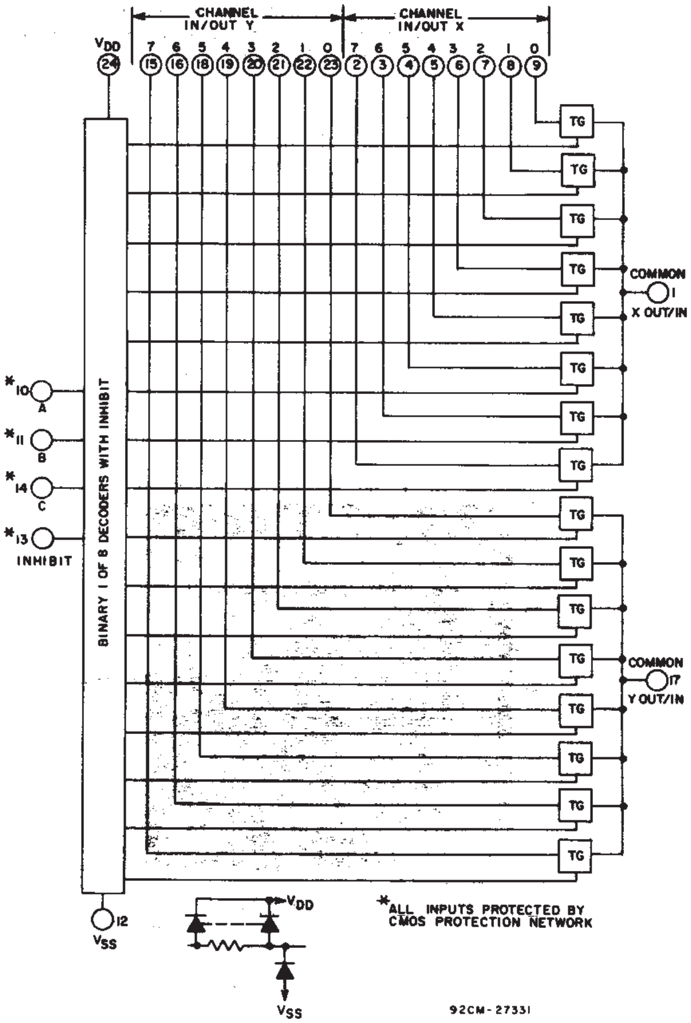

CHANNEL IN/OUT Y
CHANNEL IN/OUT X
VDD 24
7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0
15 16 18 19 20 21 22 23 2 3 4 5 6 7 8 9
TG
COMMON 1 X OUT/IN
COMMON 17 Y OUT/IN
*10 A
*11 B
*14 C
*13 INHIBIT
BINARY 1 OF 8 DECODERS WITH INHIBIT
12 VSS
VDD
VSS
*ALL INPUTS PROTECTED BY CMOS PROTECTION NETWORK
92CM-27331

Fig. 17—CD4097 logic diagram.

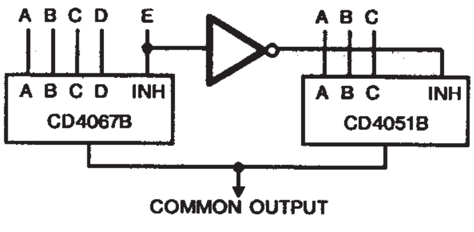

A B C D
E
A B C
A B C D INH
CD4067B
A B C INH
CD4051B
COMMON OUTPUT

Fig. 18–24-to-1 MUX Addressing

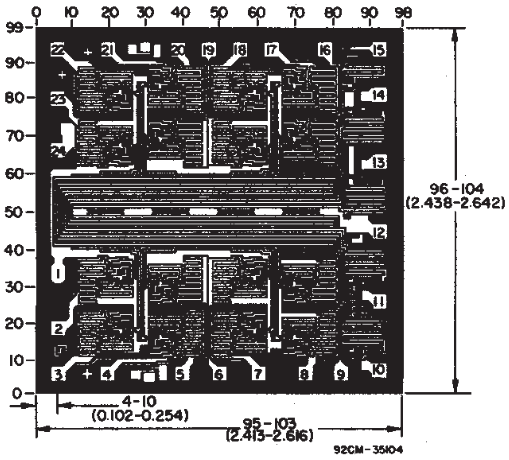
SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L=effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4067B or CD4097B.

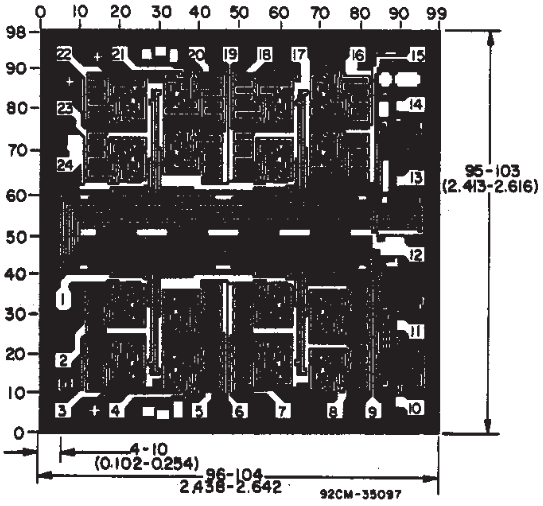
When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to V_{SS}, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to V_{SS}.

The amount of charge dumped is mostly a function of the signal level above V_{SS}. Typically, at $V_{DD}-V_{SS}=10$ V, a 100-pF capacitor connected to the input or output of the channel will lose 3-4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 μs. When the inhibit signal turns a channel off, there is no charge dumping to V_{SS}. Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067B, terminals 1 and 17 on the CD4097B.


0 10 20 30 40 50 60 70 80 90 98
99 90 80 70 60 50 40 30 20 10 0
22 21 20 19 18 17 16 15
14 13 12 11 10
23 24 1 2
3 4 5 6 7 8 9
96-104
(2.438-2.642)
4-10
(0.102-0.254)
95-103
(2.413-2.616)
92CM-35104

Dimensions and pad layout for CD4067BH.


0 10 20 30 40 50 60 70 80 90 99
98 90 80 70 60 50 40 30 20 10 0
22 21 20 19 18 17 16 15
14 13 12 11 10
23 24 1 2
3 4 5 6 7 8 9
95-103
(2.413-2.616)
4-10
(0.102-0.254)
96-104
2.438-2.642
92CM-35097

Dimensions and pad layout for CD4097BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Insert Tab Here

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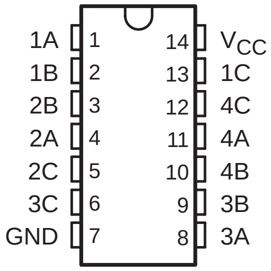
SN74HC4066
QUADRUPLE BILATERAL ANALOG SWITCH

SCLS325G − MARCH 1996 − REVISED JULY 2003

- **Wide Operating Voltage Range of 2 V to 6 V**
- **Typical Switch Enable Time of 18 ns**
- **Low Power Consumption, 20-µA Max I_{CC}**
- **Low Input Current of 1 µA Max**
- **High Degree of Linearity**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Low On-State Impedance . . . 50-Ω TYP at V_{CC} = 6 V**
- **Individual Switch Controls**

D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74HC4066 is a silicon-gate CMOS quadruple analog switch designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 6 V (peak) to be transmitted in either direction.

Each switch section has its own enable input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube of 25	SN74HC4066N	SN74HC4066N
	SOIC − D	Tube of 50	SN74HC4066D	HC4066
		Reel of 2500	SN74HC4066DR	
		Reel of 250	SN74HC4066DT	
	SOP − NS	Reel of 2000	SN74HC4066NSR	HC4066
	SSOP − DB	Reel of 2000	SN74HC4066DBR	HC4066
	TSSOP − PW	Tube of 90	SN74HC4066PW	HC4066
		Reel of 2000	SN74HC4066PWR	
		Reel of 250	SN74HC4066PWT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each switch)

INPUT CONTROL (C)	SWITCH
L	OFF
H	ON

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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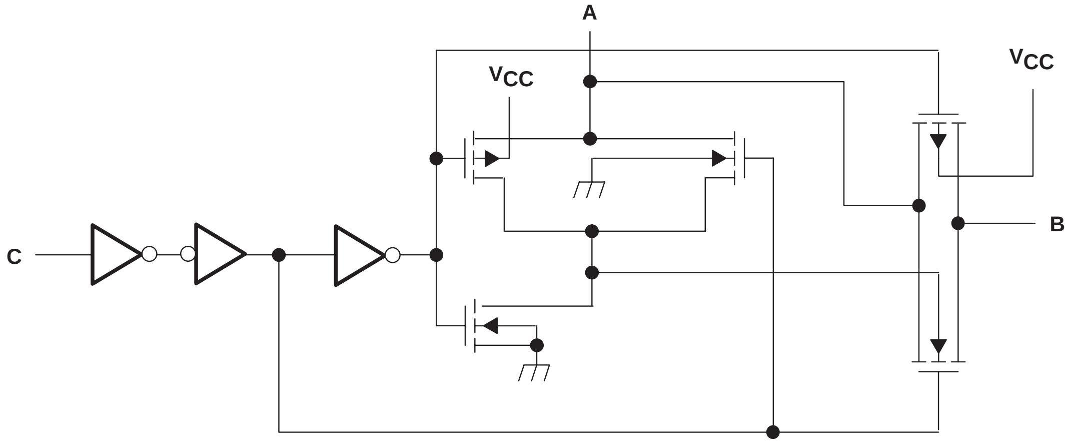
logic diagram, each switch (positive logic)



One of Four Switches

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)		−0.5 V to 7 V
Control-input diode current, I_I ($V_I < 0$ or $V_I > V_{CC}$)		±20 mA
I/O port diode current, I_I ($V_I < 0$ or $V_{I/O} > V_{CC}$)		±20 mA
On-state switch current ($V_{I/O}$ = 0 to V_{CC})		±25 mA
Continuous current through V_{CC} or GND		±50 mA
Package thermal impedance, θ_{JA} (see Note 2):	D package	86°C/W
	DB package	96°C/W
	N package	80°C/W
	NS package	76°C/W
	PW package	113°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2[†]	5	6	V
$V_{I/O}$	I/O port voltage		0		V_{CC}	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		V_{CC}	V
		V_{CC} = 4.5 V	3.15		V_{CC}	
		V_{CC} = 6 V	4.2		V_{CC}	
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	
		V_{CC} = 6 V	0		1.2	
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature		−40		85	°C

[†] With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	T_A = 25°C					UNIT
					MIN	TYP	MAX	MIN	MAX	
r_{on}	On-state switch resistance		I_T = −1 mA, V_I = 0 to V_{CC}, V_C = V_{IH} (see Figure 1)	2 V		150				Ω
				4.5 V		50	85		106	
				6 V		30				
$r_{on(p)}$	Peak on-state resistance		V_I = V_{CC} or GND, V_C = V_{IH}, I_T = −1 mA	2 V		320				Ω
				4.5 V		70	170		215	
				6 V		50				
I_I	Control input current		V_C = 0 or V_{CC}	6 V		±0.1	±100		±1000	nA
I_{soff}	Off-state switch leakage current		V_I = V_{CC} or 0, V_O = V_{CC} or 0, V_C = V_{IL} (see Figure 2)	6 V			±0.1		±5	µA
I_{son}	On-state switch leakage current		V_I = V_{CC} or 0, V_C = V_{IH} (see Figure 3)	6 V			±0.1		±5	µA
I_{CC}	Supply current		V_I = 0 or V_{CC}, I_O = 0	6 V			2		20	µA
C_i	Input capacitance	A or B		5 V		9				pF
		C				3	10		10	
C_f	Feed-through capacitance	A to B	V_I = 0			0.5				pF
C_o	Output capacitance	A or B		5 V		9				pF

switching characteristics over recommended operating free-air temperature range

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
						MIN	TYP	MAX			
t_{PLH}, t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50 pF (see Figure 4)	2 V		10	60		75	ns
					4.5 V		4	12		15	
					6 V		3	10		13	
t_{PZH}, t_{PZL}	Switch turn-on time	C	A or B	R_L = 1 kΩ, C_L = 50 pF (see Figure 5)	2 V		70	180		225	ns
					4.5 V		21	36		45	
					6 V		18	31		38	
t_{PLZ}, t_{PHZ}	Switch turn-off time	C	A or B	R_L = 1 kΩ, C_L = 50 pF (see Figure 5)	2 V		50	200		250	ns
					4.5 V		25	40		50	
					6 V		22	34		43	
f_I	Control input frequency	C	A or B	C_L = 15 pF, R_L = 1 kΩ, V_C = V_{CC} or GND, V_O = V_{CC}/2 (see Figure 6)	2 V		15				MHz
					4.5 V		30				
					6 V		30				
	Control feed-through noise	C	A or B	C_L = 50 pF, R_{in} = R_L = 600 Ω, V_C = V_{CC} or GND, f_{in} = 1 MHz (see Figure 7)	4.5 V		15				mV (rms)
					6 V		20				

operating characteristics, V_{CC} = 4.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 1 MHz	45	pF
	Minimum through bandwidth, A to B or B to A† [20 log (V_O/V_I)] = −3 dB	C_L = 50 pF, V_C = V_{CC}	R_L = 600 Ω, (see Figure 8)	30	MHz
	Crosstalk between any switches‡	C_L = 10 pF, f_{in} = 1 MHz	R_L = 50 Ω, (see Figure 9)	45	dB
	Feed through, switch off, A to B or B to A‡	C_L = 50 pF, f_{in} = 1 MHz	R_L = 600 Ω, (see Figure 10)	42	dB
	Amplitude distortion rate, A to B or B to A	C_L = 50 pF, f_{in} = 1 kHz	R_L = 10 kΩ, (see Figure 11)	0.05%	

† Adjust the input amplitude for output = 0 dBm at f = 1 MHz. Input signal must be a sine wave.
‡ Adjust the input amplitude for input = 0 dBm at f = 1 MHz. Input signal must be a sine wave.

PARAMETER MEASUREMENT INFORMATION

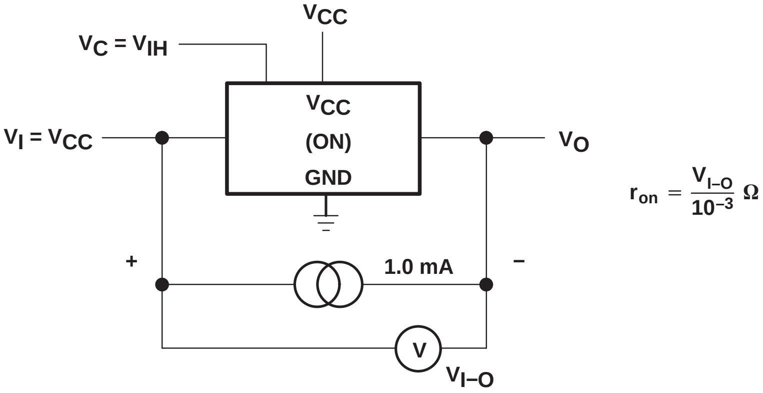
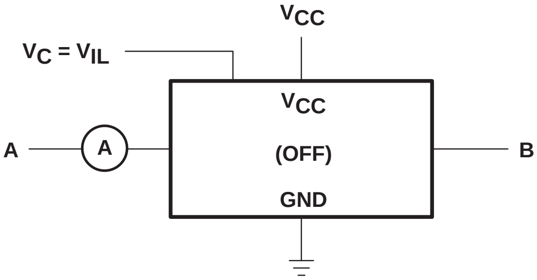

V_{CC}
$V_C = V_{IH}$
V_{CC}
(ON)
GND
$V_I = V_{CC}$
V_O
$r_{on} = \frac{V_{I-O}}{10^{-3}}\ \Omega$
+
1.0 mA
−
V
V_{I-O}

Figure 1. On-State Resistance Test Circuit


V_{CC}
$V_C = V_{IL}$
V_{CC}
A
A
(OFF)
GND
B

$V_S = V_A - V_B$
CONDITION 1: $V_A = 0$, $V_B = V_{CC}$
CONDITION 2: $V_A = V_{CC}$, $V_B = 0$

Figure 2. Off-State Switch Leakage-Current Test Circuit

PARAMETER MEASUREMENT INFORMATION

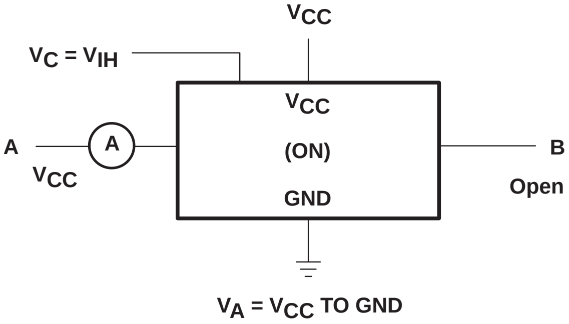

V_{CC}
$V_C = V_{IH}$
V_{CC}
(ON)
GND
A
A
V_{CC}
B
Open
$V_A = V_{CC}$ TO GND

Figure 3. On-State Leakage-Current Test Circuit

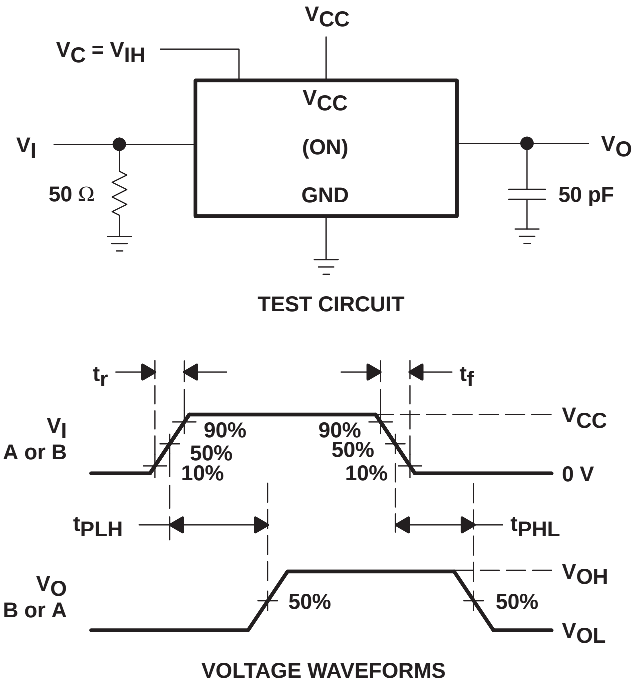
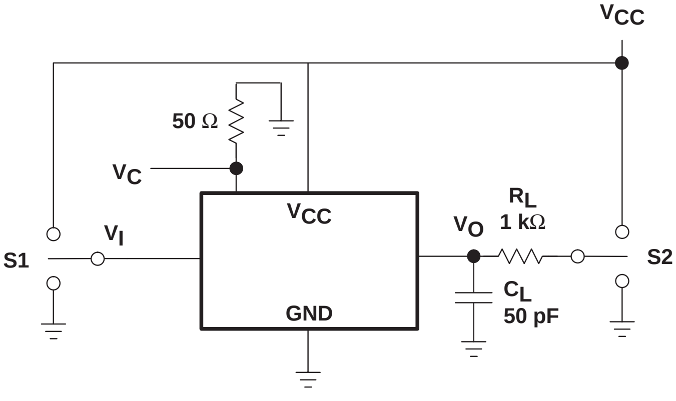

V_{CC}
$V_C = V_{IH}$
V_{CC}
(ON)
GND
V_I
50 Ω
V_O
50 pF
TEST CIRCUIT
t_r
t_f
V_I
A or B
90%
50%
10%
90%
50%
10%
V_{CC}
0 V
t_{PLH}
t_{PHL}
V_O
B or A
50%
50%
V_{OH}
V_{OL}
VOLTAGE WAVEFORMS

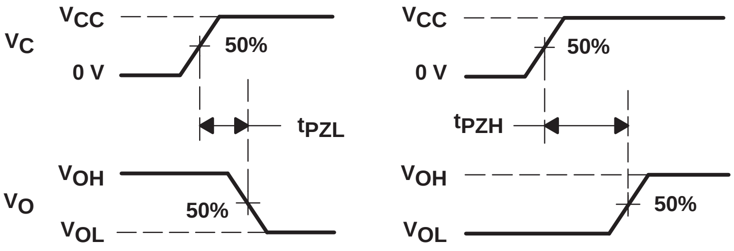
Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION

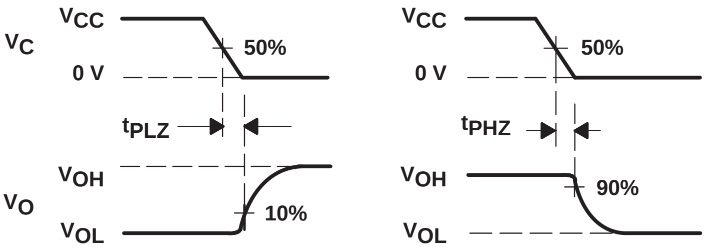

VCC
50 Ω
VC
VCC
GND
VI
S1
VO
RL
1 kΩ
S2
CL
50 pF

TEST	S1	S2
t_{PZL}	GND	V_{CC}
t_{PZH}	V_{CC}	GND
t_{PLZ}	GND	V_{CC}
t_{PHZ}	V_{CC}	GND

TEST CIRCUIT


VCC
VC
0 V
50%
VCC
0 V
50%
tPZL
tPZH
VOH
VO
VOL
50%
VOH
VOL
50%

(t_{PZL}, t_{PZH})


VCC
VC
0 V
50%
VCC
0 V
50%
tPLZ
tPHZ
VOH
VO
VOL
10%
VOH
VOL
90%

(t_{PLZ}, t_{PHZ})

VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output

PARAMETER MEASUREMENT INFORMATION

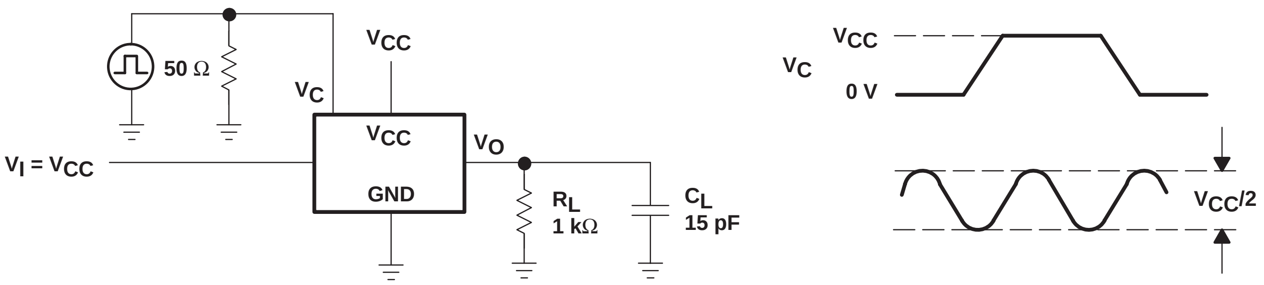

50 Ω
VCC
VC
VCC
GND
VO
VI = VCC
RL
1 kΩ
CL
15 pF
VCC
VC
0 V
VCC/2

Figure 6. Control-Input Frequency

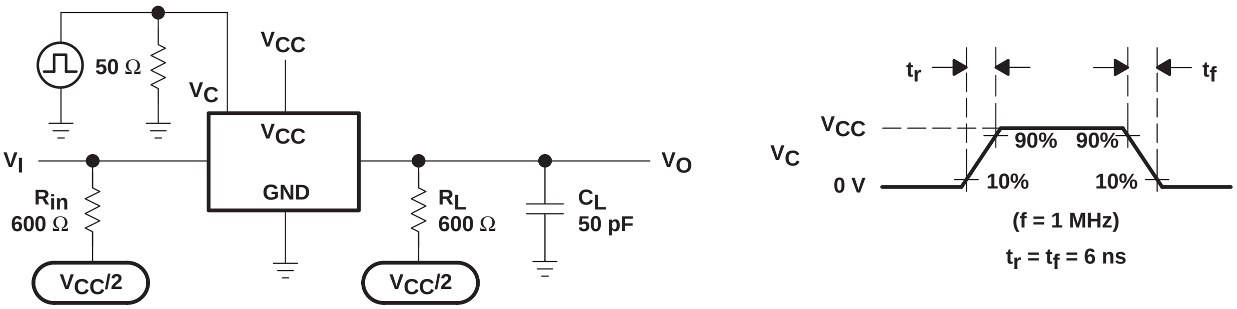

50 Ω
VCC
VC
VCC
GND
VI
Rin
600 Ω
VCC/2
RL
600 Ω
CL
50 pF
VO
VCC/2
tr
tf
VCC
VC
0 V
90%
90%
10%
10%
(f = 1 MHz)
tr = tf = 6 ns

Figure 7. Control Feed-Through Noise

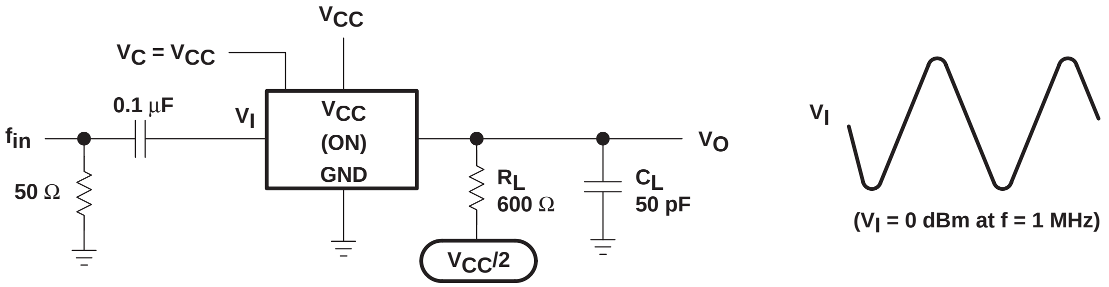

VCC
VC = VCC
0.1 µF
VI
VCC
(ON)
GND
fin
50 Ω
RL
600 Ω
VCC/2
CL
50 pF
VO
VI
(VI = 0 dBm at f = 1 MHz)

Figure 8. Minimum Through Bandwidth

PARAMETER MEASUREMENT INFORMATION

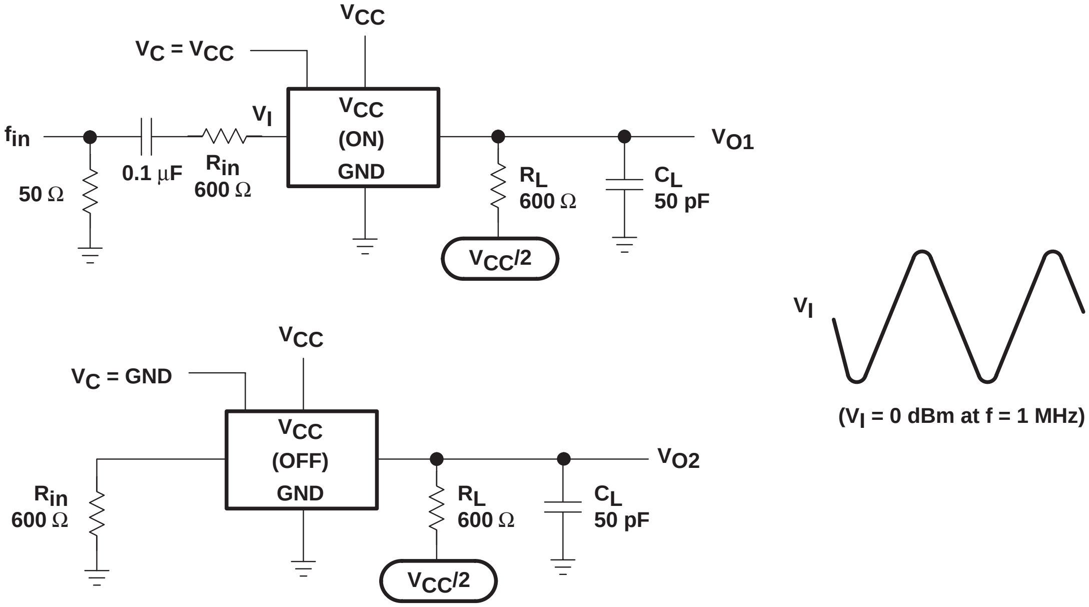

VCC
VC = VCC
fin
0.1 µF
VI
Rin
600 Ω
50 Ω
VCC
(ON)
GND
RL
600 Ω
CL
50 pF
VO1
VCC/2
VCC
VC = GND
Rin
600 Ω
VCC
(OFF)
GND
RL
600 Ω
CL
50 pF
VO2
VCC/2
VI
(VI = 0 dBm at f = 1 MHz)

Figure 9. Crosstalk Between Any Two Switches

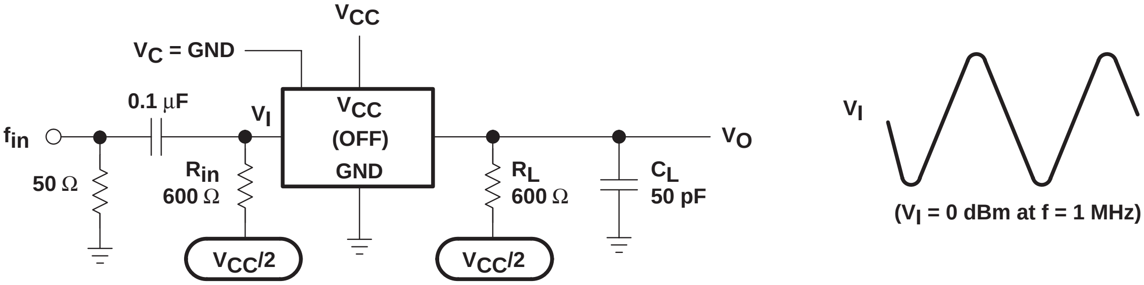

VCC
VC = GND
0.1 µF
VI
fin
50 Ω
Rin
600 Ω
VCC
(OFF)
GND
RL
600 Ω
CL
50 pF
VO
VCC/2
VCC/2
VI
(VI = 0 dBm at f = 1 MHz)

Figure 10. Feed Through, Switch Off

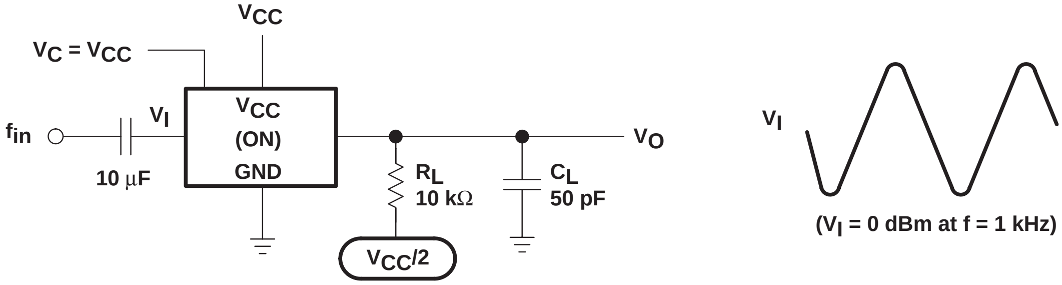

VCC
VC = VCC
VI
fin
10 µF
VCC
(ON)
GND
RL
10 kΩ
CL
50 pF
VO
VCC/2
VI
(VI = 0 dBm at f = 1 kHz)

Figure 11. Amplitude-Distortion Rate

Insert Tab Here

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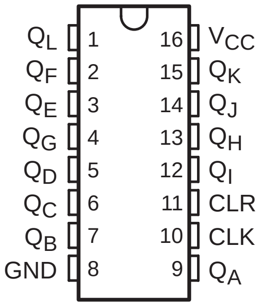
SN54LV4040A, SN74LV4040A
12-BIT ASYNCHRONOUS BINARY COUNTERS

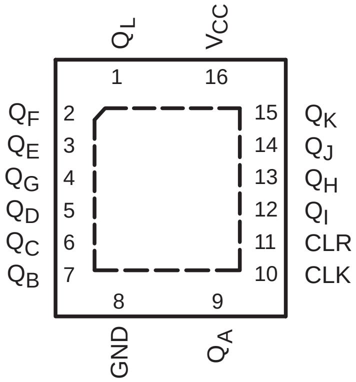
SCES226G − APRIL 1999 − REVISED AUGUST 2003

- **2-V to 5.5-V V_{CC} Operation**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **− 2000-V Human-Body Model (A114-A)**
  - **− 200-V Machine Model (A115-A)**
  - **− 1000-V Charged-Device Model (C101)**

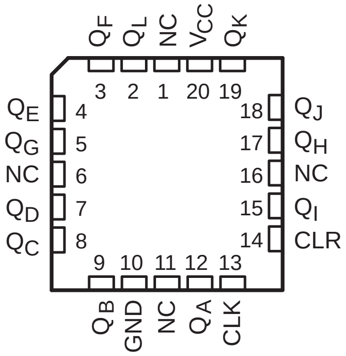
SN54LV4040A . . . J OR W PACKAGE
SN74LV4040A . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)


Q_L 1
Q_F 2
Q_E 3
Q_G 4
Q_D 5
Q_C 6
Q_B 7
GND 8
16 V_{CC}
15 Q_K
14 Q_J
13 Q_H
12 Q_I
11 CLR
10 CLK
9 Q_A

SN74LV4040A . . . RGY PACKAGE
(TOP VIEW)


Q_L
V_{CC}
1
16
Q_F 2
Q_E 3
Q_G 4
Q_D 5
Q_C 6
Q_B 7
15 Q_K
14 Q_J
13 Q_H
12 Q_I
11 CLR
10 CLK
8
9
GND
Q_A

SN54LV4040A . . . FK PACKAGE
(TOP VIEW)


Q_F
Q_L
NC
V_{CC}
Q_K
3 2 1 20 19
Q_E 4
Q_G 5
NC 6
Q_D 7
Q_C 8
18 Q_J
17 Q_H
16 NC
15 Q_I
14 CLR
9 10 11 12 13
Q_B
GND
NC
Q_A
CLK

NC − No internal connection

description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube of 25	SN74LV4040AN	SN74LV4040AN
	QFN − RGY	Reel of 1000	SN74LV4040ARGYR	LW040A
	SOIC − D	Tube of 40	SN74LV4040AD	LV4040A
		Reel of 2500	SN74LV4040ADR	
	SOP − NS	Reel of 2000	SN74LV4040ANSR	74LV4040A
	SSOP − DB	Reel of 2000	SN74LV4040ADBR	LW040A
	TSSOP − PW	Tube of 90	SN74LV4040APW	LW040A
		Reel of 2000	SN74LV4040APWR	
		Reel of 250	SN74LV4040APWT	
	TVSOP − DGV	Reel of 2000	SN74LV4040ADGVR	LW040A
−55°C to 125°C	CDIP − J	Tube of 25	SNJ54LV4040AJ	SNJ54LV4040AJ
	CFP − W	Tube of 150	SNJ54LV4040AW	SNJ54LV4040AW
	LCCC − FK	Tube of 55	SNJ54LV4040AFK	SNJ54LV4040AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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description/ordering information (continued)

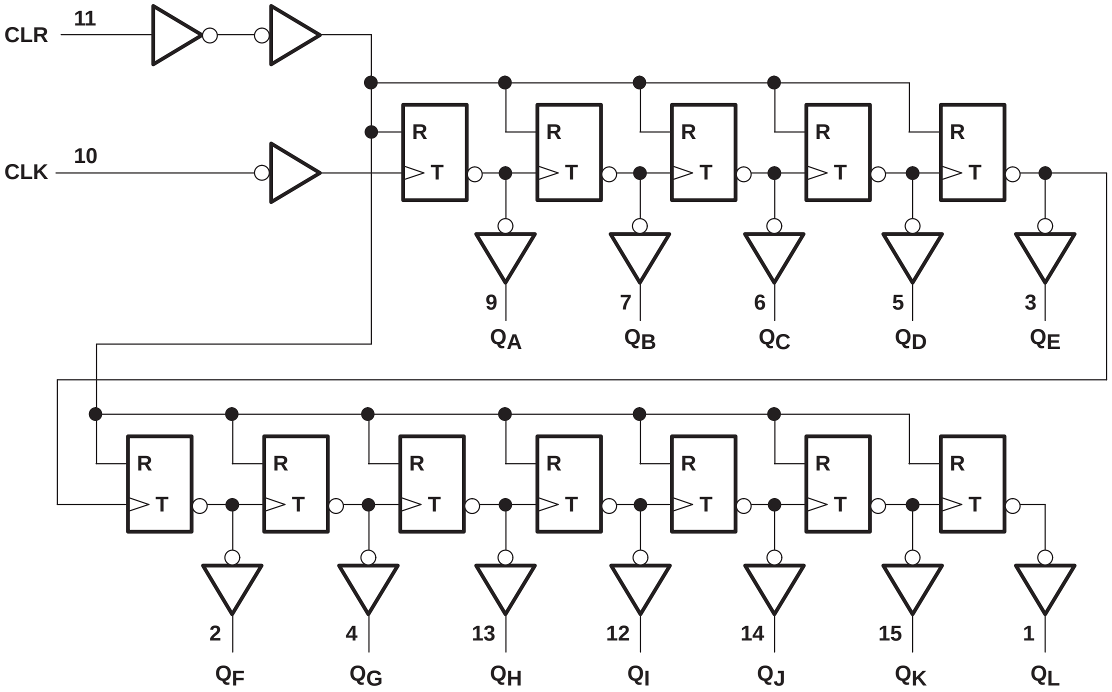
The ’LV4040A devices are 12-bit asynchronous binary counters with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE
(each buffer)

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	−0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	−20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
(see Note 3): DB package	82°C/W
(see Note 3): DGV package	120°C/W
(see Note 3): N package	67°C/W
(see Note 3): NS package	64°C/W
(see Note 3): PW package	108°C/W
(see Note 4): RGY package	39°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LV4040A		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	µA
		V_{CC} = 2.3 V to 2.7 V		−2		−2	mA
		V_{CC} = 3 V to 3.6 V		−6		−6	
		V_{CC} = 4.5 V to 5.5 V		−12		−12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

PRODUCT PREVIEW

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV4040A			SN74LV4040A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = −50 µA	2 V to 5.5 V	V_{CC}−0.1			V_{CC}−0.1			V
	I_{OH} = −2 mA	2.3 V	2			2			
	I_{OH} = −6 mA	3 V	2.48			2.48			
	I_{OH} = −12 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	
	I_{OL} = 6 mA	3 V			0.44			0.44	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1			±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5			5	µA
C_i	V_I = V_{CC} or GND	3.3 V		1.9			1.9		pF

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV4040A		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	7		7		7		ns
		CLR high	6.5		6.5		6.5		
t_{su}	Setup time	CLR inactive before CLK↓	6.5		6.5		6.5		ns

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV4040A		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		5		ns
		CLR high	5		5		5		
t_{su}	Setup time	CLR inactive before CLK↓	5		5		5		ns

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV4040A		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		5		ns
		CLR high	5		5		5		
t_{su}	Setup time	CLR inactive before CLK↓	5		5		5		ns

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV4040A		SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	50*	115*		40*		40		MHz
			C_L = 50 pF	40	95		35		35		
t_{PLH}	CLK	Q_A	C_L = 15 pF		8.7*	19.4*	1*	23*	1	23	ns
t_{PHL}					8.7*	19.4*	1*	23*	1	23	
t_{PHL}	CLR	Any Q	C_L = 15 pF		9.3*	19.9*	1*	24*	1	24	ns
t_{PLH}	$\overline{CLK}$	Q_A	C_L = 50 pF		10.5	24.1	1	28	1	28	ns
t_{PHL}					10.5	24.1	1	28	1	28	
t_{PHL}	CLR	Any Q	C_L = 50 pF		11.7	24.5	1	28	1	28	ns
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50 pF		1.7	5.9		7		7	ns

PRODUCT PREVIEW

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV4040A		SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	75*	160*		75*		75		MHz
			C_L = 50 pF	55	130		50		50		
t_{PLH}	CLK	Q_A	C_L = 15 pF		6.1*	11.9*	1*	14*	1	14	ns
t_{PHL}					6.1*	11.9*	1*	14*	1	14	
t_{PHL}	CLR	Any Q	C_L = 15 pF		7.1*	12.8*	1*	15*	1	15	ns
t_{PLH}	$\overline{CLK}$	Q_A	C_L = 50 pF		7.5	15.4	1	17.5	1	17.5	ns
t_{PHL}					7.5	15.4	1	17.5	1	17.5	
t_{PHL}	CLR	Any Q	C_L = 50 pF		9	16.3	1	18.5	1	18.5	ns
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50 pF		1.2	4.4		5		5	ns

PRODUCT PREVIEW

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV4040A		SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	150*	235*		125*		125		MHz
			C_L = 50 pF	95	185		80		80		
t_{PLH}	CLK	Q_A	C_L = 15 pF		4.2*	7.3*	1*	8.5*	1	8.5	ns
t_{PHL}					4.2*	7.3*	1*	8.5*	1	8.5	
t_{PHL}	CLR	Any Q	C_L = 15 pF		5.3*	8.6*	1*	10*	1	10	ns
t_{PLH}	$\overline{CLK}$	Q_A	C_L = 50 pF		5.3	9.3	1	10.5	1	10.5	ns
t_{PHL}					5.3	9.3	1	10.5	1	10.5	
t_{PHL}	CLR	Any Q	C_L = 50 pF		6.8	10.6	1	12	1	12	ns
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50 pF		0.8	3.1		3.5		3.5	ns

PRODUCT PREVIEW

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 6)

PARAMETER		SN74LV4040A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.5	−0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	11.9	pF
			5 V	13.1	

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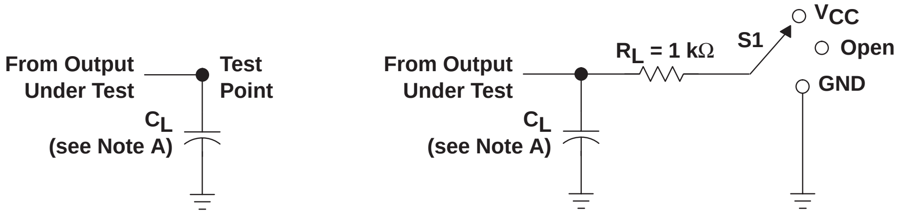
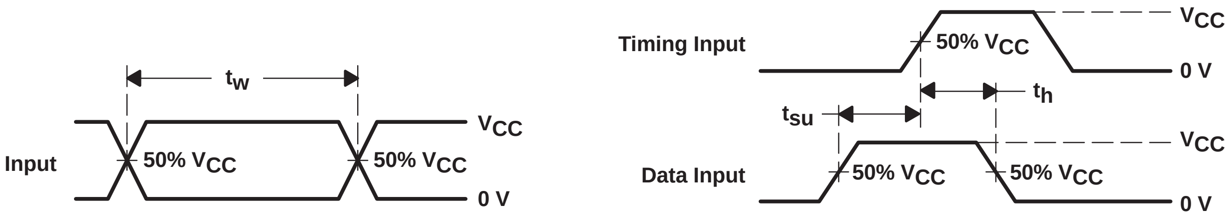
PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
Test
Point
C_L
(see Note A)
From Output
Under Test
R_L = 1 kΩ
S1
V_{CC}
Open
GND
C_L
(see Note A)

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

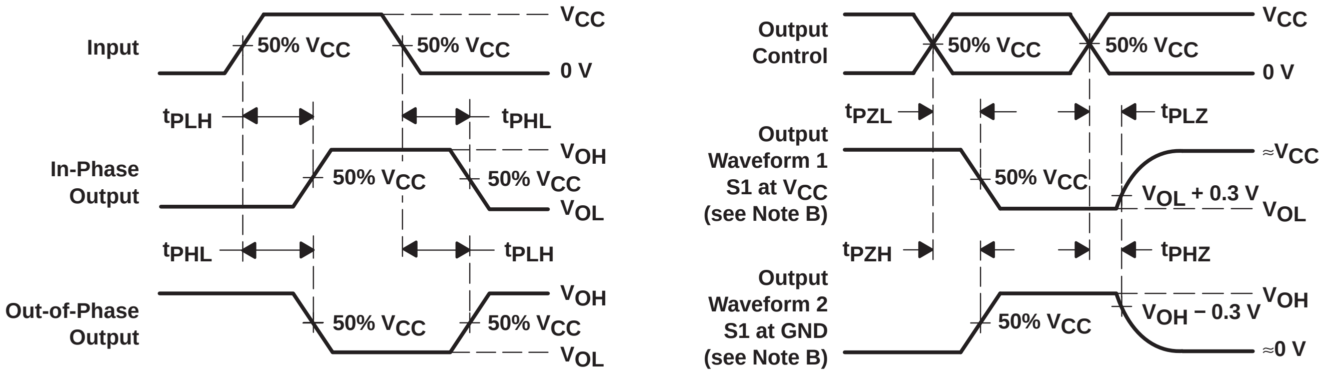
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}


t_w
Input
50% V_{CC}
50% V_{CC}
V_{CC}
0 V
Timing Input
50% V_{CC}
V_{CC}
0 V
t_{su}
t_h
Data Input
50% V_{CC}
50% V_{CC}
V_{CC}
0 V

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
50% V_{CC}
50% V_{CC}
V_{CC}
0 V
t_{PLH}
t_{PHL}
In-Phase
Output
50% V_{CC}
50% V_{CC}
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Out-of-Phase
Output
50% V_{CC}
50% V_{CC}
V_{OH}
V_{OL}
Output
Control
50% V_{CC}
50% V_{CC}
V_{CC}
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at V_{CC}
(see Note B)
50% V_{CC}
≈V_{CC}
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at GND
(see Note B)
50% V_{CC}
V_{OH} − 0.3 V
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

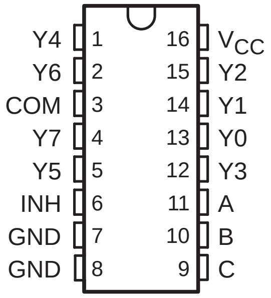
Figure 1. Load Circuit and Voltage Waveforms

SN54LV4051A, SN74LV4051A
8-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

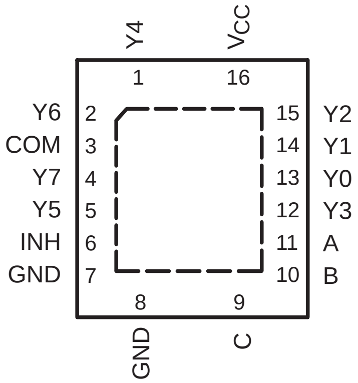
SCLS428F − MAY 1999 − REVISED AUGUST 2003

- **2-V to 5.5-V V_{CC} Operation**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54LV4051A . . . J OR W PACKAGE
SN74LV4051A . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN74LV4051A . . . RGY PACKAGE
(TOP VIEW)



description/ordering information

These 8-channel CMOS analog multiplexers/ demultiplexers are designed for 2-V to 5.5-V V_{CC} operation.

The ’LV4051A devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube of 25	SN74LV4051AN	SN74LV4051AN
	QFN − RGY	Reel of 1000	SN74LV4051ARGYR	LW051A
	SOIC − D	Tube of 40	SN74LV4051AD	LV4051A
		Reel of 2500	SN74LV4051ADR	
	SOP − NS	Reel of 2000	SN74LV4051ANSR	74LV4051A
	SSOP − DB	Reel of 2000	SN74LV4051ADBR	LW051A
	TSSOP − PW	Tube of 90	SN74LV4051APW	LW051A
		Reel of 2000	SN74LV4051APWR	
		Reel of 250	SN74LV4051APWT	
	TVSOP − DGV	Reel of 2000	SN74LV4051ADGVR	LW051A
−55°C to 125°C	CDIP − J	Tube of 25	SNJ54LV4051AJ	SNJ54LV4051AJ
	CFP − W	Tube of 150	SNJ54LV4051AW	SNJ54LV4051AW

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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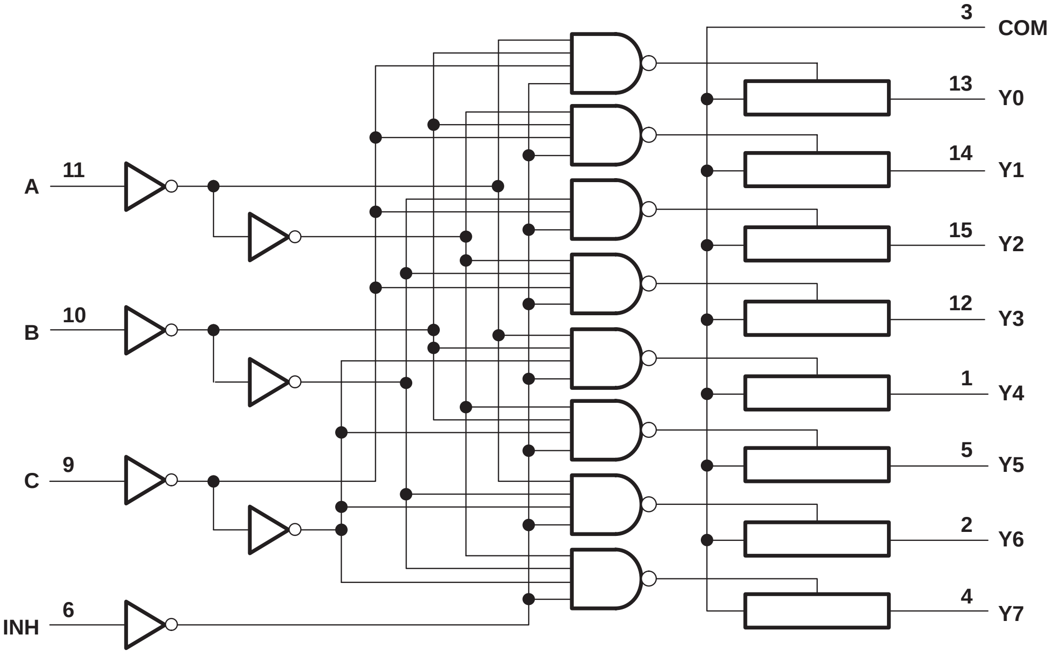
FUNCTION TABLE

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

logic diagram (positive logic)


A
11
B
10
C
9
INH
6
3
COM
13
Y0
14
Y1
15
Y2
12
Y3
1
Y4
5
Y5
2
Y6
4
Y7

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7.0 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7.0 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	−20 mA
I/O diode current, I_{IOK} ($V_{IO} < 0$ or $V_{IO} > V_{CC}$)	±50 mA
Switch through current, I_T (V_{IO} = 0 to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
(see Note 3): DB package	82°C/W
(see Note 3): DGV package	120°C/W
(see Note 3): N package	67°C/W
(see Note 3): NS package	64°C/W
(see Note 3): PW package	108°C/W
(see Note 4): RGY package	39°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LV4051A		SN74LV4051A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2‡	5.5	2‡	5.5	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		V_{CC} × 0.7		
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3		V_{CC} × 0.3	
V_I	Control input voltage		0	5.5	0	5.5	V
V_{IO}	Input/output voltage		0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

PRODUCT PREVIEW

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54LV4051A		SN74LV4051A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
r_{on}	On-state switch resistance	I_T = 2 mA, $V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ (see Figure 1)	2.3 V		38	180		225		225	Ω
			3 V		30	150		190		190	
			4.5 V		22	75		100		100	
$r_{on(p)}$	Peak on-state resistance	I_T = 2 mA, $V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$	2.3 V		113	500		600		600	Ω
			3 V		54	180		225		225	
			4.5 V		31	100		125		125	
Δr_{on}	Difference in on-state resistance between switches	I_T = 2 mA, $V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$	2.3 V		2.1	30		40		40	Ω
			3 V		1.4	20		30		30	
			4.5 V		1.3	15		20		20	
I_I	Control input current	V_I = 5.5 V or GND	0 to 5.5 V			±0.1		±1		±1	µA
$I_{S(off)}$	Off-state switch leakage current	$V_I = V_{CC}$ and V_O = GND, or V_I = GND and $V_O = V_{CC}$, $V_{INH} = V_{IH}$ (see Figure 2)	5.5 V			±0.1		±1		±1	µA
$I_{S(on)}$	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ (see Figure 3)	5.5 V			±0.1		±1		±1	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	5.5 V					20		20	µA
C_{IC}	Control input capacitance	f = 10 MHz	3.3 V		2						pF
C_{IS}	Common terminal capacitance		3.3 V		23.4						pF
C_{OS}	Switch terminal capacitance		3.3 V		5.7						pF
C_F	Feedthrough capacitance		3.3 V		0.5						pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4051A		SN74LV4051A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF, (see Figure 4)		1.9	10		16		16	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		6.6	18		23		23	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		7.4	18		23		23	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF, (see Figure 5)		3.8	12		18		18	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		7.8	28		35		35	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		11.5	28		35		35	ns

PRODUCT PREVIEW

PRODUCT PREVIEW

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4051A		SN74LV4051A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF, (see Figure 4)		1.2	6		10		10	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		4.7	12		15		15	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		5.7	12		15		15	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF, (see Figure 4)		2.5	9		12		12	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		5.5	20		25		25	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		8.8	20		25		25	ns

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4051A		SN74LV4051A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF, (see Figure 4)		0.6	4		7		7	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		3.5	8		10		10	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		4.4	8		10		10	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF, (see Figure 4)		1.5	6		8		8	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		4	14		18		18	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		6.2	14		18		18	ns

PRODUCT PREVIEW

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analog switch characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	T_A = 25°C MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Note 6 and Figure 6)		2.3 V		20		MHz
					3 V		25		
					4.5 V		35		
Crosstalk (control input to signal output)	INH	COM or Yn	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 7)		2.3 V		20		mV
					3 V		35		
					4.5 V		60		
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (see Note 7 and Figure 8)		2.3 V		−45		dB
					3 V		−45		
					4.5 V		−45		
Sine-wave distortion	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 9)	V_I = 2 V_{p-p}	2.3 V		0.1		%
				V_I = 2.5 V_{p-p}	3 V		0.1		
				V_I = 4 V_{p-p}	4.5 V		0.1		

NOTES: 6. Adjust f_{in} voltage to obtain 0-dBm output. Increase f_{in} frequency until dB meter reads −3 dB.
7. Adjust f_{in} voltage to obtain 0-dBm input.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	5.9	pF

PARAMETER MEASUREMENT INFORMATION

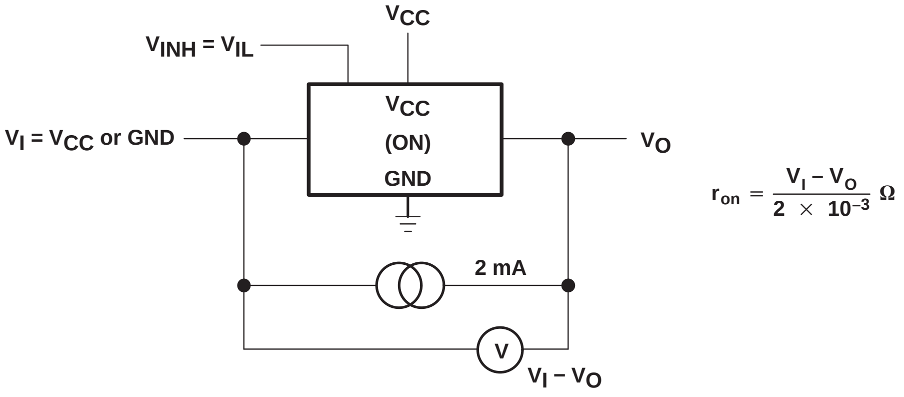
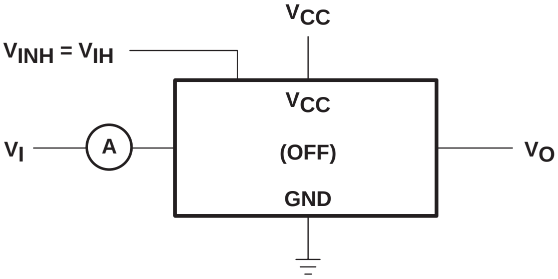


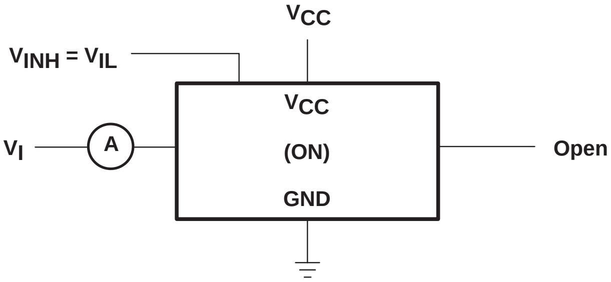
Figure 1. On-State Resistance Test Circuit

PARAMETER MEASUREMENT INFORMATION


V_{CC}
$V_{INH} = V_{IH}$
V_{CC}
V_I
A
(OFF)
V_O
GND

Condition 1: $V_I = 0$, $V_O = V_{CC}$
Condition 2: $V_I = V_{CC}$, $V_O = 0$

Figure 2. Off-State Switch Leakage-Current Test Circuit


V_{CC}
$V_{INH} = V_{IL}$
V_{CC}
V_I
A
(ON)
Open
GND

$V_I = V_{CC}$ or GND

Figure 3. On-State Switch Leakage-Current Test Circuit

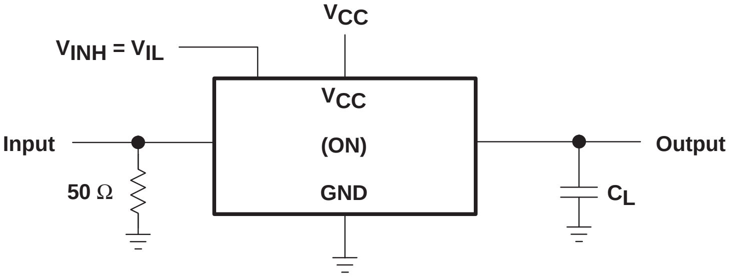
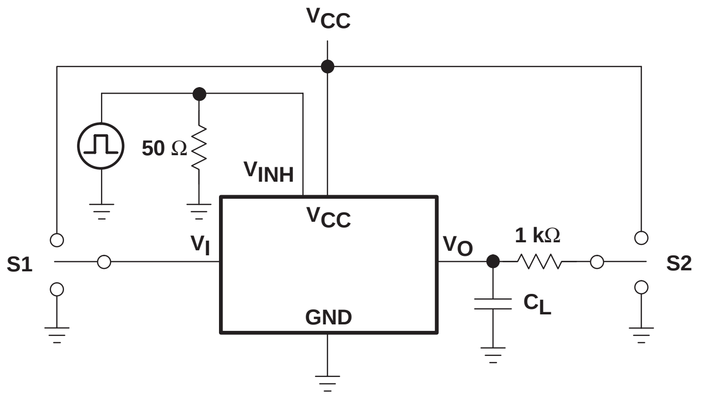

V_{CC}
$V_{INH} = V_{IL}$
V_{CC}
Input
(ON)
Output
50 Ω
GND
C_L

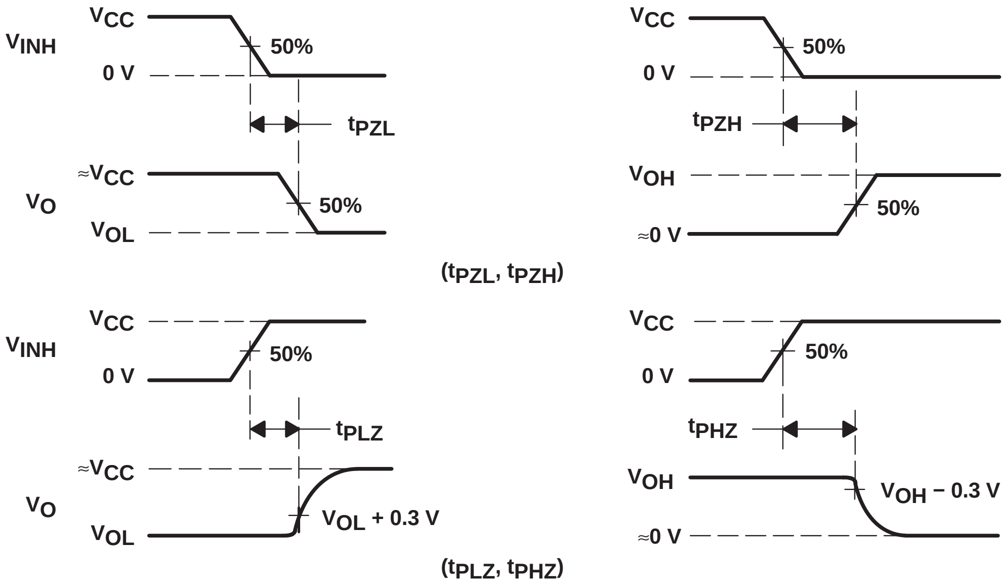
Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION


V_{CC}
50 Ω
V_{INH}
V_{CC}
V_I
V_O
1 kΩ
S1
S2
C_L
GND

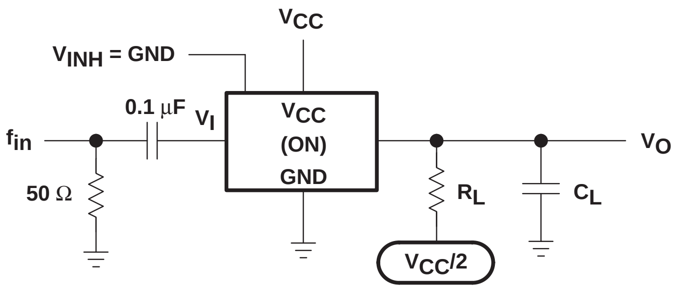
TEST	S1	S2
t_{PLZ}/t_{PZL}	GND	V_{CC}
t_{PHZ}/t_{PZH}	V_{CC}	GND

TEST CIRCUIT


V_{CC}
V_{INH}
0 V
50%
t_{PZL}
≈V_{CC}
V_O
V_{OL}
50%
V_{CC}
0 V
50%
t_{PZH}
V_{OH}
≈0 V
50%
(t_{PZL}, t_{PZH})
V_{CC}
V_{INH}
0 V
50%
t_{PLZ}
≈V_{CC}
V_O
V_{OL}
V_{OL} + 0.3 V
V_{CC}
0 V
50%
t_{PHZ}
V_{OH}
V_{OH} − 0.3 V
≈0 V
(t_{PLZ}, t_{PHZ})

VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output


V_{CC}
V_{INH} = GND
0.1 μF
V_I
V_{CC}
(ON)
GND
f_{in}
50 Ω
R_L
C_L
V_O
$V_{CC}/2$

NOTE A: f_{in} is a sine wave.

Figure 6. Frequency Response (Switch On)

PARAMETER MEASUREMENT INFORMATION

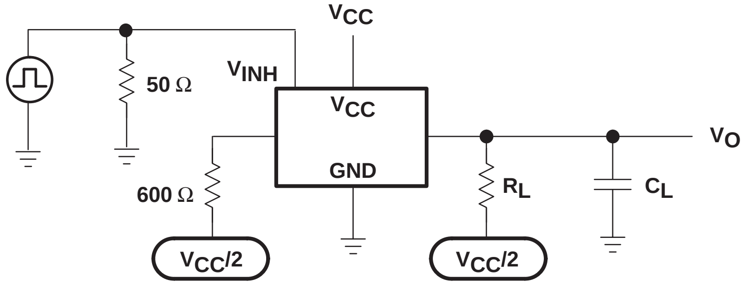

VCC
VINH
50 Ω
VCC
GND
600 Ω
VCC/2
RL
VCC/2
CL
VO

Figure 7. Crosstalk (Control Input, Switch Output)

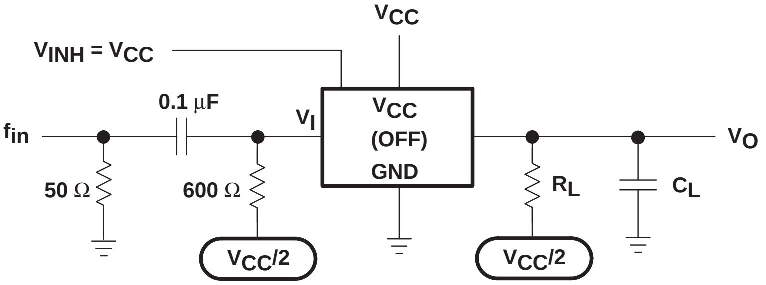

VCC
VINH = VCC
0.1 µF
fin
VI
VCC
(OFF)
GND
50 Ω
600 Ω
VCC/2
RL
VCC/2
CL
VO

Figure 8. Feedthrough Attenuation (Switch Off)

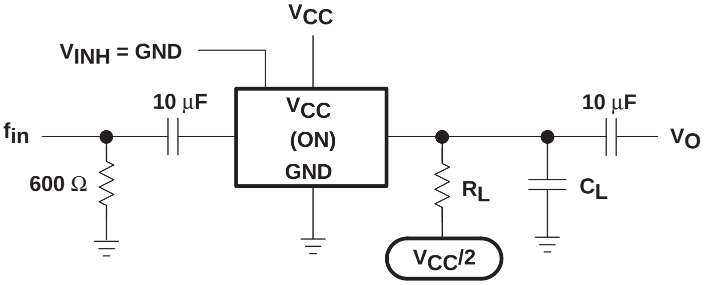

VCC
VINH = GND
10 µF
fin
VCC
(ON)
GND
600 Ω
RL
VCC/2
CL
10 µF
VO

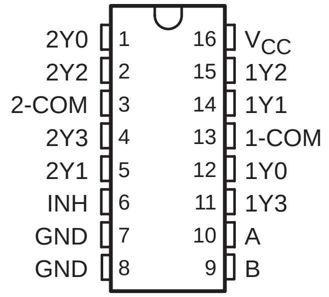
Figure 9. Sine-Wave Distortion

SN54LV4052A, SN74LV4052A
DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

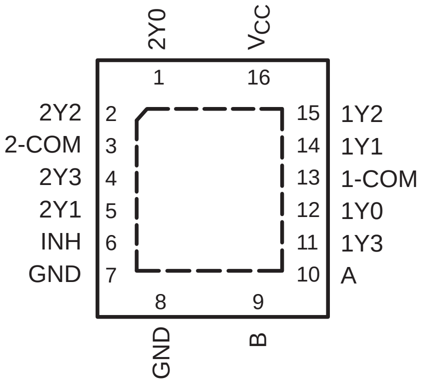
SCLS429F − MAY 1999 − REVISED AUGUST 2003

- **2-V to 5.5-V V_{CC} Operation**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Fast Switching**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Extremely Low Input Current**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54LV4052A . . . J OR W PACKAGE
SN74LV4052A . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN74LV4052A . . . RGY PACKAGE
(TOP VIEW)



description/ordering information

These dual 4-channel CMOS analog multiplexers/demultiplexers are designed for 2-V to 5.5-V V_{CC} operation.

The ’LV4052A devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube of 25	SN74LV4052AN	SN74LV4052AN
	QFN − RGY	Reel of 1000	SN74LV4052ARGYR	LW052A
	SOIC − D	Tube of 40	SN74LV4052AD	LV4052A
		Reel of 2500	SN74LV4052ADR	
	SOP − NS	Reel of 2000	SN74LV4052ANSR	74LV4052A
	SSOP − DB	Reel of 2000	SN74LV4052ADBR	LW052A
	TSSOP − PW	Tube of 90	SN74LV4052APW	LW052A
		Reel of 2000	SN74LV4052APWR	
		Reel of 250	SN74LV4052APWT	
	TVSOP − DGV	Reel of 2000	SN74LV4052ADGVR	LW052A
−55°C to 125°C	CDIP − J	Tube of 25	SNJ54LV4052AJ	SNJ54LV4052AJ
	CFP − W	Tube of 150	SNJ54LV4052AW	SNJ54LV4052AW

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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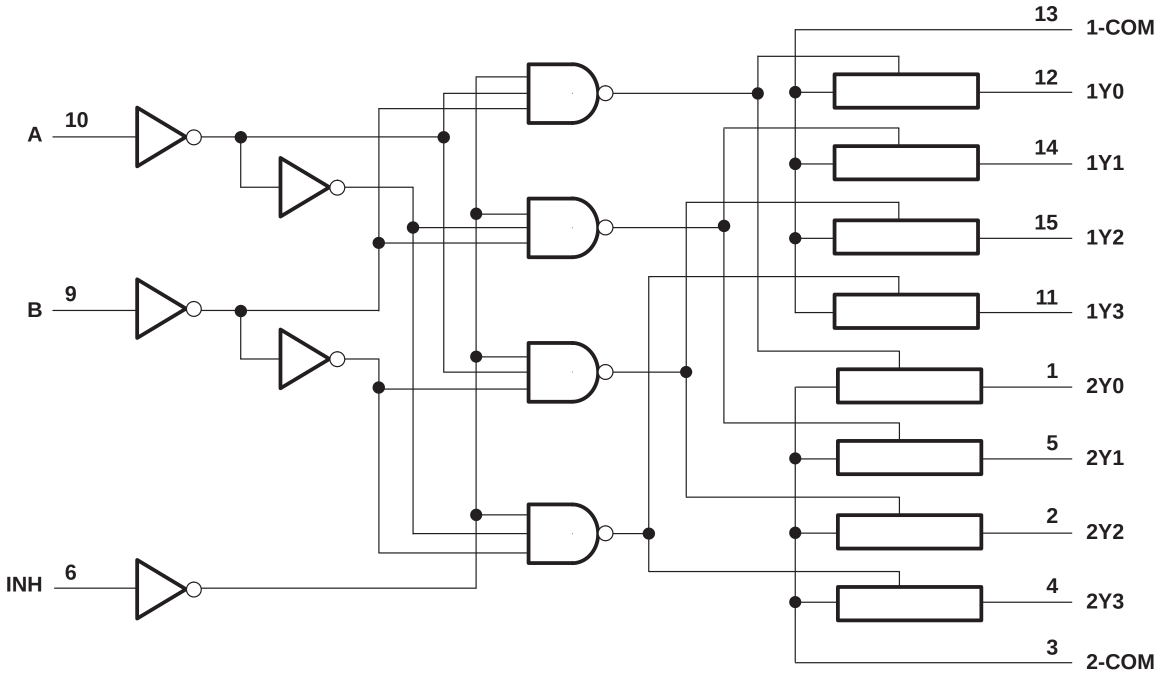
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

FUNCTION TABLE

INPUTS			ON CHANNEL
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

logic diagram (positive logic)


A
10
B
9
INH
6
13
1-COM
12
1Y0
14
1Y1
15
1Y2
11
1Y3
1
2Y0
5
2Y1
2
2Y2
4
2Y3
3
2-COM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7.0 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7.0 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2)		−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		−20 mA
I/O diode current, I_{IOK} ($V_{IO} < 0$ or $V_{IO} > V_{CC}$)		±50 mA
Switch through current, I_T (V_{IO} = 0 to V_{CC})		±25 mA
Continuous current through V_{CC} or GND		±50 mA
Package thermal impedance, θ_{JA}	(see Note 3): D package	73°C/W
	(see Note 3): DB package	82°C/W
	(see Note 3): DGV package	120°C/W
	(see Note 3): N package	67°C/W
	(see Note 3): NS package	64°C/W
	(see Note 3): PW package	108°C/W
	(see Note 4): RGY package	39°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LV4052A		SN74LV4052A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2‡	5.5	2‡	5.5	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Control input voltage		0	5.5	0	5.5	V
V_{IO}	Input/output voltage		0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

PRODUCT PREVIEW

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54LV4052A		SN74LV4052A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
r_{on}	On-state switch resistance	I_T = 2 mA, $V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ (see Figure 1)	2.3 V		43	180		225		225	Ω
			3 V		34	150		190		190	
			4.5 V		25	75		100		100	
$r_{on(p)}$	Peak on-state resistance	I_T = 2 mA, $V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$	2.3 V		133	500		600		600	Ω
			3 V		63	180		225		225	
			4.5 V		35	100		125		125	
Δr_{on}	Difference in on-state resistance between switches	I_T = 2 mA, $V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$	2.3 V		1.5	30		40		40	Ω
			3 V		1.1	20		30		30	
			4.5 V		0.7	15		20		20	
I_I	Control input current	V_I = 5.5 V or GND	0 to 5.5 V			±0.1		±1		±1	μA
$I_{S(off)}$	Off-state switch leakage current	$V_I = V_{CC}$ and V_O = GND, or V_I = GND and $V_O = V_{CC}$, $V_{INH} = V_{IH}$ (see Figure 2)	5.5 V			±0.1		±1		±1	μA
$I_{S(on)}$	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ (see Figure 3)	5.5 V			±0.1		±1		±1	μA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	5.5 V					20		20	μA
C_{IC}	Control input capacitance	f = 10 MHz	3.3 V		2.1						pF
C_{IS}	Common terminal capacitance		3.3 V		13.1						pF
C_{OS}	Switch terminal capacitance		3.3 V		5.6						pF
C_F	Feedthrough capacitance		3.3 V		0.5						pF

PRODUCT PREVIEW

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4052A		SN74LV4052A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 15 pF, (see Figure 4)		1.9	10		16		16	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 15 pF, (see Figure 5)		8	18		23		23	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 15 pF, (see Figure 5)		8.3	18		23		23	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 50 pF, (see Figure 4)		3.8	12		18		18	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 50 pF, (see Figure 5)		9.4	28		35		35	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 50 pF, (see Figure 5)		12.4	28		35		35	ns

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4052A		SN74LV4052A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 15 pF, (see Figure 4)		1.2	6		10		10	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 15 pF, (see Figure 5)		5.7	12		15		15	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 15 pF, (see Figure 5)		6.6	12		15		15	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 50 pF, (see Figure 4)		2.5	9		12		12	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 50 pF, (see Figure 5)		6.7	20		25		25	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 50 pF, (see Figure 5)		9.5	20		25		25	ns

PRODUCT PREVIEW

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4052A		SN74LV4052A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 15 pF, (see Figure 4)		0.7	4		7		7	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 15 pF, (see Figure 5)		4	8		10		10	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 15 pF, (see Figure 5)		5	8		10		10	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	C_L = 50 pF, (see Figure 4)		1.5	6		8		8	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	C_L = 50 pF, (see Figure 5)		4.7	14		18		18	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	C_L = 50 pF, (see Figure 5)		6.9	14		18		18	ns

PRODUCT PREVIEW

analog switch characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	T_A = 25°C			UNIT
						MIN	TYP	MAX	
Frequency response (switch on)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Note 6 and Figure 6)		2.3 V		30		MHz
					3 V		35		
					4.5 V		50		
Crosstalk (between any switches)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Note 7 and Figure 7)		2.3 V		−45		dB
					3 V		−45		
					4.5 V		−45		
Crosstalk (control input to signal output)	INH	COM or Y	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)		2.3 V		20		mV
					3 V		35		
					4.5 V		65		
Feedthrough attenuation (switch off)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Note 7 and Figure 9)		2.3 V		−45		dB
					3 V		−45		
					4.5 V		−45		
Sine-wave distortion	COM or Y	Y or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	V_I = 2 V_{p-p}	2.3 V		0.1		%
				V_I = 2.5 V_{p-p}	3 V		0.1		
				V_I = 4 V_{p-p}	4.5 V		0.1		

NOTES: 6. Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads −3 dB.
7. Adjust f_{in} voltage to obtain 0 dBm at input.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	11.8	pF

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PARAMETER MEASUREMENT INFORMATION

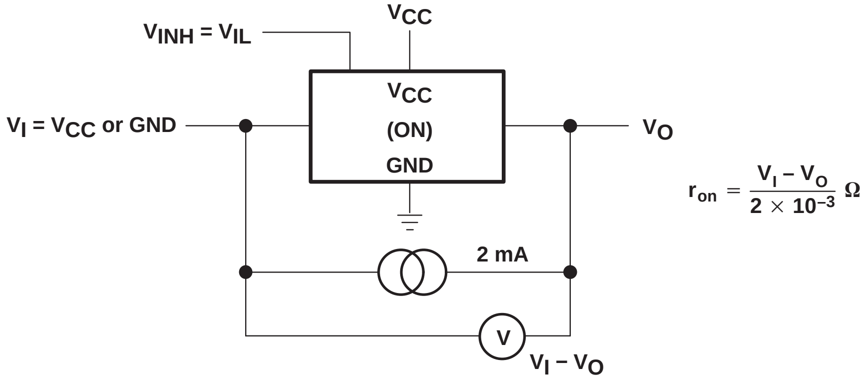
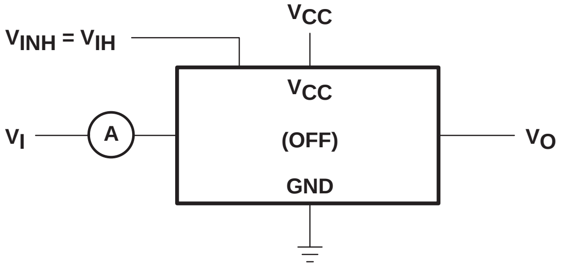
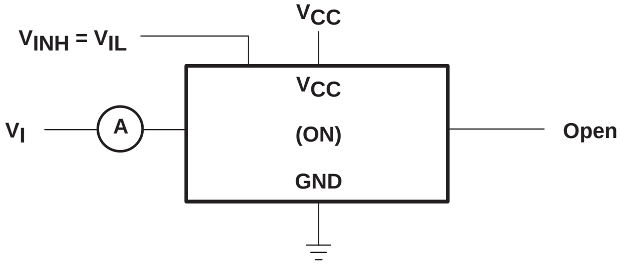

$V_{INH} = V_{IL}$
V_{CC}
V_{CC}
(ON)
GND
$V_I = V_{CC}$ or GND
V_O
$r_{on} = \frac{V_I - V_O}{2 \times 10^{-3}}\ \Omega$
2 mA
V
$V_I - V_O$

Figure 1. On-State Resistance Test Circuit


$V_{INH} = V_{IH}$
V_{CC}
V_{CC}
V_I
A
(OFF)
V_O
GND

Condition 1: $V_I = 0$, $V_O = V_{CC}$
Condition 2: $V_I = V_{CC}$, $V_O = 0$

Figure 2. Off-State Switch Leakage-Current Test Circuit


$V_{INH} = V_{IL}$
V_{CC}
V_{CC}
V_I
A
(ON)
Open
GND

$V_I = V_{CC}$ or GND

Figure 3. On-State Switch Leakage-Current Test Circuit

PARAMETER MEASUREMENT INFORMATION

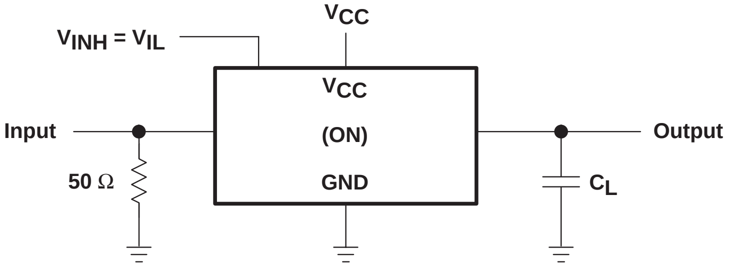
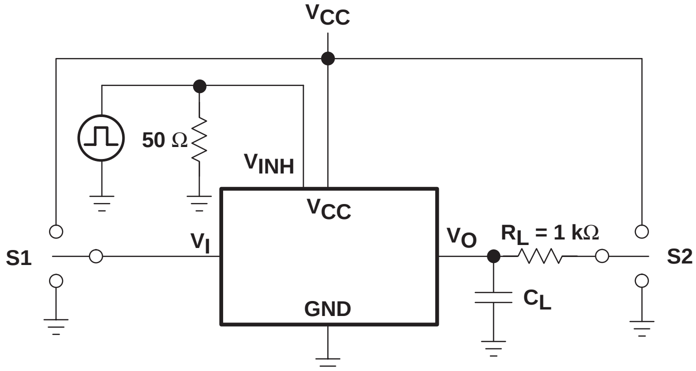
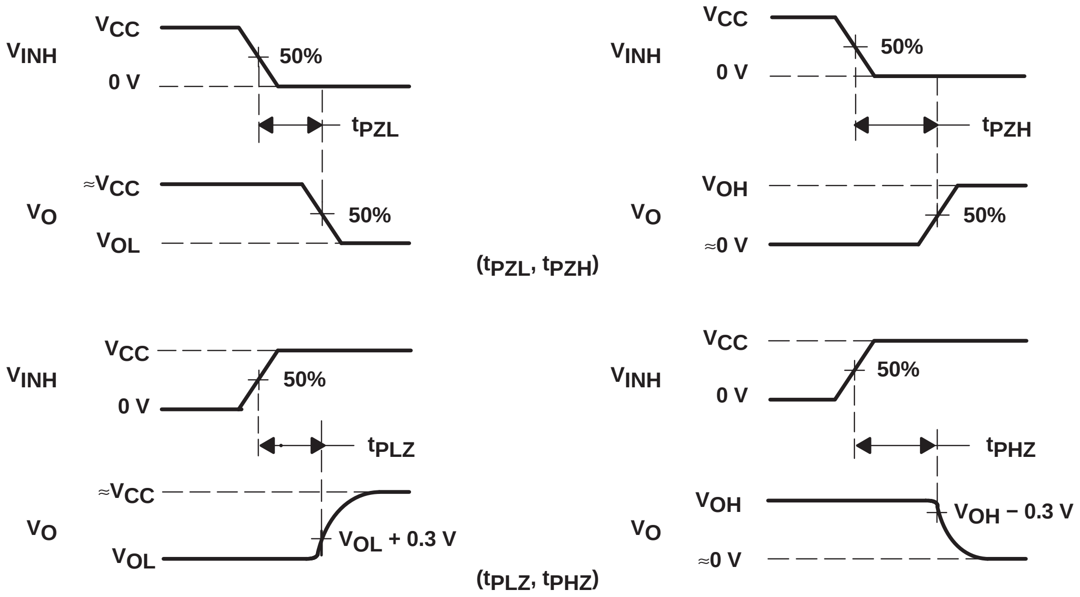

V_{CC}
$V_{INH} = V_{IL}$
V_{CC}
(ON)
GND
Input
50 Ω
Output
C_L

Figure 4. Propagation Delay Time, Signal Input to Signal Output


V_{CC}
50 Ω
V_{INH}
V_{CC}
V_I
V_O
R_L = 1 kΩ
S1
S2
C_L
GND

TEST CIRCUIT

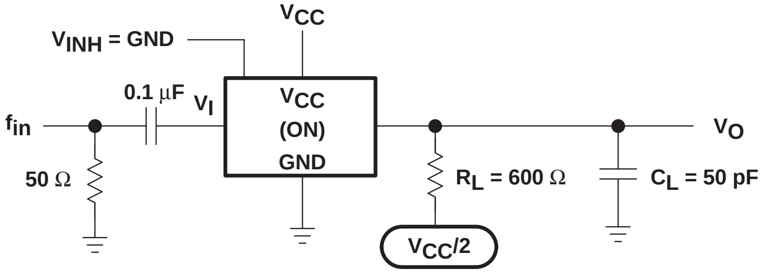
TEST	S1	S2
t_{PLZ}/t_{PZL}	GND	V_{CC}
t_{PHZ}/t_{PZH}	V_{CC}	GND



VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output

PARAMETER MEASUREMENT INFORMATION


V_{CC}
V_{INH} = GND
0.1 µF
V_I
V_{CC}
(ON)
GND
f_{in}
50 Ω
V_O
R_L = 600 Ω
C_L = 50 pF
$V_{CC}/2$

NOTE A: f_{in} is a sine wave.

Figure 6. Frequency Response (Switch On)

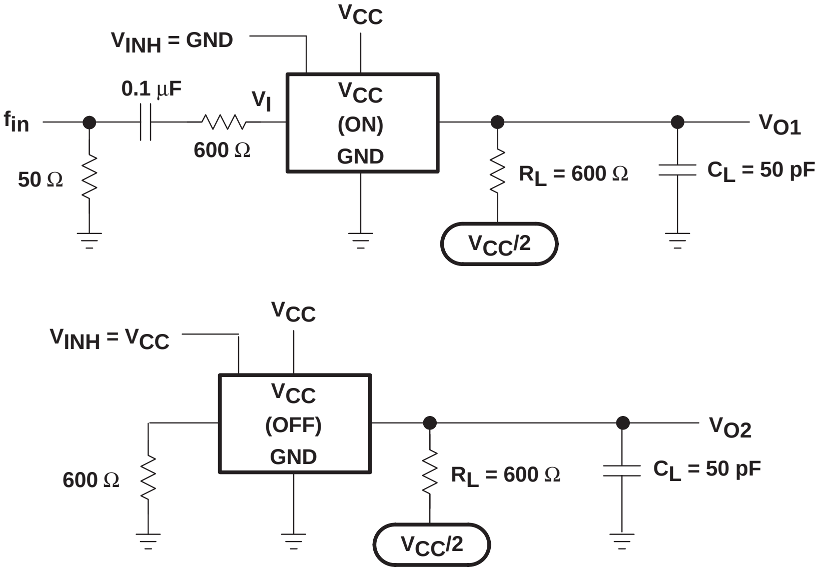

V_{CC}
V_{INH} = GND
0.1 µF
V_I
V_{CC}
(ON)
GND
f_{in}
600 Ω
50 Ω
V_{O1}
R_L = 600 Ω
C_L = 50 pF
$V_{CC}/2$
V_{CC}
V_{INH} = V_{CC}
V_{CC}
(OFF)
GND
600 Ω
V_{O2}
R_L = 600 Ω
C_L = 50 pF
$V_{CC}/2$

Figure 7. Crosstalk Between Any Two Switches

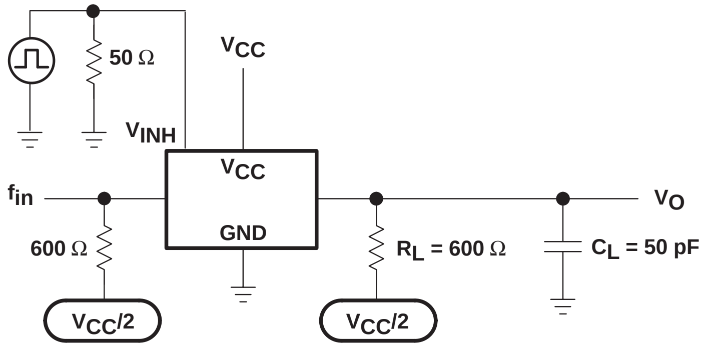

50 Ω
V_{CC}
V_{INH}
V_{CC}
GND
f_{in}
600 Ω
V_O
R_L = 600 Ω
C_L = 50 pF
$V_{CC}/2$
$V_{CC}/2$

Figure 8. Crosstalk Between Control Input and Switch Output

PARAMETER MEASUREMENT INFORMATION

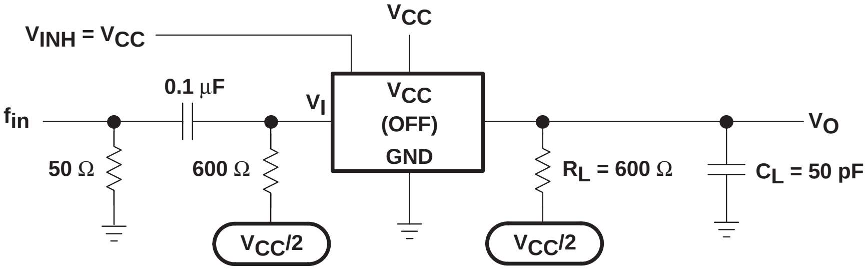

$V_{INH} = V_{CC}$
V_{CC}
0.1 μF
f_{in}
V_I
V_{CC}
(OFF)
GND
V_O
50 Ω
600 Ω
R_L = 600 Ω
C_L = 50 pF
$V_{CC}/2$
$V_{CC}/2$

Figure 9. Feedthrough Attenuation (Switch Off)

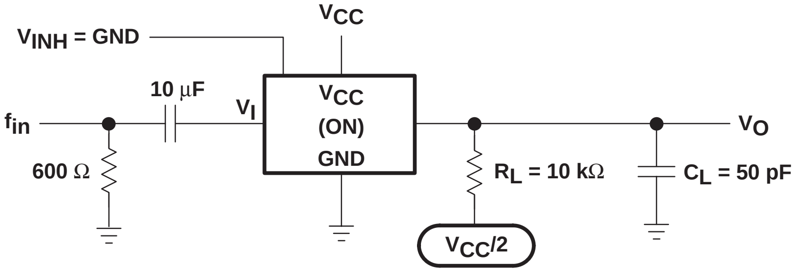

V_{INH} = GND
V_{CC}
10 μF
f_{in}
V_I
V_{CC}
(ON)
GND
V_O
600 Ω
R_L = 10 kΩ
C_L = 50 pF
$V_{CC}/2$

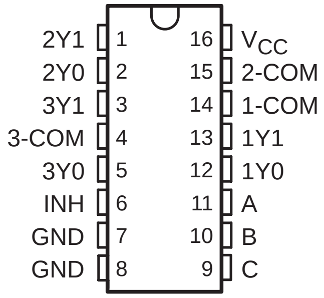
Figure 10. Sine-Wave Distortion

SN54LV4053A, SN74LV4053A
TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

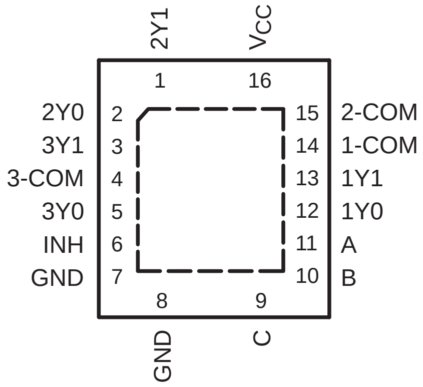
SCLS430H − MAY 1999 − REVISED AUGUST 2003

- **2-V to 5.5-V V_{CC} Operation**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54LV4053A . . . J OR W PACKAGE
SN74LV4053A . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN74LV4053A . . . RGY PACKAGE
(TOP VIEW)



description/ordering information

These triple 2-channel CMOS analog multiplexers/demultiplexers are designed for 2-V to 5.5-V V_{CC} operation.

The ’LV4053A devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube of 25	SN74LV4053AN	SN74LV4053AN
	QFN − RGY	Reel of 1000	SN74LV4053ARGYR	LW053A
	SOIC − D	Tube of 40	SN74LV4053AD	LV4053A
		Reel of 2500	SN74LV4053ADR	
	SOP − NS	Reel of 2000	SN74LV4053ANSR	74LV4053A
	SSOP − DB	Reel of 2000	SN74LV4053ADBR	LW053A
	TSSOP − PW	Tube of 90	SN74LV4053APW	LW053A
		Reel of 2000	SN74LV4053APWR	
		Reel of 250	SN74LV4053APWT	
	TVSOP − DGV	Reel of 2000	SN74LV4053ADGVR	LW053A
−55°C to 125°C	CDIP − J	Tube of 25	SNJ54LV4053AJ	SNJ54LV4053AJ
	CFP − W	Tube of 150	SNJ54LV4053AW	SNJ54LV4053AW

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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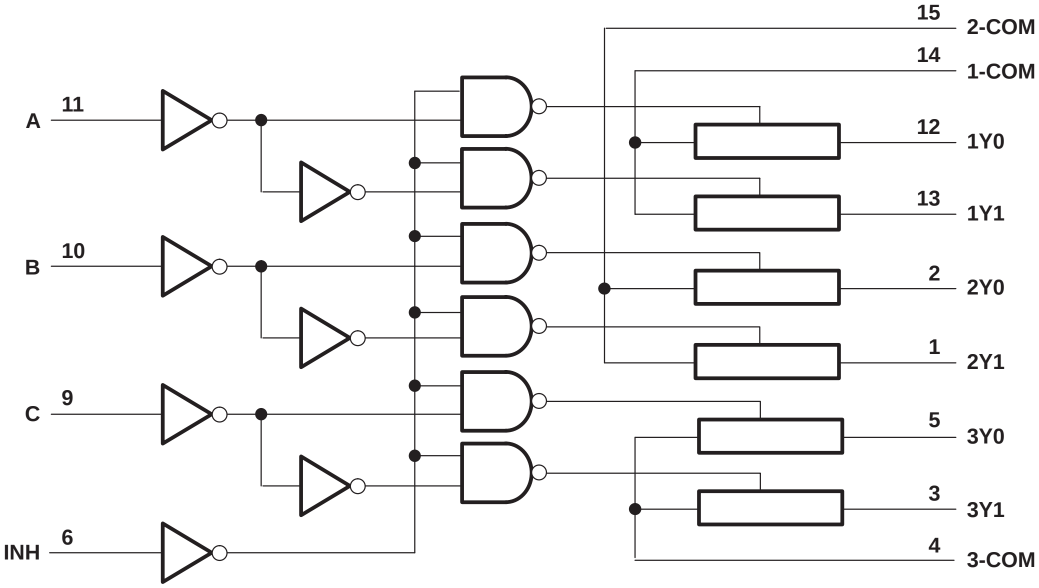
FUNCTION TABLE

INPUTS				ON CHANNELS
INH	C	B	A	
L	L	L	L	1Y0, 2Y0, 3Y0
L	L	L	H	1Y1, 2Y0, 3Y0
L	L	H	L	1Y0, 2Y1, 3Y0
L	L	H	H	1Y1, 2Y1, 3Y0
L	H	L	L	1Y0, 2Y0, 3Y1
L	H	L	H	1Y1, 2Y0, 3Y1
L	H	H	L	1Y0, 2Y1, 3Y1
L	H	H	H	1Y1, 2Y1, 3Y1
H	X	X	X	None

logic diagram (positive logic)


15
2-COM
14
1-COM
A
11
12
1Y0
13
1Y1
B
10
2
2Y0
1
2Y1
C
9
5
3Y0
3
3Y1
INH
6
4
3-COM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		−0.5 V to 7.0 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7.0 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2)		−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		−20 mA
I/O diode current, I_{IOK} ($V_{IO} < 0$ or $V_{IO} > V_{CC}$)		±50 mA
Switch through current, I_T (V_{IO} = 0 to V_{CC})		±25 mA
Continuous current through V_{CC} or GND		±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	D package	73°C/W
(see Note 3):	DB package	82°C/W
(see Note 3):	DGV package	120°C/W
(see Note 3):	NS package	64°C/W
(see Note 3):	PW package	108°C/W
(see Note 4):	RGY package	39°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN74LV4053A		SN74LV4053A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2‡	5.5	2‡	5.5	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Control input voltage		0	5.5	0	5.5	V
V_{IO}	Input/output voltage		0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54LV4053A		SN74LV4053A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
r_{on}	On-state switch resistance	I_T = 2 mA, $V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ (see Figure 1)	2.3 V		41	180		225		225	Ω
			3 V		30	150		190		190	
			4.5 V		23	75		100		100	
$r_{on(p)}$	Peak on-state resistance	I_T = 2 mA, $V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$	2.3 V		139	500		600		600	Ω
			3 V		63	180		225		225	
			4.5 V		35	100		125		125	
Δr_{on}	Difference in on-state resistance between switches	I_T = 2 mA, $V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$	2.3 V		2	30		40		40	Ω
			3 V		1.6	20		30		30	
			4.5 V		1.3	15		20		20	
I_I	Control input current	V_I = 5.5 V or GND	0 to 5.5 V			±0.1		±1		±1	µA
$I_{S(off)}$	Off-state switch leakage current	$V_I = V_{CC}$ and V_O = GND, or V_I = GND and $V_O = V_{CC}$, $V_{INH} = V_{IH}$ (see Figure 2)	5.5 V			±0.1		±1		±1	µA
$I_{S(on)}$	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IH}$ (see Figure 3)	5.5 V			±0.1		±1		±1	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	5.5 V					20		20	µA
C_{IC}	Control input capacitance				2						pF
C_{IS}	Common terminal capacitance				8.2						pF
C_{OS}	Switch terminal capacitance				5.6						pF
C_F	Feedthrough capacitance				0.5						pF

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4053A		SN74LV4053A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF, (see Figure 4)		2.5	10		16		16	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		7.6	18		23		23	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		7.7	18		23		23	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF, (see Figure 4)		4.4	12		18		18	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		8.8	28		35		35	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		11.7	28		35		35	ns

PRODUCT PREVIEW

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4053A		SN74LV4053A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF, (see Figure 4)		1.6	6		10		10	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		5.3	12		15		15	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		6.1	12		15		15	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF, (see Figure 4)		2.9	9		12		12	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		6.1	20		25		25	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		8.9	20		25		25	ns

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4053A		SN74LV4053A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF, (see Figure 4)		0.9	4		7		7	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		3.8	8		10		10	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		4.6	8		10		10	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF, (see Figure 4)		1.8	6		8		8	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		4.3	14		18		18	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		6.3	14		18		18	ns

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

analog switch characteristics

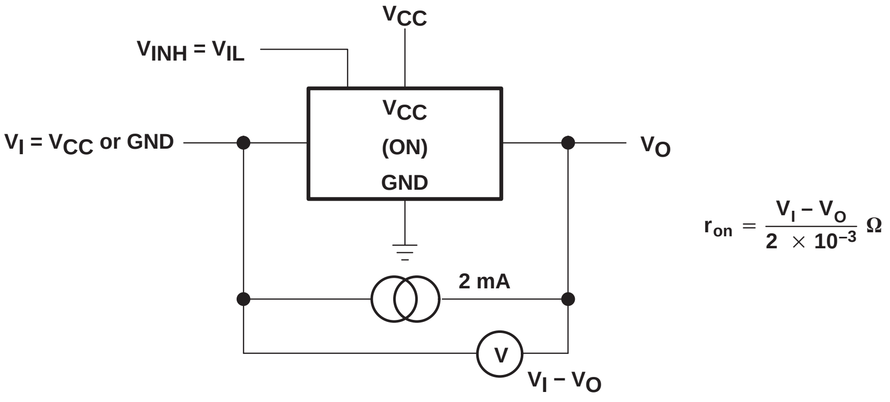
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	T_A = 25°C MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Note 6 and Figure 6)		2.3 V		30		MHz
					3 V		35		
					4.5 V		50		
Crosstalk (between any switches)	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Note 7 and Figure 7)		2.3 V		−45		dB
					3 V		−45		
					4.5 V		−45		
Crosstalk (control input to signal output)	INH	COM or Yn	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)		2.3 V		20		mV
					3 V		35		
					4.5 V		65		
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (see Note 7 and Figure 9)		2.3 V		−45		dB
					3 V		−45		
					4.5 V		−45		
Sine-wave distortion	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	V_I = 2 V_{p-p}	2.3 V		0.1		%
				V_I = 2.5 V_{p-p}	3 V		0.1		
				V_I = 4 V_{p-p}	4.5 V		0.1		

NOTES: 6. Adjust f_{in} voltage to obtain 0-dBm output. Increase f_{in} frequency until dB meter reads −3 dB.
7. Adjust f_{in} voltage to obtain 0-dBm input.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	5.3	pF

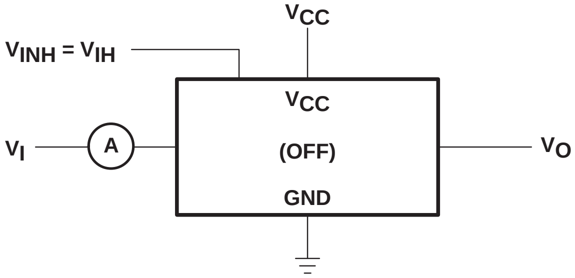
PARAMETER MEASUREMENT INFORMATION



$$r_{on} = \frac{V_I - V_O}{2 \times 10^{-3}}\ \Omega$$

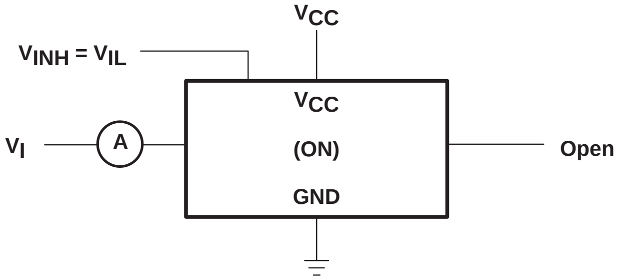
Figure 1. On-State Resistance Test Circuit

PARAMETER MEASUREMENT INFORMATION


V_{CC}
$V_{INH} = V_{IH}$
V_{CC}
V_I
A
(OFF)
V_O
GND

Condition 1: $V_I = 0$, $V_O = V_{CC}$
Condition 2: $V_I = V_{CC}$, $V_O = 0$

Figure 2. Off-State Switch Leakage-Current Test Circuit


V_{CC}
$V_{INH} = V_{IL}$
V_{CC}
V_I
A
(ON)
Open
GND

$V_I = V_{CC}$ or GND

Figure 3. On-State Switch Leakage-Current Test Circuit

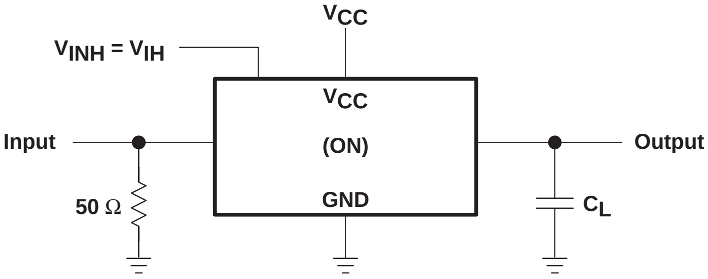
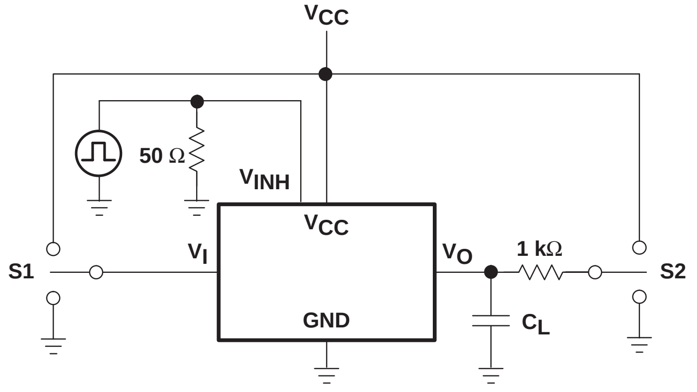

V_{CC}
$V_{INH} = V_{IH}$
V_{CC}
Input
(ON)
Output
50 Ω
GND
C_L

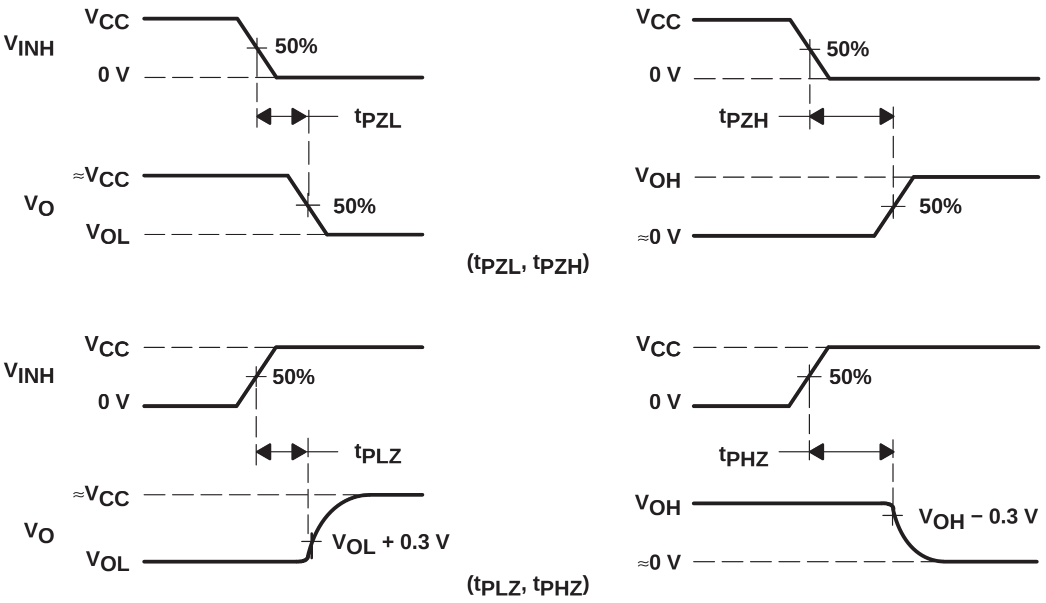
Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION


V_{CC}
50 Ω
V_{INH}
V_{CC}
S1
V_I
V_O
1 kΩ
S2
GND
C_L

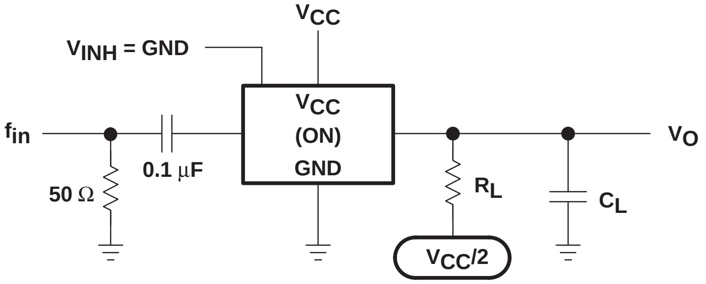
TEST	S1	S2
t_{PLZ}/t_{PZL}	GND	V_{CC}
t_{PHZ}/t_{PZH}	V_{CC}	GND

TEST CIRCUIT


V_{INH}
V_{CC}
0 V
50%
t_{PZL}
V_O
≈V_{CC}
V_{OL}
50%
V_{CC}
0 V
50%
t_{PZH}
V_{OH}
≈0 V
50%
(t_{PZL}, t_{PZH})
V_{INH}
V_{CC}
0 V
50%
t_{PLZ}
V_O
≈V_{CC}
V_{OL}
V_{OL} + 0.3 V
V_{CC}
0 V
50%
t_{PHZ}
V_{OH}
≈0 V
V_{OH} − 0.3 V
(t_{PLZ}, t_{PHZ})

VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output


V_{CC}
V_{INH} = GND
V_{CC}
(ON)
GND
f_{in}
0.1 µF
50 Ω
R_L
$V_{CC}/2$
C_L
V_O

NOTE A: f_{in} is a sine wave.

Figure 6. Frequency Response (Switch On)

PARAMETER MEASUREMENT INFORMATION

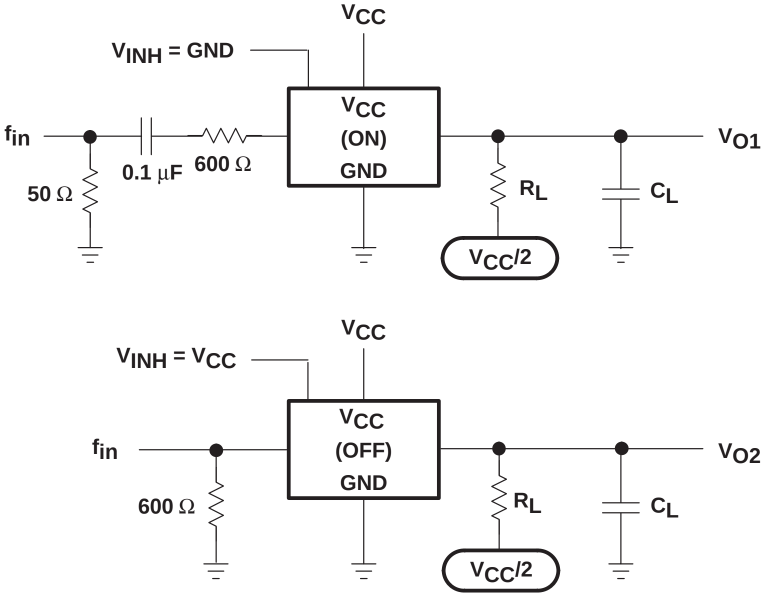

V_{CC}
V_{INH} = GND
V_{CC}
(ON)
GND
f_{in}
0.1 µF
600 Ω
50 Ω
V_{O1}
R_L
C_L
$V_{CC}/2$
V_{CC}
V_{INH} = V_{CC}
V_{CC}
(OFF)
GND
f_{in}
600 Ω
V_{O2}
R_L
C_L
$V_{CC}/2$

Figure 7. Crosstalk Between Any Two Switches

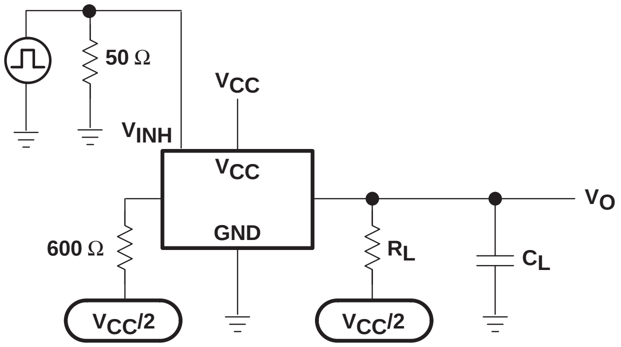

50 Ω
V_{CC}
V_{INH}
V_{CC}
GND
600 Ω
V_O
R_L
C_L
$V_{CC}/2$
$V_{CC}/2$

Figure 8. Crosstalk Between Control Input and Switch Output

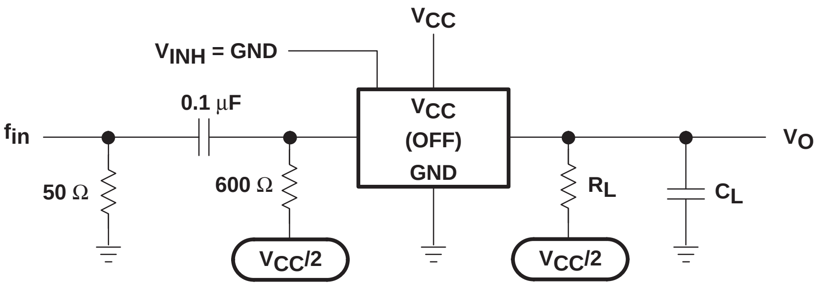

V_{CC}
V_{INH} = GND
0.1 µF
V_{CC}
(OFF)
GND
f_{in}
50 Ω
600 Ω
V_O
R_L
C_L
$V_{CC}/2$
$V_{CC}/2$

Figure 9. Feedthrough Attenuation (Switch Off)

PARAMETER MEASUREMENT INFORMATION

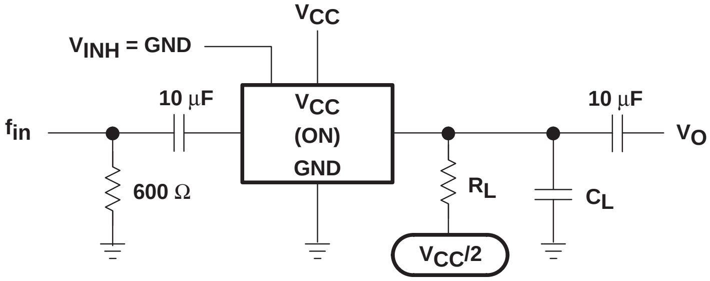

V_{CC}
V_{INH} = GND
10 μF
V_{CC}
(ON)
GND
10 μF
f_{in}
V_O
600 Ω
R_L
C_L
$V_{CC}/2$

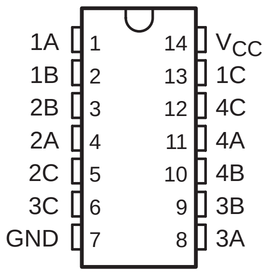
Figure 10. Sine-Wave Distortion

SN54LV4066A, SN74LV4066A
QUADRUPLE BILATERAL ANALOG SWITCHES

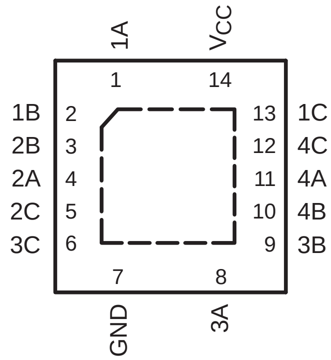
SCLS427G − APRIL 1999 − REVISED AUGUST 2003

- **2-V to 5.5-V V_{CC} Operation**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54LV4066A . . . J OR W PACKAGE
SN74LV4066A . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN74LV4066A . . . RGY PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

This quadruple silicon-gate CMOS analog switch is designed for 2-V to 5.5-V V_{CC} operation.

These switches are designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube of 25	SN74LV4066AN	SN74LV4066AN
	QFN − RGY	Reel of 1000	SN74LV4066ARGYR	LW066A
	SOIC − D	Tube of 50	SN74LV4066AD	LV4066A
		Reel of 2500	SN74LV4066ADR	
	SOP − NS	Reel of 2000	SN74LV4066ANSR	74LV4066A
	SSOP − DB	Reel of 2000	SN74LV4066ADBR	LW066A
	TSSOP − PW	Tube of 90	SN74LV4066APW	LW066A
		Reel of 2000	SN74LV4066APWR	
		Reel of 250	SN74LV4066APWT	
	TVSOP − DGV	Reel of 2000	SN74LV4066ADGVR	LW066A
−55°C to 125°C	CDIP − J	Tube of 25	SNJ54LV4066AJ	SNJ54LV4066AJ
	CFP − W	Tube of 150	SNJ54LV4066AW	SNJ54LV4066AW

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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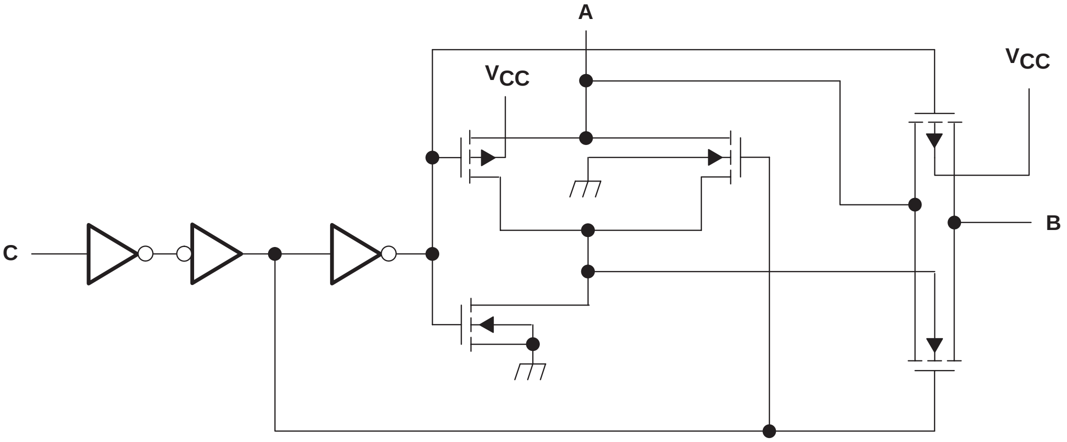
FUNCTION TABLE
(each switch)

INPUT CONTROL (C)	SWITCH
L	OFF
H	ON

logic diagram (positive logic)



One of Four Switches

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)		−0.5 V to 7 V
Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2)		−0.5 V to V_{CC} + 0.5 V
Control-input clamp current, I_{IK} ($V_I < 0$)		−20 mA
I/O diode current, I_{IOK} ($V_{IO} < 0$ or $V_{IO} > V_{CC}$)		±50 mA
On-state switch current, I_T (V_{IO} = 0 to V_{CC})		±25 mA
Continuous current through V_{CC} or GND		±50 mA
Package thermal impedance, θ_{JA}	(see Note 3): D package	86°C/W
	(see Note 3): DB package	96°C/W
	(see Note 3): DGV package	127°C/W
	(see Note 3): N package	80°C/W
	(see Note 3): NS package	76°C/W
	(see Note 3): PW package	113°C/W
	(see Note 4): RGY package	47°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LV4066A		SN74LV4066A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2†	5.5	2†	5.5	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Control input voltage		0	5.5	0	5.5	V
V_{IO}	Input/output voltage		0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

† With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. Only digital signals should be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54LV4066A		SN74LV4066A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
r_{on}	On-state switch resistance	$I_T = -1$ mA, $V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see Figure 1)	2.3 V		38	180		225		225	Ω
			3 V		29	150		190		190	
			4.5 V		21	75		100		100	
$r_{on(p)}$	Peak on-state resistance	$I_T = -1$ mA, $V_I = V_{CC}$ to GND, $V_C = V_{IH}$	2.3 V		143	500		600		600	Ω
			3 V		57	180		225		225	
			4.5 V		31	100		125		125	
Δr_{on}	Difference in on-state resistance between switches	$I_T = -1$ mA, $V_I = V_{CC}$ to GND, $V_C = V_{IH}$	2.3 V		6	30		40		40	Ω
			3 V		3	20		30		30	
			4.5 V		2	15		20		20	
I_I	Control input current	V_I = 5.5 V or GND	0 to 5.5 V			±0.1		±1		±1	µA
$I_{S(off)}$	Off-state switch leakage current	$V_I = V_{CC}$ and V_O = GND, or V_I = GND and $V_O = V_{CC}$, $V_C = V_{IL}$ (see Figure 2)	5.5 V			±0.1		±1		±1	µA
$I_{S(on)}$	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see Figure 3)	5.5 V			±0.1		±1		±1	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	5.5 V					20		20	µA
C_{ic}	Control input capacitance				1.5						pF
C_{io}	Switch input/output capacitance				5.5						pF
C_F	Feed-through capacitance				0.5						pF

PRODUCT PREVIEW

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4066A		SN74LV4066A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	A or B	B or A	C_L = 15 pF, (see Figure 4)		1.2	10		16		16	ns
t_{PZH} t_{PZL}	Switch turn-on time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		3.3	15		20		20	ns
t_{PLZ} t_{PHZ}	Switch turn-off time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		6	15		23		23	ns
t_{PLH} t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50 pF, (see Figure 4)		2.6	12		18		18	ns
t_{PZH} t_{PZL}	Switch turn-on time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		4.2	25		32		32	ns
t_{PLZ} t_{PHZ}	Switch turn-off time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		9.6	25		32		32	ns

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4066A		SN74LV4066A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	A or B	B or A	C_L = 15 pF, (see Figure 4)		0.8	6		10		10	ns
t_{PZH} t_{PZL}	Switch turn-on time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		2.3	11		15		15	ns
t_{PLZ} t_{PHZ}	Switch turn-off time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		4.5	11		15		15	ns
t_{PLH} t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50 pF, (see Figure 4)		1.5	9		12		12	ns
t_{PZH} t_{PZL}	Switch turn-on time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		3	18		22		22	ns
t_{PLZ} t_{PHZ}	Switch turn-off time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		7.2	18		22		22	ns

PRODUCT PREVIEW

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4066A		SN74LV4066A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	A or B	B or A	C_L = 15 pF, (see Figure 4)		0.3	4		7		7	ns
t_{PZH} t_{PZL}	Switch turn-on time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		1.6	7		10		10	ns
t_{PLZ} t_{PHZ}	Switch turn-off time	C	A or B	C_L = 15 pF, R_L = 1 kΩ (see Figure 5)		3.2	7		10		10	ns
t_{PLH} t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50 pF, (see Figure 4)		0.6	6		8		8	ns
t_{PZH} t_{PZL}	Switch turn-on time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		2.1	12		16		16	ns
t_{PLZ} t_{PHZ}	Switch turn-off time	C	A or B	C_L = 50 pF, R_L = 1 kΩ (see Figure 5)		5.1	12		16		16	ns

PRODUCT PREVIEW

analog switch characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	T_A = 25°C			UNIT
						MIN	TYP	MAX	
Frequency response (switch on)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) $20\log_{10}(V_O/V_I) = -3$ dB (see Figure 6)		2.3 V		30		MHz
					3 V		35		
					4.5 V		50		
Crosstalk (between any switches)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)		2.3 V		−45		dB
					3 V		−45		
					4.5 V		−45		
Crosstalk (control input to signal output)	C	A or B	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)		2.3 V		15		mV
					3 V		20		
					4.5 V		50		
Feed-through attenuation (switch off)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (see Figure 9)		2.3 V		−40		dB
					3 V		−40		
					4.5 V		−40		
Sine-wave distortion	A or B	B or A	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	$V_I = 2\ V_{p-p}$	2.3 V		0.1		%
				$V_I = 2.5\ V_{p-p}$	3 V		0.1		
				$V_I = 4\ V_{p-p}$	4.5 V		0.1		

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	4.5	pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

PARAMETER MEASUREMENT INFORMATION

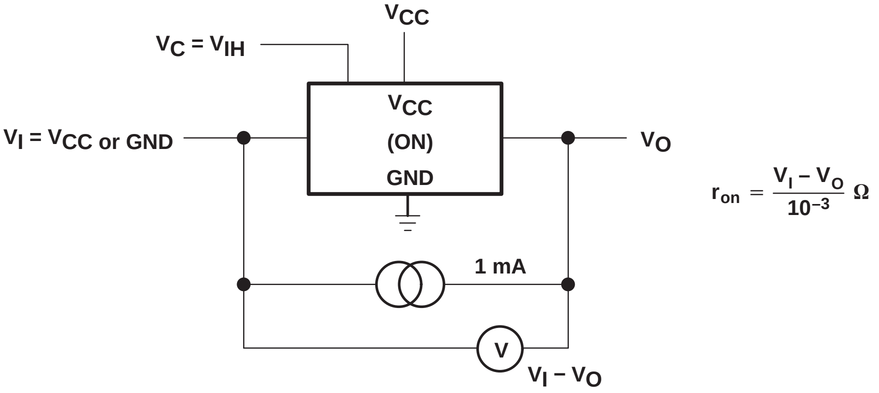
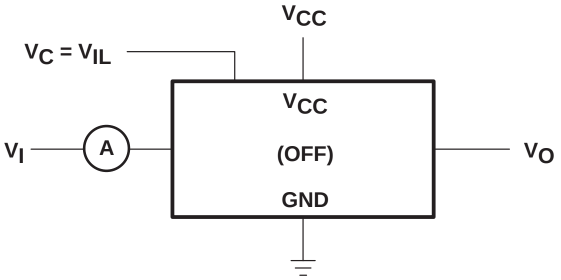
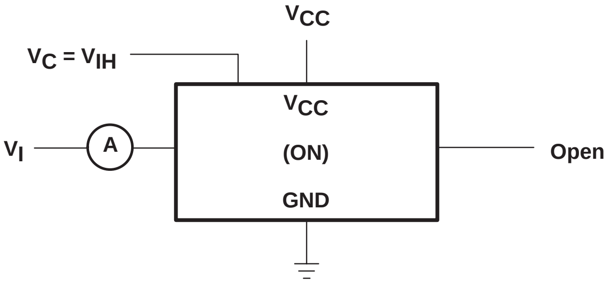

V_{CC}
$V_C = V_{IH}$
V_{CC}
(ON)
GND
$V_I = V_{CC}$ or GND
V_O
$r_{on} = \frac{V_I - V_O}{10^{-3}}\ \Omega$
1 mA
V
$V_I - V_O$

Figure 1. On-State Resistance Test Circuit


V_{CC}
$V_C = V_{IL}$
V_{CC}
V_I
A
(OFF)
V_O
GND

Condition 1: $V_I = 0$, $V_O = V_{CC}$
Condition 2: $V_I = V_{CC}$, $V_O = 0$

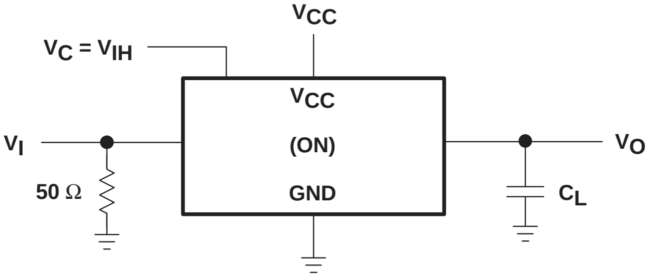
Figure 2. Off-State Switch Leakage-Current Test Circuit


V_{CC}
$V_C = V_{IH}$
V_{CC}
V_I
A
(ON)
Open
GND

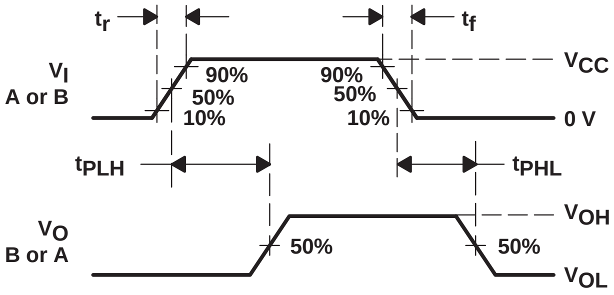
$V_I = V_{CC}$ or GND

Figure 3. On-State Leakage-Current Test Circuit

PARAMETER MEASUREMENT INFORMATION


VCC
VC = VIH
VCC
(ON)
GND
VI
50 Ω
VO
CL

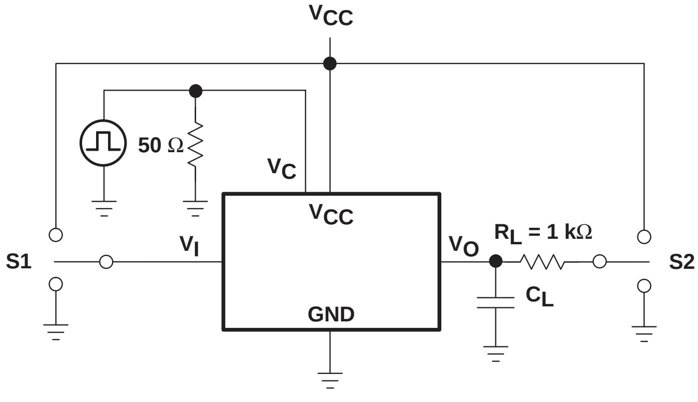
TEST CIRCUIT


tr
tf
VI
A or B
90%
50%
10%
90%
50%
10%
VCC
0 V
tPLH
tPHL
VO
B or A
50%
50%
VOH
VOL

VOLTAGE WAVEFORMS

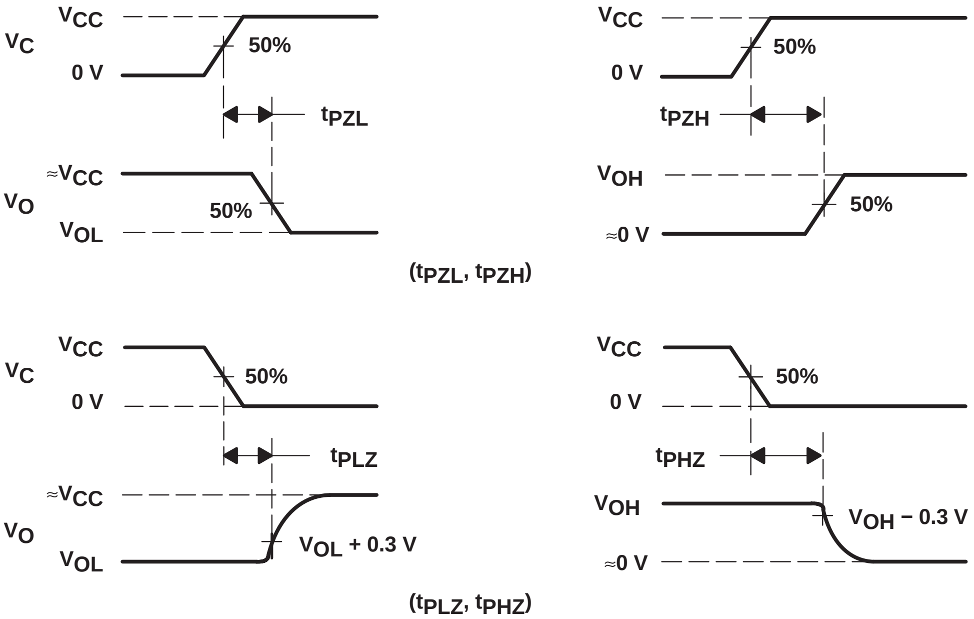
Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION


V_{CC}
50 Ω
V_C
V_{CC}
S1
V_I
V_O
R_L = 1 kΩ
S2
C_L
GND

TEST	S1	S2
t_{PZL}	GND	V_{CC}
t_{PZH}	V_{CC}	GND
t_{PLZ}	GND	V_{CC}
t_{PHZ}	V_{CC}	GND

TEST CIRCUIT


V_{CC}
V_C
0 V
50%
t_{PZL}
≈V_{CC}
V_O
50%
V_{OL}
V_{CC}
0 V
50%
t_{PZH}
V_{OH}
50%
≈0 V
(t_{PZL}, t_{PZH})
V_{CC}
V_C
0 V
50%
t_{PLZ}
≈V_{CC}
V_O
V_{OL}
V_{OL} + 0.3 V
V_{CC}
0 V
50%
t_{PHZ}
V_{OH}
V_{OH} − 0.3 V
≈0 V
(t_{PLZ}, t_{PHZ})

VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output

PARAMETER MEASUREMENT INFORMATION

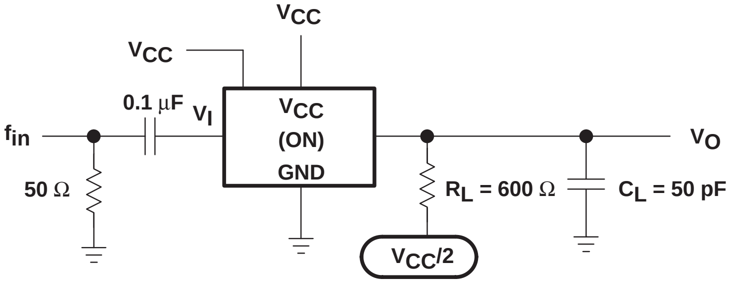

VCC
VCC
0.1 µF
VI
VCC
(ON)
GND
fin
50 Ω
RL = 600 Ω
CL = 50 pF
VO
VCC/2

Figure 6. Frequency Response (Switch On)

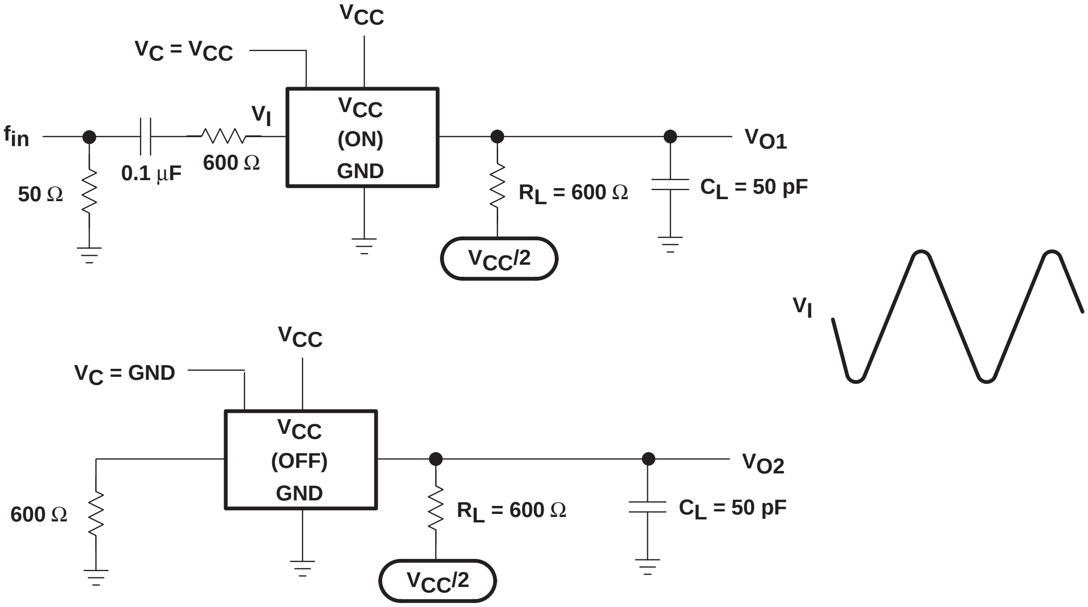

VCC
VC = VCC
VI
VCC
(ON)
GND
fin
0.1 µF
600 Ω
50 Ω
RL = 600 Ω
CL = 50 pF
VO1
VCC/2
VI
VCC
VC = GND
VCC
(OFF)
GND
600 Ω
RL = 600 Ω
CL = 50 pF
VO2
VCC/2

Figure 7. Crosstalk Between Any Two Switches

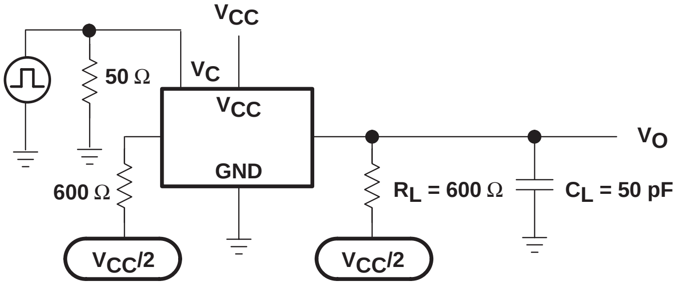

VCC
50 Ω
VC
VCC
GND
600 Ω
RL = 600 Ω
CL = 50 pF
VO
VCC/2
VCC/2

Figure 8. Crosstalk (Control Input − Switch Output)

PARAMETER MEASUREMENT INFORMATION

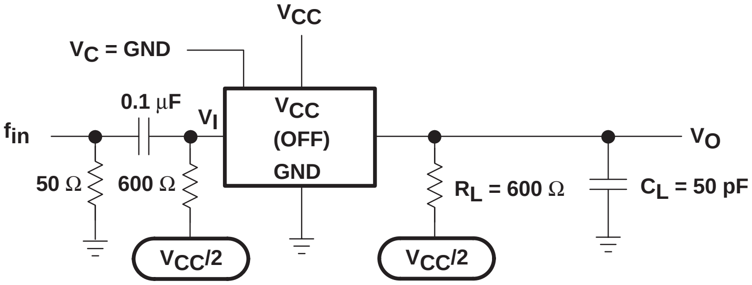

V_{CC}
V_C = GND
0.1 μF
V_I
f_{in}
V_{CC}
(OFF)
GND
V_O
50 Ω
600 Ω
R_L = 600 Ω
C_L = 50 pF
$V_{CC}/2$
$V_{CC}/2$

Figure 9. Feed-Through Attenuation (Switch Off)

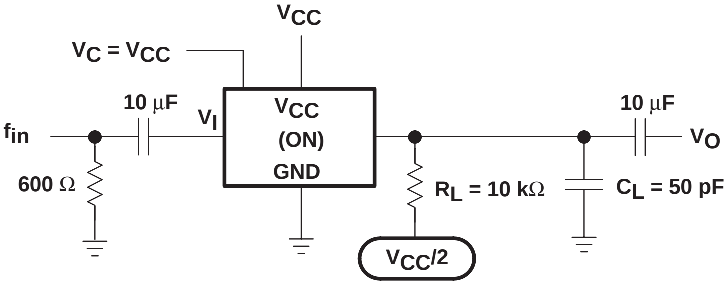

V_{CC}
V_C = V_{CC}
10 μF
V_I
f_{in}
V_{CC}
(ON)
GND
10 μF
V_O
600 Ω
R_L = 10 kΩ
C_L = 50 pF
$V_{CC}/2$

Figure 10. Sine-Wave Distortion

Insert Tab Here

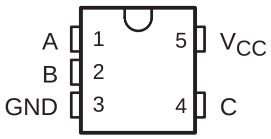
Insert Tab Here

SN74LVC1G66
SINGLE BILATERAL ANALOG SWITCH

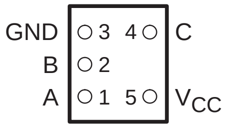
SCES323H − JUNE 2001 − REVISED SEPTEMBER 2003

- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **1.65-V to 5.5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 0.8 ns at 3.3 V**
- **High On-Off Output Voltage Ratio**
- **High Degree of Linearity**
- **High Speed, Typically 0.5 ns (V_{CC} = 3 V, C_L = 50 pF)**
- **Low On-State Resistance, Typically ≈5.5 Ω (V_{CC} = 4.5 V)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DBV OR DCK PACKAGE
(TOP VIEW)



YEA, YEP, YZA, OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

This single analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G66 can handle both analog and digital signals. The device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	NanoStar™ − WCSP (DSBGA) 0.17-mm Small Bump − YEA	Reel of 3000	SN74LVC1G66YEAR	_ _ _C6_
	NanoFree™ − WCSP (DSBGA) 0.17-mm Small Bump − YZA (Pb-free)		SN74LVC1G66YZAR	
	NanoStar™ − WCSP (DSBGA) 0.23-mm Large Bump − YEP		SN74LVC1G66YEPR	
	NanoFree™ − WCSP (DSBGA) 0.23-mm Large Bump − YZP (Pb-free)		SN74LVC1G66YZPR	
−40°C to 85°C	SOT (SOT-23) − DBV	Reel of 3000	SN74LVC1G66DBVR	C66_
		Reel of 250	SN74LVC1G66DBVT	
	SOT (SC-70) − DCK	Reel of 3000	SN74LVC1G66DCKR	C6_
		Reel of 250	SN74LVC1G66DCKT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

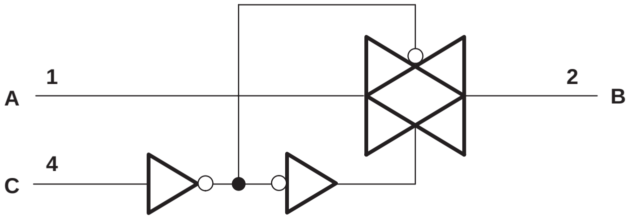
NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

FUNCTION TABLE

CONTROL INPUT (C)	SWITCH
L	OFF
H	ON

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)		−0.5 V to 6.5 V
Input voltage range, V_I (see Notes 1 and 2)		−0.5 V to 6.5 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to V_{CC} + 0.5 V
Control input clamp current, I_{IK} ($V_I < 0$)		−50 mA
I/O port diode current, I_{IOK} ($V_{I/O} < 0$ or $V_{I/O} > V_{CC}$)		±50 mA
On-state switch current, I_T ($V_{I/O} = 0$ to V_{CC})		±50 mA
Continuous current through V_{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 4):	DBV package	206°C/W
	DCK package	252°C/W
	YEA/YZA package	154°C/W
	YEP/YZP package	132°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground, unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 5.5 V maximum.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 5)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V	$V_{CC} \times 0.65$		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V		$V_{CC} \times 0.35$	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$	
V_I	Control input voltage		0	5.5	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 1.65 V to 1.95 V		20	ns/V
		V_{CC} = 2.3 V to 2.7 V		20	
		V_{CC} = 3 V to 3.6 V		10	
		V_{CC} = 4.5 V to 5.5 V		10	
T_A	Operating free-air temperature		−40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
r_{on}	On-state switch resistance	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see Figures 1 and 2)	I_S = 4 mA	1.65 V		12	30	Ω
			I_S = 8 mA	2.3 V		9	20	
			I_S = 24 mA	3 V		7.5	15	
			I_S = 32 mA	4.5 V		5.5	10	
$r_{on(p)}$	Peak on resistance	$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figures 1 and 2)	I_S = 4 mA	1.65 V		74.5	100	Ω
			I_S = 8 mA	2.3 V		20	30	
			I_S = 24 mA	3 V		11.5	20	
			I_S = 32 mA	4.5 V		7.5	15	
$I_{S(off)}$	Off-state switch leakage current	$V_I = V_{CC}$ and V_O = GND or V_I = GND and $V_O = V_{CC}$, $V_C = V_{IL}$ (see Figure 3)		5.5 V			±1	μA
							±0.1†	
$I_{S(on)}$	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$, V_O = Open (see Figure 4)		5.5 V			±1	μA
							±0.1†	
I_I	Control input current	$V_C = V_{CC}$ or GND		5.5 V			±1	μA
							±0.1†	
I_{CC}	Supply current	$V_C = V_{CC}$ or GND		5.5 V			10	μA
							1†	
ΔI_{CC}	Supply current change	$V_C = V_{CC} - 0.6$ V		5.5 V			500	μA
C_{ic}	Control input capacitance			5 V		2		pF
$C_{io(off)}$	Switch input/output capacitance			5 V		6		pF
$C_{io(on)}$	Switch input/output capacitance			5 V		13		pF

† T_A = 25°C

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}†	A or B	B or A		2		1.2		0.8		0.6	ns
t_{en}‡	C	A or B	2.5	12	1.9	6.5	1.8	5	1.5	4.2	ns
t_{dis}§	C	A or B	2.2	10	1.4	6.9	2	6.5	1.4	5	ns

† t_{PLH} and t_{PHL} are the same as t_{pd}. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

‡ t_{PZL} and t_{PZH} are the same as t_{en}.

§ t_{PLZ} and t_{PHZ} are the same as t_{dis}.

analog switch characteristics, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response¶ (switch ON)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	35	MHz
				2.3 V	120	
				3 V	175	
				4.5 V	195	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	>300	
				2.3 V	>300	
				3 V	>300	
				4.5 V	>300	
Crosstalk (control input to signal output)	C	A or B	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 7)	1.65 V	35	mV
				2.3 V	50	
				3 V	70	
				4.5 V	100	
Feed-through attenuation# (switch OFF)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 8)	1.65 V	−58	dB
				2.3 V	−58	
				3 V	−58	
				4.5 V	−58	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 8)	1.65 V	−42	
				2.3 V	−42	
				3 V	−42	
				4.5 V	−42	
Sine-wave distortion	A or B	B or A	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 9)	1.65 V	0.1	%
				2.3 V	0.025	
				3 V	0.015	
				4.5 V	0.01	
			C_L = 50 pF, R_L = 10 kΩ, f_{in} = 10 kHz (sine wave) (see Figure 9)	1.65 V	0.15	
				2.3 V	0.025	
				3 V	0.015	
				4.5 V	0.01	

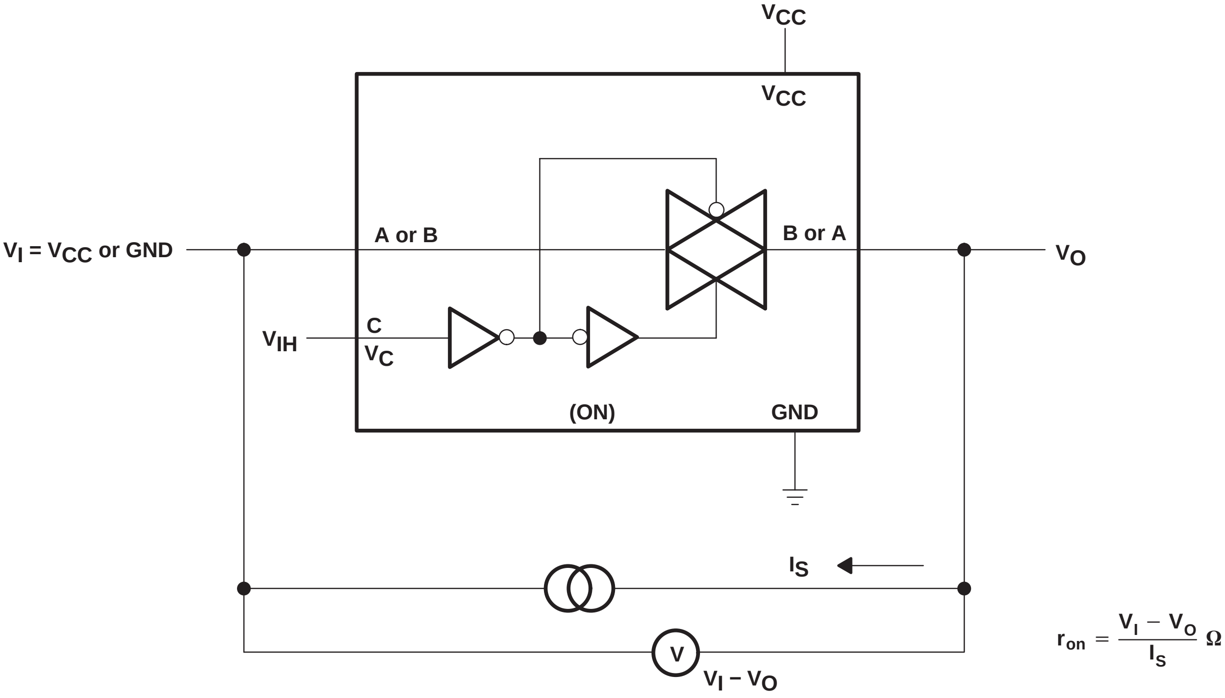
¶ Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads −3 dB.

# Adjust f_{in} voltage to obtain 0 dBm at input.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	8	9	9	11	pF

PARAMETER MEASUREMENT INFORMATION


VCC
VCC
A or B
B or A
VI = VCC or GND
VO
VIH
C
VC
(ON)
GND
IS
V
VI − VO

$$r_{on} = \frac{V_I - V_O}{I_S}\ \Omega$$

Figure 1. On-State Resistance Test Circuit

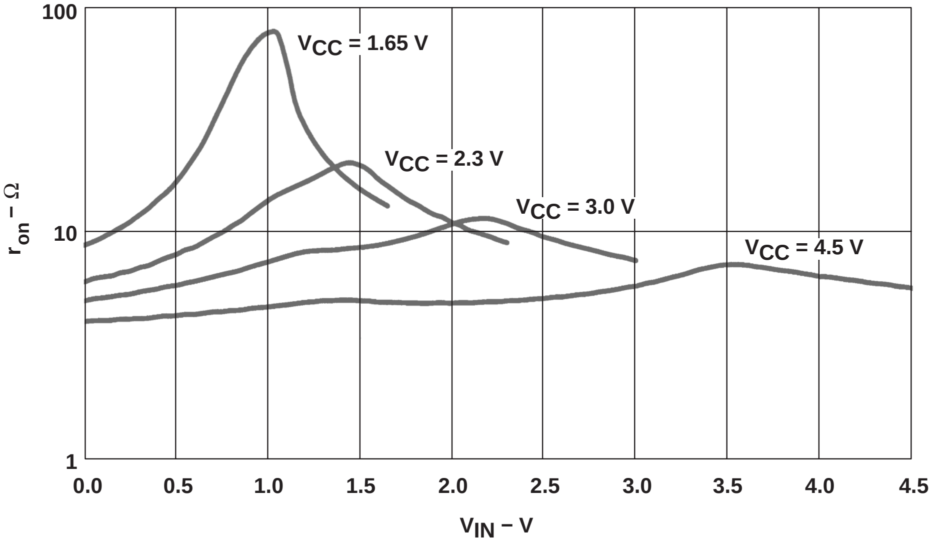


Figure 2. Typical r_{on} as a Function of Input Voltage (V_I) for V_I = 0 to V_{CC}

PARAMETER MEASUREMENT INFORMATION

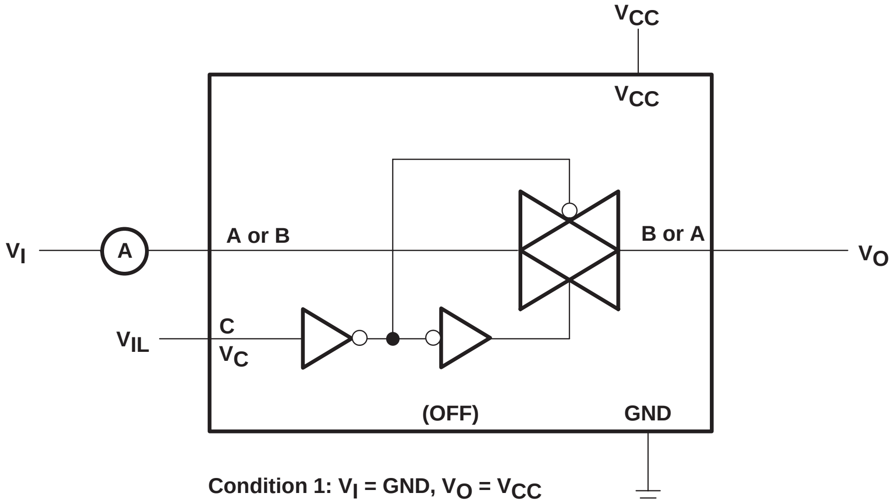

V_{CC}
V_{CC}
V_I
A
A or B
B or A
V_O
V_{IL}
C
V_C
(OFF)
GND
Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

Figure 3. Off-State Switch Leakage-Current Test Circuit

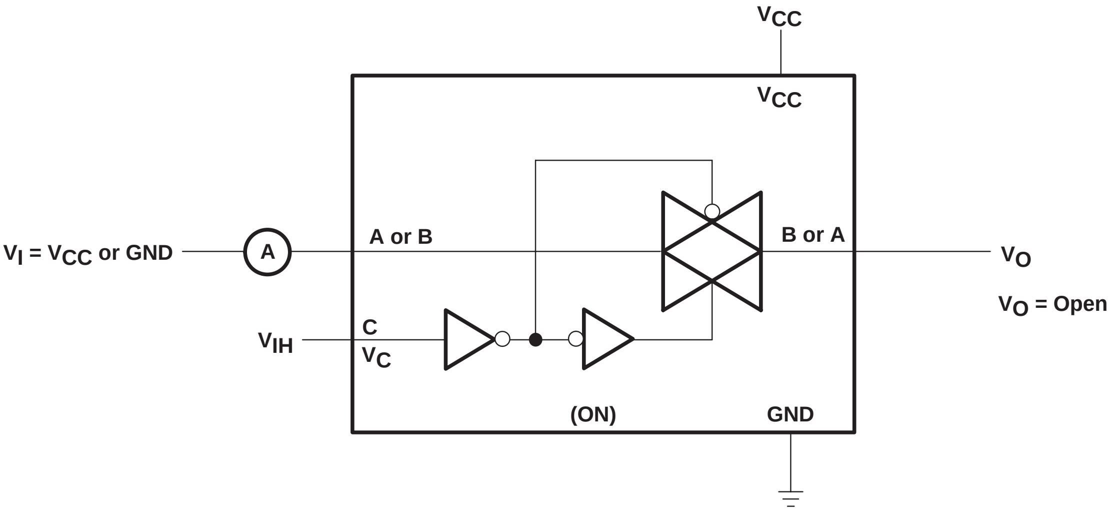
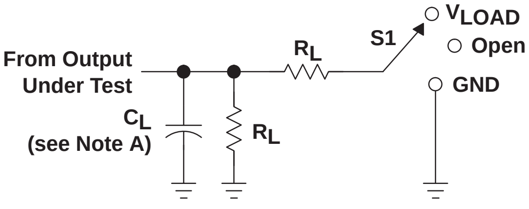

V_{CC}
V_{CC}
V_I = V_{CC} or GND
A
A or B
B or A
V_O
V_O = Open
V_{IH}
C
V_C
(ON)
GND

Figure 4. On-State Leakage-Current Test Circuit

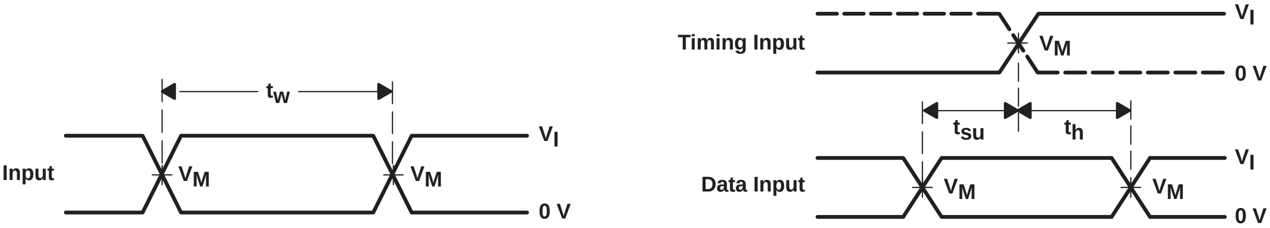
PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
C_L
(see Note A)
R_L
R_L
S1
V_{LOAD}
Open
GND

LOAD CIRCUIT

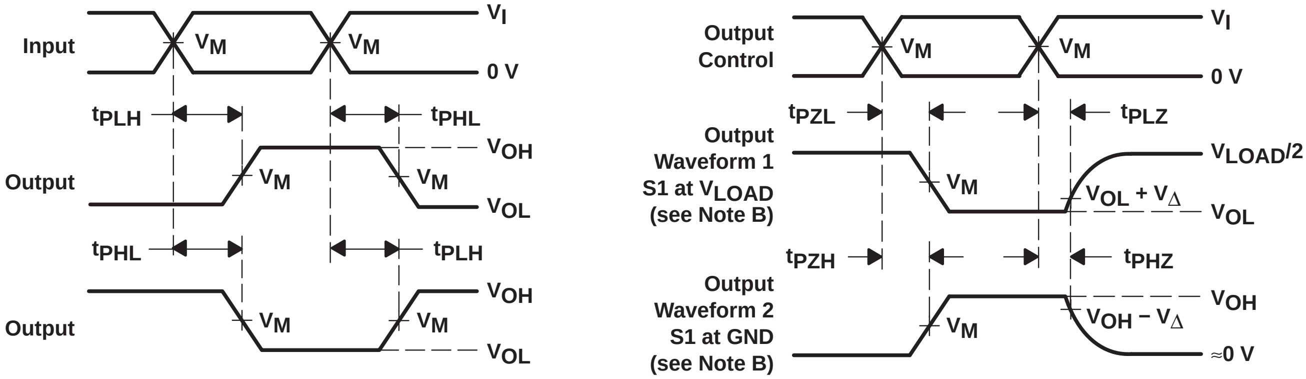
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V


t_w
Input
V_M
V_M
V_I
0 V
Timing Input
V_M
V_I
0 V
t_{su}
t_h
Data Input
V_M
V_M
V_I
0 V

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
V_M
V_M
V_I
0 V
t_{PLH}
t_{PHL}
Output
V_M
V_M
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
V_M
V_M
V_{OH}
V_{OL}
Output
Control
V_M
V_M
V_I
0 V
t_{PZL}
t_{PLZ}
Output
Waveform 1
S1 at V_{LOAD}
(see Note B)
V_M
$V_{OL} + V_\Delta$
$V_{LOAD}/2$
V_{OL}
t_{PZH}
t_{PHZ}
Output
Waveform 2
S1 at GND
(see Note B)
V_M
$V_{OH} - V_\Delta$
V_{OH}
≈0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

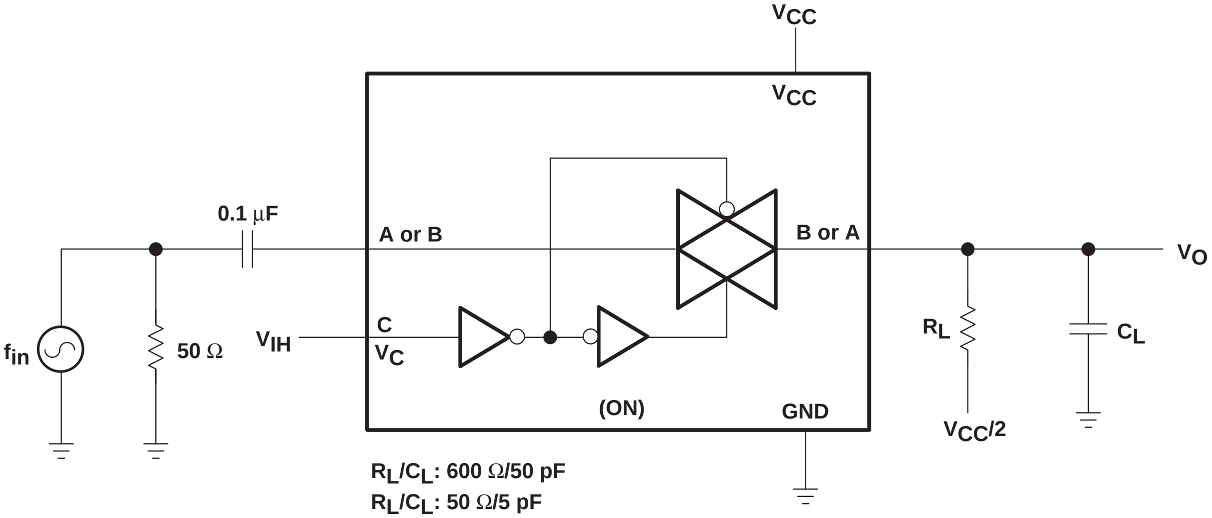

V_{CC}
V_{CC}
0.1 μF
A or B
B or A
V_O
f_{in}
50 Ω
V_{IH}
C
V_C
R_L
C_L
(ON)
GND
$V_{CC}/2$
R_L/C_L: 600 Ω/50 pF
R_L/C_L: 50 Ω/5 pF

Figure 6. Frequency Response (Switch ON)

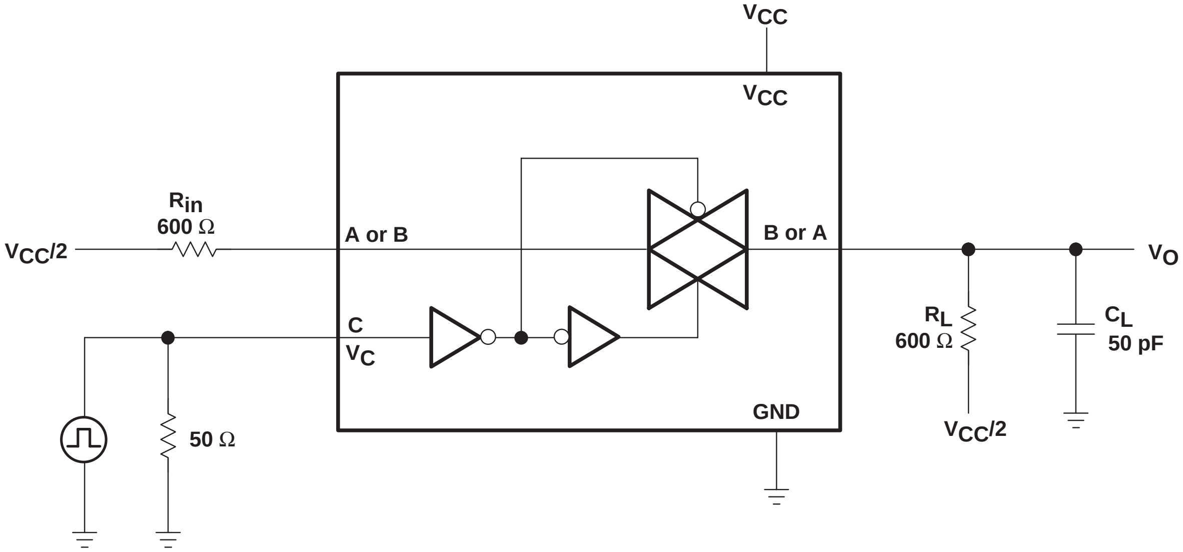

V_{CC}
V_{CC}
R_{in}
600 Ω
$V_{CC}/2$
A or B
B or A
V_O
C
V_C
R_L
600 Ω
C_L
50 pF
50 Ω
GND
$V_{CC}/2$

Figure 7. Crosstalk (Control Input − Switch Output)

PARAMETER MEASUREMENT INFORMATION

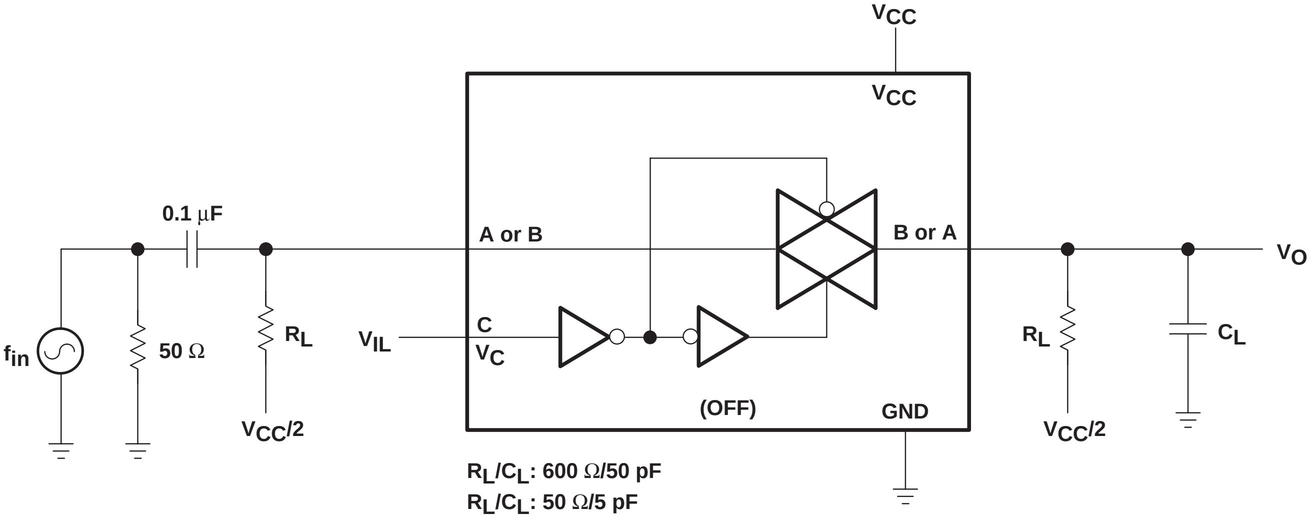

V_{CC}
V_{CC}
0.1 μF
A or B
B or A
V_O
f_{in}
50 Ω
R_L
V_{IL}
C
V_C
R_L
C_L
(OFF)
GND
$V_{CC}/2$
$V_{CC}/2$
R_L/C_L: 600 Ω/50 pF
R_L/C_L: 50 Ω/5 pF

Figure 8. Feed-Through (Switch OFF)

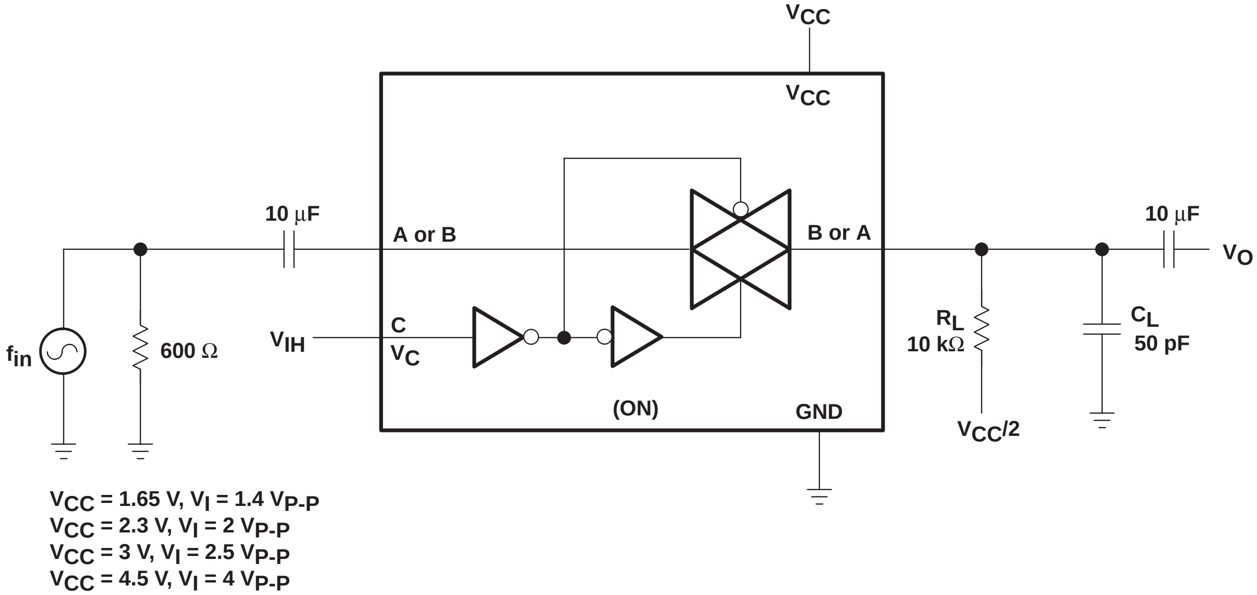

V_{CC}
V_{CC}
10 μF
A or B
B or A
10 μF
V_O
f_{in}
600 Ω
V_{IH}
C
V_C
R_L
10 kΩ
C_L
50 pF
(ON)
GND
$V_{CC}/2$
V_{CC} = 1.65 V, V_I = 1.4 $V_{P\text{-}P}$
V_{CC} = 2.3 V, V_I = 2 $V_{P\text{-}P}$
V_{CC} = 3 V, V_I = 2.5 $V_{P\text{-}P}$
V_{CC} = 4.5 V, V_I = 4 $V_{P\text{-}P}$

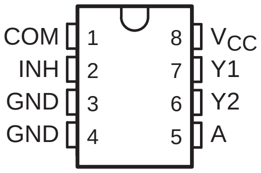
Figure 9. Sine-Wave Distortion

SN74LVC2G53
SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH OR 2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

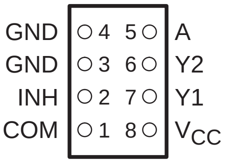
SCES324K − JULY 2001 − REVISED SEPTEMBER 2003

- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **1.65-V to 5.5-V V_{CC} Operation**
- **High On-Off Output Voltage Ratio**
- **High Degree of Linearity**
- **High Speed, Typically 0.5 ns (V_{CC} = 3 V, C_L = 50 pF)**
- **Low On-State Resistance, Typically ≈6.5 Ω (V_{CC} = 4.5 V)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DCT OR DCU PACKAGE
(TOP VIEW)



YEA, YEP, YZA, OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

This dual analog multiplexer/demultiplexer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G53 can handle both analog and digital signals. The device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[‡]
−40°C to 85°C	NanoStar™ − WCSP (DSBGA) 0.17-mm Small Bump − YEA	Reel of 3000	SN74LVC2G53YEAR	_ _ _C4_
	NanoFree™ − WCSP (DSBGA) 0.17-mm Small Bump − YZA (Pb-free)		SN74LVC2G53YZAR	
	NanoStar™ − WCSP (DSBGA) 0.23-mm Large Bump − YEP		SN74LVC2G53YEPR	
	NanoFree™ − WCSP (DSBGA) 0.23-mm Large Bump − YZP (Pb-free)		SN74LVC2G53YZPR	
	SSOP − DCT	Reel of 3000	SN74LVC2G53DCTR	C53_ _ _
	VSSOP − DCU	Reel of 3000	SN74LVC2G53DCUR	C53_
		Reel of 250	SN74LVC2G53DCUT	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

[‡] DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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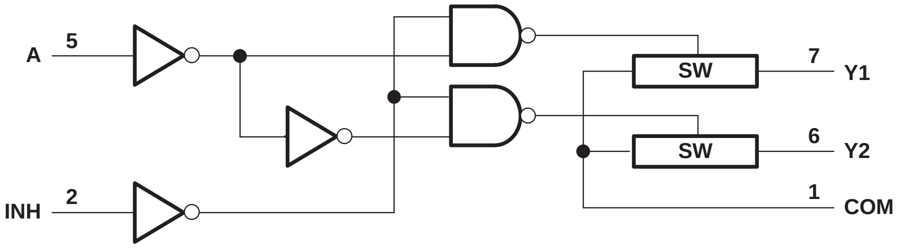
TEXAS INSTRUMENTS

FUNCTION TABLE

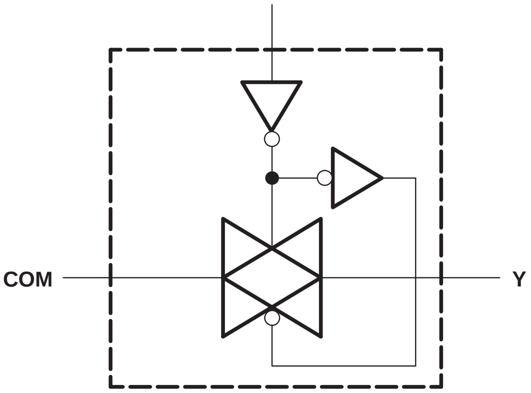
CONTROL INPUTS		ON CHANNEL
INH	A	
L	L	Y1
L	H	Y2
H	X	None

logic diagram (positive logic)



NOTE A: For simplicity, the test conditions shown in Figures 1 through 4 and 6 through 10 are for the demultiplexer configuration. Signals can be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

simplified schematic, each switch (SW)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.5 V to 6.5 V
Input voltage range, V_I (see Notes 1 and 2)	−0.5 V to 6.5 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	−0.5 V to V_{CC} + 0.5 V
Control input clamp current, I_{IK} ($V_I < 0$)	−50 mA
I/O port diode current, I_{IOK} ($V_{I/O} < 0$ or $V_{I/O} > V_{CC}$)	±50 mA
On-state switch current, I_T ($V_{I/O}$ = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 4): DCT package	220°C/W
DCU package	227°C/W
YEA/YZA package	140°C/W
YEP/YZP package	102°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 5.5 V maximum.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 5)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V	$V_{CC} \times 0.65$		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V		$V_{CC} \times 0.35$	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$	
V_I	Control input voltage		0	5.5	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 1.65 V to 1.95 V		20	ns/V
		V_{CC} = 2.3 V to 2.7 V		20	
		V_{CC} = 3 V to 3.6 V		10	
		V_{CC} = 4.5 V to 5.5 V		10	
T_A	Operating free-air temperature		−40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
r_{on}	On-state switch resistance		$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ (see Figures 1 and 2)	I_S = 4 mA	1.65 V		13	30	Ω
				I_S = 8 mA	2.3 V		10	20	
				I_S = 24 mA	3 V		8.5	17	
				I_S = 32 mA	4.5 V		6.5	13	
$r_{on(p)}$	Peak on-state resistance		$V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$ (see Figures 1 and 2)	I_S = 4 mA	1.65 V		86.5	120	Ω
				I_S = 8 mA	2.3 V		23	30	
				I_S = 24 mA	3 V		13	20	
				I_S = 32 mA	4.5 V		8	15	
Δr_{on}	Difference of on-state resistance between switches		$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figures 1 and 2)	I_S = 4 mA	1.65 V			7	Ω
				I_S = 8 mA	2.3 V			5	
				I_S = 24 mA	3 V			3	
				I_S = 32 mA	4.5 V			2	
$I_{S(off)}$	Off-state switch leakage current		$V_I = V_{CC}$ and V_O = GND or V_I = GND and $V_O = V_{CC}$, $V_{INH} = V_{IH}$ (see Figure 3)		5.5 V			±1	µA
								±0.1†	
$I_{S(on)}$	On-state switch leakage current		$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$, V_O = Open (see Figure 4)		5.5 V			±1	µA
								±0.1†	
I_I	Control input current		$V_C = V_{CC}$ or GND		5.5 V			±1	µA
								±0.1†	µA
I_{CC}	Supply current		$V_C = V_{CC}$ or GND		5.5 V			1	µA
ΔI_{CC}	Supply-current change		$V_C = V_{CC} - 0.6$ V		5.5 V			500	µA
C_{ic}	Control input capacitance				5 V		3.5		pF
$C_{io(off)}$	Switch input/output capacitance	Y			5 V		6.5		pF
		COM					10		
$C_{io(on)}$	Switch input/output capacitance				5 V		19.5		pF

† T_A = 25°C

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}‡	COM or Y	Y or COM		2		1.2		0.8		0.6	ns
t_{en}§	INH	COM or Y	3.3	9	2.5	6.1	2.2	5.4	1.8	4.5	ns
t_{dis}¶			3.2	10.9	2.3	8.3	2.3	8.1	1.6	8	
t_{en}§	A	COM or Y	2.9	10.3	2.1	7.2	1.9	5.8	1.3	5.4	ns
t_{dis}¶			2.1	9.4	1.4	7.9	1.1	7.2	1	5	

‡ t_{PLH} and t_{PHL} are the same as t_{pd}. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

§ t_{PZL} and t_{PZH} are the same as t_{en}.

¶ t_{PLZ} and t_{PHZ} are the same as t_{dis}.

analog switch characteristics, T_A = 25°C

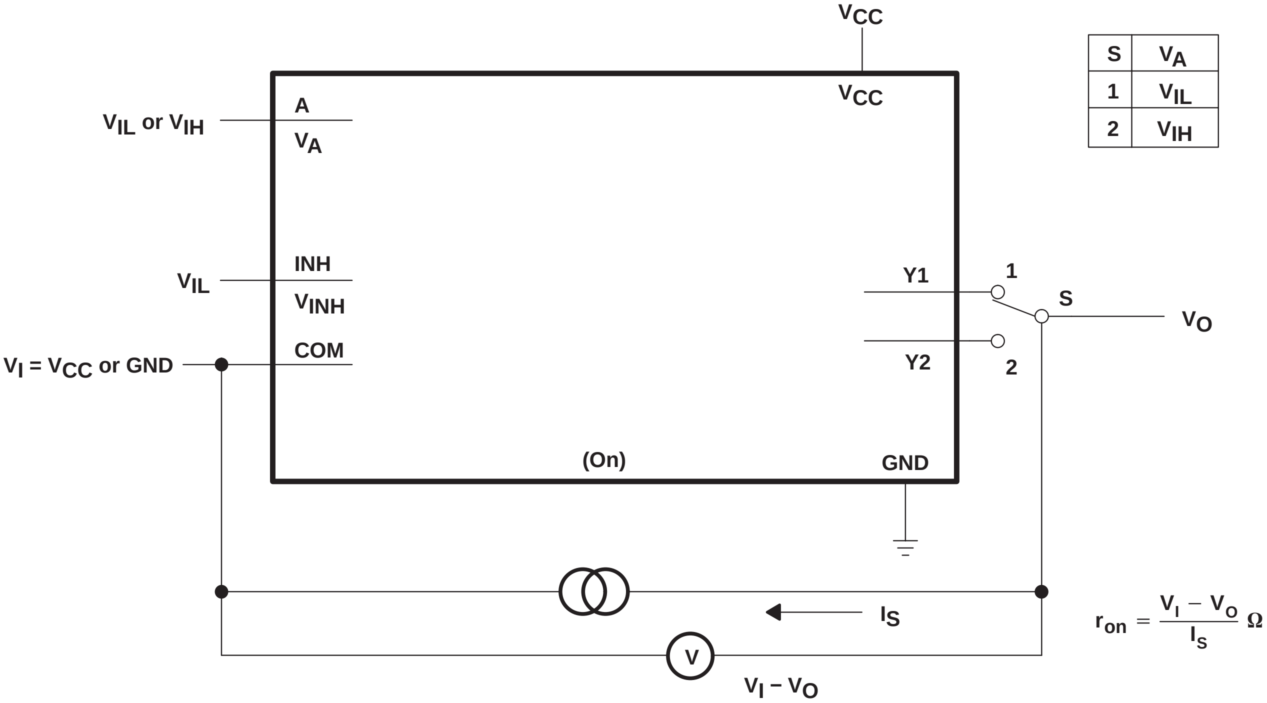
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response† (switch on)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	35	MHz
				2.3 V	120	
				3 V	190	
				4.5 V	215	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	>300	
				2.3 V	>300	
				3 V	>300	
				4.5 V	>300	
Crosstalk‡ (between switches)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	1.65 V	−58	dB
				2.3 V	−58	
				3 V	−58	
				4.5 V	−58	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	1.65 V	−42	
				2.3 V	−42	
				3 V	−42	
				4.5 V	−42	
Crosstalk (control input to signal output)	INH	COM or Y	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)	1.65 V	35	mV
				2.3 V	50	
				3 V	70	
				4.5 V	100	
Feed-through attenuation‡ (switch off)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	1.65 V	−60	dB
				2.3 V	−60	
				3 V	−60	
				4.5 V	−60	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	1.65 V	−50	
				2.3 V	−50	
				3 V	−50	
				4.5 V	−50	
Sine-wave distortion	COM or Y	Y or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	1.65 V	0.1	%
				2.3 V	0.025	
				3 V	0.015	
				4.5 V	0.01	
			C_L = 50 pF, R_L = 10 kΩ, f_{in} = 10 kHz (sine wave) (see Figure 10)	1.65 V	0.15	
				2.3 V	0.025	
				3 V	0.015	
				4.5 V	0.01	

† Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads −3 dB.
‡ Adjust f_{in} voltage to obtain 0 dBm at input.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	9	10	10	12	pF

PARAMETER MEASUREMENT INFORMATION


V_{CC}
V_{CC}
V_{IL} or V_{IH}
A
V_A
V_{IL}
INH
V_{INH}
$V_I = V_{CC}$ or GND
COM
Y1
Y2
1
2
S
V_O
(On)
GND
I_S
V
$V_I - V_O$
$r_{on} = \frac{V_I - V_O}{I_S}\ \Omega$

S	V_A
1	V_{IL}
2	V_{IH}

Figure 1. On-State Resistance Test Circuit

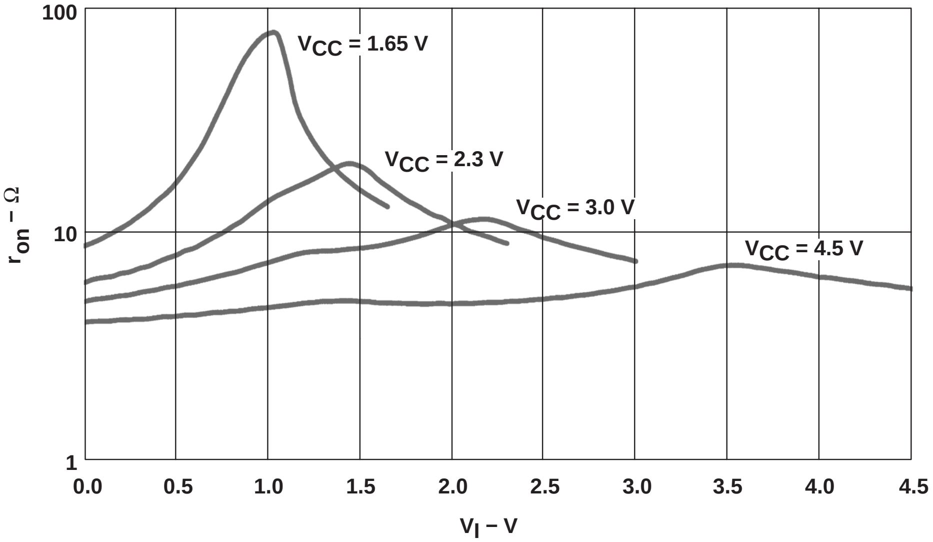
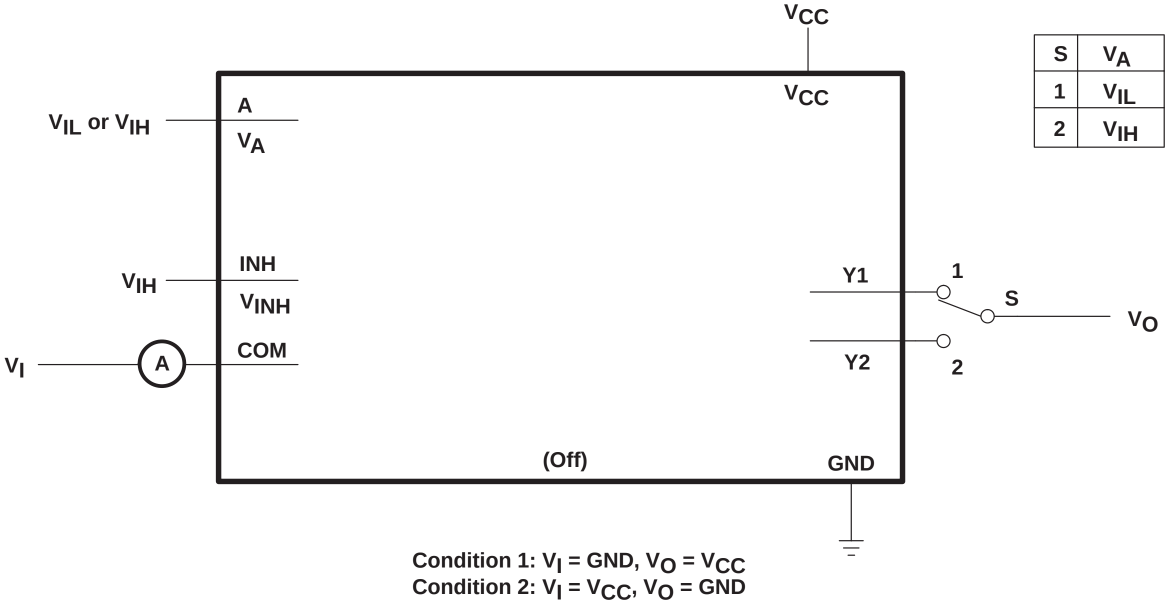


Figure 2. Typical r_{on} as a Function of Input Voltage (V_I) for $V_I = 0$ to V_{CC}

PARAMETER MEASUREMENT INFORMATION


V_{CC}
V_{CC}
V_{IL} or V_{IH}
A
V_A
V_{IH}
INH
V_{INH}
V_I
A
COM
Y1
Y2
1
2
S
V_O
(Off)
GND
S | V_A
1 | V_{IL}
2 | V_{IH}

Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

Figure 3. Off-State Switch Leakage-Current Test Circuit

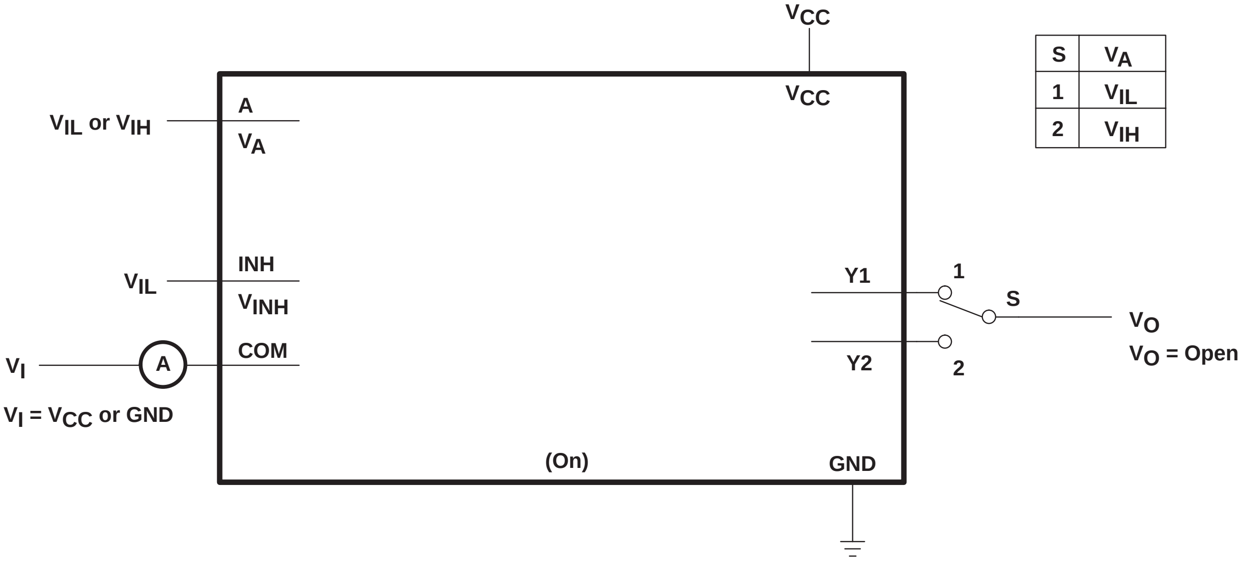
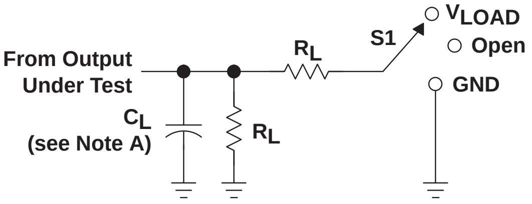

V_{CC}
V_{CC}
V_{IL} or V_{IH}
A
V_A
V_{IL}
INH
V_{INH}
V_I
A
COM
V_I = V_{CC} or GND
Y1
Y2
1
2
S
V_O
V_O = Open
(On)
GND
S | V_A
1 | V_{IL}
2 | V_{IH}

Figure 4. On-State Switch Leakage-Current Test Circuit

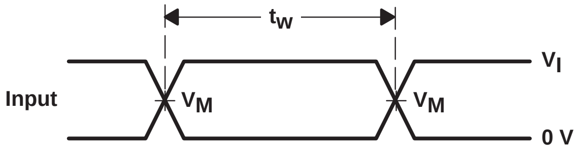
PARAMETER MEASUREMENT INFORMATION


From Output Under Test
C_L (see Note A)
R_L
R_L
S1
V_{LOAD}
Open
GND

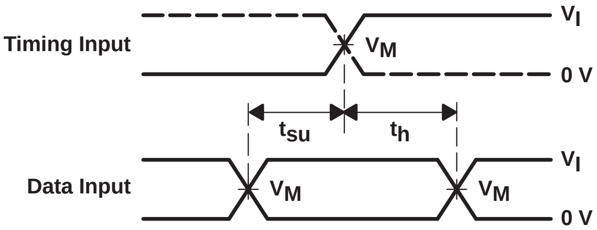
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

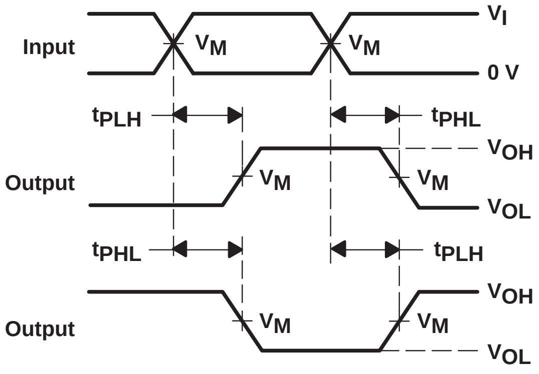
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V


t_w
Input
V_M
V_M
V_I
0 V

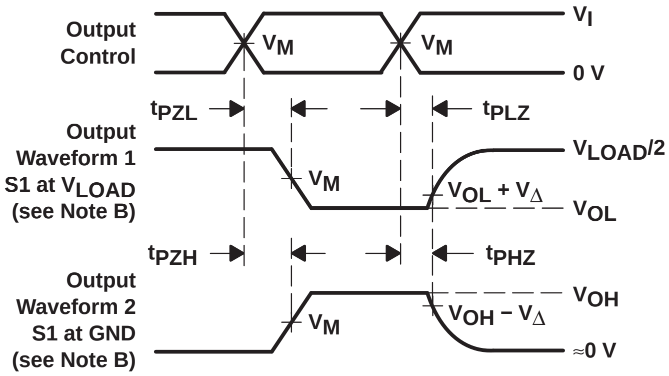
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
V_I
V_M
0 V
t_{su}
t_h
Data Input
V_I
V_M
V_M
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
V_M
V_M
V_I
0 V
t_{PLH}
t_{PHL}
Output
V_M
V_M
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Output
V_M
V_M
V_{OH}
V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

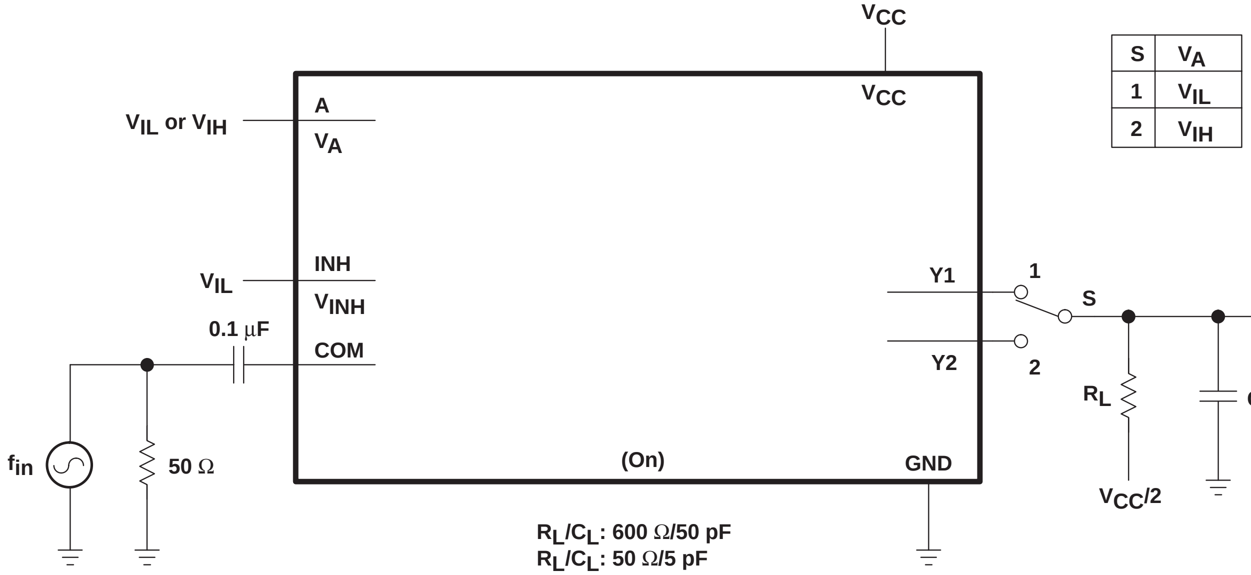

Output Control
V_M
V_M
V_I
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at V_{LOAD} (see Note B)
V_M
$V_{LOAD}/2$
$V_{OL} + V_\Delta$
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
V_M
V_{OH}
$V_{OH} - V_\Delta$
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION


V_{CC}
S | V_A
1 | V_{IL}
2 | V_{IH}
V_{IL} or V_{IH}
A
V_A
V_{CC}
V_{IL}
INH
V_{INH}
0.1 µF
COM
Y1
Y2
1
S
2
V_O
R_L
C_L
f_{in}
50 Ω
(On)
GND
$V_{CC}/2$

R_L/C_L: 600 Ω/50 pF
R_L/C_L: 50 Ω/5 pF

Figure 6. Frequency Response (Switch On)

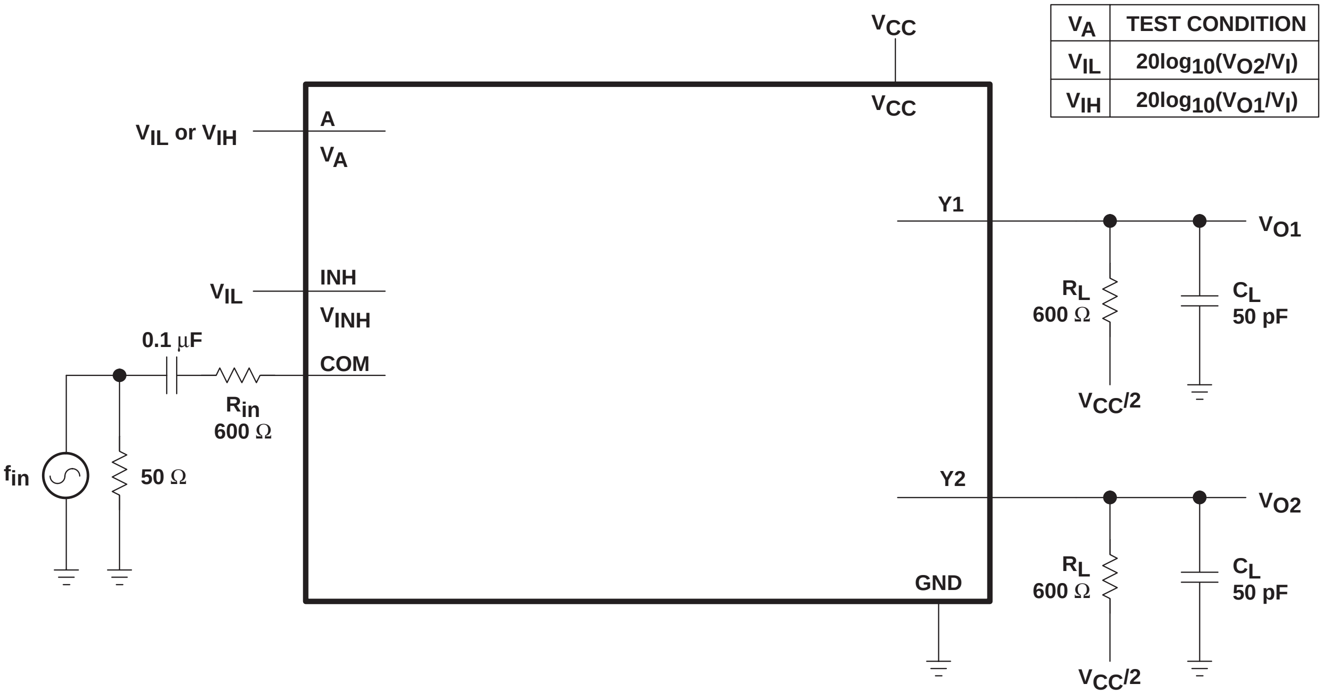
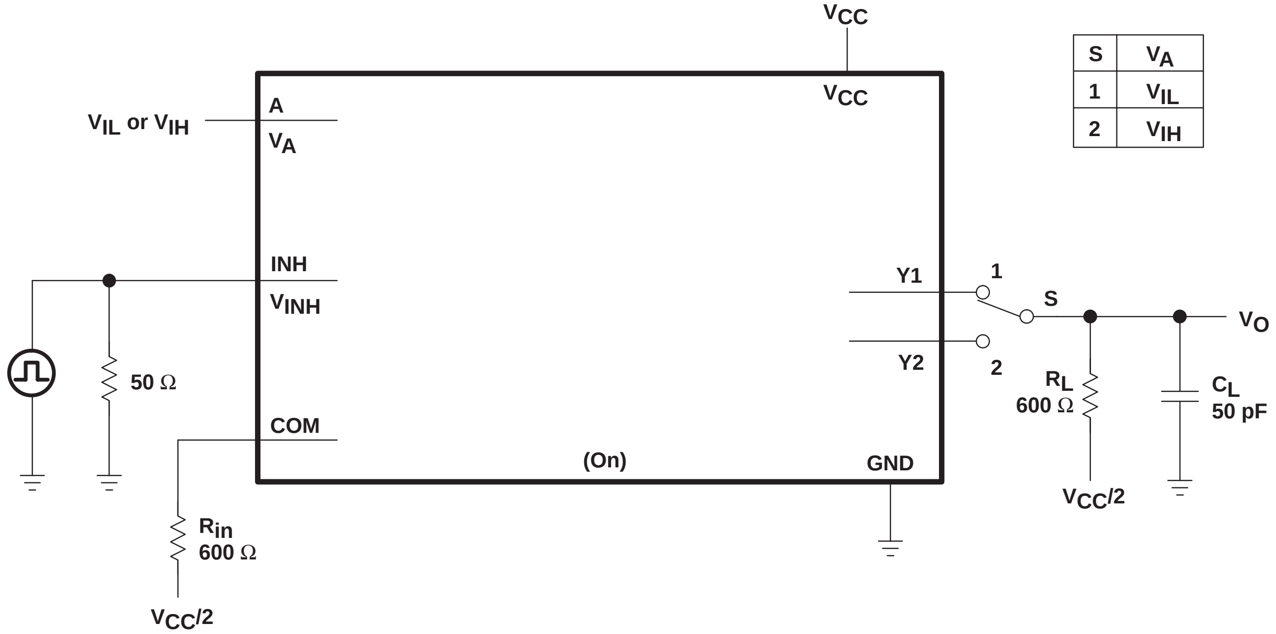

V_{CC}
V_A | TEST CONDITION
V_{IL} | $20\log_{10}(V_{O2}/V_I)$
V_{IH} | $20\log_{10}(V_{O1}/V_I)$
V_{IL} or V_{IH}
A
V_A
V_{CC}
Y1
V_{O1}
V_{IL}
INH
V_{INH}
0.1 µF
COM
R_{in}
600 Ω
f_{in}
50 Ω
R_L
600 Ω
C_L
50 pF
$V_{CC}/2$
Y2
V_{O2}
R_L
600 Ω
C_L
50 pF
GND
$V_{CC}/2$

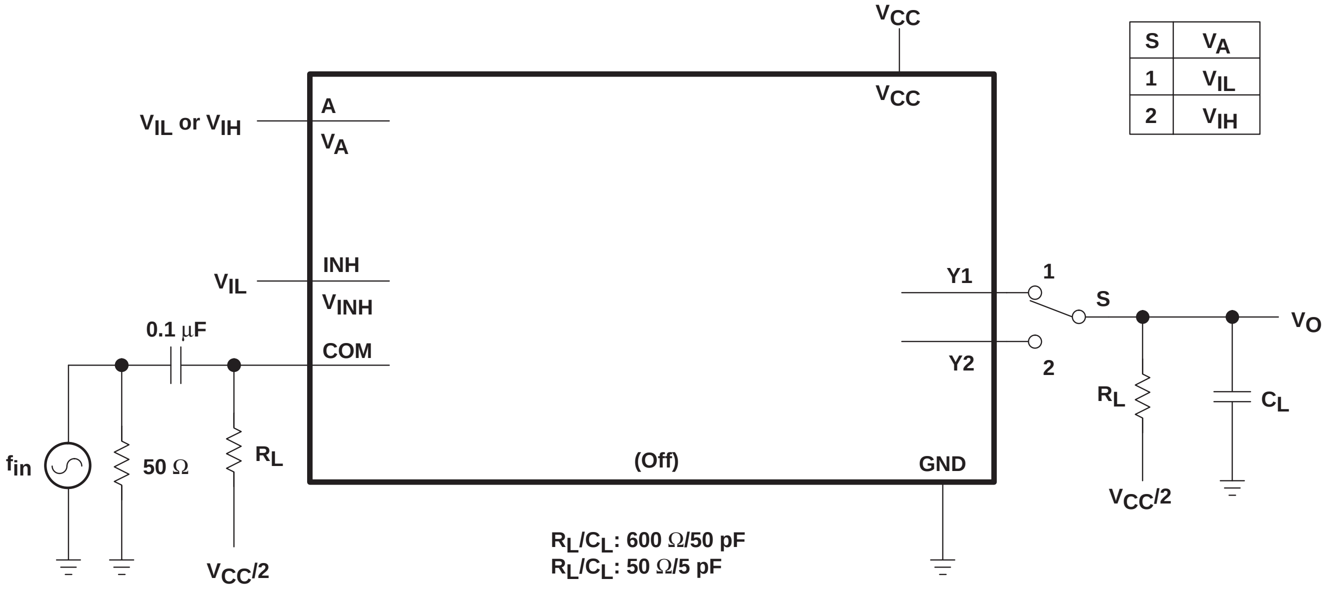
Figure 7. Crosstalk (Between Switches)

PARAMETER MEASUREMENT INFORMATION


V_{CC}
V_{CC}
V_{IL} or V_{IH}
A
V_A
INH
V_{INH}
50 Ω
COM
R_{in}
600 Ω
$V_{CC}/2$
(On)
GND
Y1
Y2
1
2
S
V_O
R_L
600 Ω
$V_{CC}/2$
C_L
50 pF

S	V_A
1	V_{IL}
2	V_{IH}

Figure 8. Crosstalk (Control Input, Switch Output)

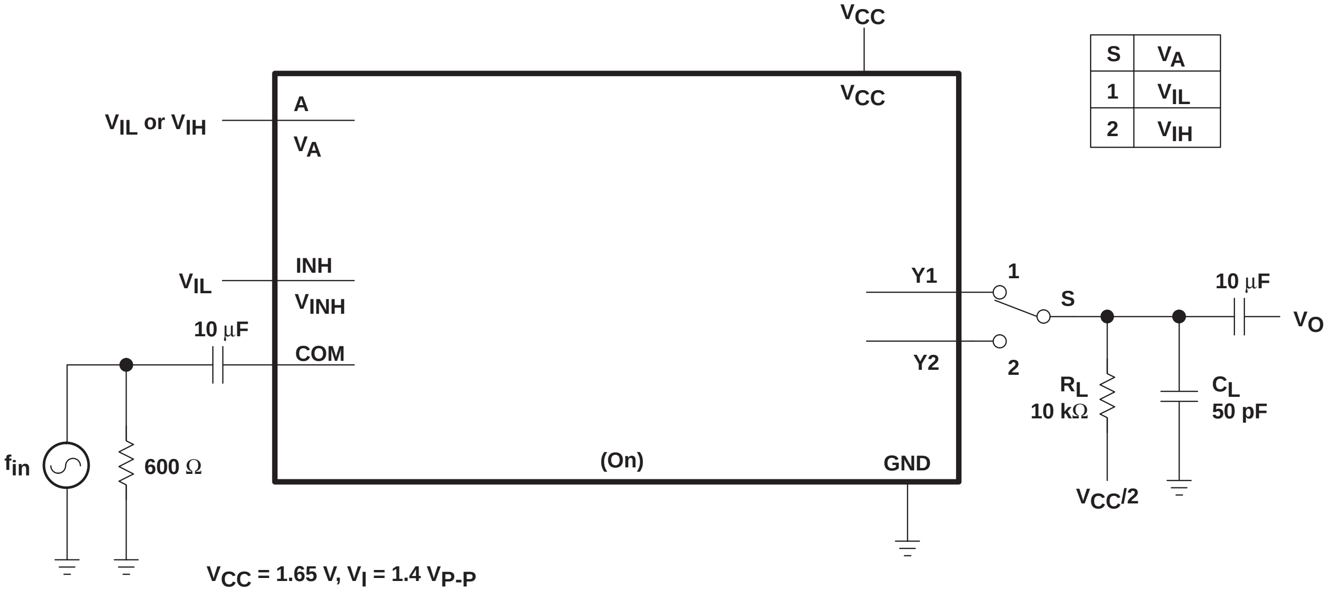

V_{CC}
V_{CC}
V_{IL} or V_{IH}
A
V_A
V_{IL}
INH
V_{INH}
0.1 µF
COM
f_{in}
50 Ω
R_L
$V_{CC}/2$
(Off)
GND
Y1
Y2
1
2
S
V_O
R_L
C_L
$V_{CC}/2$

S	V_A
1	V_{IL}
2	V_{IH}

R_L/C_L: 600 Ω/50 pF
R_L/C_L: 50 Ω/5 pF

Figure 9. Feed Through (Switch Off)

PARAMETER MEASUREMENT INFORMATION


V_{CC}
V_{CC}
A
V_A
V_{IL} or V_{IH}
INH
V_{INH}
V_{IL}
10 µF
COM
f_{in}
600 Ω
(On)
GND
Y1
Y2
1
2
S
R_L
10 kΩ
$V_{CC}/2$
C_L
50 pF
10 µF
V_O

S	V_A
1	V_{IL}
2	V_{IH}

V_{CC} = 1.65 V, V_I = 1.4 $V_{P\text{-}P}$
V_{CC} = 2.30 V, V_I = 2.0 $V_{P\text{-}P}$
V_{CC} = 3.00 V, V_I = 2.5 $V_{P\text{-}P}$
V_{CC} = 4.50 V, V_I = 4.0 $V_{P\text{-}P}$

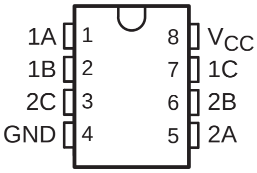
Figure 10. Sine-Wave Distortion

SN74LVC2G66
DUAL BILATERAL ANALOG SWITCH

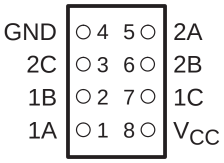
SCES325G − JULY 2001 − REVISED SEPTEMBER 2003

- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **1.65-V to 5.5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 0.8 ns at 3.3 V**
- **High On-Off Output Voltage Ratio**
- **High Degree of Linearity**
- **High Speed, Typically 0.5 ns (V_{CC} = 3 V, C_L = 50 pF)**
- **Rail-to-Rail Input/Output**
- **Low On-State Resistance, Typically ≈6 Ω (V_{CC} = 4.5 V)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DCT OR DCU PACKAGE
(TOP VIEW)



YEA, YEP, YZA, OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

This dual bilateral analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G66 can handle both analog and digital signals. The device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	NanoStar™ − WCSP (DSBGA) 0.17-mm Small Bump − YEA	Reel of 3000	SN74LVC2G66YEAR	_ _ _C6_
	NanoFree™ − WCSP (DSBGA) 0.17-mm Small Bump − YZA (Pb-free)		SN74LVC2G66YZAR	
	NanoStar™ − WCSP (DSBGA) 0.23-mm Large Bump − YEP		SN74LVC2G66YEPR	
	NanoFree™ − WCSP (DSBGA) 0.23-mm Large Bump − YZP (Pb-free)		SN74LVC2G66YZPR	
	SSOP − DCT	Reel of 3000	SN74LVC2G66DCTR	C66_ _ _
	VSSOP − DCU	Reel of 3000	SN74LVC2G66DCUR	C66_
		Reel of 250	SN74LVC2G66DCUT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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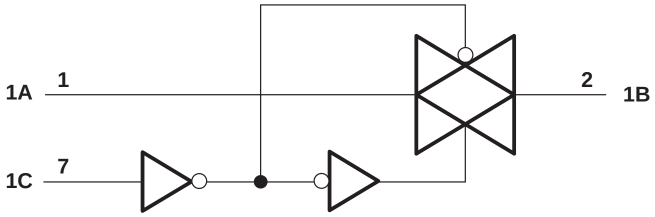
description/ordering information (continued)

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

FUNCTION TABLE
(each section)

CONTROL INPUT (C)	SWITCH
L	Off
H	On

logic diagram, each switch (positive logic)



One of Two Switches

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)		−0.5 V to 6.5 V
Input voltage range, V_I (see Notes 1 and 2)		−0.5 V to 6.5 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)		−0.5 V to V_{CC} + 0.5 V
Control input clamp current, I_{IK} ($V_I < 0$)		−50 mA
I/O port diode current, I_{IOK} ($V_{I/O} < 0$ or $V_{I/O} > V_{CC}$)		±50 mA
On-state switch current, I_T ($V_{I/O} = 0$ to V_{CC})		±50 mA
Continuous current through V_{CC} or GND		±100 mA
Package thermal impedance, θ_{JA} (see Note 4):	DCT package	220°C/W
	DCU package	227°C/W
	YEA/YZA package	140°C/W
	YEP/YZP package	102°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 5.5 V maximum.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 5)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V	$V_{CC} \times 0.65$		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V		$V_{CC} \times 0.35$	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$	
V_I	Control input voltage		0	5.5	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 1.65 V to 1.95 V		20	ns/V
		V_{CC} = 2.3 V to 2.7 V		20	
		V_{CC} = 3 V to 3.6 V		10	
		V_{CC} = 4.5 V to 5.5 V		10	
T_A	Operating free-air temperature		−40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
r_{on}	On-state switch resistance	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see Figures 1 and 2)	I_S = 4 mA	1.65 V		12.5	30	Ω
			I_S = 8 mA	2.3 V		9	20	
			I_S = 24 mA	3 V		7.5	15	
			I_S = 32 mA	4.5 V		6	10	
$r_{on(p)}$	Peak on-state resistance	$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figures 1 and 2)	I_S = 4 mA	1.65 V		85	120	Ω
			I_S = 8 mA	2.3 V		22	30	
			I_S = 24 mA	3 V		12	20	
			I_S = 32 mA	4.5 V		7.5	15	
Δr_{on}	Difference of on-state resistance between switches	$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figures 1 and 2)	I_S = 4 mA	1.65 V			7	Ω
			I_S = 8 mA	2.3 V			5	
			I_S = 24 mA	3 V			3	
			I_S = 32 mA	4.5 V			2	
$I_{S(off)}$	Off-state switch leakage current	$V_I = V_{CC}$ and V_O = GND or V_I = GND and $V_O = V_{CC}$, $V_C = V_{IL}$ (see Figure 3)		5.5 V			±1	μA
							±0.1†	
$I_{S(on)}$	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$, V_O = Open (see Figure 4)		5.5 V			±1	μA
							±0.1†	
I_I	Control input current	$V_C = V_{CC}$ or GND		5.5 V			±1	μA
							±0.1†	
I_{CC}	Supply current	$V_C = V_{CC}$ or GND		5.5 V			10	μA
							1†	
ΔI_{CC}	Supply-current change	$V_C = V_{CC} - 0.6$ V		5.5 V			500	μA
C_{ic}	Control input capacitance			5 V		3.5		pF
$C_{io(off)}$	Switch input/output capacitance			5 V		6		pF
$C_{io(on)}$	Switch input/output capacitance			5 V		14		pF

† T_A = 25°C

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}‡	A or B	B or A		2		1.2		0.8		0.6	ns
t_{en}§	C	A or B	2.3	10	1.6	5.6	1.5	4.4	1.3	3.9	ns
t_{dis}¶	C	A or B	2.5	10.5	1.2	6.9	2	7.2	1.1	6.3	ns

‡ t_{PLH} and t_{PHL} are the same as t_{pd}. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

§ t_{PZL} and t_{PZH} are the same as t_{en}.

¶ t_{PLZ} and t_{PHZ} are the same as t_{dis}.

analog switch characteristics, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response[†] (switch on)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	35	MHz
				2.3 V	120	
				3 V	175	
				4.5 V	195	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	>300	
				2.3 V	>300	
				3 V	>300	
				4.5 V	>300	
Crosstalk[‡] (between switches)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	1.65 V	−58	dB
				2.3 V	−58	
				3 V	−58	
				4.5 V	−58	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	1.65 V	−42	
				2.3 V	−42	
				3 V	−42	
				4.5 V	−42	
Crosstalk (control input to signal output)	C	A or B	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)	1.65 V	35	mV
				2.3 V	50	
				3 V	70	
				4.5 V	100	
Feed-through attenuation[‡] (switch off)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	1.65 V	−58	dB
				2.3 V	−58	
				3 V	−58	
				4.5 V	−58	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	1.65 V	−42	
				2.3 V	−42	
				3 V	−42	
				4.5 V	−42	
Sine-wave distortion	A or B	B or A	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	1.65 V	0.1	%
				2.3 V	0.025	
				3 V	0.015	
				4.5 V	0.01	
			C_L = 50 pF, R_L = 10 kΩ, f_{in} = 10 kHz (sine wave) (see Figure 10)	1.65 V	0.15	
				2.3 V	0.025	
				3 V	0.015	
				4.5 V	0.01	

[†] Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads −3 dB.
[‡] Adjust f_{in} voltage to obtain 0 dBm at input.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	8	9	9.5	11	pF

PARAMETER MEASUREMENT INFORMATION

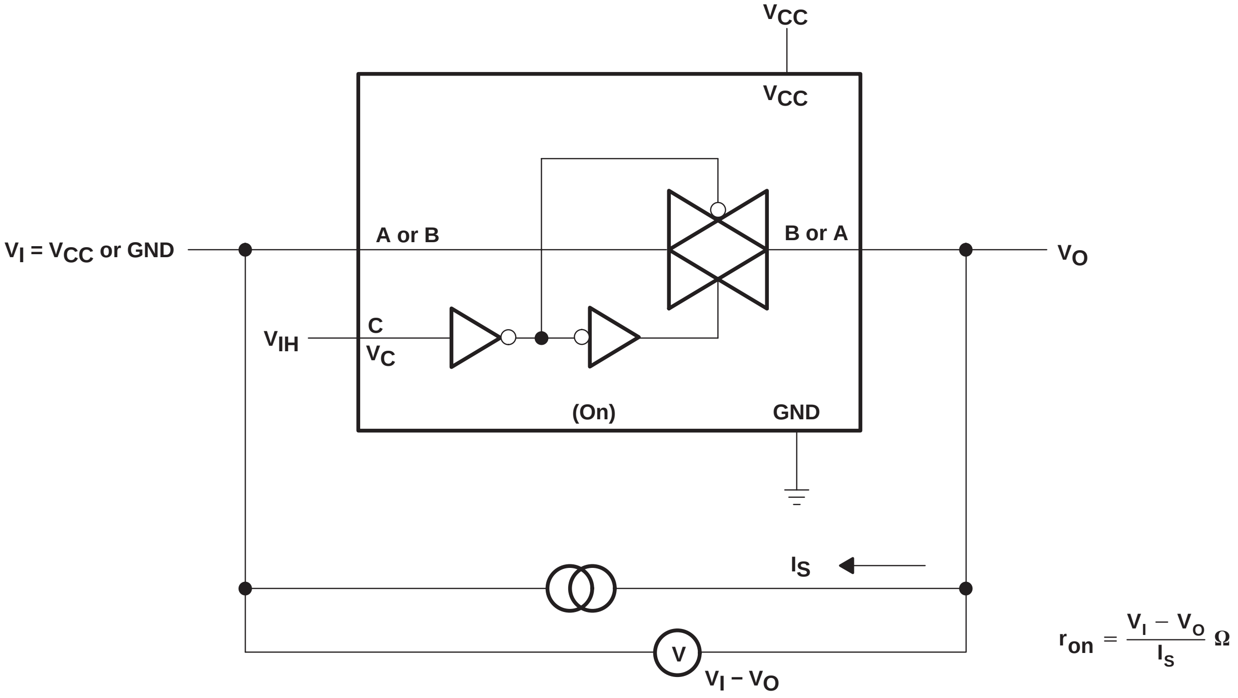

V_{CC}
V_{CC}
$V_I = V_{CC}$ or GND
A or B
B or A
V_O
V_{IH}
C
V_C
(On)
GND
I_S
V
$V_I - V_O$
$r_{on} = \frac{V_I - V_O}{I_S}\ \Omega$

Figure 1. On-State Resistance Test Circuit

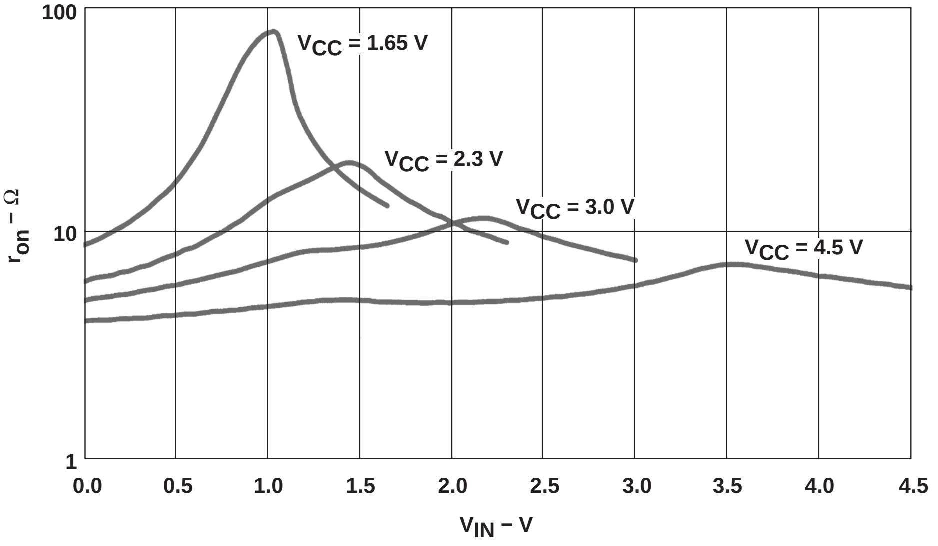
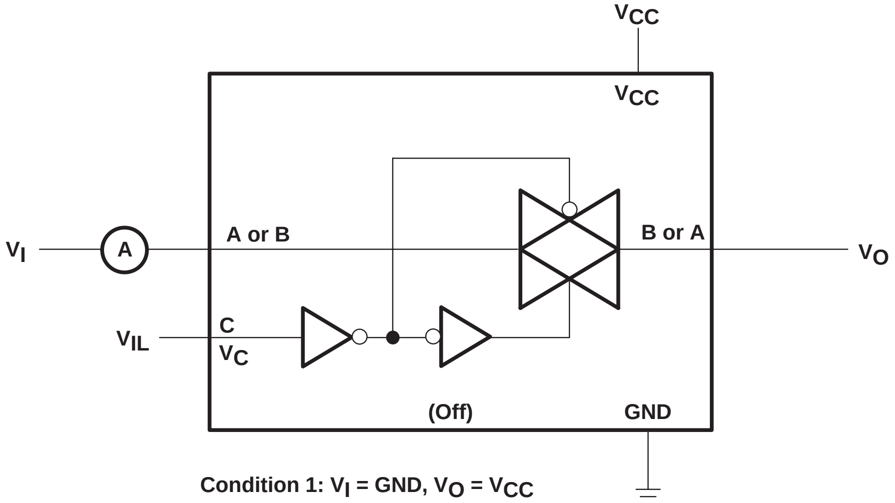


Figure 2. Typical r_{on} as a Function of Input Voltage (V_I) for $V_I = 0$ to V_{CC}

PARAMETER MEASUREMENT INFORMATION


V_{CC}
V_{CC}
V_I
A
A or B
B or A
V_O
V_{IL}
C
V_C
(Off)
GND

Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

Figure 3. Off-State Switch Leakage-Current Test Circuit

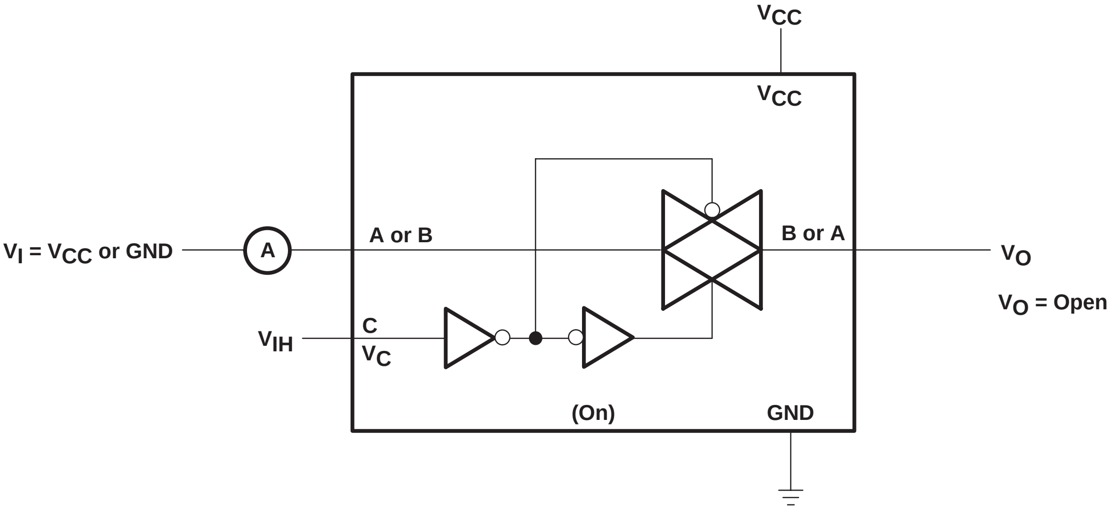
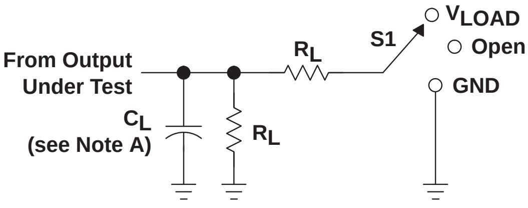

V_{CC}
V_{CC}
$V_I = V_{CC}$ or GND
A
A or B
B or A
V_O
V_O = Open
V_{IH}
C
V_C
(On)
GND

Figure 4. On-State Leakage-Current Test Circuit

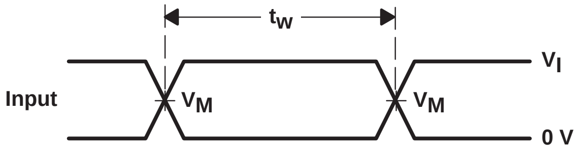
PARAMETER MEASUREMENT INFORMATION


From Output
Under Test
CL
(see Note A)
RL
RL
S1
VLOAD
Open
GND

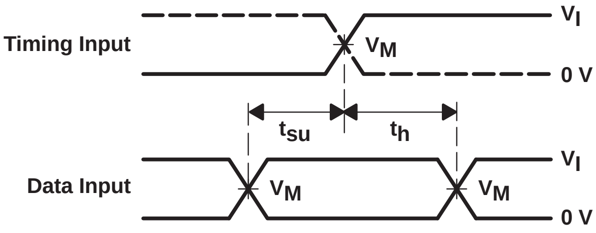
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

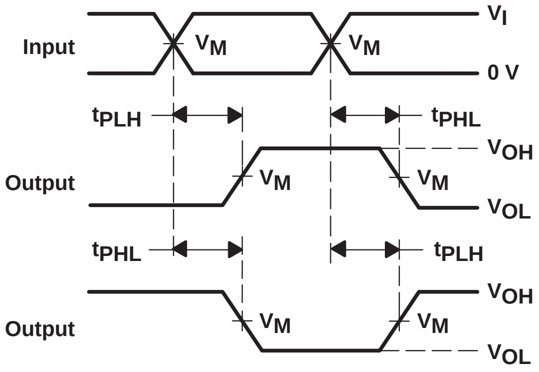
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V


tw
Input
VM
VM
VI
0 V

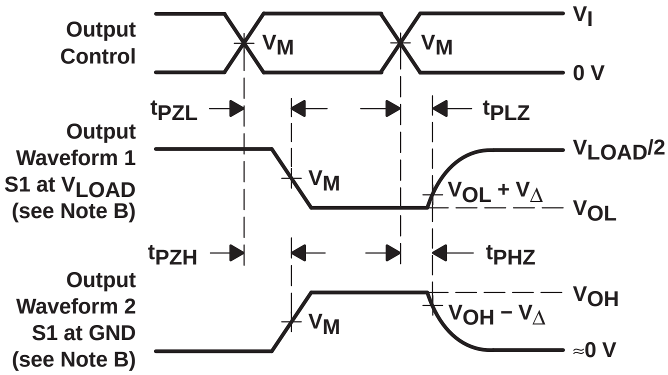
VOLTAGE WAVEFORMS
PULSE DURATION


Timing Input
VI
VM
0 V
tsu
th
Data Input
VI
VM
VM
0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


Input
VM
VM
VI
0 V
tPLH
tPHL
Output
VM
VM
VOH
VOL
tPHL
tPLH
Output
VM
VM
VOH
VOL

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS


Output
Control
VM
VM
VI
0 V
tPZL
tPLZ
Output
Waveform 1
S1 at VLOAD
(see Note B)
VM
VLOAD/2
VOL + VΔ
VOL
tPZH
tPHZ
Output
Waveform 2
S1 at GND
(see Note B)
VM
VOH
VOH − VΔ
≈0 V

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

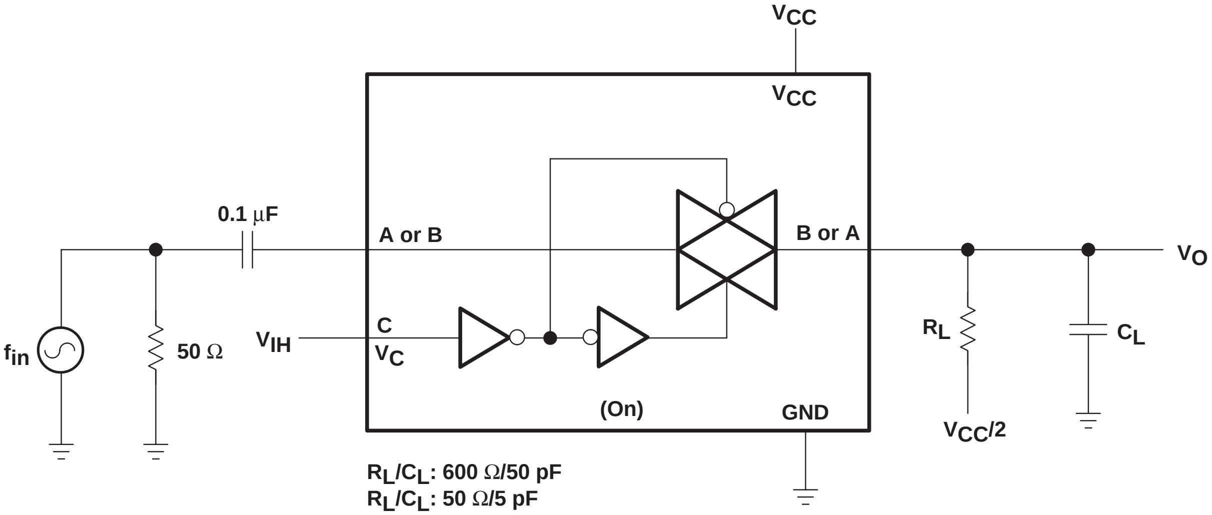

V_{CC}
V_{CC}
0.1 µF
A or B
B or A
V_O
f_{in}
50 Ω
V_{IH}
C
V_C
R_L
C_L
(On)
GND
$V_{CC}/2$
R_L/C_L: 600 Ω/50 pF
R_L/C_L: 50 Ω/5 pF

Figure 6. Frequency Response (Switch On)

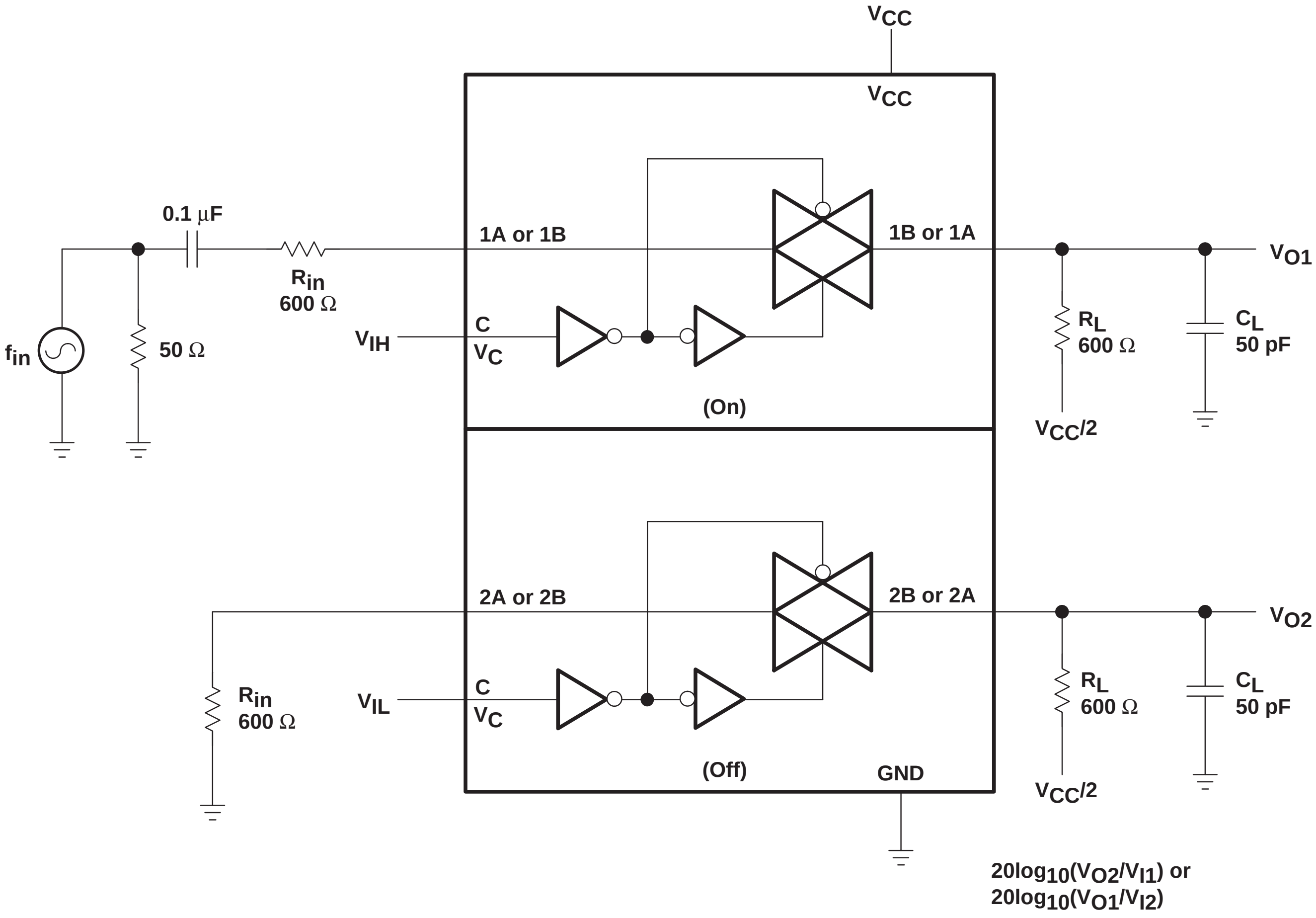

V_{CC}
V_{CC}
0.1 µF
R_{in}
600 Ω
1A or 1B
1B or 1A
V_{O1}
f_{in}
50 Ω
V_{IH}
C
V_C
R_L
600 Ω
C_L
50 pF
(On)
$V_{CC}/2$
2A or 2B
2B or 2A
V_{O2}
R_{in}
600 Ω
V_{IL}
C
V_C
R_L
600 Ω
C_L
50 pF
(Off)
GND
$V_{CC}/2$
$20\log_{10}(V_{O2}/V_{I1})$ or
$20\log_{10}(V_{O1}/V_{I2})$

Figure 7. Crosstalk (Between Switches)

PARAMETER MEASUREMENT INFORMATION

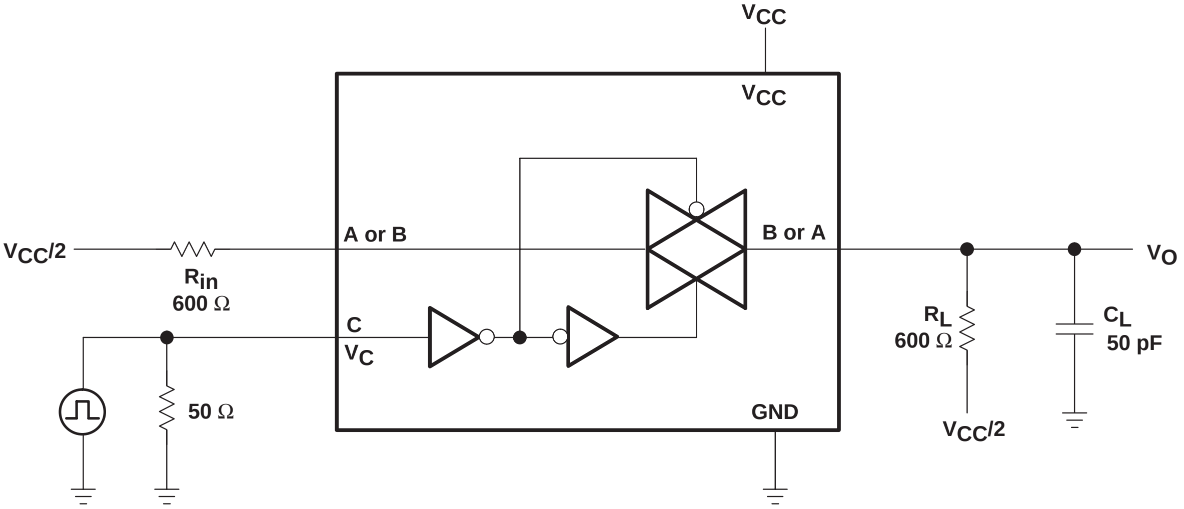

VCC
VCC
A or B
B or A
VCC/2
Rin
600 Ω
C
VC
50 Ω
GND
RL
600 Ω
CL
50 pF
VCC/2
VO

Figure 8. Crosstalk (Control Input, Switch Output)

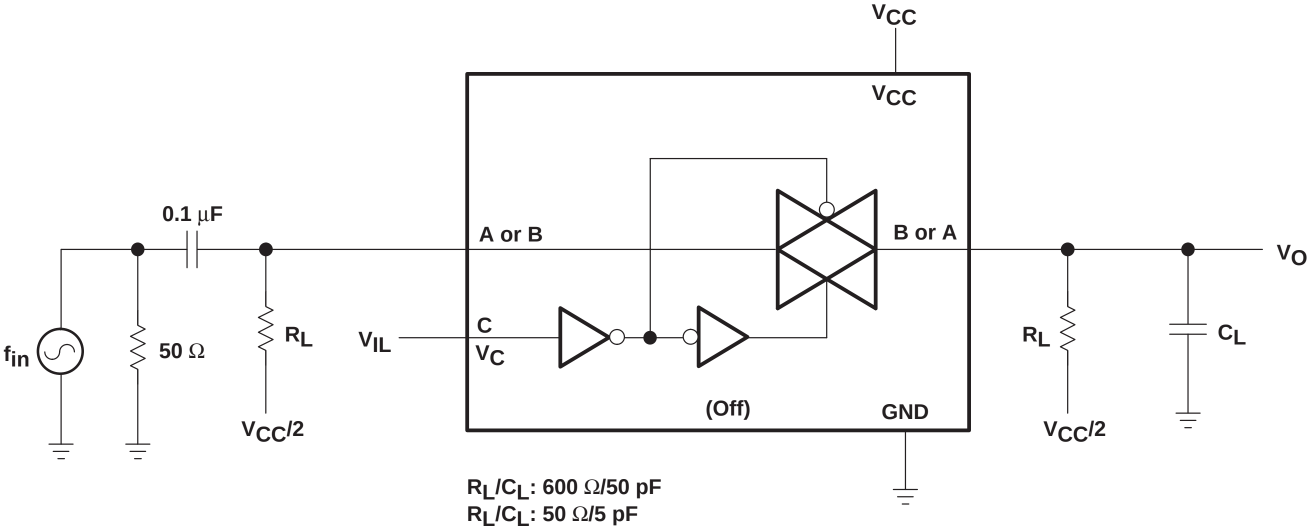
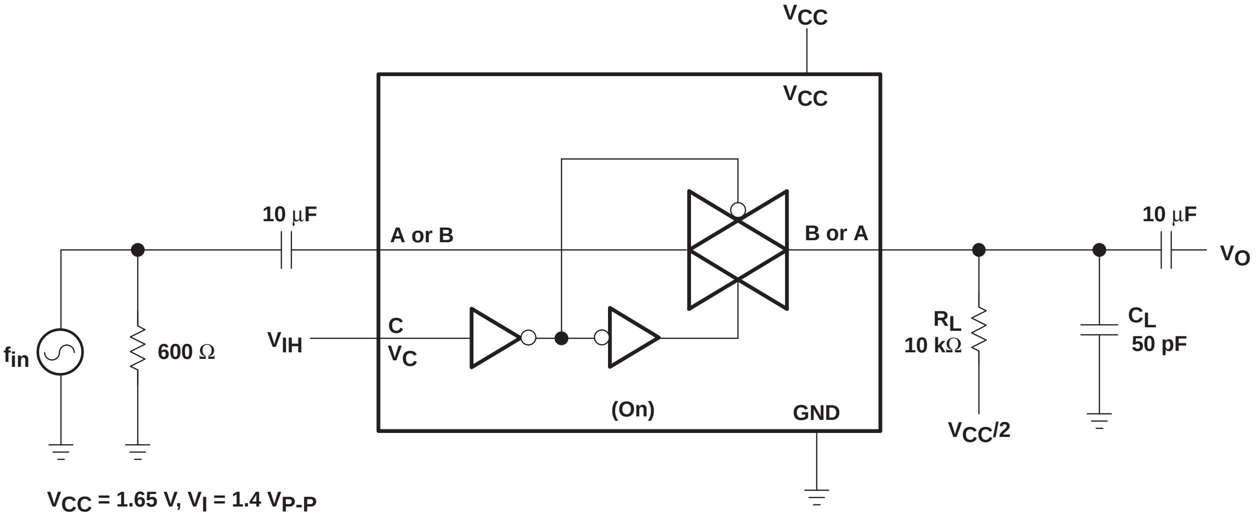

VCC
VCC
0.1 µF
A or B
B or A
VO
fin
50 Ω
RL
VCC/2
VIL
C
VC
(Off)
GND
RL
VCC/2
CL
RL/CL: 600 Ω/50 pF
RL/CL: 50 Ω/5 pF

Figure 9. Feed Through (Switch Off)

PARAMETER MEASUREMENT INFORMATION


VCC
VCC
10 μF
A or B
B or A
10 μF
VO
fin
600 Ω
VIH
C
VC
RL
10 kΩ
CL
50 pF
(On)
GND
VCC/2

V_{CC} = 1.65 V, V_I = 1.4 V_{P-P}
V_{CC} = 2.3 V, V_I = 2 V_{P-P}
V_{CC} = 3 V, V_I = 2.5 V_{P-P}
V_{CC} = 4.5 V, V_I = 4 V_{P-P}

Figure 10. Sine-Wave Distortion

Insert Tab Here

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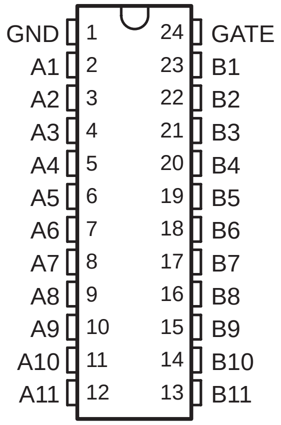
SN74TVC3010
10-BIT VOLTAGE CLAMP

- **Designed to be Used in Voltage-Limiting Applications**
- **6.5-Ω On-State Connection Between Ports A and B**
- **Flow-Through Pinout for Ease of Printed Circuit Board Trace Routing**
- **Direct Interface With GTL+ Levels**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **1000-V Charged-Device Model (C101)**

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74TVC3010 provides 11 parallel NMOS pass transistors with a common gate. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device can be used as a 10-bit switch with the gates cascaded together to a reference transistor. The low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. This is done to protect components with inputs that are sensitive to high-state voltage-level overshoots. (See Application Information in this data sheet.)

All of the transistors in the TVC array have the same electrical characteristics; therefore, any one of them can be used as the reference transistor. Since, within the device, the characteristics from transistor to transistor are equal, the maximum output high-state voltage (V_{OH}) is approximately the reference voltage (V_{REF}), with minimal deviation from one output to another. This is a large benefit of the TVC solution over discrete devices. Because the fabrication of the transistors is symmetrical, either port connection of each bit can be used as the low-voltage side, and the I/O signals are bidirectional through each FET.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Tube	SN74TVC3010DW	TVC3010
		Tape and reel	SN74TVC3010DWR	
	SSOP (QSOP) − DBQ	Tape and reel	SN74TVC3010DBQR	TVC3010
	TSSOP − PW	Tape and reel	SN74TVC3010PWR	TT010
	TVSOP − DGV	Tape and reel	SN74TVC3010DGVR	TT010

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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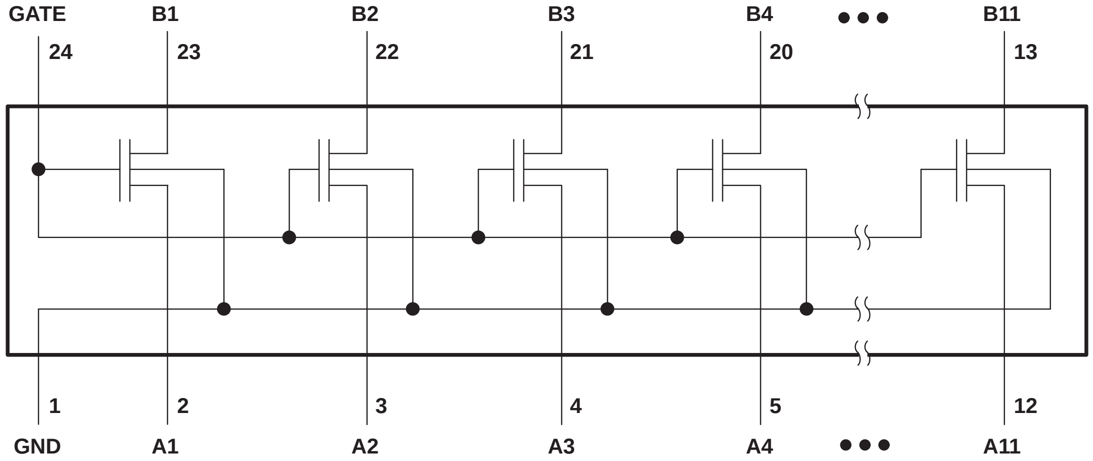
simplified schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Input/output voltage range, $V_{I/O}$ (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	TYP	MAX	UNIT
$V_{I/O}$	Input/output voltage	0		5	V
V_{GATE}	GATE voltage	0		5	V
I_{PASS}	Pass-transistor current		20	64	mA
T_A	Operating free-air temperature	−40		85	°C

application operating conditions (see Figure 3)

		MIN	TYP	MAX	UNIT
V_{BIAS}	BIAS voltage	V_{REF} + 0.6	2.1	5	V
V_{GATE}	GATE voltage	V_{REF} + 0.6	2.1	5	V
V_{REF}	Reference voltage	0	1.5	4.4	V
V_{DPU}	Drain pullup voltage	2.36	2.5	2.64	V
I_{PASS}	Pass-transistor current		14		mA
I_{REF}	Reference-transistor current		5		µA
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	V_{BIAS} = 0,	I_I = −18 mA				−1.2	V
V_{OL}	I_{REF} = 5 µA, V_{DPU} = 2.625 V,	V_{REF} = 1.365 V, R_{DPU} = 150 Ω	V_S = 0.175 V, See Figure 1			350	mV
$C_{i(GATE)}$	V_I = 3 V or 0				24		pF
$C_{io(off)}$	V_O = 3 V or 0				4	12	pF
$C_{io(on)}$	V_O = 3 V or 0				12	30	pF
r_{on}[‡]	I_{REF} = 5 µA, V_{DPU} = 2.625 V,	V_{REF} = 1.365 V, R_{DPU} = 150 Ω	V_S = 0.175 V, See Figure 1			12.5	Ω

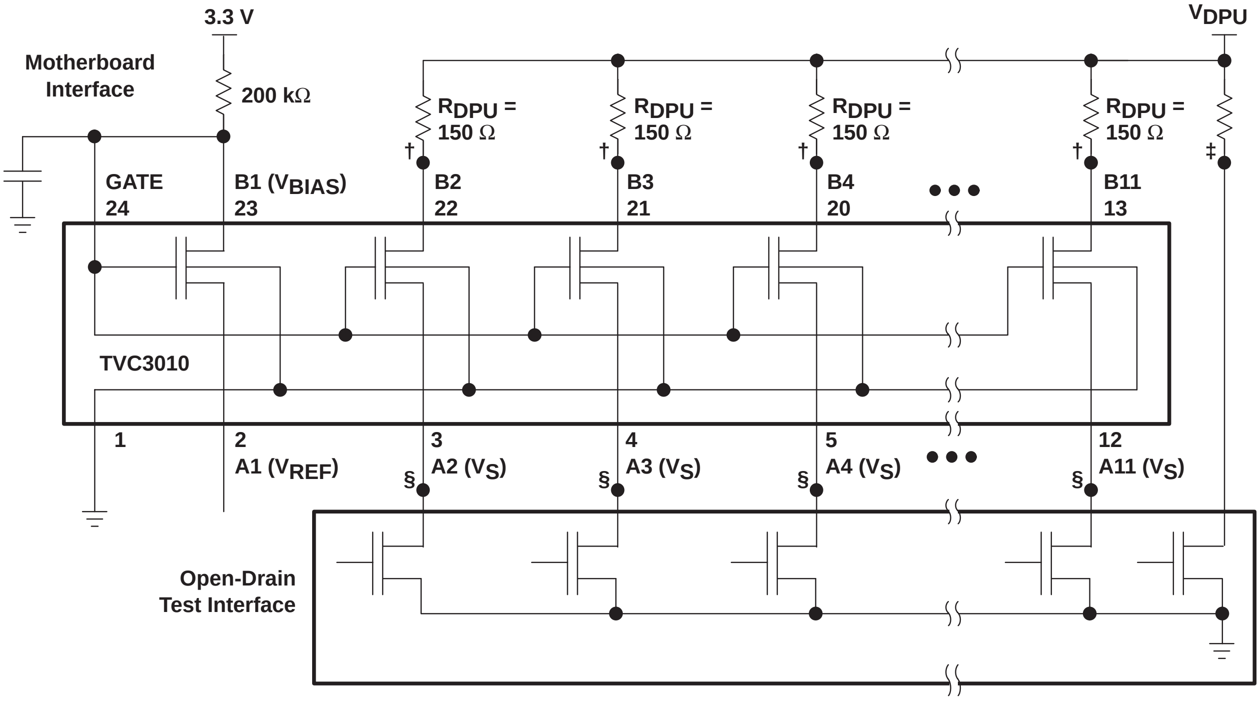
[†] All typical values are at T_A = 25°C.

[‡] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, V_{DPU} = 2.36 V to 2.64 V (unless otherwise noted) (see Figure 1)

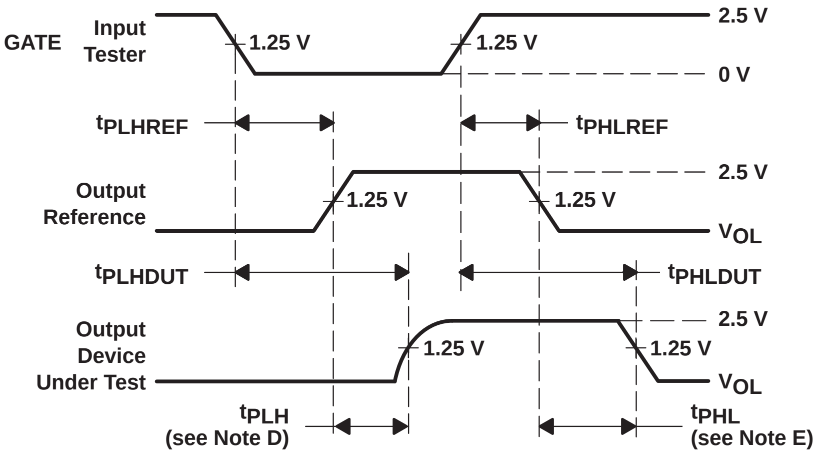
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	A or B	B or A	0	4	ns
t_{PHL}			0	4	

PARAMETER MEASUREMENT INFORMATION


3.3 V
V_{DPU}
Motherboard Interface
200 kΩ
R_{DPU} = 150 Ω
†
‡
GATE 24
B1 (V_{BIAS}) 23
B2 22
B3 21
B4 20
B11 13
TVC3010
1
2 A1 (V_{REF})
3 A2 (V_S)
4 A3 (V_S)
5 A4 (V_S)
12 A11 (V_S)
§
Open-Drain Test Interface

TESTER CALIBRATION SETUP (see Note C)

DEFINITION	SYMBOL
Output tested	†
Output reference	‡
Input tested	§


GATE
Input Tester
1.25 V
1.25 V
2.5 V
0 V
t_{PLHREF}
t_{PHLREF}
Output Reference
1.25 V
1.25 V
2.5 V
V_{OL}
t_{PLHDUT}
t_{PHLDUT}
Output Device Under Test
1.25 V
1.25 V
2.5 V
V_{OL}
t_{PLH} (see Note D)
t_{PHL} (see Note E)

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES:
- A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le 2$ ns, $t_f \le 2$ ns.
- B. The outputs are measured one at a time with one transition per measurement.
- C. Test procedure: t_{PLHREF} and t_{PHLREF} are obtained by measuring the propagation delay of a reference measuring point. t_{PLHDUT} and t_{PHLDUT} are obtained by measuring the propagation delay of the device under test.
- D. $t_{PLH} = t_{PLHDUT} - t_{PLHREF}$
- E. $t_{PHL} = t_{PHLDUT} - t_{PHLREF}$

Figure 1. Tester Calibration Setup and Voltage Waveforms

APPLICATION INFORMATION

TVC background information

In personal computer (PC) architecture, there are industry-accepted bus standards. These standards define, among other things, the I/O voltage levels at which the bus communicates. Examples include the GTL+ host bus, the AGP graphics port, and the PCI local bus. In new designs, the system components must communicate with existing bus infrastructure. Providing an evolutionary upgrade path is important in the design of PC architecture, but the existing bus standards must be preserved.

To achieve the ever-present need for smaller, faster, lighter devices that draw less power, yet have faster performance, most new high-performance digital integrated circuits are being designed and produced with advanced submicron semiconductor process technologies. These devices have thin gate-oxide or short channel lengths and very low absolute-maximum voltages that can be tolerated at the inputs/outputs (I/Os) without causing damage. In many cases, the I/Os of these devices are not tolerant of the high-state voltage levels on the preexisting buses with which they must communicate. Therefore, it became necessary to protect the I/Os of devices by limiting the I/O voltages.

The Texas Instruments (TI) translation voltage-clamp (TVC) family was designed specifically for protecting sensitive I/Os (see Figure 2). The information in this data sheet describes the I/O-protection application of the TVC family and should enable the design engineer to successfully implement an I/O-protection circuit utilizing the TI TVC solution.

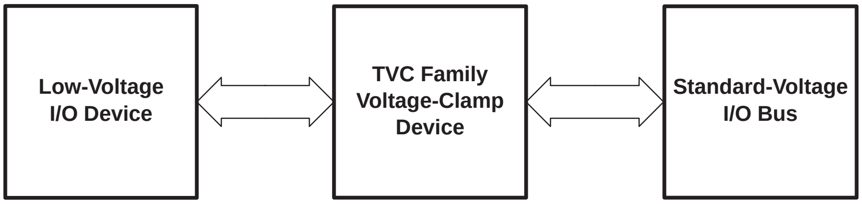
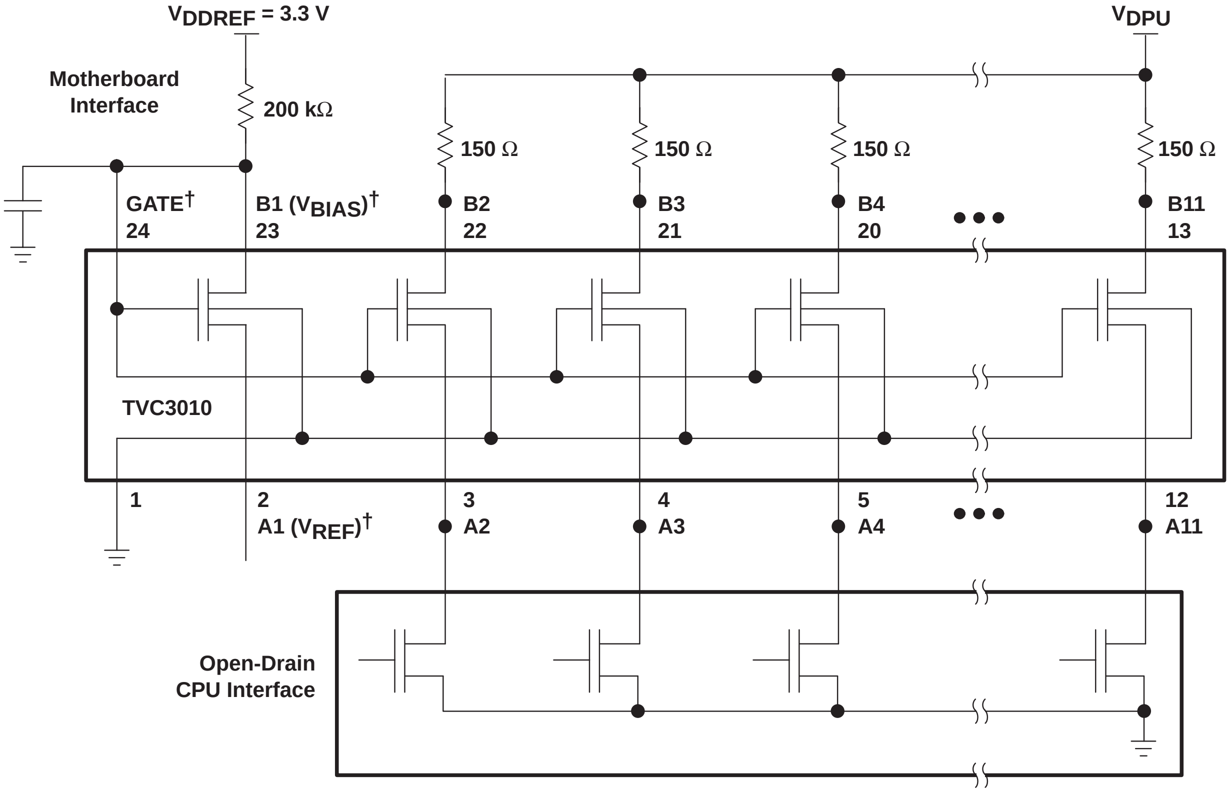


Figure 2. Thin Gate-Oxide Protection Application

APPLICATION INFORMATION

TVC voltage-limiting application

For the voltage-limiting configuration, the common GATE input must be connected to one side (A or B) of any one of the transistors (see Figure 3). This connection determines the V_{BIAS} input of the reference transistor. The V_{BIAS} input is connected through a pullup resistor (typically, 200 kΩ) to the V_{DD} supply. A filter capacitor on V_{BIAS} is recommended. The opposite side of the reference transistor is used as the reference voltage (V_{REF}) connection. The V_{REF} input must be less than V_{DDREF} − 1 V to bias the reference transistor into conduction. The reference transistor regulates the gate voltage (V_{GATE}) of all the pass transistors. V_{GATE} is determined by the characteristic gate-to-source voltage difference (V_{GS}) because $V_{GATE} = V_{REF} + V_{GS}$. The low-voltage side of the pass transistors has a high-level voltage limited to a maximum of $V_{GATE} − V_{GS}$, or V_{REF}.


VDDREF = 3.3 V
VDPU
Motherboard Interface
200 kΩ
150 Ω
150 Ω
150 Ω
150 Ω
GATE†
24
B1 (VBIAS)†
23
B2
22
B3
21
B4
20
B11
13
TVC3010
1
2
A1 (VREF)†
3
A2
4
A3
5
A4
12
A11
Open-Drain CPU Interface

† V_{REF} and V_{BIAS} can be applied to any one of the pass transistors. GATE must be connected externally to V_{BIAS}.

Figure 3. Typical Application Circuit

APPLICATION INFORMATION

electrical characteristics

The electrical characteristics of the NMOS transistors used in the TVC devices are illustrated by TI SPICE simulations. Figure 4 shows the test configuration for the TI SPICE simulations. The results, shown in Figures 5 and 6, show the current through a pass transistor versus the voltage at the source for different reference voltages. The plots of the dc characteristics clearly reveal that the device clamps at the desired reference voltage for the varying device environments.

Figure 5 shows the V-I characteristics, with low reference voltages and a reference-transistor drain-supply voltage of 3.3 V. To further investigate the spread of the V-I characteristic curves, V_{REF} was held at 2.5 V and I_{REF} was increased by raising V_{DDREF} (see Figure 6). The result was a tighter grouping of the V-I curves.

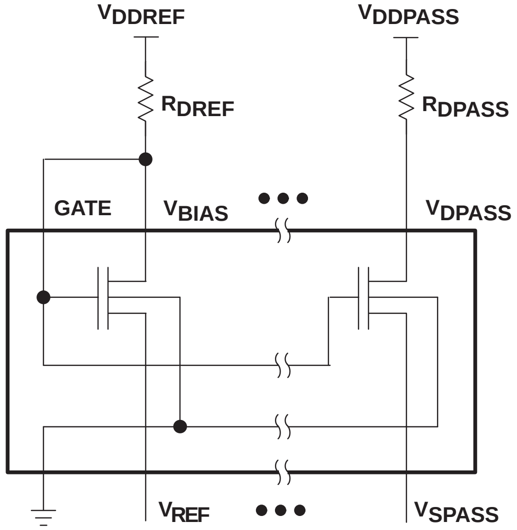


Figure 4. TI SPICE Simulation Schematic and Voltage-Node Names

APPLICATION INFORMATION

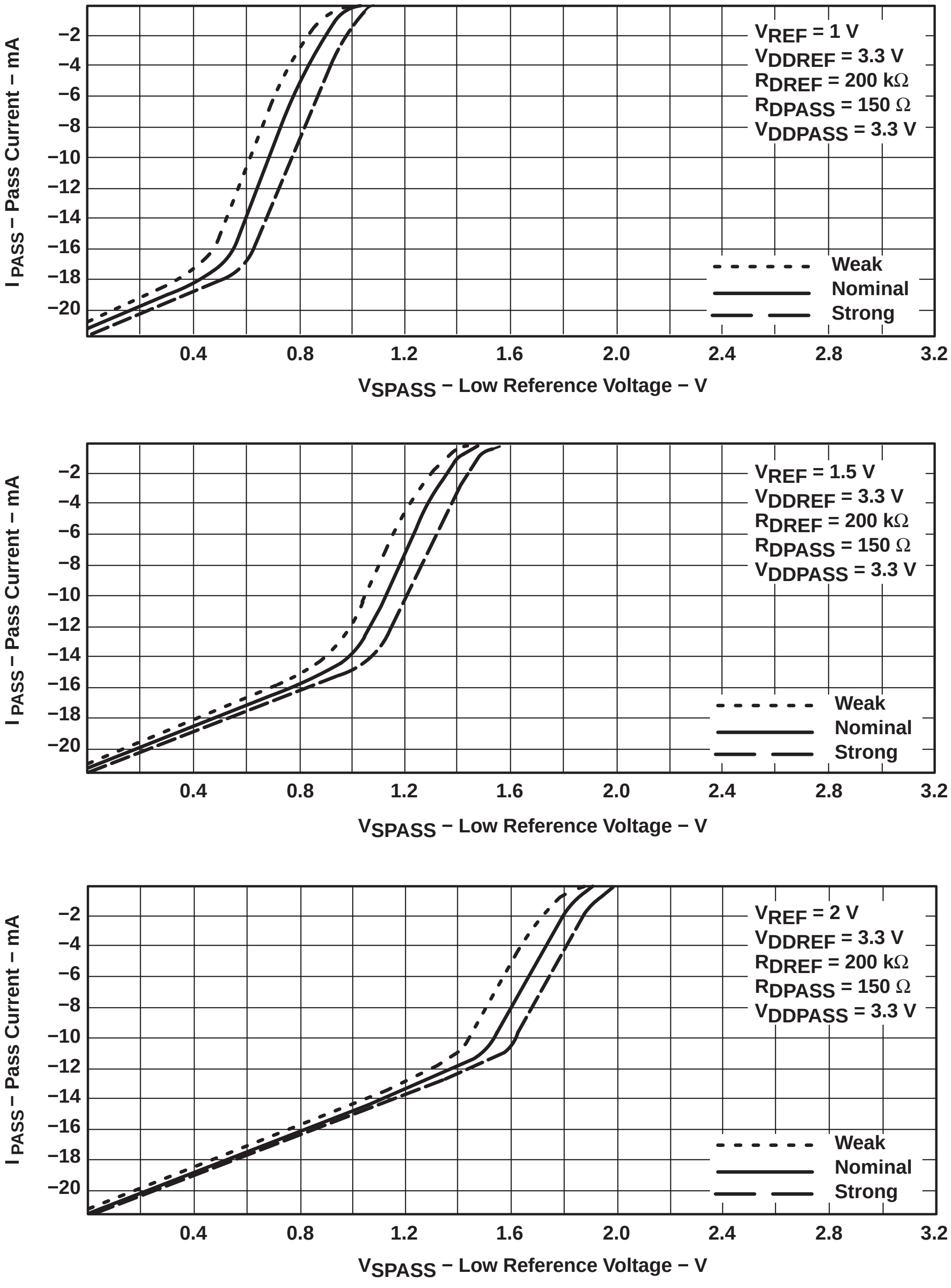


Figure 5. Electrical Characteristics at Low V_{REF} Voltages

APPLICATION INFORMATION

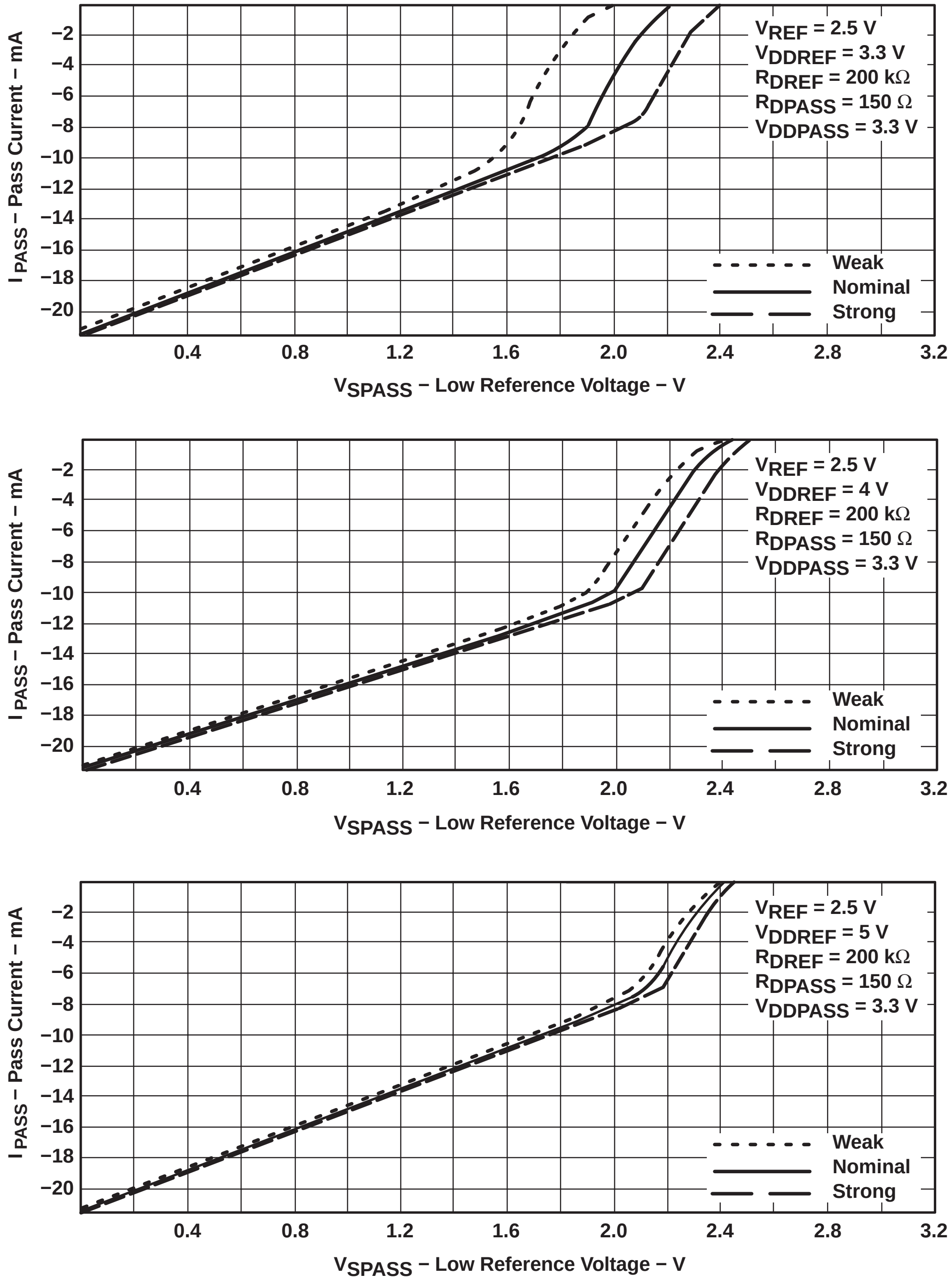


Figure 6. Electrical Characteristics at V_{REF} = 2.5 V

APPLICATION INFORMATION

features and benefits

The TVC family has several features that benefit a system designer when implementing a sensitive-I/O-protection solution. Table 1 lists these features and their associated benefits.

Table 1. Features and Benefits

FEATURES	BENEFITS
Any FET can be used as the reference transistor.	Ease of layout
All FETs on one die, tight process control	Very low spread of V_O relative to V_{REF}
No active control logic (passive device)	No logic power supply (V_{CC}) required
Flow-through pinout	Ease of trace routing
Devices offered in different bit-widths and packages	Optimizes design and cost effectiveness
Designer flexibility with V_{REF} input	Allows migration to lower-voltage I/Os without board redesign

conclusion

The TI TVC family provides the designer with a solution for protection of circuits with I/Os that are sensitive to high-state voltage-level overshoots. The flexibility of TVC enables a low-voltage migration path for advanced designs to align with industry standards.

frequently asked questions (FAQ)

1. Q: Can any of the transistors in the array be used as the reference transistor?

   A: Yes, any transistor can be used as long as its V_{BIAS} pin is connected to the GATE pin.

2. Q: In the recommended operating conditions table of the data sheet, the typical V_{BIAS} is 3.3 V. Should V_{BIAS} be equal to or greater than V_{REF} on the reference transistor?

   A: V_{BIAS} is a variable that is determined by V_{REF}. V_{BIAS} is connected to V_{DD} through a resistor to allow the bias voltage to be controlled by V_{REF}. V_{DD} can be as high as 5.5 V. V_{REF} needs to be at least 1 V less than V_{DDREF} on the reference transistor.

3. Q: Do both A and B ports have 5-V I/O tolerance or is 5-V I/O tolerance provided only on the low-voltage side?

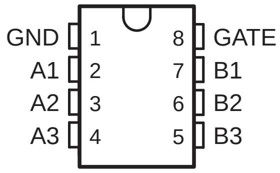
   A: Both ports are 5-V tolerant.

SN74TVC3306
DUAL VOLTAGE CLAMP

SCDS112C − MARCH 2001 − REVISED MARCH 2002

- **Designed to Be Used in Voltage-Limiting Applications**
- **3.5-Ω On-State Connection Between Ports A and B**
- **Flow-Through Pinout for Ease of Printed Circuit Board Trace Routing**
- **Direct Interface With GTL+ Levels**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DCT OR DCU PACKAGE
(TOP VIEW)



description

The SN74TVC3306 provides three parallel NMOS pass transistors with a common unbuffered gate. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

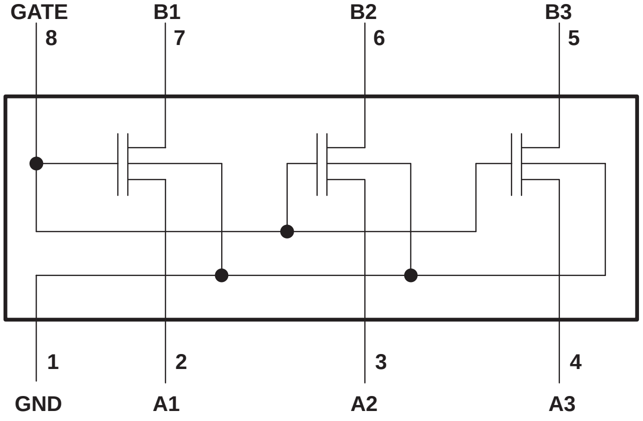
The device can be used as a dual switch, with the gates cascaded together to a reference transistor. The low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. This is done to protect components with inputs that are sensitive to high-state voltage-level overshoots.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DCT	Tape and reel	SN74TVC3306DCTR	FA6
	VSSOP − DCU	Tape and reel	SN74TVC3306DCUR	FA6

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

logic diagram (positive logic)



NOTE A: The SN74TVC3306 has bidirectional capability across many voltage levels. The voltage levels documented in this data sheet are examples.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Input/output voltage range, $V_{I/O}$ (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DCT package	220°C/W
	DCU package	227°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	5	V
V_{GATE}	GATE voltage	0	5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP[‡]	MAX	UNIT
V_{IK}	$I_I = -18$ mA,		$V_{GATE} = 0$			−1.2	V
I_{IH}	$V_I = 5$ V,		$V_{GATE} = 0$			5	μA
$C_{i(GATE)}$	$V_I = 3$ V or 0				11		pF
$C_{io(off)}$	$V_O = 3$ V or 0,		$V_{GATE} = 0$		4	6	pF
$C_{io(on)}$	$V_O = 3$ V or 0,		$V_{GATE} = 3$ V		10.5	12.5	pF
r_{on}[§]	$V_I = 0$	$I_O = 64$ mA	$V_{GATE} = 4.5$ V		3.5	5.5	Ω
			$V_{GATE} = 3$ V		4.7	7	
			$V_{GATE} = 2.3$ V		6.3	9.5	
			$V_{GATE} = 1.5$ V		25.5	32	
	$V_I = 2.4$ V	$I_O = 15$ mA	$V_{GATE} = 4.5$ V		4.8	7.5	
			$V_{GATE} = 3$ V		14.7	23	
	$V_I = 1.7$ V		$V_{GATE} = 2.3$ V		11.3	16.5	

[‡] All typical values are at $T_A = 25°C$.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

ac performance (translating down)

switching characteristics over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 3.3 V, V_{IL} = 0, and V_M = 1.15 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	0.8	0	0.6	0	0.3	ns
t_{PHL}			0	1.2	0	1	0	0.5	

switching characteristics over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 2.5 V, V_{IL} = 0, and V_M = 0.75 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	1	0	0.7	0	0.4	ns
t_{PHL}			0	1.3	0	1	0	0.6	

ac performance (translating up)

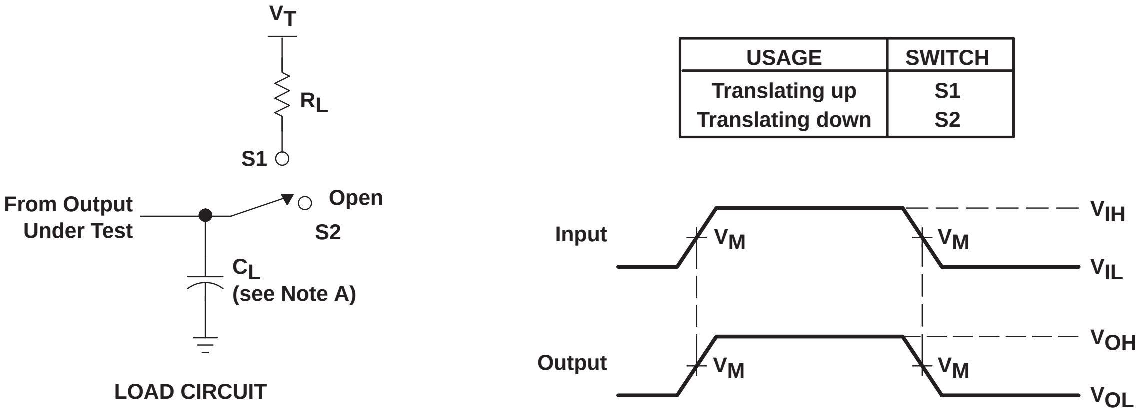
switching characteristics over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 2.3 V, V_{IL} = 0, V_T = 3.3 V, V_M = 1.15 V, and R_L = 300 Ω (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	0.9	0	0.6	0	0.4	ns
t_{PHL}			0	1.4	0	1.1	0	0.7	

switching characteristics over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 1.5 V, V_{IL} = 0, V_T = 2.5 V, V_M = 0.75 V, and R_L = 300 Ω (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	1	0	0.6	0	0.4	ns
t_{PHL}			0	1.3	0	1.3	0	0.8	

PARAMETER MEASUREMENT INFORMATION

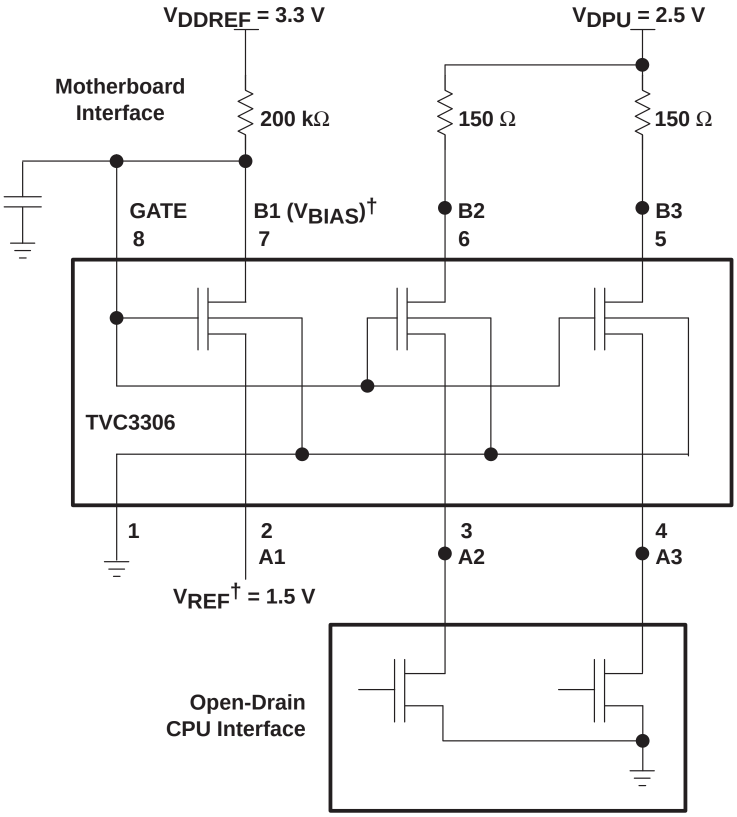

V_T
R_L
S1
From Output Under Test
Open
S2
C_L (see Note A)
LOAD CIRCUIT
Input
V_M
V_M
V_{IH}
V_{IL}
Output
V_M
V_M
V_{OH}
V_{OL}

USAGE	SWITCH
Translating up	S1
Translating down	S2

NOTES:
- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
- C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit for Outputs

APPLICATION INFORMATION


V_{DDREF} = 3.3 V
V_{DPU} = 2.5 V
Motherboard Interface
200 kΩ
150 Ω
150 Ω
GATE
8
B1 (V_{BIAS})†
7
B2
6
B3
5
TVC3306
1
2
A1
3
A2
4
A3
V_{REF}† = 1.5 V
Open-Drain CPU Interface

† V_{REF} and V_{BIAS} can be applied to any one of the pass transistors. GATE must be connected externally to V_{BIAS}.

Figure 2. Typical Application Circuit

For the clamping configuration, the common GATE input must be connected to one side (An or Bn) of any one of the pass transistors, making that the V_{BIAS} connection of the reference transistor and the opposite side (Bn or An) the V_{REF} connection. When V_{BIAS} is connected through a 200-kΩ resistor to a 3-V to 5.5-V V_{CC} supply and V_{REF} is set to 0 V to V_{CC} − 0.6 V, the output of each switch has a maximum clamp voltage equal to V_{REF}. A filter capacitor on V_{BIAS} is recommended.

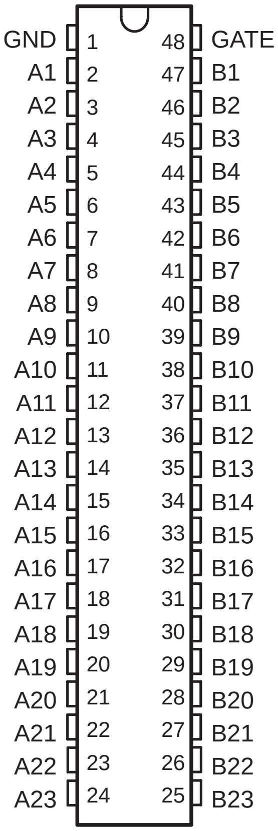
application operating conditions (see Figure 2)

		MIN	TYP‡	MAX	UNIT
V_{BIAS}	BIAS voltage	V_{REF} + 0.6	2.1	5	V
V_{GATE}	GATE voltage	V_{REF} + 0.6	2.1	5	V
V_{REF}	Reference voltage	0	1.5	4.4	V
V_{DPU}	Drain pullup voltage	2.36	2.5	2.64	V
I_{PASS}	Pass-transistor current		14		mA
I_{REF}	Reference-transistor current		5		µA
T_A	Operating free-air temperature	−40		85	°C

‡ All typical values are at T_A = 25°C.

- **Member of the Texas Instruments Widebus™ Family**
- **Designed to Be Used in Voltage-Limiting Applications**
- **6.5-Ω On-State Connection Between Ports A and B**
- **Flow-Through Pinout for Ease of Printed Circuit Board Trace Routing**
- **Direct Interface With GTL+ Levels**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The SN74TVC16222A provides 23 parallel NMOS pass transistors with a common gate. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device can be used as a 22-bit switch, with the gates cascaded together to a reference transistor. The low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. This is done to protect components with inputs that are sensitive to high-state voltage-level overshoots. (See *Application Information* in this data sheet.)

All of the transistors in the TVC array have the same electrical characteristics; therefore, any one of them can be used as the reference transistor. Because, within the device, the characteristics from transistor to transistor are equal, the maximum output high-state voltage (V_{OH}) is approximately the reference voltage (V_{REF}), with minimal deviation from one output to another. This is a benefit of the TVC solution over discrete devices. Because the fabrication of the transistors is symmetrical, either port connection of each bit can be used as the low-voltage side, and the I/O signals are bidirectional through each FET.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74TVC16222DL	TVC16222A
		Tape and reel	SN74TVC16222DLR	
	TSSOP − DGG	Tape and reel	SN74TVC16222DGGR	TVC16222A
	TVSOP − DGV	Tape and reel	SN74TVC16222DGVR	TW222A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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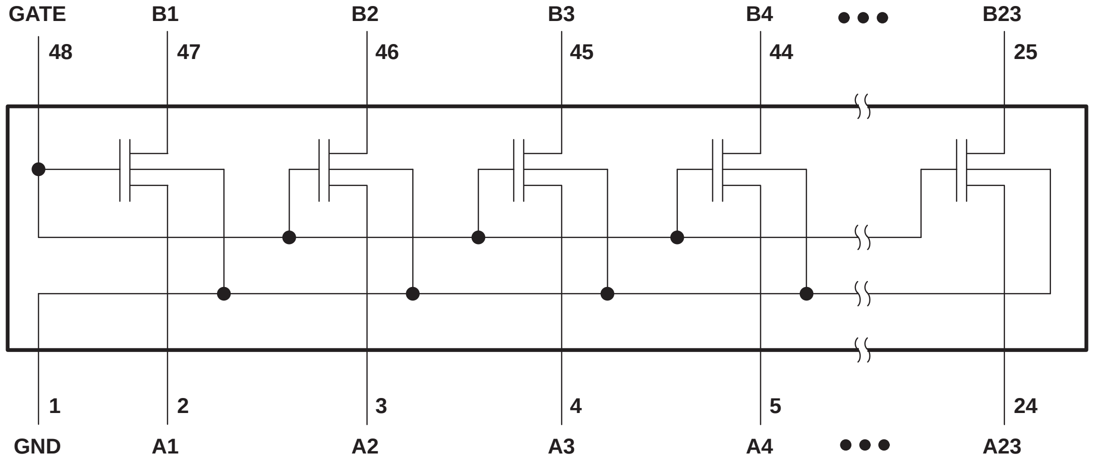
simplified schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, V_I (see Note 1)		−0.5 V to 7 V
Input/output voltage range, $V_{I/O}$ (see Note 1)		−0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	TYP	MAX	UNIT
$V_{I/O}$	Input/output voltage	0		5	V
V_{GATE}	GATE voltage	0		5	V
I_{PASS}	Pass-transistor current		20	64	mA
T_A	Operating free-air temperature	−40		85	°C

application operating conditions (see Figure 3)

		MIN	TYP	MAX	UNIT
V_{BIAS}	BIAS voltage	V_{REF} + 0.6	2.1	5	V
V_{GATE}	GATE voltage	V_{REF} + 0.6	2.1	5	V
V_{REF}	Reference voltage	0	1.5	4.4	V
V_{DPU}	Drain pullup voltage	2.36	2.5	2.64	V
I_{PASS}	Pass-transistor current		14	20	mA
I_{REF}	Reference-transistor current		5		µA
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	$V_{BIAS} = 0$,	$I_I = -18$ mA				−1.2	V
V_{OL}	$I_{REF} = 5\ \mu A$, $V_{DPU} = 2.625$ V,	$V_{REF} = 1.365$ V, $R_{DPU} = 150\ \Omega$	$V_S = 0.175$ V, See Figure 2			350	mV
$C_{i(GATE)}$	$V_I = 3$ V or 0				73		pF
$C_{io(off)}$	$V_O = 3$ V or 0				4	12	pF
$C_{io(on)}$	$V_O = 3$ V or 0				12	25	pF
r_{on}‡	$I_{REF} = 5\ \mu A$, $V_{DPU} = 2.625$ V,	$V_{REF} = 1.365$ V, $R_{DPU} = 150\ \Omega$	$V_S = 0.175$ V, See Figure 2			12.5	Ω

† All typical values are at $T_A = 25°C$.

‡ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

electrical characteristics from −40°C to 75°C

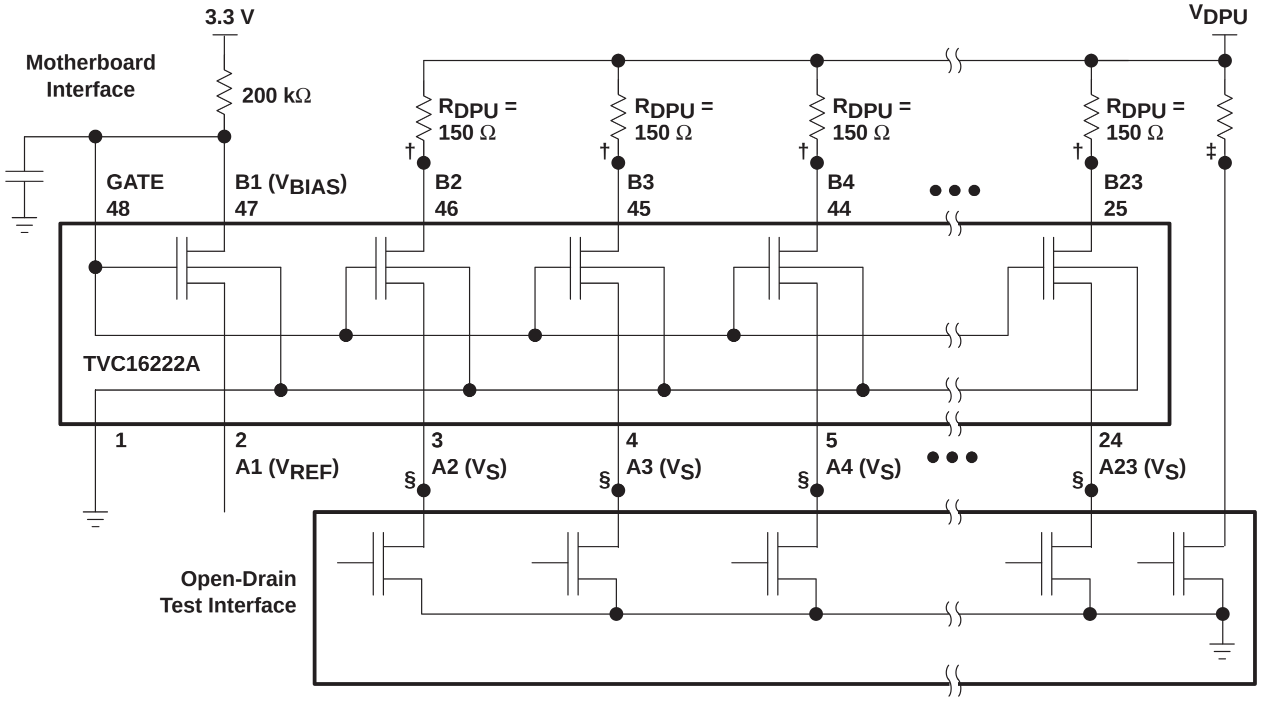
PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
r_{on}‡	$I_{REF} = 5\ \mu A$, $V_{DPU} = 2.625$ V,	$V_{REF} = 1.552$ V, $R_{DPU} = 150\ \Omega$	$V_S = 0.175$ V, See Figure 2		10	Ω

‡ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, V_{DPU} = 2.36 V to 2.64 V (unless otherwise noted) (see Figure 1)

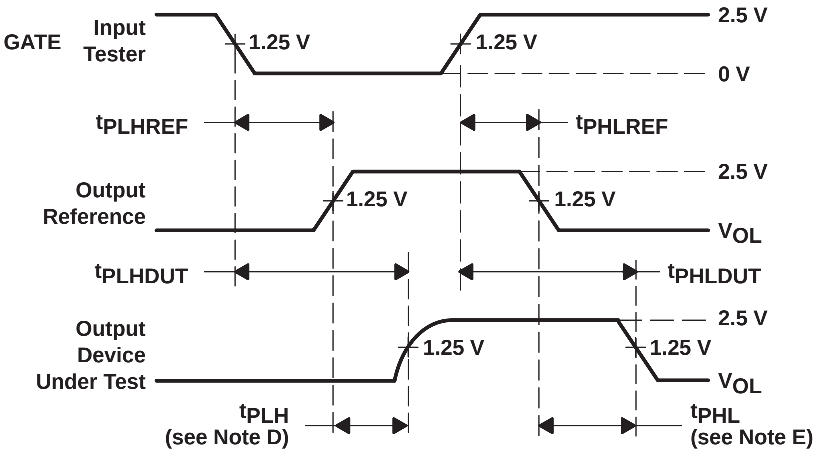
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	A or B	B or A	0	4	ns
t_{PHL}			0	4	

PARAMETER MEASUREMENT INFORMATION


3.3 V
Motherboard Interface
200 kΩ
VDPU
RDPU = 150 Ω
RDPU = 150 Ω
RDPU = 150 Ω
RDPU = 150 Ω
†
‡
GATE 48
B1 (VBIAS) 47
B2 46
B3 45
B4 44
B23 25
TVC16222A
1
2 A1 (VREF)
3 A2 (VS)
4 A3 (VS)
5 A4 (VS)
24 A23 (VS)
§
Open-Drain Test Interface

TESTER CALIBRATION SETUP (see Note C)

DEFINITION	SYMBOL
Output tested	†
Output reference	‡
Input tested	§


GATE
Input Tester
1.25 V
1.25 V
2.5 V
0 V
tPLHREF
tPHLREF
Output Reference
1.25 V
1.25 V
2.5 V
VOL
tPLHDUT
tPHLDUT
Output Device Under Test
1.25 V
1.25 V
2.5 V
VOL
tPLH (see Note D)
tPHL (see Note E)

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES:
- A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \le$ 2 ns, $t_f \le$ 2 ns.
- B. The outputs are measured one at a time with one transition per measurement.
- C. Test procedure: t_{PLHREF} and t_{PHLREF} are obtained by measuring the propagation delay of a reference measuring point. t_{PLHDUT} and t_{PHLDUT} are obtained by measuring the propagation delay of the device under test.
- D. $t_{PLH} = t_{PLHDUT} - t_{PLHREF}$
- E. $t_{PHL} = t_{PHLDUT} - t_{PHLREF}$

Figure 1. Tester Calibration Setup and Voltage Waveforms

APPLICATION INFORMATION

TVC background information

In personal computer (PC) architecture, there are industry-accepted bus standards. These standards define, among other things, the I/O voltage levels at which the bus communicates. Examples include the GTL+ host bus, the AGP graphics port, and the PCI local bus. In new designs, the system components must communicate with existing bus infrastructure. Providing an evolutionary upgrade path is important in the design of PC architecture, but the existing bus standards must be preserved.

To achieve the ever-present need for smaller, faster, lighter devices that draw less power, yet have faster performance, most new high-performance digital integrated circuits are designed and produced with advanced submicron semiconductor process technologies. These devices have thin gate-oxide or short channel lengths and very low absolute-maximum voltages that can be tolerated at the inputs/outputs (I/Os) without causing damage. In many cases, the I/Os of these devices are not tolerant of the high-state voltage levels on the preexisting buses with which they must communicate. Therefore, it became necessary to protect the I/Os of devices by limiting the I/O voltages.

The Texas Instruments (TI) translation voltage-clamp (TVC) family is designed specifically for protecting sensitive I/Os (see Figure 2). The information in this data sheet describes the I/O-protection application of the TVC family and should enable the design engineer to successfully implement an I/O-protection circuit utilizing the TI TVC solution.

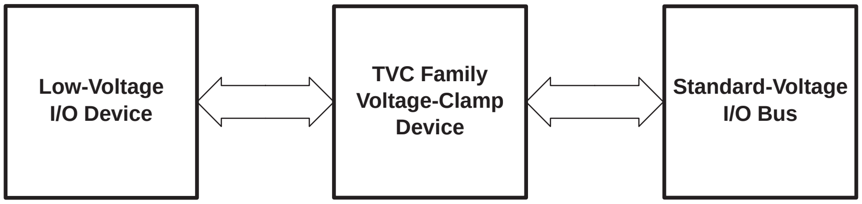
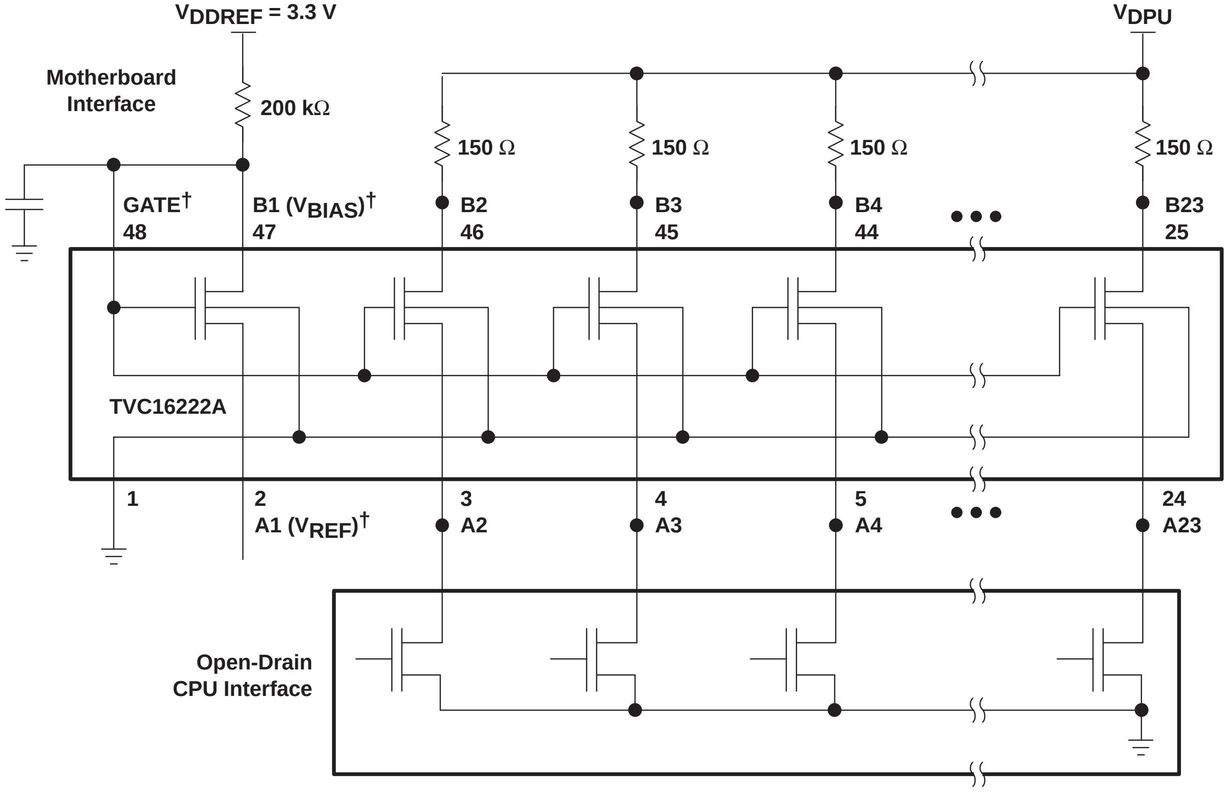


Figure 2. Thin Gate-Oxide Protection Application

APPLICATION INFORMATION

TVC voltage-limiting application

For the voltage-limiting configuration, the common GATE input must be connected to one side (A or B) of any one of the transistors (see Figure 3). This connection determines the V_{BIAS} input of the reference transistor. The V_{BIAS} input is connected through a pullup resistor (typically 200 kΩ) to the V_{DD} supply. A filter capacitor on V_{BIAS} is recommended. The opposite side of the reference transistor is used as the reference voltage (V_{REF}) connection. The V_{REF} input must be less than V_{DDREF} − 1 V to bias the reference transistor into conduction. The reference transistor regulates the gate voltage (V_{GATE}) of all the pass transistors. V_{GATE} is determined by the characteristic gate-to-source voltage difference (V_{GS}) because $V_{GATE} = V_{REF} + V_{GS}$. The low-voltage side of the pass transistors has a high-level voltage limited to a maximum of $V_{GATE} - V_{GS}$, or V_{REF}.


V_{DDREF} = 3.3 V
V_{DPU}
Motherboard Interface
200 kΩ
150 Ω
150 Ω
150 Ω
150 Ω
GATE†
48
B1 (V_{BIAS})†
47
B2
46
B3
45
B4
44
B23
25
TVC16222A
1
2
A1 (V_{REF})†
3
A2
4
A3
5
A4
24
A23
Open-Drain CPU Interface

† V_{REF} and V_{BIAS} can be applied to any one of the pass transistors. GATE must be connected externally to V_{BIAS}.

Figure 3. Typical Application Circuit

APPLICATION INFORMATION

electrical characteristics

The electrical characteristics of the NMOS transistors used in the TVC devices are illustrated by TI SPICE simulations. Figure 4 shows the test configuration for the TI SPICE simulations. The results, shown in Figures 5 and 6, show the current through a pass transistor versus the voltage at the source for different reference voltages. The plots of the dc characteristics clearly reveal that the device clamps at the desired reference voltage for the varying device environments.

Figure 5 shows the V-I characteristics with low reference voltages and a reference-transistor drain-supply voltage of 3.3 V. To further investigate the spread of the V-I characteristic curves, V_{REF} was held at 2.5 V and I_{REF} was increased by raising V_{DDREF} (see Figure 6). The result was a tighter grouping of the V-I curves.

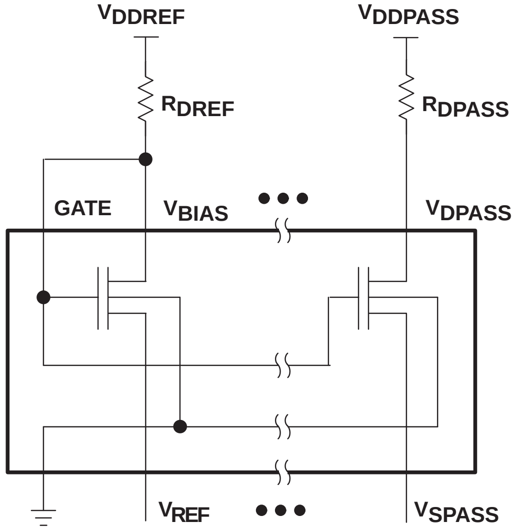


Figure 4. TI SPICE-Simulation Schematic and Voltage-Node Names

APPLICATION INFORMATION

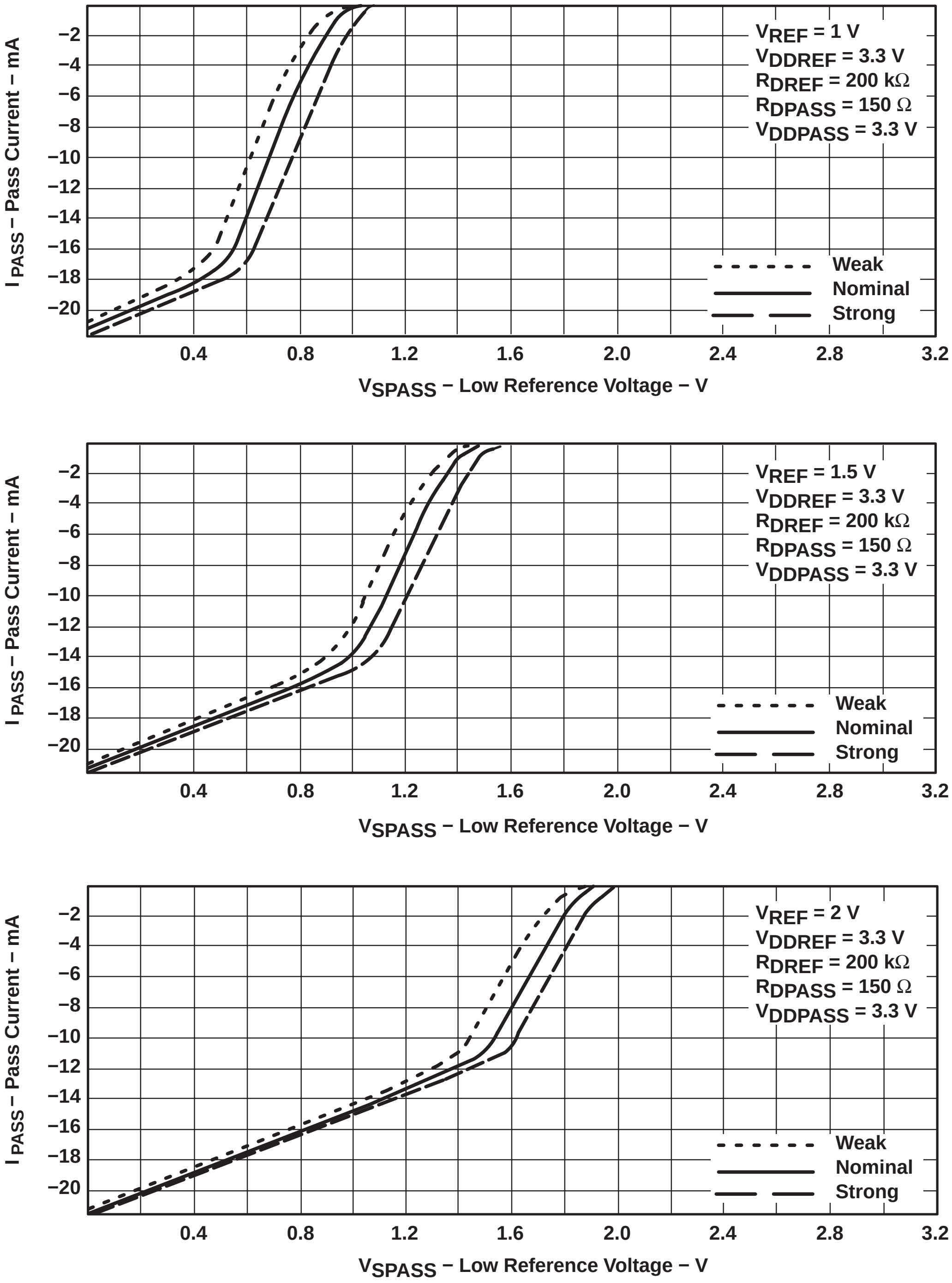


Figure 5. V-I Electrical Characteristics at Low V_{REF} Voltages

APPLICATION INFORMATION

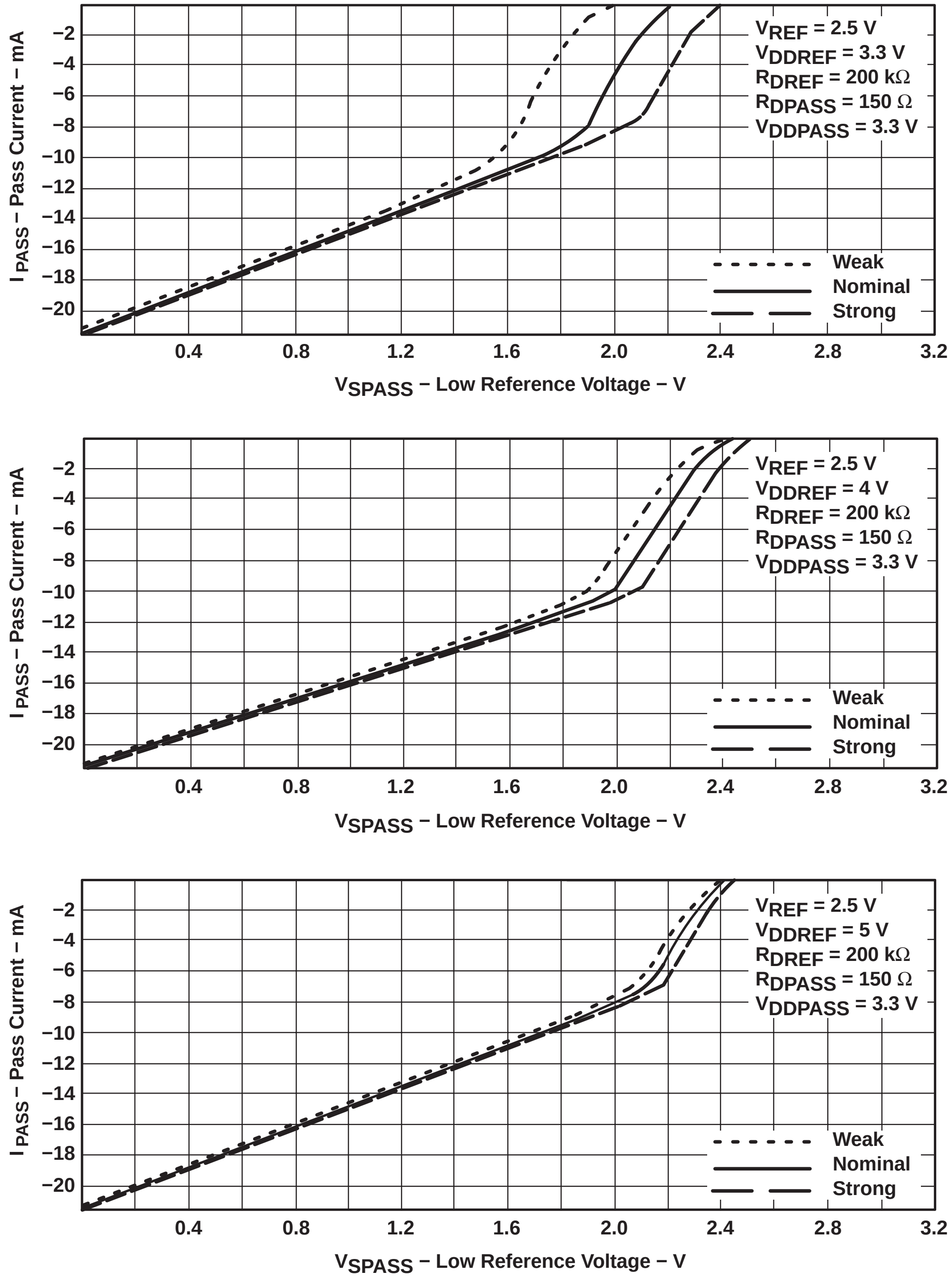


Figure 6. V-I Electrical Characteristics at V_{REF} = 2.5 V

APPLICATION INFORMATION

features and benefits

The TVC family has several features that benefit a system designer when implementing a sensitive-I/O-protection solution. Table 1 lists these features and their associated benefits.

Table 1. Features and Benefits

FEATURES	BENEFITS
Any FET can be used as the reference transistor.	Ease of layout
All FETs on one die, tight process control	Very low spread of V_O relative to V_{REF}
No active control logic (passive device)	No logic power supply (V_{CC}) required
Flow-through pinout	Ease of trace routing
Devices offered in different bit widths and packages	Optimizes design and cost effectiveness
Designer flexibility with V_{REF} input	Allows migration to lower-voltage I/Os without board redesign

conclusion

The TI TVC family provides the designer with a solution for protection of circuits with I/Os that are sensitive to high-state voltage-level overshoots. The flexibility of TVC enables a low-voltage migration path for advanced designs to align with industry standards.

frequently asked questions (FAQs)

1. Q: Can any of the transistors in the array be used as the reference transistor?

   A: Yes, any transistor can be used as long as its V_{BIAS} pin is connected to the GATE pin.

2. Q: In the *recommended operating conditions* table of the data sheet, the typical V_{BIAS} is 3.3 V. Should V_{BIAS} be equal to or greater than V_{REF} on the reference transistor?

   A: V_{BIAS} is a variable that is determined by V_{REF}. V_{BIAS} is connected to V_{DD} through a resistor to allow the bias voltage to be controlled by V_{REF}. V_{DD} can be as high as 5.5 V. V_{REF} needs to be at least 1 V less than V_{DDREF} on the reference transistor.

3. Q: Do both A and B ports have 5-V I/O tolerance or is 5-V I/O tolerance provided only on the low-voltage side?

   A: Both ports are 5-V tolerant.

Insert Tab Here

Insert Tab Here

Texas Instruments

Application Report

SCDA008 - July 2003

CBT-C, CB3T, and CB3Q Signal-Switch Families

Christopher Graves, Moshiul Haque, and Ernest Cox *Standard Linear & Logic*

ABSTRACT

Signal-switch devices are used widely in applications requiring bus isolation, multiplexing, demultiplexing, and voltage translation. Compared to other logic and linear product alternatives, signal switches are the fastest and least power consuming. Texas Instruments (TI) CBT-C, CB3Q, and CB3T signal-switch families have low on-state resistance, negligible power consumption, and better undershoot protection, compared to the older switch families. These qualities make CBT-C, CB3Q, and CB3T devices very good candidates for today's high-speed applications that require switches. This application report discusses some of the critical characteristics, features, and applications of TI's newest switches.

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1 Introduction

On-off switches are one of the most common control elements in electrical circuitry. This has evolved over the years, from the manually operated circuit breaker of the early experiments to the multiswitch integrated circuit of today. In every application, the function of the switch remains the same: to isolate or connect two sections of an electrical circuit. Therefore, an ideal switch should have zero resistance (short circuit) when on and infinite resistance (open circuit) when off. However, in practical applications, a bus switch should have as low resistance as possible when on, for bus connection, and as high resistance as possible when off, for bus isolation.

2 Semiconductor Switches

An insulated-gate field-effect transistor (IGFET) switch is a widely used electronic switch. A metal-oxide semiconductor field-effect transistor (MOSFET) is one type of IGFET. Although the term MOSFET is more commonly used, now most of the electronic switches do not use the metal oxide as the gate. Instead, a more advanced process is being used to form the gate. TI uses advanced poly-silicon gate-enhancement-mode transistor technology to fabricate semiconductor switches, which gives more control of performance characteristics. Throughout this application report the term MOSFET and the associated terms related to MOSFET are used because they are more common in semiconductor literature. When sufficient bias voltage is applied to the gate of a MOSFET, it creates a low-resistance path between its source and drain. When the bias voltage is removed, the resistance of this path becomes very large. MOSFETs can be of two types, n-channel MOSFET (NMOS) and p-channel MOSFET (PMOS).

2.1 NMOS Switch

The symbol of an NMOS is shown in Figure 1. The source and the drain of an NMOS are interchangeable. The terminal with the lowest voltage is considered to be the source. The resistance between the drain and the source depends on the voltage difference between the gate and the source (V_{GS}). When there is sufficient voltage applied to the gate with respect to the source, the switch becomes conductive, and a voltage signal applied to the drain passes through this switch without distortion. The gate-to-source voltage at which the NMOS begins conduction is known as the threshold voltage (V_T). If the gate-to-source voltage becomes significantly less than the threshold voltage of the NMOS (V_T), the channel resistance increases rapidly.

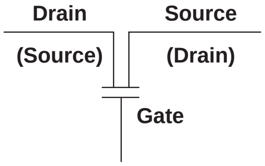


Figure 1. NMOS

2.2 PMOS Switch

A PMOS is similar to an NMOS (see Figure 2). However, to keep the source-to-drain resistance low, the difference in the source-to-gate voltage (V_{SG}) should be greater than the threshold voltage. In a PMOS, the terminal with the lowest voltage is considered to be the drain.

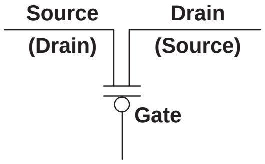


Figure 2. PMOS

3 Basic Signal-Switch Structures

Signal switches in their simplest form are MOSFET structures, with the gate driven by a CMOS inverter. Three types of structures are most common:

- NMOS series switch
- NMOS/PMOS parallel switch
- NMOS series switch, with the charge pump

3.1 NMOS Series Switch

The most basic signal-switch structure is an NMOS pass transistor, with the gate driven by a CMOS inverter. The simplified structure is shown in Figure 3.

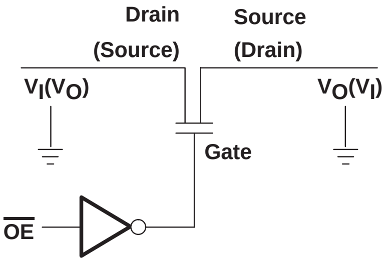


Figure 3. NMOS Series Switch

When the output enable ($\overline{OE}$) signal is low, the voltage at the gate is high, or equal to V_{CC}. If the voltage at the drain (V_I) is less than V_{CC} by the threshold voltage of the n-channel transistor, the on-state resistance (r_{on}) is low and the voltage at the source is equal to V_I ($V_O = V_I$). If V_I approaches V_{CC}, r_{on} increases rapidly, the source voltage does not increase with the drain voltage, and the output voltage remains at $V_{CC} - V_T$. A limitation of the NMOS series switch is that it can pass signals only up to a threshold voltage below V_{CC}. Figure 4 shows the general shape of r_{on} vs V_I characteristic of a typical NMOS series switch.

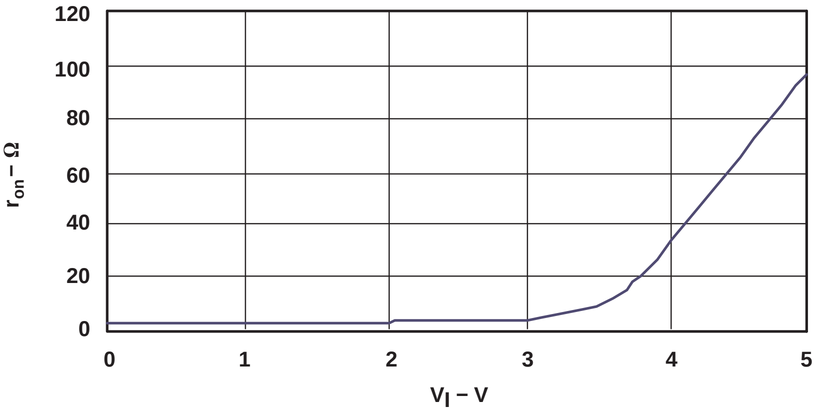


Figure 4. r_{on} **vs** V_I **Characteristic of an NMOS Series Switch (**V_{CC} **= 5 V,** I_O **= −15 mA)**

3.2 NMOS/PMOS Parallel Switch

An NMOS/PMOS parallel switch consists of an n-channel pass transistor in parallel with a p-channel pass transistor. Figure 5 shows the basic structure of an NMOS/PMOS parallel switch. In an n-channel MOSFET, the source-to-drain resistance is low when the drain voltage is less than $V_G – V_T$, where V_G is the gate voltage. In a p-channel MOSFET, the source-to-drain resistance is low when the source voltage is greater than $V_T + V_G$. With the parallel combination of n-channel and p-channel pass transistors, the source-to-drain, or channel resistance, can be lowered for the entire input voltage range from 0 V to V_G. When $\overline{OE}$ is low, V_G in NMOS/PMOS parallel switch is V_{CC}, and signals ranging from 0 V to V_{CC} can be passed through this switch. Figure 6 shows the general shape of the r_{on} vs V_I characteristics of a typical NMOS/PMOS parallel switch, as well as the NMOS and PMOS characteristics. The shape of r_{on} vs V_I curve may be different, depending on the structures of NMOS and PMOS. The disadvantage of the NMOS/PMOS parallel switch is that the input and output capacitances increase due to the additional source and drain area of the combined transistors.

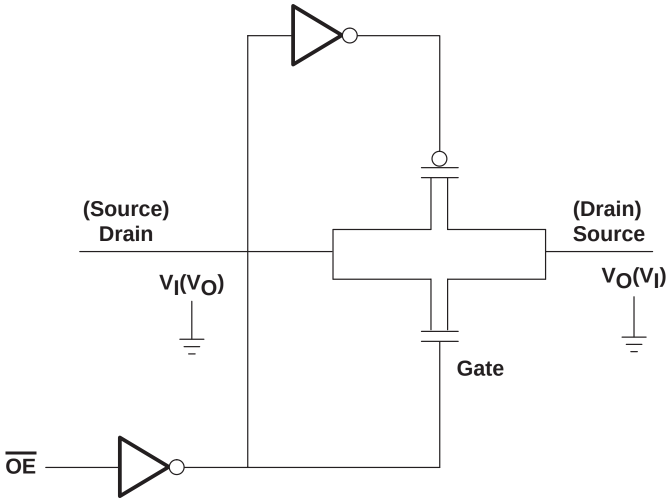


Figure 5. Basic Structure of an NMOS/PMOS Parallel Switch

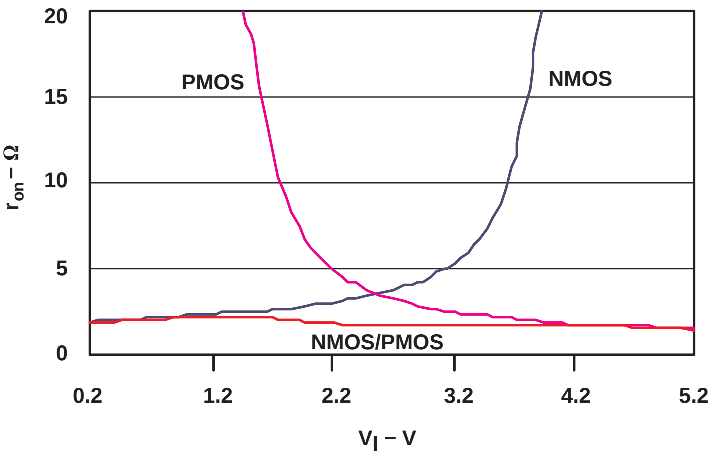


Figure 6. r_{on} vs V_I Characteristics of a Typical NMOS/PMOS Parallel Switch (V_{CC} = 5 V)

3.3 NMOS Series Switch With the Charge Pump

Although, in an NMOS/PMOS parallel switch, source-to-drain resistance is lower than in an NMOS series switch, the PMOS adds capacitance, which is undesirable for some applications. To solve this problem, another type of switch structure is used that involves a charge-pump circuit in the NMOS series switch. The charge-pump circuit generates a voltage at the gate of the NMOS that is 2 V to 3 V higher than V_{CC}. As a result, when the input reaches the V_{CC} level, the switch still is on and the output voltage is equal to the input voltage over the 0 V to V_{CC} input voltage range. The disadvantage of implementing a charge-pump circuit in the NMOS series switch is the additional power consumption because of the charge-pump circuit. Figure 7 shows a simple schematic of an NMOS series switch with the charge pump, and Figure 8 shows the r_{on} vs V_I characteristic.

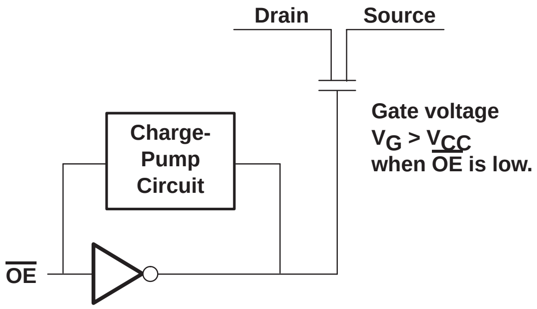


Figure 7. Basic Structure of an NMOS Series Switch With the Charge Pump

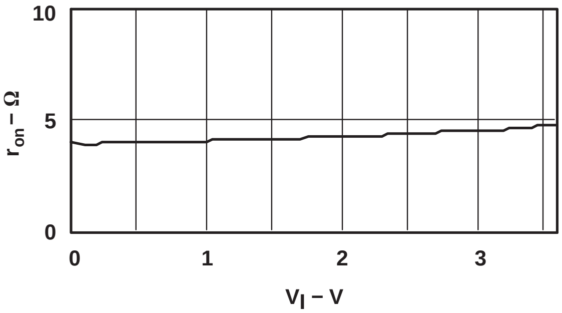


Figure 8. r_{on} vs V_I in an NMOS Series Switch With the Charge Pump (V_{CC} = 3.6 V)

4 Key Concerns in Digital-Switch Applications

4.1 Undershoot

Undershoot is a typical phenomenon in high-speed applications where impedance mismatches cause excessive ringing in the system. This poses a serious problem to bus switches that are turned off and attempt to isolate different buses. In this state, the gate voltage of the n-channel pass transistors are at ground potential, but a negative voltage on either I/O port with a magnitude greater than the NMOS V_T will cause the switch to conduct and no longer isolate the buses. Therefore, undershoots with a large magnitude and long duration result in data corruption, if no undershoot protection circuitry is included in the signal-switch design. The schematics in Figure 9 demonstrate the phenomenon of undershoots. For normal input voltages ranging from 0 V to V_{CC}, the switch is in the high-impedance state and the output bus is isolated from the input bus. The undershoot produces a glitch at the isolated bus, as shown in Figure 9.

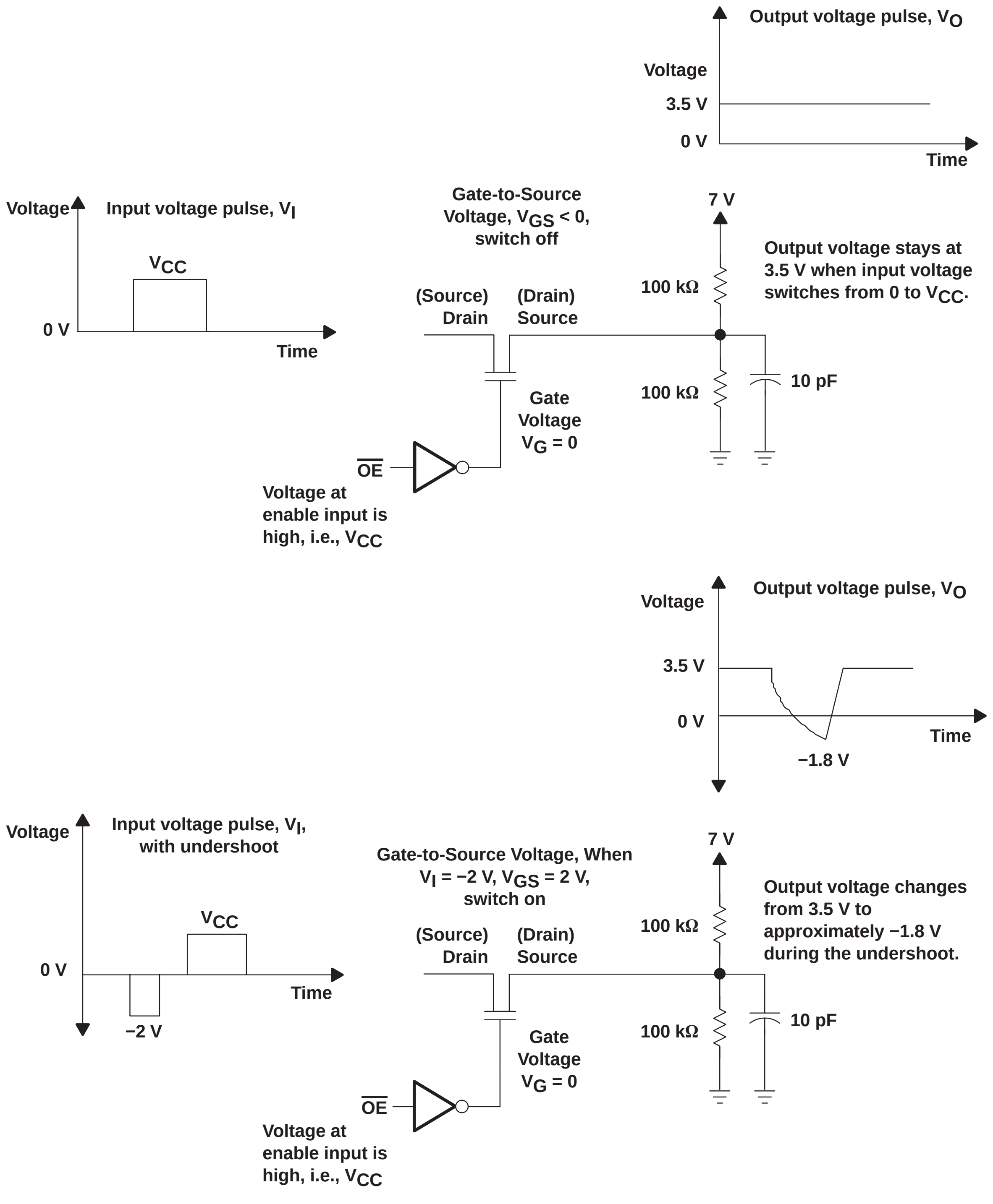

Output voltage pulse, V_O
Voltage
3.5 V
0 V
Time
Voltage
Input voltage pulse, V_I
V_{CC}
0 V
Time
Gate-to-Source Voltage, $V_{GS} < 0$, switch off
7 V
Output voltage stays at 3.5 V when input voltage switches from 0 to V_{CC}.
100 kΩ
(Source) Drain
(Drain) Source
100 kΩ
10 pF
Gate Voltage $V_G = 0$
OE
Voltage at enable input is high, i.e., V_{CC}
Voltage
Output voltage pulse, V_O
3.5 V
0 V
Time
−1.8 V
Voltage
Input voltage pulse, V_I, with undershoot
Gate-to-Source Voltage, When $V_I = -2$ V, $V_{GS} = 2$ V, switch on
7 V
Output voltage changes from 3.5 V to approximately −1.8 V during the undershoot.
V_{CC}
0 V
Time
−2 V
100 kΩ
(Source) Drain
(Drain) Source
100 kΩ
10 pF
Gate Voltage $V_G = 0$
OE
Voltage at enable input is high, i.e., V_{CC}

Figure 9. Undershoot in NMOS Series-Switch Devices When Disabled

There are two solutions to prevent the NMOS from turning on during the undershoot event while disabled:

- Capture or clamp the input undershoot energy. In this method, a clamp circuit is connected to ground or V_{CC}. This clamp circuit prevents the NMOS from turning on while an undershoot event occurs.
  - Schottky Clamp. In this method, a Schottky diode is connected from the I/O port of the switch to ground. When the voltage at the I/O port goes below ground, the diode is forward biased and clamps the source or drain voltage, keeping the input and output isolated. An example of this type of device is the CBTS bus switch provided by TI.
  - Active clamp to V_{CC}. In this method, an active clamp circuit is connected to V_{CC}, which tries to counteract the undershoot voltage by pulling the input voltage to V_{CC}. An example of this type of device is the CBTK bus switch provided by TI.
- Force the gate voltage of the NMOS to track the negative input voltage. TI’s new CBT-C family uses this method to prevent undershoot. This method of protection is described later in this application report.

4.2 r_{on}

r_{on} is the resistance of the switch when turned on. r_{on} should be as low as possible to reduce signal loss and to reduce propagation delay. Propagation delay of the switch depends on the RC time constant, which is made up of the switch r_{on} and the load capacitance. For applications in transmission-line environments, r_{on} should be less than, or equal to, the line impedance to minimize unwanted signal reflections. For digital applications where the switch is connected to a resistive load, the switch resistance and the load resistance form a voltage divider. Therefore, in this case, r_{on} should be as low as possible to maintain a valid input logic high (i.e., V_{IH}) of the downstream devices. r_{on} not only should be small, but also should be flat across the input voltage range to maintain a linear signal change from input to output. Signal distortion depends on the flatness of the r_{on} vs V_I curve, that is, equal to $20\log\Delta r_{on} / R_L$, where R_L is the load resistance. So, to keep signal distortion minimum as the signal amplitude varies, r_{on} should be kept flat over the whole input signal range. In NMOS series switches, special gate voltage-boost circuitry is needed to keep r_{on} flat over the V_{CC} range. In NMOS/PMOS parallel switches, r_{on} is fairly constant and may have multiple peak values within 0 V to V_{CC} input voltage range. The shape of the r_{on} vs V_I curve depends on the threshold voltages of NMOS and PMOS (see Figure 6).

4.3 $C_{io(off)}$

$C_{io(off)}$ for a through switch is the off-state capacitance of one channel, measured from either the input or output of the switch. For a multiplexer or bus-exchange switch, $C_{io(off)}$ may include off-state capacitance for multiple channels. $C_{io(off)}$ should be as small as possible to prevent capacitive loading of the bus. Reducing C_{io} requires less drain and source area of the pass transistors that otherwise would increase on-state resistance. So, there is a trade-off between $C_{io(off)}$ and r_{on}.

4.4 $C_{io(on)}$

This is the on-state capacitance of the switch, measured from either the input or output of the switch. Usually $C_{io(on)}$ is greater than twice the $C_{io(off)}$ because it includes the capacitance on both input and output of the switch, as well as the channel capacitance. Like $C_{io(off)}$, $C_{io(on)}$ should be as small as possible to reduce capacitive loading of the bus. Reducing $C_{io(on)}$ requires less drain and source area of the pass transistors that otherwise would increase the on-state resistance. So, like the $C_{io(off)}$, there is a trade-off between $C_{io(on)}$ and r_{on}.

4.5 C_i (Control Input Capacitance)

When switching control input, a large control input capacitance will inject more charge to the gate of the pass transistor. This will cause crosstalk and degrade performance of the switch.

4.6 Leakage Current

Leakage current during the high-impedance state should be very small. Leakage current, if high, may load an isolated bus and corrupt the data.

4.7 Enable and Disable Delays

Enable and disable delays are measures of how quickly the switch can be turned on and off. Not only should these delays be as small as possible for high-speed operation, but also the difference of enable and disable delays should be as small as possible to reduce the current flow between the off switch and on switch. This is significant in multiplexing and demultiplexing operations where the difference, if large, can cause bus contention. For break-before-make functions, disable time should be less than enable time and for make-before-break functions, enable time should be less than disable time.

4.8 Partial Power Down

Today’s high-speed applications require that a device can be powered-down while still connected to a live bus. This requires the switch to be in the high-impedance state while the power is down. A special I_{off} circuit is incorporated to ensure that the switch is in the high-impedance state while the power is off. I_{off} circuitry prevents damaging current backflow through the device when it is powered down.

4.9 Voltage Translation

One popular application of the bus switch is voltage translation in a mixed-voltage environment. A simple NMOS can pass a signal from 0 V to $V_{CC} – V_T$, where V_T is the threshold voltage of the NMOS. This characteristic can be used for down translation. Figure 10 shows an example of 5-V to 3.3-V translation using an NMOS series switch, diode, and resistors.

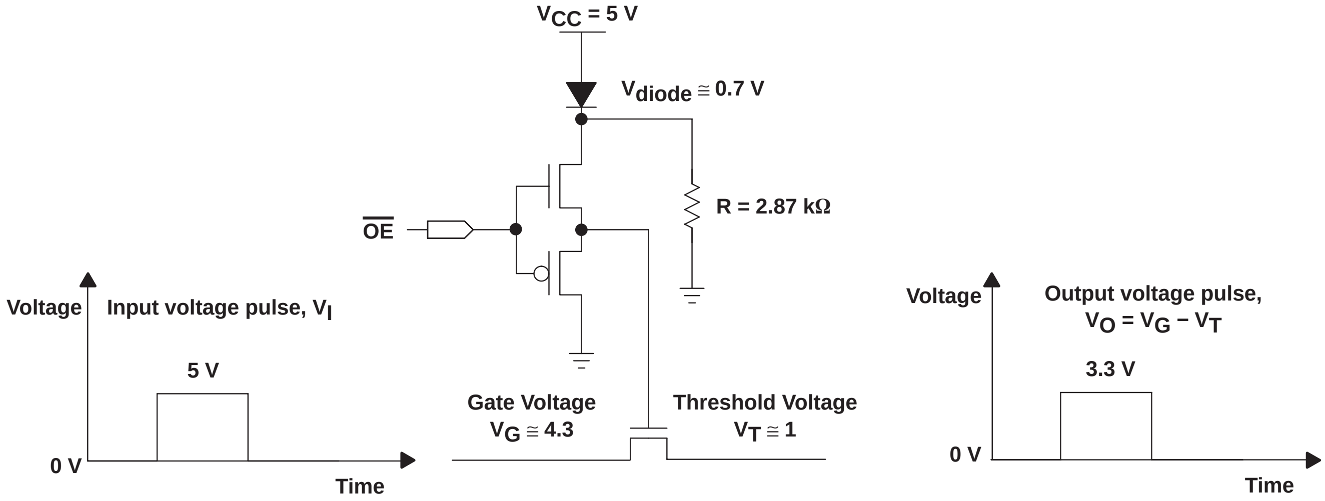


Figure 10. Voltage Translation Using an NMOS Series Switch

For voltage-translation applications, the switch is required to translate efficiently over a wide frequency range and is required to maintain the proper signal level. For example, when translating from a 5-V TTL to a 3.3-V LVTTL signal, the switch is required to maintain the required V_{OH} (output high voltage) and V_{OL} (output low voltage) of 3.3-V LVTTL signal. One important consideration is that the bus switch can be used only for down translation, i.e., high to low level. For low- to high-level translation, additional components (for example, pullup resistors) are required.

5 Signal Switch Families from TI

TI offers a wide variety of signal switches suitable for many different types of applications. Some of the signal-switch families are discussed in the following sections:

- CBT-C: 5-V NMOS switches with –2-V undershoot protection
- CB3Q: NMOS switches with a charge-pump circuit for low and flat r_{on}
- CB3T: Level-shifting NMOS bus switch

CBT-C and CB3Q devices can pass digital and analog signals.

5.1 CBT-C Family

The switches of this family are NMOS series switches. The operating V_{CC} of this family is 5 V, and switching for various standards (i.e., LVCMOS, LVTTL etc.) can be accomplished. This family also has an undershoot protection circuit integrated in the bus switch. The undershoot protection circuit prevents the n-channel pass transistor from turning on when the switch is off. When undershoot occurs, this circuit senses the negative voltage at the input and biases the gate of the n-channel pass transistor to that negative voltage. Since the gate and source voltage are now at the same potential (<0 V), the switch remains off. Undershoot protection on one side of the off switch can prevent up to –2 V undershoots on the other side of the switch. Static power consumption of this family is negligible. Dynamic power consumption depends on the frequency of the enable input of the device. Switching high and low at the enable input causes internal CMOS inverters to switch between low and high; therefore, a higher frequency of the control input signal results in higher dynamic power consumption. Undershoot protection in CBT-C is shown in Figure 11.

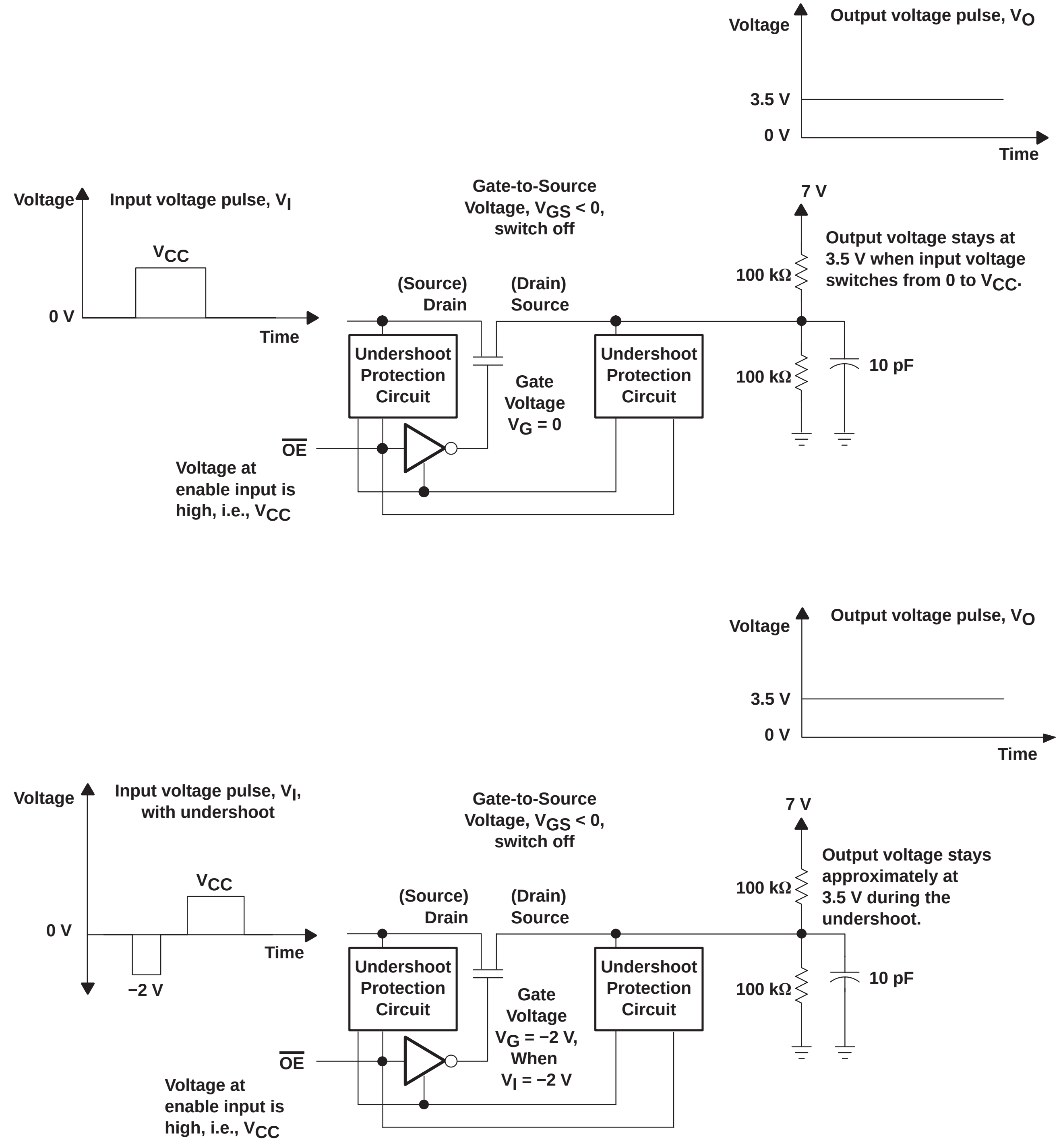

Voltage
Output voltage pulse, V$_O$
3.5 V
0 V
Time
Voltage
Input voltage pulse, V$_I$
V$_{CC}$
0 V
Time
Gate-to-Source Voltage, V$_{GS}$ < 0, switch off
(Source) Drain
(Drain) Source
7 V
100 kΩ
Output voltage stays at 3.5 V when input voltage switches from 0 to V$_{CC}$.
Undershoot Protection Circuit
Gate Voltage V$_G$ = 0
Undershoot Protection Circuit
100 kΩ
10 pF
OE
Voltage at enable input is high, i.e., V$_{CC}$
Voltage
Output voltage pulse, V$_O$
3.5 V
0 V
Time
Voltage
Input voltage pulse, V$_I$, with undershoot
V$_{CC}$
0 V
Time
−2 V
Gate-to-Source Voltage, V$_{GS}$ < 0, switch off
(Source) Drain
(Drain) Source
7 V
100 kΩ
Output voltage stays approximately at 3.5 V during the undershoot.
Undershoot Protection Circuit
Gate Voltage V$_G$ = −2 V, When V$_I$ = −2 V
Undershoot Protection Circuit
100 kΩ
10 pF
OE
Voltage at enable input is high, i.e., V$_{CC}$

Figure 11. Undershoot Protection in CBT-C When Enable Input ($\overline{OE}$) Voltage is High

5.1.1 Characteristics of the CBT-C Family

The following paragraphs discuss some of the critical performance characteristics of the CBT16211C. The setup for measurements is given in Appendix A.

5.1.1.1 V_O vs V_I

Figure 12 shows the output-voltage vs input-voltage characteristics of the CBT16211C at an output load of 3 kΩ to ground. The output follows the input approximately until 3.5 V and remains flat as the switch begins to turn off. Output voltage also depends on the output current. If output current increases, the output voltage will become flat at a lower input voltage.

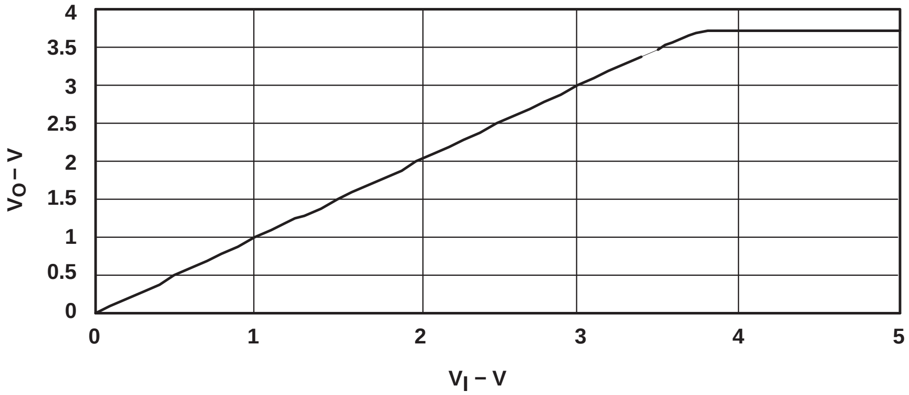


Figure 12. V_O vs V_I at V_{CC} = 5 V

5.1.1.2 r_{on} vs V_I

Figure 13 shows the switch resistance (r_{on}) when on, as a function of the input voltage. The output current is –15 mA. The on-state resistance is low when the input voltage is below 3.5 V and increases rapidly above 3.5 V. r_{on} depends on the output current and increases rapidly at a lower input voltage when the output current increases.

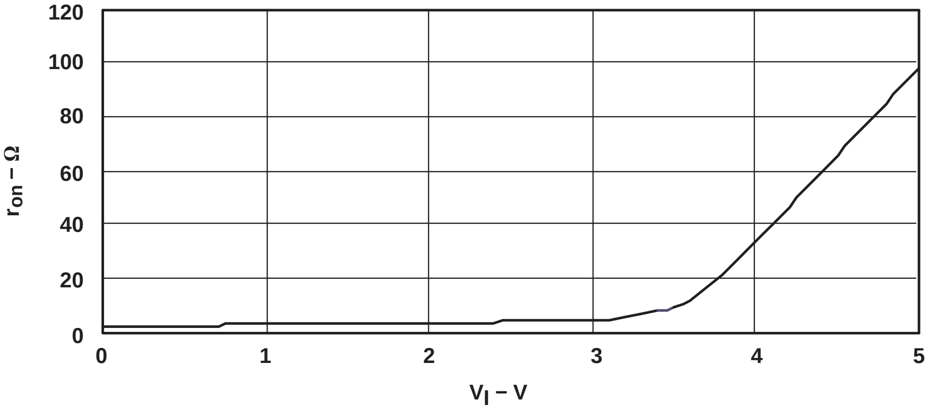


Figure 13. r_{on} vs V_I at V_{CC} = 5 V (I_O = –15 mA)

5.1.1.3 Undershoot Protection

Figure 14 shows the undershoot protection performance of the CBT16211C when the switch is disabled. The output pin is connected to ground through a 100-kΩ resistor, a 10-pF capacitor, and to 10 V through a 100-kΩ pullup resistor. The test load is similar to a high-impedance application load. There is very little variation in output voltage caused by input-voltage undershoot.

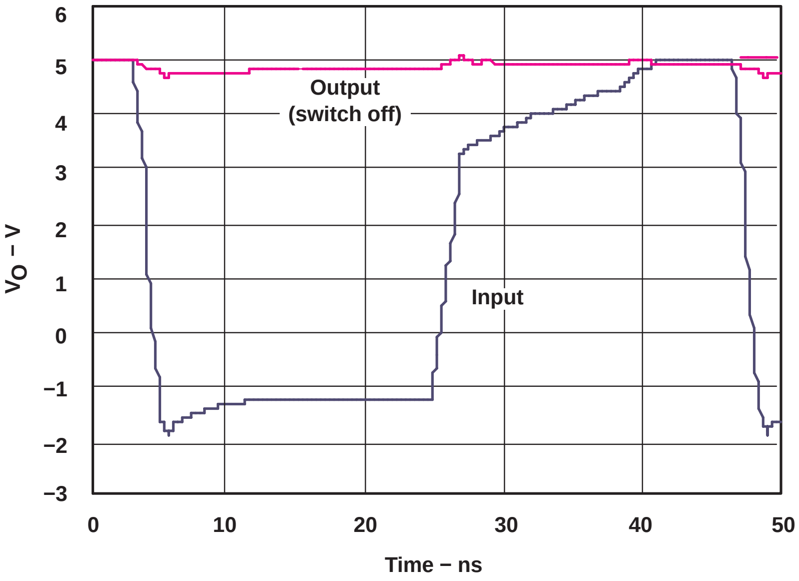


Figure 14. Undershoot in CBT16211C When Switch Is Off (V_{CC} = 5 V)

5.1.2 Application of CBT-C Family

5.1.2.1 Bus Isolation

CBT-C devices can be used for 5-V PCI bus isolation for hot-plug applications (see Figure 15). PCI is an unterminated interface; therefore, undershoot may occur. CBT-C provides good isolation when an undershoot event occurs.

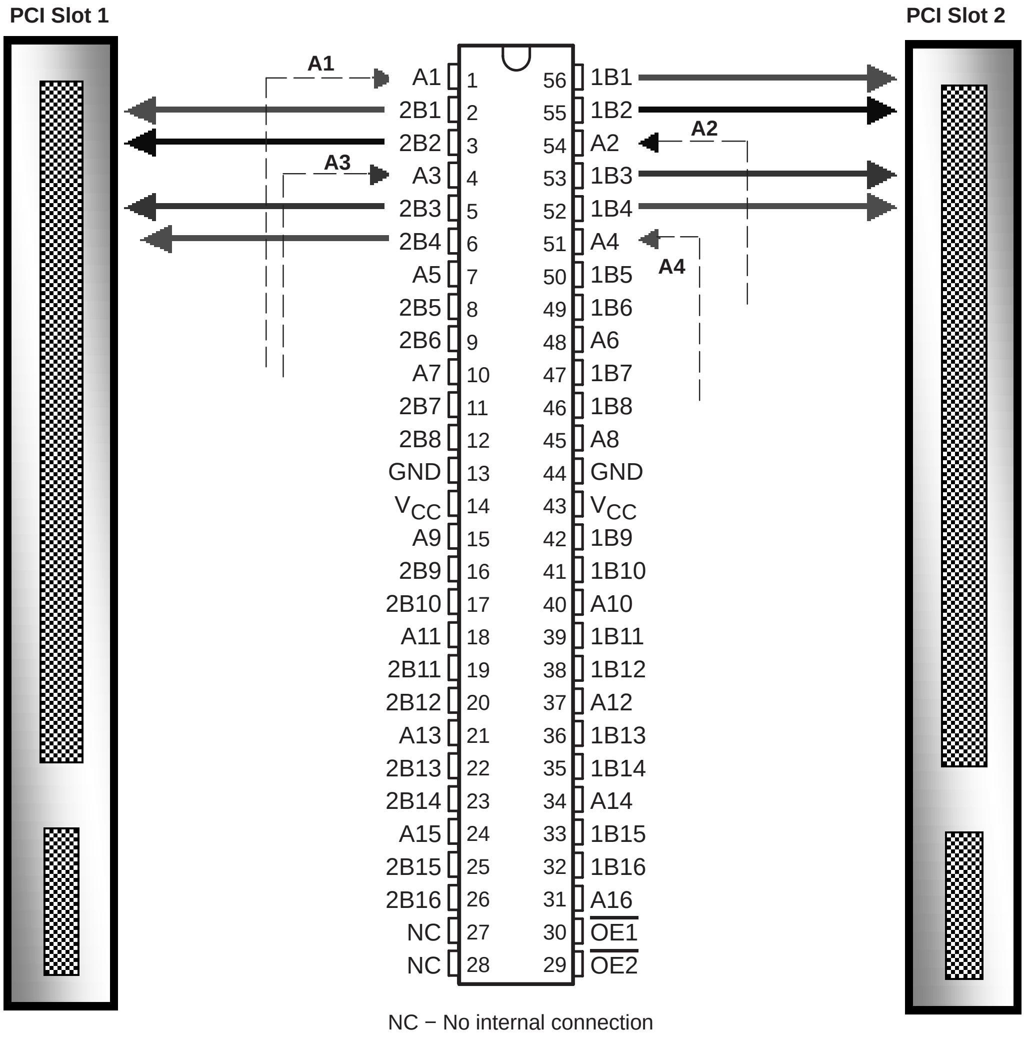

PCI Slot 1
PCI Slot 2
A1
A2
A3
A4
A1 1
2B1 2
2B2 3
A3 4
2B3 5
2B4 6
A5 7
2B5 8
2B6 9
A7 10
2B7 11
2B8 12
GND 13
V_{CC} 14
A9 15
2B9 16
2B10 17
A11 18
2B11 19
2B12 20
A13 21
2B13 22
2B14 23
A15 24
2B15 25
2B16 26
NC 27
NC 28
56 1B1
55 1B2
54 A2
53 1B3
52 1B4
51 A4
50 1B5
49 1B6
48 A6
47 1B7
46 1B8
45 A8
44 GND
43 V_{CC}
42 1B9
41 1B10
40 A10
39 1B11
38 1B12
37 A12
36 1B13
35 1B14
34 A14
33 1B15
32 1B16
31 A16
30 $\overline{OE1}$
29 $\overline{OE2}$
NC − No internal connection

Figure 15. Example of Bus Isolation Using a CBT-C Device

5.2 CB3Q Family

The switches of this family are NMOS only, with a low and flat r_{on}. The flat characteristics of r_{on} are accomplished by a charge-pump circuit that generates a voltage of approximately 7 V at the gate of the n-channel pass transistor. As a result, 0-V to 5-V rail-to-rail switching can be accomplished because the gate-to-source voltage is well above the threshold of the n-channel transistor, and the switch is completely on over the whole 0-V to 5-V range. An internal oscillator circuit is a part of the charge-pump circuit; therefore, static power consumption of this family is higher than the CBT-C family. Dynamic power consumption depends on the frequency of the enable input. In addition to the low and flat r_{on} characteristics, this family has low input and output capacitance, making them suitable for high-performance applications. The maximum switching frequency for I/O signals depends on various factors, such as type of load, input-signal magnitude, input-signal edge rates, type of package, etc. With a larger package, the inductance and capacitance can form a resonant circuit that may cause phase and magnitude distortion. With a large capacitive load, the RC time constant becomes higher and limits the frequency. Figure 16 shows a simplified schematic of a CB3Q device.

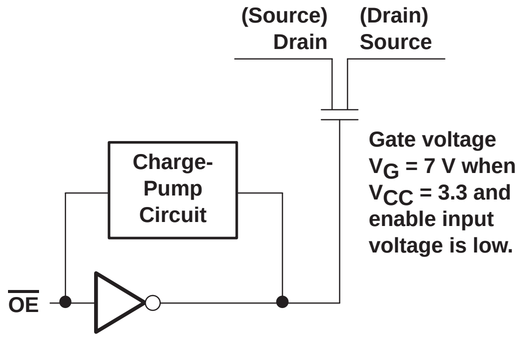


Figure 16. Simplified Schematic of a CB3Q Device

5.2.1 Characteristics of the CB3Q Family

Following sections discuss some of the critical performance characteristics of the CB3Q3306A. The measurements setup can be found in Appendix A.

5.2.1.1 V_O vs V_I

Figures 17 and 18 show the V_O vs V_I characteristics of the CB3Q3306A at different values of V_{CC} and at different temperatures. For V_{CC} = 3.6 V, the output exactly follows the input from 0 V to 5 V. Because of this characteristic, CB3Q devices can be used for switching analog and digital signals, ranging from 0 V to 5 V. For V_{CC} = 2.3 V, the gate voltage produced by the charge-pump circuit is reduced to about 4 V. So, the output approximately follows the input from 0 V to 3.3 V and becomes constant above 3.3 V.

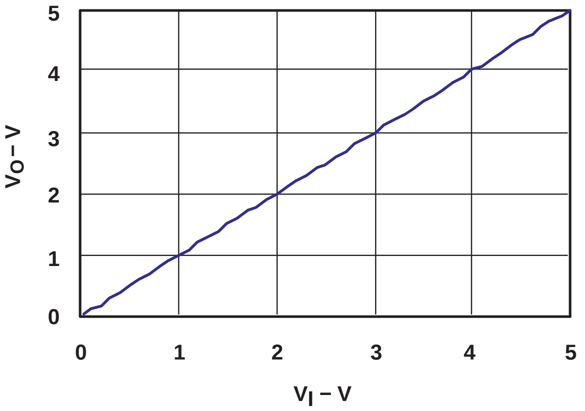


Figure 17. V_O vs V_I for the CB3Q3306A at V_{CC} = 3.6 V, T_A = 85°C

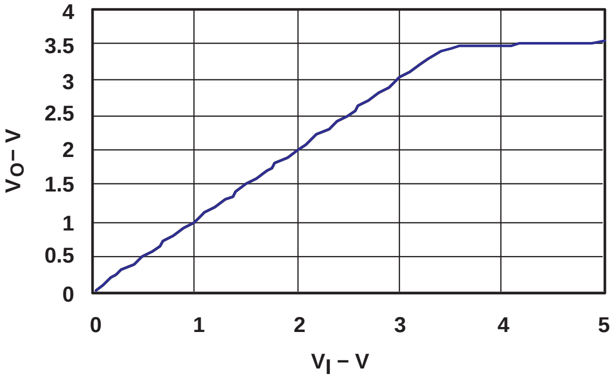


Figure 18. V_O vs V_I for the CB3Q3306A at V_{CC} = 2.3 V, T_A = 85°C

5.2.1.2 r_{on} vs V_I

The CB3Q3306A has low and flat r_{on} characteristics. Figure 19 and Figure 20 show r_{on} vs input voltage characteristics at different values of V_{CC} and at different temperatures. The output current for r_{on} vs V_I characteristics is –15 mA, and this characteristic is dependent on output current. For V_{CC} = 3.6 V, r_{on} is fairly constant from the 0-V to 5-V input-voltage range. For V_{CC} = 2.3 V, r_{on} is flat over the range of 0 V to 2.5 V and increases rapidly above 2.5 V.

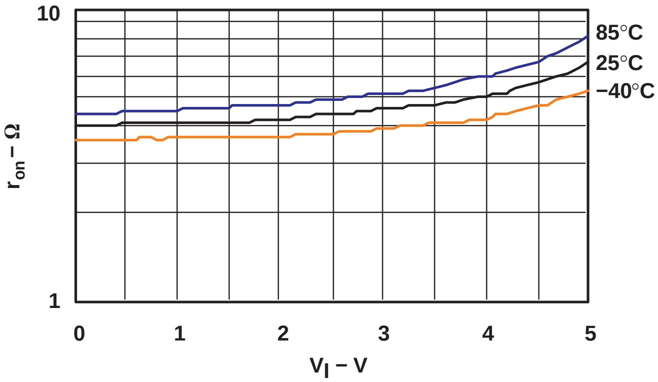


Figure 19. r_{on} vs V_I for the CB3Q3306A at V_{CC} = 3.6 V (I_O = –15 mA)

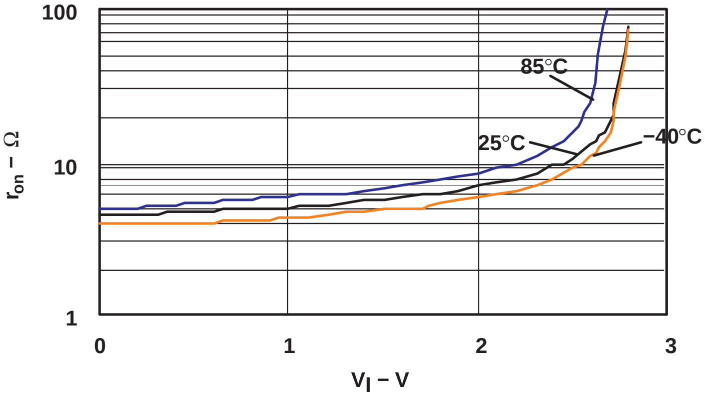


Figure 20. r_{on} vs V_I for the CB3Q3306A at V_{CC} = 2.3 V (I_O = −15 mA)

5.2.1.3 Operation at High Frequency

Low input and output capacitance, low r_{on}, and low feed-through capacitance makes the CB3Q devices suitable for high-speed applications. Maximum frequency of operation depends on input voltage range, type of load, edge rate, type of package, off-isolation, crosstalk requirement, etc. At high frequencies, off-isolation and crosstalk also increase, which limits the maximum frequency of operation. Figure 21 shows the input and output voltage waveforms at a frequency of 420 MHz, with a 500-Ω and 3-pF load. From Figure 21, it is clear that the switch, when on, allows high-frequency signals to pass without distortion. Also, the switch provides very good isolation between the input and output when it is turned off or disabled.

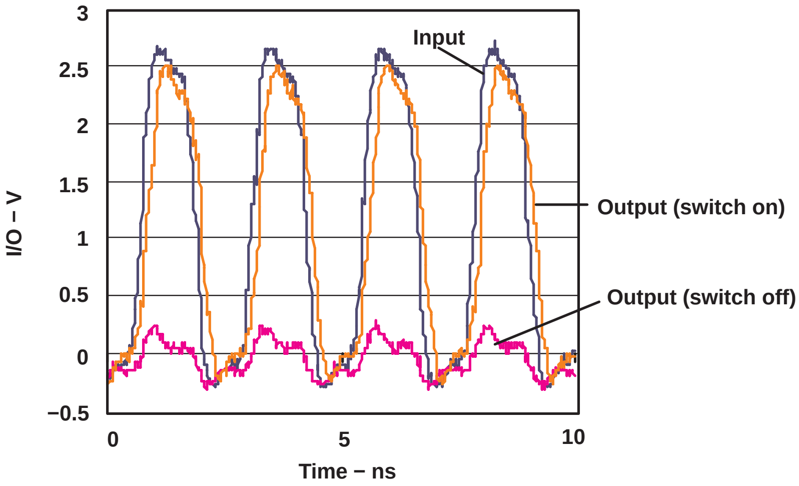


Figure 21. Input and Output Voltage Waveforms for the CB3Q3306A at 420 MHz (V_{CC} = 3.3 V)

5.2.1.4 Output Skew

Output skew is a measure of the variation of r_{on} over the channels in a multibit switch. This is specifically significant when switching differential signals. For minimal signal distortion and noise in differential signaling, the variation of r_{on} should be as small as possible. Output skew at a specific voltage can be determined by measuring the time difference of the output voltage at various channels. Figure 22 and Figure 23 show the output voltage of the CB3Q3306A at different channels. Output skew can be determined from this graph. For example, for –40°C at 2.5 V, the skew is approximately 30 ps, which is fairly constant from 2.2 V to 2.6 V. For 100°C, the output skew is approximately 40 ps, which is fairly constant from 2.2 V to 2.6 V.

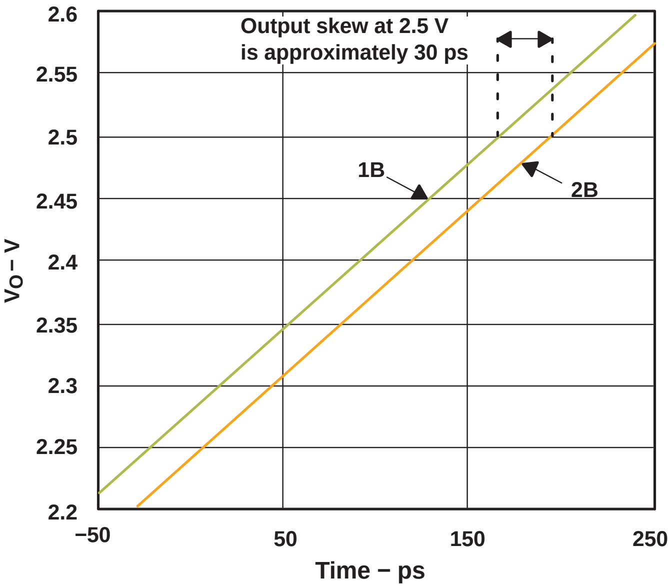


Figure 22. Output Skew at –40°C (V_{CC} = 3.3 V)

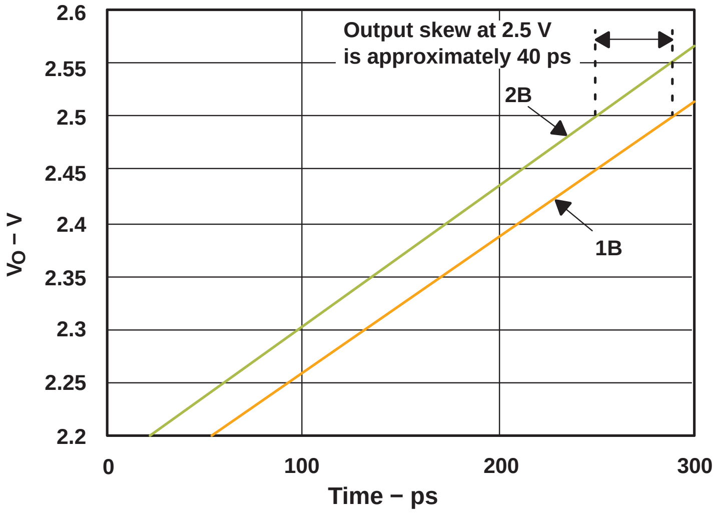


Figure 23. Output Skew at 100°C (V_{CC} = 3.3 V)

5.2.1.5 Frequency Response

Figure 24 and Figure 25 show the attenuation and off-isolation for the CB3Q3306A at different loads as a function of frequency. The bandwidth depends on the type of load, and bandwidth decreases as the load increases.

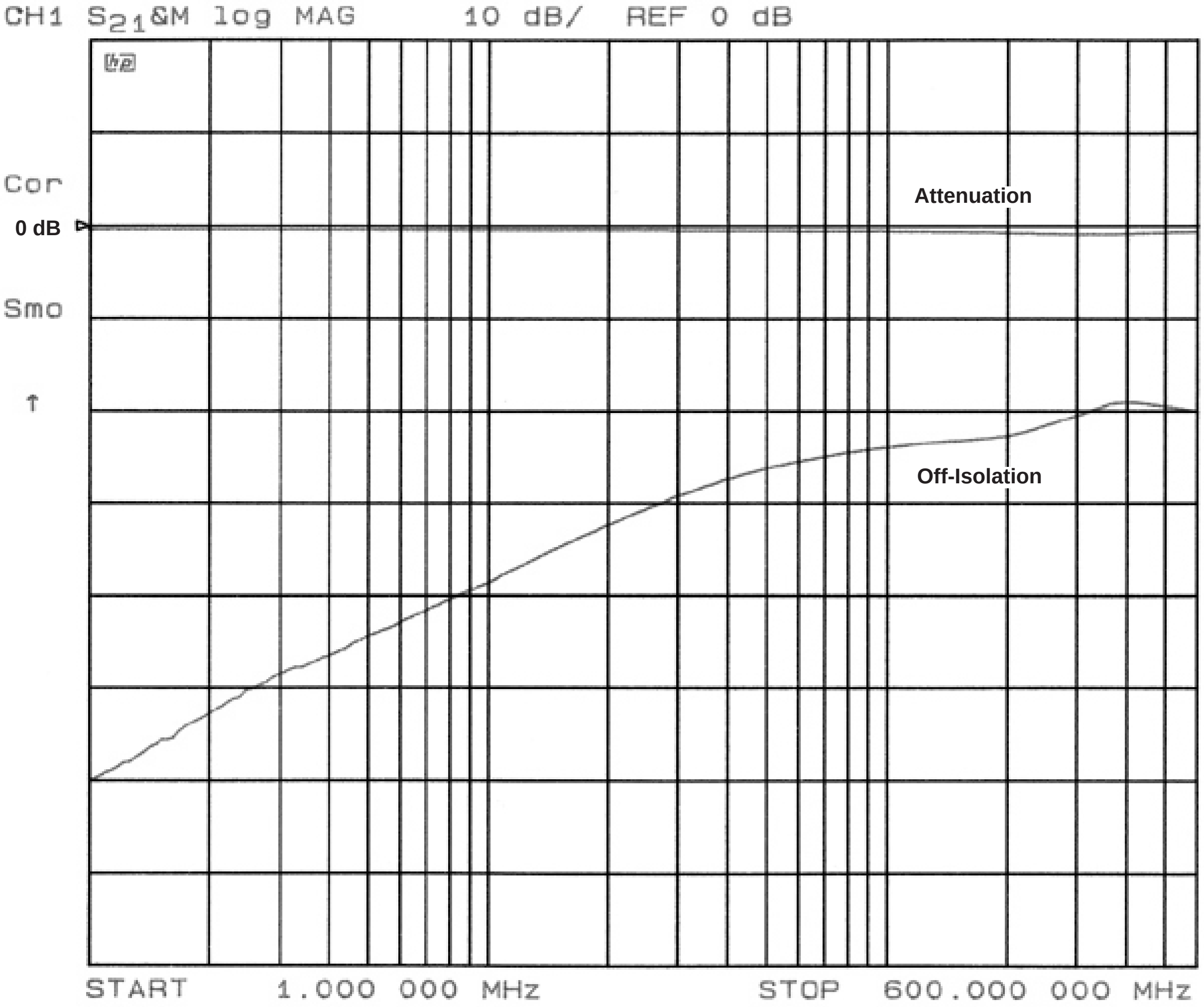


Figure 24. Attenuation and Off-Isolation for the CB3Q3306A at 3-pF Load (V_{CC} = 3.3 V)

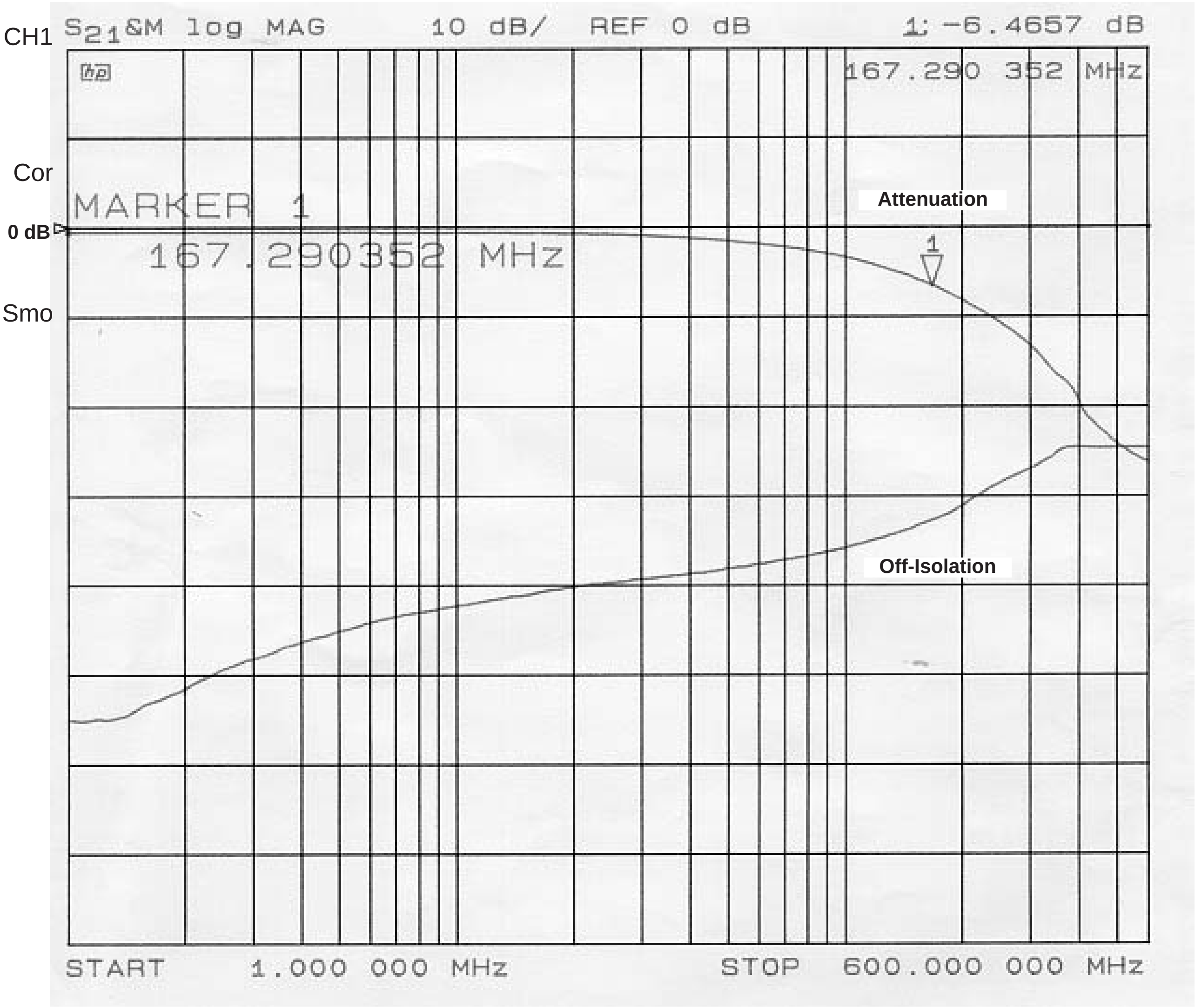


Figure 25. Attenuation and Off-Isolation for the CB3Q3306A at 50-pF Load (V_{CC} = 3.3 V)

5.2.1.6 Adjacent Channel Crosstalk

For some applications, crosstalk is an important parameter. Figure 26 shows the crosstalk between adjacent channels in the CB3Q3306A.

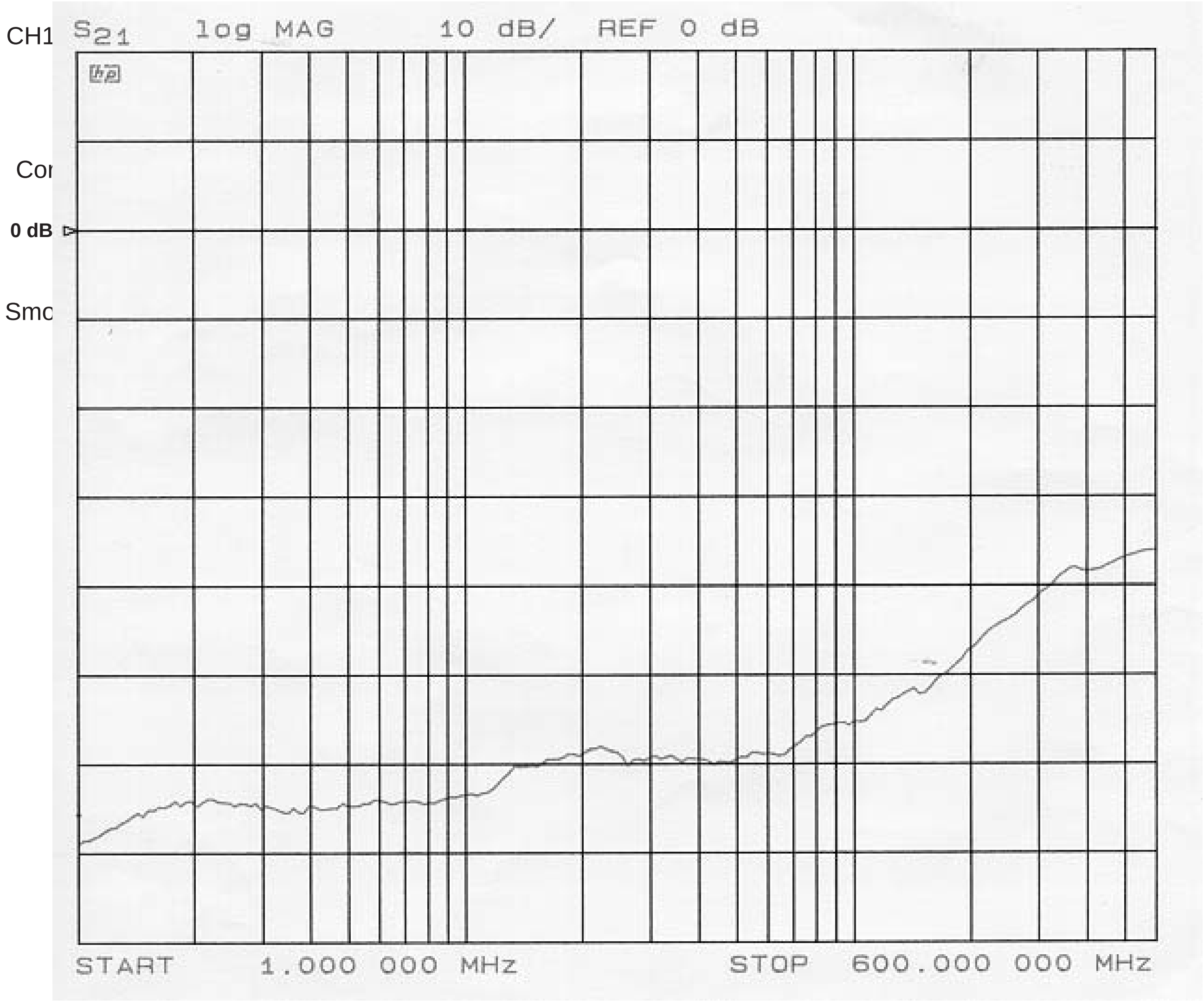


Figure 26. Crosstalk of the CB3Q3306A at 3-pF Load (V_{CC} = 3.3 V)

5.2.2 Application of the CB3Q Family

5.2.2.1 Multiplexer in USB Applications

Figure 27 shows a USB 2.0 application in which a bus-switch device can be used. The first switch in a notebook PC is used to isolate between a notebook PC and the docking station. The switches on the docking station are used as a mutiplexer to provide two different paths for the DATA+ and DATA– signals. If the operating system is Windows 95, the USB 2.0 hub is not supported. Switches 1 and 2 are on, and the USB line is connected directly to Port 1. Figure 28 shows the use of a CB3Q3257 in this type of application.

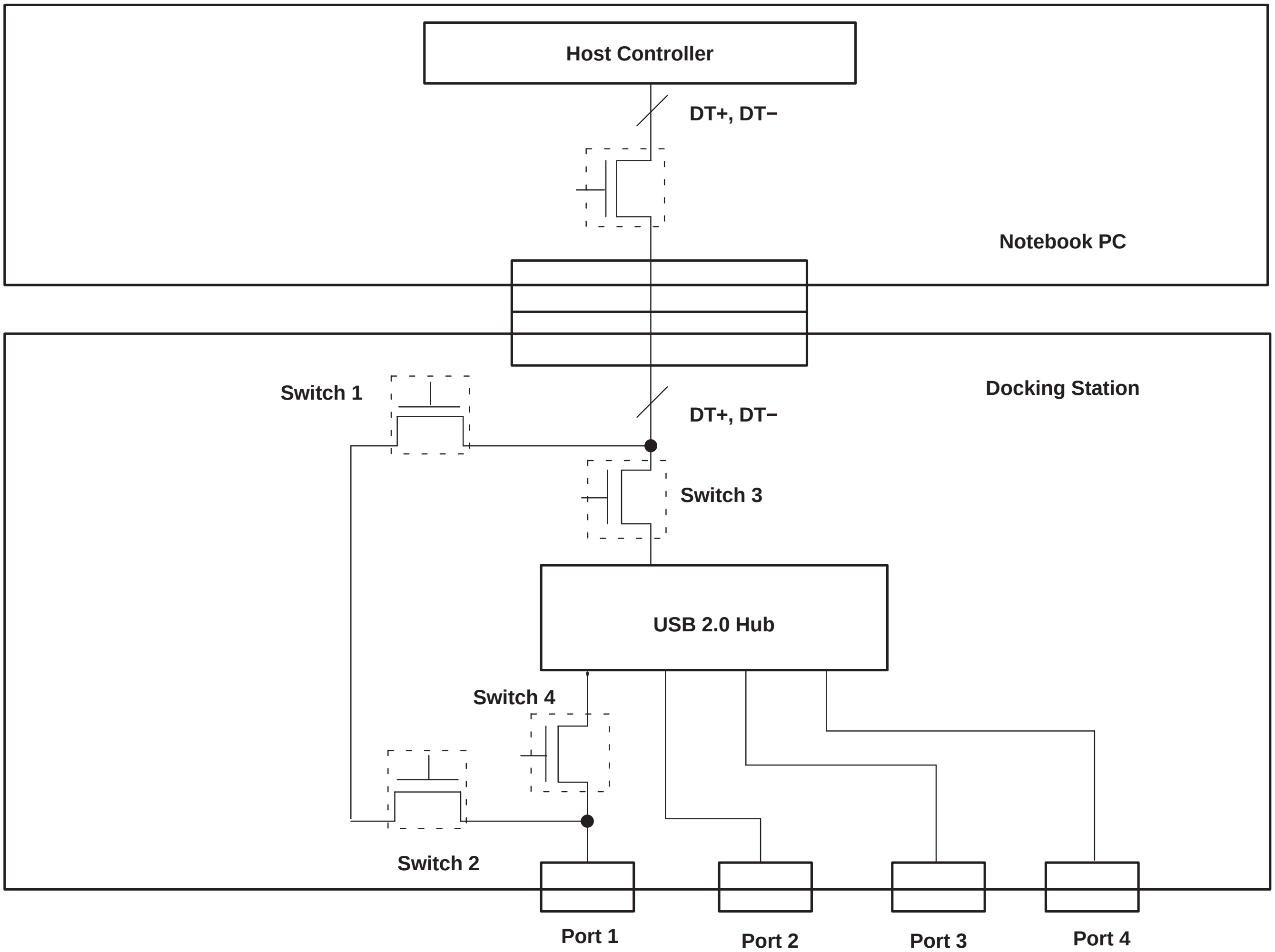
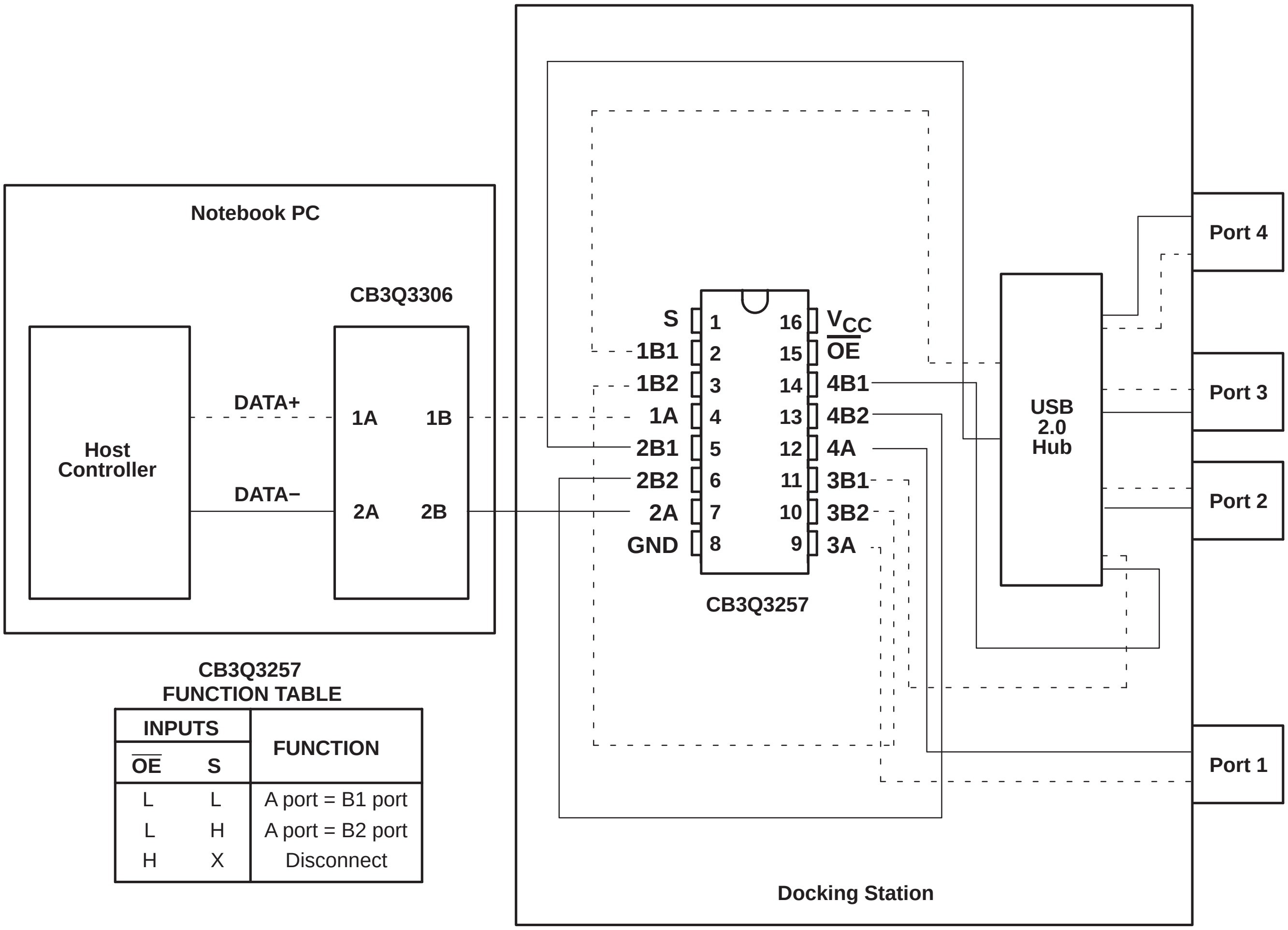

Host Controller
DT+, DT−
Notebook PC
Docking Station
Switch 1
DT+, DT−
Switch 3
USB 2.0 Hub
Switch 4
Switch 2
Port 1
Port 2
Port 3
Port 4

Figure 27. Multiplexing in a USB Application


Notebook PC
Host Controller
CB3Q3306
DATA+
DATA−
1A
1B
2A
2B
S
1B1
1B2
1A
2B1
2B2
2A
GND
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
V_{CC}
$\overline{OE}$
4B1
4B2
4A
3B1
3B2
3A
CB3Q3257
USB 2.0 Hub
Port 4
Port 3
Port 2
Port 1
Docking Station

CB3Q3257
FUNCTION TABLE

INPUTS		FUNCTION
$\overline{OE}$	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

Figure 28. CB3Q3257 in a USB Application

DATA+ signal path is shown as a dotted line and the DATA– signal is shown as a solid line. The DATA+ signal goes to 1A. Depending on the select signal (S) levels, the output can be 1B1 or 1B2. When S is low, DATA+ from the host controller is connected to the port through the USB 2.0 hub (1A → 1B1 → USB 2.0 Hub → 3B1 → 3A → Port 1). When S is high, the DATA+ is connected to port 1 directly (1A → 1B2 → 3B2 → 3A). Similarly, DATA– uses the 2A, 2B1, 2B2 and 4A, 4B1, 4B2 switches for connecting to port 1.

5.3 CB3T Family

CB3T is a voltage-translation bus-switch family. This family can operate with a power-supply voltage range of 2.3 V to 3.6 V. When V_{CC} = 3.3 V, the device can translate from a 5-V input to a 3.3-V output. In addition, when V_{CC} = 2.3 V the device can translate from 5-V or 3.3-V inputs to a 2.3-V output. The CB3T family can be used for voltage translation at moderately high frequencies. Figure 29 shows the simplified structure of the CB3T3306.

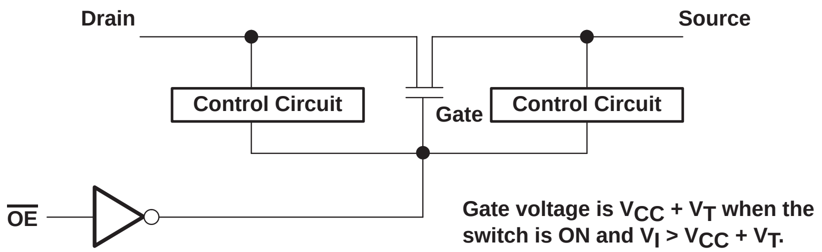

Drain
Source
Control Circuit
Gate
Control Circuit
$\overline{OE}$
Gate voltage is V_{CC} + V_T when the switch is ON and V_I > V_{CC} + V_T.

Figure 29. Simplified Structure of the CB3T3306

When the switch is on, the voltage at the gate of the NMOS pass transistor in the CB3T3306 is biased at $V_{CC} + V_T$, where V_T is the threshold voltage of the NMOS. When input voltage starts to rise from low to high, the output follows the input voltage. As the input voltage reaches about one-half of V_{CC}, the control circuit senses this voltage and pulls the output voltage close to the V_{CC} level and keeps the voltage constant as the input voltage increases. When the input reaches $V_{CC} + V_T$, the output voltage again increases to V_{CC} and remains nearly flat, as the input voltage continues to rise. Input voltages at which these transitions occur depend on the output current, power supply, temperature, and transistor characteristics. The level of output high voltage (V_{OH}) also depends on the output current.

5.3.1 Characteristics of the CB3T Family

The following paragraphs discuss some of the critical performance characteristics of the CB3T3306. The measurements setup is given in Appendix A.

5.3.1.1 V_O vs V_I

Figures 30 and 31 show the output voltage vs input voltage (V_O vs V_I) characteristics of the CB3T3306 for different values of V_{CC}. The rapid increase in output voltage is due to the control circuit sensing the output voltage and pulling it high, close to the V_{CC} level. The slope of this rapid rise in the curve depends on the output current being drawn from the switch.

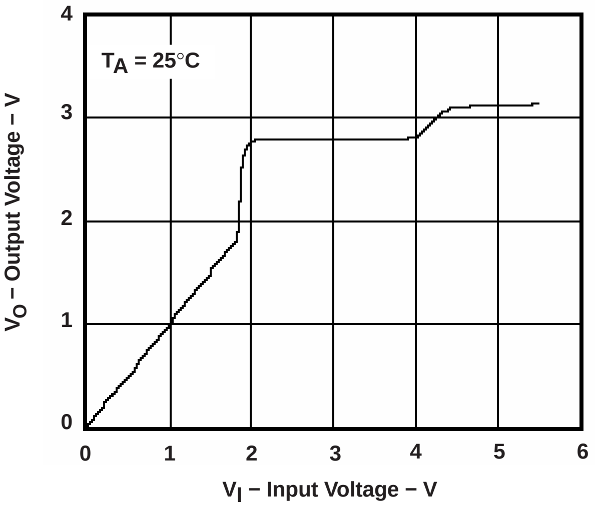


Figure 30. V_O vs V_I in the CB3T3306 at I_O = −1 µA (V_{CC} = 2.3 V)

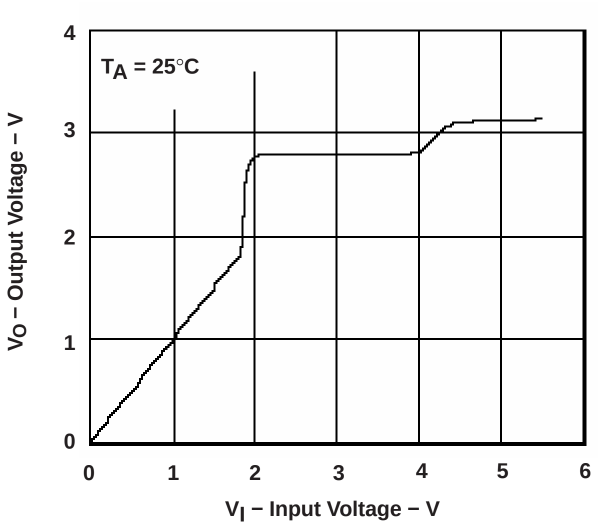


Figure 31. V_O vs V_I in the CB3T3306 I_O = –1 µA (V_{CC} = 3.0 V)

5.3.1.2 r_{on} vs V_I

Figure 32 and Figure 33 shows the r_{on} vs V_I characteristics of the CB3T3306 at different V_{CC} voltages. r_{on} increases rapidly when the input voltage crosses approximately one-half of V_{CC} and becomes flat above that voltage. The value of r_{on} above that voltage depends greatly on the output current. As the output current increases, r_{on} decreases.

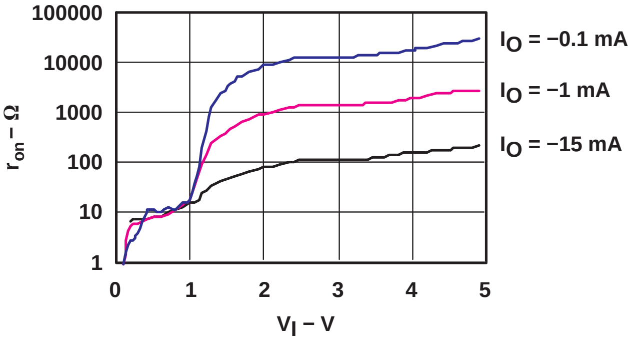


Figure 32. r_{on} vs V_I for the CB3T3306 at V_{CC} = 2.3 V

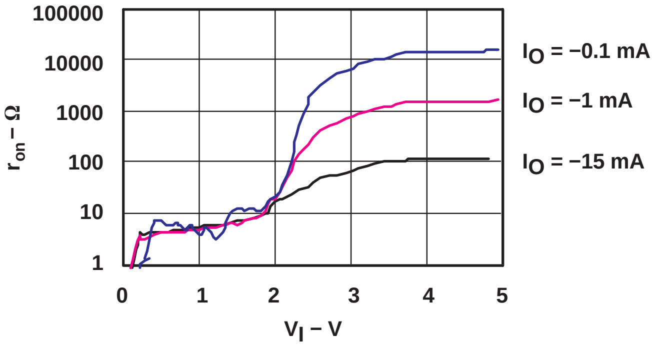


Figure 33. r_{on} vs V_I for the CB3T3306 at V_{CC} = 3.6 V

5.3.1.3 Operation at High Frequency

CB3T devices can be used for voltage translation at moderately high frequencies. Figure 34 shows the operation of the CB3T3306 at 200 MHz. The load is 500 Ω and 3 pF to ground. Like the CB3Q family, the maximum I/O switching frequency depends on various factors, such as type of load, input signal magnitude, input signal edge rates, type of package, etc. With a larger package, the inductance and capacitance can form a resonant circuit that may cause phase and magnitude distortion. With a large capacitive load, the RC time constant becomes higher and limits the practical operating frequency.

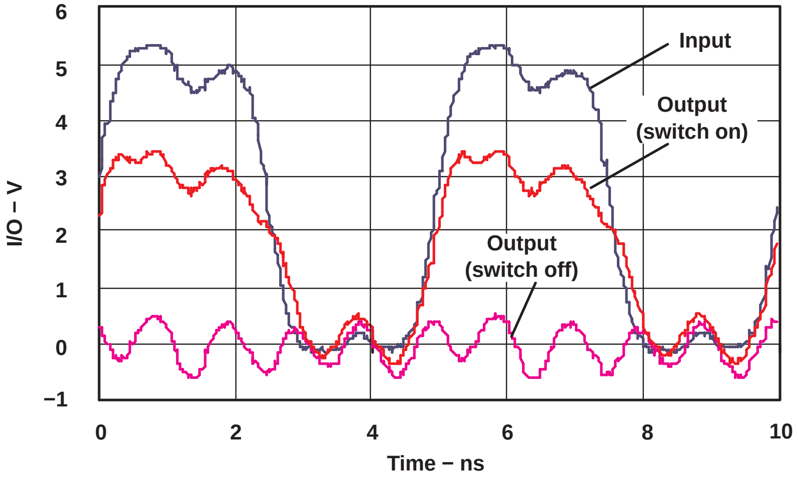


Figure 34. Input and Output Voltage Waveforms at 200 MHz (V_{CC} = 3.3 V)

5.3.2 Application of the CB3T Family

5.3.2.1 Voltage Translation for an External Monitor Terminal in a Notebook PC

Figure 35 shows a typical application for the level-translation feature of the CB3T3306. The CB3T3306 is used as a voltage translator between a monitor and a graphic controller. Data transfer between these two systems is bidirectional, while the clock signal transfer is unidirectional and flows only from graphic controller to monitor. Pullup resistors are used for translating from low to high.

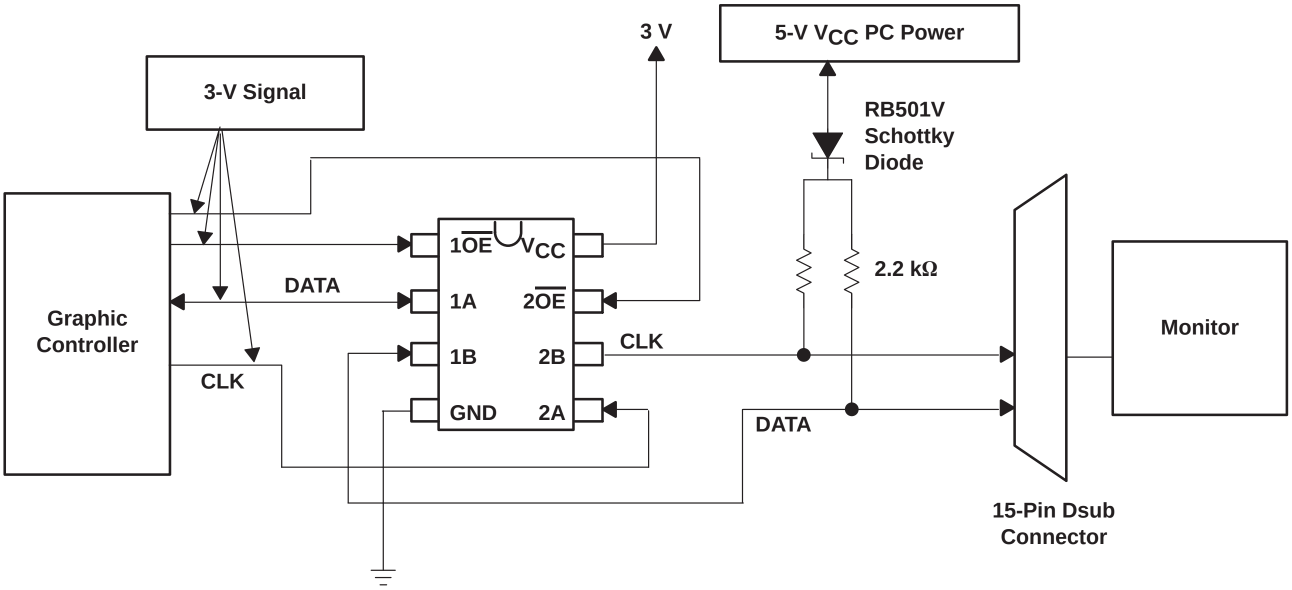

3 V
5-V VCC PC Power
3-V Signal
RB501V
Schottky
Diode
2.2 kΩ
Graphic
Controller
DATA
CLK
1OE
VCC
1A
2OE
1B
2B
GND
2A
CLK
DATA
Monitor
15-Pin Dsub
Connector

Figure 35. Data and Clock-Signal Data Transfer Using the CB3T3306

6 Conclusion

TI’s CBT-C and CB3Q signal switches can be used for various types of high-speed applications, such as hot insertion for PCI interface, LAN signaling, I^2C bus expansion, video switching, etc. CB3T devices can be used for high-speed voltage translation in a mixed-voltage system. This application report has discussed some of the application performance characteristics of TI’s high-speed signal switches that are critical for the previously mentioned applications.

7 References

13. *Selecting the Right Texas Instruments Signal Switch*, John Perry and Chris Cockrill
14. *5-V to 3.3-V Translation With the SN74CBTD3384*, Nalin Yogasundram
15. *Texas Instruments Solution for Undershoot Protection for Bus Switches*, Nadira Sultana and Chris Graves.

Appendix A Test Measurement Circuits

A.1 Measurement Setup for r_{on}

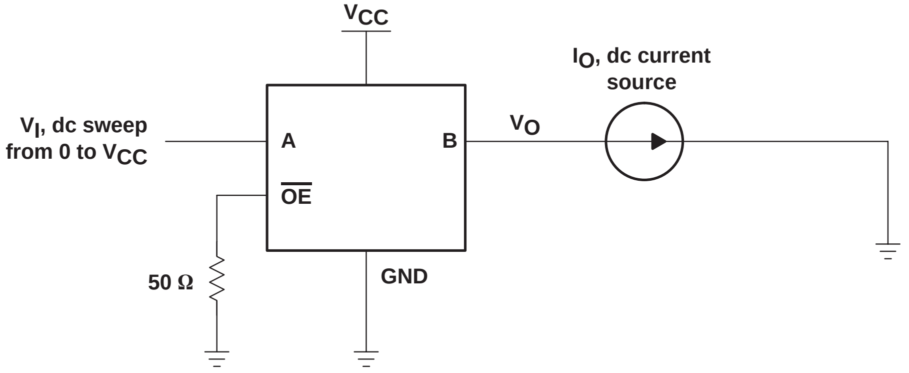

V_{CC}
I_O, dc current source
V_I, dc sweep from 0 to V_{CC}
A
B
$\overline{OE}$
V_O
50 Ω
GND

Figure A−1. r_{on} Measurement Setup

A.2 Measurement Setup for V_O vs V_I Characteristics

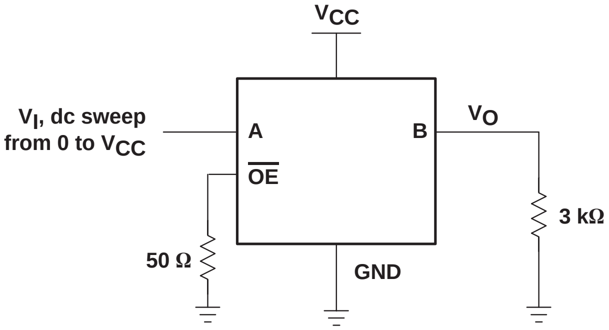

V_{CC}
V_I, dc sweep from 0 to V_{CC}
A
B
$\overline{OE}$
V_O
3 kΩ
50 Ω
GND

Figure A−2. V_O vs V_I Measurement Setup

A.3 Voltage-Time Waveform Measurement (Switch On)

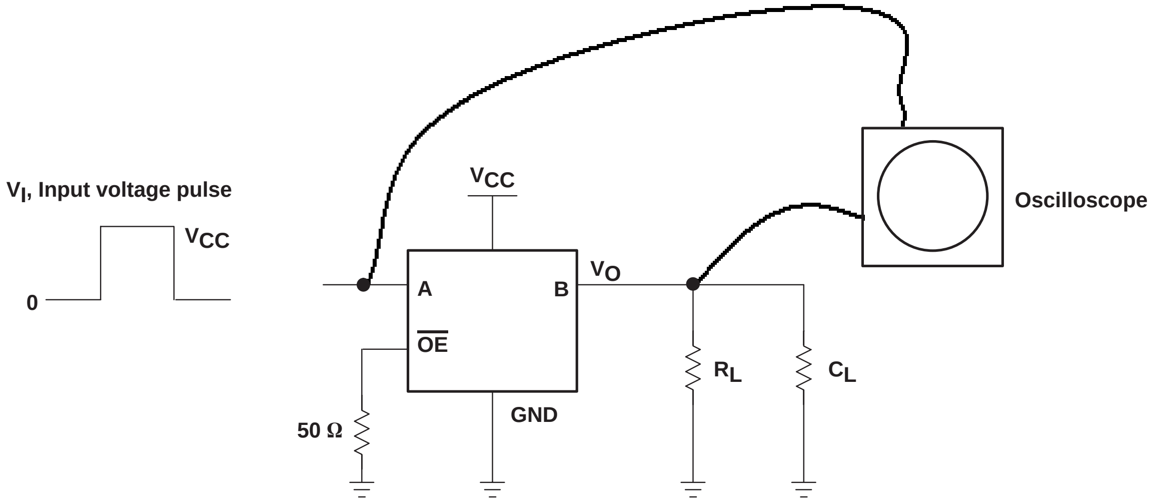

V_I, Input voltage pulse
V_{CC}
0
V_{CC}
A
B
$\overline{OE}$
GND
50 Ω
V_O
R_L
C_L
Oscilloscope

Figure A−3. Voltage-Time Waveform Measurement (Switch On)

A.4 Voltage-Time Waveform Measurement (Switch Off)

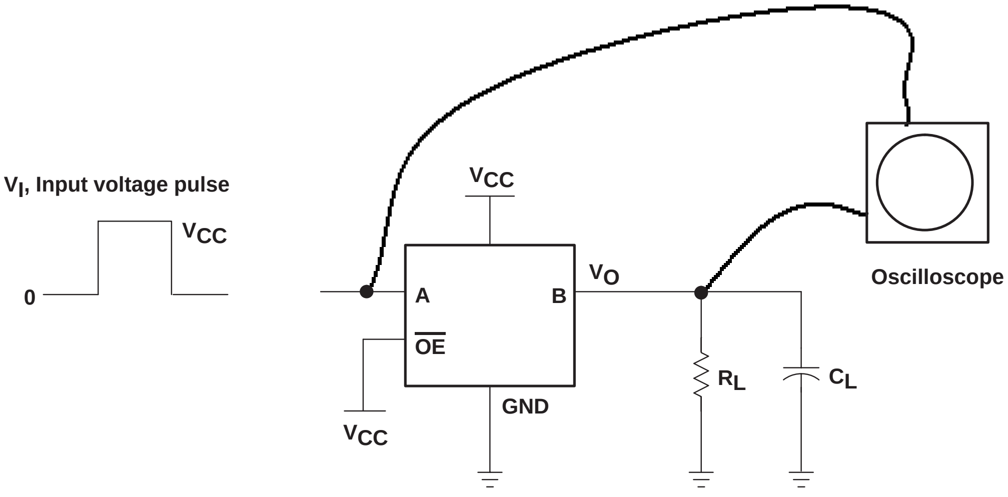

V_I, Input voltage pulse
V_{CC}
0
V_{CC}
A
B
$\overline{OE}$
GND
V_{CC}
V_O
R_L
C_L
Oscilloscope

Figure A−4. Voltage-Time Waveform Measurement (Switch Off)

A.5 Output-Skew Measurement

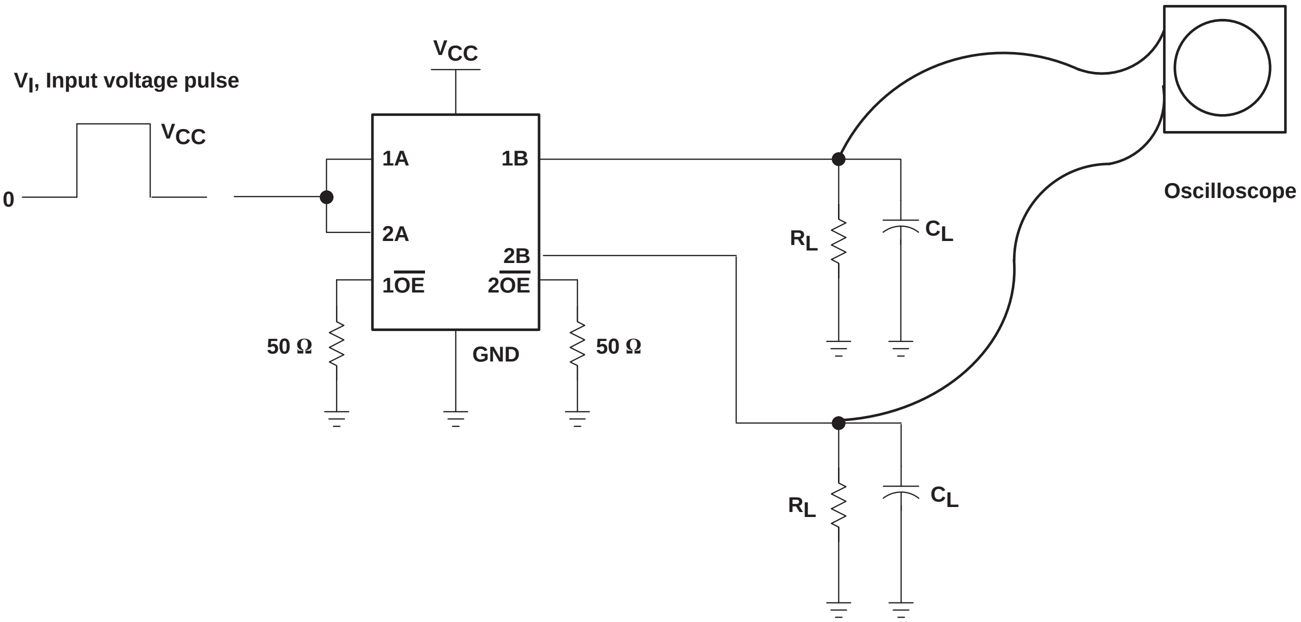

V_I, Input voltage pulse
V_{CC}
0
V_{CC}
1A
1B
2A
2B
1OE
2OE
50 Ω
GND
50 Ω
R_L
C_L
R_L
C_L
Oscilloscope

Figure A−5. Output-Skew Measurement Setup

A.6 Simulation Setup for Undershoot Measurement

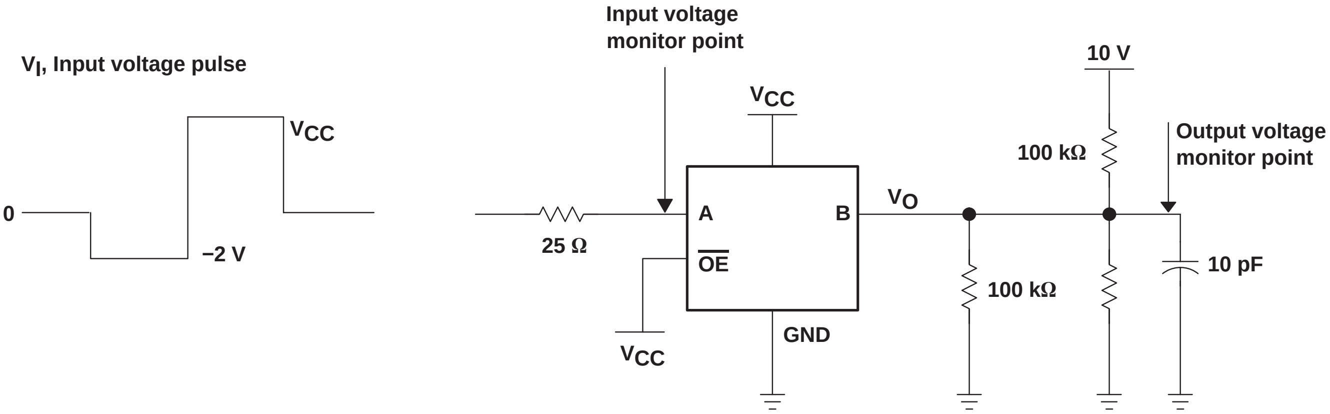

V_I, Input voltage pulse
V_{CC}
0
−2 V
Input voltage monitor point
V_{CC}
25 Ω
A
B
OE
V_{CC}
GND
V_O
10 V
100 kΩ
100 kΩ
Output voltage monitor point
10 pF

Figure A−6. SPICE Simulation Setup for Undershoot Measurement

A.7 Laboratory Setup for Attenuation Measurement

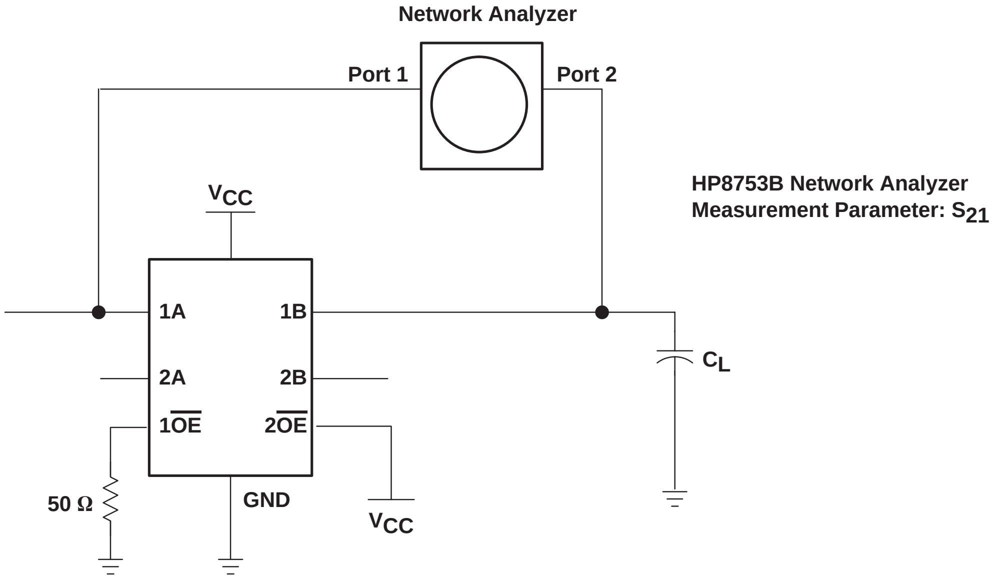

Network Analyzer
Port 1
Port 2
HP8753B Network Analyzer
Measurement Parameter: S_{21}
V_{CC}
1A
1B
2A
2B
$1\overline{OE}$
$2\overline{OE}$
C_L
50 Ω
GND
V_{CC}

Figure A−7. Attenuation Measurement Setup

A.8 Laboratory Setup for Off Isolation Measurement

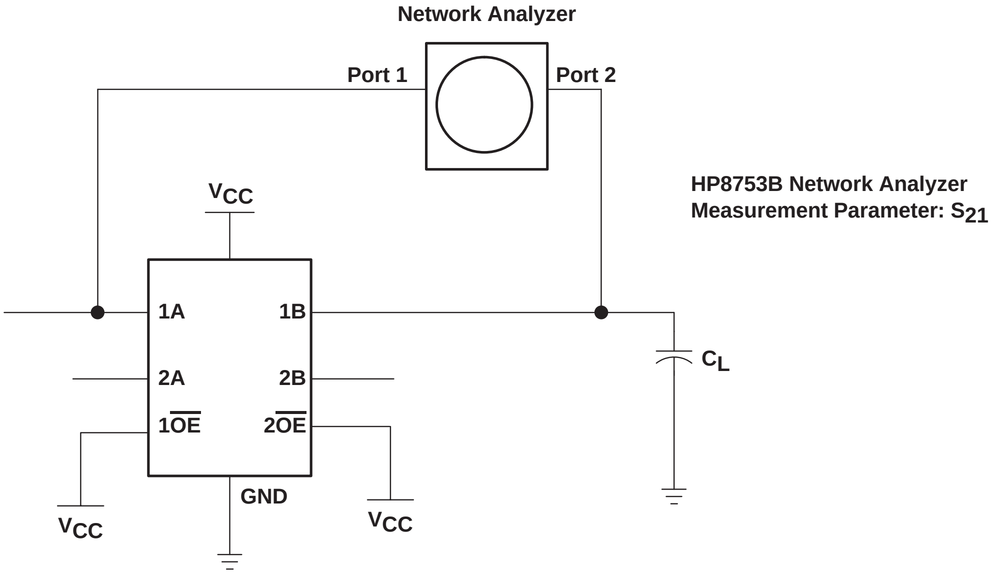

Network Analyzer
Port 1
Port 2
HP8753B Network Analyzer
Measurement Parameter: S_{21}
V_{CC}
1A
1B
2A
2B
$1\overline{OE}$
$2\overline{OE}$
C_L
GND
V_{CC}
V_{CC}

Figure A−8. Off Isolation Measurement Setup

A.9 Laboratory Setup for Crosstalk Measurement

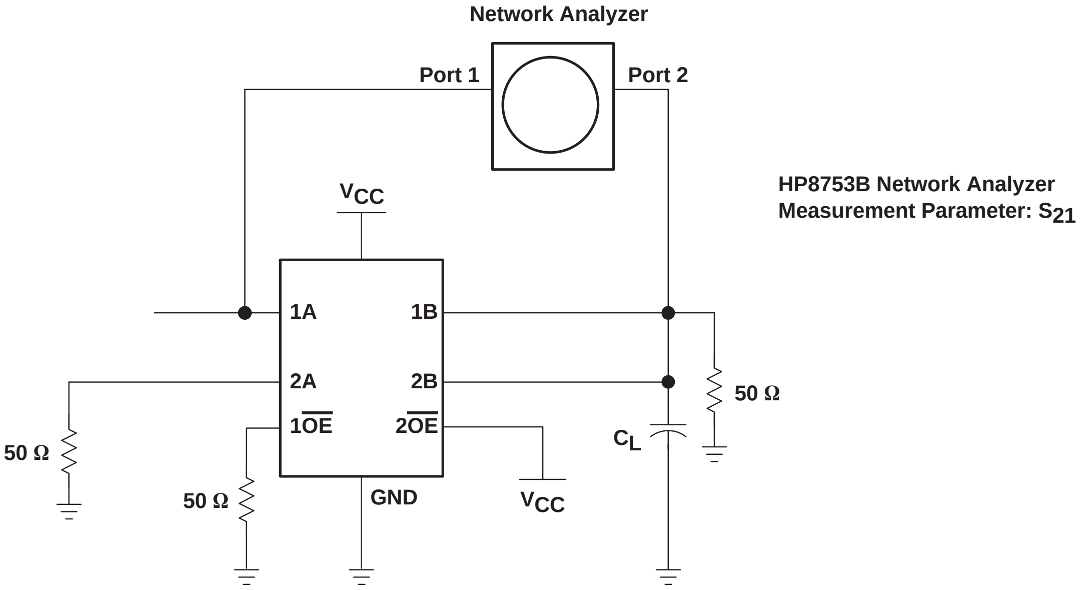

Network Analyzer
Port 1
Port 2
HP8753B Network Analyzer
Measurement Parameter: S_{21}
V_{CC}
1A
1B
2A
2B
$1\overline{OE}$
$2\overline{OE}$
50 Ω
50 Ω
50 Ω
C_L
GND
V_{CC}

Figure A−9. Adjacent-Channel Crosstalk Measurement

TEXAS INSTRUMENTS

Application Report
SZZA030 - October 2001

Selecting the Right Texas Instruments Signal Switch

John Perry and Chris Cockrill *Standard Linear & Logic*

ABSTRACT

Texas Instruments offers a wide variety of electronic switches (digital, analog, bilateral, bilateral analog) in a variety of families, including CBT, CBTLV, HC, LV, and LVC. Depending on the application, the right solution may be an analog switch that passes digital signals, or vice versa. This application report summarizes the various switching technologies and provides application considerations for choosing the appropriate TI signal switch.

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Trademarks are the property of their respective owners.

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47 r_{on} vs V_I, V_{CC} = 2.5 V (SN74CBTLV3125) . . . . 13−75
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1 Introduction

Texas Instruments offers a wide variety of signal switches in a variety of families, including CBT, CBTLV, CD4000, HC, LV-A, and LVC. These signal switches can be digital, analog, bilateral, or bilateral analog. Selecting the right one can be a formidable task. The purpose of this application report is to make the selection process easier by illustrating the differences between the families and removing ambiguity in the naming conventions.

2 Background

When first considering switches, a schematic of the ideal switch (similar to Figure 1) might come to mind.

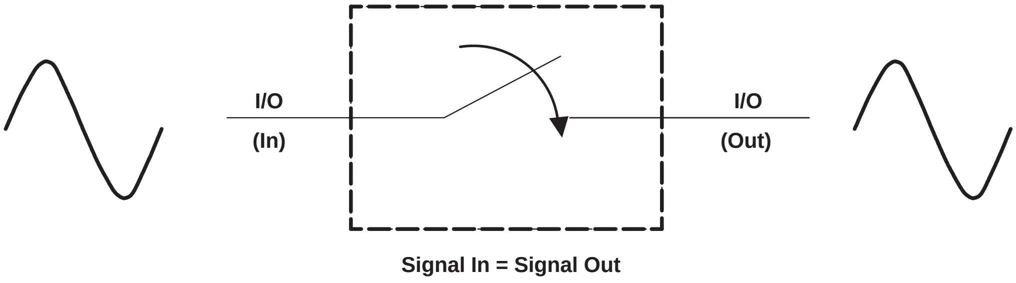


Figure 1. Ideal Switch

An input signal applied to the left I/O pin (or port) in Figure 1 results in an identical output signal at the right I/O pin, and vice versa. However, in the real world, switches are not ideal and there always is some loss. In the case of clean, properly working mechanical switches, the loss is so miniscule that it hardly bears noting.

Like mechanical switches, solid-state switches are not ideal either. In fact, losses associated with solid-state switches can be significant. Why use a switch like this if it is so far from ideal? The answer is convenience. Solid-state switches are small, fast, easy to use, easy to control, and consume relatively little power compared to traditional electrically controlled switches, such as relays. The switches referred to in this application report are complementary metal-oxide semiconductor (CMOS) field-effect transistor (FET) switches. As mentioned previously, they are not ideal, so we need a way to examine and compare the performance characteristics of the different CMOS families. Figure 2 shows a simplified-circuit model of a CMOS switch.

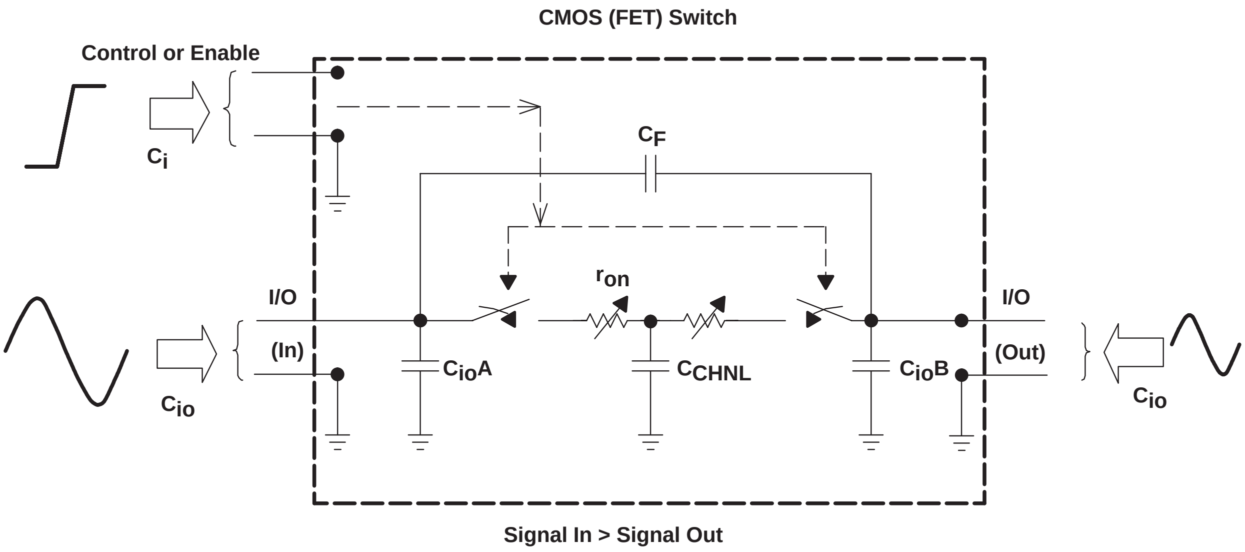


Figure 2. Simplified CMOS (FET) Switch

The output signal (right side, Figure 2) is altered due to parasitic effects of the switch. Results may include decreased amplitude, signal distortion, phase shift, the introduction of noise, and frequency attenuation.

Parameters contributing to the nonideal characteristics include:

- C_i – Control (enable) pin input capacitance
- C_F – Feedthrough capacitance
- C_{io} – Capacitance measured from either the input or output of the switch
- C_{CHNL} – NMOS (PMOS) channel capacitance
- r_{on} – On-state resistance from drain to source $r_{ds(on)}$ of the pass FET

As mentioned previously, TI offers a variety of CMOS-technology switches. Table 1 summarizes the families by switch type.

Table 1. TI Switch Technologies

TECHNOLOGY	ABBREVIATION	SWITCH TYPE
Crossbar	CBT	N-channel FET
CMOS	CD4000	Parallel n-/p-channel FET
High-speed CMOS	HC	Parallel n-/p-channel FET
Low-voltage CMOS	LV-A	Parallel n-/p-channel FET
Low-voltage CMOS	LVC	Parallel n-/p-channel FET
Low-voltage crossbar	CBTLV	Parallel n-/p-channel FET

2.1 Single FET Switch

Figure 3 shows a simplified FET switch, which consists of an n-channel transistor and gate bias and enable circuitry. The switch is bidirectional; the source and drain are interchangeable (while operating, the side with the lowest $V_{I/O}$ is the source). TI CBT bus switches are this type.

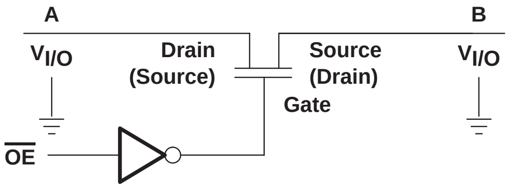


Figure 3. N-Channel FET Switch

For an n-channel FET to operate properly, the gate should be biased more positive than the magnitude of the signals to be passed. This is because the on-state resistance, r_{on} (or $r_{DS(on)}$ as it also is called), increases as the gate, minus source voltage, V_{GS}, decreases. In the case of CBT, when $\overline{OE}$ is low, the gate of the FET is biased to near V_{CC}. If the lowest $V_{I/O}$ signal approaches the magnitude of V_{CC}, V_{GS} decreases and r_{on} increases (see Figure 4). The ability to maintain a low r_{on} in a FET switch depends on maintaining V_{GS} as large as possible. In many applications, this characteristic is not a problem, but the designer should be aware of the nonlinearity of this type of device.

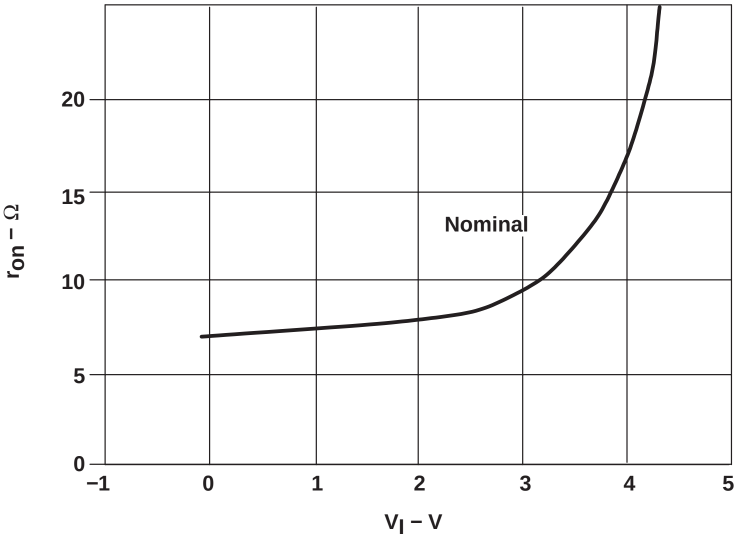


Figure 4. On-State Resistance vs Lowest I/O Voltage for an n-Channel FET Switch With V_{CC} = 5 V

2.2 Analog (Bilateral) Switches

Analog (or bilateral, as they also are called) switches consist of a single n-channel transistor in parallel with a single p-channel transistor (see Figure 5).

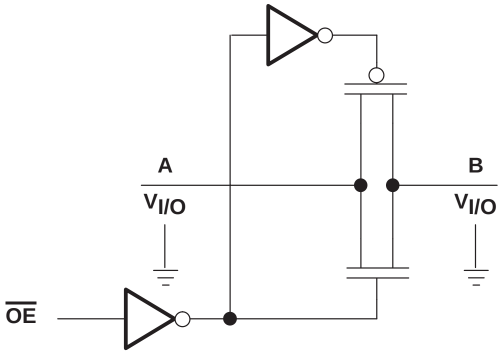


Figure 5. Parallel n-/p-Channel FET Switch

As before, when $V_{I/O}$ approaches V_{CC}, the n-channel conductance decreases (r_{on} increases) while the p-channel gate-source voltage is maximum and its r_{on} is minimal. The resulting parallel resistance combination is much flatter than individual channel resistances (see Figure 6).

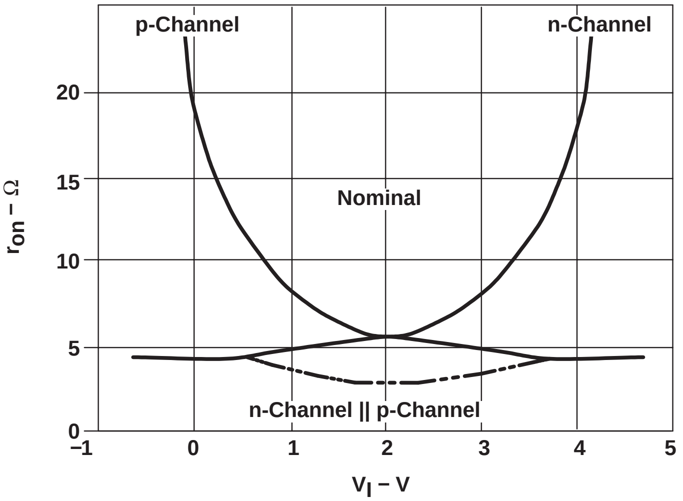


Figure 6. On-State Resistance vs Input Voltage for a Parallel n-/p-Channel FET Switch

A flat r_{on} is especially important if $V_{I/O}$ signals must swing from rail to rail. However, the tradeoff is increased switch capacitance due to the additional p-channel transistor and associated bias circuitry. TI offers a variety of choices of analog switches: HCT, HC, CD4000, LV-A, LVC, and CBTLV.

Some manufacturers offer n-channel signal switches with charge-pump-enabled pass transistors. A design of this type allows the gate voltage to be higher than V_{CC}. This increases V_{GS} above what is possible in noncharge-pump devices and allows signals at or above V_{CC} to be passed. A switch of this type has the advantage of low, relatively flat r_{on} (over the signal range), without the addition of a p channel and while maintaining C_{io} values comparable to pure n-channel FET switches. This performance comes at the expense of increased I_{CC} (from a few µA to several mA in some cases).

2.3 Analog Versus Digital Signal Switches

TI offers a wide variety of signal switches, and sometimes the nomenclature can be confusing to the point of implying limited functionality for a device or family. In reality, a switch, is a switch, is a switch (well, almost):

- Digital switch. Designed to pass (or isolate) digital signal levels. May exhibit the capability to satisfactorily pass analog signals. Examples are CBT and CBTLV switch families.
- Analog switch. Designed to pass (or isolate) analog signals. Often exhibits good digital signal performance as well. Examples are CD4066B, CD74HCT4066, CD74HC4066, SN74HC4066, SN74LV4066A, and SN74LVC1G66 switches.
- Bilateral switch. There are two meanings:
  - Signals can be passed in either direction (A to B, or B to A) through the switch.
  - Switch can be used in analog or digital applications.

  Examples are CD4066B, CD74HCT4066, CD74HC4066, SN74HC4066, SN74LV4066A, and SN74LVC1G66 switches.
- Bus switch. Digital switches designed for multibit switching in computing applications. Examples are CBT and CBTLV switch families.

The name bus switch implies digital only. However, with better understanding of switch characteristics, it is apparent that this view of their application might be too limited. Tables 2, 4, 5, 6, 7 and 14 summarize the performance of the CBT3125 and CBTLV3125 quadruple FET bus switches versus other TI bilateral analog switches. With regard to analog performance, these bus switches outperformed at least one bilateral switch in every parameter measurement.

It should be apparent that the most important switch characteristic depends on how it is used:

- What V_{CC} levels are present?
- What amplitude signals are required to be passed?
- What is the maximum signal distortion limit for the system?

In the following paragraphs, performance of TI signal switches is summarized to aid in the selection of the best signal switch for a given application.

2.4 Application Considerations

2.4.1 Digital Signal Considerations

- V_{CC}. There are a number of considerations and tradeoffs here. What voltage levels are present on the board? What is the amplitude of the signal levels to be passed? Is level translation required?
- V_{IH}/V_{IL}. Switch control (Enable). How will the switch be controlled? Logic level output? Comparator? ASIC? Should the switch turn on if the control signal is high or low?
- Switch output level. The maximum signal level a switch without a charge pump can pass is limited to the switch V_{CC}. Is there sufficient noise margin on the device downstream of the switch such that signal attenuation in the switch will not cause data errors? For instance, the n-channel transistor of a CBT device clamps the switch output at a little more than 1 V below the operating V_{CC}, making it unsuitable for 5-V CMOS high-level (V_{IH} = 3.5 V) signal transmission unless operated from at least 4.5-V V_{CC}.
- r_{on}.
  - Is the switch connected to a transmission line? If so, what is the impedance? The switch r_{on} should be less than or equal to the line impedance to allow for proper matching and to prevent unwanted signal reflections.
  - For nontransmission-line connections, the switch r_{on} and the load resistance form an undesired voltage divider. In this case, that is a switch with a r_{on} small enough to ensure the switch output is not reduced below a valid input high level (V_{IH}) for the connected load. As mentioned previously, the tradeoff for low r_{on} is often higher signal-path capacitance, which reduces frequency response.
- t_{en}/t_{dis}. These parameters determine how quickly the switch can respond to a desired on or off state. In general, switch enable and disable times are not symmetrical. This is not usually an issue, as few applications require high control (enable) signal frequencies.
- t_{pd}. This parameter is negligible for all but the most critical timing budgets. When the switch is on, the propagation delay through the pass transistor(s) is minimal. TI specifies this number as the mathematical calculation of the typical r_{on} times the load capacitance.
- Number of bits required to be switched. With TI’s wide variety of signal switches, it is possible to switch between 1 to 32 bits at the same time with a single device. For instance, the LVC1G66 or CBT1G125 can be used to switch a single bit, while the CBTLV16211 is capable of switching 24 bits total in banks of 12. Or, by tying the adjacent enable pins together, it is possible to control 24 bits with one enable signal.
- Special features. TI offers bus switches with special features, such as an integrated diode for single-component level shifting (CBTD), active clamps for undershoot protection (CBTK), Schottky-diode clamps for undershoot protection (CBTS), a bus-hold option (CBTH) for holding floating or unused I/O pins at valid logic levels, and an integrated-series-resistor option (CBTR) to reduce signal-reflection noise.

Table 2 summarizes the digital performance characteristics of eight TI signal switches from which generalities can be derived regarding switch-family performance. For exact parameters, refer to the respective data sheets.

2.4.2 Digital Performance

Table 2. Summary of Digital Performance[†]

PARAMETER	CD4066	CD74HC4066	CD74HCT4066	SN74HC4066	LVC1G66	LV4066A	CBT3125	CBTLV3125
V_{CC}	3−18 V	2−10 V	4.5−5.5 V	2−6 V	1.65−5.5V	2−5.5 V	4−5.5 V	2.3−3.6 V
r_{on}	200−1300 Ω	15−142 Ω	25−142 Ω	30−150 Ω	3−30 Ω	21−225 Ω	5−22 Ω	5−40 Ω
t_{pd}[‡]	7−40 ns	4−90 ns	4−18 ns	3−75 ns	0.6−2 ns	0.3−18 ns	0.25−0.35ns	0.15−0.25 ns
t_{en}[§]	15−70 ns	8−150 ns	4−18 ns	18−225 ns	1.5−10 ns	1.6−32 ns	1.8−5.6 ns	2−4.6 ns
t_{dis}[¶]	15−70 ns	12−225 ns	9−36 ns	22−250 ns	1.4−10 ns	3.2−32 ns	1−4.6 ns	1−4.2 ns
V_{IH} (control inputs)	approx. 0.7 × V_{CC}	5-V CMOS	5-V TTL	5-V CMOS	5-V CMOS	5-V CMOS	5-V TTL/ LVTTL	LVTTL/ 2.5-V CMOS
V_{IL} (control inputs)	approx. 0.2 × V_{CC}	5-V CMOS	5-V TTL	5-V CMOS	5-V CMOS	5-V CMOS	5-V TTL/ LVTTL	LVTTL/ 2.5-V CMOS
C_i (control)	5−7.5 pF	10 pF	10 pF	3−10 pF	2 pF	1.5 pF	3 pF	2.5 pF
C_{io} (on)					13 pF			
C_{io} (off)	8 pF	5 pF	5 pF	9 pF	6 pF	5.5 pF	4 pF	7 pF

[†] Data are based on data-sheet parameters for the parts tested for this application report. Refer to the respective data sheets for specific parameters and load conditions.

[‡] t_{pd} is the same as t_{PLH}/t_{PHL}. The switch contributes no significant propagation delay other than the RC delay of the typical on-state resistance of the switch and the load capacitance when driven by an ideal voltage source (zero output impedance)

[§] t_{en} is the same as t_{PZL}/t_{PZH}.

[¶] t_{dis} is the same as t_{PLZ}/t_{PHZ}.

2.4.3 Analog Signal Considerations

- V_{CC}. For noncharge-pump switches, V_{CC} determines the amplitude of the analog signals that can be passed without clipping. The gate(s) of the pass transistors must be biased relative to the minimum and maximum values of the expected input voltage range. Switches, such as the CD4000 series, allow for biasing from two supplies, making it easy to pass both positive and negative signals. Switches with integrated charge pumps can elevate the gate voltage above V_{CC} (at the expense of larger I_{CC}) and, thus, pass signals of a magnitude greater than V_{CC}.
- V_{IH}/V_{IL}. Why are these important analog switch considerations? In most applications, the signal switch is controlled by the output of a digital source, therefore, the control signal levels, V_{IH} and V_{IL}, must be compatible with that source to ensure proper operation of the switch. The CD74HC4066 and CD74HCT4066 are excellent examples of switches with almost exactly the same performance characteristics, but very different control signal levels. The V_{IH} of the CD74HC4066 is 3.15 V, with V_{CC} at 4.5 V, while CD74HCT4066 is specified with V_{IH} of 2 V for V_{CC} between 4.5 and 5.5 V.
- r_{on}. Because it contributes to signal loss and degradation, low r_{on} tradeoffs must be considered. Noncharge-pump switches achieve low r_{on} with large pass transistors. These larger transistors lead to larger die sizes and increased C_{io}. This additional channel capacitance can be very significant as it limits the frequency response of the switch. As stated in section 2.4.1, switches utilizing charge-pump technology can achieve low r_{on} and C_{io}, but require significantly higher I_{CC}.

- Frequency response. All CMOS switches have an upper limit to the frequency that can be passed. No matter how low r_{on} and C_{io} can be maintained in the chip manufacturing process, they still form an undesired low-pass filter that attenuates the switch output signal.
- Sine-wave distortion or total harmonic distortion. These are measurements of the linearity of the device. Nonlinearity can be introduced a number of ways (design, device physics, etc.) but, typically, the largest contributor is r_{on}. As shown in Figures 2 and 4, r_{on} varies with $V_{I/O}$ for all types of CMOS switches. Having a low r_{on} is important, but a flat r_{on} over the signal range is almost equally important. N-channel switches, such as CBT, exhibit very flat r_{on} characteristics for signal ranges of $0 < V_{I/O} < (V_{CC} - 2\ V)$, but r_{on} increases very rapidly as $V_{I/O}$ approaches V_{CC} and V_{GS} decreases. Parallel n-/p-channel switches offer good r_{on} flatness for signal ranges of $0 < V_{I/O} < V_{CC}$, with the best flatness characteristic at the highest recommended switch V_{CC}.
- Crosstalk. There are two types of crosstalk to consider:
  - Control (enable) to output. The level of crosstalk is a measure of how well decoupled the switch control signal is from the switch output. Due to the parasitic capacitance of CMOS processes, changing the state on the control signal causes noise to appear on the output. In audio applications, this can be a source of the annoying pop that is sometimes heard when switching the unit on or off.
  - Between switches. The level of crosstalk also is a measure of adjacent-channel rejection. As with control-to-output crosstalk, parasitic capacitance can couple the signal on one switch with that on another switch.
- Charge Injection (Q). TI specifies enable-to-output crosstalk and some competitors use this parameter. As with enable-to-output crosstalk, changing the state on the control pin causes a charge to be coupled to the channel of the transistor introducing signal noise. It is presented in this report for a relative comparison with the competition.
- Feedthrough. This characteristic is related to the ability of the switch to block signals when off. As with crosstalk, parasitic capacitance allows high frequencies to couple through the switch, making it appear to be on.

2.4.4 Analog Performance

Table 3. V_{CC} Above 5.5 V[†]

PARAMETER	← BETTER PERFORMANCE		
r_{on} (typical to maximum)	CD74HC4066 15−126 Ω	CD74HC4066[‡] 30 Ω	CD4066 200−550 Ω
r_{on} (peak) (typical to maximum)	SN74HC4066[‡] 50 Ω (typ)	CD74HC4066 not specified	CD4066 not specified
Frequency response	CD74HC4066[§] 200 MHz	CD4066 40 MHz	SN74HC4066[§] 30 MHz
THD/Sine-wave distortion	CD74HC4066 0.008%	SN74HC4066[§] 0.05%	CD4066 0.4%
Crosstalk (enable to output)	SN74HC4066 20 mV	CD4066 50 mV	CD74HC4066 550 mV
Crosstalk (between switches)	CD4066 −50 dB at 8 MHz	CD74HC4066[§] −72 dB at 1 MHz	SN74HC4066[§] −45 dB at 1 MHz
Feedthrough attenuation	CD74HC4066[§] −72 dB at 1 MHz	CD4066 −50 dB at 1 MHz	SN74HC4066[§] −42 dB at 1 MHz

[†] Data are based on data-sheet parameters for the parts tested for this application report. Refer to the respective data sheets for specific parameters and load conditions.

[‡] Specification at V_{CC} = 6 V

[§] Specification at V_{CC} = 4.5 V

Table 4. V_{CC} = 4.5 V[†]

PARAMETER	← BETTER PERFORMANCE					
r_{on} (typical to maximum)	LVC1G66 3−10 Ω	CBT3125[‡] 5−15 Ω	LV4066A 21−100 Ω	CD74HC/ HCT4066 25−142 Ω	SN74HC4066 50−106 Ω	CBT3125[§] 5−1000 Ω
r_{on} (peak) (typical to maximum)	CBT3125[‡§] 10 Ω	LVC1G66 6−15 Ω	LV4066A 31−125 Ω	CD74HC/ HCT4066[§] 50−70 Ω	SN74HC4066 70−215 Ω	CBT3125[§] 1000 Ω
Frequency response	CBT3125[‡§] >200 MHz	LVC1G66 195 MHz	CD74HC/ HCT4066[¶] 200 MHz	LV4066A 50 MHz	SN74HC4066 30 MHz	
THD/Sine-wave distortion	LVC1G66 0.01%	CD74HC/ HCT4066 0.023%	CBT3125[‡§] 0.035%	SN74HC4066 0.05%	LV4066A 0.1%	
Crosstalk (enable to output)	SN74HC4066 15 mV	LV4066A 50 mV	LVC1G66 100 mV	CBT3125[§] 120 mV	CD74HCT4066 130 mV	CD74HC4066 200 mV
Crosstalk (between switches)	CD74HC/HCT4066 −72 dB	LVC2G66 −58 dB	CBT3125[‡§] −53 dB	SN74HC4066 −45 dB	LV4066A −45 dB	
Feedthrough attenuation	CD74HC/HCT4066 −72 dB	LVC1G66 −58 dB	SN74HC4066 −42 dB	LV4066A −40 dB	CBT3125[§] −36 dB	

[†] Data are based on data-sheet parameters for the parts tested for this application report. Refer to the respective data sheets for specific parameters and load conditions.

[‡] CBT3125, $0 \le V_{I/O} \le (V_{CC} - 2\text{ V})$

[§] Value from application report measurement. Not specified in data sheet.

[¶] Ranked here due to load variation from other devices in this report

Table 5. V_{CC} = 3 V[†]

PARAMETER	← **BETTER PERFORMANCE**				
r_{on} (typical to maximum)	LVC1G66 6−15 Ω	CBTLV3125 5−15 Ω	LV4066A 29−190 Ω	CD74HC4066[‡] Not specified	SN74HC4066[‡] Not specified
r_{on} (peak) (typical to maximum)	CBTLV3125[§] 15−20 Ω	LVC1G66 12−20 Ω	LV4066A 57−225 Ω	CD74HC4066[‡] Not specified	SN74HC4066[‡] Not specified
Frequency response	CBTLV3125[§] >200 MHz	LVC1G66 175 MHz	CD74HC4066[‡] Not specified	LV4066A 35MHz	SN74HC4066[†] Not specified
THD/Sine-wave distortion	LVC1G66 0.015%	CD74HC4066[‡] Not specified	SN74HC4066[‡] Not specified	CBTLV3125[§] 0.09%	LV4066A 0.1%
Crosstalk (enable to output)	SN74HC4066[‡] Not specified	LV4066A 20 mV	LVC1G66 70 mV	CBTLV3125[§] 70 mV	CD74HC4066[‡] Not specified
Crosstalk (between switches)	CD74HC4066[‡] Not specified	LVC2G66 −58 dB	CBTLV3125[§] −49 dB	SN74HC4066[‡] Not specified	LV4066A −45 dB
Feedthrough attenuation	CD74HC4066[‡] Not specified	LVC1G66 −58 dB	CBTLV3125 −52 dB	SN74HC4066[‡] Not specified	LV4066A −40 dB

[†] Data are based on data-sheet parameters for the parts tested for this application report. Refer to the respective data sheets for specific parameters and load conditions.

[‡] Position in table based on estimated performance. Information not specified in data sheet.

[§] Value from application report measurement. Not specified in data sheet.

Table 6. V_{CC} = 2.5 V[†]

PARAMETER	← **BETTER PERFORMANCE**				
r_{on} (typical to maximum)	LVC1G66 9−20 Ω	CBTLV3125 5−40 Ω	LV4066A 38−225 Ω	CD74HC4066[‡] Not specified	SN74HC4066[§] 150 Ω
r_{on} (peak) (typical to maximum)	CBTLV3125[¶] 15−45 Ω	LVC1G66 20−30 Ω	LV4066A 143−600 Ω	CD74HC4066[‡] Not specified	SN74HC4066[§] 320 Ω
Frequency response	CBTLV3125[¶] >200 MHz	LVC1G66 120 MHz	CD74HC4066[‡] Not specified	LV4066A 30 MHz	SN74HC4066[‡] Not specified
THD/Sine-wave distortion	LVC1G66 0.025%	CD74HC4066[‡] Not specified	SN74HC4066[‡] Not specified	LV4066A 0.1%	CBTLV3125[¶] 0.11%
Crosstalk (enable to output)	SN74HC4066[‡] Not specified	LV4066A 15 mV	CBTLV3125[‡] 30 mV	LVC1G66 50 mV	CD74HC4066[‡] Not specified
Crosstalk (between switches)	CD74HC4066[‡] Not specified	LVC2G66 −58 dB	CBTLV3125 −45 dB	SN74HC4066[‡] Not specified	LV4066A −45 dB
Feedthrough attenuation	CD74HC4066[‡] Not specified	LVC1G66 −58 dB	CBTLV3125 −52 dB	SN74HC4066[‡] Not specified	LV4066A −40 dB

[†] Data are based on data-sheet parameters for the parts tested for this application report. Refer to the respective data sheets for specific parameters and load conditions.

[‡] Position in table based on estimated performance. Information not specified in data sheet.

[§] Data at V_{CC} = 2 V

[¶] Value from application report measurement. Not specified in data sheet.

2.4.5 SN74CBT Characteristics

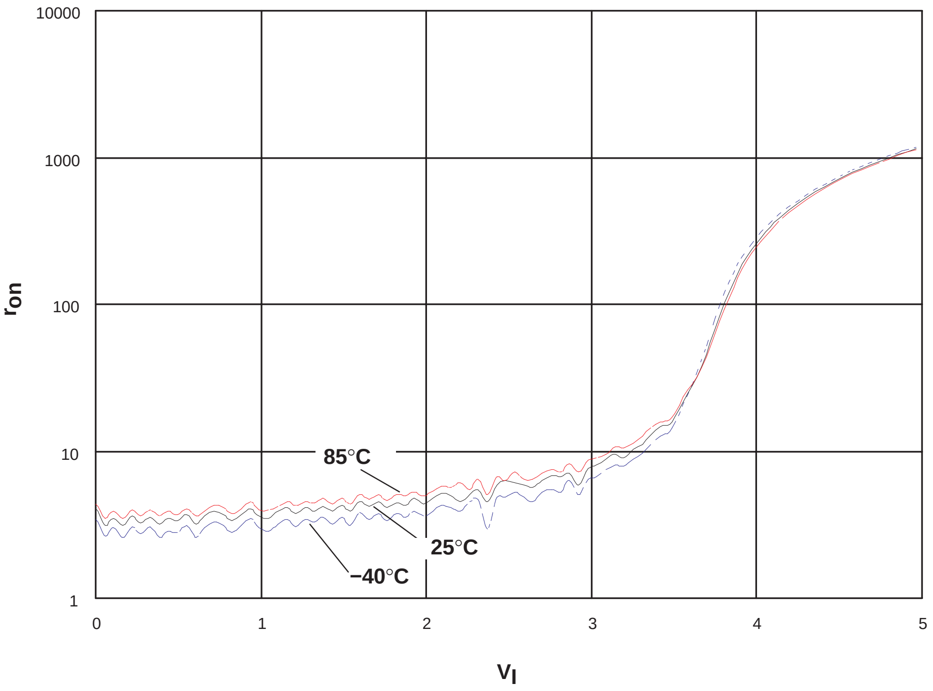


Figure 7. Log r_{on} vs V_I, V_{CC} = 5 V (SN74CBT3125)

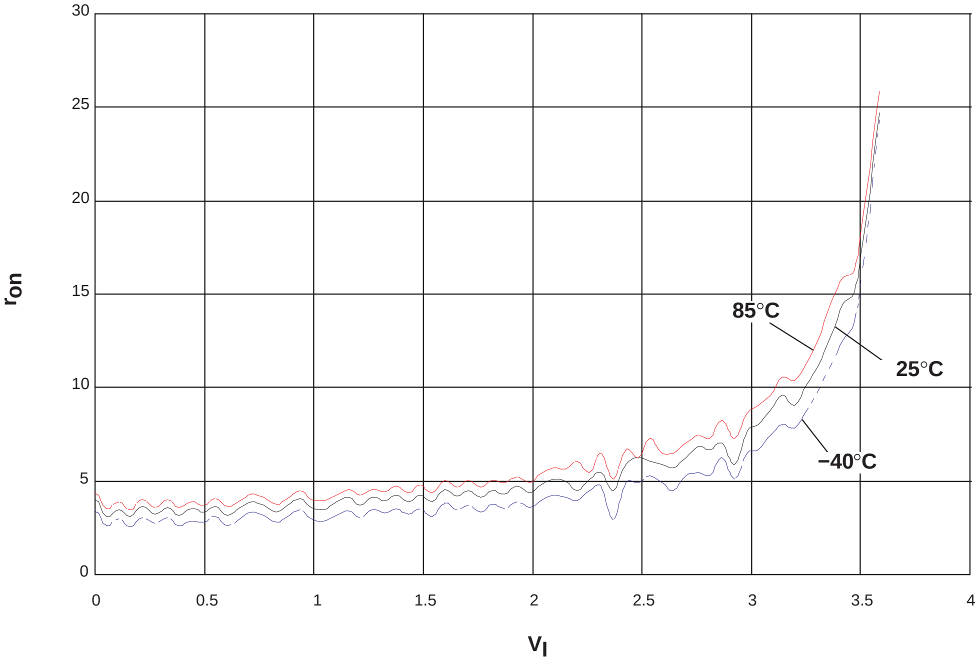


Figure 8. r_{on} vs V_I, V_{CC} = 5 V (SN74CBT3125)

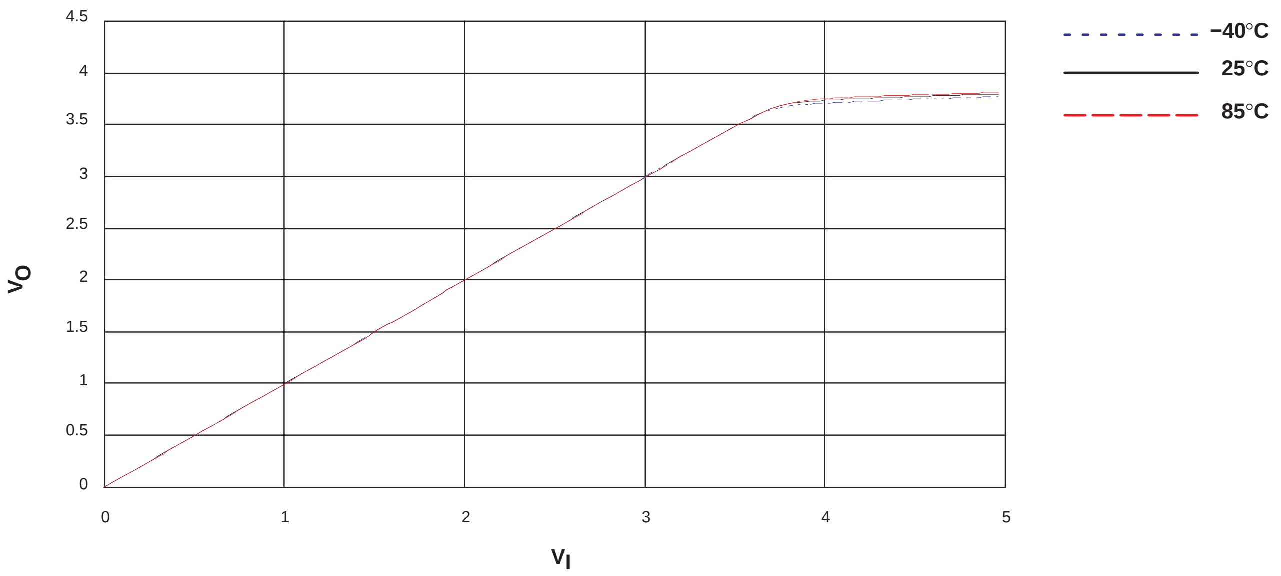


Figure 9. V_I vs V_O, V_{CC} = 5 V (SN74CBT3125)

Table 7. SN74CBT3125 Analog Parameter Measurement Data†

V_{CC}	Frequency Response	Sine-Wave Distortion	Total Harmonic Distortion	Crosstalk		Charge Injection	Feedthrough
		1 kHz		Between Switches	Enable to Output		
5 V	>200 MHz	0.035%	0.15%	−53 dB	120 mV	7.2 pC	−36 dB

† Postcharacterization measurement for SN74CBT3125

2.4.6 CD74HCT Characteristics

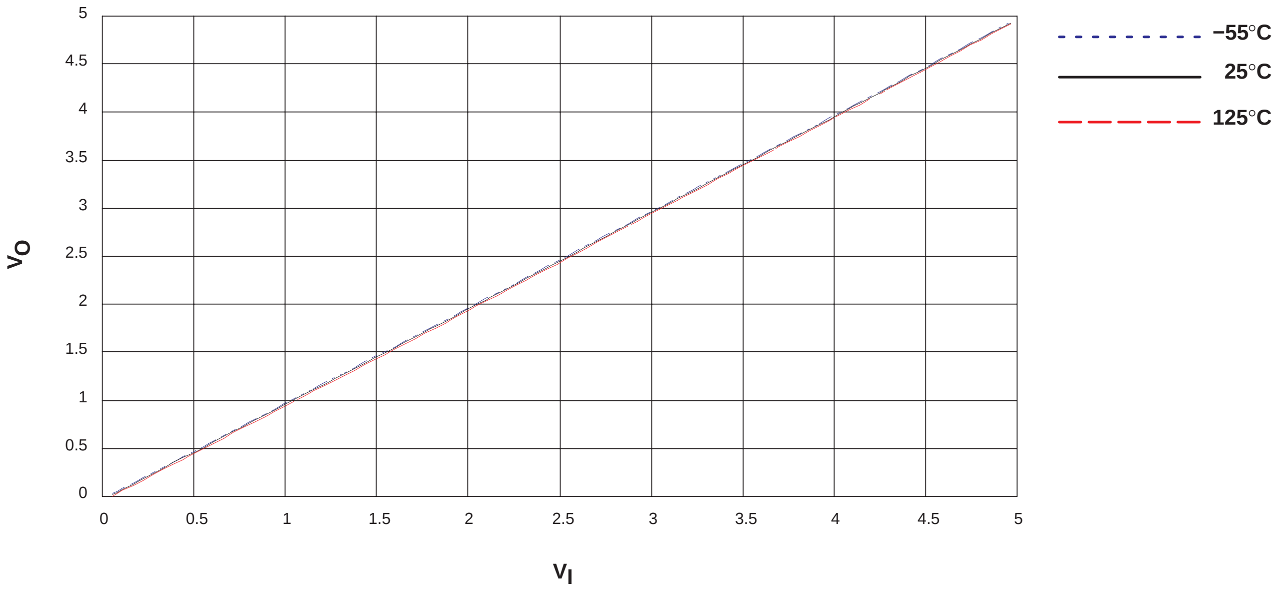


Figure 10. V_I vs V_O, V_{CC} = 5 V (CD74HCT4066)

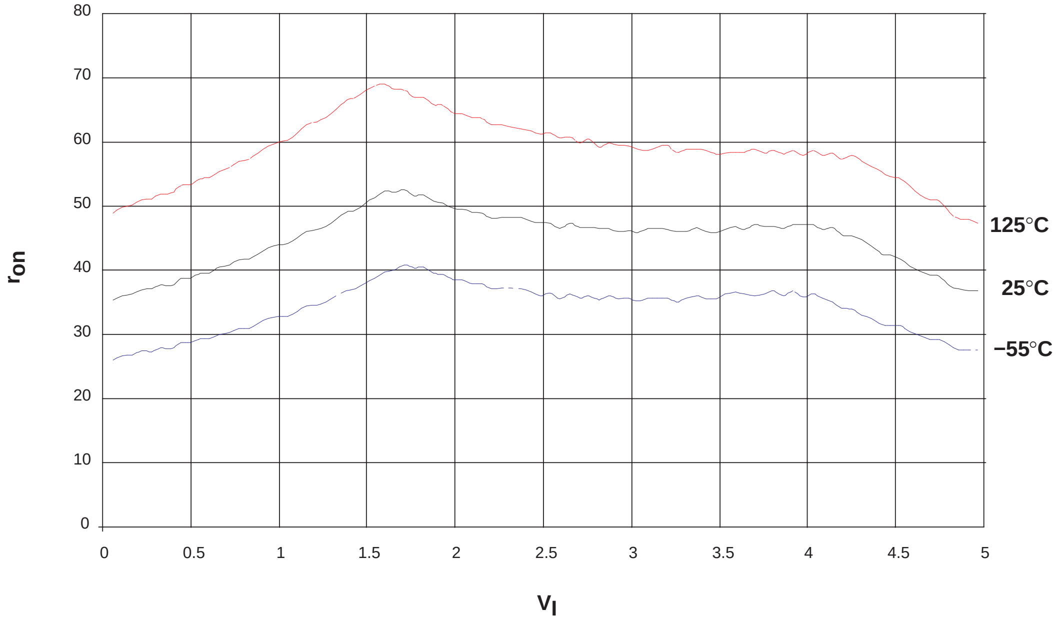


Figure 11. r_{on} vs V_I, V_{CC} = 5 V (CD74HCT4066)

Table 8. CD74HCT4066 Analog Parameter Measurement Data[†]

V_{CC}	Frequency Response	Total Harmonic Distortion	Crosstalk		Charge Injection[‡]	Feedthrough
		1 kHz	Between Switches	Enable to Output		
4.5 V	200 MHz	0.023%	−72 dB	130 mV	8.1 pC	−72 dB

[†] Data-sheet values for CD74HCT4066, except as noted
[‡] Postcharacterization measurement for CD74HCT4066

2.4.7 CD74HC Characteristics

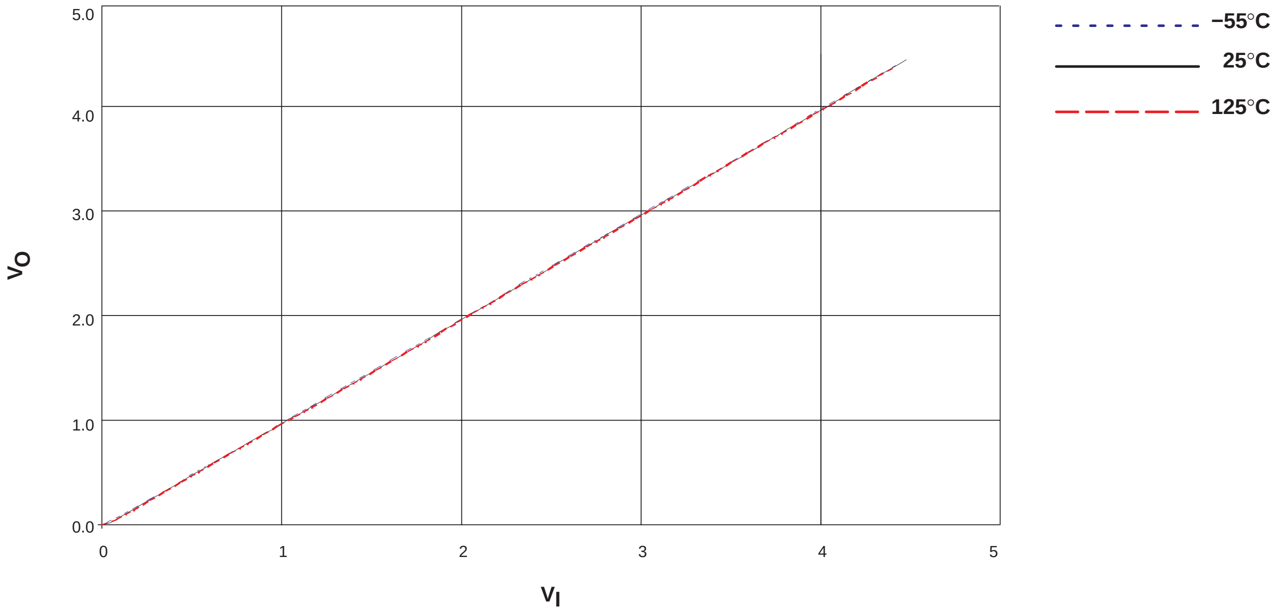


Figure 12. V_I vs V_O, V_{CC} = 4.5 V (CD74HC4066)

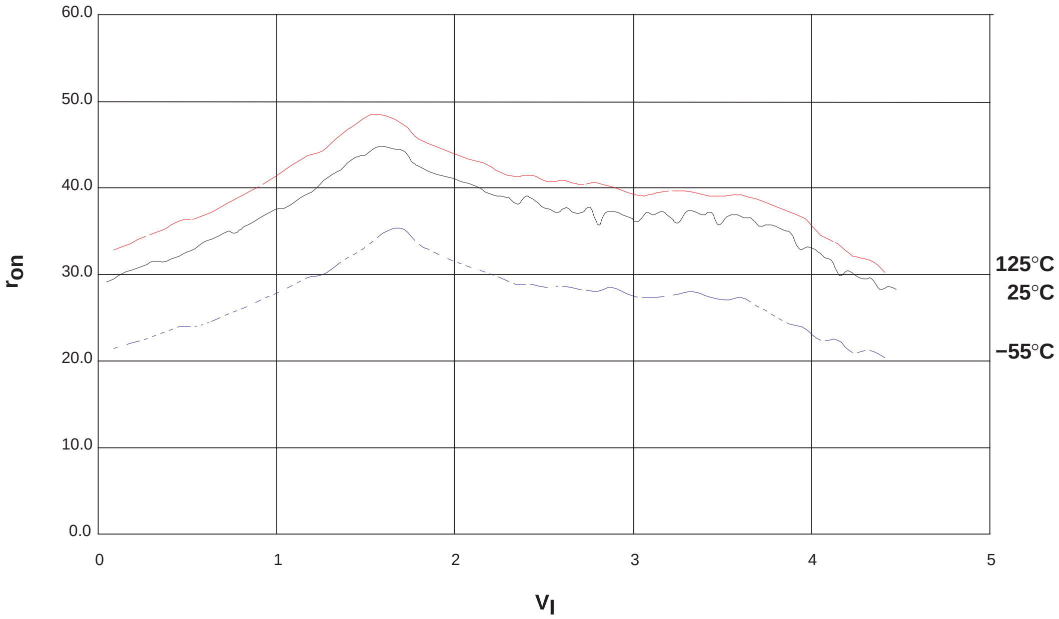


Figure 13. r_{on} vs V_I, V_{CC} = 4.5 V (CD74HC4066)

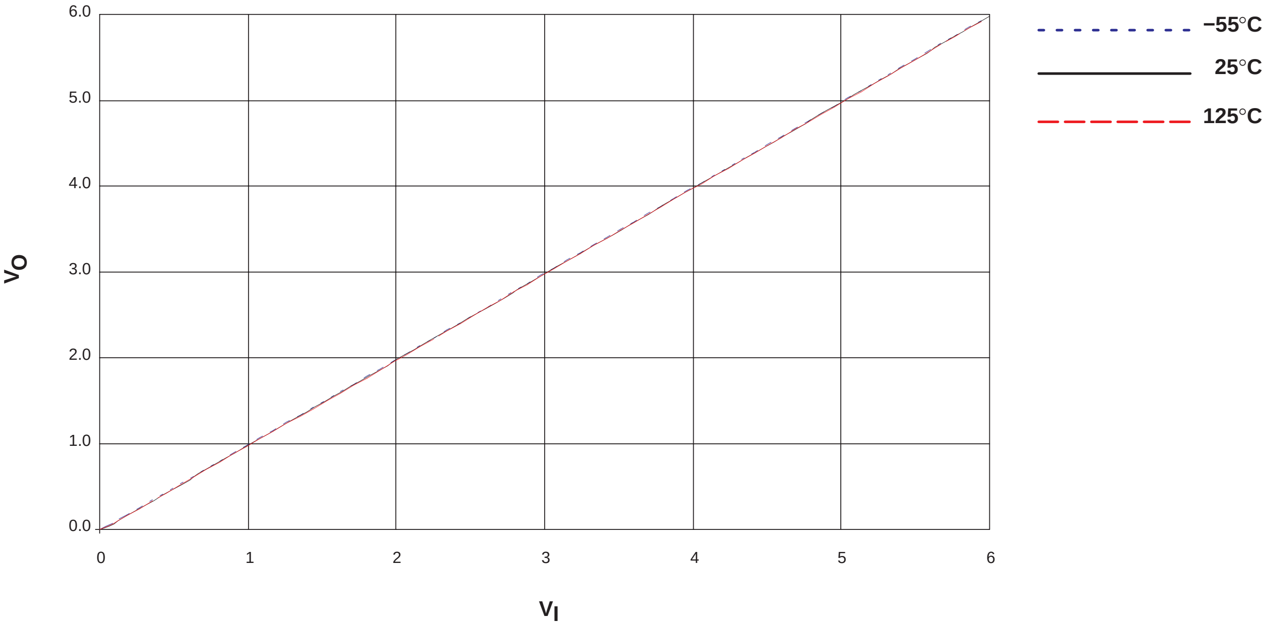


Figure 14. V_O vs V_I, V_{CC} = 6 V (CD74HC4066)

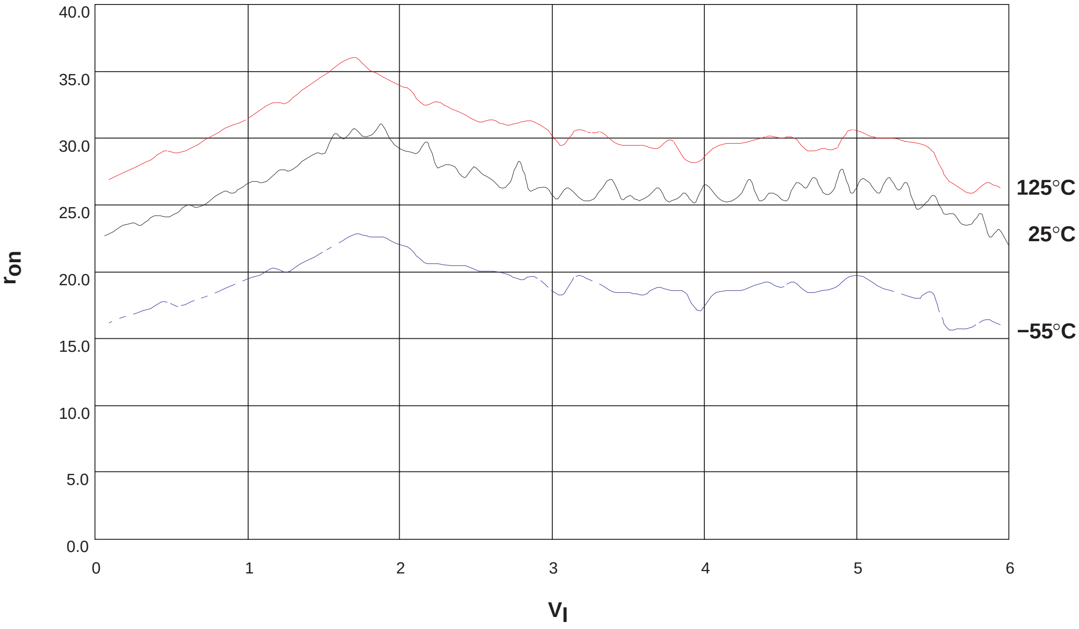


Figure 15. r_{on} vs V_I, V_{CC} = 6 V (CD74HC4066)

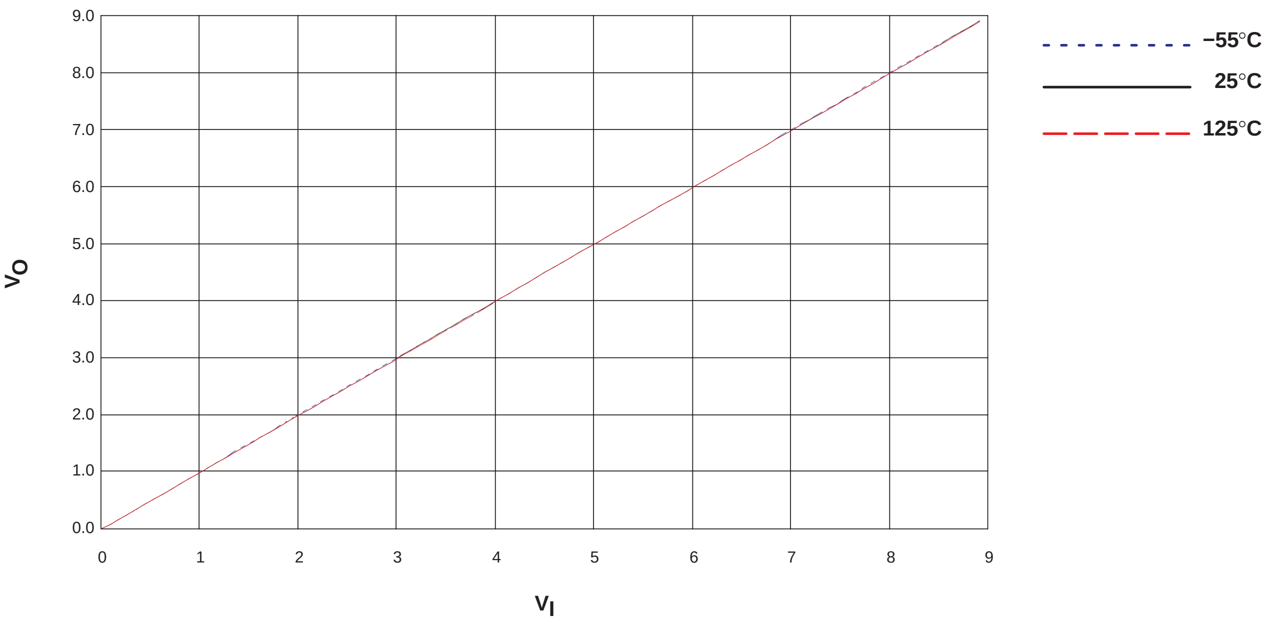


Figure 16. V_O vs V_I, V_{CC} = 9 V (CD74HC4066)

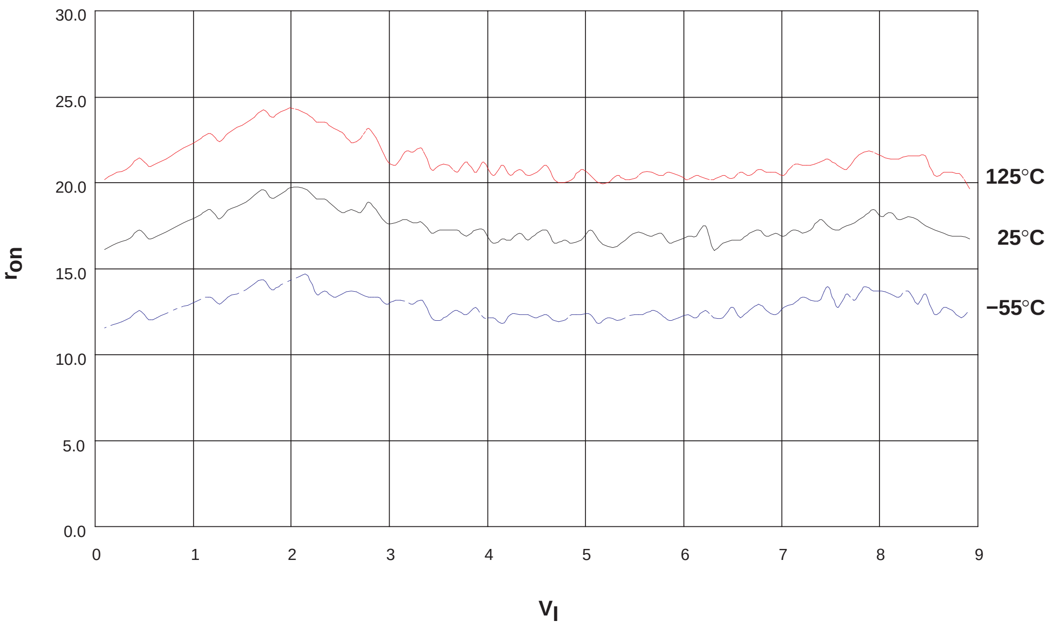


Figure 17. r_{on} vs V_I, V_{CC} = 9 V (CD74HC4066)

Table 9. CD74HC4066 Analog Parameter Measurement Data[†]

V_{CC}	Frequency Response	Total Harmonic Distortion	Crosstalk		Charge Injection[‡]	Feedthrough
		1 kHz	Between Switches	Enable to Output		
4.5 V	200 MHz	0.022%	−72 dB	200 mV	6.2 pC	−72 dB
9 V	200 MHz	0.008%	N/A	550 mV	9.0 pC	N/A

[†] Data-sheet values for CD74HC4066, except as noted
[‡] Postcharacterization measurement for CD74HC4066

2.4.8 SN74HC Characteristics

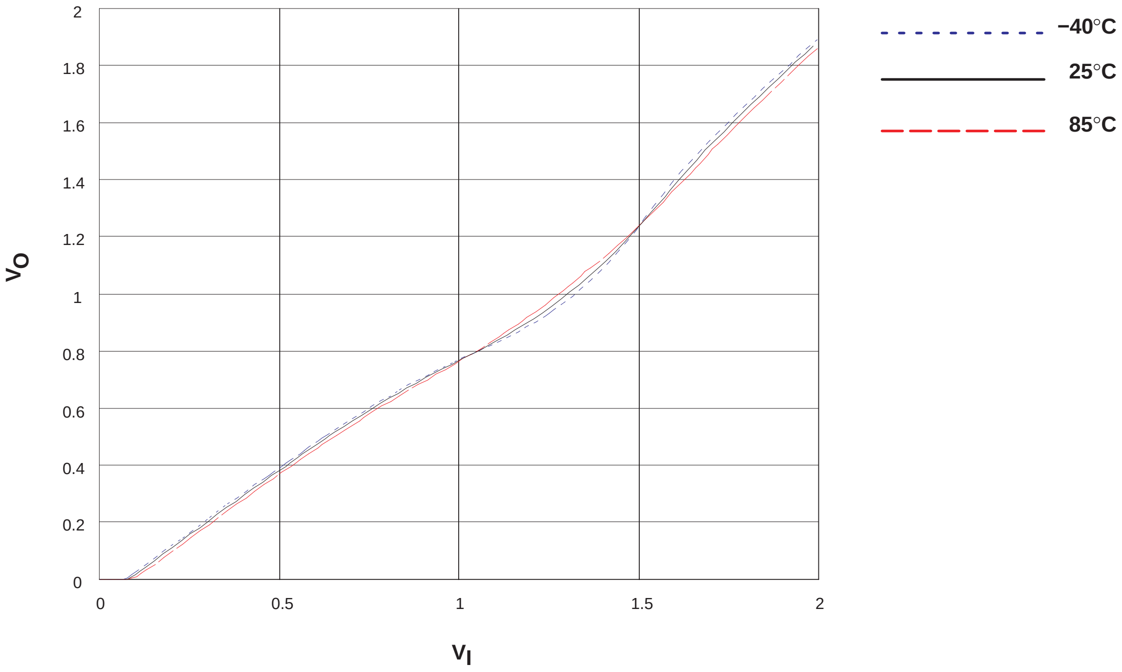


Figure 18. V_O vs V_I, V_{CC} = 2 V (SN74HC4066)

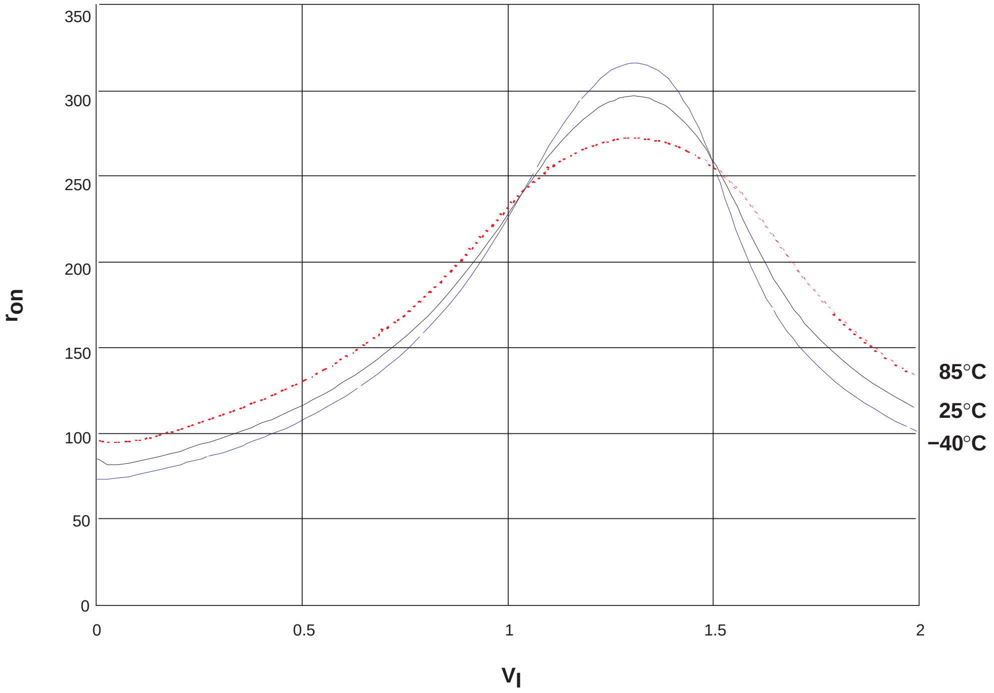


Figure 19. r_{on} vs V_I, V_{CC} = 2 V (SN74HC4066)

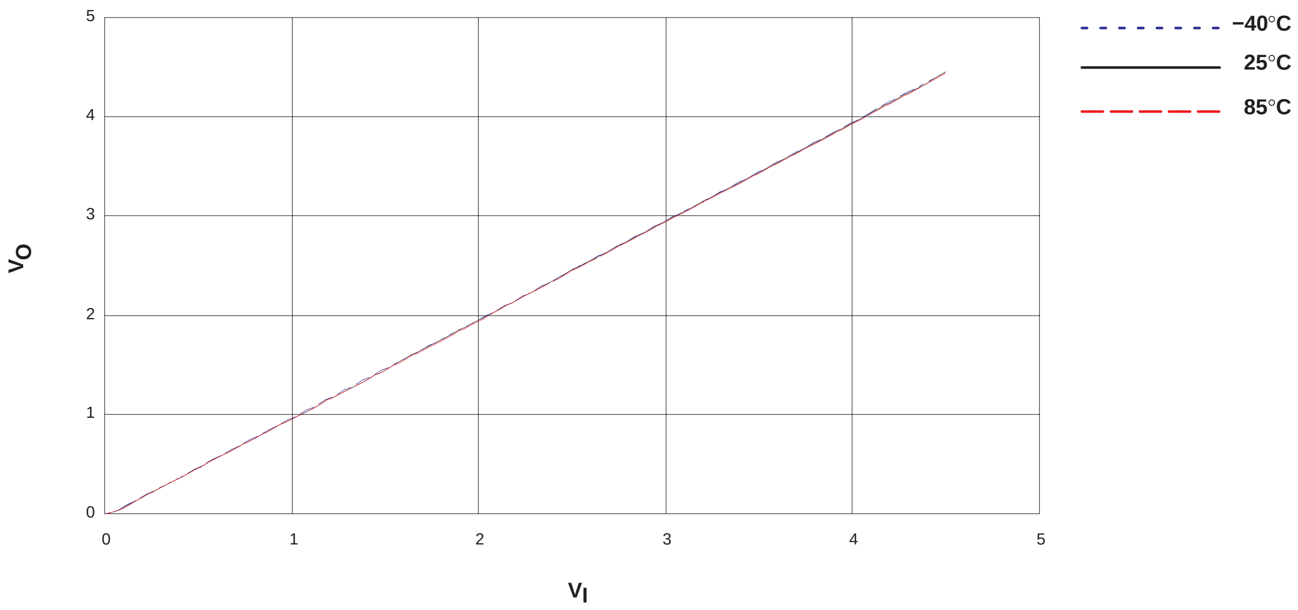


Figure 20. V_O vs V_I, V_{CC} = 4.5 V (SN74HC4066)

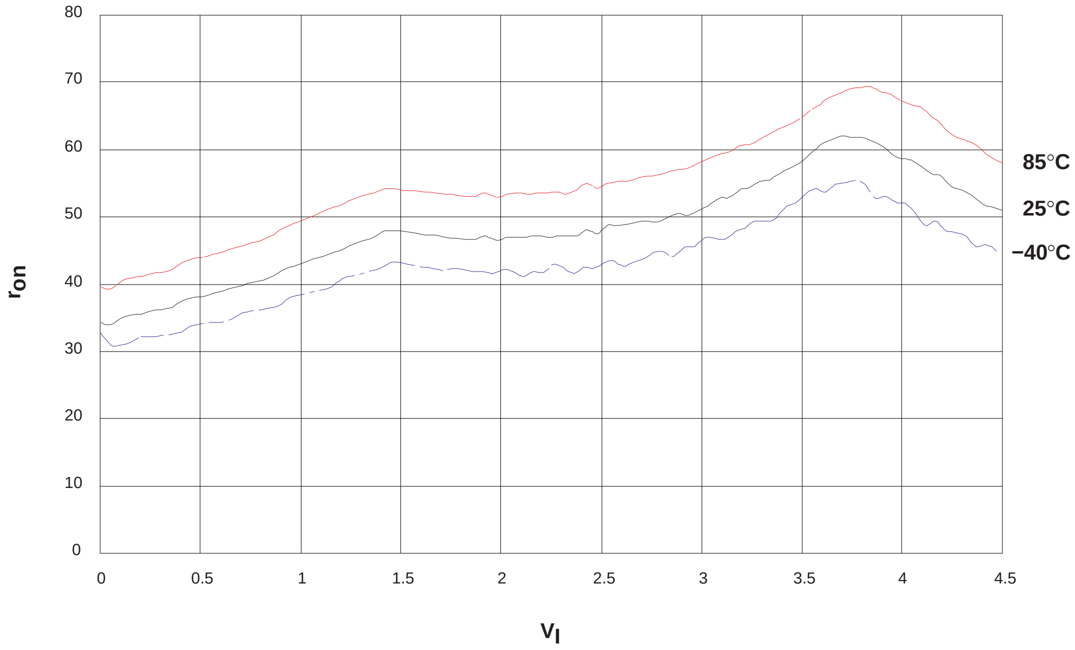


Figure 21. r_{on} vs V_I, V_{CC} = 4.5 V (SN74HC4066)

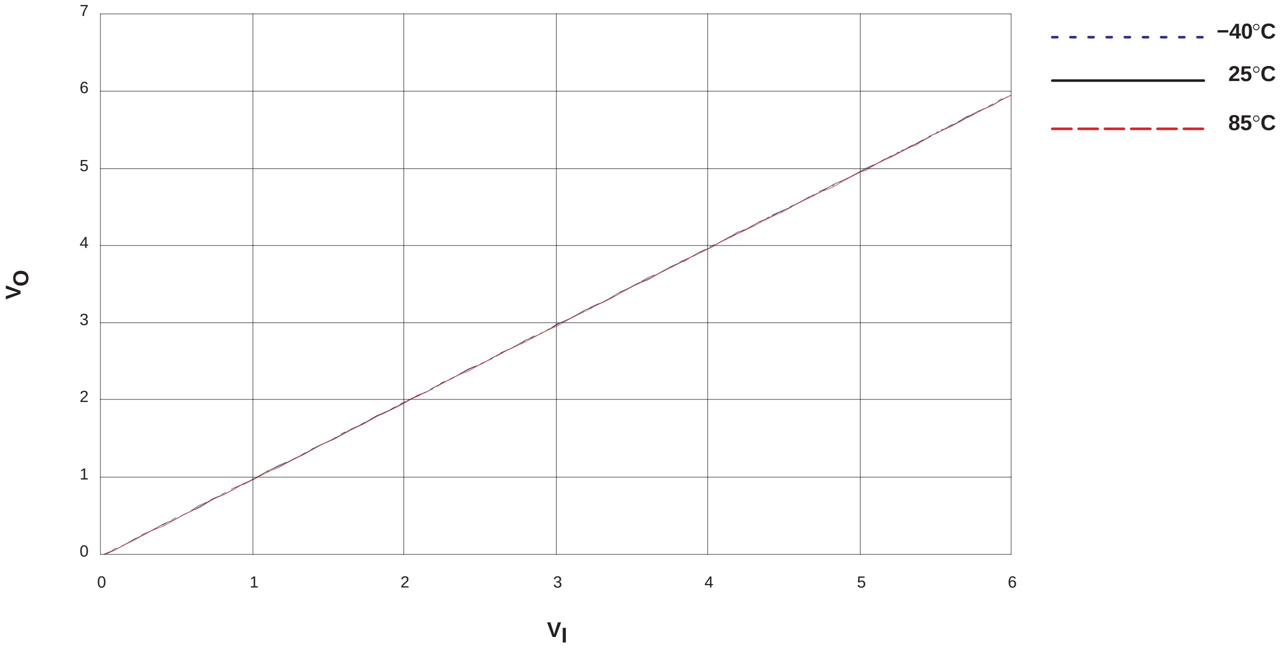


Figure 22. V_O vs V_I, V_{CC} = 6 V (SN74HC4066)

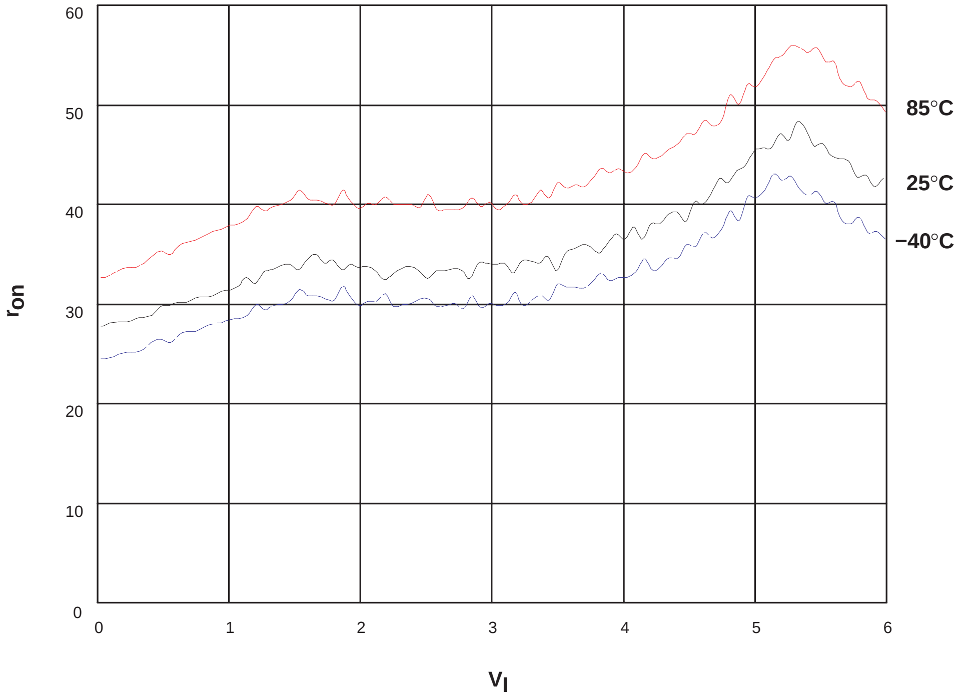


Figure 23. r_{on} vs V_I, V_{CC} = 6 V (SN74HC4066)

Table 10. SN74HC4066 Analog Parameter Measurement Data[†]

V_{CC}	Frequency Response	Sine-Wave Distortion	Crosstalk		Charge Injection[‡]	Feedthrough
		1 kHz	Between Switches	Enable to Output		
2 V	N/A	N/A	N/A	N/A	3.8 pC	N/A
4.5 V	30 MHz	0.05%	−45 dB	15 mV	5.9 pC	−42 dB
6 V	N/A	N/A	N/A	20 mV	7.9 pC	N/A

[†] Data-sheet values for SN74HC4066, except as noted

[‡] Postcharacterization measurement for SN74HC4066

2.4.9 CD4066B Characteristics

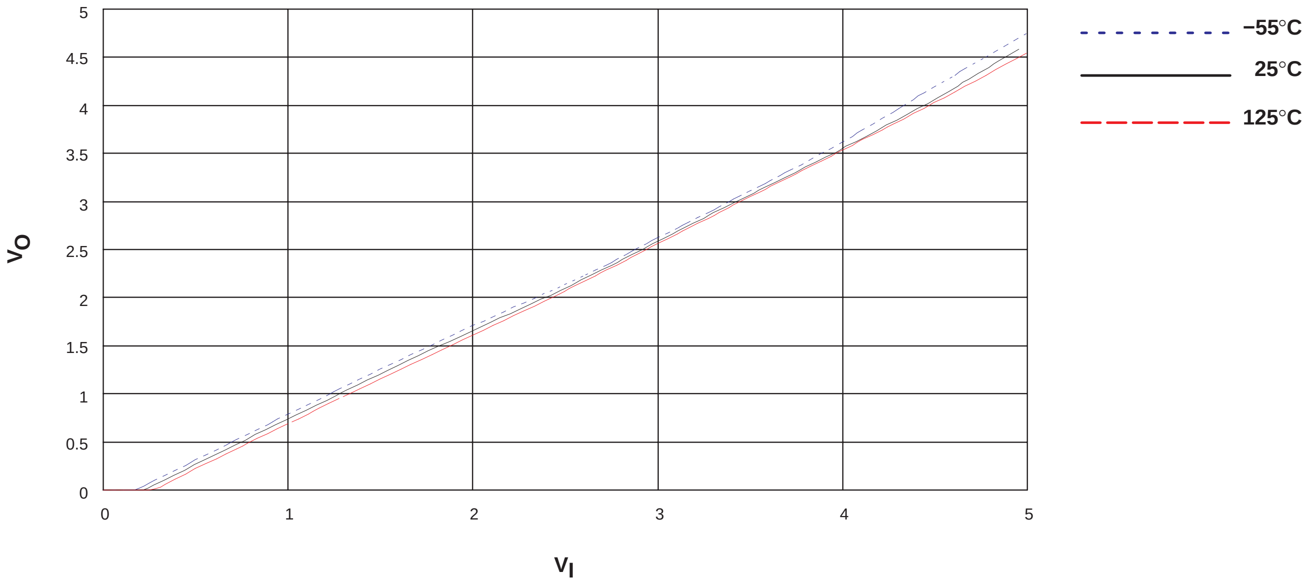


Figure 24. V_O vs V_I, V_{CC} = 5 V (CD4066B)

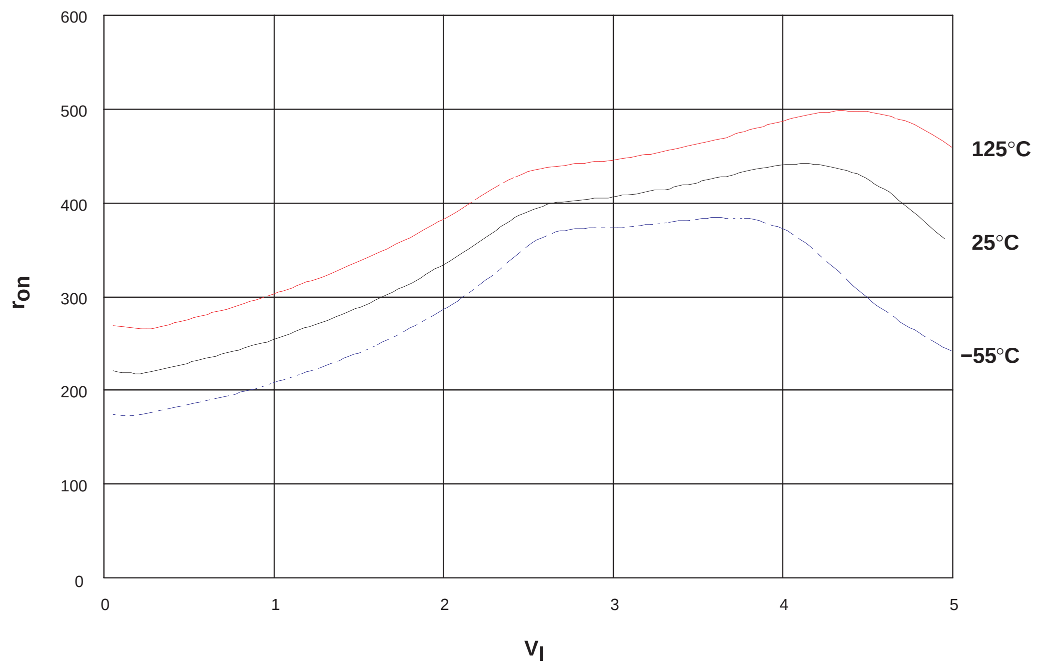


Figure 25. r_{on} vs V_I, V_{CC} = 5 V (CD4066B)

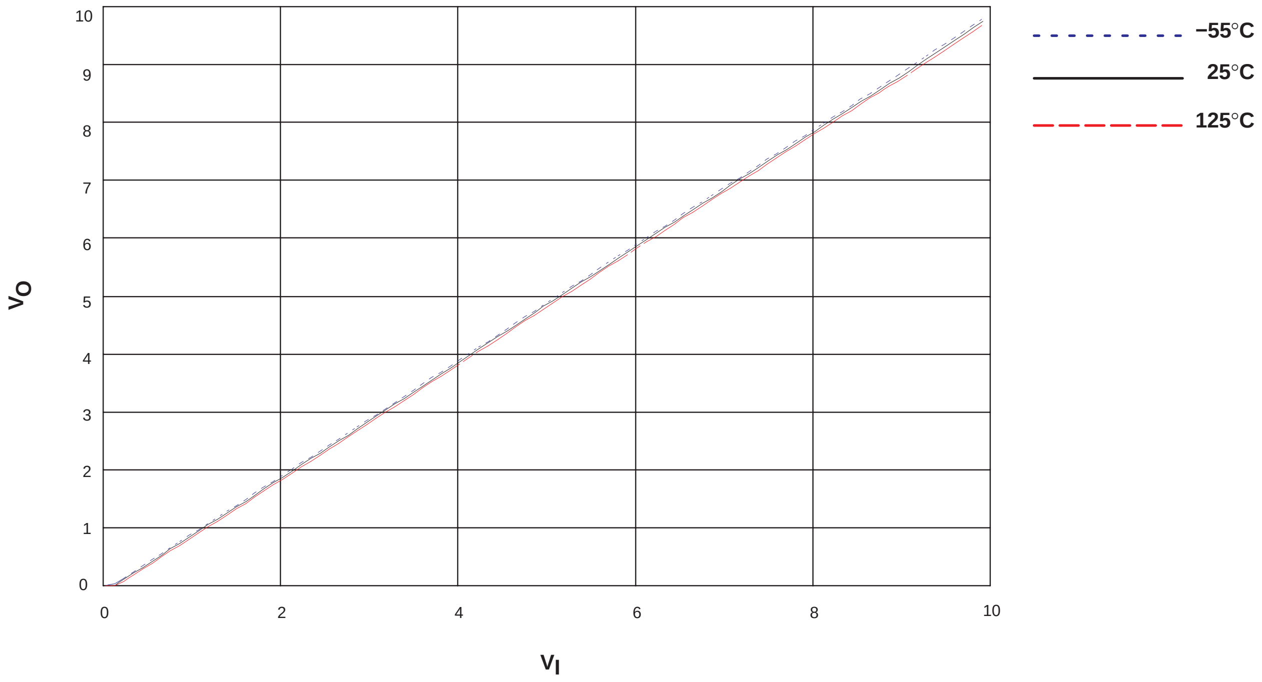


Figure 26. V_O vs V_I, V_{CC} = 10 V (CD4066B)

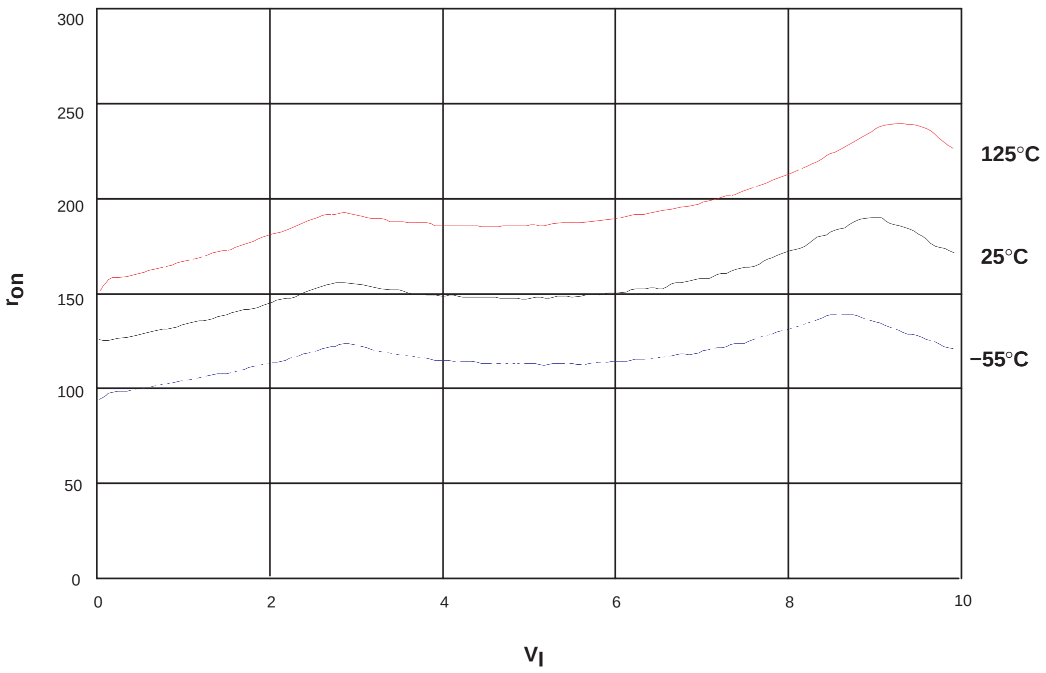


Figure 27. r_{on} vs V_I, V_{CC} = 10 V (CD4066B)

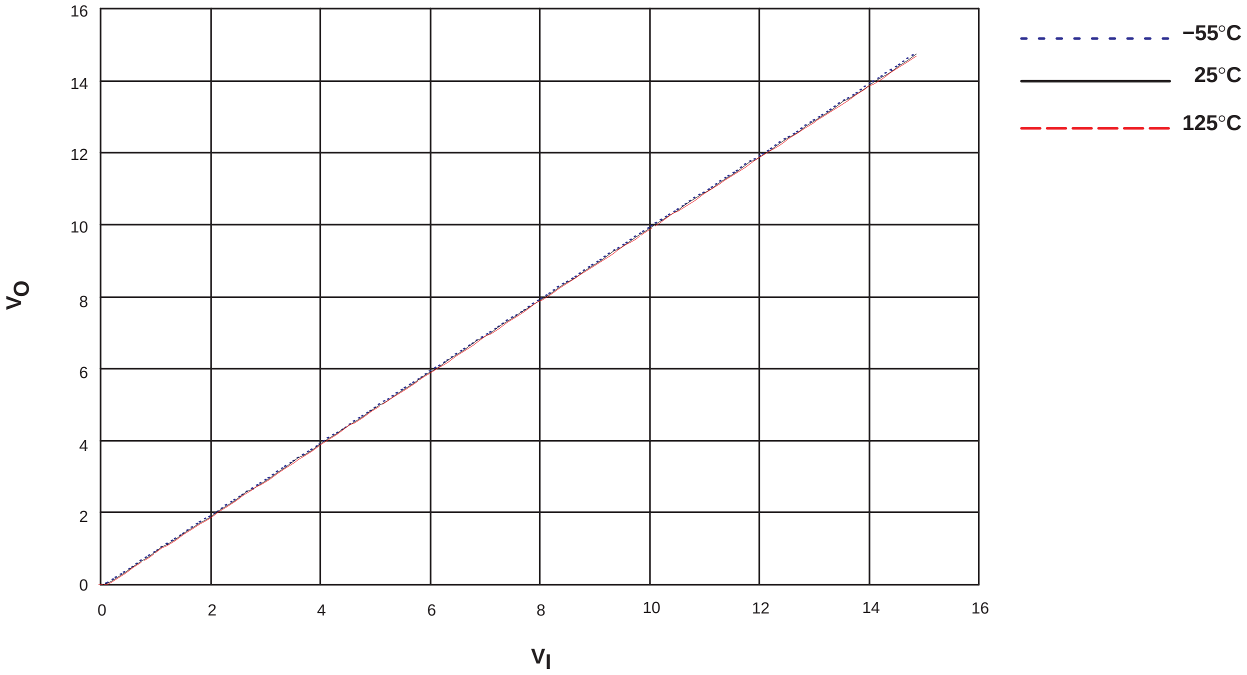


Figure 28. V_O vs V_I, V_{CC} = 15 V (CD4066B)

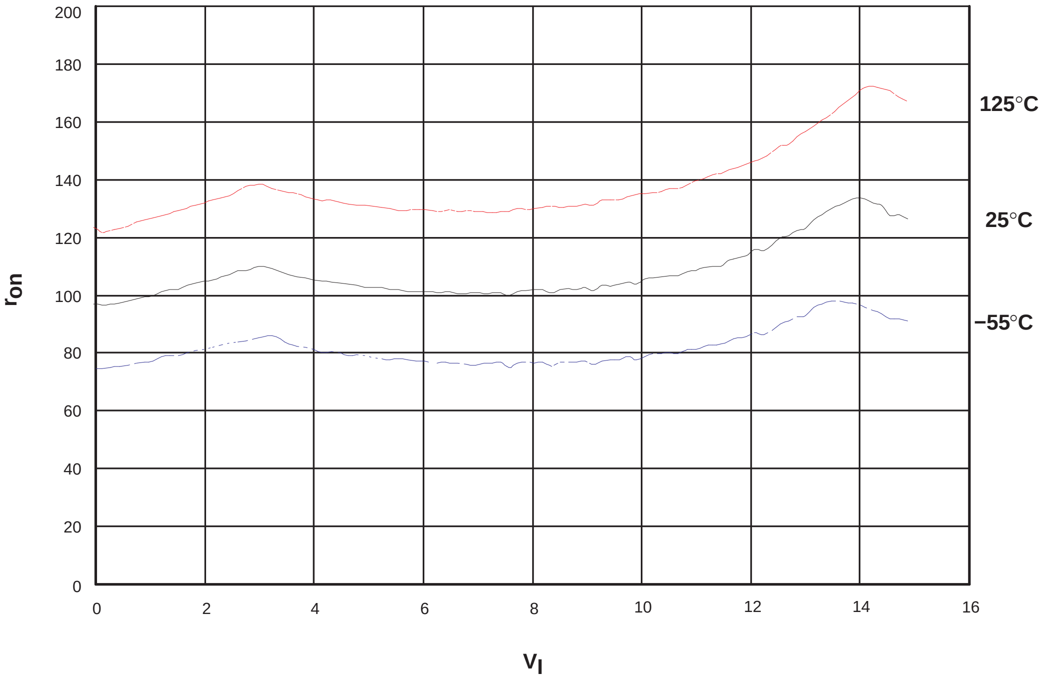


Figure 29. r_{on} vs V_I, V_{CC} = 15 V (CD4066B)

Table 11. CD4066B Analog Parameter Measurement Data[†]

V_{CC}/V_{SS}	Frequency Response	Total Harmonic Distortion	Crosstalk		Charge Injection[‡]	Feedthrough
		1 kHz	Between Switches	Enable to Output		
5 V/−5 V	40 MHz	0.04%	−50 dB at 8 MHz	50 mV		−50 dB at 1 MHz
10 V/0 V	141 MHz[‡]	0.032%[‡]	−75 dB[‡]	35 mV[‡]	18.8 pC	−65 dB[‡]

[†] Data-sheet values for CD4066B, except as noted

[‡] Postcharacterization measurement for CD4066B. Frequency response, THD, crosstalk, and feedthrough measured using load conditions specified in Appendix A, in order to make a more valid comparison with other devices in this report.

2.4.10 LV-A Characteristics

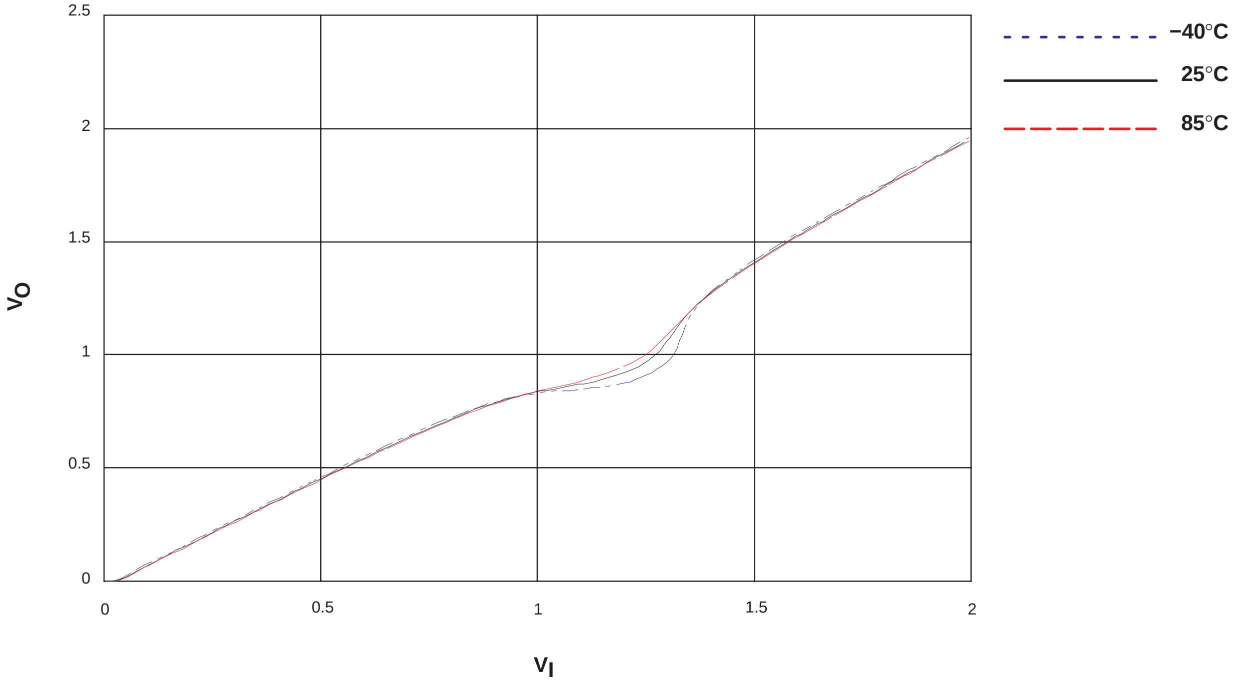


Figure 30. V_O vs V_I, V_{CC} = 2 V (SN74LV4066A)

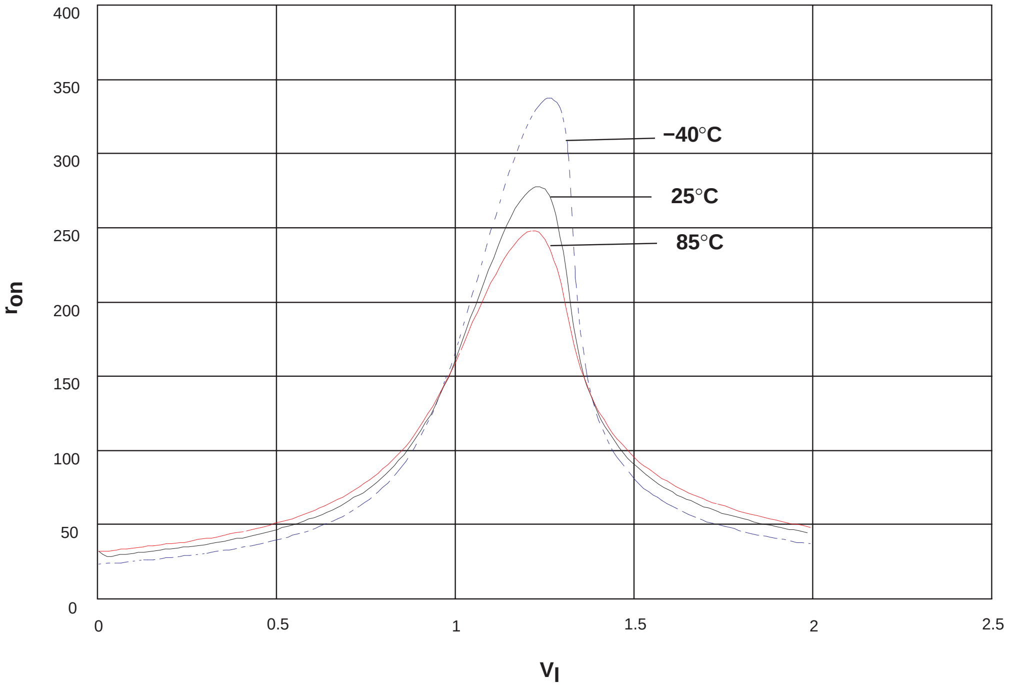


Figure 31. r_{on} vs V_I, V_{CC} = 2 V (SN74LV4066A)

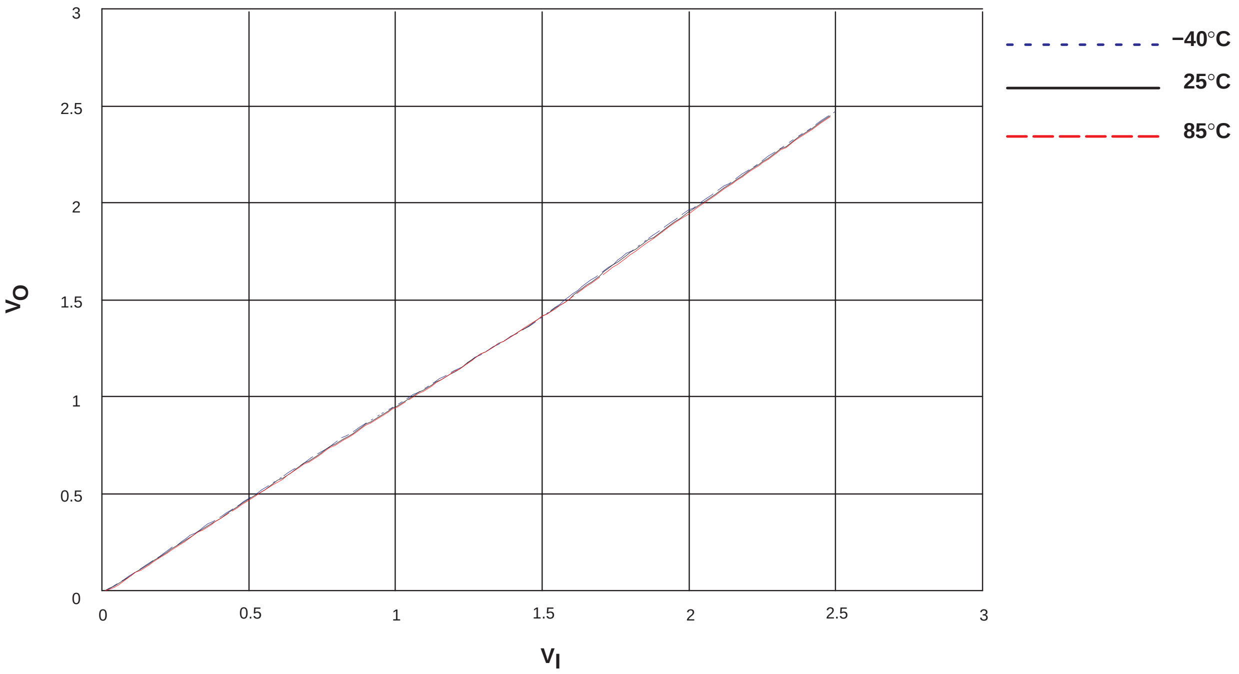


Figure 32. V_O vs V_I, V_{CC} = 2.5 V (SN74LV4066A)

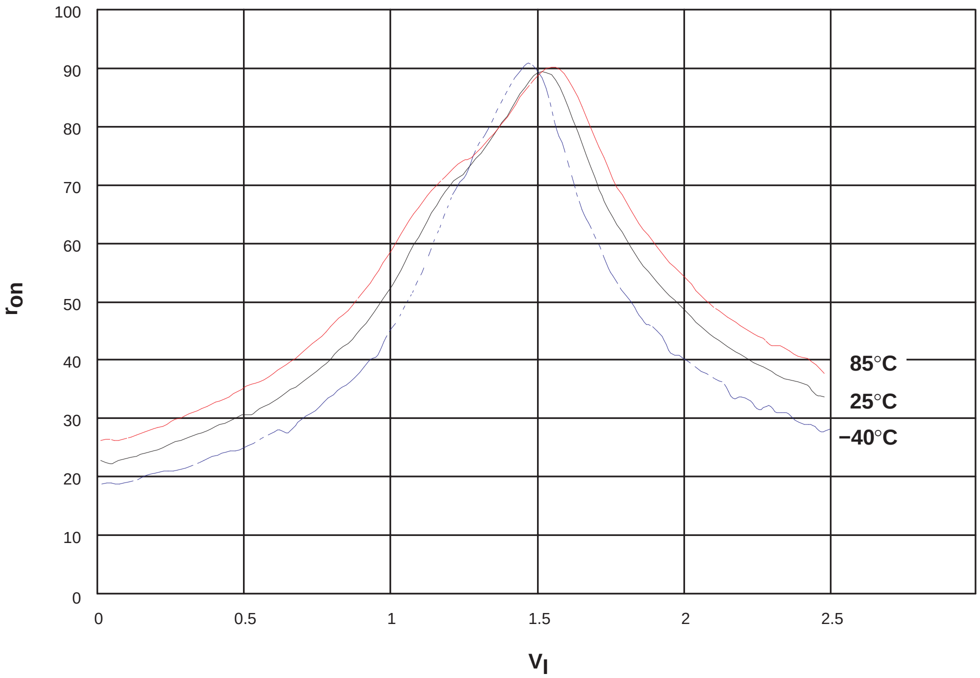


Figure 33. r_{on} vs V_I, V_{CC} = 2.5 V (SN74LV4066A)

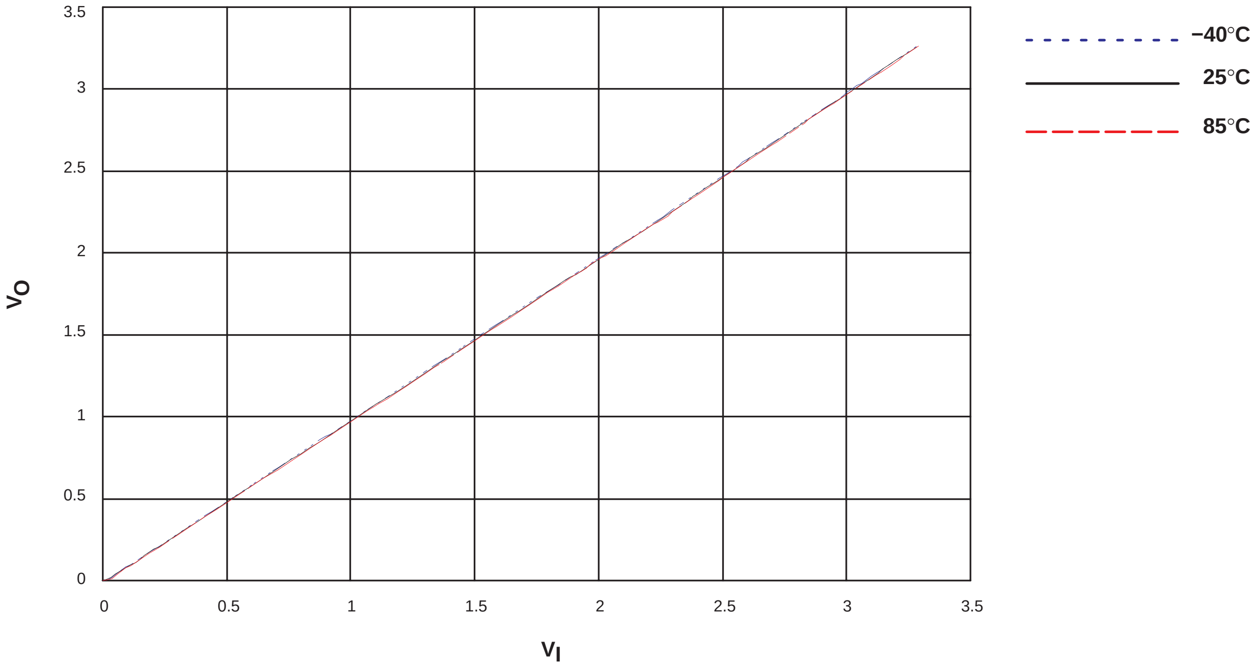


Figure 34. V_O vs V_I, V_{CC} = 3.3 V (SN74LV4066A)

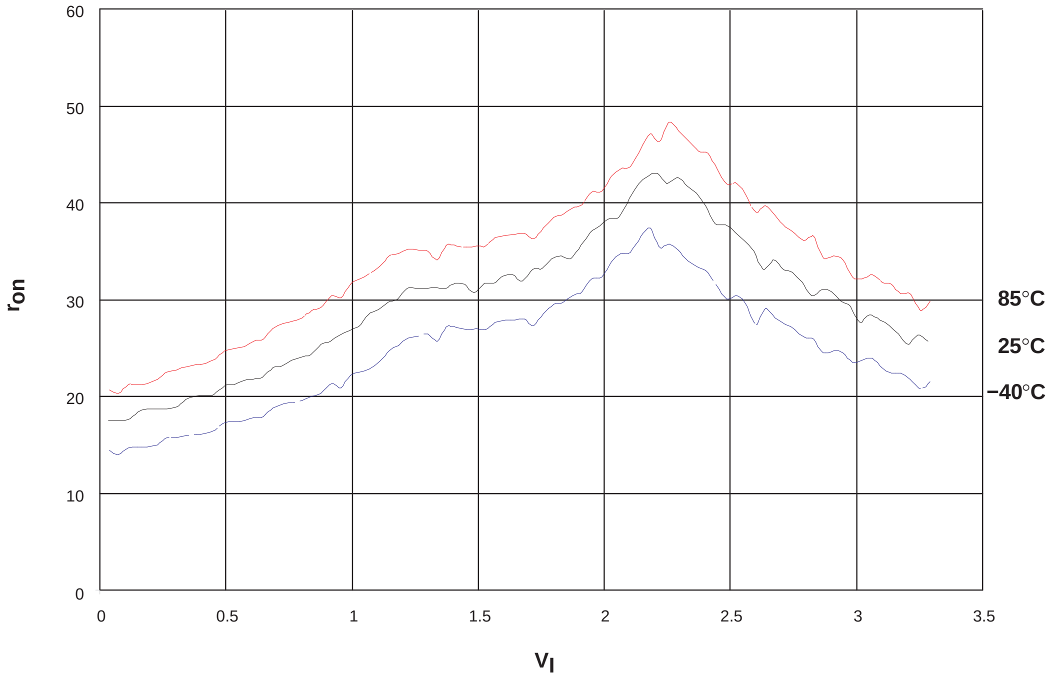


Figure 35. r_{on} vs V_I, V_{CC} = 3.3 V (SN74LV4066A)

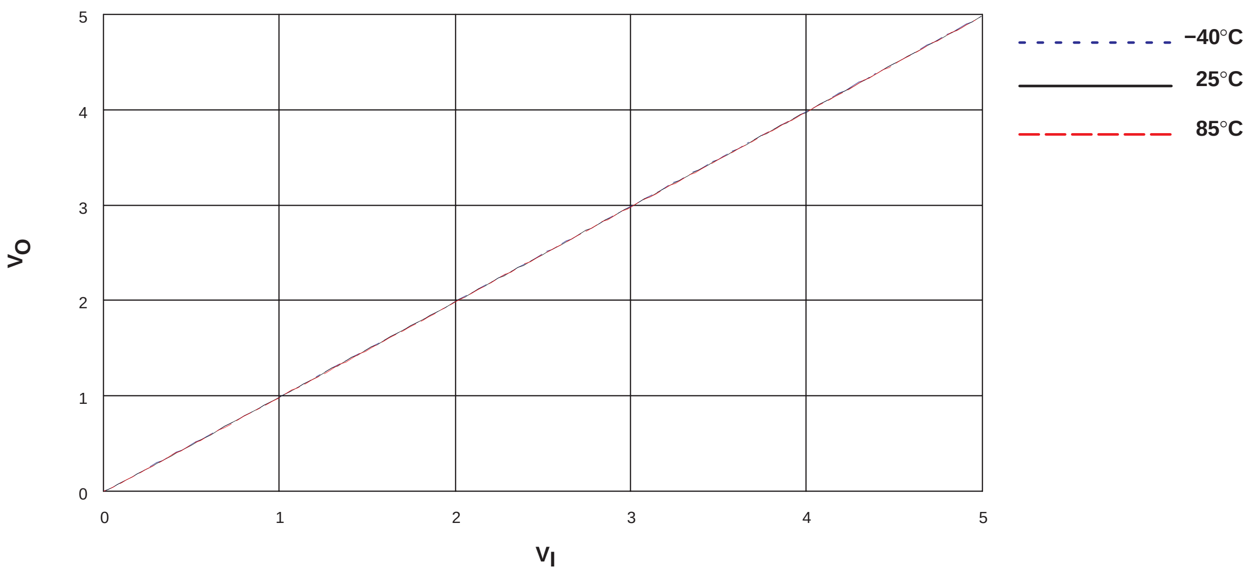


Figure 36. V_O vs V_I, V_{CC} = 5 V (SN74LV4066A)

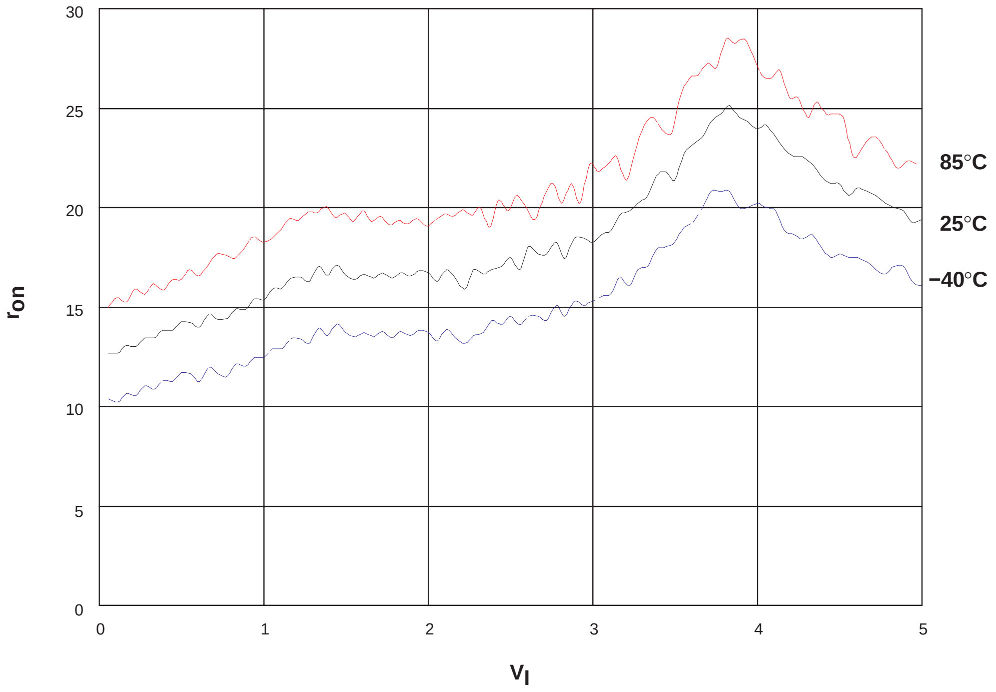


Figure 37. r_{on} vs V_I, V_{CC} = 5 V (SN74LV4066A)

Table 12. SN74LV4066A Analog Parameter Measurement Data[†]

V_{CC}	Frequency Response	Sine-Wave Distortion	Crosstalk		Charge Injection[‡]	Feedthrough
		1 kHz	Between Switches	Enable to Output		
2.3 V	30 MHz	0.1%	−45 dB	15 mV	2.1 pC	−40 dB
3 V	35 MHz	0.1%	−45 dB	20 mV	2.7 pC	−40 dB
4.5 V	50 MHz	0.1%	−45 dB	50 mV	3.0 pC	−40 dB

[†] Data-sheet values for SN74LV4066A, except as noted

[‡] Postcharacterization measurement for SN74LV4066A

2.4.11 LVC Characteristics

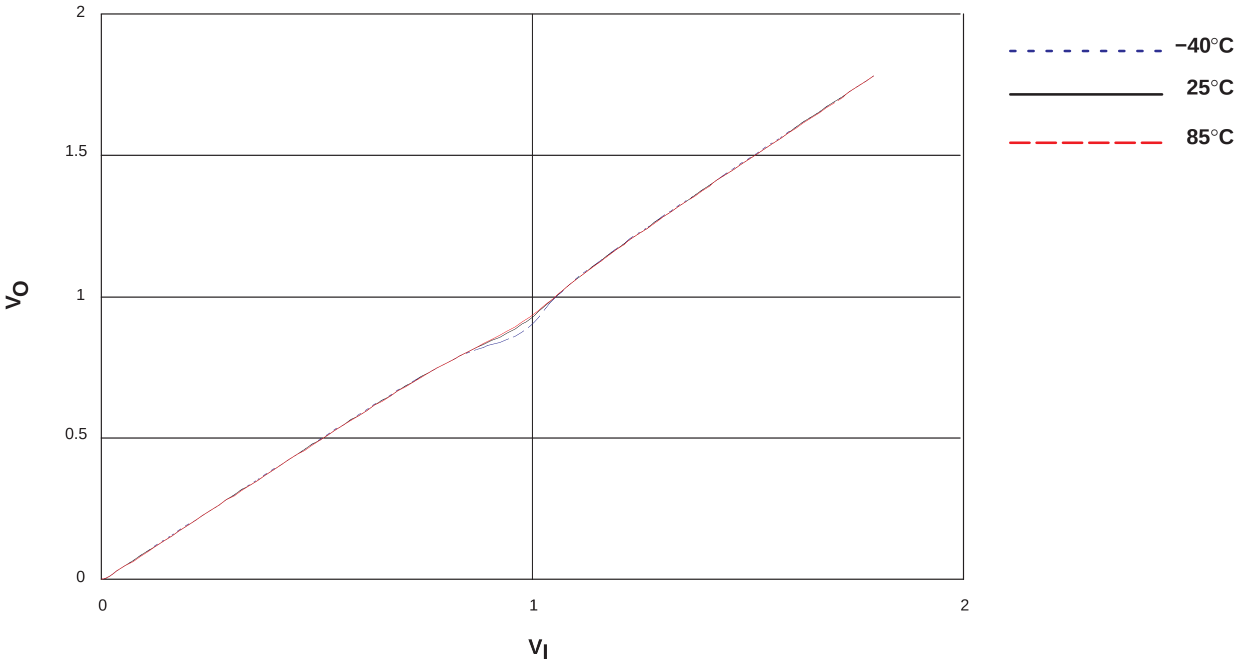


Figure 38. V_O vs V_I, V_{CC} = 1.8 V (SN74LVC1G66)

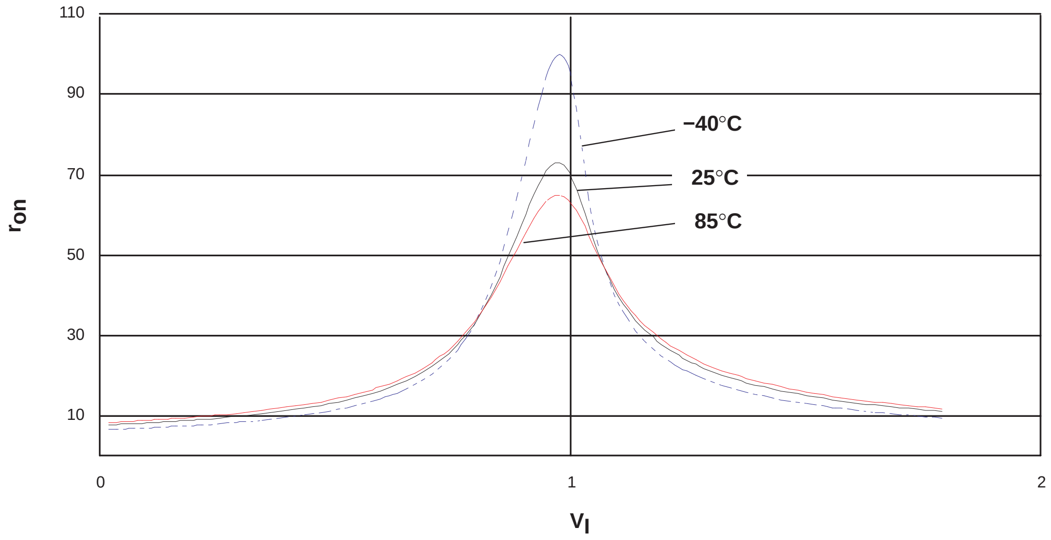


Figure 39. r_{on} vs V_I, V_{CC} = 1.8 V (SN74LVC1G66)

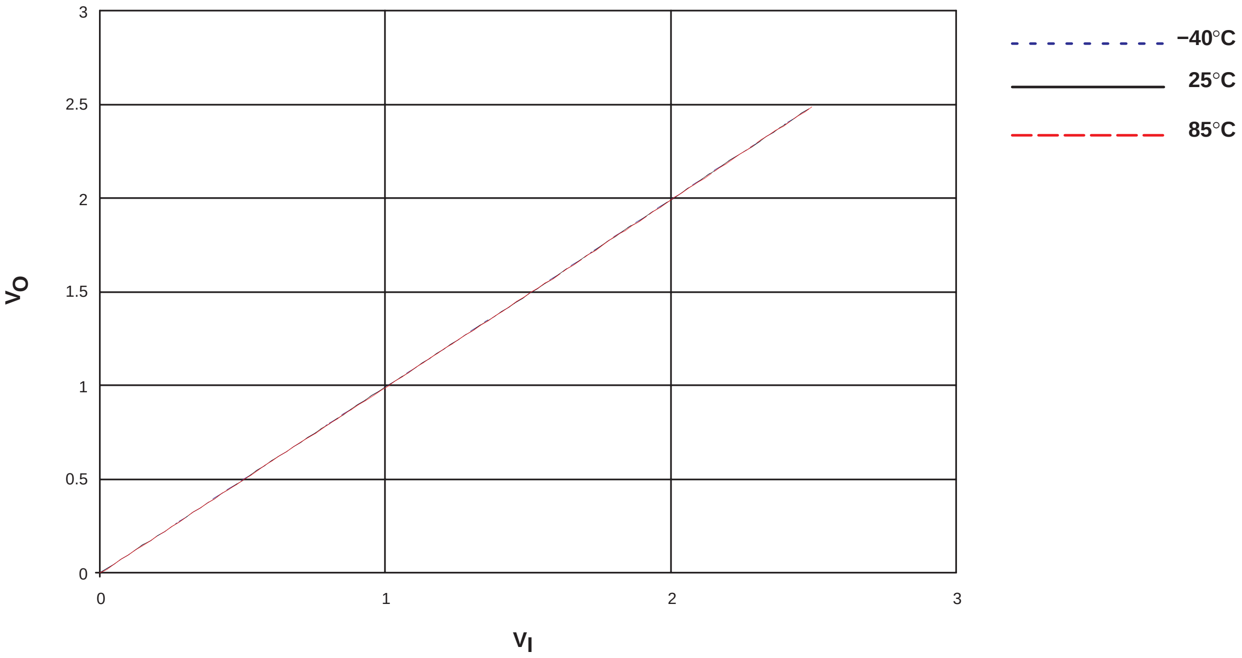


Figure 40. V_O vs V_I, V_{CC} = 2.5 V (SN74LVC1G66)

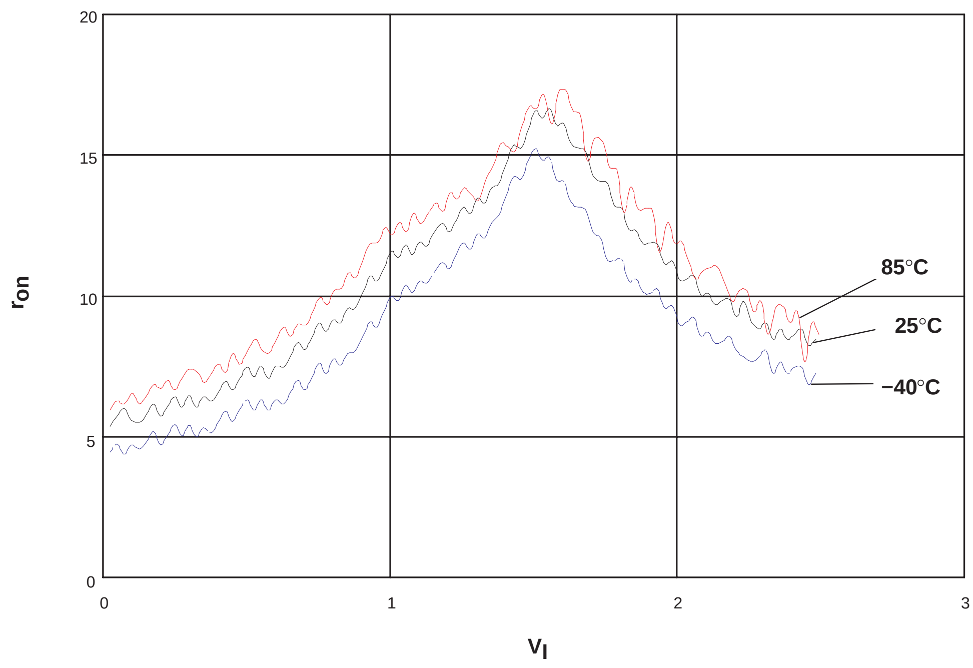


Figure 41. r_{on} vs V_I, V_{CC} = 2.5 V (SN74LVC1G66)

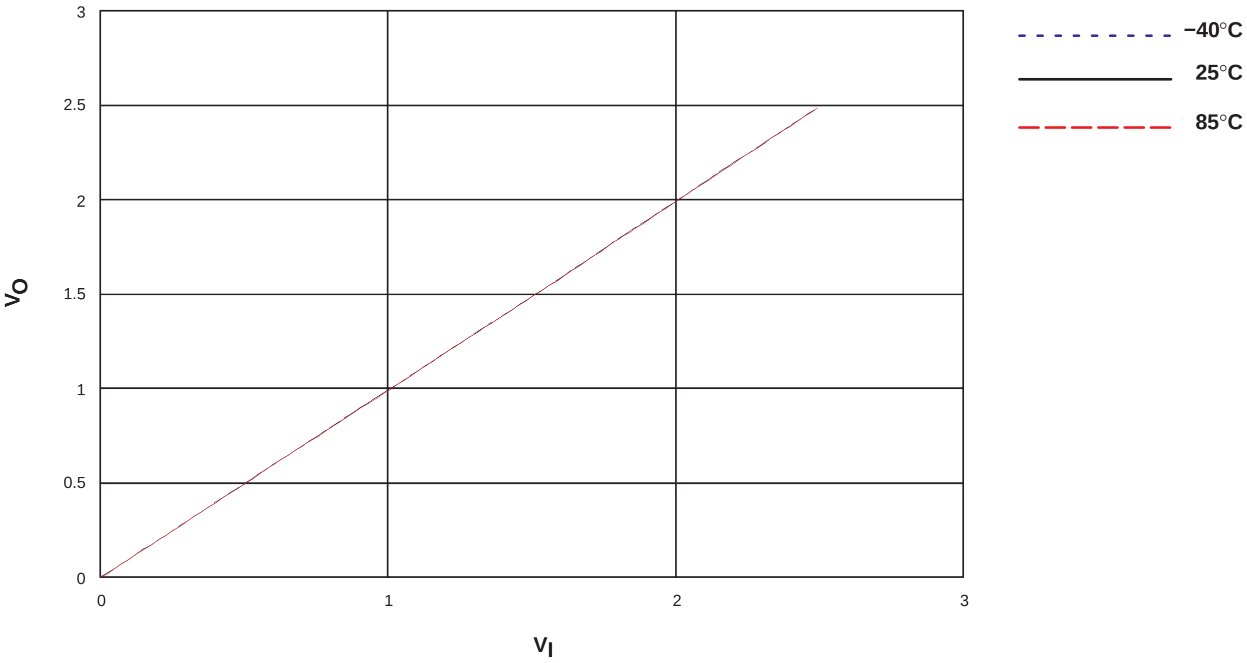


Figure 42. V_O vs V_I, V_{CC} = 3.3 V (SN74LVC1G66)

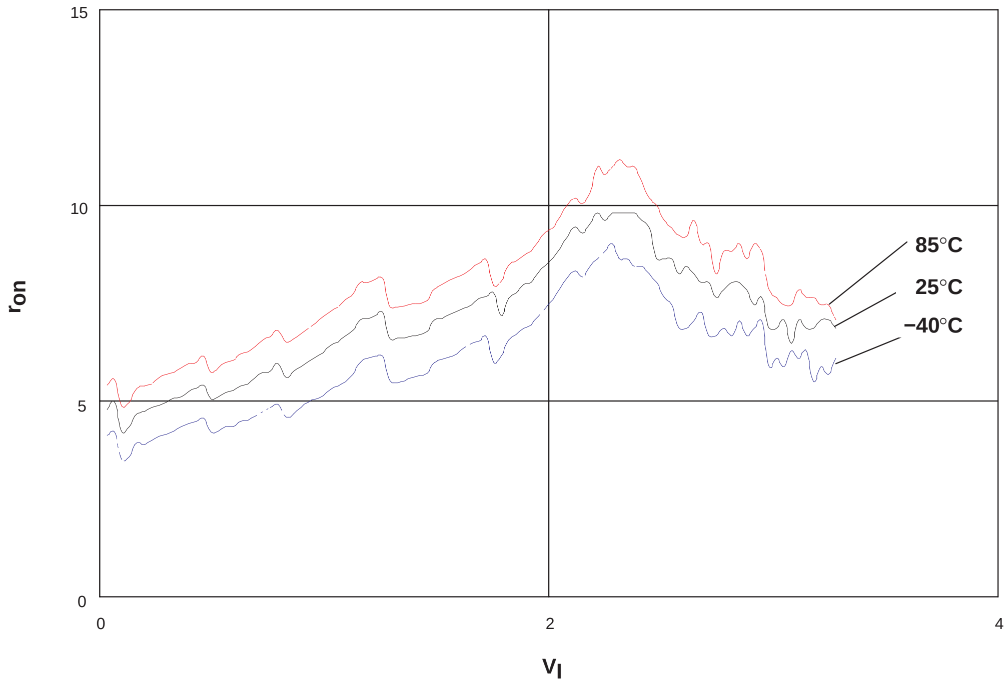


Figure 43. r_{on} vs V_I, V_{CC} = 3.3 V (SN74LVC1G66)

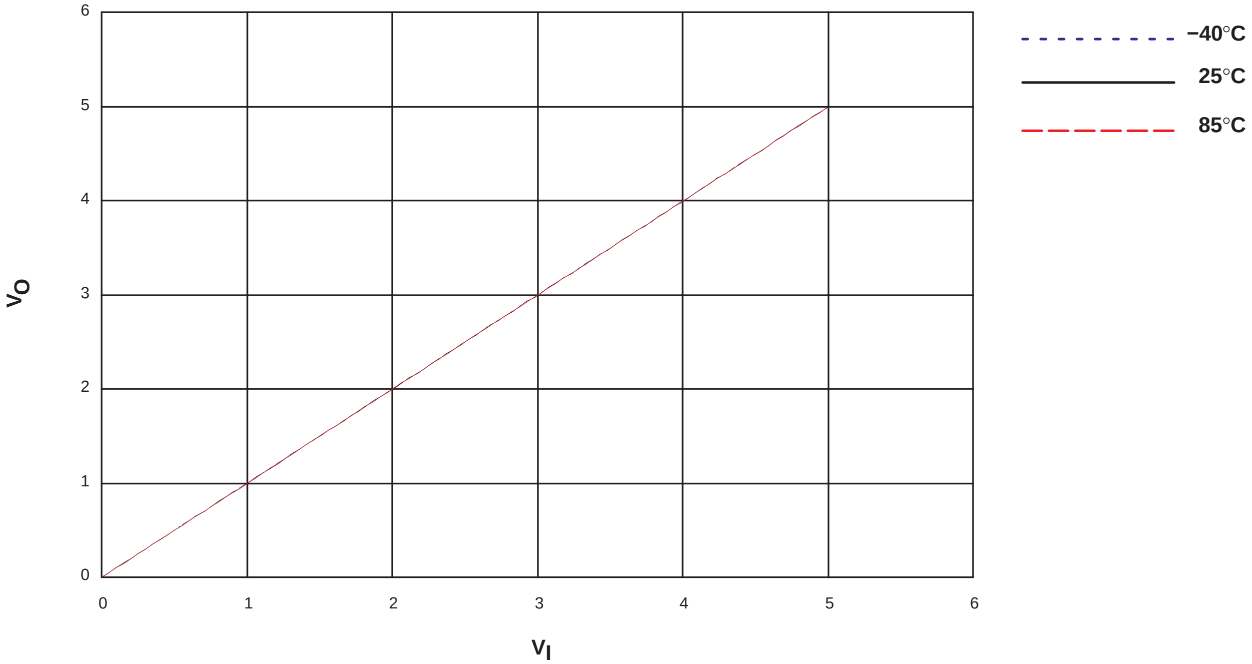


Figure 44. V_O vs V_I, V_{CC} = 5 V (SN74LVC1G66)

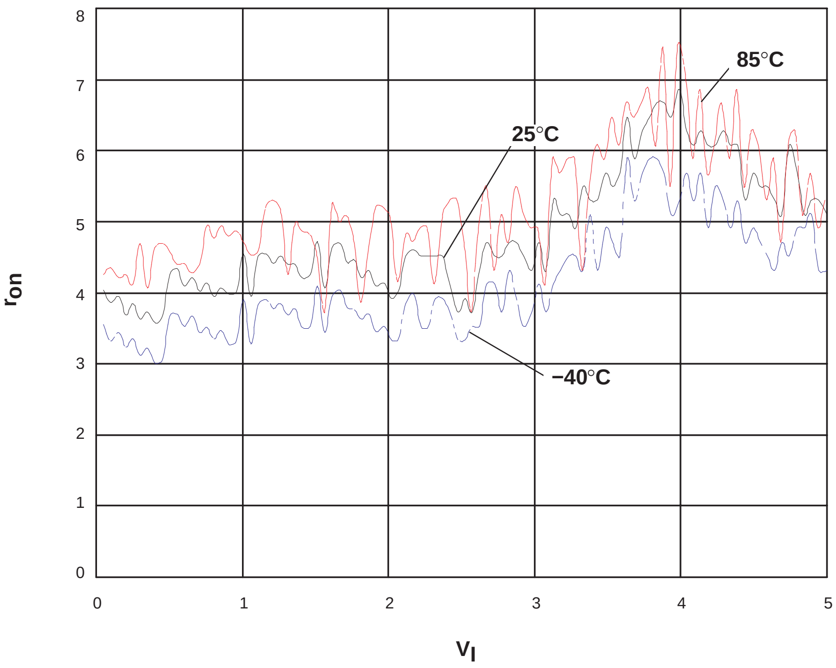


Figure 45. r_{on} vs V_I, V_{CC} = 5 V (SN74LVC1G66)

Table 13. SN74LVC1G66 Analog Parameter Measurement Data†

V_{CC}	Frequency Response	Sine-Wave Distortion		Crosstalk Enable to Output	Charge Injection‡	Feedthrough
		1 kHz	10 kHz			
1.8 V	35 MHz	0.1%	0.15%	35 mV	2.5 pC	−42 dB
2.5 V	120 MHz	0.025%	0.025%	50 mV	3.0 pC	−42 dB
3 V	175 MHz	0.015%	0.015%	70 mV	3.3 pC	−42 dB
4.5 V	195 MHz	0.01%	0.01%	100 mV	3.5 pC	−42 dB

† Data-sheet values for SN74LVC1G66, except as noted

‡ Postcharacterization measurement for SN74LVC1G66

2.4.12 CBTLV Characteristics

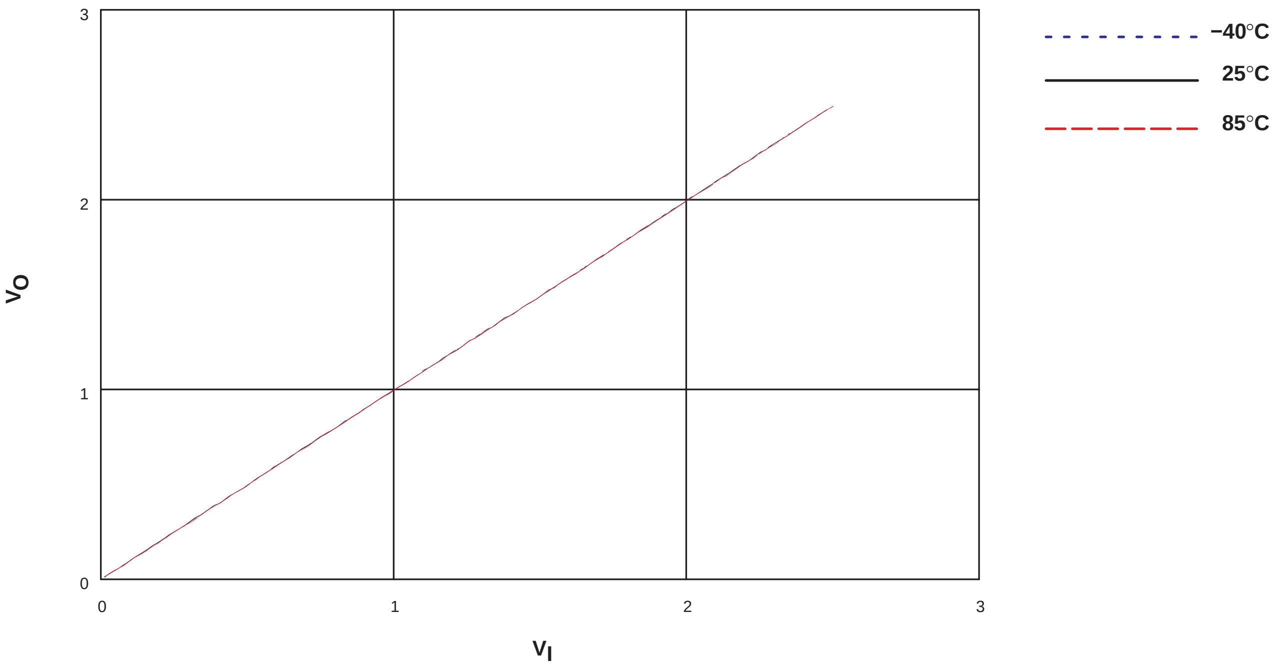


Figure 46. V_O vs V_I, V_{CC} = 2.5 V (SN74CBTLV3125)

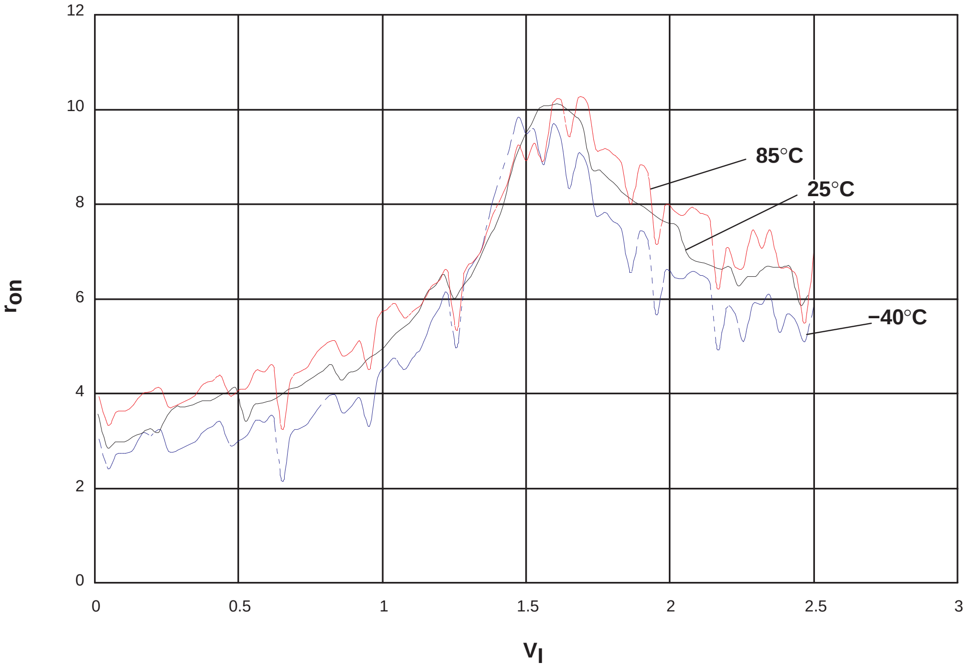


Figure 47. r_{on} vs V_I, V_{CC} = 2.5 V (SN74CBTLV3125)

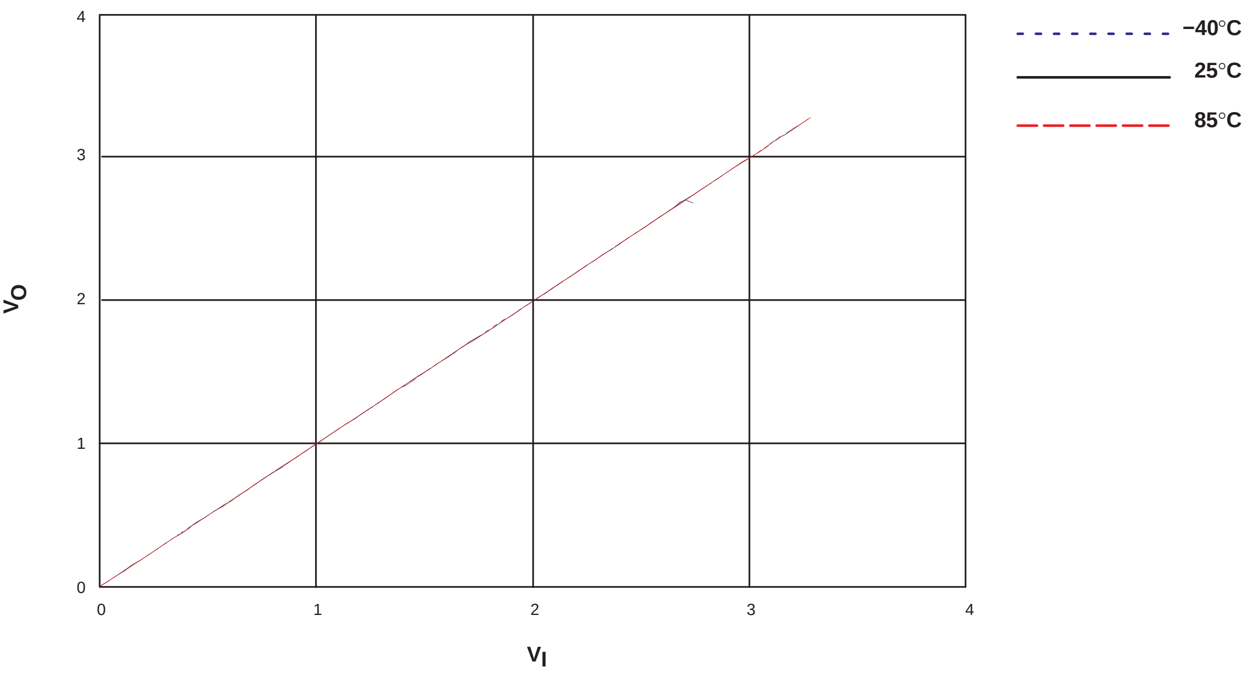


Figure 48. V_O vs V_I, V_{CC} = 3.3 V (SN74CBTLV3125)

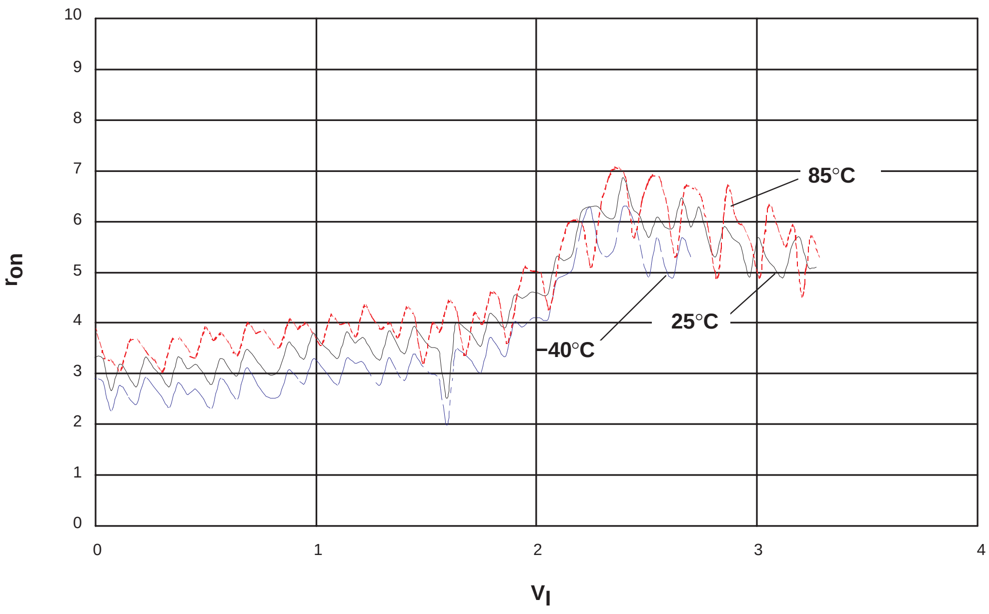


Figure 49. r_{on} vs V_I, V_{CC} = 3.3 V (SN74CBTLV3125)

Table 14. SN74CBTLV3125 Analog Parameter Measurement Data[†]

V_{CC}	Frequency Response	Sine-Wave Distortion	Total Harmonic Distortion	Crosstalk		Charge Injection	Feedthrough
		1 kHz	1 kHz	Between Switches	Enable to Output		
2.5 V	>200 MHz	0.089%	0.11%	−45 dB	30 mV	12.1 pC	−52 dB
3.3 V	>200 MHz	0.033%	0.09%	−49 dB	70 mV	15.5 pC	−52 dB

[†] Postcharacterization measurement for CBTLV3125

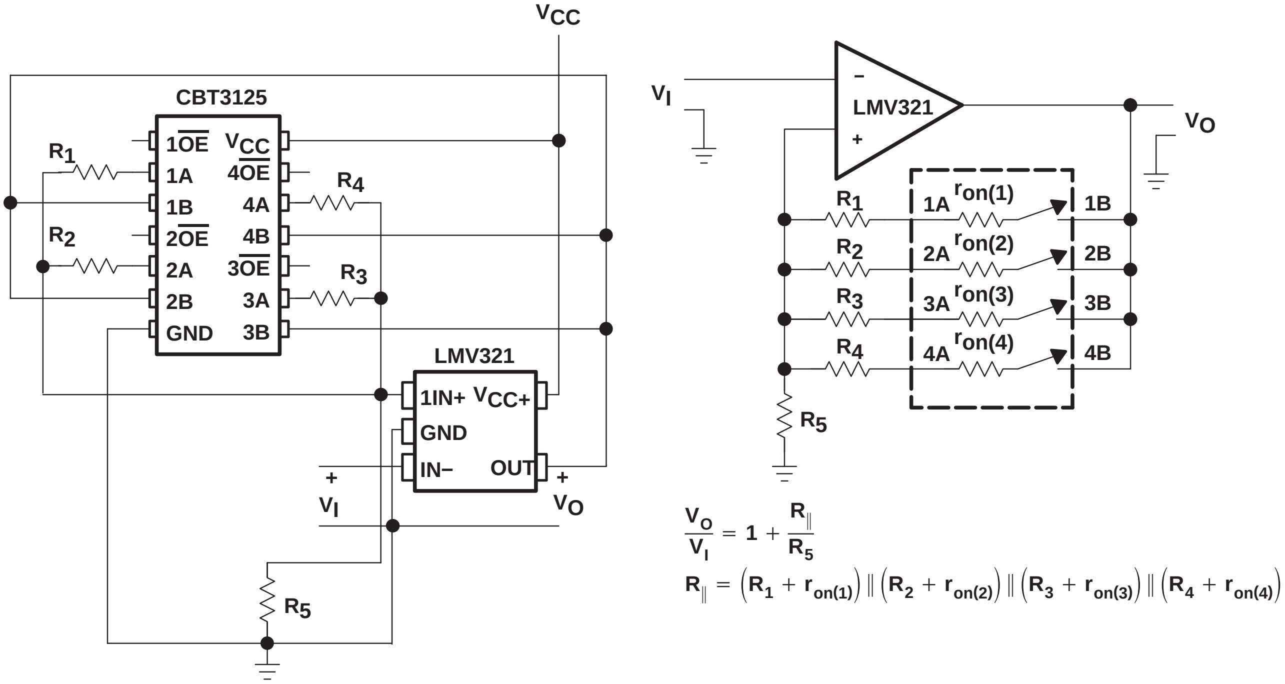
3 Applications

TI signal switches can be configured for numerous applications. Three switches are presented here for illustrative purposes:

- A bus switch in an analog application (digital switch in an analog application)
- Improvement of off-isolation characteristics with a T configuration
- Single-bit level shifting with an analog switch (analog switch in a digital application)

3.1 CBT3125 as a Gain-Control Circuit [for $V_I < (V_{CC} - 2\ V)$] With LMV321

An example of the CBT3125 in a gain-control circuit is shown in Figure 50.


VCC
CBT3125
1OE
VCC
1A
4OE
1B
4A
2OE
4B
2A
3OE
2B
3A
GND
3B
R1
R2
R3
R4
R5
LMV321
1IN+
VCC+
GND
IN−
OUT
+
VI
+
VO
VI
−
LMV321
+
VO
R1
R2
R3
R4
R5
1A
2A
3A
4A
ron(1)
ron(2)
ron(3)
ron(4)
1B
2B
3B
4B

$$\frac{V_O}{V_I} = 1 + \frac{R_{\parallel}}{R_5}$$

$$R_{\parallel} = \left(R_1 + r_{on(1)}\right) \parallel \left(R_2 + r_{on(2)}\right) \parallel \left(R_3 + r_{on(3)}\right) \parallel \left(R_4 + r_{on(4)}\right)$$

Figure 50. CBT3125 Gain-Control Circuit

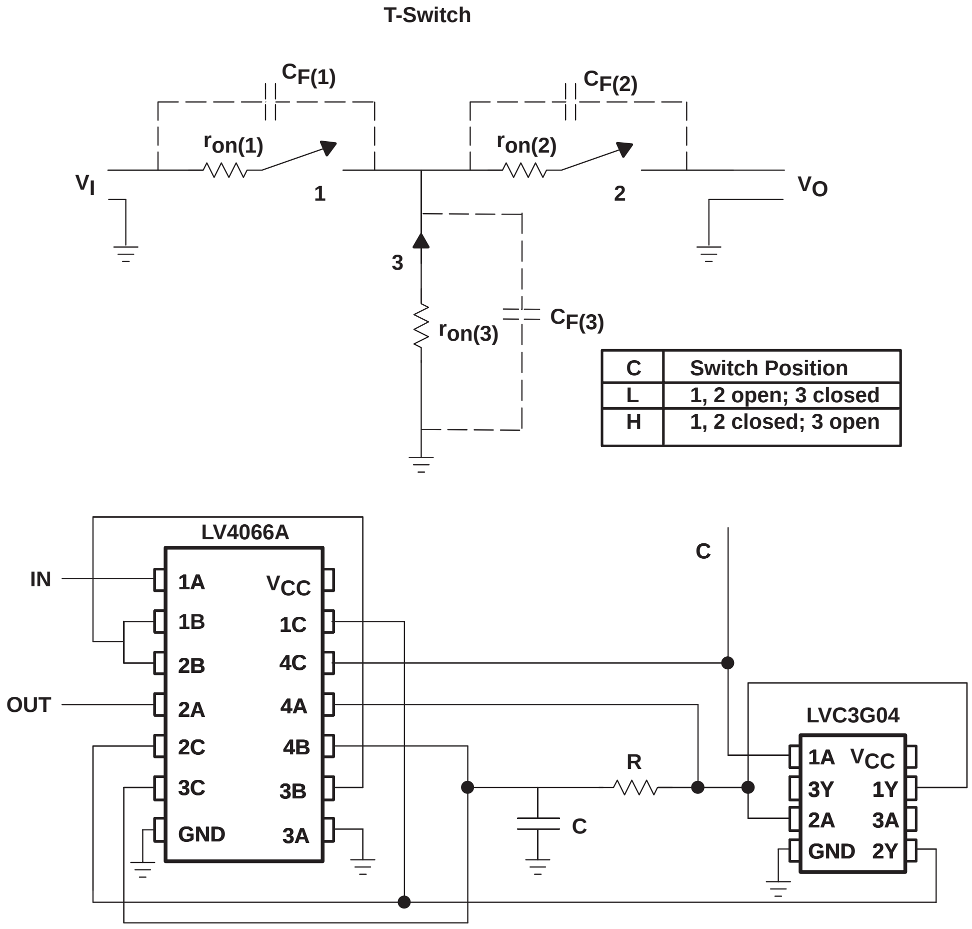
By choosing values for R_1 through R_4, such that $R_X >> r_{on(x)}$, the on-state resistance of the CBT3125 can be ignored. Thus, R_{II} simplifies to:

$$R_{II} = R_1 \text{ II } R_2 \text{ II } R_3 \text{ II } R_4$$

Because the CBT device uses 5-V TTL switching levels, it can be controlled easily from either CMOS or TT logic.

3.2 LVC4066A T-Switch

The series connection doubles the effective switch r_{on} when passing signals, but the tradeoff is improved off isolation—a key concern when passing high-frequency signals. Feedthrough attenuation for the LV4066A is specified as –40 dB using a single switch. However, when connected in a T configuration as shown in Figure 51, isolation in excess of −65 dB was measured using a 5-V V_{CC}.


T-Switch

$C_{F(1)}$
$C_{F(2)}$
$r_{on(1)}$
$r_{on(2)}$
V_I
1
2
V_O
3
$r_{on(3)}$
$C_{F(3)}$
LV4066A
IN
OUT
1A
1B
2B
2A
2C
3C
GND
V_{CC}
1C
4C
4A
4B
3B
3A
C
R
C
LVC3G04
1A
3Y
2A
GND
V_{CC}
1Y
3A
2Y

C	Switch Position
L	1, 2 open; 3 closed
H	1, 2 closed; 3 open

Figure 51. LV4066A/LVC2G04 T-Switch Configuration

The values of R and C (including PCB resistance and capacitance) are chosen such that the R || $r_{on(4)}$ × C time constant is faster than the propagation delay through the inverter. This allows switch 3 to open before switches 1 and 2 close. Conversely, the R × C time constant slows the transition of the control signal to switch 3, allowing switches 1 and 2 to open before switch 3 closes.

3.3 LVC1G66 TTL-to-LVTTL Level Shifter

The LVC1G66 can be used for simple translation from 5-V TTL levels to LVTTL (see Figure 52). The control pin is tolerant to 5.5 V and, with a maximum r_{on} at V_{CC} = 3.3 V of 15 Ω, the voltage drop across the switch is only 0.36 V with 24 mA of through current.

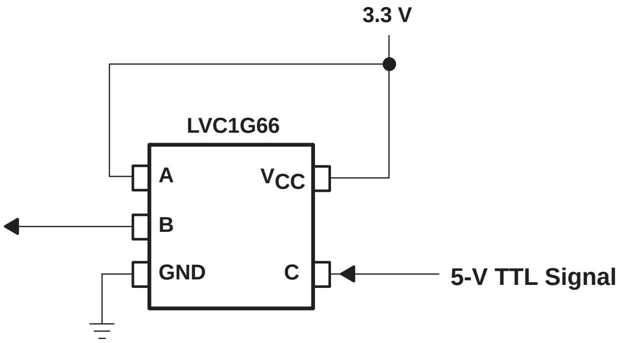


Figure 52. LVC1G66 TTL-to-LVTTL Level Shifter

4 Conclusion

Factors that go into selecting a signal switch can be numerous (analog, digital, V_{CC}, t_{en}/t_{dis}, etc.). This application report has presented the various TI signal-switch technologies (CBT, CBTLV, CD4000, HC, HCT, LV-A, and LVC), explained TI switch nomenclature, and provided example applications of switches to aid the designer in selecting the right TI signal switch.

Appendix A Test Circuits

A.1 r_{on} Measurement

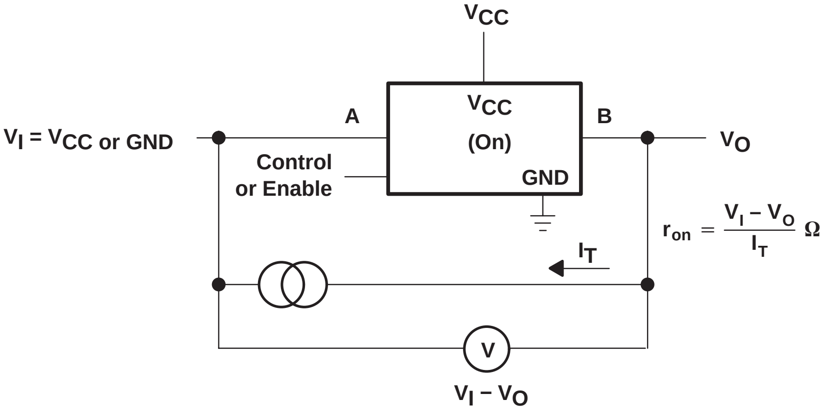

V_{CC}
A
V_{CC}
(On)
B
$V_I = V_{CC}$ or GND
V_O
Control
or Enable
GND
$r_{on} = \frac{V_I - V_O}{I_T}\ \Omega$
I_T
V
$V_I - V_O$

Figure A−1. r_{on} Test Circuit

A.2 V_O vs V_I Measurement

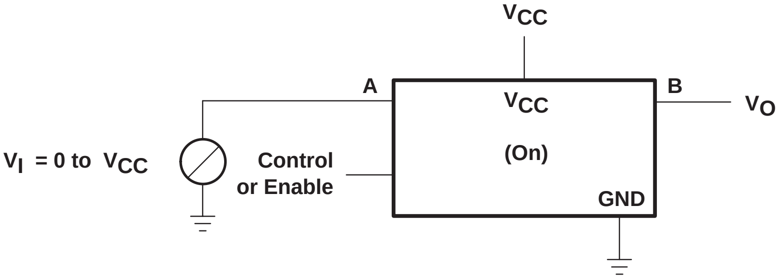
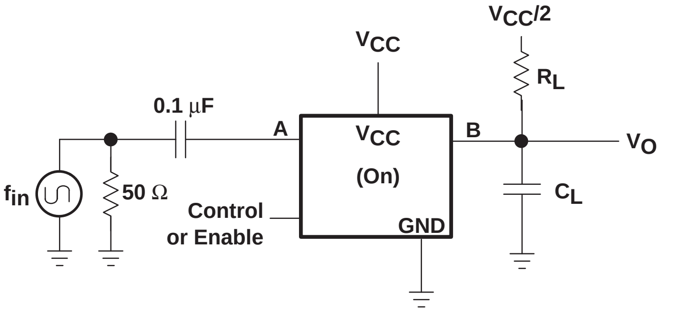

V_{CC}
A
V_{CC}
B
V_O
(On)
V_I = 0 to V_{CC}
Control
or Enable
GND

Figure A−2. V_O vs V_I Test Circuit

A.3 Frequency-Response Measurement

DEVICE	R_L	C_L
SN74CBT3125	600 Ω	50 pF
CD74HCT4066	50 Ω	10 pF
CD74HC4066	50 Ω	10 pF
SN74HC4066	600 Ω	50 pF
CD4066B†	1 kΩ	–
CD4066B‡	600 Ω	50 pF
SN74LV4066A	600 Ω	50 pF
SN74LVC1G66	600 Ω	50 pF
SN74CBTLV3125	600 Ω	50 pF

† Data-sheet load
‡ Application-report load



$V_{CC}/2$
V_{CC}
R_L
0.1 μF
A
V_{CC}
(On)
B
V_O
f_{in}
50 Ω
Control or Enable
GND
C_L

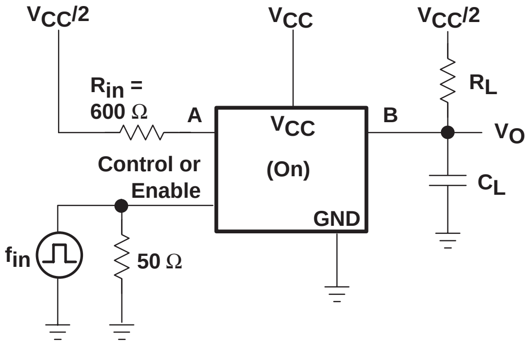
Adjust f_{in} to obtain 0 dBm at output. Increase f_{in} until dB meter reads −3 dB.

Figure A−3. Frequency-Response Test Circuit

A.4 Crosstalk Measurement

DEVICE	R_L	C_L
SN74CBT3125	600 Ω	50 pF
CD74HCT4066	600 Ω	50 pF
CD74HC4066	600 Ω	50 pF
SN74HC4066	600 Ω	50 pF
CD4066B†	10 kΩ	–
CD4066B‡	600 Ω	50 pF
SN74LV4066A	600 Ω	50 pF
SN74LVC1G66	600 Ω	50 pF
SN74CBTLV3125	600 Ω	50 pF

† Data-sheet load
‡ Application-report load



$V_{CC}/2$
V_{CC}
$V_{CC}/2$
R_{in} = 600 Ω
A
V_{CC}
(On)
B
R_L
V_O
Control or Enable
GND
C_L
f_{in}
50 Ω

f_{in} = 1 MHz (square wave)

Figure A−4. Crosstalk (Switch Control to Output) Test Circuit

A.5 Charge-Injection Measurement

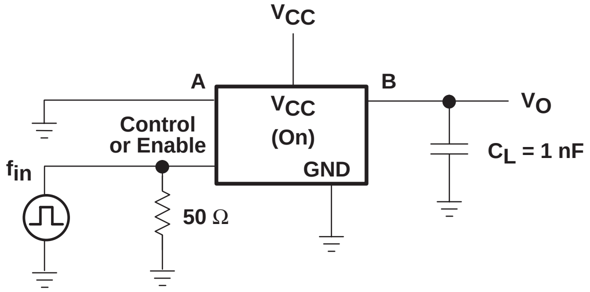
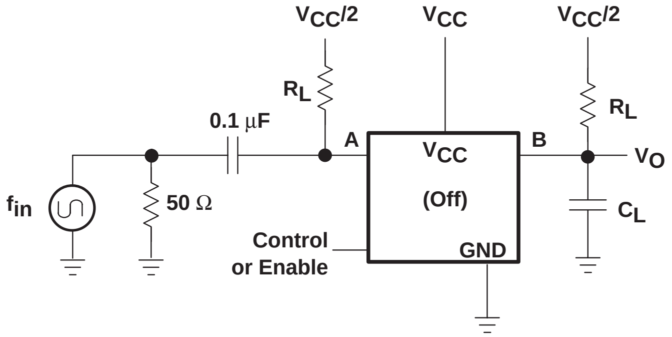

V_{CC}
A
B
V_{CC}
(On)
GND
V_O
Control
or Enable
C_L = 1 nF
f_{in}
50 Ω

Figure A−5. Charge-Injection Test Circuit

A.6 Feedthrough Measurement

DEVICE	R_L	C_L
SN74CBT3125	600 Ω	50 pF
CD74HCT4066	50 Ω	10 pF
CD74HC4066	50 Ω	10 pF
SN74HC4066	600 Ω	50 pF
CD4066B†	1 kΩ	–
CD4066B‡	600 Ω	50 pF
SN74LV4066A	600 Ω	50 pF
SN74LVC1G66	600 Ω	50 pF
SN74CBTLV3125	600 Ω	50 pF

† Data-sheet load
‡ Application-report load


$V_{CC}/2$
V_{CC}
$V_{CC}/2$
R_L
R_L
0.1 µF
A
B
V_{CC}
V_O
f_{in}
50 Ω
(Off)
C_L
Control
or Enable
GND

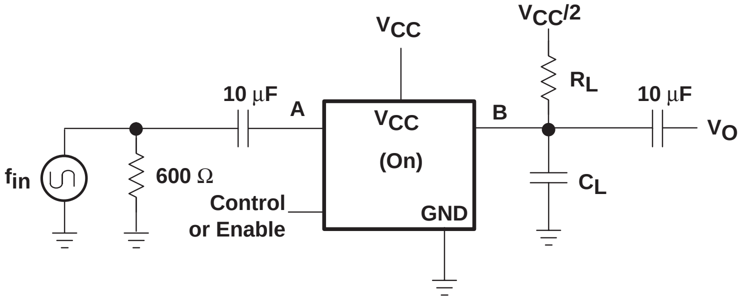
f_{in} = 1 MHz (sine wave)
Adjust f_{in} to obtain 0 dBm at input.

Figure A−6. Feedthrough Test Circuit

A.7 Sine-Wave and Total-Harmonic-Distortion Measurement

DEVICE	R_L	C_L
SN74CBT3125	10 kΩ	50 pF
CD74HCT4066	10 kΩ	50 pF
CD74HC4066	10 kΩ	50 pF
SN74HC4066	10 kΩ	50 pF
CD4066B†	10 kΩ	–
CD4066B‡	10 kΩ	50 pF
SN74LV4066A	10 kΩ	50 pF
SN74LVC1G66	10 kΩ	50 pF
SN74CBTLV3125	10 kΩ	50 pF

† Data-sheet load
‡ Application-report load


V_{CC}
$V_{CC}/2$
R_L
10 μF
A
V_{CC}
(On)
B
10 μF
V_O
f_{in}
600 Ω
Control
or Enable
GND
C_L

f_{in} = 1 kHz (sine wave)

Figure A−7. Sine-Wave and Total-Harmonic-Distortion Test Circuit

A.8 Crosstalk-Between-Switches Measurement

DEVICE	R_L	C_L
SN74CBT3125	600 kΩ	50 pF
CD74HCT4066	50 Ω	10 pF
CD74HC4066	10 kΩ	50 pF
SN74HC4066	600 kΩ	50 pF
CD4066B†	1 kΩ	–
CD4066B‡	600 kΩ	50 pF
SN74LV4066A	600 kΩ	50 pF
SN74LVC2G66	600 kΩ	50 pF
SN74CBTLV3125	600 kΩ	50 pF

† Data-sheet load
‡ Application-report load

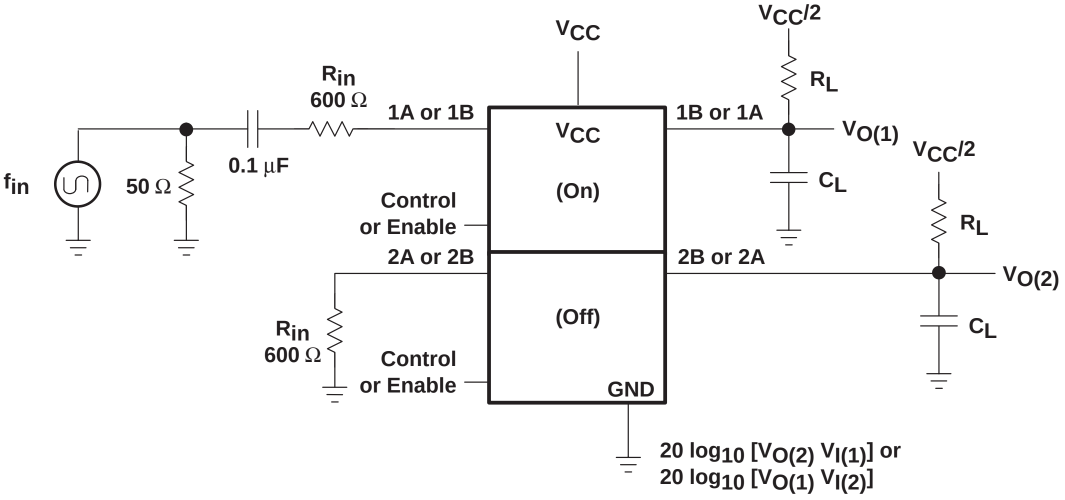

V_{CC}
$V_{CC}/2$
R_{in}
600 Ω
1A or 1B
1B or 1A
R_L
$V_{O(1)}$
V_{CC}
$V_{CC}/2$
0.1 μF
f_{in}
50 Ω
(On)
C_L
Control
or Enable
2A or 2B
2B or 2A
R_L
$V_{O(2)}$
(Off)
R_{in}
600 Ω
C_L
Control
or Enable
GND
20 $\log_{10}$ [$V_{O(2)}$ $V_{I(1)}$] or
20 $\log_{10}$ [$V_{O(1)}$ $V_{I(2)}$]

Figure A−8. Crosstalk-Between-Switches Test Circuit

TEXAS INSTRUMENTS

Application Report

SZZA039 - August 2003

FET Switches in Docking Stations

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ABSTRACT

Docking stations for portable electronics require the capability to connect a system with a live-running bus to a disabled or powered-down system. This hot-docking event must not cause any electrical damage, electrical signal glitches, or data corruption. This application report explains the use of TI FET bus-switch products with precharge to accomplish this connection.

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Introduction

The popularity of mobile electronics is increasing steadily. The use of mobile phone handsets, personal digital assistants (PDAs), laptops, game sets, and other portable devices is ubiquitous. Many of these devices are made more functional by the use of a docking system that allows for connection to power supplies, computers, printers, networks, and other fixed infrastructure.

The design of a docking system for portable electronics usually includes a method for connecting the system in the dock to an actively running high-impedance (reflective-wave switching) bus (for example, PCI bus) in the portable device. Connection of the electronic devices in the docking system, which are powered down or are in a standby state, can cause electrical signal glitches, data corruption, or electrical damage if the system has been designed without regard to certain fundamental criteria. Because of these concerns, typically, FET switch devices are used to enable and disable the connection between the live bus in the portable equipment and the systems in the docking station during docking and removal. This application report explains the recommended procedures and some devices that can be used.

System Considerations

A typical bus in a portable device usually is driven by high-impedance drivers and is not parallel terminated to any power-supply voltage (see Figure 1). This results in quiescent power savings, but causes the bus to be sensitive to changes in the electrical load capacitance.

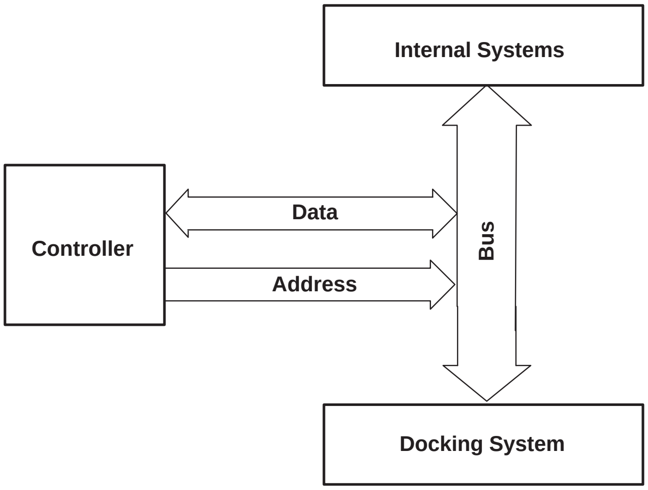

Figure 1. Typical Bus Structure

Connecting a docking system that is powered down or in a standby state can cause a glitch on the bus (see Figure 2).

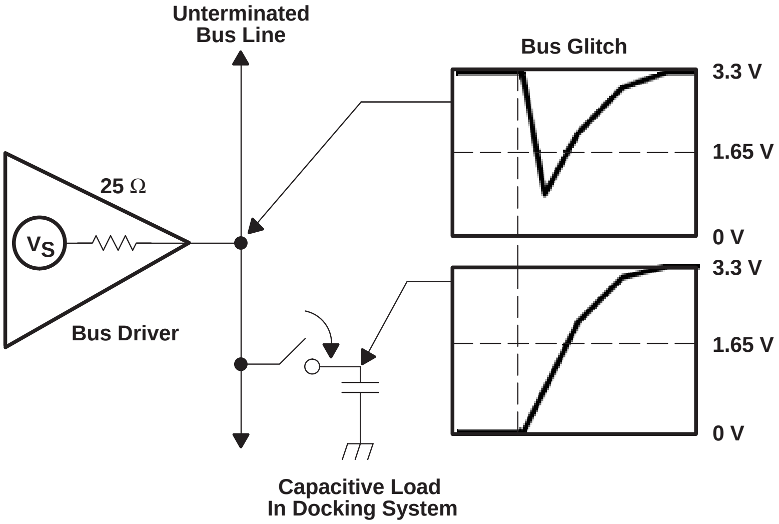

Figure 2. Bus Glitch

The connector pins, PCB traces, and device I/Os in the docking system form a large capacitor that, essentially, is charged to 0 V. If a bus line is at a logic-high level (e.g., 3.3 V) when a low-impedance connection is made to a discharged capacitive load (the docking system), the voltage on that line immediately will droop or glitch, possibly below the switching threshold voltage, while the energy from the relatively high-impedance driver slowly charges the large capacitance of the docking system. This is a slow RC delay. In addition to the obvious electrical glitch, there is a tremendous surge current required from the power supply. This results in potential data corruption.

Solution

The amplitude of the electrical glitch must be reduced to prevent data corruption and other detrimental system effects. The solution to reduce the glitch on the active data bus is to precharge the discharged capacitive load to a voltage level that is halfway between a logic high and a logic low prior to connecting the active bus to the load (see Figure 3).

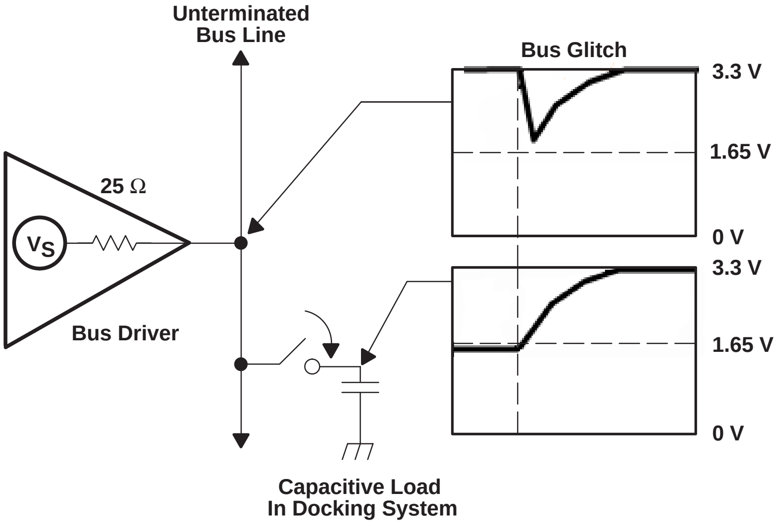

Figure 3. Reduced Glitch With Precharged Load

If the load is at a voltage that is halfway between a high and a low when the connection is made to the active bus, the amplitude of the glitch is reduced to a level that does not cross the threshold level and corrupt data.

FET Switches for Docking

TI provides the crossbar technology (CBT) family of devices for a variety of purposes. CBT devices are a 5-V family; basically, they are field-effect transistors (FETs) that system design engineers use for isolation. The 5-V CBT family of devices isolates one part of a system from another. Because the devices essentially are FET switches, when the transistor is on, they operate as a short circuit, and the voltage on the input is passed through to the output. When the transistor is off, it functions as an open circuit, and the input is completely isolated from the output. CBT devices are useful for docking or live-insertion applications when a 5-V power-supply voltage is available.

With the reduction of power-supply voltages from 5 V to 3.3 V, TI also has created a family of low-voltage crossbar technology (CBTLV) devices that operate from a 3.3-V power supply. The CBTLV is a 3.3-V logic family with a variety of uses similar to those of the CBT. As with the CBT family, CBTLV devices can be used for isolation purposes, and they can be used for hot-plug or docking applications where a 3.3-V power-supply voltage is available.

For systems with a 5-V supply and 5-V or 3.3-V signals, TI recommends the use of the SN74CBT6800A 10-bit FET switch with precharged outputs. Alternatives include the SN74CBTS6800 and SN74CBTK6800 devices, which include additional undershoot clamping for use in systems where signal integrity on the bus is an issue. For systems with a 3.3-V supply and 3.3-V signals, TI recommends the use of the SN74CBTLV16800 low-voltage 20-bit FET switch with precharged outputs. These devices provide precharge voltage to the outputs, which reduces system glitches. By using the recommended TI FET switches with precharged outputs to switch the I/O signals, a complete solution can be designed that provides a robust docking system.

FET Switches Onboard the Mobile System

System Configuration

One method of achieving isolation is to place the bus switches in the mobile system between the mobile system bus and the docking system connector (see Figure 4).

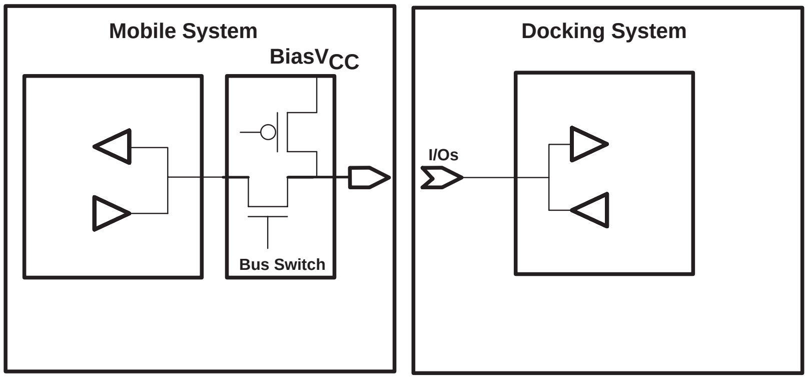

Figure 4. System Diagram With FET Switch in the Mobile System

In this configuration, the precharged port of the FET switch should be connected to the external connector. After insertion, the I/Os in the docking system are precharged by the FET switch to the bias voltage prior to enabling the switch connection between the active bus in the mobile system and the docking system circuitry. This is the recommended implementation; however, it might be undesirable due to the board area and power consumed by the addition of the FET switch devices in the mobile system.

Docking Sequence

With the use of FET switches in the configuration shown in Figure 4, consideration should be given to the sequence of events during a hot-docking event.

Prior to insertion of the mobile device into the dock, the ground, V_{CC} and BiasV_{CC} voltages should be applied to the FET switch. The FET switch should be disabled by placing the OE control line into the inactive state. This enables the precharge voltage to be applied to the port on the connector side. When the mobile device is inserted into an inactive dock system, the I/Os of the devices in that system become precharged to the BiasV_{CC} voltage level. Typically, this BiasV_{CC} voltage is set at a level that is at the threshold voltage. Therefore, it is best if the devices in the docking station remain powered down at this time or that the receivers be disabled because it never is good design practice to leave a CMOS input at its threshold voltage. If the devices within the dock remain powered down while the FET switch is enabled, they must have the I_{off} feature to prevent bus loading after the FET switch connection is made. The I_{off} feature prevents the outputs or I/Os of a device from loading the live signaling on a bus to ground through parasitic paths to V_{CC} when V_{CC} is grounded. At this time, the FET switch connection can be enabled, and the temporary, but reduced, glitch will be seen on the mobile system bus. Then, the devices in the dock system should be powered up, with their control inputs actively driven to a disabled mode until everything is initialized into a valid state.

FET Switches On the Docking Station

System Configuration

The other configuration is to place the FET switch into the docking system, with the precharged port connected to the docking connector (see Figure 5).

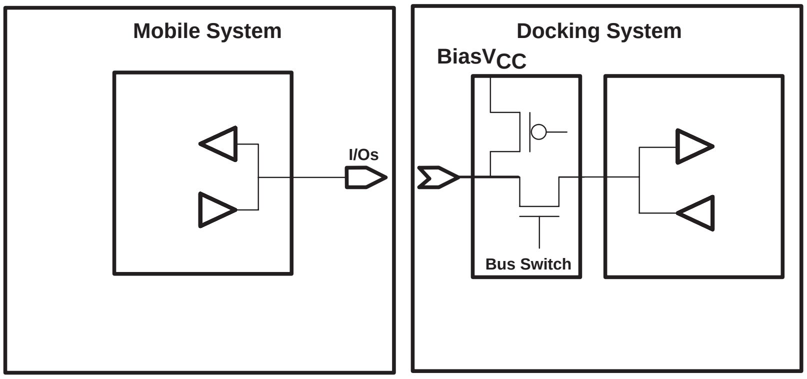

Figure 5. System Diagram with FET Switches in the Docking System

In this configuration, the docking system connections create a glitch during the insertion of the mobile device, and there also is a glitch when the FET switch is enabled. The advantage is that the space and power consumed by the FET switches is inside the docking system, not onboard the mobile device.

Docking Sequence

With the use of FET switches in the configuration shown in Figure 5, the following sequence of events should be followed during a hot-docking event.

Prior to insertion of the mobile device into the dock, the ground, V_{CC} and BiasV$_{CC}$ voltages should be applied to the FET switch. The FET switch should be disabled by placing the /OE control line in the inactive state. This enables the precharge voltage to be applied to the port on the connector side. When the mobile device is inserted into an inactive docking system, there is a temporary, but reduced, glitch as the capacitance of the connector, lead-in PCB trace, and FET-switch I/O becomes charged from the BiasV$_{CC}$ level to the active voltage levels on the mobile-system bus.

Upon recognizing the insertion into the docking station, the mobile system should temporarily halt activity on its internal bus. At this time, the FET switch connection can be enabled, and another glitch will be seen on the mobile system bus as the capacitance of the I/Os in the docking system becomes charged. If the I/O capacitance and bus capacitance in the docking system is large, this glitch can be considerable. If bus activity has been halted, this glitch should have no effect on data integrity. If it is not possible to halt bus activity prior to enabling the switch connection, it may be necessary to manage the glitch by precharging the docking system internal bus. However, this also would require that the devices in the docking system be powered down and that they support I_{off}. After the devices in the docking system are stabilized, they can be enabled, and activity on the bus can be restored to normal.

Summary and Conclusion

The use of TI FET bus switches with integrated precharge onboard a mobile device is a recommended method to reduce bus glitches during live insertion into an inactive docking system. By precharging the I/Os of the docking station to the threshold voltage level prior to enabling the bus switch, the resultant glitch is reduced to a level that does not disturb active data on the bus.

If the addition of bus switches to the mobile device is undesirable due to space or power constraints, the switches can be employed in the docking station. However, the activity on the bus in the mobile device should be temporarily disabled prior to enabling the switch connection to the docking station. This reduces the effect the secondary glitch might create.

TI FET switch products that support precharged outputs include the SN74CBT6800A, SN74CBTS6800, SN74CBTK6800, and SN74CBTLV16800. Data sheets and information on pricing and availability can be found at http://www.ti.com.

Bus FET Switch Solutions for Live Insertion Applications

Tomdio Nana and Gary Khazan *Standard Linear & Logic*

ABSTRACT

In today's competitive computing and networking industry, any equipment downtime due to component interconnects or bus failures impedes communication, hinders productivity, and hampers financial growth. In recognizing this increasingly costly unplanned downtime, the industry introduced live-insertion technology to minimize the impact of any such failures. The live-insertion feature enables a network administrator to replace a failed unit without powering down the system, thereby maintaining high-availability solutions. This application report discuses the Texas Instruments bus-switch solutions for live-insertion technology. The following TI products are used as examples: SN74CBT6800A, SN74CBTLV16800, SN74CBTS6800, and SN74CBTK6800.

Keywords: bus contention, CBT, CBTLV, electrical performance, hot plug, live insertion, partial power down, precharged outputs

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Introduction and Background

In today's computing industry, there is a tremendous increase in the demand for enhanced subsystem functionalities, prevailing mass storage capacity, extensive block data transfer, and improved system operating speed. This remarkable leap in technology and functionality has led to more dependence on computing systems having reliable and accurate information. To keep the varied and critical information flowing to end users, the computer industry has made innovations to overcome the challenges that face it. The peripheral component interconnect (PCI) technology is one of the latest innovations to meet the growing demand for information computer systems to be continuously available. PCI provides a high-speed data path between the central processing unit (CPU) and peripheral devices (video, disk, network, etc.)

Computing systems based on the industry-standard personal computer architecture have undergone steady improvement in the areas of reliability and availability. Some subsystems have been further enhanced by a process commonly referred to as live insertion, which allows the rest of the system to remain operational when circuit boards are removed or inserted.

The PCI bus has been improved with live-insertion capabilities, enabling standard PCI adapter cards to be inserted and removed in systems without turning off the system power. The PCI live-insertion technology benefits those systems in which a PCI adapter failure affects productivity of a large number of users, or affects sales; or, where the applications are too critical to have even a minimal amount of down time. It gives the network administrator valuable tools that keep the system operational by conducting the live-insertion operation without interfacing with the other PCI devices on the bus. The PCI adapter cards that are designed to meet *PCI Local Bus Specification, Revision 2.1,*[1] have a standard for removal and installation.

The reduction or complete elimination of noise and transients generated during live-insertion is a primary concern in the preservation of signal integrity on the PCI bus. Texas Instruments (TI) manufactures field-effect transistor (FET) bus switches that are designed to isolate the local bus from the PCI adapter during live insertion and removal. This application report introduces TI's bus-switch solutions for live-insertion applications, discusses their logic functionality, and their use in the intended applications. The information in this application report, along with the data sheets, should enable a system designer to successfully implement a live-insertion solution.

Definition of Terms

This section lists and defines some key terms used in this application report. The following definitions are specifically defined by TI and may or may not agree with other semiconductor vendor definitions.

Bus Contention

Bus contention occurs in a system when two (or more) drivers connected on the same bus are inadvertently placed in opposing states (one driver is driving a low while the other is driving a high). For example, if several bus drivers with 3-state outputs are connected to a single bus, it often cannot be ensured that, while switching from one bus driver to another, both are not simultaneously active for a short time. During this time, a short circuit of the outputs exists, resulting in an overload of the circuit. This situation also is known as bus conflict.

Figure 1 shows an illustration of bus contention in a system in which two devices are driving the same bus. One has high-level output and the other has low-level output. This results in the opposing logic levels producing a short between the drivers, creating a current surge that may damage the devices. However, an FET switch in the data path (see Figure 1) can isolate the two drivers when opposite logic levels are driven.

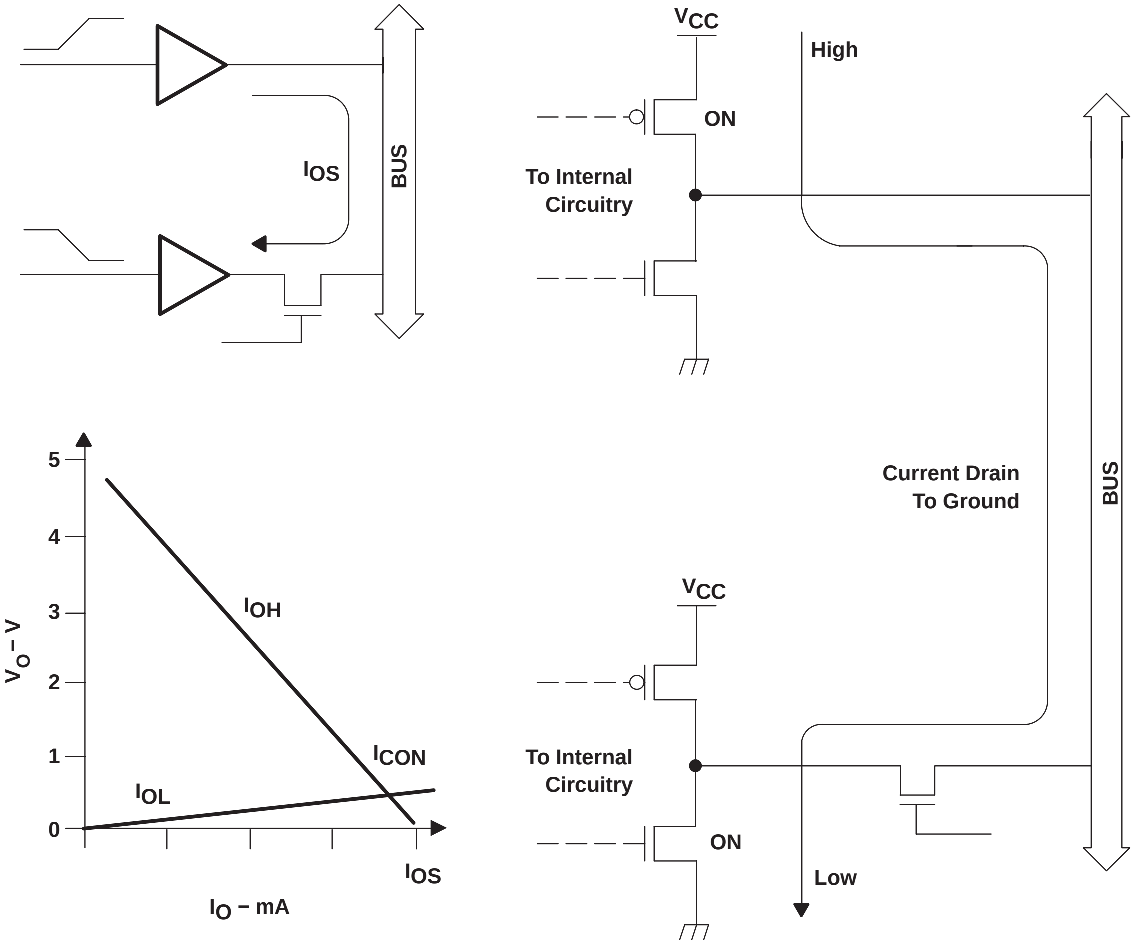


Figure 1. Short-Circuit Current With Bus Contention

During bus contention, the bus state may be unpredictably low, high, or somewhere in between. This unpredictable state during bus contention can cause data corruption during system operation. The current that results from bus contention can be calculated by means of the output characteristics of the devices. As shown in Figure 1, the short-circuit current (I_{OS}) is limited by the high output current of the device involved in the bus-contention situation.

TI data sheets specify the maximum continuous current through a single output or through V_{CC} and GND. These values are absolute maximum ratings, which are stress ratings, not recommended operating conditions. If bus contention occurs, these specifications can be exceeded, and it may cause permanent damage to the devices.

Partial Power Down

Partial power down is a system function or capability in which it is desired to power off some part of the system in order to conserve power. The system recognizes that some part of the system is not in use and places it in a power-off mode (in which the supply voltage, V_{CC}, is 0 V for the affected part of the system).

Because the system coordinates and controls the power-down/power-up sequence, typically it is required only to ensure that no circuit (either those that are powered on or those that are powered off) is damaged during the partial-power-off mode. This can be ensured if the circuits to be powered off have input and/or output circuits that maintain a high-impedance state while V_{CC} = 0 V.

With TI standard CMOS logic devices, this circuit capability is indicated by the specification of pin current at V_{CC} = 0 V, I_{off}. Typically, I_{off} is tested at pin voltages that approximate valid logic low and high levels (0.5 V, 3 V) and is specified in the range of ±100 µA.

For TI standard CMOS logic devices, the circuit modifications that are/may be required to support the I_{off} specification are the elimination of any diodes placed explicitly (as for ESD protection) between the pin and V_{CC} terminals. Many input and/or output circuits also may have parasitic diodes from pin to V_{CC}. In such cases, it is required to insert a reverse-oriented blocking diode to prevent unwanted currents from moving from the I/O pin to V_{CC}.

TI CBT and CBTS FET switches basically are pass transistors, with no path from the I/O to V_{CC}. Consequently, there is no leakage current from the I/O to V_{CC} when the device is powered off. I_{off} is, therefore, inherent to the CBT and CBTS FET switch devices due to the nature of their design, and I_{off} is not specified on the FET switches data sheets. Conversely, when the TI CBTK and CBTLV FET switches are powered off, a current leakage path from the device input may exist. Thus, a current-limiting circuit is included in the switch design to limit the current leak through the channel when the device is powered down. With the SN74CBTK6800 device, I_{off} is characterized over the valid input voltage range (0 V to 5 V) and is specified at 20 µA. Similarly, with the SN74CBTLV16800 device, I_{off} is characterized over the valid input voltage range (0 V to 3.6 V) and is specified at 10 µA.

Precharged Inputs/Outputs

During insertion (or removal) of a daughter card into (or from) a live bus, the data may be corrupted to the point where the signal transition actually traverses through the threshold region of an input device and switches the logic state of its output. This situation results in false data transfer, and damage to the device is possible.

Precharging the driver I/Os before insertion is a method used to minimize data corruption during insertion. Consider, for example, an energized bus at a high logic state. Before a daughter card is inserted into the live bus, the daughter card output voltage could be close to, or at, GND. Each signal pin that is being attached to the bus has an inherent capacitance due to the input and output IC structure, the IC package, the stub, and the connector itself.

The purpose of a capacitor is to resist a change in voltage. Therefore, when the connector pin makes contact, the daughter card's capacitance tries to force the bus signal as close to GND as it can and then increase, asymptotically, toward the original voltage. The degree to which the voltage can be forced low is dependent on the parasitics of the daughter card and the live bus. The larger the supporting parasitics, the bigger the perturbation.

Figure 2 shows what can happen when a high-parasitic capacitance is associated with the plug-in card. When the voltage spike crosses the input threshold voltage of a receiver, the data is corrupted. Insertion or removal of a daughter card does not present a concern when a live bus is biased to a logic-low level because any perturbation will, at most, force the bus voltage very close to 0 V.

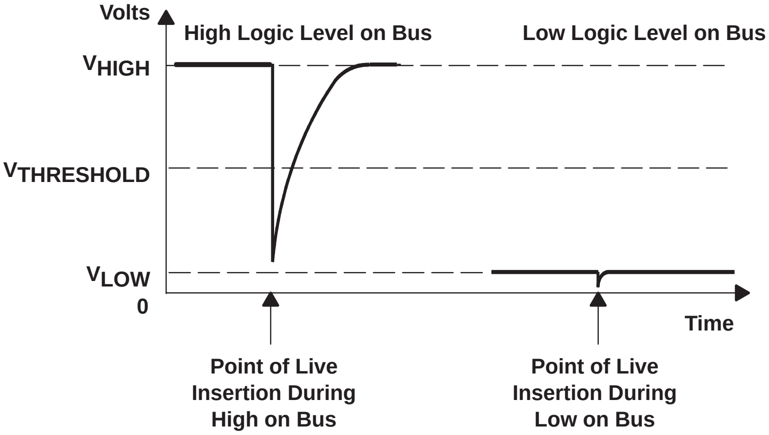


Figure 2. Possible Data-Corruption Scenarios Without Precharged Outputs

One way of limiting the glitch from crossing the threshold voltage is to reduce the parasitic capacitance. Ideally, it would be better to eliminate the capacitance altogether, but that is not possible. Another way in which the glitching effect can be reduced is to precharge the output pin of the device to a voltage centered between the low-level and high-level output voltage before the connector pin is attached to the active bus.

Figure 3 shows that, by setting the precharged voltage (BIASV) equal to the input threshold voltage, this perturbation can be reduced. Any glitch produced on the bus no longer crosses the input threshold region of the receiver, regardless of the state the bus is in when the glitch is generated. However, in the low state, the bus voltage is forced high and approaches the precharged voltage level, but never actually crosses the threshold, eliminating any chance of propagating a false data bit throughout the system.

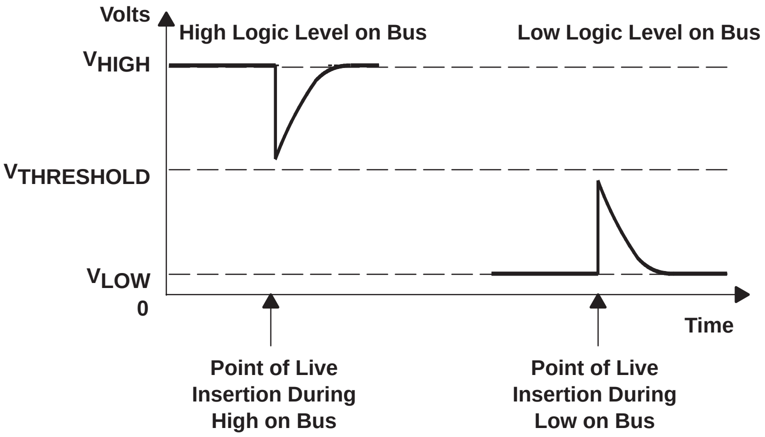


Figure 3. Precharge BIASV Functionality Eliminates Data Corruption

Live Insertion

Live insertion is a system functionality or capability in which it is desired to be able to insert unpowered circuit elements into a fully operational system. Generally, it also must support removal of powered circuits. This is typified by a card-rack system in which a malfunctioning card might need to be removed and replaced with a properly functioning card, without interrupting or otherwise adversely affecting the operation of other system circuits.

In many applications, there is a strict requirement for it to be possible to exchange system modules without interrupting normal system operation. A typical example is an electronic telephone exchange, in which the replacement of an individual telephone circuit must be possible at any time, without adversely affecting the operation or use of other telephone circuits. From a quality-of-service perspective, this capability is essential for such applications.

Since the act of live insertion (or removal) cannot take place in a maintenance mode in which the system is not expected to operate normally or without interruption, it is necessary to not only ensure that no circuits are damaged while the module is inserted or removed, but also to ensure that the insertion (or removal) does not cause the bus state to become invalid (even in a transient, glitch sense). The latter requirement is necessary to ensure that the live insertion (or removal) does not adversely affect bus transactions that may be occurring at the instant of insertion (removal).

Due to the capacitive nature of a circuit pin and the fact that this capacitance typically is uncharged upon insertion, a negative transient can occur on bus lines, which should be driven high. If the capacitive effect is idealized, the bus voltage would be expected to drop to 0 V at the point of insertion. However, if this capacitance can be precharged to a level that mitigates the magnitude of the bus glitch (approximately $V_{CC}/2$ for totem-pole signaling and V_{OH} for open-collector or open-drain signaling), the transient will have no ill effect.

This circuit capability is indicated by the specification of a precharged bias voltage, BIASV. Typically, bias currents also are provided as supporting specifications.

The required circuit provisions are referred to collectively as a precharge circuit. Typically, this consists of a voltage-divider resistor network, or something similar. Of course, since the primary supply voltage, V_{CC}, is 0 V, the precharge circuit must be powered otherwise. This requires the provision of a special supply-voltage terminal, typically designated BIASV. In use, it must be possible for BIASV to be powered before the primary supply voltage, V_{CC}. Typically, this is ensured through the use of mechanical sequencing, in which the connector pins, which bring BIASV (and GND) onto the module, make contact before the connector pins that bring V_{CC} onto the module.

Hot Plug

Hot plug is a system functionality or capability in which unpowered circuit elements are inserted into a fully powered (hot) system. Generally, also it must support removal of powered circuits. This is typified by a card-rack system, in which a malfunctioning card might need to be removed and replaced.

If this can be done while the system remains powered, then, although the system may be placed in a nonoperational or maintenance mode, the system can be returned more quickly to normal operation than if the system were powered off for maintenance. PCMCIA is a familiar example in which card-based functions can be removed or inserted without having to power off and cold-start the system. From a quality-of-service perspective, this capability is essential for many applications.

Because the act of hot plug (or removal) usually can take place in a maintenance mode in which the system is not expected to operate normally (i.e., without interruption), typically it is required only to ensure that no circuits are damaged while the module to be inserted (or removed) is unpowered, as well as during its power-up (or power-down) sequence. This requires that circuits that interface the module to be inserted in the system bus have input and/or output circuits that maintain the high-impedance state while V_{CC} = 0 V (see I_{off}, above) *and* while V_{CC} is powering up to (or powering down from) an operational level. The latter requirement ensures that these circuits do not contend on the system bus with circuits already in place and powered up.

TI Live-Insertion FET Switch Devices

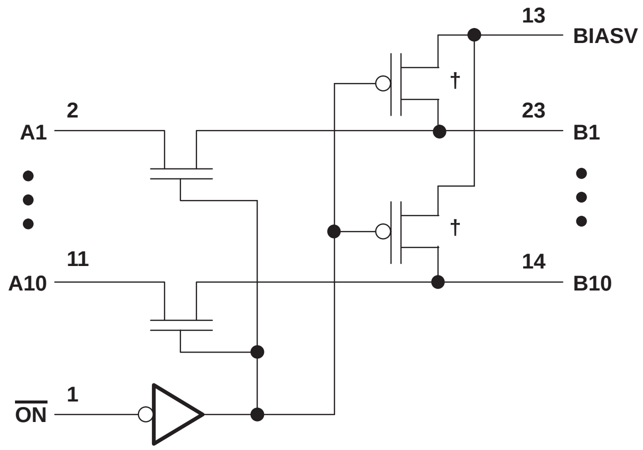
SN74CBT6800A 10-Bit FET Bus Switch with Precharged Outputs

The SN74CBT6800A provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made, while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The SN74CBT6800A is organized as one 10-bit switch with a single enable ($\overline{\text{ON}}$) input. When $\overline{\text{ON}}$ is low, the switch is on, and port A is connected to port B. When $\overline{\text{ON}}$ is high, the switch between port A and port B is open. When $\overline{\text{ON}}$ is high or V_{CC} is 0 V, B port is precharged to BIASV through the equivalent of a 10-kΩ resistor. The functional operation of the SN74CBT6800A is shown in Table 1 and the logic diagram is shown in Figure 4.

Table 1. SN74CBT6800A Function Table

INPUT $\overline{\text{ON}}$	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV



† Equivalent 10-kΩ resistance when turned on

Figure 4. SN74CBT6800A Logic Diagram (Positive Logic)

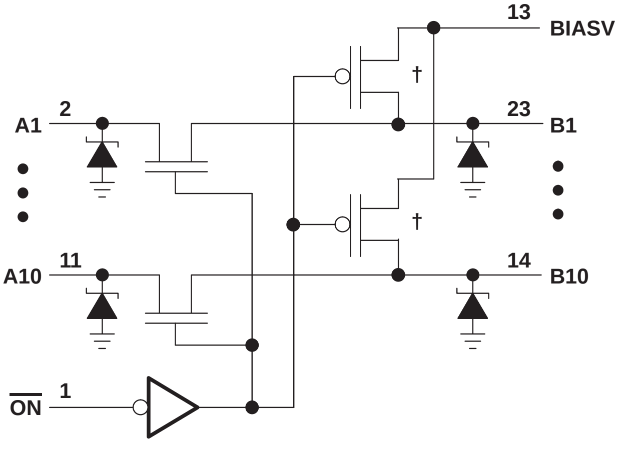
The SN74CBT6800A is characterized for operation from –40°C to 85°C, with a supply voltage from 4-V to 5.5-V V_{CC}.

SN74CBTS6800 10-Bit FET Bus Switch with Precharged Outputs and Schottky-Diode Clamping

The SN74CBTS6800 provides ten bits of high-speed TTL-compatible bus switching, with Schottky diodes on the I/Os to clamp undershoots. Functionally, the device is identical to and pin-to-pin compatible with, the SN74CBT6800A. In addition, the SN74CBTS6800 has Schottky diodes at the I/O ports for undershoot protection.

The undershoot event does not affect performance of the switch when the switch is on. But, if undershoots occur when the bus switch is off, passing unwanted data can cause data errors. To prevent this, two Schottky diodes are connected from the source and drain to ground. When one of the buses has negative voltage that exceeds the forward turn-on voltage of the Schottky diode, the diode turns on and clamps the source or drain voltage of the NMOS switch, keeping the buses isolated.

Functional operation of the SN74CBTS6800 is same as that for the SN74CBT6800A (see Table 1). The logic diagram of the SN74CBTS6800 is shown in Figure 5.



† Equivalent 10-kΩ resistance when turned on

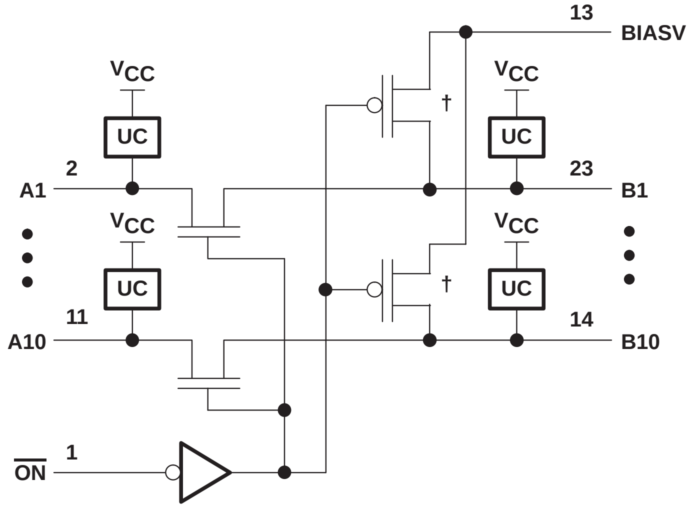
Figure 5. SN74CBTS6800 Logic Diagram (Positive Logic)

SN74CBTK6800 10-Bit FET Bus Switch with Precharged Outputs and Active-Clamp Undershoot-Protection Circuit

The SN74CBTK6800 provides ten bits of high-speed TTL-compatible bus switching with an active-clamp undershoot-protection circuit. Functionally, the device is identical to, and pin-to-pin compatible with, the SN74CBT6800A. When there is an undershoot, the active-clamp circuit in the SN74CBTK6800 is enabled, and current from V_{CC} is supplied to clamp the output, preventing the pass transistor from turning on.

In the active-clamp circuit, a bias generator sets a voltage slightly above ground potential, which allows the active-clamp pullup voltage to turn on during an undershoot event. The clamp counteracts the undershoot voltage and limits V_{GS}, V_{GD} of the n-channel, and V_{be} of the parasitic npn transistor.

Functional operation of the SN74CBTK6800 is same as that for the SN74CBT6800A (see Table 1). The logic diagram of the SN74CBTK6800 is shown in Figure 6.



UC = undershoot clamp circuit
† Equivalent 10-kΩ resistance when turned on

Figure 6. SN74CBTK6800 Logic Diagram (Positive Logic)

The SN74CBT6800A, SN74CBTS6800, and SN74CBTK6800 are 10-bit FET bus switches that are characterized for operation from –40°C to 85°C, with a supply voltage from 4-V to 5.5-V V_{CC}. The major differences between the three devices are summarized in Table 2.

Table 2. Differences Between the SN74CBT6800A, SN74CBTS6800, and SN74CBTK6800

FEATURES	SN74CBT6800A	SN74CBTS6800	SN74CBTK6800
Undershoot protection	No undershoot protection. This could cause the n-channel pass transistor to turn on and affect the buses.	Some undershoot protection. Slow to react to undershoot voltage with fast edge rates.	Excellent undershoot protection
I/O capacitance	Low C_{io}	Minimal addition of the input/output capacitance	Increased C_{io}
Power requirement	More power required	Less power required	Average power required
Overvoltage tolerance	No overvoltage tolerance	No overvoltage tolerance	Overvoltage-tolerant I/Os

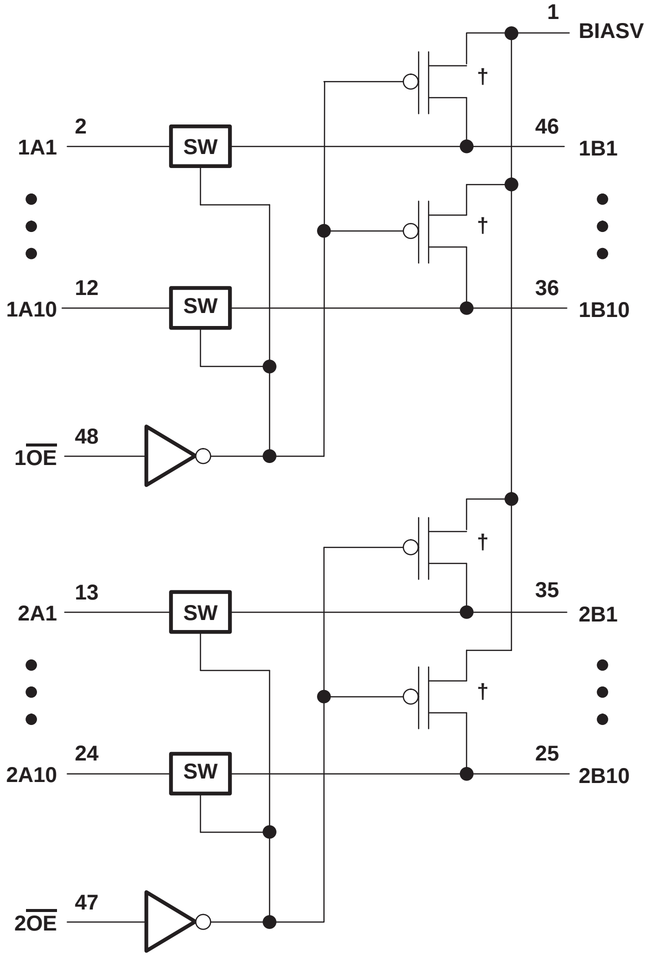
SN74CBTLV16800 Low-Voltage 20-Bit FET Bus Switch with Precharged Outputs

The SN74CBTLV16800 provides 20 bits of high-speed bus switching. The low on-state resistance of the switch allows bidirectional connections to be made, while adding near-zero propagation delay. The device also precharges the B port to BIASV to minimize live-insertion noise.

The SN74CBTLV16800 is organized as dual 10-bit bus switches with separate output-enables ($\overline{OE}$) input. It can be used as two 10-bit bus switches or one 20-bit bus switch. When $\overline{OE}$ is low, the associated 10-bit bus switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, the high-impedance state exist between the two ports, and port B is precharged to BIASV through the equivalent of a 10-kΩ resistor. The functional operation of the SN74CBTLV16800 is shown in Table 3 and the logic diagram is shown in Figure 7.

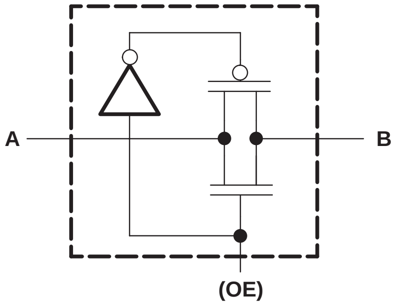
Table 3. SN74CBTLV16800 Function Table for Each 10-Bit Bus Switch

INPUT $\overline{\mathrm{OE}}$	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV



1
BIASV
†
2
1A1
SW
46
1B1
†
12
1A10
SW
36
1B10
48
1OE
†
13
2A1
SW
35
2B1
†
24
2A10
SW
25
2B10
47
2OE

Simplified Schematic of Each FET Switch (SW)



† Equivalent 10-kΩ resistance when turned on

Figure 7. SN74CBTLV16800 Logic Diagram (Positive Logic)

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. For information on calculating the desired pullup resistor value, refer to application report *HCMOS Design Considerations*, literature number SCLA007.[8]

The SN74CBTLV16800 is characterized for operation from –40°C to 85°C and the supply voltage from 2.3-V to 3.6-V V_{CC}.

Live-Insertion Applications with FET Switch Devices

In many applications, the system cannot be shut down at any time. Examples include industrial control systems, communications, and financial networks. All maintenance and replacements should be done when the system is running without bus disruptions. Figure 8 shows a diagram of a typical distributed control system.

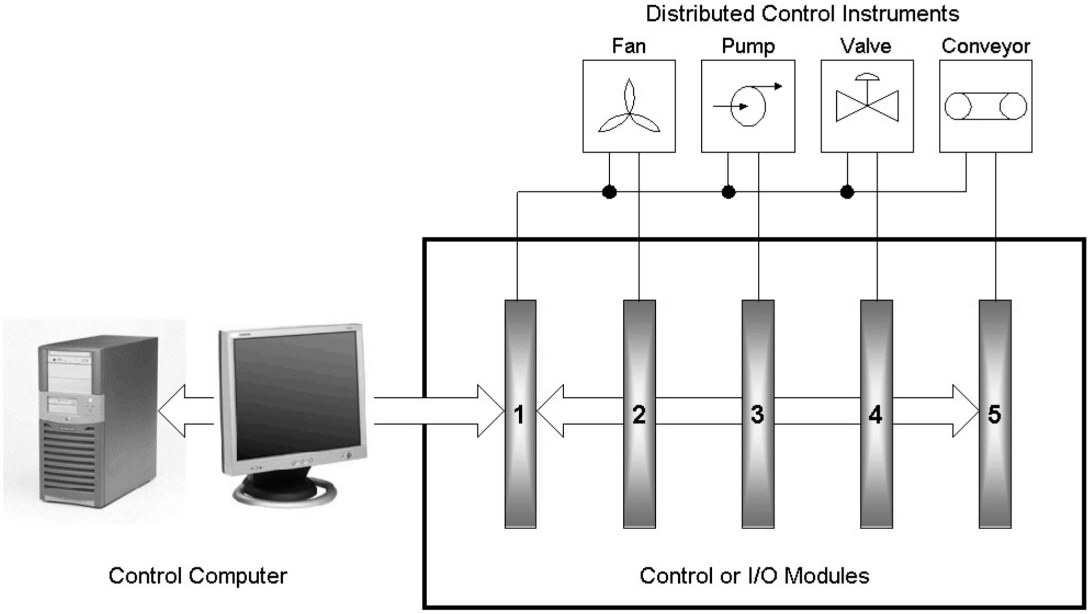


Figure 8. Example of a Typical Distributed Control System

In most cases, control modules should be replaced without shutting down the system, without interruptions for other modules, and without bus errors. The TI live-insertion FET switches can be used for this purpose.

TI FET switches, with precharged outputs, offer an opportunity for successful live-insertion design. A proper insertion sequence always should be followed to avoid excessive current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems.

1. A good ground connection must make the first contact with the bus connector.
2. Power-up of BIASV supply. BIASV supply should make contact consistent with, or after, GND.
3. The V_{CC} power supply, output-enable control, and then the signal lines (in that order) must make the connection.
4. The full insertion of the PCI adapter should prompt the PCI local bus to start communicating with the new device.

A six-slot board was made to accommodate six PCBs, each having one SN74CBTLV16800, driven independently as if it were a separate control module. The modules were connected as shown in Figure 9. In the experiment, only two modules were used, module 1 and module 6.

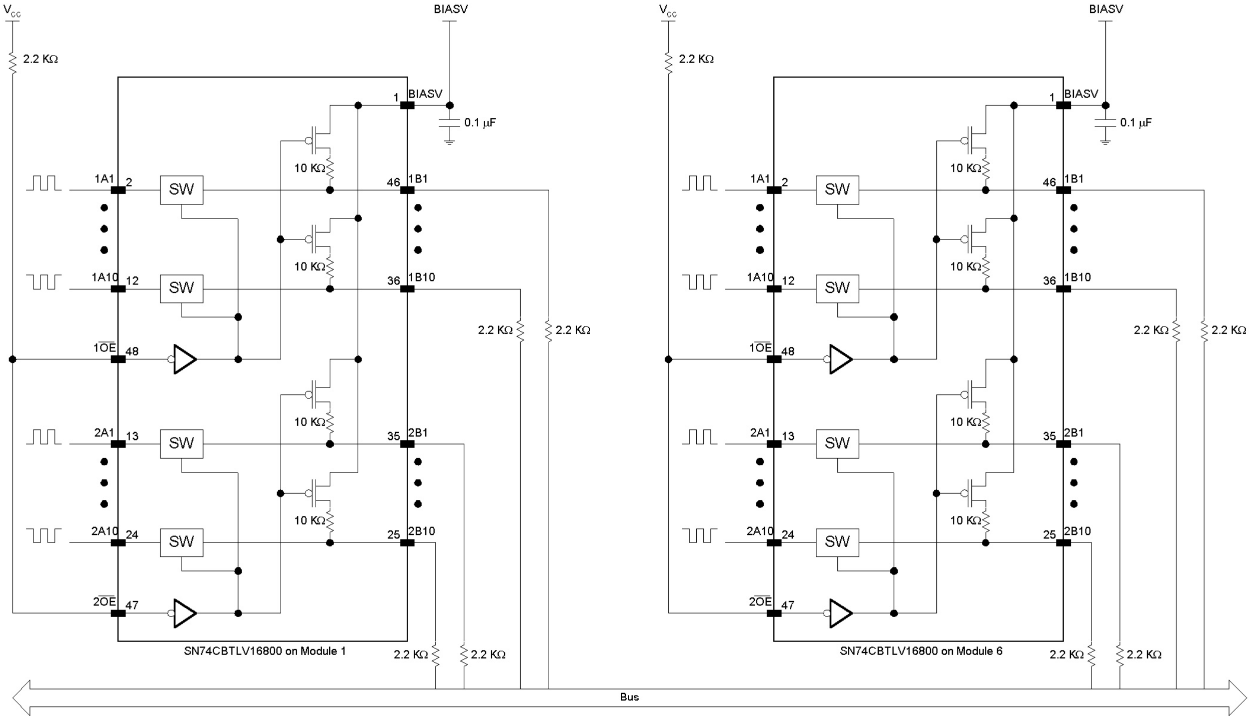

VCC
2.2 KΩ
BIASV
1
BIASV
0.1 µF
10 KΩ
1A1
2
SW
46
1B1
10 KΩ
1A10
12
SW
36
1B10
2.2 KΩ
2.2 KΩ
1OE
48
10 KΩ
2A1
13
SW
35
2B1
10 KΩ
2A10
24
SW
25
2B10
2OE
47
SN74CBTLV16800 on Module 1
2.2 KΩ
2.2 KΩ
VCC
2.2 KΩ
BIASV
1
BIASV
0.1 µF
10 KΩ
1A1
2
SW
46
1B1
10 KΩ
1A10
12
SW
36
1B10
2.2 KΩ
2.2 KΩ
1OE
48
10 KΩ
2A1
13
SW
35
2B1
10 KΩ
2A10
24
SW
25
2B10
2OE
47
SN74CBTLV16800 on Module 6
2.2 KΩ
2.2 KΩ
Bus

Figure 9. Laboratory Set-Up for Live-Insertion Experiments With the SN74CBTLV16800

The laboratory tests were done with different bus input-level combinations and, in all cases, the GND and BIASV made contact first, followed by V_{CC}, $\overline{\text{OE}}$s, and signal lines. 1$\overline{\text{OE}}$ was tied to V_{CC} through a 2.2-kΩ resistor (for a data generator used as an input source).

Figures 10 through 13 show the relationships of the module 1 1B1 output (CH1) and module 6 BIASV (CH2) signal, 1$\overline{\text{OE}}$ (CH3) input, and 1A1 (CH4) input. During the experiment, module 1, with one SN74CBTLV16800, already was plugged into the six-slot PCB, and module 6, with one SN74CBTLV16800, was inserted at the time, T, as shown on the plots. The 1A1 input signal of the inserted module 6 is driven either low or high during insertion, and the 1B1 output signal (from module 1) driven on the bus is either low or high.

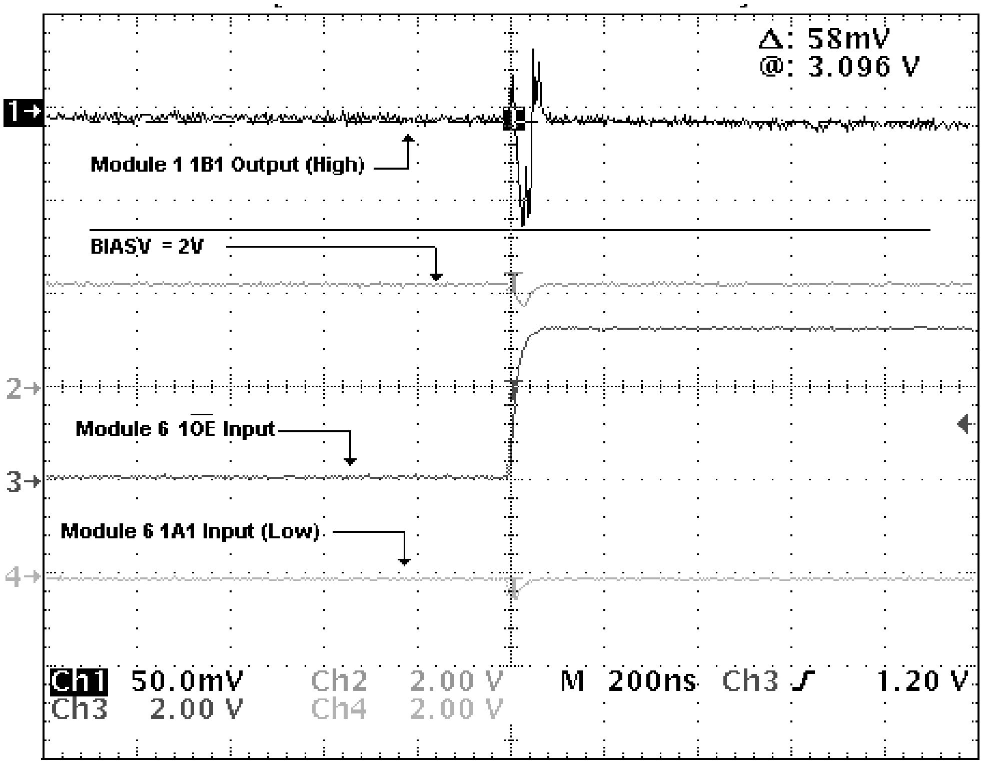


Figure 10. SN74CBTLV16800 Signals During Live Insertion (1A1 = Low, 1B1 = High)

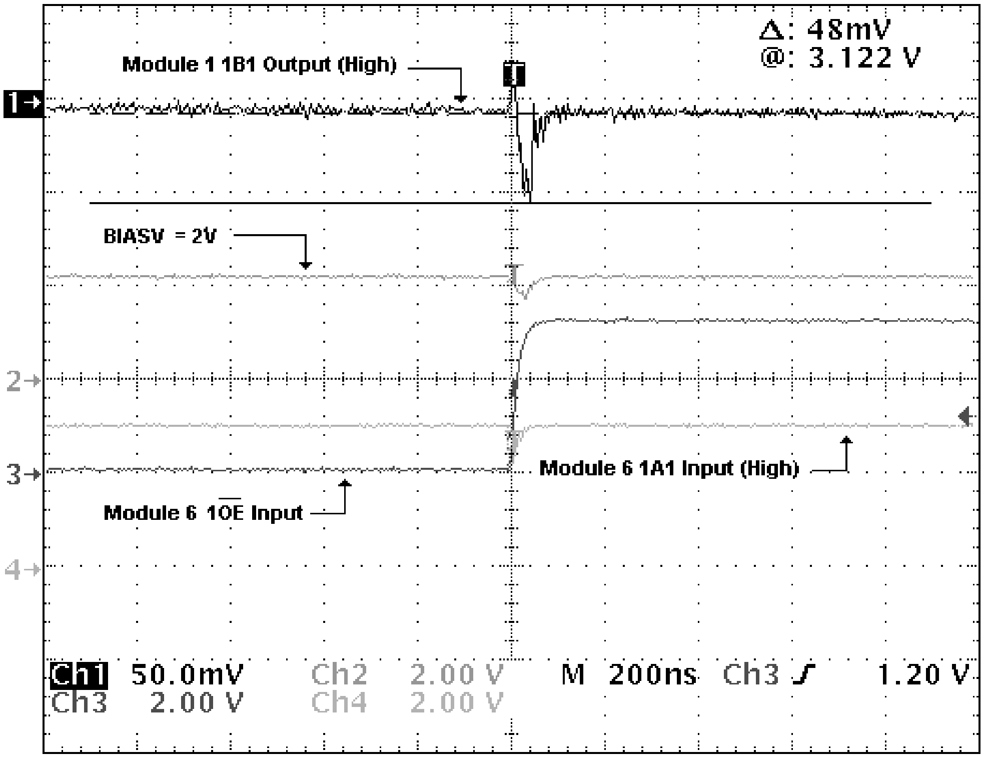


Figure 11. SN74CBTLV16800 Signals During Live Insertion (1A1 = High, 1B1 = High)

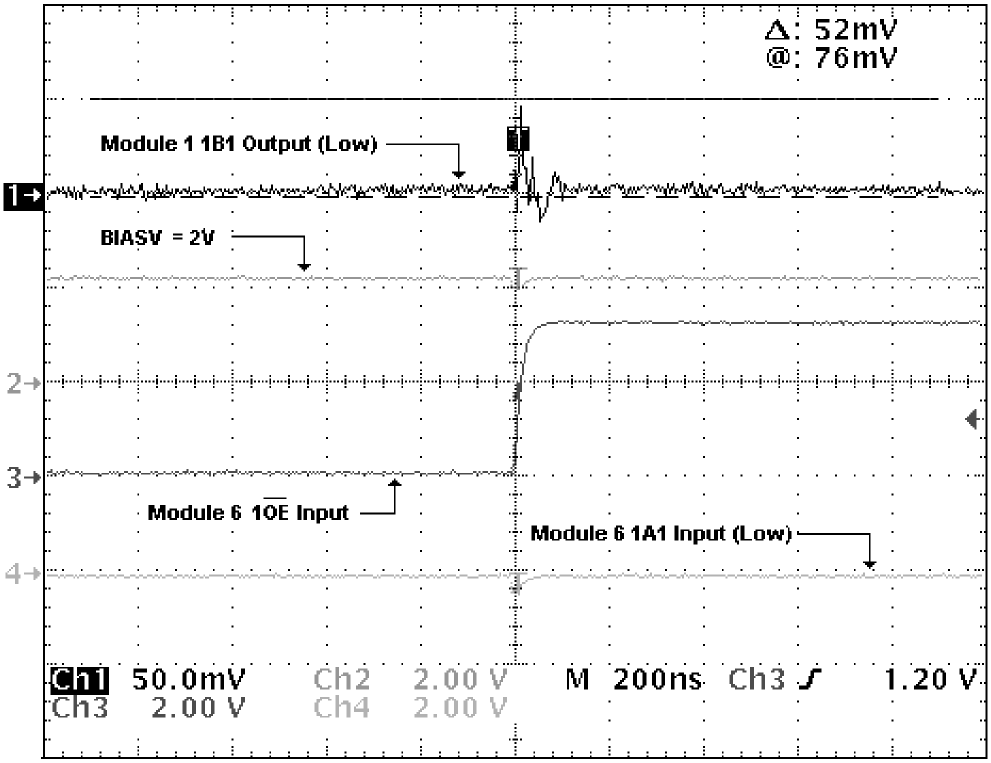


Figure 12. SN74CBTLV16800 Signals During Live Insertion (1A1 = Low, 1B1 = Low)

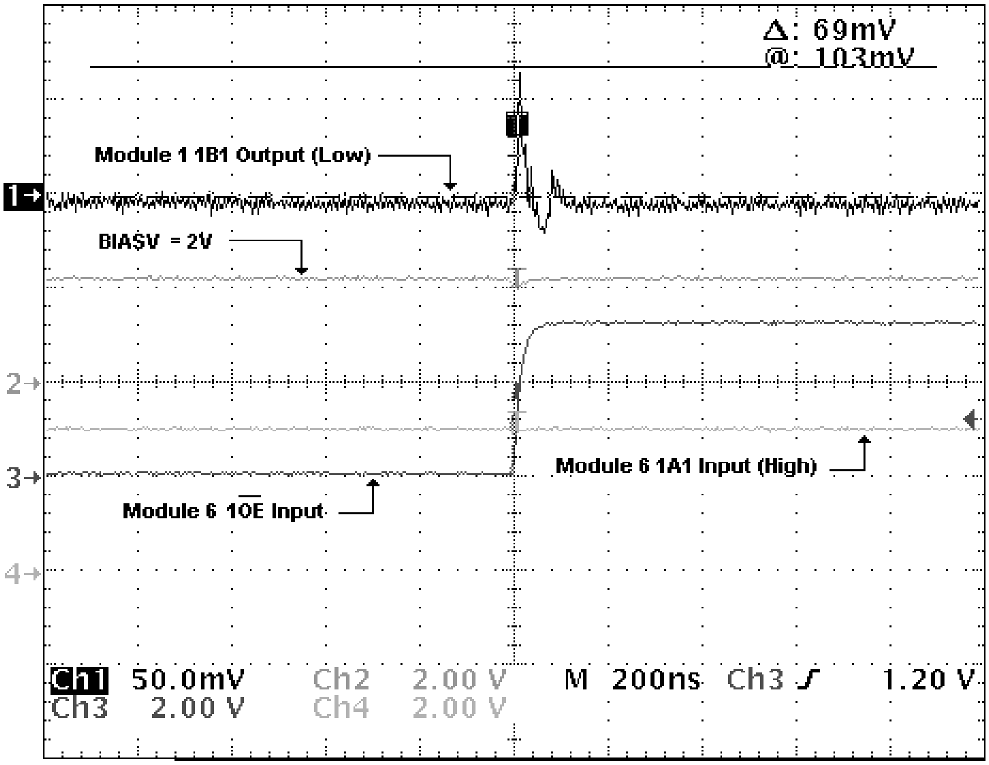


Figure 13. SN74CBTLV16800 Signals During Live Insertion (1A1 = High, 1B1 = Low)

During the tests, the outputs were pulled to BIASV level (set to 2 V in these cases) when they are disabled (1$\overline{\text{OE}}$ = high). As observed in the plots, the bus-signal glitch does not exceed 100 mV and cannot cause data corruption. Also, the glitch is very narrow (in these cases, less than 0.5 µs). In reality, the duration of the “pulse” depends on signal level, connector quality, bus impedance at the insertion point, and operating frequency.

To demonstrate the benefit of using the FET switch with precharged output, the same test was done using the SN74CBTLV16800, with BIASV disconnected (floating). In this case, during live insertion, the outputs were not precharged and the signal quality was the same as using any ordinary FET switch without the precharged feature. Figure 14 shows the relationships of input (1A1), 1$\overline{\text{OE}}$, BIASV, and Output (1B1) signals for one channel of the SN74CBTLV16800 that is being inserted at time, T. The 1A1 input signal of the inserted module either is driven low or high during insertion, and the 1B1 output signal driven on the bus either is low or high.

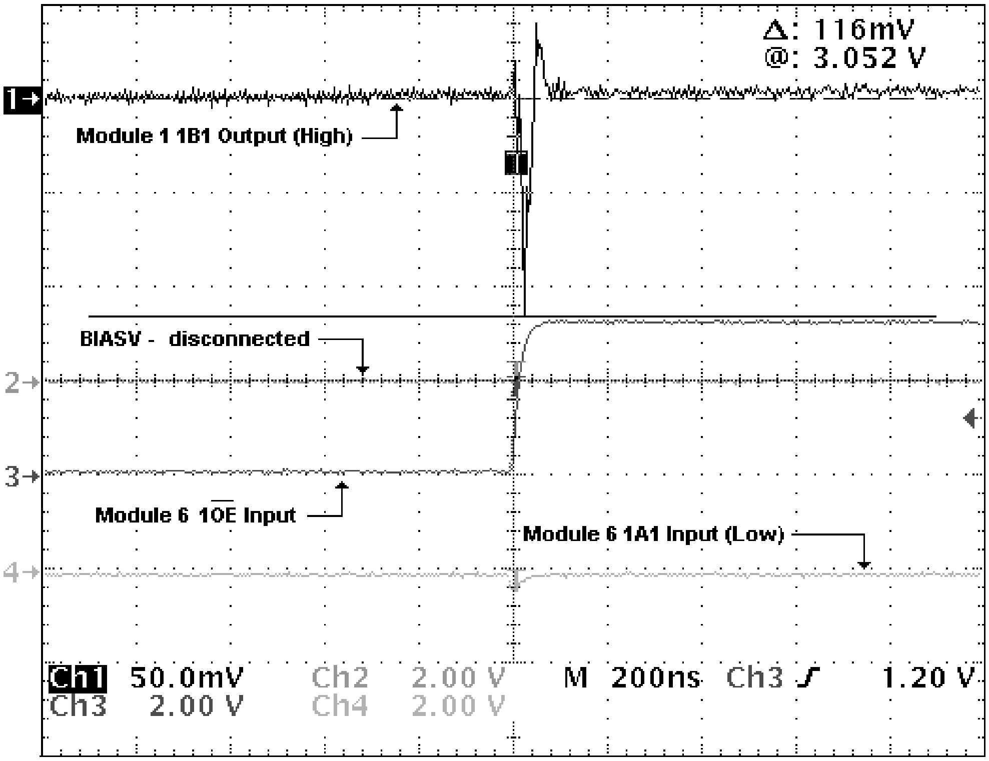


Figure 14. SN74CBTLV16800 Signals During Live Insertion, No Precharge

As shown in Figure 14, without the precharge feature, the bus signal glitches and exceeds 150 mV (peak-to-peak).

Features and Benefits

Table 4 summarizes the features and benefits of TI live-insertion FET switch devices.

Table 4. Features and Benefits

FEATURES	BENEFITS
Live insertion with uninterruptable operation	Ability to replace or upgrade a card without disrupting the operation or degrading the signal on the bus
User-selectable bias voltage	Enables the user to set the outputs precharged voltage
Output-enable feature	Allows device to be placed in the high-impedance state and prevent bus contention
Flow-through pinout	Ease of trace routing

Conclusion

The live-insertion technology has raised the level of system availability with zero-downtime support. Therefore, it is possible to have a system that may never need to be shut down for maintenance. These new hardware designs have built-in redundancy and, at the same time, provision for upgrades. This application report presents TI bus-switch solutions for live-insertion applications, discusses their logic functionality, and their use in the intended applications.

Frequently Asked Questions (FAQs)

What are Texas Instruments crossbar switches?

Crossbar switches are high-speed bus-connect devices. Each CBT FET switch consists of an n-channel MOS transistor driven by a CMOS gate. When enabled, the n-channel transistor gate is pulled to V_{CC} and the switch is on. Conversely, each CBTLV FET switch consists of an n-channel MOS transistor in parallel with a p-channel MOS transistor. The control signal driving the gate of the n-channel transistor is inverted to drive the gate of the p-channel transistor. When enabled, the n-channel transistor gate is pulled to V_{CC}, the p-channel transistor gate is pulled to GND, and the switch is on. The crossbar switches typically have an on resistance of 5 Ω and a propagation delay of 250 ps.

How do I get copies of the logic data sheets and samples?

The logic data sheets can be obtained by accessing http://www.ti.com. Samples of the logic devices can be obtained by contacting your local TI sales representative.

How do I get copies of logic HSPICE and IBIS models?

The HSPICE models for logic devices can be obtained by contacting your local TI sales representative. The IBIS models can be obtained by accessing http://www.ti.com.

What is important about live insertion?

Many systems in communication applications must remain operational 24 hours a day, 7 days a week. These systems cannot be shut down when a board is inserted or removed from the system, as frequently happens during regular maintenance or system upgrades, nor can active system data be disturbed.

The devices discussed in this application report fully support live insertion, with BIASV circuitry for precharging the outputs during power-up. BIAS circuitry allows easy internal precharging of the daughter-card connections to mid-threshold levels to prevent glitching active data during card insertion or removal.

What are the advantages of using the live-insertion bus FET switch solutions?

The advantages of using the live-insertion bus FET switch solutions include:

- Live insertion with uninterruptable operation makes them usable in systems that require replacing or upgrading a card without disrupting the operation or degrading the signal on the bus.
- User-selectable bias voltage enables the user to set the outputs' precharge voltage.
- The output-enable feature allows the device to be placed in the high-impedance state, preventing bus contention.
- Flow-through pinout eases PCB trace routing.

References

16. *PCI Local Bus Specification*, Revision 2.1, June 1, 1995, PCI Special Interest Group, Portland, Oregon.
17. *PCI Hot-Plug Specification*, Revision 1.0, October 6, 1997, PCI Special Interest Group, Portland, Oregon.
18. *Logic in Live-Insertion Applications With a Focus on GTLP*, application report, literature number SCEA026.
19. *SN74CBT6800A 10-Bit FET Bus Switch with Precharged Outputs*, data sheet, literature number SCDS005.
20. *SN74CBTS6800 10-Bit FET Bus Switch with Precharged Outputs and Schottky Diodes Clamping*, data sheet, literature number SCDS102.
21. *SN74CBTK6800 10-Bit FET Bus Switch with Precharged Outputs and Active-Clamp Undershoot-Protection Circuit*, data sheet, literature number SCDS107.
22. *SN74CBTLV16800 Low-Voltage 20-Bit FET Bus Switch with Precharged Outputs*, data sheet, literature number SCDS045.
23. *HCMOS Design Considerations*, application report, literature number SCLA007.
24. *Live Insertion*, application report, literature number SDYA012.

Glossary

BiCMOS	Bipolar and complementary metal-oxide-semiconductor process
BIASV	A user-selectable bias voltage to which a live-insertion device is precharged in order to minimize live-insertion noise.
CBT	Crossbar technology logic
CBTLV	Low-voltage crossbar technology logic
CMOS	Complementary metal-oxide-silicon; a device technology that has balanced drive outputs and low power consumption
CPU	Central processing unit
FET	Field-effect transistor
IBIS	I/O buffer information specification
I_{OFF}	Input/output power-off leakage current. The maximum leakage current into or out of the input/output transistors when forcing the input or output to 2.7 V and V_{CC} = 0 V
PCB	Printed circuit board
PCI	Peripheral-component interconnect
SPICE	Simulation program with integrated-circuit emphasis
TI	Texas Instruments
TTL	Transistor-transistor logic
V_{OH}	High-level output voltage. The voltage at an output terminal with input conditions applied that, according to the product specification, establishes a high level at the output.
V_{OL}	Low-level output voltage. The voltage at an output terminal with input conditions applied that, according to the product specification, establishes a low level at the output.

Texas Instruments Crossbar Switches

SCDA001A
July 1995

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What Are Texas Instruments Crossbar Switches?

Crossbar switches are high-speed bus-connect devices. Each switch consists of an n-channel MOS transistor driven by a CMOS gate. When enabled, the n-channel transistor gate is pulled to V_{CC} and the switch is on. These devices have an on-state resistance of approximately 5 Ω and a propagation delay of 250 ps. They are capable of conducting a current of 64 mA each. The transistor clamps the output at ≈1 V less than the gate potential, regardless of the level at the input pin. This is one of the n-channel transistor characteristics (see Figures 1 and 2). Note the ≈1-V difference between the gate (V_{CC}) and the source (V_O) at any point on the graph.

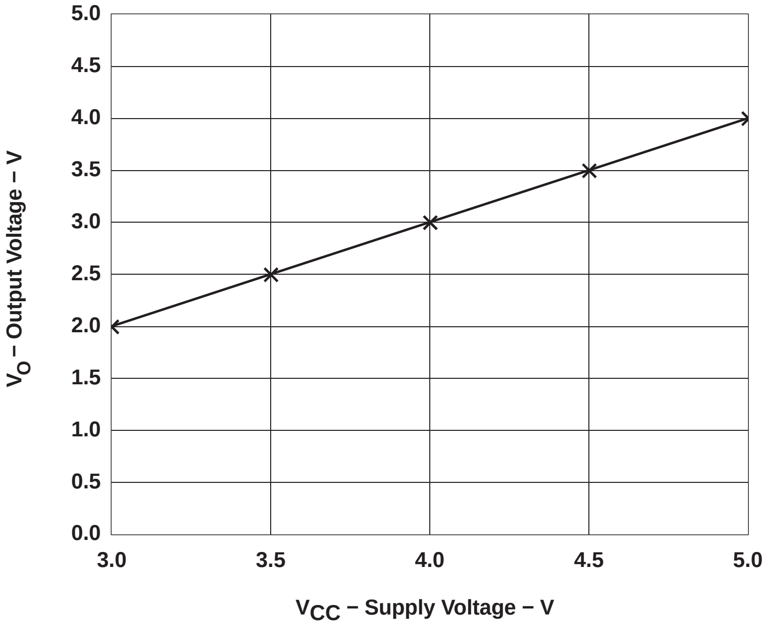


Figure 1. Output Voltage Versus Supply Voltage

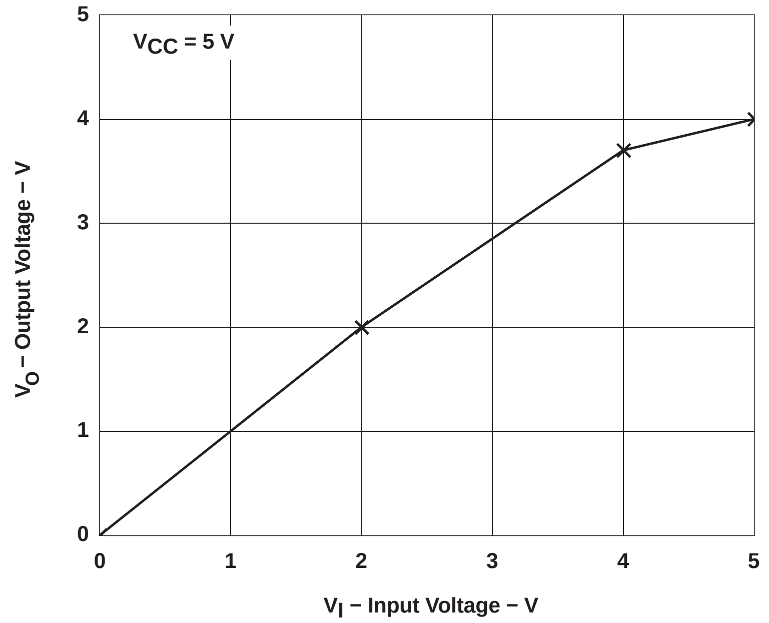


Figure 2. Output Voltage Versus Input Voltage

The on-state resistance (r_{on}) increases gradually with V_I until V_I approaches V_{CC} − 1 V, where r_{on} rapidly increases, clamping V_O at V_{CC} − 1 V (see Figure 3). Also, by the nature of the n-channel transistor design, the input and output terminals are fully isolated when the transistor is off. Leakage and capacitance are to ground and not between input and output, which minimizes feedthrough when the transistor is off.

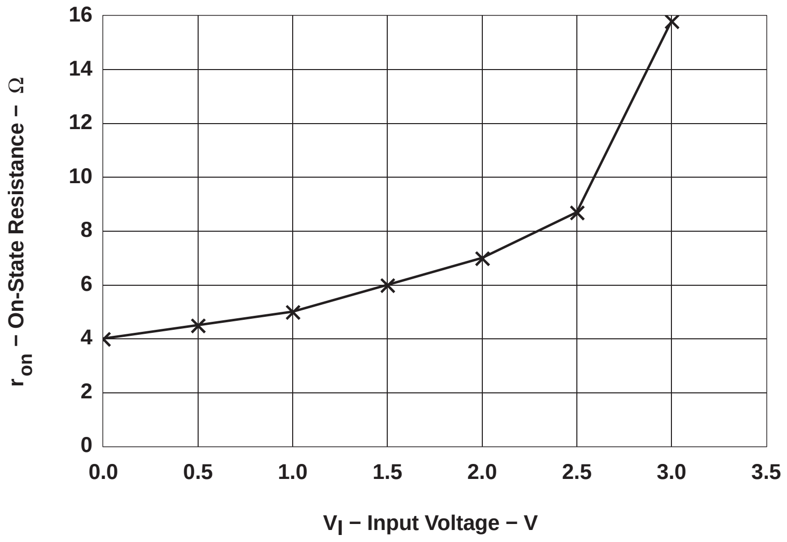


Figure 3. On-State Resistance Versus Input Voltage

Bus Switches Provide 5-V to 3-V Translation When 3-V Supply Line Is Not Provided

These devices also can provide bidirectional 5-V to 3-V translation with minimal propagation delay or direction control, using only a 5-V supply line and a diode. Figure 4 illustrates this application. A 4.3-V V_{CC} can be created by placing a diode between V_{CC} and the switch. This causes gate voltage of 4.3 V due to the diode drop of approximately 0.7 V. This drop, coupled with the gate-to-source drop of 1 V, brings V_O to a maximum 3.3-V level that can be used to drive a signal in a 3-V environment.

These devices consume very little current ($I_{CC} = 3\,\mu A$). This current is not satisfactory for the diode to operate. Using a resistor from the cathode of the diode to GND allows more current from the supply voltage, causing the diode to operate and to clamp at the specified 4.3 V (see Figure 4). The recommended value of the resistor is 1 kΩ or less.

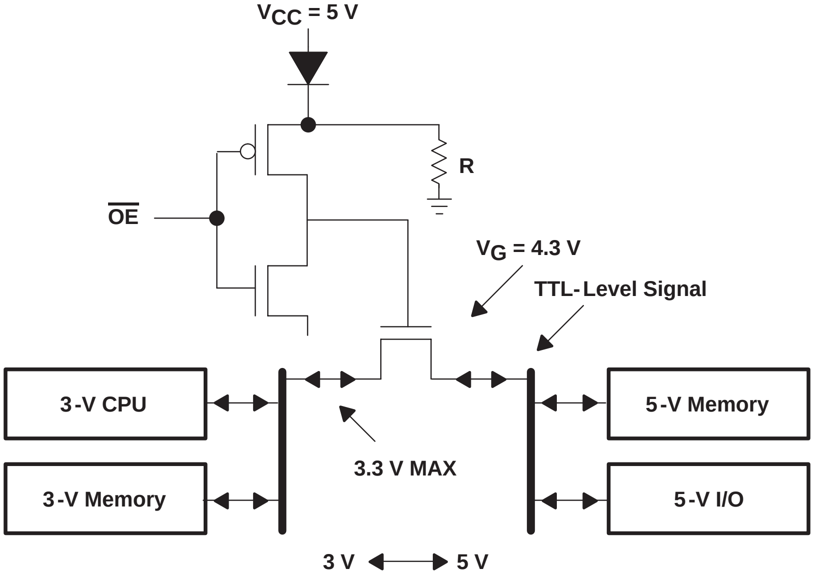


Figure 4. 5-V TTL to 3-V TTL Translator System

Bus Switches Can Be Used to Replace Drivers and Transceivers in Bus Applications

Bus switches introduce near-zero propagation delay. They can replace drivers and transceivers in systems in which signal buffering is not required. They can be used in a multiprocessor system as a fast bus connect, or they can be used as a bus-exchange switch for crossbar systems, ping-pong memory connect, or bus-byte swap. These devices also can replace relays that are used in automated test equipment (ATE) to connect or disconnect load resistors in negligible time with the same low on-state resistance and without relay-reliability problems.

Bus Switches Convert TTL Logic to Hot Card-Insertion Capability

This application is used mostly in systems that require hot card insertion or removal of cards without disturbing or loading down the bus. These systems are designed to run continuously and cannot be shut down for any reason, such as telephone switches, manufacturing controls, real-time transaction systems, and airline-reservation networks. These systems/cards use some logic families like ACL, HCMOS, etc., which do not provide isolation from the bus when power is partially removed, causing system error. Also, connectors are designed so that the ground pins are connected first, followed by the signal pins, then V_{CC} last. In this condition, the existing logic must ensure that the I/O signals do not disturb or load down the bus. This assurance cannot be achieved using CMOS logic since it contains p-channel transistors that provide an inherent diode between the I/O pins and V_{CC}. The diode is forward biased when driven above V_{CC} (see Figure 5). In a situation where V_{CC} is disconnected, these diodes are capable of pulling the system bus to approximately one diode drop above ground, leaving the bus disturbed.

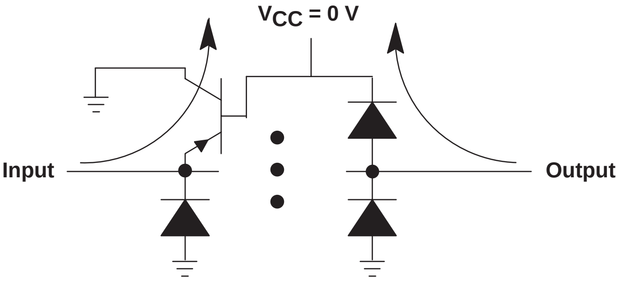


Figure 5. ACL Direction of Current Flow When V_{CC} = 0 V

Another issue to consider is that, when V_{CC} is ramping, but still below the device-operating voltage, the logic should ensure that the outputs are in the high-impedance state and that the bus is totally isolated until the card is ready for operation. Finally, the capacitance of the card must be seen by the system bus as low as possible so that when the card is inserted and the capacitance is charged up, disturbance or bus error does not occur.

There are two solutions to this problem; one is to use Texas Instruments BiCMOS technology (BCT) or advanced BiCMOS technology (ABT) families, since both ensure the input and output to be off when V_{CC} is removed due to the absence of the clamping diodes to V_{CC} (see Figure 6). They also provide an active circuit that ensures the output to be in the high-impedance state during part of the V_{CC} power up or power down.

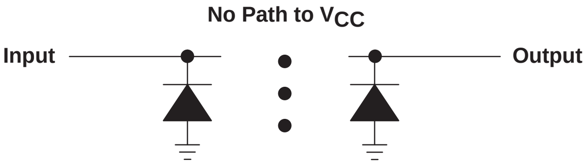


Figure 6. No ABT Current Flow When V_{CC} = 0 V

The second solution is to use the Texas Instruments CBT family. This can be done by placing the switch between the card logic and the connector to serve as an isolator when power is removed. The switch uses an n channel that prevents the current from flowing into the switch when powered down (see Figure 7). One device in particular, the SN74CBT6800, is designed specifically for hot card insertion. It has a built-in channel pullup tied to a bias voltage (BIASV) that is provided to ensure power up with the buses not connected. Other devices can be used in the same manner, however, to ensure the high-impedance state during power up or power down. The enable pins of the switch should be tied to V_{CC} through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver (see Figure 8).

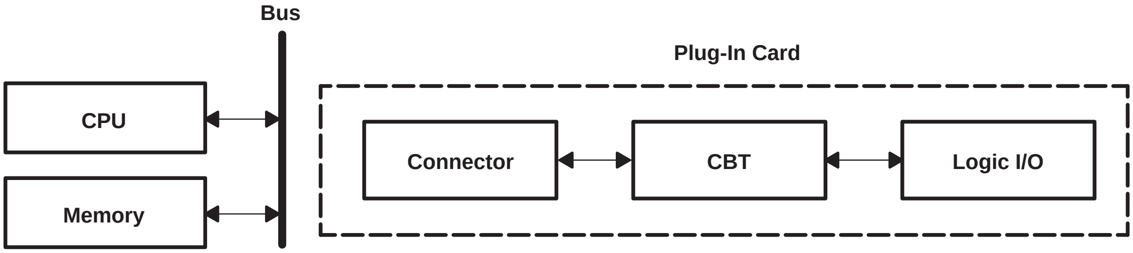
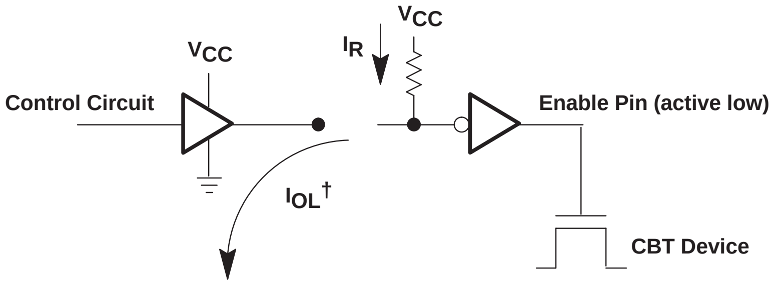


Figure 7. Hot Card-Insertion Application


V_{CC}
I_R
V_{CC}
Control Circuit
Enable Pin (active low)
I_{OL}†
CBT Device

† $I_{OL} > I_R$, so the control signal can override the pullup resistor.

Figure 8. Power-Up High-Impedance State With CBT

Conclusion

Texas Instruments crossbar switches can be used in several applications. Although they are simple n-channel transistors, they are capable of providing several important bus functions, such as hot card insertion, near-zero-delay communication, 5-V to 3-V translation, and memory management in multiprocessor environments.

Acknowledgment

The author of this document is Ramzi Ammar.

SN74CBTS3384 Bus Switches Provide Fast Connection and Ensure Isolation

SCDA002A
August 1996

Texas Instruments

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Introduction

Buses are the pathways for communication between the CPU, memory, and I/O ports in electronic systems. Today’s standards demand both fast connection as well as isolation of these buses. Bus switches are usually used to address these demands because the use of a single MOSFET provides negligible propagation delay, low power dissipation and bidirectional switching; however, the use of a single transistor also can allow large negative undershoots below −1 V to cause unwanted switching and possible disruption of the bus. To prevent this problem from occurring, the SN74CBTS3384 bus switches are developed with Schottky diodes at the inputs that clamp any undershoot to approximately −300 mV (see Figure 1).

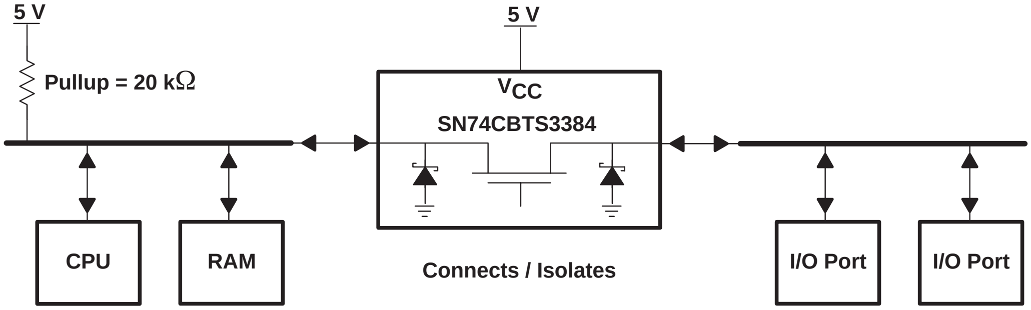
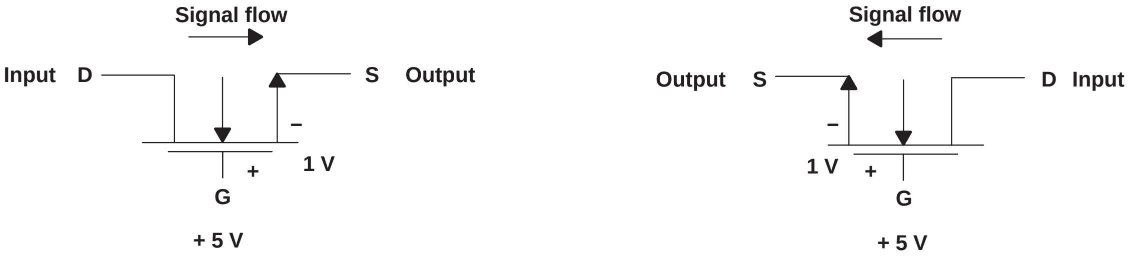


Figure 1. The SN74CBTS3384 With Schottky Diodes Attached at Both Ports

The Mechanics of the MOSFET Switch Leading to False Switching

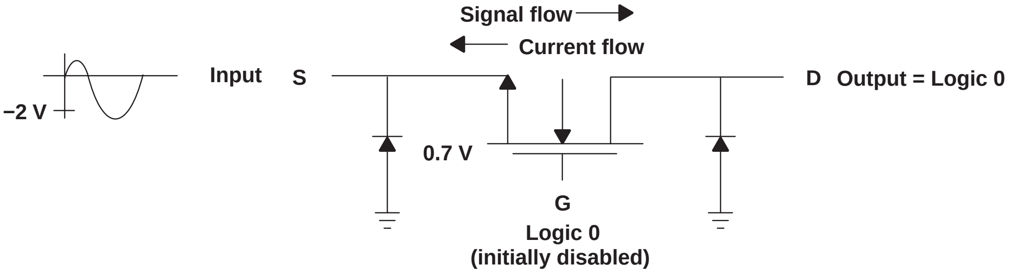
The MOSFET is used for bus switches because of its enabling and disabling speed, its low on-state resistance, and its high off-state resistance. The substrate of the N-channel MOSFET is grounded and the two n-type doped regions are interchangeable. As shown in Figure 2, when a logic high is applied to the gate, the region with a voltage of 1V or more below the gate becomes the source and the other region the drain. At this point, the switch turns fully on and a signal flows from the input side. While this physical structure of the MOSFET provides bidirectional capability in a switch, it also allows large negative undershoots on either port to turn on a disabled switch.



The interchangeability of the source and drain provides bidirectional signal flow.

Figure 2. Switching Mechanics of the NMOS Switch

As Figure 3 shows, even though the switch is initially disabled and there is a logic low at the gate, large negative undershoots at the input cause the existing clamping diode to clamp to approximately −650 mV. Since this voltage is parallel to the gate-to-source voltage of the transistor and lasts for a few nanoseconds, the transistor starts conducting a certain amount of current. This causes a logic low to appear on the bus and disrupts any signals on it.

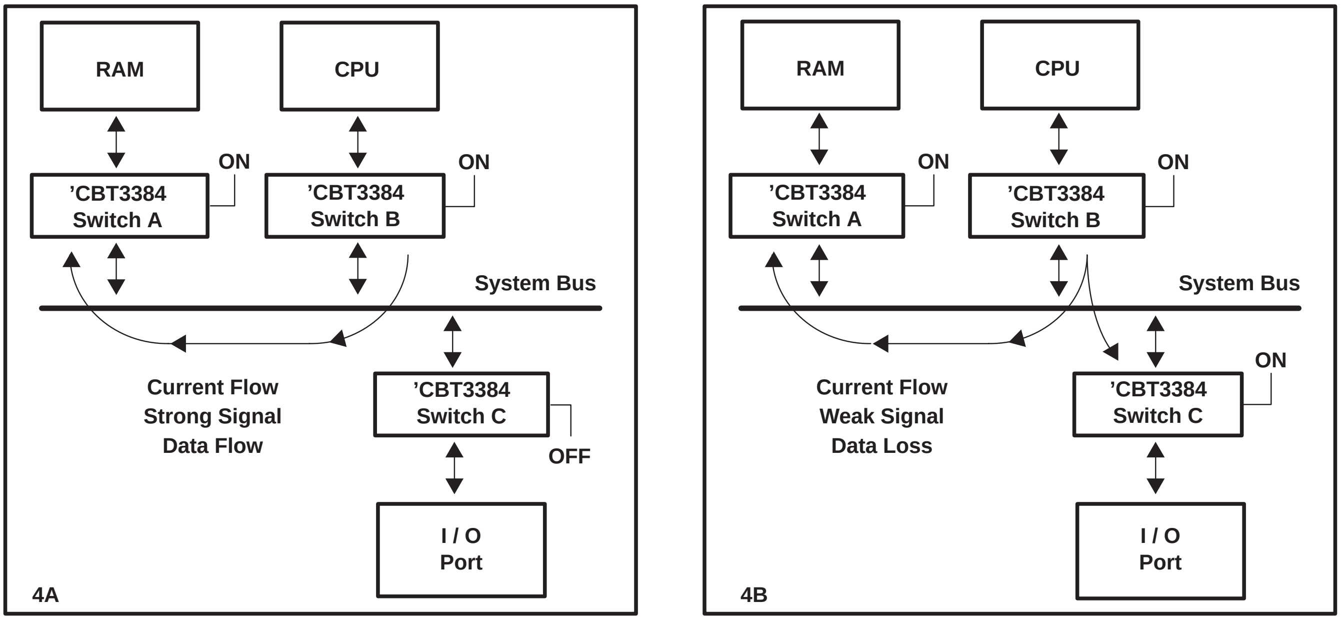

Signal flow
Current flow
Input
S
D
Output = Logic 0
−2 V
0.7 V
G
Logic 0
(initially disabled)

Output enable ($\overline{OE}$) is high, but large negative undershoot causes NMOS switch to turn on.

Figure 3. Mechanics Behind False Switching

Disruption of the Bus

False switching can disrupt the bus in many ways. Bus switches connect two buses or several components on a bus when on, and isolates them when off. Because each component has a certain amount of capacitance, an unexpected connection loads the bus with additional capacitance. Under normal circumstances, a signal is given enough drive to charge the expected capacitance on the bus and then switch voltage levels at the receiver. A signal propagating on the disrupted line may not have enough drive to overcome the additional load capacitance. In fact, the logic low introduced to the bus by the false connection can absorb some of the drive current from the signal. In any case, the end result is signal weakening, loss of speed, and failure to switch voltage levels at the receiver. Figure 4A shows a transaction between a CPU and a RAM chip connected by switches A and B. When switch C is off, the data flow is uninterrupted. As shown in Figure 4B, switch C can turn on unexpectedly and connect the I/O port to the bus. This results in signal degradation and data loss.


RAM
CPU
ON
'CBT3384
Switch A
ON
'CBT3384
Switch B
System Bus
Current Flow
Strong Signal
Data Flow
'CBT3384
Switch C
OFF
I / O
Port
4A
RAM
CPU
ON
'CBT3384
Switch A
ON
'CBT3384
Switch B
System Bus
ON
Current Flow
Weak Signal
Data Loss
'CBT3384
Switch C
I / O
Port
4B

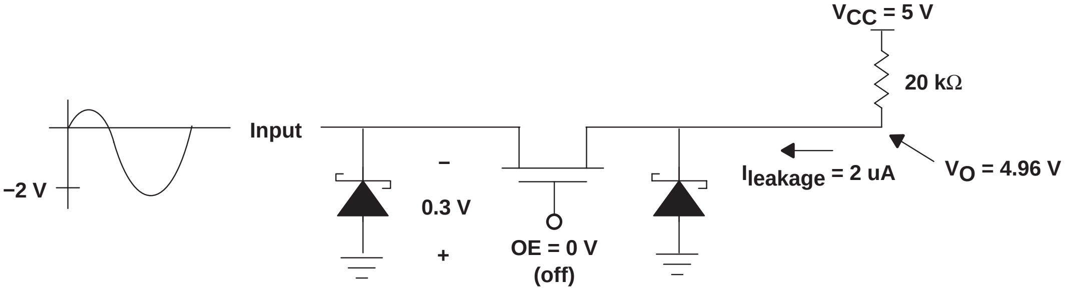
Uninterrupted data flow from CPU to RAM **Resulting bus interruption and data loss**

Figure 4. The Effect of Bus Interruption on Data Flow and Signal Integrity

False switching also can cause bus contention, a case occurring when two or more transmitters on a bus are active at the same time. If the logic levels of these outputs are different, a high current flows on the line, possibly damaging the line or the components connected to it. These problems can cause serious setbacks to the high performance and reliability demands of today's systems. The use of the SN74CBTS3384 bus switch helps prevent false switching and addresses many of these problems.

The SN74CBTS3384 Solution

The SN74CBTS3384 utilizes Schottky diode at the inputs to clamp undershoot to about 300 mV below ground (see Figure 5). With the gate grounded in the disabled state, the Schottky diode prevents the gate-to-source voltage from exceeding the threshold voltage of the NMOS transistor, thus preventing weak enabling. In addition, a disabled SN74CBTS3384 switch offers a very low capacitance of about 6 pF and very low leakage current. Figure 5 shows total leakage current of only 2 μA. As a result, the disabled SN74CBTS3384 bus switch succeeds in isolating its output from any unwanted undershoots at the input. The buses are left uninterrupted and the signals on the buses are not disturbed.



Test conditions showing output isolation

Figure 5. Test Conditions of the SN74CBTS3384 With Switch Disabled

Figure 6 shows the output of a disabled SN74CBT3384A (without Schottky diodes) as it turns on and follows the input to a negative level. This level is low enough to possibly disrupt the bus. Figure 6 also shows the SN74CBTS3384 where the Schottky diode prevents any switching throughout the wide input sweep and keeps the output at a steady level. Figure 7 shows the input current of the SN74CBTS3384 as the Schottky diode turns on, conducting about 10 mA from ground.

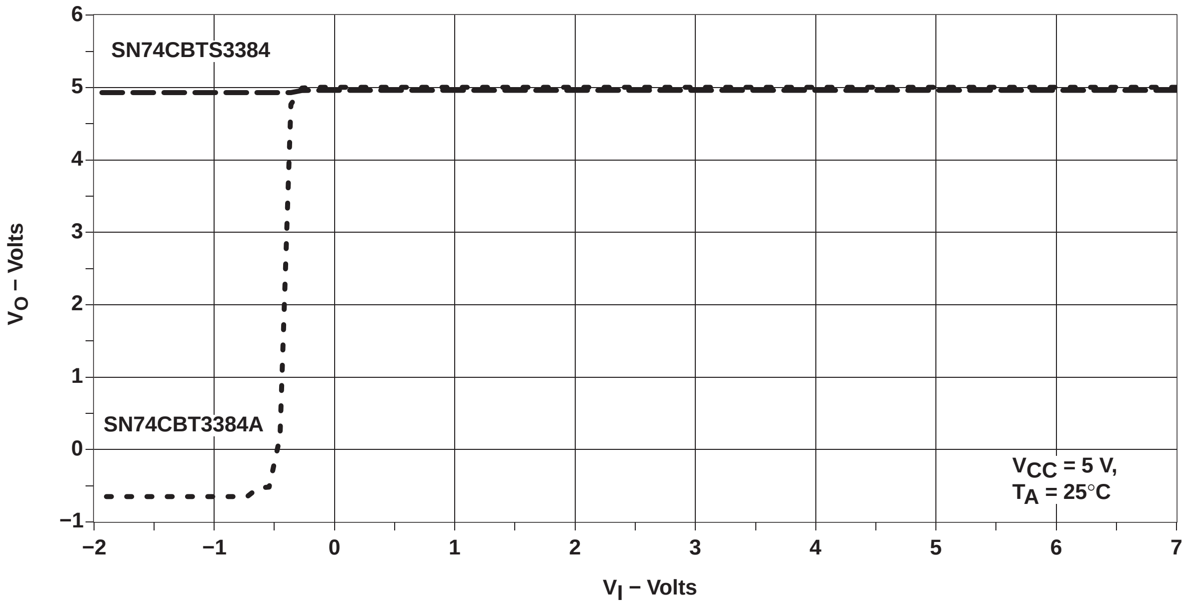


Figure 6. V_O vs V_I of the SN74CBTS3384 and a SN74CBT3384A in the Disabled State

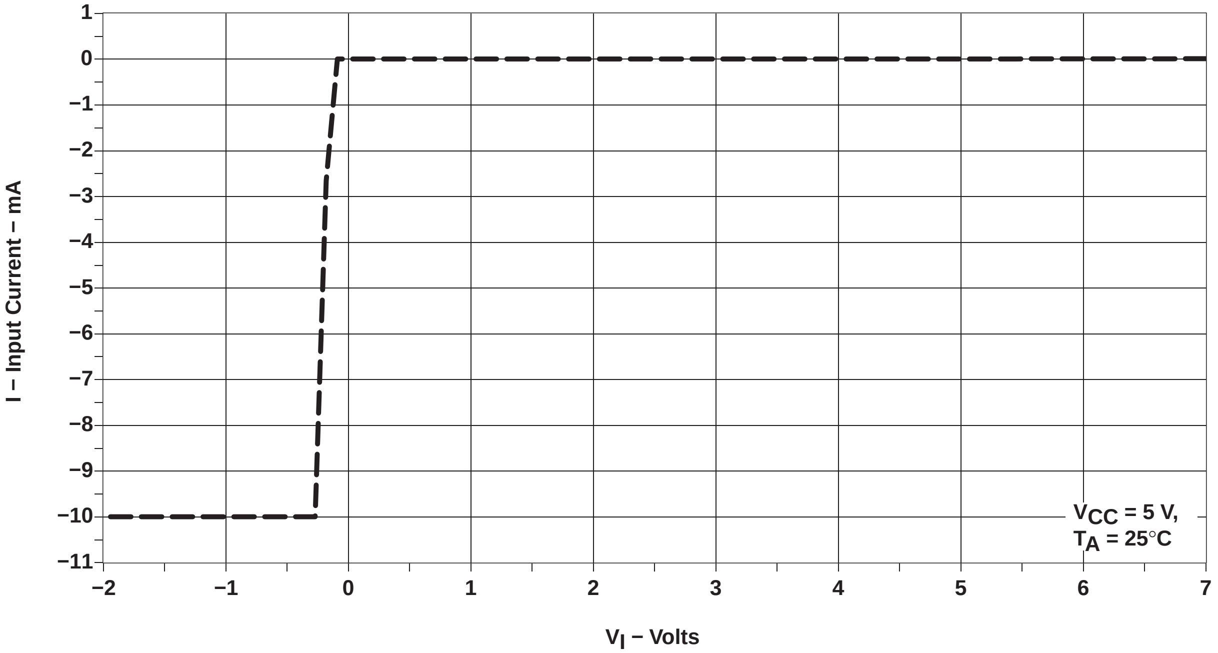


Figure 7. Input Current vs V_I of SN74CBTS3384 in the Disabled State

Conclusion

The SN74CBTS3384 bus switch provides a high-speed, low-power solution to bus connection, while providing a reliable solution to bus isolation. As a result, buses function properly without any problematic interruptions and the high-performance demands of today's systems are easily reached.

Acknowledgment

The author of this report is Nalin Yogasundram.

Implications of Slow or Floating CMOS Inputs

SCBA004C
February 1998

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Introduction

In recent years, CMOS (AC/ACT, AHC/AHCT, ALVC, CBT, CBTLV, HC/HCT, LVC, LV/LV-A) and BiCMOS (ABT, ALVT, BCT, FB, GTL, and LVT) logic families have further strengthened their position in the semiconductor market. New designs have adopted both technologies in almost every system that exists, whether it is a PC, a workstation, or a digital switch. The reason is obvious: power consumption is becoming a major issue in today's market. However, when designing systems using CMOS and BiCMOS devices, one must understand the characteristics of these families and the way inputs and outputs behave in systems. It is very important for the designer to follow all rules and restrictions that the manufacturer requires, as well as to design within the data-sheet specifications. Because data sheets do not cover the input behavior of a device in detail, this application report explains the input characteristics of CMOS and BiCMOS families in general. It also explains ways to deal with issues when designing with families in which floating inputs are a concern. Understanding the behavior of these inputs results in more robust designs and better reliability.

Characteristics of Slow or Floating CMOS Inputs

Both CMOS and BiCMOS families have a CMOS input structure. This structure is an inverter consisting of a p-channel to V_{CC} and an n-channel to GND as shown in Figure 1. With low-level input, the p-channel transistor is on and the n-channel is off, causing current to flow from V_{CC} and pulling the node to a high state. With high-level input, the n-channel transistor is on, the p-channel is off, and the current flows to GND, pulling the node low. In both cases, no current flows from V_{CC} to GND. However, when switching from one state to another, the input crosses the threshold region, causing the n-channel and the p-channel to turn on simultaneously, generating a current path between V_{CC} and GND. This current surge can be damaging, depending on the length of time that the input is in the threshold region (0.8 to 2 V). The supply current (I_{CC}) can rise to several milliamperes per input, peaking at approximately 1.5-V V_I (see Figure 2). This is not a problem when switching states within the data-sheet-specified input transition time limit specified in the recommended operating conditions table for the specific devices. Examples are shown in Figure 3.

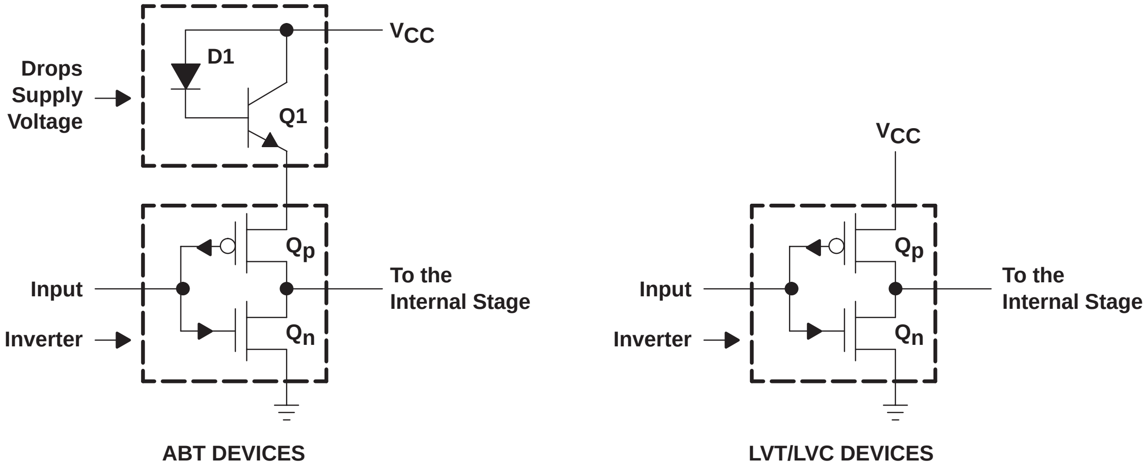

Figure 1. Input Structures of ABT and LVT/LVC Devices

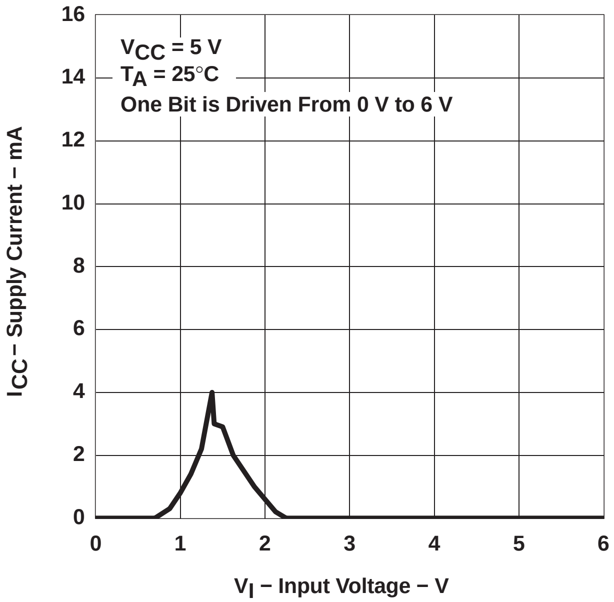

Figure 2. Supply Current Versus Input Voltage (One Input)

recommended operating conditions[†]

				MIN	MAX	UNIT
Δt/Δv	Input transition rise or fall rate	ABT octals			5	ns/V
		ABT Widebus™ and Widebus+™			10	
		AHC, AHCT			20	
		FB			10	
		LVT, LVC, ALVC, ALVT			10	
		LV			100	
		LV-A	V_{CC} = 2.3 V to 2.7 V		200	
			V_{CC} = 3 V to 3.6 V		100	
			V_{CC} = 4.5 V to 5.5 V		20	
t_t	Input transition (rise and fall) time	HC, HCT	V_{CC} = 2 V		1000	ns
			V_{CC} = 4.5 V		500	
			V_{CC} = 6 V		400	

[†] Refer to the latest TI data sheets for device specifications.

Figure 3. Input Transition Rise or Fall Rate as Specified in Data Sheets

Slow Input Edge Rate

With increased speed, logic devices have become more sensitive to slow input edge rates. A slow input edge rate, coupled with the noise generated on the power rails when the output switches, can cause excessive output errors or oscillations. Similar situations can occur if an unused input is left floating or is not actively held at a valid logic level.

These functional problems are due to voltage transients induced on the device's power system as the output load current (I_O) flows through the parasitic lead inductances during switching (see Figure 4). Because the device's internal power-supply nodes are used as voltage references throughout the integrated circuit, inductive voltage spikes, V_{GND}, affect the way signals appear to the internal gate structures. For example, as the voltage at the device's ground node rises, the input signal, V_I', appears to decrease in magnitude. This undesirable phenomenon can then erroneously change the output if a threshold violation occurs.

In the case of a slowly rising input edge, if the change in voltage at GND is large enough, the apparent signal, V_I', at the device appears to be driven back through the threshold and the output starts to switch in the opposite direction. If worst-case conditions prevail (simultaneously switching all of the outputs with large transient load currents), the slow input edge is repeatedly driven back through the threshold, causing the output to oscillate. Therefore, the maximum input transition time of the device should not be violated, so no damage to the circuit or the package occurs.

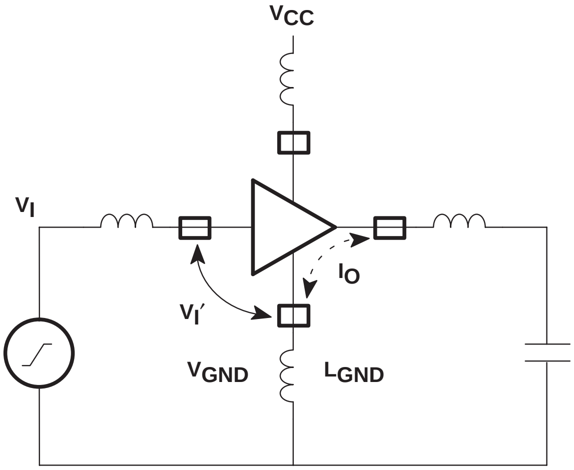

Figure 4. Input/Output Model

Floating Inputs

If a voltage between 0.8 V and 2 V is applied to the input for a prolonged period of time, this situation becomes critical and should not be ignored, especially with higher bit count and more dense packages (SSOP, TSSOP). For example, if an 18-bit transceiver has 36 I/O pins floating at the threshold, the current from V_{CC} can be as high as 150 mA to 200 mA. This is approximately 1 W of power consumed by the device, which leads to a serious overheating problem. This continuous overheating of the device affects its reliability. Also, because the inputs are in the threshold region, the outputs tend to oscillate, resulting in damage to the internal circuit over a long period of time. The data sheet shows the increase in supply current (ΔI_{CC}) when the input is at a TTL level [for ABT $V_I = 3.4$ V, $\Delta I_{CC} = 1.5$ mA (see Figure 5)]. This becomes more critical when the input is in the threshold region as shown in Figure 6.

These characteristics are typical for all CMOS input circuits, including microprocessors and memories.

For CBT or CBTLV devices, this applies to the control inputs. For FB and GTL devices, this applies to the control inputs and the TTL ports only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)†

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
ΔI_{CC}‡	ABT, AHCT	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND		1.5	mA
	CBT Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND		2.5	
ΔI_{CC}‡	CBTLV Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND		750	µA
ΔI_{CC}‡	LVT	V_{CC} = 3 V to 3.6 V,	One input at V_{CC} − 0.6 V,	Other inputs at V_{CC} or GND		0.2	mA
	LVC, ALVC, LV					0.5	

† Refer to the latest TI data sheets for device specifications.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Figure 5. Examples of Supply-Current Change of the Input at TTL Level as Specified in Data Sheets

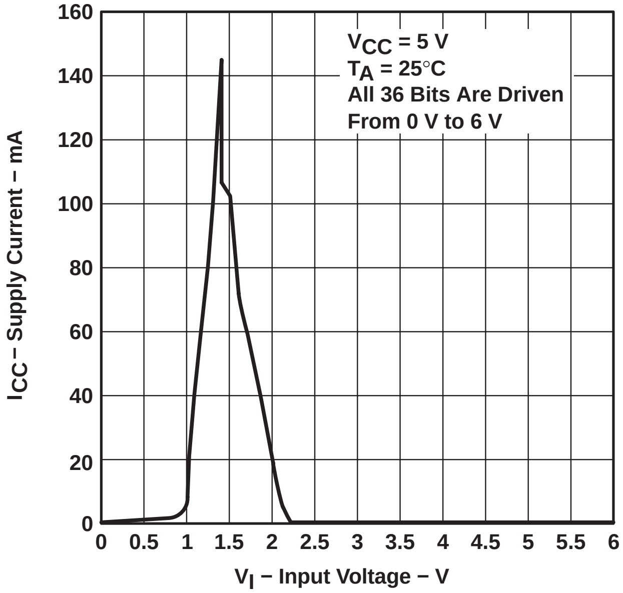

Figure 6. Supply Current Versus Input Voltage (36 Inputs)

As long as the driver is active in a transmission path or bus, the receiver’s input is always in a valid state. No input specification is violated as long as the rise and fall times are within the data-sheet limits. However, when the driver is in a high-impedance state, the receiver input is no longer at a defined level and tends to float. This situation can worsen when several transceivers share the same bus. Figure 7 is an example of a typical bus system. When all transceivers are inactive, the bus-line levels are undefined. When a voltage that is determined by the leakage currents of each component on the bus is reached, the condition is known as a *floating state*. The result is a considerable increase in power consumption and a risk of damaging all components on the bus. Holding the inputs or I/O pins at a valid logic level when they are not being used or when the part driving them is in the high-impedance state is recommended.

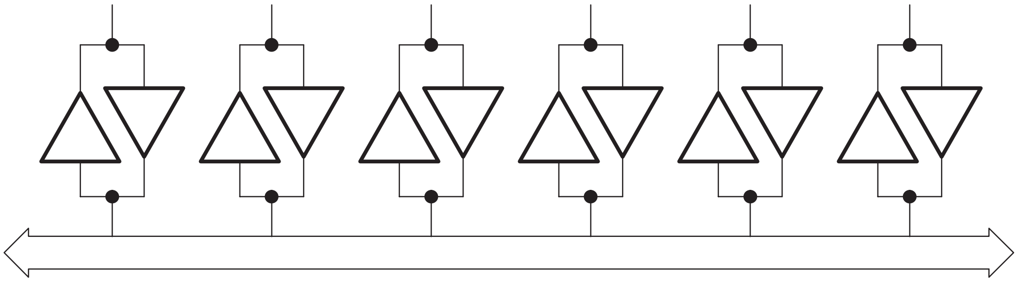

Figure 7. Typical Bidirectional Bus

Recommendations for Designing More-Reliable Systems

Bus Control

The simplest way to avoid floating inputs in a bus system is to ensure that the bus always is either active or inactive for a limited time when the voltage buildup does not exceed the maximum V_{IL} specification (0.8 V for TTL-compatible input). At this voltage, the corresponding I_{CC} value is too low and the device operates without any problem or concern (see Figures 2 and 4).

To avoid damaging components, the designer must know the maximum time the bus can float. First, assuming that the maximum leakage current is $I_{OZ} = 50\ \mu A$ and the total capacitance (I/O and line capacitance) is C = 20 pF, the change in voltage with respect to time on an inactive line that exceeds the 0.8-V level can be calculated as shown in equation 1.

$$\Delta V/\Delta t = \frac{I_{OZ}}{C} = \frac{50\ \mu A}{20\ pF} = 2.5\ V/\mu s \tag{1}$$

The permissible floating time for the bus in this example should be reduced to 320 ns maximum, which ensures that the bus does not exceed the 0.8-V level specified. The time constant does not change when multiple components are involved because their leakage currents and capacitances are summed.

The advantage of this method is that it requires no additional cost for adding special components. Unfortunately, this method does not always apply because buses are not always active.

Pullup or Pulldown Resistors

When buses are disabled for more than the maximum allowable time, other ways should be used to prevent components from being damaged or overheated. A pullup or a pulldown resistor to V_{CC} or GND, respectively, should be used to keep the bus in a defined state. The size of the resistor plays an important role and, if its resistance is not chosen properly, a problem may occur. Usually, a 1-kΩ to 10-kΩ resistor is recommended. The maximum input transition time must not be violated when selecting pullup or pulldown resistors (see Figure 3). Otherwise, components may oscillate, or device reliability may be affected.

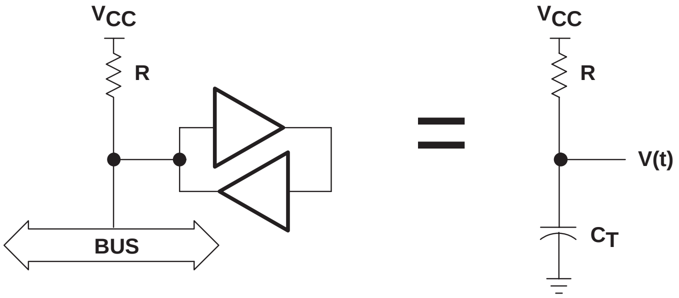

Figure 8. Inactive-Bus Model With a Defined Level

Assume that an active-low bus goes to the high-impedance state as modeled in Figure 8. C_T represents the device plus the bus-line capacitance and R is a pullup resistor to V_{CC}. The value of the required resistor can be calculated as shown in equation 2.

$$V(t) = V_{CC} - [e^{-t/RC_T} (V_{CC} - V_i)] \tag{2}$$

Where:

$V(t)$ = 2 V, minimum voltage at time t
V_i = 0.5 V, initial voltage
V_{CC} = 5 V
C_T = total capacitance
R = pullup resistor
t = maximum input rise time as specified in the data sheets (see Figure 3).

Solving for R, the equation becomes:

$$R = \frac{t}{0.4 \times C_T} \tag{3}$$

For multiple transceivers on a bus:

$$R = \frac{t}{0.4 \times C \times N} \tag{4}$$

Where:

C = individual component and trace capacitance
N = number of components connected to the bus

Assuming that there are two components connected to the bus, each with a capacitance C = 15 pF, requiring a maximum rise time of 10 ns/V and t = 15-ns total rise time for the input (2 V), the maximum resistor size can be calculated:

$$R = \frac{15\text{ ns}}{0.4 \times 15\text{ pF} \times 2} = 1.25\text{ k}\Omega \tag{5}$$

This pullup resistor method is recommended for ac-powered systems; however, it is not recommended for battery-operated equipment because power consumption is critical. Instead, use the bus-hold feature that is discussed in the next section. The overall advantage of using pullup resistors is that they ensure defined levels when the bus is floating and help eliminate some of the line reflections, because resistors also can act as bus terminations.

Bus-Hold Circuits

The most effective method to provide defined levels for a floating bus is to use Texas Instruments (TI™) built-in bus-hold feature on selected families or as an external component like the SN74ACT1071 and SN74ACT1073 (refer to Table 1).

Table 1. Devices With Bus Hold

DEVICE TYPE	BUS HOLD INCORPORATED
SN74ACT1071	10-bit bus hold with clamping diodes
SN74ACT1073	16-bit bus hold with clamping diodes
ABT Widebus+ (32 and 36 bit)	All devices
ABT Octals and Widebus	Selected devices only
AHC/AHCT Widebus	TBA (Selected devices only)
Low Voltage (LVT and ALVC)	All devices
LVC Widebus	All devices

Bus-hold circuits are used in selected TI families to help solve the floating-input problem and eliminate the need for pullup and pulldown resistors. Bus-hold circuits consist of two back-to-back inverters with the output fed back to the input through a resistor (see Figure 9). To understand how the bus-hold circuit operates, assume that an active driver has switched the line to a high level. This results in no current flowing through the feedback circuit. Now, the driver goes to the high-impedance state and the bus-hold circuit holds the high level through the feedback resistor. The current requirement of the bus-hold circuit is determined only by the leakage current of the circuit. The same condition applies when the bus is in the low state and then goes inactive.

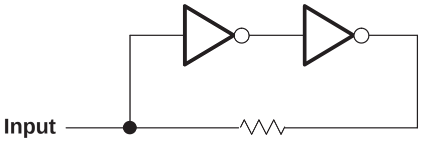

Figure 9. Typical Bus-Hold Circuit

As mentioned previously in this section, TI offers the bus-hold capability as stand-alone 10-bit and 16-bit devices (SN74ACT1071 and SN74ACT1073) with clamping diodes to V_{CC} and GND for added protection against line reflections caused by impedance mismatch on the bus. Because purely ohmic resistors cannot be implemented easily in CMOS circuits, a configuration known as a transmission gate is used as the feedback element (see Figure 10). An n-channel and a p-channel are arranged in parallel between the input and the output of the buffer stage. The gate of the n-channel transistor is connected to V_{CC} and the gate of the p-channel is connected to GND. When the output of the buffer is high, the p-channel is on, and when the output is low, the n-channel is on. Both channels have a relatively small surface area — the on-state resistance from drain to source, R_{dson}, is about 5 kΩ.

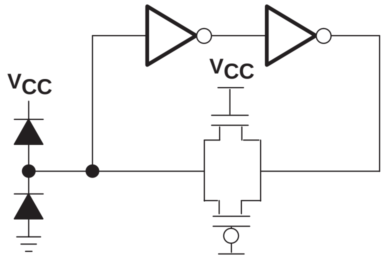

Figure 10. Stand-Alone Bus-Hold Circuit (SN74ACT107x)

Assume that in a practical application the leakage current of a driver on a bus is I_{OZ} = 10 µA and the voltage drop across the 5-kΩ resistance is V_D = 0.8 V (this value is assumed to ensure a defined logic level). Then, the maximum number of components that a bus-hold circuit can handle is calculated as follows:

$$N = \frac{V_D}{I_{OZ} \times R} = \frac{0.8\ \text{V}}{10\ \mu\text{A} \times 5\ \text{k}\Omega} = 16\ \text{components} \tag{6}$$

The 74ACT1071 and 74ACT1073 also provide clamping diodes as an added feature to the bus-hold circuit. These diodes are useful for clamping any overshoot or undershoot generated by line reflections. Figure 11 shows the characteristics of the diodes when the input voltage is above V_{CC} or below GND. At $V_I = -1$V, the diode can source about 50 mA, which can help eliminate undershoots. This can be very useful when noisy buses are a concern.

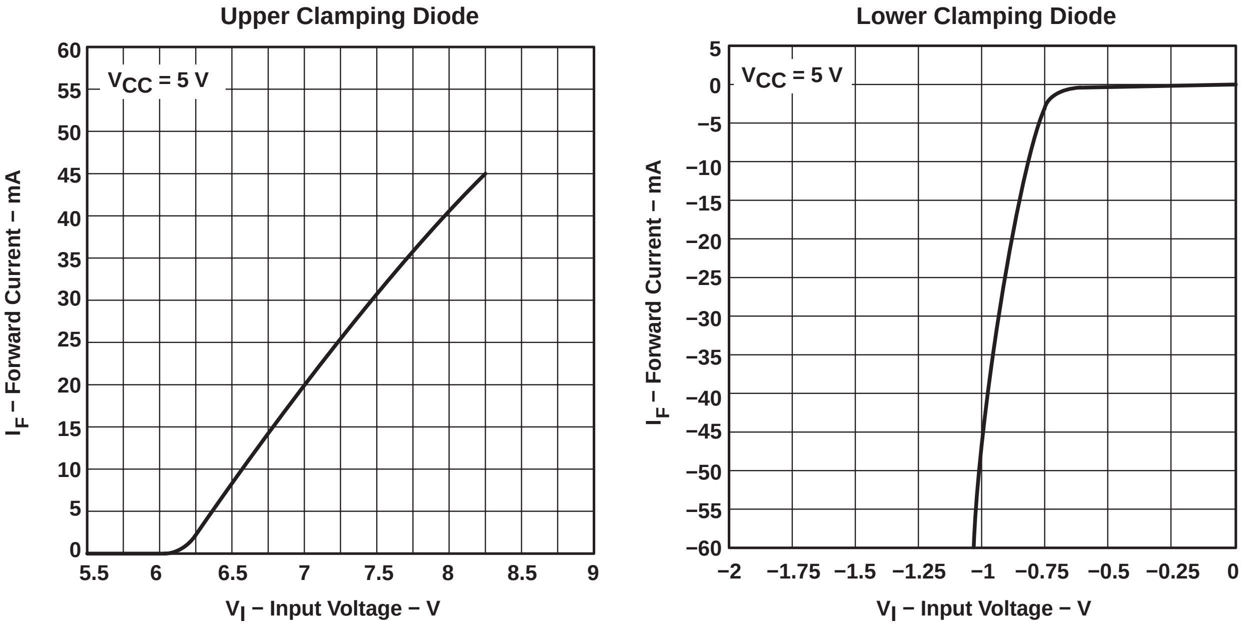

Figure 11. Diode Characteristics (SN74ACT107x)

TI also offers the bus-hold circuit as a feature added to some of the advanced-family drivers and receivers. This circuit is similar to the stand-alone circuit, with a diode added to the drain of the second inverter (ABT and LVT only, see Figure 12). The diode blocks the overshoot current when the input voltage is higher than V_{CC} ($V_I > V_{CC}$), so only the leakage current is present. This circuit uses the device's input stage as its first inverter; a second inverter creates the feedback feature. The calculation of the maximum number of components that the bus-hold circuit can handle is similar to the previous example. However, the advantage of this circuit over the stand-alone bus-hold circuit is that it eliminates the need for external components or resistors that occupy more area on the board. This becomes critical for some designs, especially when wide buses are used. Also, because cost and board-dimension restrictions are a major concern, designers prefer the easy fix: drop-in replaceable parts. TI offers this feature in most of the commonly used functions in several families (refer to Table 1 for more details).

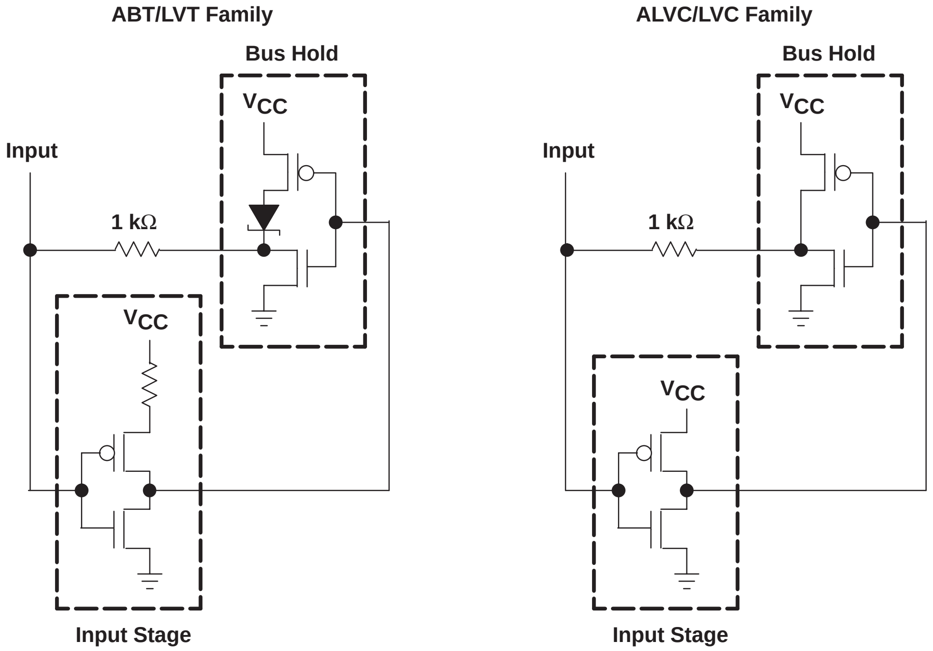

Figure 12. Input Structure of ABT/LVT and ALVC/LVC Families With Bus-Hold Circuit

Figure 13 shows the input characteristics of the bus-hold circuit at 3.3-V and 5-V operations, as the input voltage is swept from 0 to 5 V. These characteristics are similar in behavior to a weak driver. This driver sinks current into the part when the input is low and sources current out of the part when the input is high. When the voltage is near the threshold, the circuit tries to switch to the other state, always keeping the input at a valid level. This is the result of the internal feedback circuit. The plot also shows that the current is at its maximum when the input is near the threshold. $I_{I(hold)}$ maximum is approximately 25 µA for 3.3-V input and 400 µA for 5-V input.

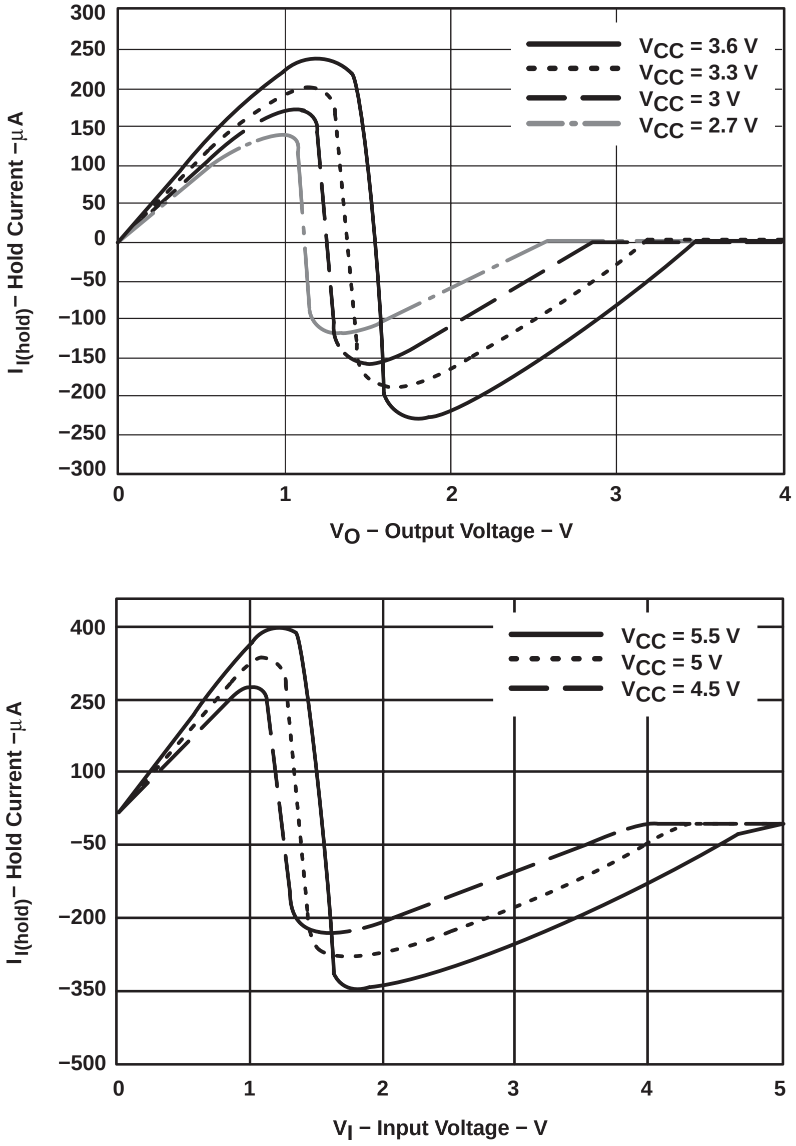

Figure 13. Bus-Hold Input Characteristics

When multiple devices with bus-hold circuits are driven by a single driver, there may be some concern about the ac switching capability of the driver becoming weaker. As small drivers, bus-hold circuits require an ac current to switch them. This current is not significant when using TI CMOS and BiCMOS families. Figure 14 shows a 4-mA buffer driving six LVTH16244 devices. The trace is a 75-Ω transmission line. The receivers are separated by 1cm, with the driver located in the center of the trace. Figure 15 shows the bus-hold loading effect on the driver when connected to six receivers switching low or high. It also shows the same system with the bus-hold circuit disconnected from the receivers. Both plots show the effect of bus hold on the driver’s rise and fall times. Initially, the bus-hold circuit tries to counteract the driver, causing the rise or fall time to increase. Then, the bus-hold circuit changes states (note the crossover point), which helps the driver switch faster, decreasing the rise or fall time.

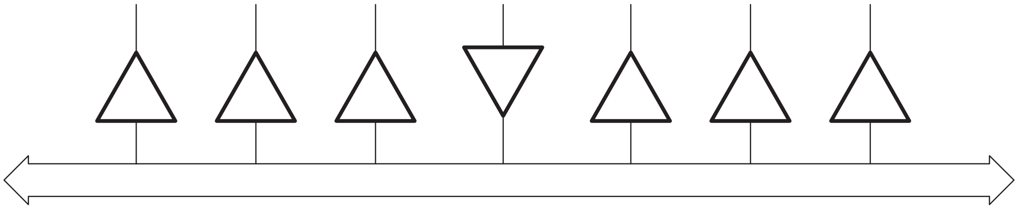

Figure 14. Driver and Receiver System

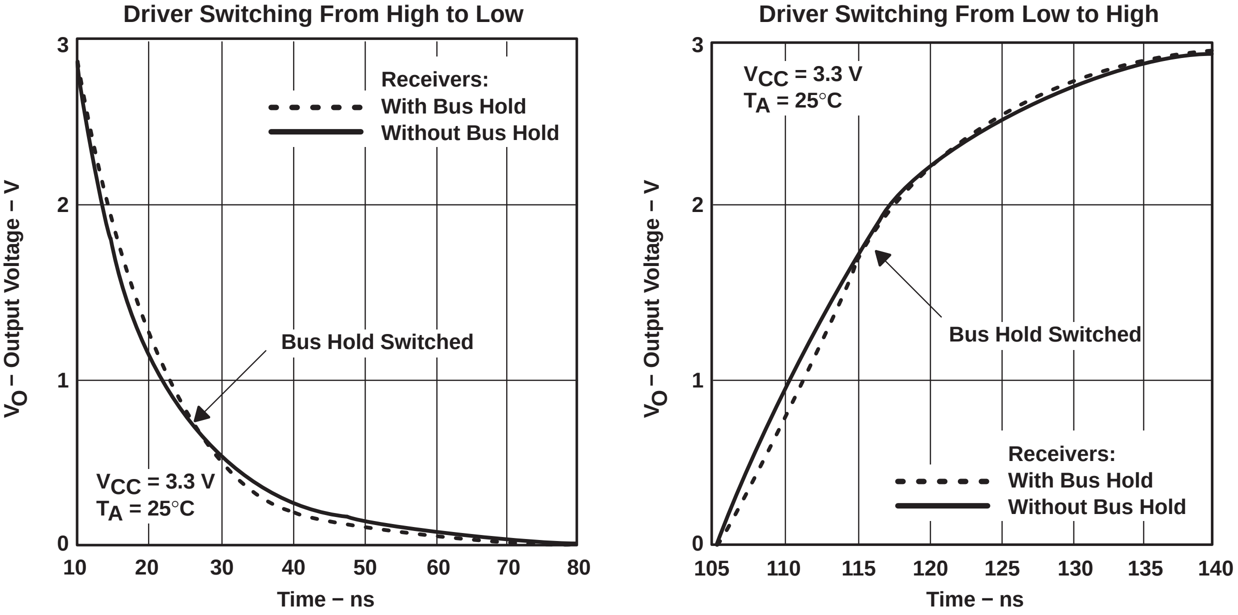

Figure 15. Output Waveforms of Driver With and Without Receiver Bus-Hold Circuit

Figure 16 shows the supply current (I_{CC}) of the bus-hold circuit as the input is swept from 0 to 5 V. The spike at about 1.5-V V_I is due to both the n-channel and the p-channel conducting simultaneously. This is one of the CMOS transistor characteristics.

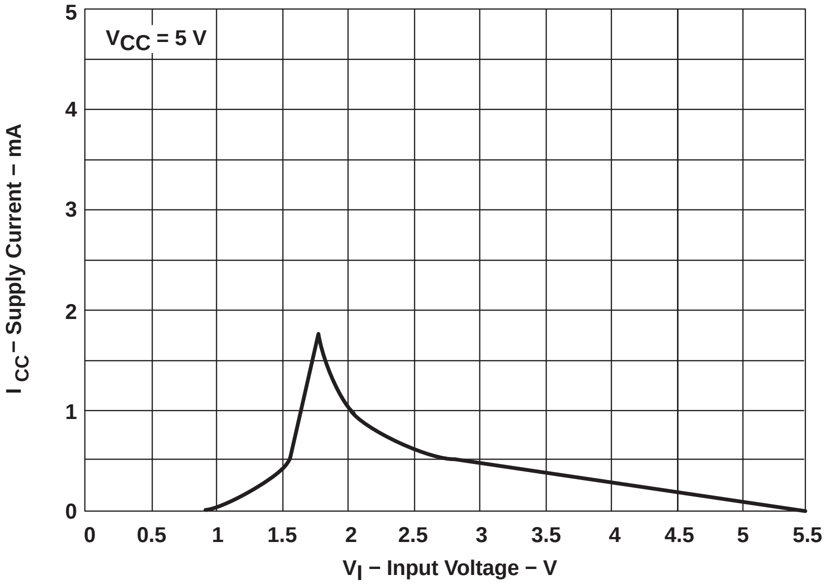

Figure 16. Bus-Hold Circuit Supply Current Versus Input Voltage

The power consumption of the bus-hold circuit is minimal when switching the input at higher frequencies. Figure 17 shows the power consumed by the input at different frequencies, with or without bus hold. The increase in power consumption of the bus-hold circuit at higher frequencies is not significant enough to be considered in power calculations.

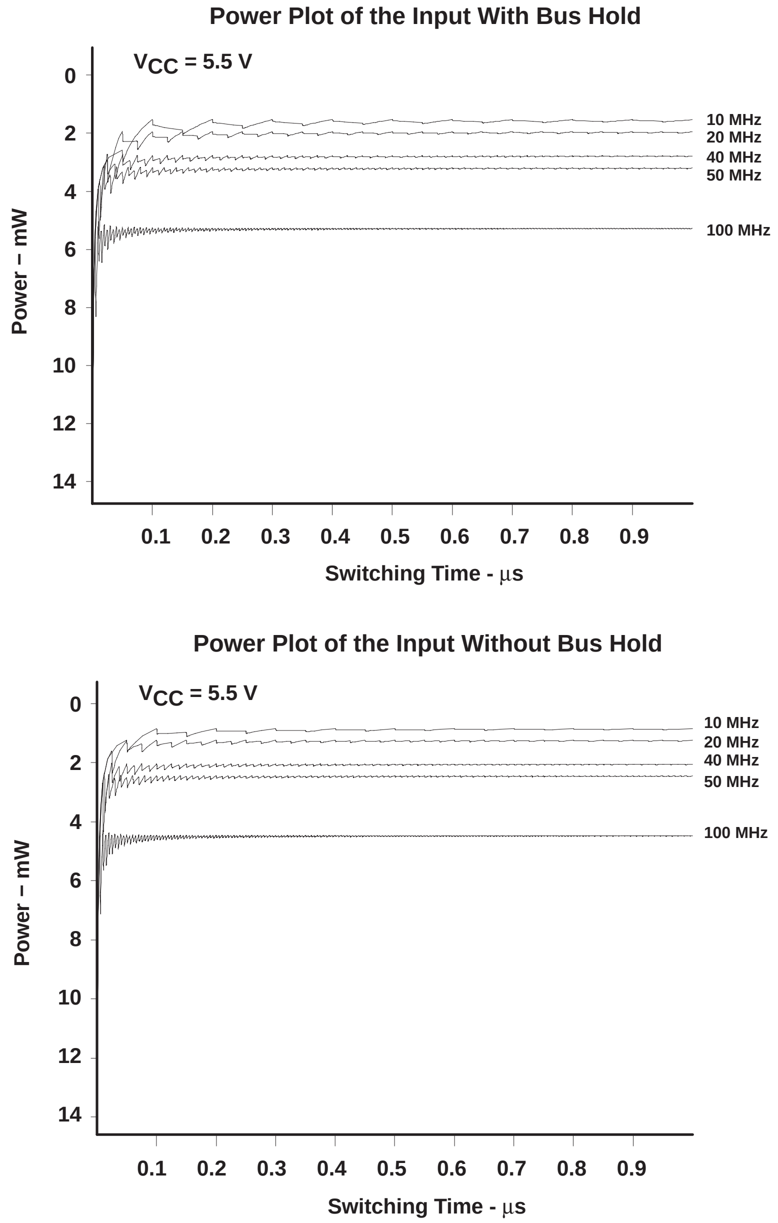

Figure 17. Input Power With and Without Bus Hold at Different Frequencies

Figure 18 shows the data-sheet dc specifications for bus hold. The first test condition is the minimum current required to hold the bus at 0.8 V or 2 V. These voltages meet the specified low and high levels for TTL inputs. The second test condition is the maximum current that the bus-hold circuit sources or sinks at any input voltage between 0 V and 3.6 V (for low-voltage families) or between 0 V and 5.5 V (for ABT). The bus-hold current becomes minimal as the input voltage approaches the rail voltage. The output leakage currents, I_{OZH} and $I_{OZL,}$ are insignificant for transceivers with bus hold because a true leakage test cannot be performed due to the existence of the bus-hold circuit. Because the bus-hold circuit behaves as a small driver, it tends to source or sink a current that is opposite in direction to the leakage current. This situation is true for transceivers with the bus-hold feature only and does not apply to buffers. All LVT, ABT Widebus+, and selected ABT octal and Widebus devices have the bus-hold feature (refer to Table 1 or contact the local TI sales office for more information).

electrical characteristics over recommended operating free-air temperature range (for families with bus-hold feature)†

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
$I_{I(hold)}$	Data inputs or I/Os	LVT, LVC, ALVC	V_{CC} = 3 V	V_I = 0.8 V	75		µA
				V_I = 2 V	−75		
		LVC, ALVC	V_{CC} = 3.6 V,	V_I = 0 to 3.6 V		±500	
		ABT Widebus+ and selected ABT	V_{CC} = 4.5 V	V_I = 0.8 V	100		
				V_I = 2 V	−100		
I_{OZH}/I_{OZL}	Transceivers with bus hold	ABT	This test is not a true I_{OZ} test because bus hold always is active on an I/O pin. Bus hold tends to supply a current that is opposite in direction to the output leakage current.			±1	µA
		LVT, LVC, ALVC					
	Buffers with bus hold	ABT	This test is a true I_{OZ} test since bus hold does not exist on an output pin.			±10	
		LVT, LVC, ALVC				±5	

† Refer to the latest TI data sheets for device specifications.

Figure 18. Example of Data-Sheet Minimum Specification for Bus Hold

Summary

Floating inputs and slow rise and fall times are important issues to consider when designing with CMOS and advanced BiCMOS families. It is important to understand the complications associated with floating inputs. Terminating the bus properly plays a major role in achieving reliable systems. The three methods recommended in this application report should be considered. If it is not possible to control the bus directly, and adding pullup or pulldown resistors is impractical due to power-consumption and board-space limitations, bus hold is the best choice. TI designed bus hold to reduce the need for resistors used in bus designs, thus reducing the number of components on the board and improving the overall reliability of the system.

Voltage Translation (5 V, 3.3 V, 2.5 V, 1.8 V), Switching Standards, and Bus Contention

SCYA006
September 1999

TEXAS INSTRUMENTS

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Abstract

Voltage translation is required because many analog devices operate at 5-V V_{CC}, but most digital products operate at 3.3-V V_{CC}, or lower. Interfaces between devices must consider issues such as driver and receiver switching compatibility and bus contention. Texas Instruments (TI™) offers a variety of products that provide translation among 5-V, 3-V, 2.5-V, and 1.8-V devices.

Introduction

In today's applications there are many mixed-voltage designs that require voltage translation between different levels. Many analog products still operate at 5-V V_{CC}, whereas, most digital products have migrated to 3.3-V V_{CC}, or lower. TI's logic devices are ideal for these types of situations. This application report explains how to utilize TI logic products for both CMOS and TTL voltage translations.

Switching Compatibility Between Drivers and Receivers

To have switching compatibility between a driver and a receiver, the output of the driver must be compliant with the input of the receiver. To establish a low signal at the receiver, V_{OL} of the driver should be less than or equal to V_{IL} of the receiver. To establish a high signal at the receiver, V_{OH} of the driver should be greater than or equal to V_{IH} of the receiver (see Figure 1).

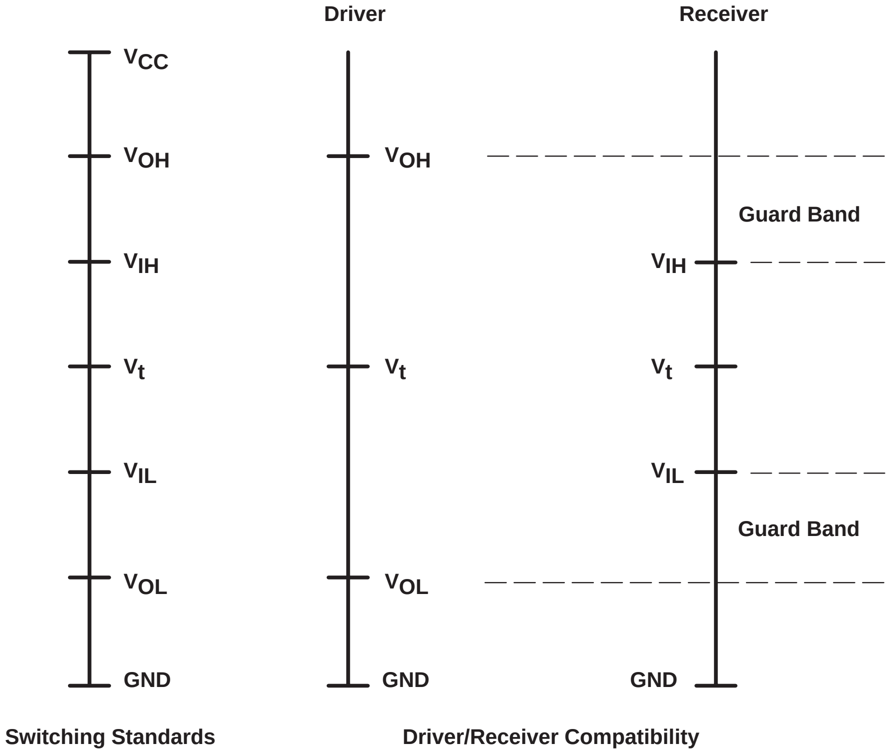

Figure 1. Switching Standards

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The guard band is the difference between the V_{OH} of the driver and the V_{IH} of the receiver and the difference between the V_{OL} of the driver and the V_{IL} of the receiver.

The threshold voltage (V_t) is the transition voltage where both the PMOS and NMOS transistors of the input stage may be turned on at the same time. At this level there is no valid signal level, and the device is unstable.

For CMOS devices, when both transistors are fully and/or partially turned on, there is a low-resistance current path from V_{CC} to ground that results in high power dissipation. When switching from low to high or high to low, the voltage passes through the threshold; however, it is not recommended that the input voltage of the receiver remains at the threshold region. This may cause a high surge of current drain that can damage the input and destroy the device (see Figure 2). A good practice is to keep the signal levels at the recommended operating conditions (above V_{IH} or below V_{IL} of the receiver).

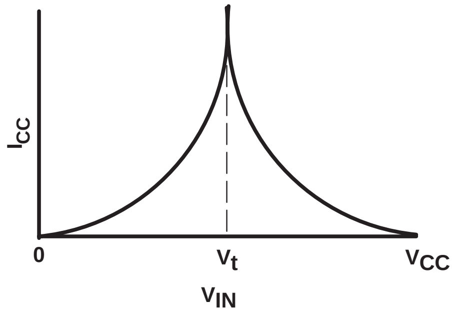


Figure 2. V_{IN} vs I_{CC}

As shown in Figure 2, the current consumption is the lowest at V_{IN} equal to 0 V or V_{CC}, and highest at the threshold voltage (V_t). Therefore, the power dissipation is lower when input voltages are at V_{CC} or ground. Refer to I_{CC} and ΔI_{CC} specification in the data sheet.

Product Families and Switching Standards

Figure 3 shows the switching standards for TI logic families.

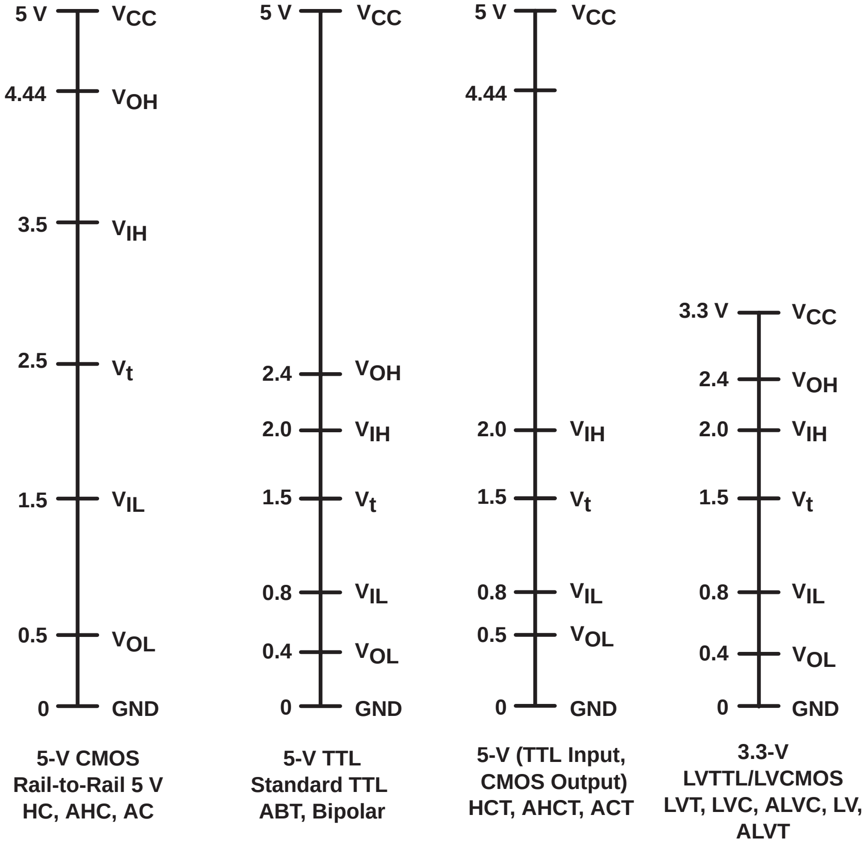

5 V
VCC
4.44
VOH
3.5
VIH
2.5
Vt
1.5
VIL
0.5
VOL
0
GND
5-V CMOS
Rail-to-Rail 5 V
HC, AHC, AC
5 V
VCC
2.4
VOH
2.0
VIH
1.5
Vt
0.8
VIL
0.4
VOL
0
GND
5-V TTL
Standard TTL
ABT, Bipolar
5 V
VCC
4.44
2.0
VIH
1.5
Vt
0.8
VIL
0.5
VOL
0
GND
5-V (TTL Input,
CMOS Output)
HCT, AHCT, ACT
3.3 V
VCC
2.4
VOH
2.0
VIH
1.5
Vt
0.8
VIL
0.4
VOL
0
GND
3.3-V
LVTTL/LVCMOS
LVT, LVC, ALVC, LV,
ALVT

Figure 3. Comparison of Switching Standards

Frequently asked questions about switching standards are:

Do 3.3-V LVTTL and 3.3-V LVCMOS have the same switching standards?

Yes, 3.3-V LVTTL and 3.3-V LVCMOS have the same switching standards.

Which switching standards are compatible?

5-V TTL and 3.3-V (LVTTL and LVCMOS) have the same switching standards for V_{OL}, V_{IL}, V_{IH}, and V_{OH}. The only difference is V_{CC}.

Is 5-V CMOS compatible with 5-V TTL or 3.3-V LVTTL/LVCMOS?

In most cases, no, because V_{IH} for 5-V CMOS is 3.5 V. The exceptions are the HCT, AHCT, and ACT devices, which have TTL-input and CMOS-output compatibility.

Where do TI logic families fit in?

5-V CMOS inputs and outputs:	HC, AHC, and AC
5-V TTL inputs and outputs:	ABT and bipolar
5-V TTL inputs and 5-V CMOS outputs:	AHCT, HCT, and ACT
3.3-V CMOS and LVTTL:	LVC, ALVC, LV, LVT, ALVT, AVC, and AHC

Unidirectional Voltage Translations

Voltage Translation From 3.3-V LVTTL/LVCMOS to 5-V TTL

Because all TI 3.3-V logic devices are output compatible with 5-V TTL, this voltage translation can be done with TI 3.3-V families, such as LVT, LVC, ALVC, LV, ALVT, AHC, HC, and AVC (see Figure 4).

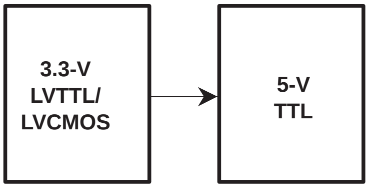


Figure 4. 3.3-V LVTTL/LVCMOS to 5-V TTL

Voltage Translation From 5-V TTL to 3.3-V LVTTL/LVCMOS

Because the 5-V TTL and 3.3-V LVTTL/LVCMOS switching standards are compatible, except for the V_{CC}, this translation can be done with TI 3.3-V logic families that have 5-V tolerant inputs, such as LVC, AHC, LVT, and ALVT. These logic families do not have a diode to V_{CC}, which was formerly used for electrostatic-discharge (ESD) protection (see Figure 5).

The diode to V_{CC} results in a current conduction at 3.3 V + 0.5 V_{be}. The resulting effects from the diode are:

- Clamping the driving signal at 3.3 V plus the diode drop
- Pulling the 3.3-V supply to a higher voltage (which may violate the data-sheet specification)
- Powering up a device that was intended to be powered down

Therefore, TI's 5-V-tolerant low-voltage families do not have this diode to V_{CC} and can be used in this voltage translation. They have other methods for ESD protection.

TI's CBTD or CBT with an external diode also can be used for 5-V TTL to 3.3-V LVTTL/LVCMOS translation.

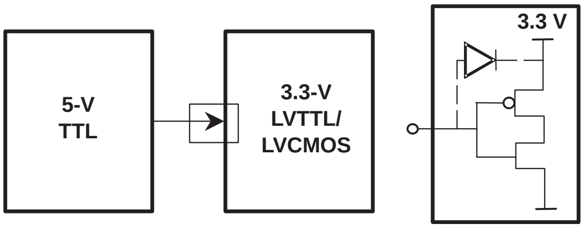


Figure 5. 5-V TTL to 3.3-V LVTTL/LVCMOS

Voltage Translation From 5-V CMOS to 3.3-V LVTTL/LVCMOS

This voltage translation can be done if the TI 3.3-V logic device is 5-V tolerant on the inputs, such as LVC, AHC, LVT, and ALVT (see Figure 6).

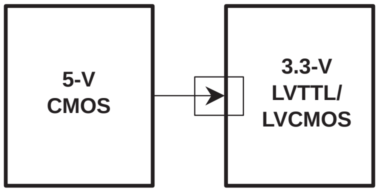


Figure 6. 5-V CMOS to 3.3-V LVTTL/LVCMOS

Voltage Translation From 3.3-V LVTTL/LVCMOS to 5-V CMOS

The 5-V CMOS V_{IH} is 3.5 V, which is above the V_{OH} of the 3.3-V devices. Therefore, a standard 3.3-V device cannot achieve this type of translation. TI has split-rail transceivers that have two voltage supplies, one on the A port and one on the B port, that allow for translation from 3.3-V LVTTL/LVCMOS to 5-V CMOS devices. The 8-bit LVCC3245A and LVCC4245A transceivers have configurable rails on the B port. The LVCC3245A A port can operate between 2.3-V and 3.6-V V_{CC}. The configurable B port can operate between 3-V and 5.5-V $V_{CC.}$ The LVCC4245A A port operates between 4.5-V and 5.5-V V_{CC}, and the configurable B port operates between 2.7-V and 5.5-V V_{CC}. TI also offers 16-bit SN74ALVC164245 transceivers in which the A port has a 5-V V_{CC} and the B port has a 3.3-V V_{CC} (see Figure 7).

TI also has 5-V logic families (AHCT, HCT, and ACT) that have TTL inputs and CMOS outputs. Therefore, these devices can interface 3.3-V outputs to 5-V CMOS inputs (see Figure 7).

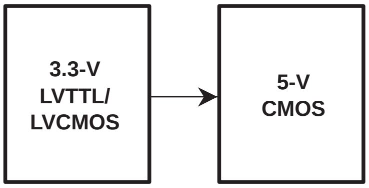
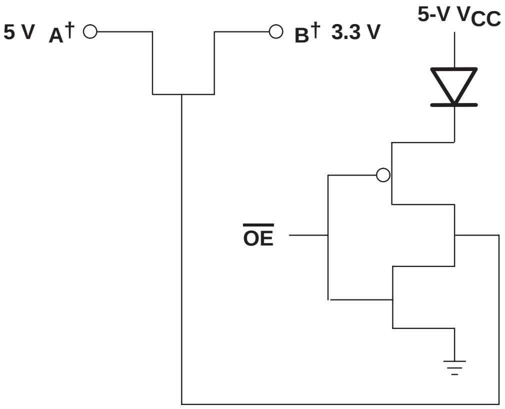


Figure 7. 3.3-V LVTTL/LVCMOS to 5-V CMOS

Bidirectional Voltage Translation

Voltage Translation From 3.3 V to 5-V TTL and From 5-V TTL to 3.3 V Using CBT or CBTD

This type of bidirectional translation (from A to B or B to A) can be done with TI's SN74CBT bus switches, using an external diode, or SN74CBTD bus switches that have the diode integrated internally. This method is suitable for voltage translation and bus-isolation applications. For example, with TI's 5-V V_{CC} SN74CBTD3384 bus switch (see Figure 8), the conditions are such that there are no pulldown resistors, and there is a minimal current passing through the FET.



† A can be 3.3 V, and B can be 5 V.

Figure 8. CBTD Bus Switch

The diode drop between V_{CC} and the PMOS gate is 0.7 V, which brings the voltage at the source to 4.3 V. With a 5-V input on the A side, the V_{gs} drop across the N channel is approximately 1.0 V, hence, the B side is translated to about 3.3 V. The typical V_{CC} vs V_{OH} graph is shown in Figure 9 and is provided in the data sheets for various temperatures and currents. In this example, the maximum voltage that can pass from B to A is 3.3 V. If a voltage less than 3.3 V is applied at B, the same voltage results on the A side. If a voltage greater than 3.3 V is applied at B, it is limited to 3.3 V on the A side. The V_{IH} min for 5-V TTL is 2.0 V. Therefore, as long as the voltage at B complies with 5-V TTL switching standards, this device can translate in both directions. Utilizing a bus switch for voltage translations also has the advantage of very fast propagation delay time.

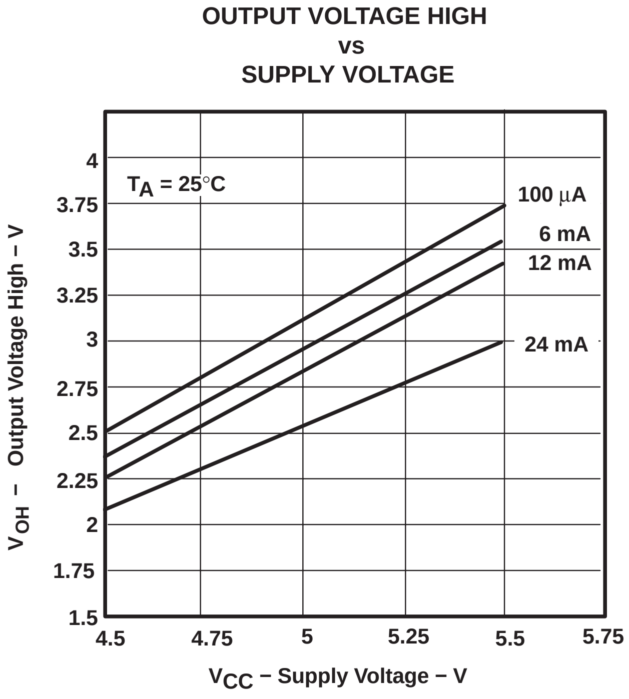


Figure 9. Typical V_{OH} vs V_{CC}

Voltage Translation From 3.3 V to 5-V TTL and 5-V TTL to 3.3 V Using TI 5-V-Tolerant Transceivers

TI’s low-voltage logic transceivers that are 5-V input and output tolerant, such as LVT, ALVT, and most LVC devices, can be used for bidirectional voltage translation between 3 V and 5-V TTL when buffering is required, and added delay is not critical to the application (see Figure 10). Output tolerance is specified as output voltage (V_O) or as the voltage range applied to any output in the high-impedance or power-off state (refer to the absolute maximum ratings in the data sheet for more information).

See the *Bus Contention* section of this application report.

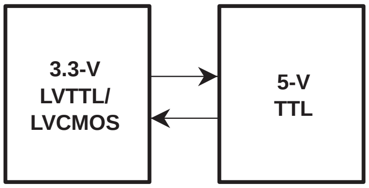


Figure 10. Translation Between 3.3 V and 5-V TTL

Voltage Translation From 3.3-V LVTTL/LVCMOS to 5-V CMOS and From 5-V CMOS to 3.3 V

Because 5-V CMOS switching standards have a $V_{IH(min)}$ of 3.5 V, TI split-rail devices, SN74LVCC4245A, SN74LVCC3245/A, and SN74ALVC164245 transceivers are the method of bidirectional voltage translation between 3.3-V and 5-V CMOS (see Figure 11).

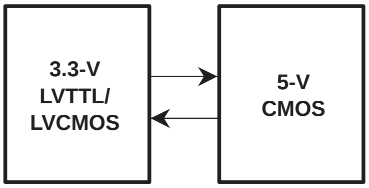

3.3-V
LVTTL/
LVCMOS
5-V
CMOS

Figure 11. Translation Between 3.3-V and 5-V CMOS

Voltage Translation Between 3.3 V, 2.5 V, and 1.8 V

The switching standards allow for voltage translation between 2.5 V and 3.3 V. Voltage translation between 3.3 V and 2.5 V also is permissible if the 2.5-V device is 3.3-V input tolerant. Voltage translation between 1.8 V and 3.3 V is not possible because the 3.3-V V_{IH} min is 2.0 V, which is not in range for a 1.8-V V_{CC} device. Voltage translation from 1.8 V to 2.5 V also is not possible because the V_{IH} min for a 2.5-V V_{CC} device is 1.7 V (see Figure 12).

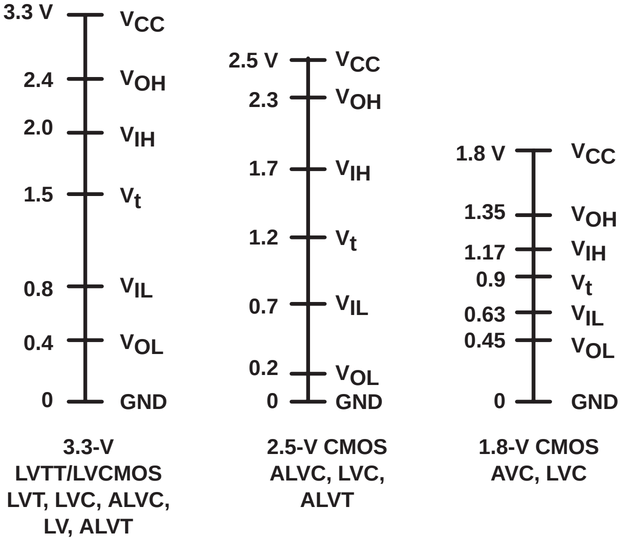

3.3 V
VCC
2.4
VOH
2.0
VIH
1.5
Vt
0.8
VIL
0.4
VOL
0
GND
3.3-V
LVTT/LVCMOS
LVT, LVC, ALVC,
LV, ALVT
2.5 V
VCC
2.3
VOH
1.7
VIH
1.2
Vt
0.7
VIL
0.2
VOL
0
GND
2.5-V CMOS
ALVC, LVC,
ALVT
1.8 V
VCC
1.35
VOH
1.17
VIH
0.9
Vt
0.63
VIL
0.45
VOL
0
GND
1.8-V CMOS
AVC, LVC

Figure 12. Comparison of Low-Voltage Switching Standards

Bus Contention

TI data sheets specify the maximum continuous current through a single output or through V_{CC} and GND. These values are absolute maximum ratings, which are stress ratings, not recommended operating conditions. These specifications most likely are exceeded when bus contention occurs.

Figure 13 shows a bus-contention situation between two devices driving the same bus. One has low-level output and the other has high-level output. This happens when drivers that have different enable and disable delays get on and off the same bus. This produces a short between the drivers, creating a current surge that may damage the devices. Typically, logic devices cannot withstand these high-current shorts that usually exceed the absolute maximum ratings of the device.

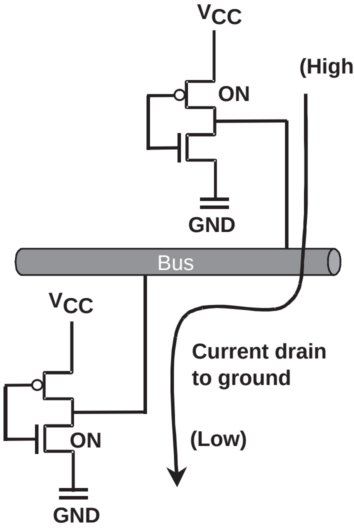


Figure 13. Bus Contention

If V_{CC} = 5 V and the resistance through the p and n channels of the transistors is about 10 Ω per output:

$$I = \frac{V}{R} = \frac{5\ V}{10\ \Omega} = 0.5\ A\ \text{per output} \quad (7)$$

Another high-current situation that may damage the device occurs when a 3.3-V device is at a high level and the output is pulled up to a higher voltage, such as 5 V (see Figure 14). Properly sizing the pullup resistor is very important. Using a pullup resistor of proper value limits the current to an allowable level. The device will not be damaged; however, there will be additional power dissipation from the current path through the 3.3-V device to V_{CC}.

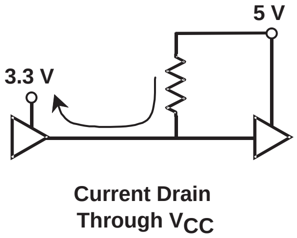


Figure 14. 3.3-V Driver Pulled to a Higher V_{CC}

The ALVT family has the auto3-state feature that automatically turns off the p-channel of the logic device to stop the current flow to V_{CC} (see Figure 15). This feature is specified in the absolute maximum ratings table of the ALVT data sheet as the voltage range applied to any output in the high state (-0.5 V to 7 V).

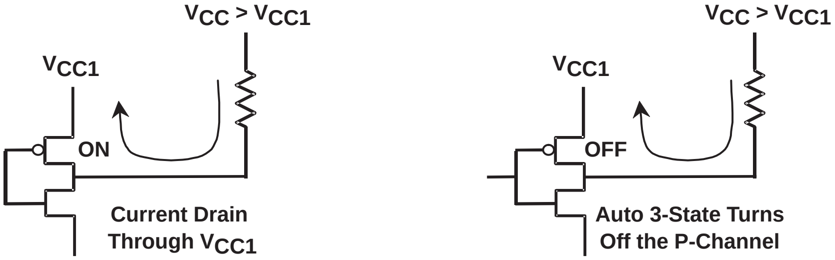

$V_{CC} > V_{CC1}$
V_{CC1}
ON
Current Drain Through V_{CC1}
$V_{CC} > V_{CC1}$
V_{CC1}
OFF
Auto 3-State Turns Off the P-Channel

Figure 15. Auto3-State

Conclusion

Voltage translation from 5 V to 3 V, 3 V to 2.5 V, and vice versa, can be done with a wide variety of TI logic products. 3.3-V and 2.5-V logic can translate to 1.8 V, if the 1.8-V device is 2.5-V and 3.3-V tolerant. However, due to switching standards, 1.8-V logic currently cannot be translated upward to 2.5 V and 3.3 V with the existing families. Newer families are being developed to handle voltage translations of these levels.

Acknowledgment

The authors of this application report are Susan Feodorov and Ramzi Ammar.

Glossary

A

ABT	Advanced BiCMOS technology
AC/ACT	Advanced CMOS logic
AHC/AHCT	Advanced high-speed CMOS logic
ALVC	Advanced low-voltage CMOS technology
ALVT	Advanced low-voltage BiCMOS technology

C

CBT	Crossbar technology
CMOS	Complementary metal-oxide semiconductor

L

LS	Low-power Schottky logic
LV	Low-voltage CMOS technology
LVC	Low-voltage CMOS technology
LVCMOS	Low-voltage CMOS
LVT	Low-voltage BiCMOS technology
LVTTL	Low-voltage TTL (3.3-V power supply and interface levels)

V

V_{CC}	Supply voltage
V_{IH}	High-level input voltage
V_{IL}	Low-level input voltage
V_{IN}	Input voltage
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
V_{OLP}	Low-level output voltage peak
V_{OLV}	Low-level output voltage valley
V_t	Threshold voltage

Benefits and Issues on Migration of 5-V and 3.3-V Logic to Lower-Voltage Supplies

SDAA011A
September 1999

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Abstract

In the last few years, the trend toward reducing supply voltage (V_{CC}) has continued, as reflected in an additional specification of 2.5-V V_{CC} for the AVC, ALVT, ALVC, LVC, LV, and the CBTLV families.

In this application report, the different logic levels at V_{CC} of 5 V, 3.3 V, 2.5 V, and 1.8 V are compared. Within the report, the possibilities for migration from 5-V logic and 3.3-V logic families to 2.5-V V_{CC} are shown, and the implications of the reduced supply voltage are discussed. Data is provided that shows the influence of reduced V_{CC} on power consumption, drive capability, and propagation delay time for the logic families.

Further, the requirements for an overvoltage tolerance (5-V/3.3-V input and output) is discussed, as well as interfacing opportunities in a mixed-mode environment in which two different supply voltages are used.

This application report is intended to be used as a designer’s guide to component selection and usage at supply voltages below 3.3-V. The data in this document is typical data taken under typical laboratory conditions (25°C) and 2.5-V or 1.8-V, except where otherwise noted. The data is intended as a design guideline only.

Background

The use of 5-V V_{CC} has long been the standard for both core and memory logic. However, with the increase in complexity and the functionality of application-specific integrated circuits (ASICs), central processing units (CPUs), microprocessors, and digital signal processors (DSPs), it has become necessary to reduce the structure size of these elements.

Using modern manufacturing processes that produce smaller structures, the thickness of the gate oxide of each single transistor has become more sensitive to electrostatic field strength. Because the field strength is proportional to the supply voltage, the direct result is that supply voltage must be reduced for a reliable operation.

In other words, making electronic devices more complex, without enlarging the overall size of the chip area, requires reducing the structure size, which also requires reducing V_{CC}.

The limit for reliable operation at less than 5-V V_{CC} is reached at a structure size of 0.6 micron, and the use of a 0.35-micron manufacturing process requires 2.5-V V_{CC} for proper operation.

Moreover, power consumption always is a concern for new system designs. A reduction in supply voltage produces an exponential decrease in power consumption; therefore, the trend is to reduce power-supply voltage. To meet these requirements, many modern logic families are specified at different voltage nodes, which enables designers to use them at 3.3-V V_{CC} and at 2.5-V V_{CC}.

This application report investigates the possibilities for migration of 5-V and 3.3-V logic to 2.5-V logic, and discusses the implications.

Input- and Output-Level Specifications at Different Supply Voltages

For each V_{CC} a standard is defined, with commonly agreed-upon levels of input and output levels. Figure 1 shows the appropriate switching levels for 5-V, 3.3-V, and 2.5-V that have passed the JEDEC committee. Additionally, the 1.8-V level specification, as given in the data sheets of the SN74LVCxxxA and SN74AVCxxx devices, is shown.

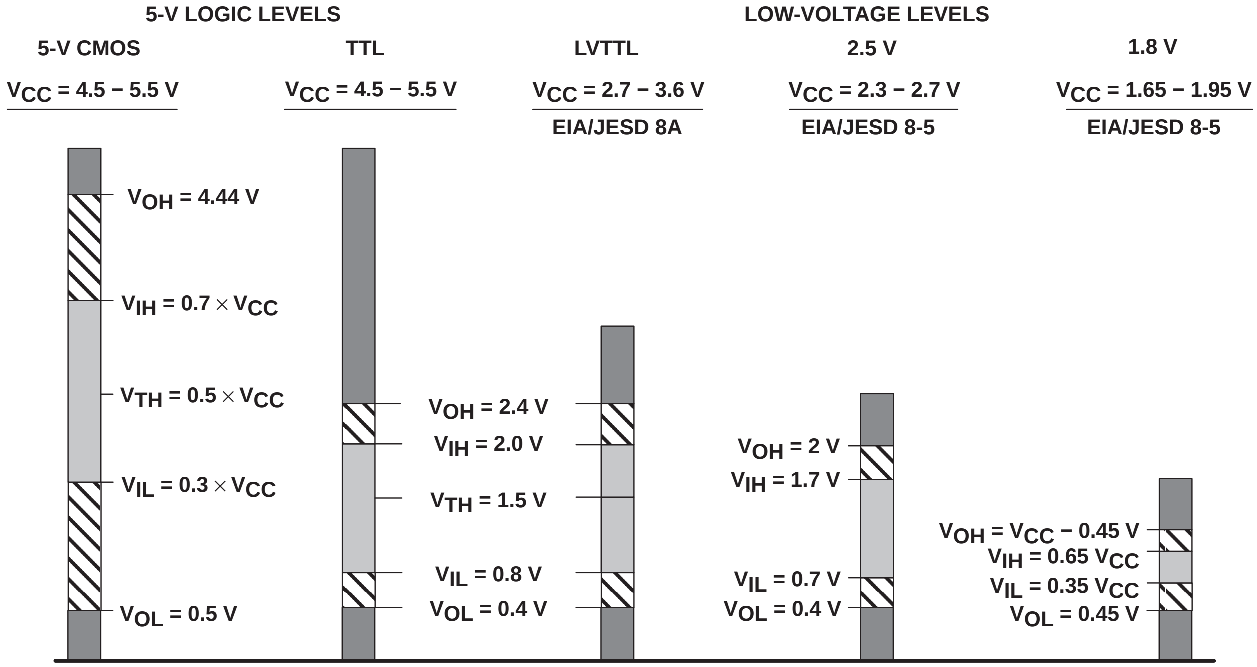

5-V LOGIC LEVELS
LOW-VOLTAGE LEVELS
5-V CMOS
TTL
LVTTL
2.5 V
1.8 V
V_{CC} = 4.5 − 5.5 V
V_{CC} = 4.5 − 5.5 V
V_{CC} = 2.7 − 3.6 V
EIA/JESD 8A
V_{CC} = 2.3 − 2.7 V
EIA/JESD 8-5
V_{CC} = 1.65 − 1.95 V
EIA/JESD 8-5
V_{OH} = 4.44 V
V_{IH} = 0.7 × V_{CC}
V_{TH} = 0.5 × V_{CC}
V_{IL} = 0.3 × V_{CC}
V_{OL} = 0.5 V
V_{OH} = 2.4 V
V_{IH} = 2.0 V
V_{TH} = 1.5 V
V_{IL} = 0.8 V
V_{OL} = 0.4 V
V_{OH} = 2 V
V_{IH} = 1.7 V
V_{IL} = 0.7 V
V_{OL} = 0.4 V
V_{OH} = V_{CC} − 0.45 V
V_{IH} = 0.65 V_{CC}
V_{IL} = 0.35 V_{CC}
V_{OL} = 0.45 V

Figure 1. 5-V, 3.3-V, and 2.5-V Switching-Level Comparison

Table 1 contains additional information regarding the various logic families, including manufacturing process, the optimal power supply, and the V_{CC} at which the logic families are functional.

The AHC family is included in this overview. Although the AHC family was targeted for the 5-V V_{CC}, after its market introduction, this family also was specified for operation at 3.3 V V_{CC}.

The low-voltage logic families (SN74LVxxxA, SN74LVCxxxA, SN7ALVCHxxx) also have been characterized at 2.5-V V_{CC}, to meet the trend of reduced supply voltages.

The AVC family is the optimal solution for 2.5-V V_{CC}, and also is fully characterized at 1.8-V and 3.3-V V_{CC}.

The data sheets for the LVC family show switching characteristics at 1.8-V V_{CC}.

Table 1. Operational Supply Voltages of Different Logic Families

LOGIC FAMILY	MANUFACTURING PROCESS	OPTIMAL POWER-SUPPLY LEVEL	OPERATIONAL AT V_{CC} = 3.3 V	OPERATIONAL AT V_{CC} = 2.5 V	OPERATIONAL AT V_{CC} = 1.8 V
AHC	CMOS	5 V	Fully specified	Yes, down to 2 V	Not specified
ALVC	CMOS	3.3 V	Fully specified	Fully specified	Planned
ALVT	BiCMOS	3.3 V	Fully specified	Fully specified	Not specified
AVC	CMOS	2.5 V	Fully specified	Fully specified	Fully specified
CBTLV	CMOS	3.3 V	Fully specified	Fully specified	Not specified
LVxxxA	CMOS	3.3 V	Fully specified	Fully specified	Not specified
LVCxxxA	CMOS	3.3 V	Fully specified	Fully specified	Fully specified

The CMOS process indicates that both the input and the output structures comprise pure CMOS circuitry, whereas, the BiCMOS process indicates that both bipolar and CMOS transistors are implemented in the data or control input circuitry and/or output circuitry.

Power-Consumption Considerations

With the reduction of the supply voltage, a proportional power saving results. This section provides comparisons of the power consumption of logic families at different voltage levels.

The total power consumption of an integrated circuit is the sum of quiescent power dissipation, or static power consumption, (see Equation 1) and dynamic power consumption (see Equation 2). Dynamic power consumption consists of two parts:

- The average power dissipation caused by current spikes (see Equation 3). This is the power consumption that is caused by the internal circuitry of the logic device.
- The power dissipation caused by driving an externally connected load (see Equation 4).

Static power consumption: $$P_{STAT} = V_{CC} \times I_{CC} \tag{1}$$

Dynamic power consumption: $$P_{DYN} = P_T + P_L \tag{2}$$

Transient power consumption: $$P_T = V_{CC}^2 \times C_{PD} \times f_I \times N_{SW} \tag{3}$$

Capacitive-load power consumption: $$P_T = V_{CC}^2 \times C_L \times f_{OI} \times N_{SW} \tag{4}$$

Where:

V_{CC} = supply voltage
C_L = load capacitance
C_{PD} = dynamic power-dissipation capacitance
f_I = input-signal frequency
f_O = output-signal frequency
I_{CC} = supply current
N_{SW} = number of outputs switching

A reduction of V_{CC} directly results in a power savings. The relation in the static power consumption is linear (assuming that static I_{CC} is independent of V_{CC}), while the term V_{CC} is included as a squared factor within the dynamic power consumption formulas (see Equation 3 and Equation 4).

Using equations 1 through 4, a 3.3-V V_{CC} system theoretically saves between 33% for the static considerations (see Equation 1) and up to 57% for the dynamic case, when compared to 5-V systems. With a 2.5-V V_{CC}, the system's power consumption decreases to between 50% (static) and 75% (dynamic), respectively, compared to the 5-V system.

The data sheets of the logic families do not show all information about power consumption. One parameter that is shown for power consumption is the supply current (I_{CC}). However, in some cases, this parameter is given at only one supply voltage. The parameter I_{CC} is given in the table of electrical characteristics (recommended operation conditions) shown for the SN74LV245A in Table 2.

Table 2. LV245A Supply Current Parameter (I_{CC})

TEST CONDITIONS		V_{CC}	MIN	MAX	UNIT
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		20	µA

However, as previously mentioned, this parameter indicates the power consumption for static states only, either for the case that the input is statically set to V_{CC} or set to GND.

Another parameter that indicates the power consumption indirectly is the power-dissipation capacitance (C_{pd}) that is given, for example, for the AVC family at three supply voltages. With this parameter, the transient power consumption can be calculated using Equation 3.

For a more comprehensive overview of Texas Instruments logic families, measurements of the dynamic power consumption at different supply voltages have been taken. The logic families investigated were AHC, ALVT, ALVC, LVC, LV, and AVC.

The measurement setup is shown in Figure 2. For the measurement of dynamic power consumption, all but one input of the device under test (DUT) were set to a static high-state or low-state logic value. One input is connected to a signal generator. The applied signal is a square wave with a duty cycle of 50% and switches between the supply voltage of the DUT and GND. The frequency of the signal was varied between 1 MHz and 50 MHz and the supply current (I_{CC}) was measured within that range. The outputs of the DUT are not connected, so that only the device's internal power consumption, not the external load, is measured.

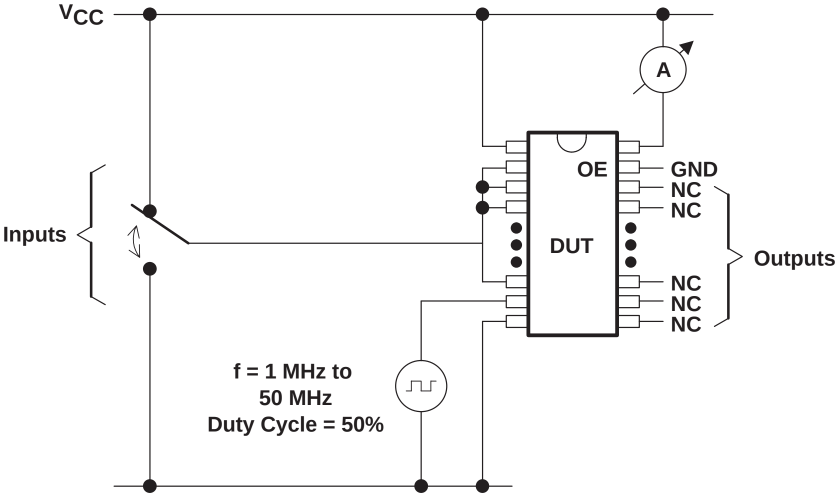


Figure 2. Power Consumption vs Frequency Measurement Setup

Figures 3 through 5 show the measurement results for 3.3-V, 2.5-V, and 1.8-V V_{CC}. The LVC and the AVC families have a specification for the 1.8-V V_{CC}, but the other logic families do not. However, the test samples of all investigated logic families showed full functionality at 1.8-V V_{CC}. For comparison, the power consumption has been measured at 1.8-V also.

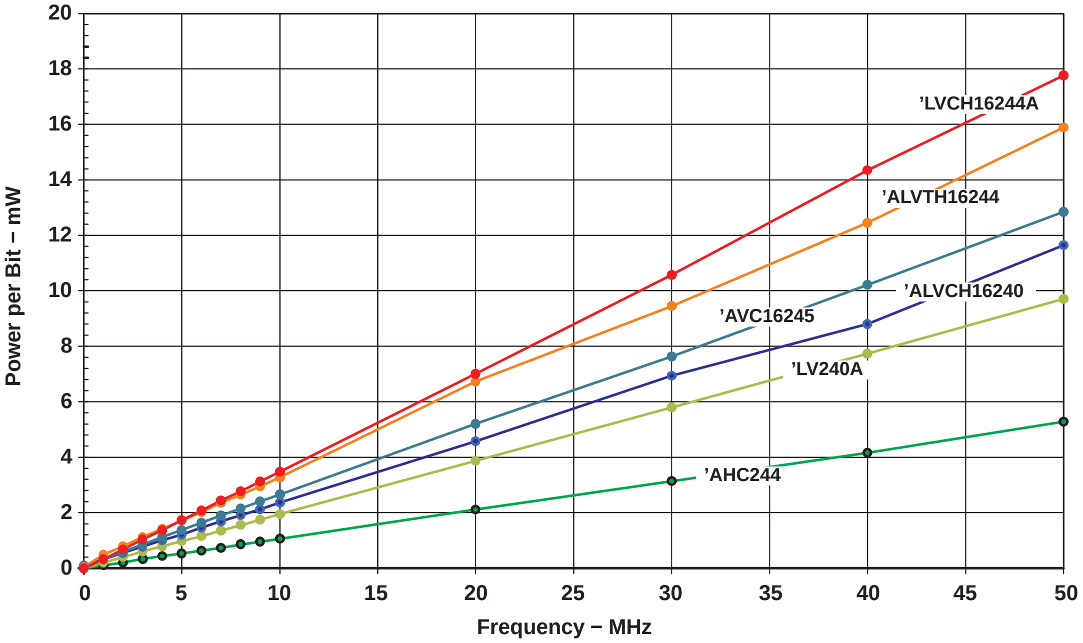


Figure 3. Power Consumption at 3.3-V V_{CC}

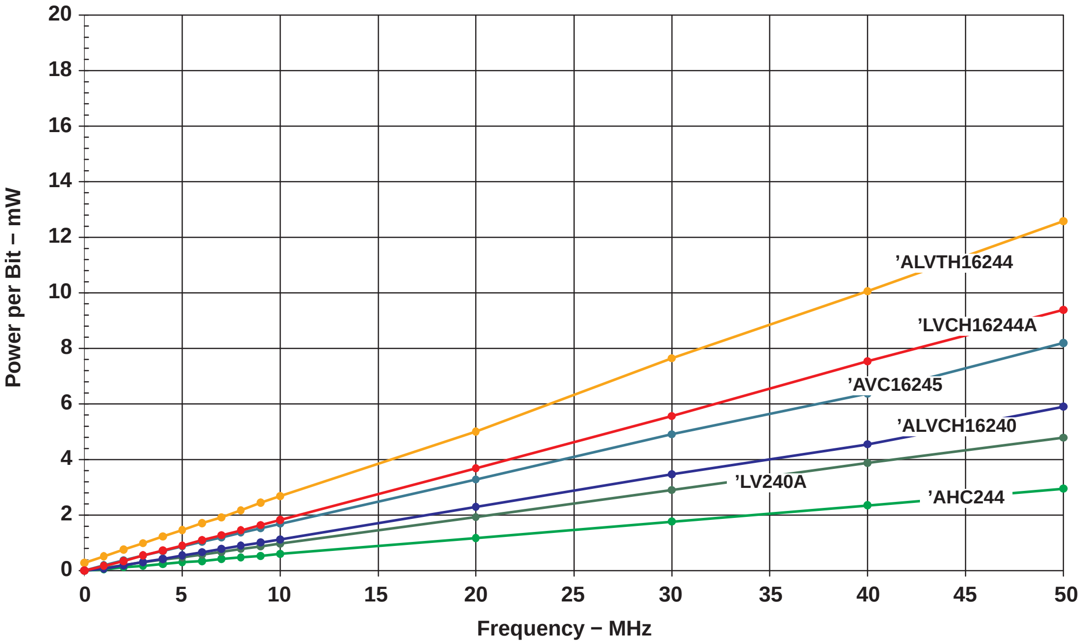


Figure 4. Power Consumption at 2.5-V V_{CC}

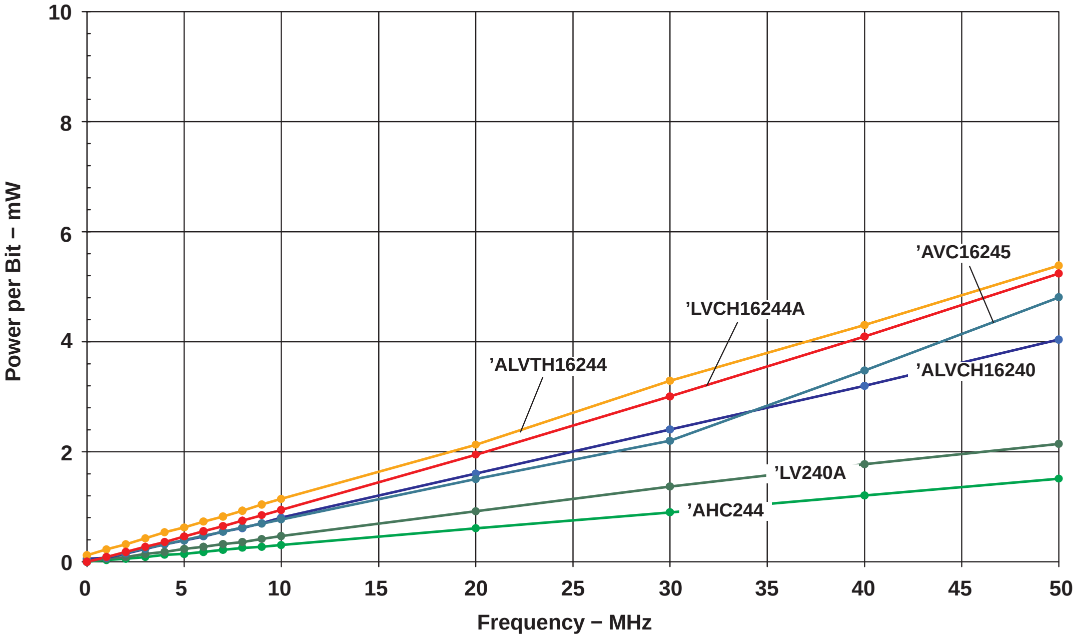


Figure 5. Power Consumption at 1.8-V V_{CC}

Figure 6 shows the relative power consumption of the tested logic devices compared to 3.3-V V_{CC}.

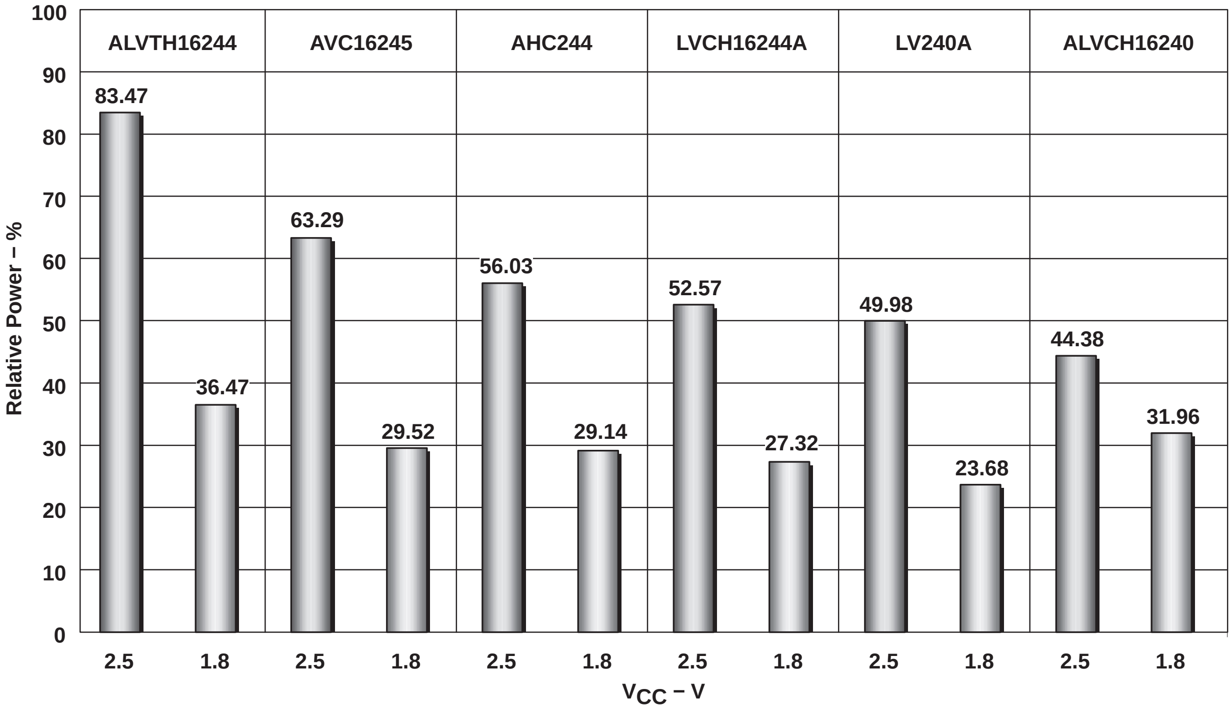


Figure 6. Relative Power Consumption at 2.5-V and 1.8-V V_{CC} Compared to 3.3-V V_{CC}

Output Characteristics at Less Than 3.3-V V_{CC}

Standard Logic Families

With the reduction of the supply voltage there is also a reduction of the drive capability of the logic circuit.

The output stage of a logic circuit in the high state behaves like a voltage source with an open-circuit voltage of V_{CC} for CMOS logic, and low-voltage BiCMOS logic, respectively.

In the low state, for positive voltages, the output resistance is based on the internal resistance of the conducting transistor, i.e., collector-emitter for BiCMOS technologies and drain-source resistance for CMOS technologies.

Negative voltage peaks at the inputs are limited by protection diodes. Output stages of the CMOS logic family SN74AHCxxx also have output protection diodes that connect output stages and V_{CC}. This diode limits the positive output voltage to V_{CC} + 0.5 V.

The available output current depends on V_{CC}, which determines the gate source voltage of the output transistors. At a supply voltage below about 1 V (less than the turn-on voltage of the MOS transistors) the output stays in the off state. With increasing supply voltage, output current increases also.

The LVC family has the dc characteristics shown in Table 3. The drive capability of this device decreases with decreasing supply voltage.

Table 3. LVCH245A Output Drive Parameters (V_{OH} and V_{OL})

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	$I_{OH} = -100\ \mu A$	1.65 to 3.6 V	V_{CC} −0.2		V
	$I_{OH} = -4$ mA	1.65 V	1.2		
	$I_{OH} = -8$ mA	2.30 V	1.7		
	$I_{OH} = -12$ mA	2.70 V	2.2		
	$I_{OH} = -12$ mA	3.00 V	2.4		
	$I_{OH} = -24$ mA	3.00 V	2.2		
V_{OL}	$I_{OL} = 100\ \mu A$	1.65 to 3.6 V		0.2	V
	$I_{OL} = 4$ mA	1.65 V		0.45	
	$I_{OL} = 8$ mA	2.30 V		0.7	
	$I_{OL} = 12$ mA	2.70 V		0.4	
	$I_{OL} = 24$ mA	3.00 V		0.55	

Figure 7 illustrates values of I_{OL} and I_{OH} and the corresponding values of V_{OL} and V_{OH} for a typical LVC device. The output characteristics of the LVC device were taken at 3.3-V, 2.5-V, and 1.8-V V_{CC}. The drive capability decreases significantly with reduced supply voltage. The same trend can be observed for all logic families.

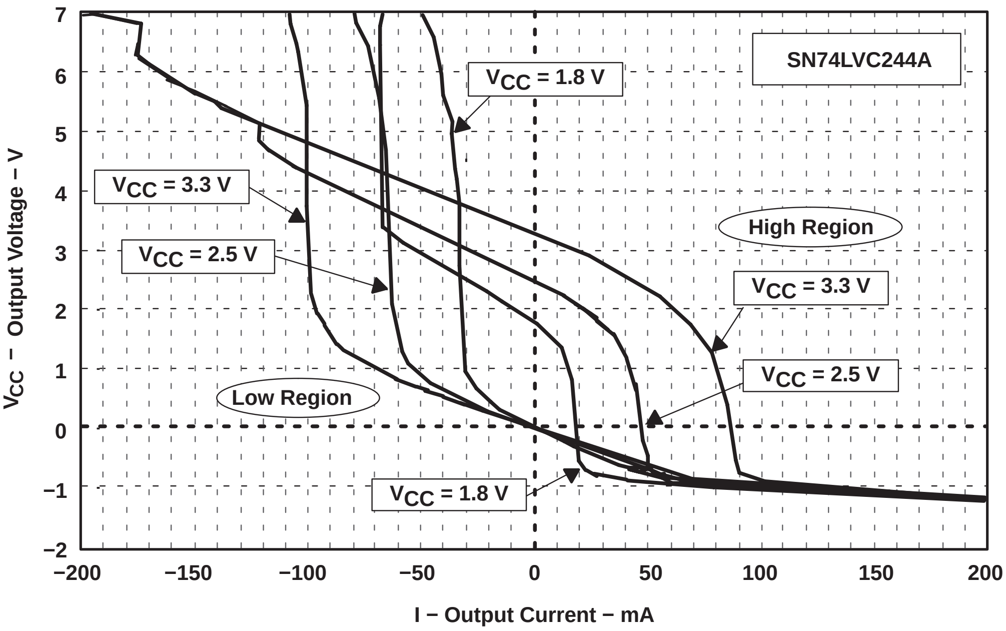


Figure 7. Output Characteristics of the LVC244 at Different Supply Voltages

Table 4 shows a comparison of the output-current specifications of the logic families discussed in this report. All families have full 3.3-V and 2.5-V specifications. LV and the AHC have additional 5.5-V drive specifications. The AVC and LVC families show full specifications regarding the high-level and low-level output voltage and output current in the data sheets at V_{CC} = 1.8 V.

Table 4. Output-Current Specifications as Shown in the Data Sheet

LOGIC FAMILY	V_{CC}	MINIMUM		MAXIMUM		SPECIFIED IN DATA SHEET
		V_{OH}	I_{OH}	V_{OL}	I_{OL}	
AHC	2 V	1.9 V	−50 µA	0.1 V	50 µA	No switching characteristic
	2.30 V					N/A
	3.00 V	2.48 V	−4 mA	0.44 V	4 mA	Yes
	4.5 V	3.8 V	−8 mA	0.44 V	8 mA	5-V specification
LV	2 V−5.5 V	V_{CC}−0.1 V	−50 µA	0.1 V	50 µA	Yes
	2.30 V	2 V	−2 mA	0.40 V	2 mA	Yes
	3.00 V	2.48 V	−8 mA	0.44 V	8 mA	Yes
	4.5 V	3.8 V	−16 mA	0.55 V	16 mA	5-V specification
LVC	1.65	1.2 V	−4 mA	0.45 V	4 mA	Yes
	2.30 V	1.7 V	−8 mA	0.70 V	8 mA	Yes
	2.70 V	2.2 V	−12 mA	0.40 V	12 mA	Yes
	3.00 V	2.2 V	−24 mA	0.55 V	24 mA	Yes
ALVC	1.65					Planned
	2.30 V	2 V	−6 mA	0.40 V	6 mA	Yes
	2.70 V	2.2 V	−12 mA	0.40 V	12 mA	Yes
	3.00 V	2 V	−24 mA	0.55 V	24 mA	Yes
ALVT	1.65					
	2.30 V	1.8 V	−8 mA	0.50 V	−24 mA	Yes
	3.00 V	2 V	−32 mA	0.55 V	−64 mA	Yes
AVC	1.65	1.2 V	−4mA	0.45 V	4 mA	Yes
	2.30 V	1.75 V	−8 mA	0.55 V	8 mA	Yes
	3.00 V	2.3 V	−12 mA	0.7 V	12 mA	Yes

Crossbar Technology (CBT)/Crossbar Technology Low Voltage (CBTLV)

The CBT families (SN74CBTxxx and SN74CBTLVxxx) are FET switches that do not have their own drive capability. They are a good solution in systems that require bus isolation and bus exchanging. The impedance of CBT devices varies with the amount of current flowing from the drain to the source. The data sheets reflect this with the parameter r_{on}.

Figure 8 shows the r_{on} measurement setup. Measurements were taken at 3.3-V, 2.5-V, and 1.8-V V_{CC} to show the influence of V_{CC} on r_{on} of the CBTLV3245A. The output was enabled by connection to GND.

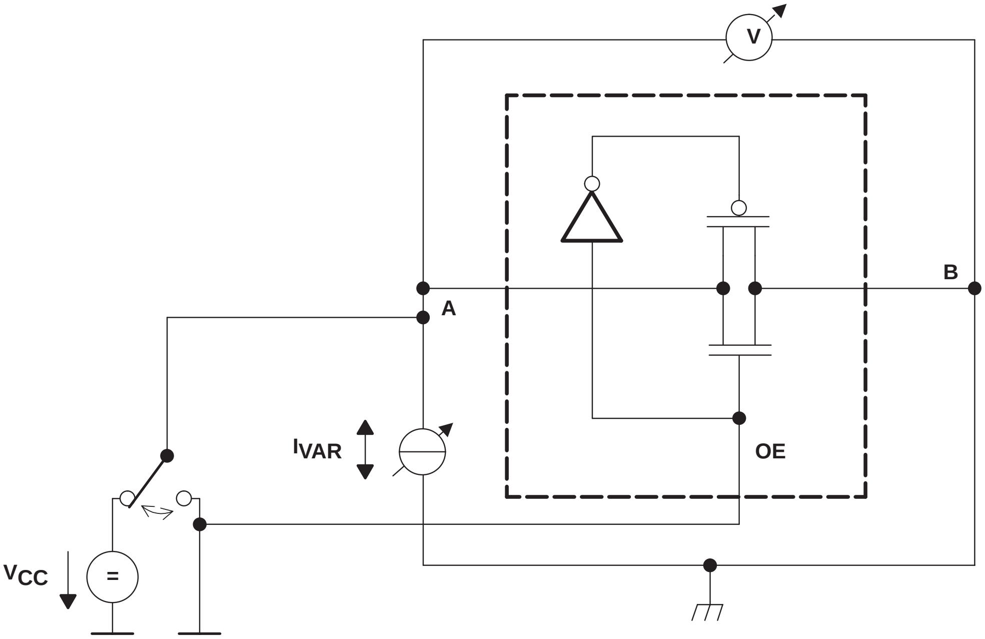


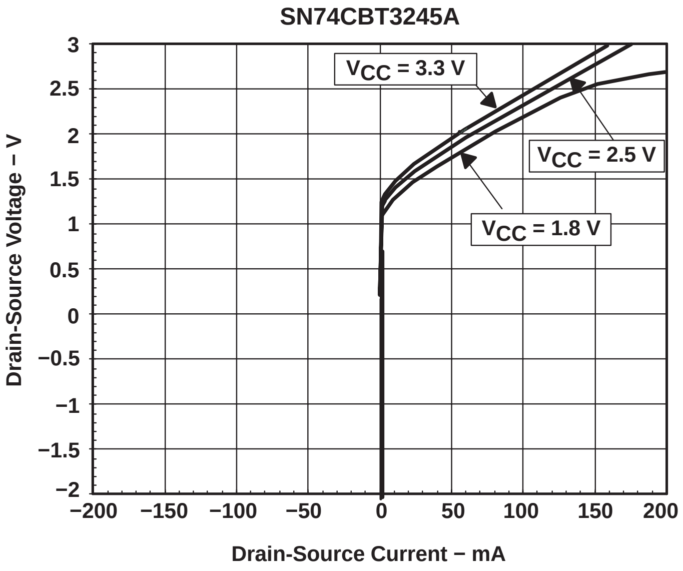
Figure 8. Setup for Measuring r_{on} of the CBTLV3245A

Input A was connected to V_{CC} to measure r_{on} in the high state. To measure r_{on} in the low state, input A was connected to GND of the supply voltage.

Also, input A was connected to a variable-current source that was swept from −200 mA to 200 mA. The voltage was measured over the drain-source of the CBTLV3245A between point A and point B.

Figures 9 and 10 show the measurement results. The linearity of r_{on} or the CBT3245A is best at 5.5-V V_{CC} with r_{on} (high state) of 10 Ω to 20 Ω and r_{on} (low state) of 4 Ω to 7 Ω.

The linearity of r_{on} for the CBTLV3245A is best at 3.3-V V_{CC} with r_{on} (high state) of 6 Ω to 10 Ω and r_{on} (low state) of 2 Ω to 5 Ω.



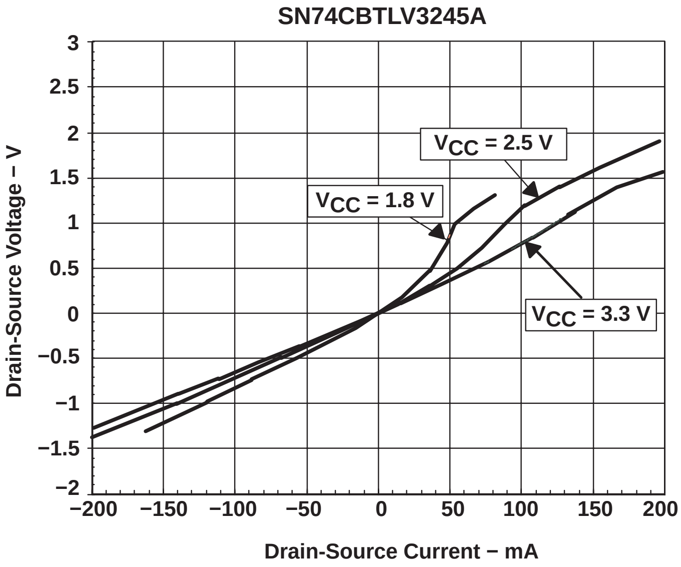


Figure 9. High-State r_{on} of CBT3245A and CBTLV3245A at Different Supply Voltages

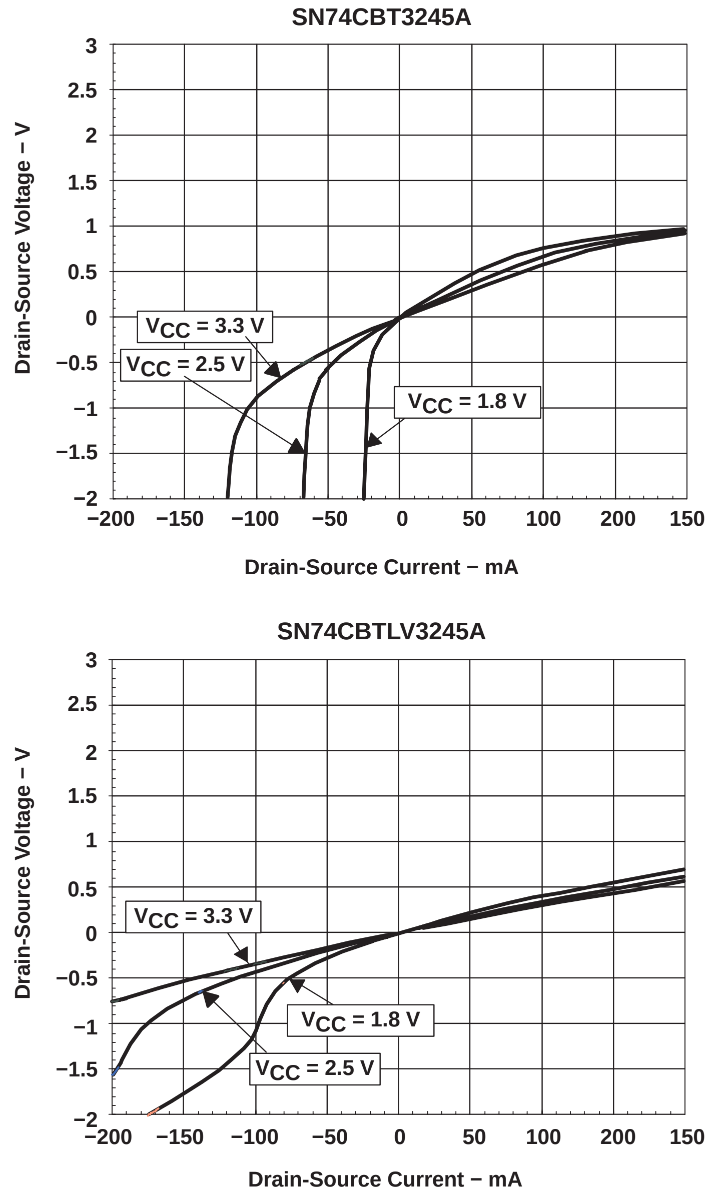


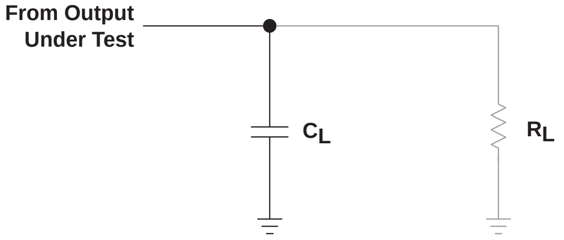
Figure 10. Low-State r_{on} of CBT3245A and CBTLV3245A at Different Supply Voltages

The linearity of r_{on} (drain-source) of the FET degrades with decreasing supply voltage. The CBT device conducts only if the drain-source voltage is more than approximately 1 V. The CBTLV devices are operational below this voltage because the P-channel FET is switched in parallel with the n-channel transistor and exhibits transmission-gate behavior. The r_{on} (high state) varies, depending on the conducted current and the supply voltage. The resistance values can be derived from Figures 9 and 10.

Propagation Delay Time at Different Supply Voltages

Decreasing a system’s supply voltage from 5 V to 3.3 V, or lower, slows its speed (increases propagation time). This section contains a comprehensive collection of measurements that shows this effect. The data sheets show that the measurement setup for the propagation delay depends on the supply voltage of the device under test (DUT).

However, not only is the supply voltage reduced, but the measurement setup for the propagation delay time is different. Figure 11 shows the test condition for the measurements of the high-to-low and low-to-high propagation delay times at 5-V, 3.3-V, 2.5-V, and 1.8-V V_{CC}.



C_L = 50 pF @ V_{CC} = 5 V
50 pF @ V_{CC} = 3.3 V
30 pF @ V_{CC} = 2.5 V
30 pF @ V_{CC} = 1.8 V

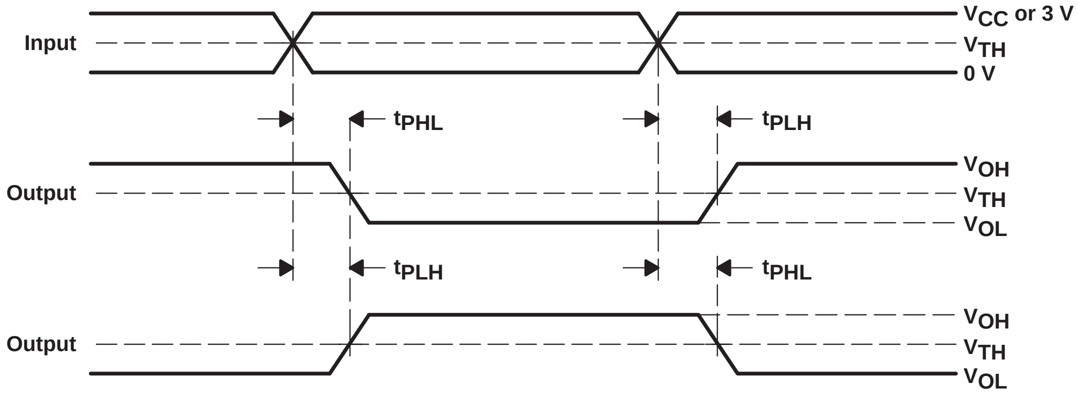
R_L = Open @ V_{CC} = 5 V
500 Ω @ V_{CC} = 3.3 V
500 Ω @ V_{CC} = 2.5 V
500 Ω @ V_{CC} = 1.8 V

Figure 11. Test Conditions for Measuring Propagation Delay Time

While at 5-V V_{CC}, a 50-pF capacitor is the only load to the device’s output, at 3.3-V V_{CC} a 500-Ω resistor (R_L) is in parallel with the capacitor for the measurement. At 2.5-V V_{CC} the value of the capacitor is reduced to 30 pF, and the value of the resistor in parallel is 500 Ω.

Figure 12 shows voltage waveforms. All input pulses are supplied by a generator having the following characteristics: signal frequency = 1 MHz, t_r, $t_f \le 2.5$ ns. One output is measured at a time, with one transition per measurement.

For ALVTH at 3.3-V V_{CC}, the input signal was switched between 3.0 V and 0 V. In this case, the threshold voltage is 1.5 V. For all other measurements the input signal was switched between V_{CC} and GND and the threshold voltage chosen was $V_{CC}/2$.



V_{TH} : Threshold Voltage

Figure 12. Propagation Delay Times of Inverting and Noninverting Outputs

Table 5 shows the results of the propagation delay time measurements. In Figure 13, the results are shown graphically for easier comparison.

Table 5. Typical Propagation Delays at Different Supply Voltages

SUPPLY VOLTAGE	LOAD CONDITION	t_{pd}	AHC244	LV240A	LVCH16244A	ALVCH16244	ALVTH16244	AVC16244	UNIT
5 V	C_L =50 pF	t_{PLH}	4.4	4.3	N/A	N/A	N/A	N/A	ns
		t_{PHL}	4.4	4.3	N/A	N/A	N/A	N/A	ns
3.3 V	C_L = 50 pF, R_L = 500 Ω	t_{PLH}	6.2	5.2	2.4	2.6	1.9	1.2†	ns
		t_{PHL}	5.5	4.9	2.0	1.7	1.5	1.6†	ns
2.5 V	C_L = 30 pF, R_L = 500 Ω	t_{PLH}	6.8	7.2	2.6	2.7	1.9	1.4	ns
		t_{PHL}	5.9	6.4	2.4	1.7	1.7	1.8	ns
1.8 V	C_L = 30 pF, R_L = 500 Ω	t_{PLH}	11.4	12.1	4.2	4.3	2.7	1.9	ns
		t_{PHL}	9.0	10.5	3.8	2.7	3.2	2.2	ns

† Measured with C_L= 30 pF

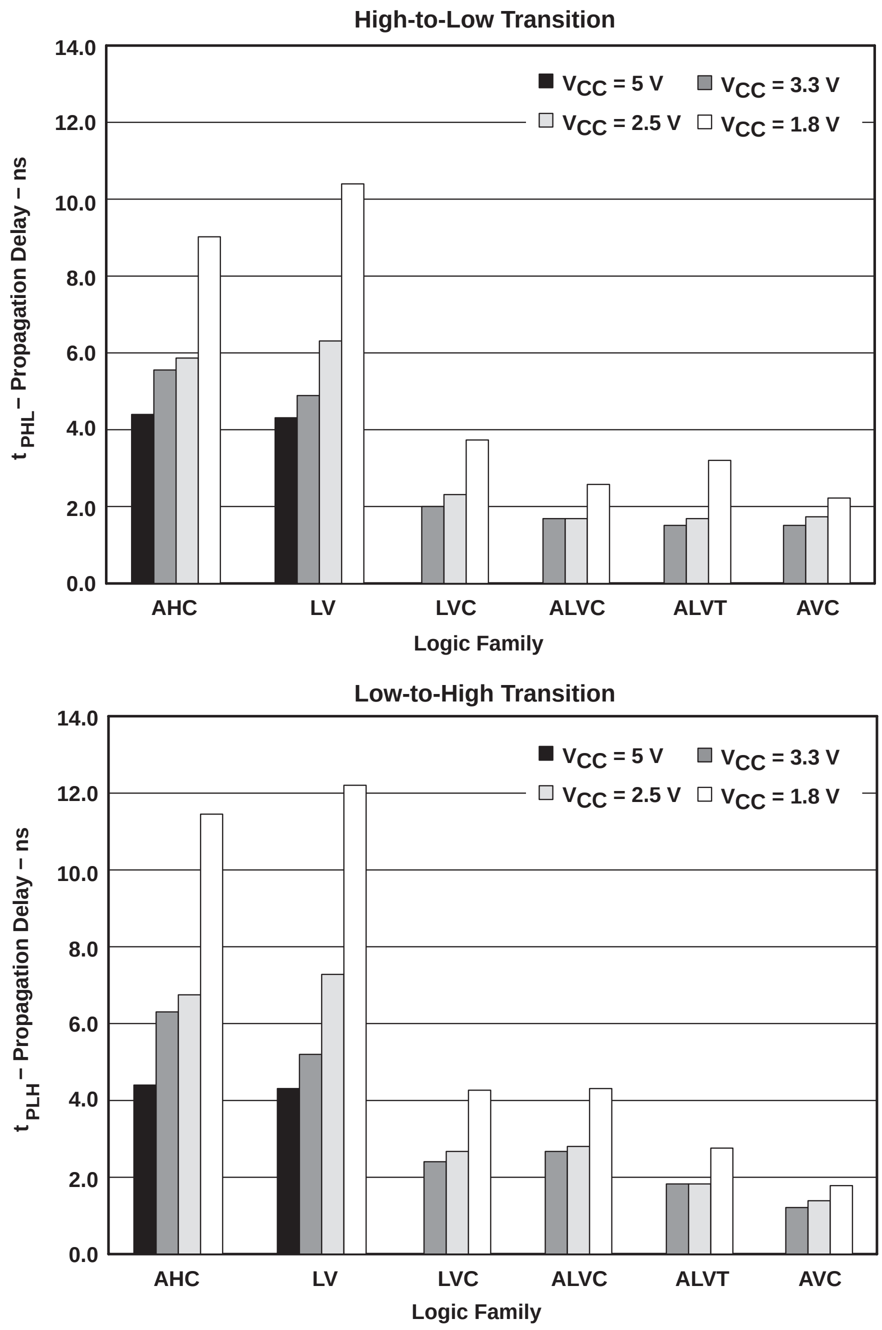


Figure 13. Typical Propagation Delays at Different Supply Voltages

With the AVC family, TI offers an optimized solution for the next low-voltage node of 2.5-V V_{CC}. This logic family is the fastest family in this comparison. Even when supplied with 1.8 V, the propagation delay time of the DUT is slightly less than 2 ns.

An application report, *AVC Logic Family Technology and Applications*, literature number SCES06, discussing the features and benefits of this 2.5-V logic, is available from TI.

Interfacing Between Different Voltage Levels

Regarding the term compatibility, possible interactions between logic devices that are supplied from different power-supply voltages must be considered. It is necessary to distinguish correctly between the terms tolerance, interfacing or translating, and level shifting. The input and output specifications are important for this discussion.

Input-Overvoltage Tolerance

A logic device is input-overvoltage tolerant if its input can withstand the presence of a higher voltage without being damaged. For example, the input-overvoltage tolerance is called 5-V tolerance if the device is powered from a 3.3-V, 2.5-V, or 1.8-V V_{CC} source and can accept a voltage level of 5 V at the inputs.

The input overvoltage tolerance is presented in the data sheet under the *recommended operating conditions* topic. The parameter is called V_I (input voltage). The LVC specification is shown as an example in Table 6.

Table 6. Extract of Recommended Operating Conditions for the LVCH245A

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.65	3.6	V
V_I	Input voltage	0	5.5	V

In this case, the input voltage (V_I) exceeds V_{CC}. This also implies that the device is tolerant of higher input voltage levels at every supply voltage between 1.65 V and 3.6 V. Table 7 shows the input overvoltage tolerance of the logic devices at the different supply voltages.

Table 7. Input-Overvoltage Tolerance of Different Logic Families

VOLTAGE (V_I) APPLIED TO INPUT	FAMILY AND SUPPLY VOLTAGE			
	ALVT, LVC, LVT, LV, AHC V_{CC} = 3 V TO 3.6 V	ALVT, LVC, LV, AHC V_{CC} = 2.3 V TO 2.7 V	LVC, LV, AHC V_{CC} = 2 V	LVC V_{CC} = 1.65 V
5 V	5-V tolerant	5-V tolerant	5-V tolerant	5-V tolerant
3.3 V		3.3-V tolerant	3.3-V tolerant	3.3-V tolerant
2.5 V			2.5-V tolerant	2.5-V tolerant

AVC logic has 3.3-V input-overvoltage tolerance with 2.5-V V_{CC} or 1.8-V V_{CC} and 2.5-V V_{CC} input-overvoltage tolerance with 1.8-V V_{CC}.

Output-Overvoltage Tolerance

A logic device is output-overvoltage tolerant if it can withstand the presence of a higher voltage during the high-impedance state at the output without being damaged.

The output-overvoltage tolerance is in the data sheet in the recommended operating conditions table as the parameter V_O. An example specification for the SN74LV245A is shown in Table 8.

Table 8. Extract of Recommended Operating Conditions for the LV245A

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	3.6	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	

During the logic high state, the device’s output must not be connected to a higher voltage than V_{CC}; otherwise, the pullup transistor of the output stage will begin operation in reverse mode and a significant current could flow into the output of the device. This will prohibit a higher voltage logic level than V_{CC} and, under worst case conditions, damage the logic device.

Table 9 summarizes the output-overvoltage tolerance during the high-impedance state.

Table 9. Output-Overvoltage Tolerance of Different Logic Families

APPLIED VOLTAGE DURING THE HIGH-IMPEDANCE STATE	FAMILY AND SUPPLY VOLTAGE			
	ALVT, LVC, LVT, LV V_{CC} = 3 V TO 3.6 V	ALVT, LVC, LV V_{CC} = 2.3 V TO 2.7 V	LVC, LV V_{CC} = 2 V	LVC V_{CC} = 1.65 V TO 1.95 V
5 V	5-V tolerant	5-V tolerant	5-V tolerant	5-V tolerant
3.3 V		3.3-V tolerant	3.3-V tolerant	3.3-V tolerant
2.5 V			2.5-V tolerant	2.5-V tolerant

The LVT logic family is 5-V overvoltage tolerant (inputs and outputs) at 3.3-V V_{CC}. The ALVT, LVC, and LV families are 5-V overvoltage tolerant (inputs and outputs) at 3.3-V and 2.5-V V_{CC}. The LVC family also is 5-V overvoltage tolerant (inputs and outputs) at 1.8 V V_{CC}.

The AVC family is 3.3-V output-overvoltage tolerant at 2.5-V and lower V_{CC}.

The specification of the ALVC logic family shows the maximum value of V_{CC} for the input and the output voltages that can be applied to the device inputs and outputs.

The AHC family is tolerant of higher voltages only at the input. At the output, AHC devices have clamping diodes to V_{CC} such that an overvoltage applied to the output results in a current that flows through the clamping diode within the device to the internal V_{CC} connection.

Auto3-State Output of the ALVT Family

The auto3-state function that is implemented in the output of the ALVT family represents a specialty. The principle is shown in Figure 14.

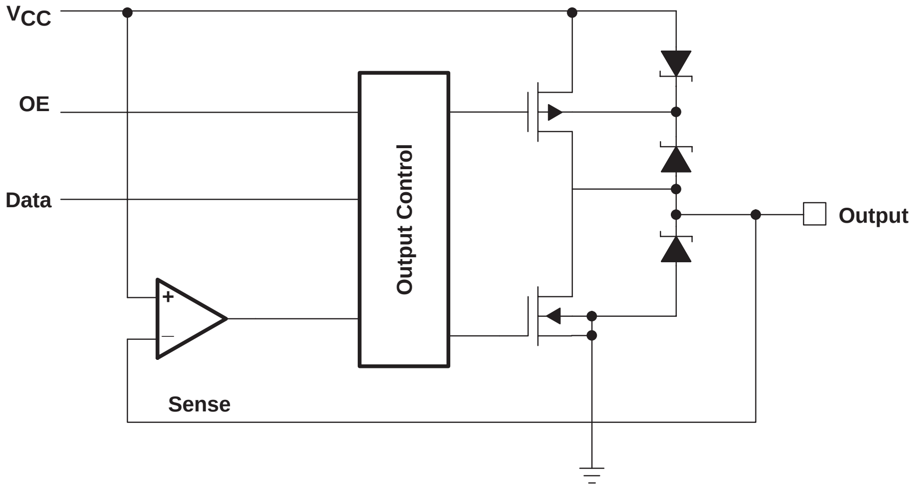


Figure 14. Simplified Auto3-state Output Stage of the ALVT Family

Assume that the output is in the active high state and a comparator monitors the voltage at the output and compares it with the supply voltage. If the voltage that is applied externally to the output exceeds the supply voltage, the output stage is switched to the high-impedance state. In this case, the logic levels that are applied to the data and control input pins of the device are irrelevant.

A current of about 30 mA is needed to reach V_{CC} + 0.6 V to trigger the auto3-state circuit, so that bus contentions are prevented, but switching noise will not trigger the auto3-state circuit. However, this also implies that the auto3-state cannot be achieved by the use of a simple pullup resistor.

It should be emphasized that a current can flow into the output only in the case of an active high. If the output is set to high impedance by the output enable (OE) control, no current will flow.

The series-opposed Schottky diodes always connect the back gate of the pullup transistor of the output stage to the higher voltage of V_{CC} or the voltage that is applied externally to the output. In this way, current flow from the output to V_{CC} is suppressed.

ALVTH logic has full overvoltage tolerance.

Translation Between Different Logic Levels

All of the logic families mentioned in this report can be operated and will function at 2.5-V and 3.3-V V_{CC}. The question is, how do they interact when one device is supplied with 2.5-V V_{CC} and the other with 3.3-V V_{CC}.

The overview of the different-level specifications from Figure 1 shows that the signal transfer from a 3.3 V V_{CC} (or higher supply voltage) logic to a 2.5-V V_{CC} logic will work perfectly if the 2.5-V part has overvoltage tolerance.

V_{OL} (3.3 V) = 0.4 V is lower than V_{IL} (2.5 V) = 0.7 V, having a noise margin of 300 mV, and V_{OH} (3.3 mV) = 2.4 V is greater than V_{IH} (2.5 V) = 1.7 V, resulting in a noise margin of 700 mV.

However, signal transfers in the opposite direction, from a 2.5-V logic to a 3.3-V (or higher supply voltage) logic is more critical. The low-level noise margin with V_{OL} (2.5 V) = 0.4 V and V_{IL} (3.3 V) = 0.7 V equals 300 mV. But the high-level definitions show that V_{OH} (2.5 V) = 2.0 V equals the input high limit of the 3.3-V V_{CC} logic V_{IH} (3.3 V) = 2.0 V (Figure 1, 5-V, 3.3-V, and 2.5 V V_{CC} switching-level comparison). In this case, the interface does not have any noise margin.

Therefore, 2.5-V V_{CC} devices should not be used to drive 3.3-V V_{CC} devices.

Table 10 gives an overview of the output-level compatibility of different logic families at 5-V, 3.3-V, 2.5-V, and 1.8-V V_{CC}.

Table 10. Output-Level Compatibility of Logic Families at Different Supply Voltages

LOGIC FAMILIES	SUPPLY VOLTAGE	CAN GENERATE 5-V LEVELS†	CAN GENERATE 3.3-V LEVELS†	CAN GENERATE 2.5-V LEVELS†	CAN GENERATE 1.8-V LEVELS†
AHC, LV	5 V	Yes	Yes‡	Yes‡	Yes‡
AHC, LV, LVC, ALVC, ALVT, AVC	3.3 V	TTL levels only	Yes	Yes§	Yes§
AHC, LV, LVC, ALVC, ALVT, AVC	2.5 V	TTL levels, but no noise margin for V_{OH}	No noise margin for V_{OH}	Yes	Yes¶
LVC, AVC	1.8 V	No#	No#	No#	Yes

† Output voltage levels exceed required input threshold voltage of the subsequent input stage at the given supply voltage.
‡ Receiver logic needs 5-V input tolerance.
§ Receiver logic needs 3.3-V input tolerance.
¶ Receiver logic needs 2.5-V input tolerance.
# V_{OH}, V_{OL} don't match, V_{OL}, V_{IL} don't match

Table 10 shows that there is a need for level-shifting devices for the interface between 5-V (CMOS) and 3.3-V V_{CC}, as well as for the translation between 2.5-V and 3.3-V V_{CC} devices.

A logic-high level at the output of the 3.3-V V_{CC} device cannot reach the required input high level of the successive 5-V CMOS input stage. Interfacing the output of the 2.5-V V_{CC} to the successive 3.3-V V_{CC} device is possible; however, in this case, there is no noise margin.

5-V to 3.3-V Level Shifters

Level shifters were developed for interfacing 5-V V_{CC} CMOS and 3.3-V V_{CC} logic. The SN74LVC4245A and SN74ALVC164245 establish a connection between 3.3-V V_{CC} and 5-V V_{CC} systems. These noninverting bus transceivers use two separate power-supply rails. The voltage ranges are defined as V_{CCA} = 4.5 V to 5.5 V and V_{CCB} = 2.7 to 3.6 V. The pin layout was designed such that they are directly replaceable by the standard devices SN74xxx245 and SN74xxx16245.

Furthermore, the SN74LVCC4245A is available for the 3.3-V to 5-V CMOS interfacing. The A-port V_{CCA} is dedicated to accepting a 5-V supply level, and the configurable B port, which is designed to track V_{CCB}, accepts voltages from 3 V to 5 V. This allows for translation from a 3.3-V V_{CC} to a 5-V V_{CC} environment, and vice versa. The LVCC4245A allows the voltage-source pin and I/O pin on the B port to float when V_{CCA} is supplied, such that there will be no disturbances on the A port if V_{CCB} and B-port I/O pins are not connected. The device will not operate until V_{CCA} and V_{CCB} are applied. This allows buffering data to and from PCMCIA sockets, permitting PCMCIA cards to be inserted and removed during operation.

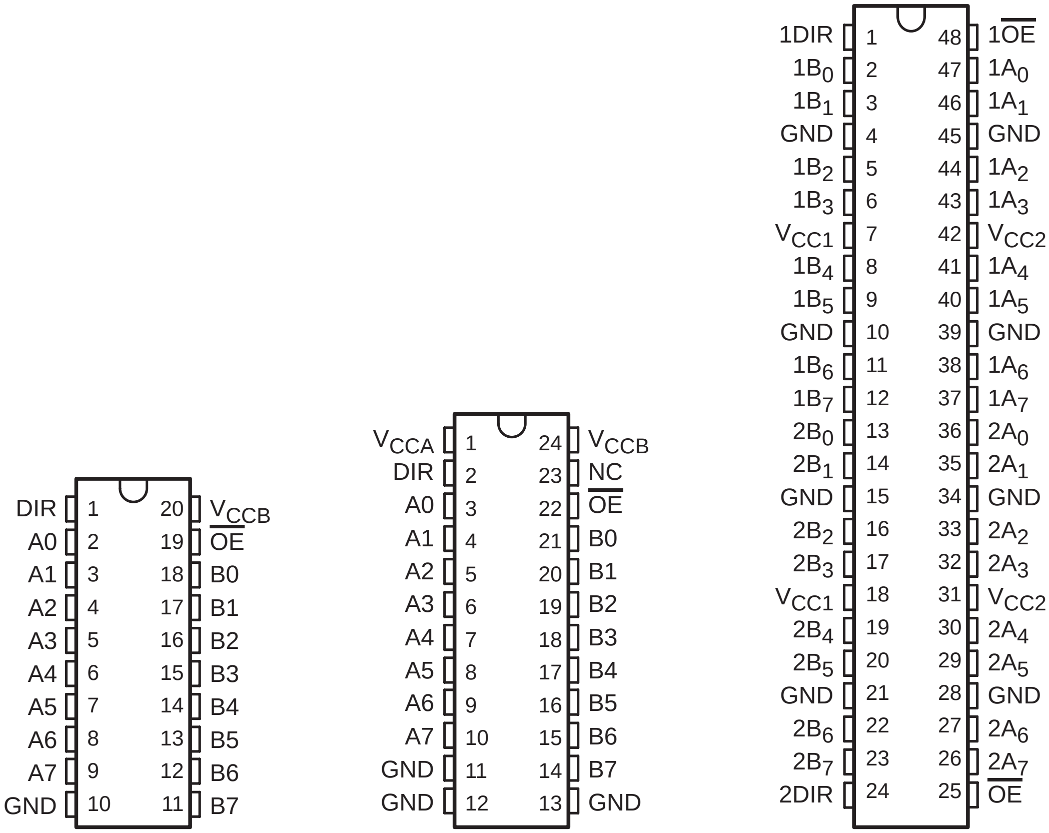
Figure 15 shows the pinouts of the SN74ALVCH164245 and the SN74LVC4245A/’LVCC4245A.

2.5-V to 3.3-V/5-V SN74LVCC3245A Level Shifter

The SN74LVCC3245A level shifter gives more flexibility for level shifting. The A-port V_{CCA} is specified for the supply-voltage range of V_{CCA} = 2.3 V to 3.6 V and V_{CCB} = 3 V to 5.5 V. This allows for translation from a 2.5-V or 3.3-V environment to 3.3-V or 5-V logic levels, and vice versa. The SN74LVCC3245A is an appropriate solution for all interfacing applications from 2.5-V or 3.3-V logic levels to 3.3-V and/or 5-V CMOS.

The LVCC3245A, like the LVCC4245A, allows the V_{CCB} voltage-source pin and I/O pin on the B port to float when outputs are disabled. This allows buffering data to and from PCMCIA sockets that permit PCMCIA cards to be inserted and removed during operation.

The pinout of the SN74LVCC3245A is shown in Figure 15.


DIR 1 20 V_{CCB}
A0 2 19 $\overline{OE}$
A1 3 18 B0
A2 4 17 B1
A3 5 16 B2
A4 6 15 B3
A5 7 14 B4
A6 8 13 B5
A7 9 12 B6
GND 10 11 B7
V_{CCA} 1 24 V_{CCB}
DIR 2 23 NC
A0 3 22 $\overline{OE}$
A1 4 21 B0
A2 5 20 B1
A3 6 19 B2
A4 7 18 B3
A5 8 17 B4
A6 9 16 B5
A7 10 15 B6
GND 11 14 B7
GND 12 13 GND
1DIR 1 48 1$\overline{OE}$
1B$_0$ 2 47 1A$_0$
1B$_1$ 3 46 1A$_1$
GND 4 45 GND
1B$_2$ 5 44 1A$_2$
1B$_3$ 6 43 1A$_3$
V_{CC1} 7 42 V_{CC2}
1B$_4$ 8 41 1A$_4$
1B$_5$ 9 40 1A$_5$
GND 10 39 GND
1B$_6$ 11 38 1A$_6$
1B$_7$ 12 37 1A$_7$
2B$_0$ 13 36 2A$_0$
2B$_1$ 14 35 2A$_1$
GND 15 34 GND
2B$_2$ 16 33 2A$_2$
2B$_3$ 17 32 2A$_3$
V_{CC1} 18 31 V_{CC2}
2B$_4$ 19 30 2A$_4$
2B$_5$ 20 29 2A$_5$
GND 21 28 GND
2B$_6$ 22 27 2A$_6$
2B$_7$ 23 26 2A$_7$
2DIR 24 25 $\overline{OE}$

’245/’C3245A **’4245A/C3234A/’C4245A** **’164245**

Figure 15. Pinouts of the LVCC3245A, LVCC4245A, LVC4245A, and ALVC164245

Open-Drain Drivers for Level Shifting

Another option for interfacing different logic levels is the use of open-drain devices. An open-drain output includes a pulldown transistor with the drain connect left open. An external connection via a pullup resistor is necessary. If the output transistor sinks current at the output, a logic-low state results. If the transistor is turned off, the logic-high state is forced by the pullup resistor, which is connected to V_{CC}.

Figure 16 shows the principle of an open-drain output interface. The value of R_{PULLUP} can be calculated from current requirements of inputs of the connected receivers, and R_{PULLUP} must be high enough to limit current into the conducting transistor.

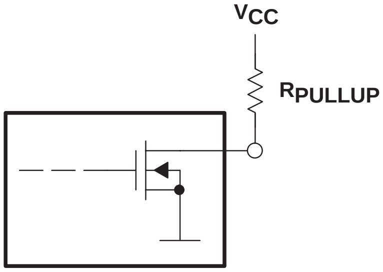


Figure 16. Open-Drain Output Principle

Table 11 shows the maximum voltage values that can be applied to the inputs and outputs of the available open-drain devices.

Table 11. Output-Overvoltage Tolerance at Open-Drain Drivers

	MAXIMUM VOLTAGE AT INPUT	MAXIMUM VOLTAGE AT OUTPUT
SN74AHC05	5.5 V	V_{CC}
SN74LV05	5.5 V	V_{CC}
SN74LVC06A	5.5 V	5.5 V
SN74LVC07A	5.5 V	5.5 V

Table 12 gives the level-shifting options for the SN74LVC07A between the different logic levels. The level shifting is possible because the pullup resistor effectively connects the output of the device to any required V_{CC}. Therefore, the correct switching level is provided to the input of the successive logic device. However, the maximum parameter values of the device, i.e., I/O voltages and current, must not be exceeded.

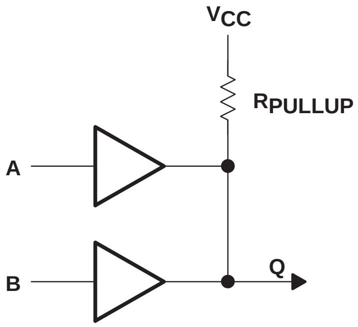
Table 12. Level Shifting Using the SN74LVC07A

SUPPLY VOLTAGE V_{CC1}	LVC07A UNDERSTANDS	PULLUP RESISTOR CAN BE CONNECTED TO	LEVEL CONVERSION RANGE
1.8 V	1.8-V levels	1.8 V, 2.5 V, 3.3 V, and 5 V	1.8 V to 1.8 V to 5.5 V
2.5 V	2.5-V levels	1.8 V, 2.5 V, 3.3 V, and 5 V	2.5 V to 1.8 V to 5.5 V
3.3 V	3.3-V levels	1.8 V, 2.5 V, 3.3 V, and 5 V	3.3 V to 1.8 V to 5.5 V
5 V	5-V levels	1.8 V, 2.5 V, 3.3 V, and 5 V	5 V to 1.8 V to 5.5 V

Wired Links

Another benefit from open-drain devices is that additional logic functionality can be built into a system without the need for additional gate devices. An active-low wired-OR and an active-high wired-AND can be implemented.

Figure 17 shows a wired connection and the resulting function table.



FUNCTION TABLE

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Figure 17. Wired Links Using Open-Drain Connections

The output (Q) is high when all inputs are high, resulting in an AND function in the case of a high-active-logic definition, and resulting in an OR function in the case of a low-active-logic definition. Those phantom links on the output side can be used to reduce component count. This kind of application is useful because a gate with n inputs can be implemented without extra active components.

Summary

The trend toward lower supply voltages continues unabated because the complexity of integrated circuits such as ASIC, CPU, and DSP requires continual reduction in structure size.

With the LV, LVC, ALVC, ALVT, AVC, and CBTLV logic families, TI offers options that are solutions for 2.5-V V_{CC} systems.

The measurement data shows that the propagation delay time of today’s 3.3-V logic families varies at V_{CC} = 2.5 V from below the 2-ns range (AVC, ALVT) to 7 ns (LV). The drive capability (I_{OH}/I_{OL}) of the devices, which were investigated at 2.5-V, varies between ±2 mA (LV) and −8 mA/24 mA (ALVT). Consequently, a suitable logic family for most of the 2.5-V applications already is available.

At 1.8-V V_{CC} the devices show good performance as well, although the SN74LVCxxxA and SN74AVC logic families are fully specified at this V_{CC} only.

All investigated samples are fully operational at 1.8 V. The migration from 3.3-V V_{CC} to 1.8-V V_{CC} can result in power savings up to 76 percent.

The logic families ALVT, LVC, and LV show full overvoltage I/O tolerance at 1.8-V, 2.5-V and 3.3-V V_{CC}.

Options on bidirectional interfacing of different logic levels are given, with the level shifters that enable bidirectional level shifting from 2.5 V to 5.5 V.

Another option enabling even more flexibility is the open-drain driver, SN74LVC07A, that interfaces 1.8-V up to 5.5-V logic levels.

Acknowledgment

The author of this report is Johannes Huchzermeier.

Glossary

A

ABT	Advanced BiCMOS Technology
AC	Advanced CMOS
AHC	Advanced High-Speed CMOS
ALS	Advanced Low-Power Schottky
ALVC	Advanced Low-Voltage CMOS
ALVT	Advanced Low-Voltage Technology
AS	Advanced Schottky
Auto3-state	During the active-high state at the output, devices with auto3-state tolerate a higher voltage level at the outputs. This is also called overvoltage protection.
AVC	Advanced Very Low-Voltage CMOS

B

BCT	BiCMOS Technology
BiCMOS	Combination of Bipolar and CMOS processes: CMOS input structure and bipolar output structure
Bus hold	Input circuitry that holds the last valid logic state that was applied to it before entering a nondefined state on the bus until a new valid logic state is driven actively.

D

DUT	Device under test

G

GND	Ground

I

I_{CC}	Supply current
I/O	Input/Output

L

LS	Low-Power Schottky
LV	Low-Voltage CMOS, originally designed for V_{CC} = 3.3-V, also specified at 5 V
LVC	Low-Voltage CMOS
LVT	Low-Voltage Technology

O

Overvoltage protection	See auto3-state and 3-/5-V tolerance

R

R_L	Load resistor
R_{PULLUP}	Resistor that is used for open-drain devices to ensure a logic-high level on the signal line
ROC	Recommended operating conditions

S

Series resistor	A resistor that is implemented on the output stage of a bus driver. With this resistor, the effective output impedance of the driver is shifted to a value of about 50 Ω, which is an optimum line termination.
S	Schottky
SPICE	Simulation Program with Integrated Circuit Emphasis

T

3-/5-V tolerance	Logic devices with 5-V (3.3-V) tolerance tolerate 5-V (3.3-V) CMOS logic levels at their input and output during the high-impedance state, while supplied with 2.5-V
TTL-level	Transistor-transistor logic levels

V

V_{CC}	Supply voltage

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Input and Output Characteristics of Digital Integrated Circuits at V_{CC} *= 3.3-V Supply Voltage*, literature number SCYA003

Standards

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EIA/JEDEC, Standard JESD 8-5, *2.5 +/− 0.2 V (Normal Range) and 1.8-V to 2.7-V (Wide Range) Power-Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits*, October 1995

EIA/JEDEC, Standard JESD 8-7, *1.8 V +/− 0.15 V (Normal Range) and 1.2-V to 1.95-V (Wide Range) Power-Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits*, February 1997

Flexible Voltage-Level Translation With CBT Family Devices

SCDA006
July 1999

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Abstract

Voltage translation between buses with incompatible logic levels can be accomplished using Texas Instruments (TI™) translation-voltage clamps (TVC) or standard crossbar technology (CBT) devices. CBT devices in this application offer flexibility in designs, protection of circuits that are sensitive to high-state voltage-level overshoots, and cost efficiency.

Introduction

In designing electronics systems, proper interfaces between buses with incompatible logic levels must be provided. Voltage-level translation is necessary to allow the interconnection with flexibility to provide a future migration path to lower-voltage input/output (I/O) levels (see Figure 1). TI offers I/O voltage translation solutions with two device families.

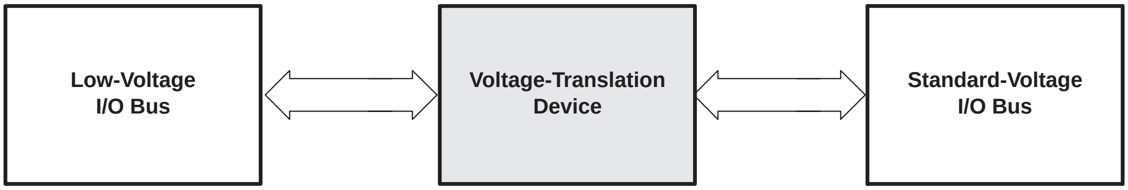

Figure 1. Flexible Voltage-Translation Application

One possible solution for flexible voltage translation is the TI translation-voltage clamp (TVC) family that has been designed specifically for protecting sensitive I/Os (see Figure 2). The information in the data sheet for each TVC-family device describes the I/O protection application of the TVC family and should enable the design engineer to successfully implement an I/O protection circuit utilizing the TI TVC solution.

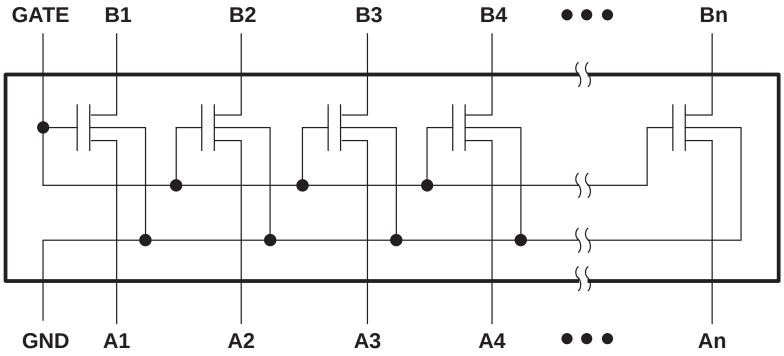

Figure 2. Simplified Schematic of a Typical TVC-Family Device

A comparable solution, allowing cost-effective and flexible voltage translation implemented with standard crossbar technology (CBT) family devices is described in this application report.

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Device Description

The CBT family of devices provides an array of n-type metal-oxide semiconductor (NMOS) field-effect transistors (FETs) with the gates cascaded together to a control circuit (see Figure 3). Within a CBT device, all of the transistors are fabricated at the same time on one integrated die. This leads to a very small fabrication-process variation in the characteristics of the transistors. Because, within the device, the characteristics from transistor-to-transistor are the same, there is minimal deviation from one output to another. This is a large benefit of the CBT solution over discrete devices.

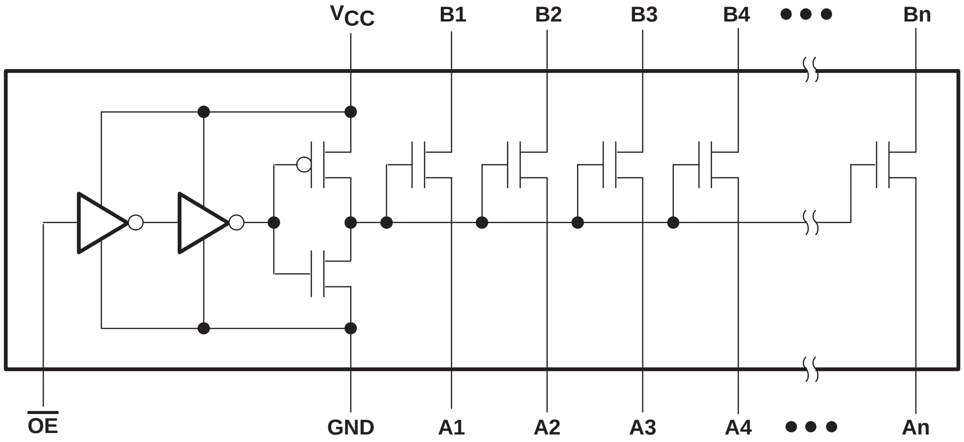


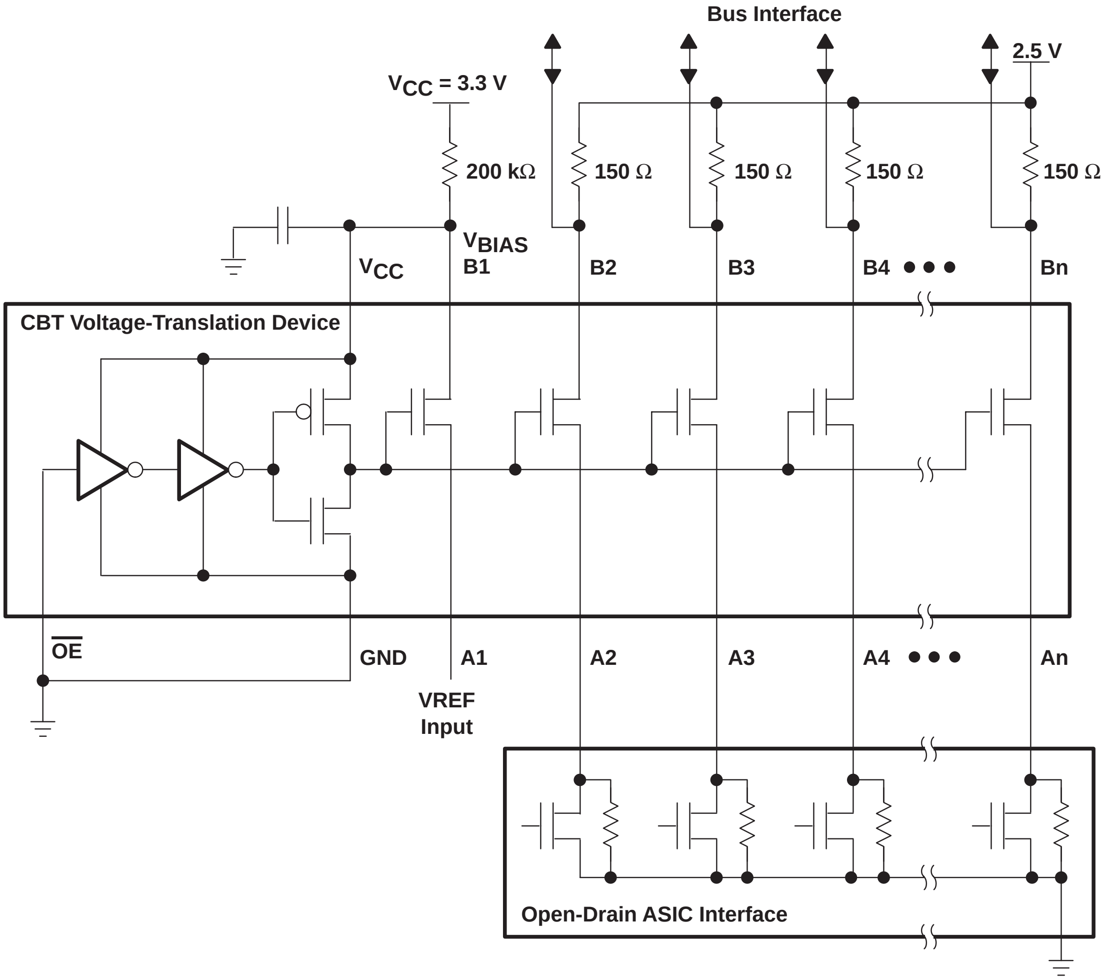
Figure 3. Simplified Schematic of a Typical CBT-Family Device

A CBT device can be used as a voltage limiter or voltage translator by connecting one of the FETs as a reference transistor, and the remainder as pass transistors. The most positive voltage on the low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. All of the transistors in the array have the same electrical characteristics; therefore, any one of them can be used as the reference transistor. Because the transistors are fabricated symmetrically and the I/O signals are bidirectional through each FET, either port connection of each bit can be used as the low-voltage side.

Application

When the active-low, output-enable ($\overline{OE}$) input is connected directly to ground, the gate of the p-channel FET in the final inverter of the control circuitry is grounded. This saturates the p-channel, turning the FET on hard, and effectively connects the V_{CC} input directly to the gates of the n-channel pass transistors, thus providing external control of the gate voltage.

For the example in Figure 4, the ASIC has an open-drain interface that is sensitive to high-state voltages. For the voltage-limiting configuration, the CBT $\overline{OE}$ input must be grounded. The V_{CC} input must be connected to one side (A or B) of any one of the transistors. This connection determines the V_{BIAS} input of the reference transistor. The V_{BIAS} input is connected through a pullup resistor (typically 200 kΩ) to the V_{DD} supply. A filter capacitor on V_{BIAS} is recommended. The opposite side is used as the reference voltage (V_{REF}) connection. The V_{REF} input must be less than $V_{BIAS} − 1$ V to bias the reference transistor into conduction. The reference transistor regulates the V_{BIAS}, thus gate voltage (V_G) of all the pass transistors. The gate voltage is determined by the characteristic gate-to-source voltage difference (V_{GS}) because $V_G = V_{REF} + V_{GS}$. The low-voltage side of the pass transistors has a high-level voltage limited to a maximum of $V_G − V_{GS}$, or V_{REF}. A weak pulldown resistor on open-drain outputs ensures that when the output switches off (logic high), overshoots do not cause the voltage to exceed the maximum voltage rating.



Bus Interface
2.5 V
VCC = 3.3 V
200 kΩ
150 Ω
150 Ω
150 Ω
150 Ω
VBIAS
B1
VCC
B2
B3
B4 ● ● ●
Bn
CBT Voltage-Translation Device
OE
GND
A1
A2
A3
A4 ● ● ●
An
VREF
Input
Open-Drain ASIC Interface

Figure 4. Typical Application of CBT as a Voltage-Translation Device

Conclusion

TI offers a line of CBT devices, including standard, Widebus™, dual-bit, and single-bit functions. The flexibility of CBT enables a low-voltage migration path for advanced designs to align with existing industry standards. The TI CBT family provides the designer with a solution for voltage-level translation and protection of circuits with I/Os that are sensitive to high-state-voltage-level overshoots.

Acknowledgment

The authors of this application report are Thomas V. McCaughey, Stephen M. Nolan, and John D. Pietrzak.

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TI Logic Solutions for Memory Interleaving with the Intel™ 440BX Chipset

SCCA001
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Abstract

Increasing performance requirements of personal computers that necessitate a larger number of SDRAMs and DIMMs can be met by an FET-switch muliplexer. Four devices for memory interleaving for the 440BX and other core-logic chipsets incorporate internal pulldown resistors, damping resistors, and make-before-break features that increase speed while maintaining minimal simultaneous-switching noise.

Introduction

Rapid advancements in hardware and software are emerging to meet the performance needs within the personal computer (PC) industry. To meet the needs of increasing memory requirements, a large number of SDRAMs are needed. Consequently, a larger number of DIMMs are needed, adding heavy loading to the memory controller and to the data lines. To reduce the loading and maintain signal integrity and reliability of the system, an FET-switch multiplexer is recommended for this application. Texas Instruments (TI™) offers four such devices for memory interleaving for the Intel™ 440BX logic chipset and for other core-logic chipsets that need interleaving capability. This report discusses TI's logic solutions using SN74CBT16292, SN74CBTLV16292, SN74CBT162292, and SN74CBTLV162292 devices.

Background

Designing a reliable, high-performance memory system forces designers to consider every detail of the system. Up to 384-Mbytes of system memory can be achieved by using 64-Mbit technology and 168-pin, 8-byte, registered SDRAM DIMMs on three double-sided DIMMs. To achieve a larger memory system with the same type of memory device, a fourth DIMM should be introduced. But, this increases loading. To reduce the loading, an FET-switch multiplexer is recommended. An FET switch on the data line splits the load and reduces it by 50%. In order to design a simple, cost-effective, reliable system, several factors must be considered during FET-switch selection. In the following section, significant information about the SN74CBT16292, SN74CBTLV16292, SN74CBT162292, and SN74CBTLV162292 devices is discussed, as well as applications of this switch on the DIMM.

Device Information

The devices discussed are members of the TI Widebus™ family, which are manufactured using TI's enhanced-performance implanted CMOS (EPIC™) submicron process. Each of these devices is a 12-bit 1-of-2 FET multiplexer/demultiplexer with 500-Ω internal pulldown resistors (R_{INT}). The pinout is the same for each device (see Figure 1). SN74CBT16292 and SN74CBT162292 are designed for 4-V to 5.5-V V_{CC} operation. SN74CBTLV16292 and SN74CBTLV162292 are designed for 2.3-V to 3.6-V V_{CC} operation. The low on-state resistance (4 Ω) of the switch allows connections to be made with minimal propagation delay. When the select (S) input is low, port A is connected to port B1 and port B2 is pulled down through R_{INT} to ground. When S is high, port A is connected to B2 and R_{INT} is connected to port B1 (see Table 1 and Figure 2).

All four devices have the same function. They are different from each other with respect to special features that are discussed in the following paragraphs.

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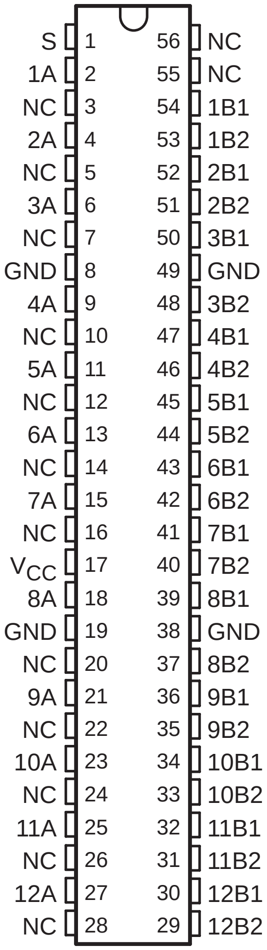
Special Features

Internal pulldown resistors

On all four of these devices, ports B1 and B2 have an internal 500-Ω pulldown resistor connected to GND through a switch. When port B is disconnected from port A, instead of floating, port B is connected to GND through the 500-Ω resistor. If unused inputs are not connected to GND or V_{CC}, they follow any stray noise on that pin, creating unpredictable circuit performance. Termination of unused inputs by connecting them with the internal pulldown resistor increases system reliability and minimizes power dissipation.


S 1
1A 2
NC 3
2A 4
NC 5
3A 6
NC 7
GND 8
4A 9
NC 10
5A 11
NC 12
6A 13
NC 14
7A 15
NC 16
VCC 17
8A 18
GND 19
NC 20
9A 21
NC 22
10A 23
NC 24
11A 25
NC 26
12A 27
NC 28
56 NC
55 NC
54 1B1
53 1B2
52 2B1
51 2B2
50 3B1
49 GND
48 3B2
47 4B1
46 4B2
45 5B1
44 5B2
43 6B1
42 6B2
41 7B1
40 7B2
39 8B1
38 GND
37 8B2
36 9B1
35 9B2
34 10B1
33 10B2
32 11B1
31 11B2
30 12B1
29 12B2

NC − No internal connection

Figure 1. Pinout for SN74CBT16292, SN74CBT162292, SN74CBTLV16292, and SN74CBTLV162292 Devices

Table 1. Function Table for SN74CBT16292, SN74CBT162292, SN74CBTLV16292, and SN74CBTLV162292 Devices

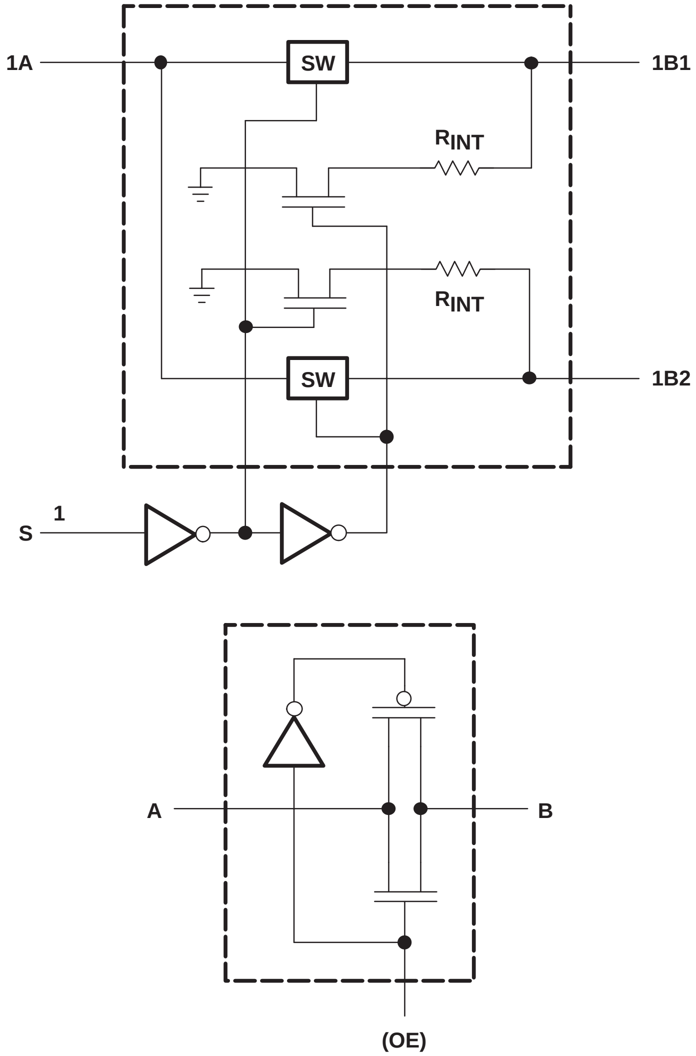
S INPUT	FUNCTION
L	A port = B1 port R_{INT} = B2 port
H	A port = B2 port R_{INT} = B1 port

Damping resistors

SN74CBT162292 and SN74CBTLV162292 have a 25-Ω internal damping resistor connected to port A inputs/outputs. This series termination resistor matches line impedance with the transmission line to reduce noise due to line reflection. It controls signal overshoot and undershoot and maintains noise at a minimum value. If a designer is concerned about the signal integrity, a series damping resistor can be added externally, if it is not incorporated into the device. By using the SN74CBT162292 or SN74CBTLV162292 devices, no external resistors are required.

Make-before-break feature

This unique make-before-break feature is available on all four of these devices. Figure 2 is the logic diagram of CBTLV16292. When S is low, 1A is connected to 1B1 and R_{INT} is connected to 1B2 through the load n channel. When S is high, 1A is connected to 1B2, and R_{INT} is connected to 1B1 through the load n channel. During this transition, the pass p channel or n channel will turn on first, then the load transistor will turn off. This feature causes port 1B1 and 1B2 (outputs) always to be connected either to GND through R_{INT} or to the input, preventing the output from floating and ensuring system reliability. The interval between these two events is known as make-before-break time (t_{mbb}). Figure 3 shows the make-before-break switching, where t_{mbb} is approximately 1.75 ns. The maximum value for t_{mbb} can be 2 ns, which means that the maximum interval between switching on the pass transistor and switching off the load transistor can be 2 ns maximum, which is very low.



Simplified Schematic of Each FET Switch

Figure 2. Logic Diagram for SN74CBTLV16292

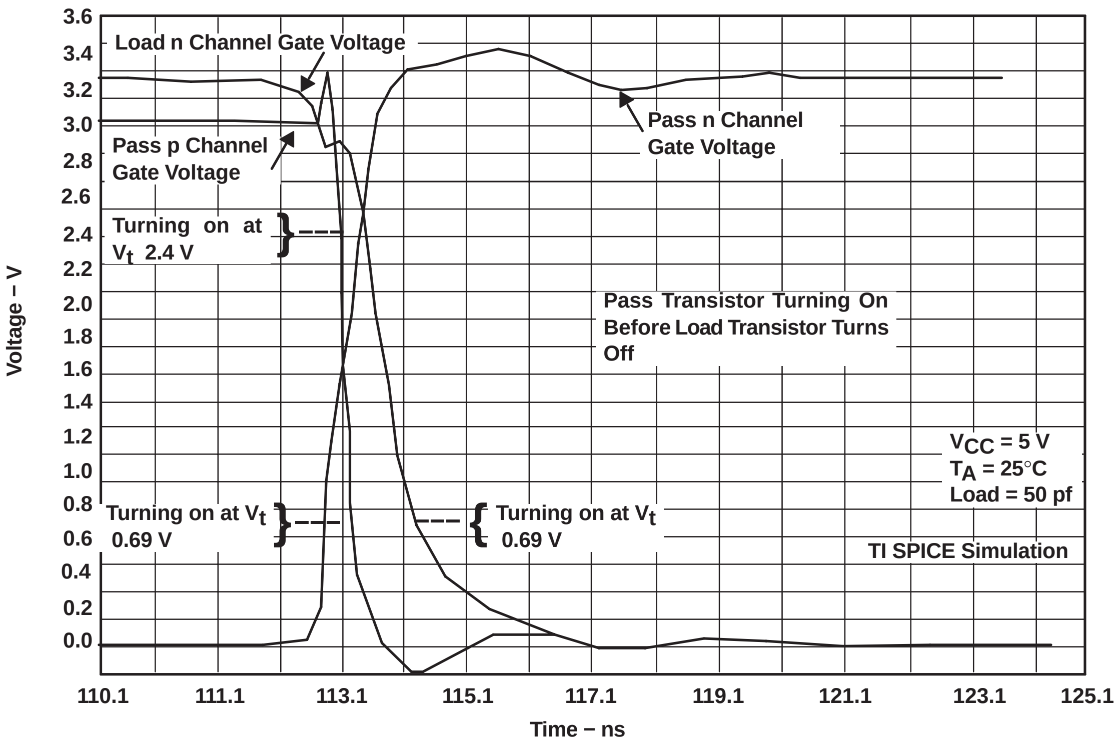


Figure 3. Make-Before-Break Switching for CBTLV16292

Tables 2 and 3 summarize the features and benefits of the CBT16292, CBT162292, CBTLV16292, and CBTLV162292 devices.

Table 2. Features of the CBT Devices

DEVICE	PINS	V_{CC} NOMINAL	I/O VOLTAGES	SERIES RESISTORS	INTERNAL PULLDOWN RESISTORS
CBT16292	56	5 V	3.3 V or 5 V	No	Yes
CBT162292	56	5 V		Yes	Yes
CBTLV16292	56	3.3 V	3.3 V only	No	Yes
CBTLV162292	56	3.3 V		Yes	Yes

Table 3. Benefits of the CBT Devices

DEVICE	SERIES DAMPING RESISTOR	UNUSED INPUTS	V_{CC}
CBT16292	External resistor necessary for impedance match	Connected to ground through 500-Ω pulldown resistor	
CBT162292	No external resistor required	Connected to ground through 500-Ω pulldown resistor	
CBTLV16292	External resistor necessary for impedance match	Connected to ground through 500-Ω pulldown resistor	3-V V_{CC} allows same power plane as memory
CBTLV162292	No external resistor required	Connected to ground through 500-Ω pulldown resistor	3-V V_{CC} allows same power plane as memory

Performance

Speed

In memory-interleaving applications, t_{en} and t_{dis} of the bus switches determine the speed of data transfer. All four of these devices have very fast enable and disable times. Figure 4 shows the enable time vs load capacitance for the four devices. The graph shows a very fast enable time over a wide range of load capacitance. At 25-pF to 30-pF load, which closely matches the DIMM loading, all the devices have t_{en} of 3 ns to 4 ns.

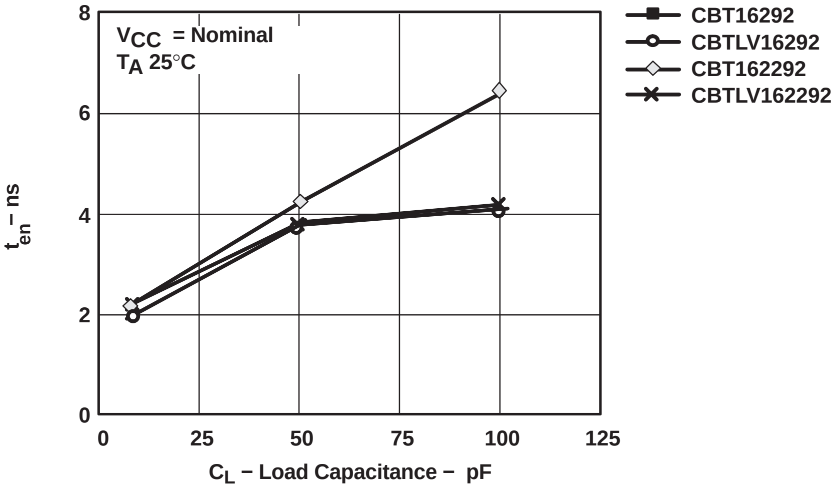


Figure 4. t_{en} vs C_L

Figure 5 shows the disable time over a wide range of load capacitance. The graph shows that, at a load of 25 pF to 30 pF, t_{dis} is between 3 and 4 ns.

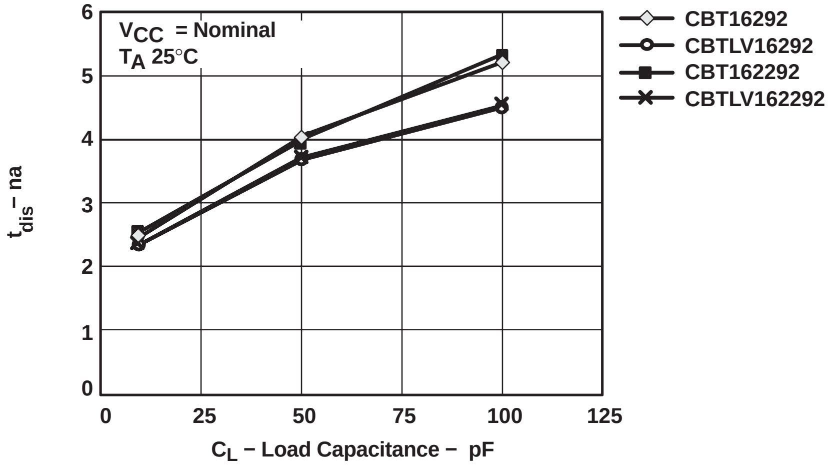


Figure 5. t_{dis} vs C_L

Simultaneous-switching noise

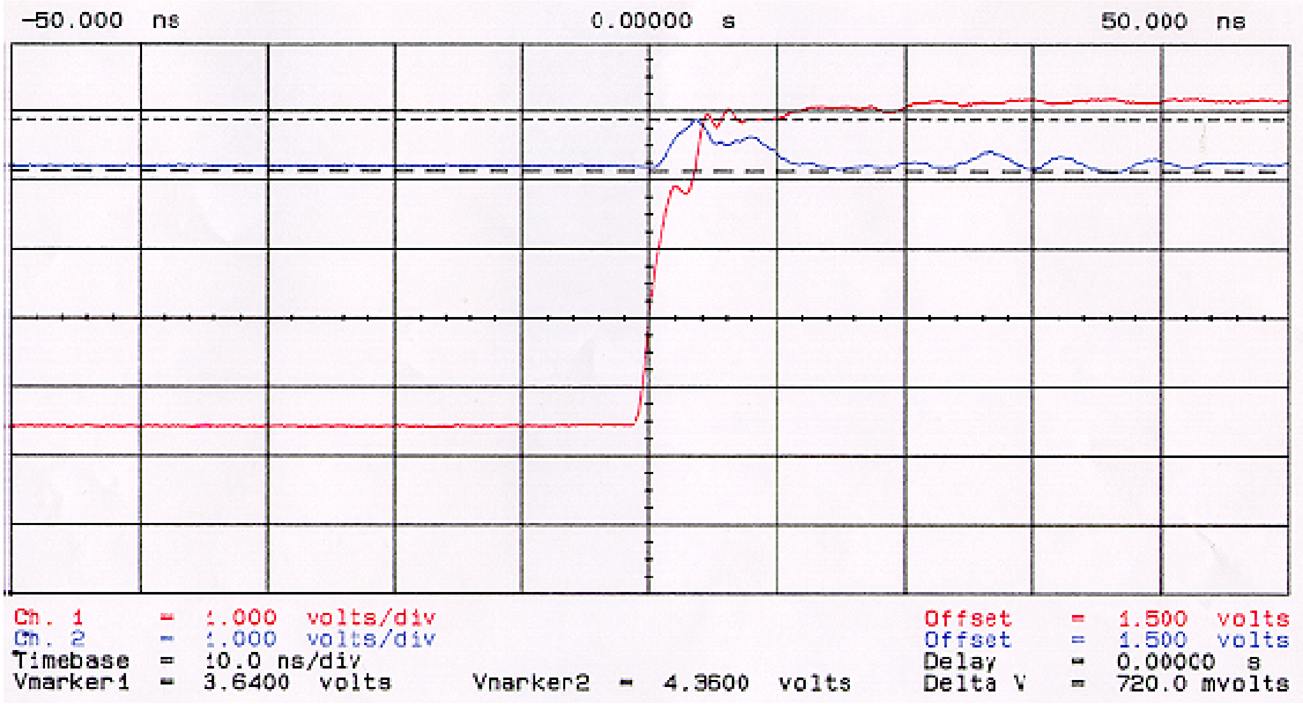
The effects of simultaneously switching multiple outputs of a single device can be examined using a standard procedure. The method of measuring simultaneous switching consists of holding one output low and switching all other outputs from the high state to the low state. Because of the package mutual inductance, transient current flows through the package and into the output pin that is being held low. This causes a rise in voltage and the output begins to ring. The peak of this ringing is called output low peak voltage (V_{OLP}). This is the most common and critical measure of ground bounce. Output low valley voltage (V_{OLV}) is the lowest point the low output reaches, which is usually a negative voltage.

In a similar way, a single output is held high and all other outputs are switched from the low state to the high state. Due to the package mutual inductance, the high output voltage drops, causing the outputs to ring. This valley is called output high valley voltage (V_{OHV}) and the peak is called output high peak voltage (V_{OHP}).

When V_{OLP} goes above 0.8 V, the device enters the threshold region and can switch from the low state to the high state. If V_{OHV} drops below 2 V, the device can switch from high to low. Table 4 shows the simultaneous switching data for the four CBT devices under discussion. Table 4 shows that these devices maintain a safe value for both V_{OLP} and V_{OHV}. Figures 6 through 13 show the simultaneous-switching plots for CBT16292, CBT162292, CBTLV16292, and CBTLV162292.

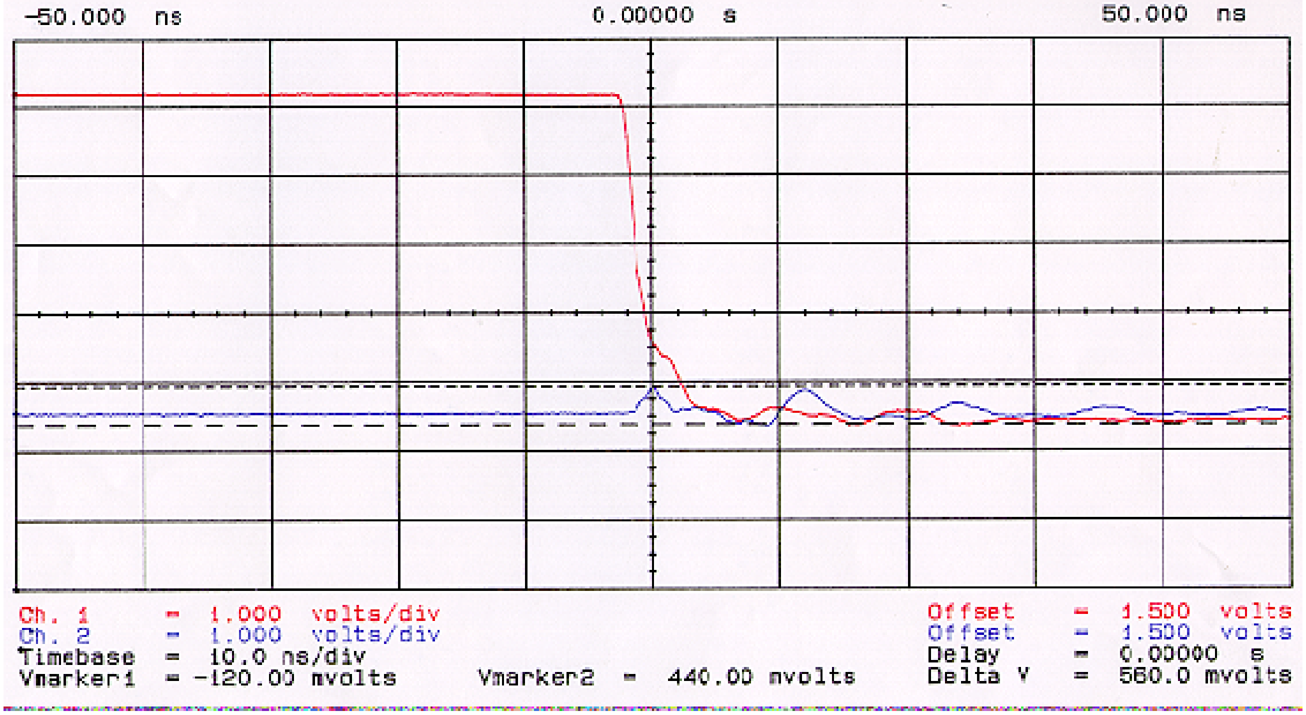
Table 4. Simultaneous-Switching Data

OPERATING CONDITION	DEVICE	V_{OLV} (mV)	V_{OLP} (mV)	V_{OHV} (mV)	V_{OHP} (mV)
V_{CC} = Nominal T_A= 25°C C_L = 50 pF	CBT16292	−0.12	0.44	3.64	4.36
	CBT162292	−0.08	0.24	3.44	4.00
	CBTLV16292	−0.14	0.28	3.14	3.44
	CBTLV162292	−0.06	0.24	2.98	3.24



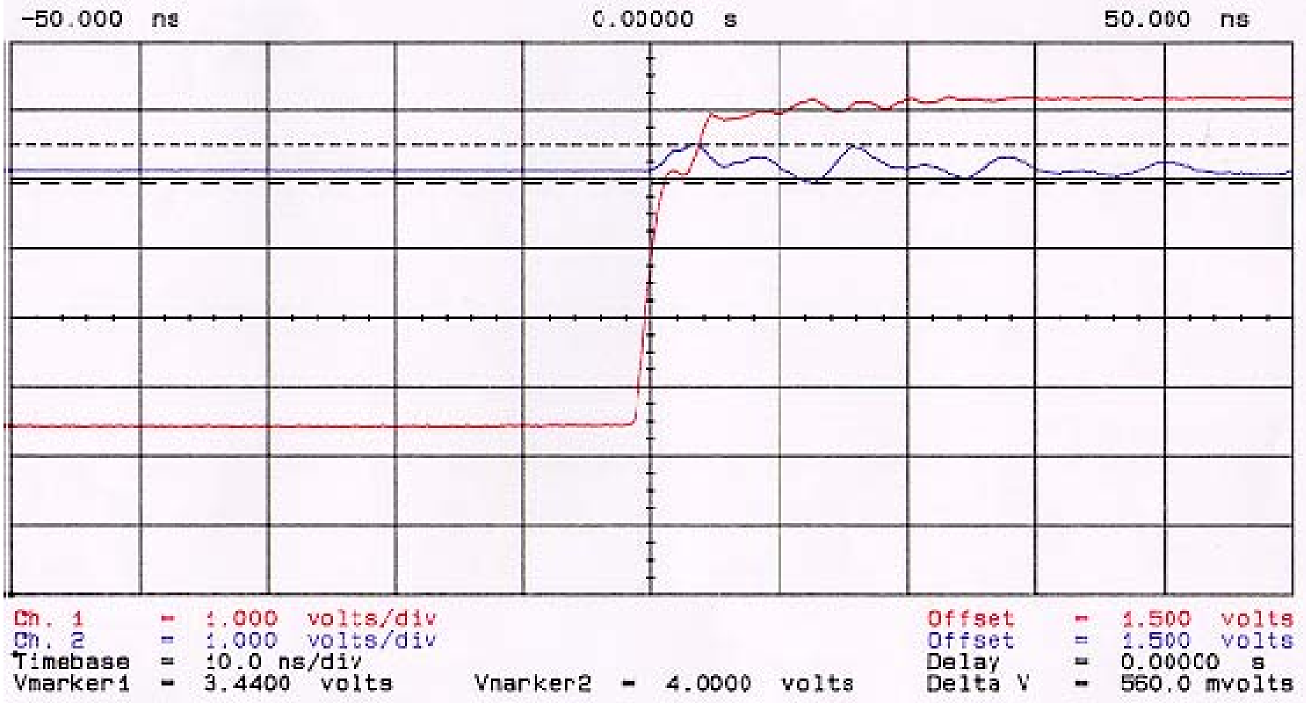
```
Ch. 1      =  1.000  volts/div                          Offset    =  1.500  volts
Ch. 2      =  1.000  volts/div                          Offset    =  1.500  volts
Timebase   =  10.0 ns/div                               Delay     =  0.00000  s
Vmarker1   =  3.6400  volts     Vmarker2  =  4.3600  volts   Delta V  =  720.0 mvolts
```

Figure 6. Simultaneous-Switching Plot for CBT16292 (V_{OHV}, V_{OHP})



```
Ch. 1     = 1.000  volts/div                         Offset  = 1.500  volts
Ch. 2     = 1.000  volts/div                         Offset  = 1.500  volts
Timebase  = 10.0 ns/div                              Delay   = 0.00000  s
Vmarker1  = -120.00 mvolts     Vmarker2  =  440.00 mvolts    Delta V = 560.0 mvolts
```

Figure 7. Simultaneous-Switching Plot for CBT16292 (V_{OLV}, V_{OLP})



```
Ch. 1     = 1.000  volts/div                         Offset  = 1.500  volts
Ch. 2     = 1.000  volts/div                         Offset  = 1.500  volts
Timebase  = 10.0 ns/div                              Delay   = 0.00000  s
Vmarker1  = 3.4400   volts     Vmarker2  =  4.0000   volts    Delta V = 560.0 mvolts
```

Figure 8. Simultaneous-Switching Plot for CBT162292 (V_{OHV}, V_{OHP})

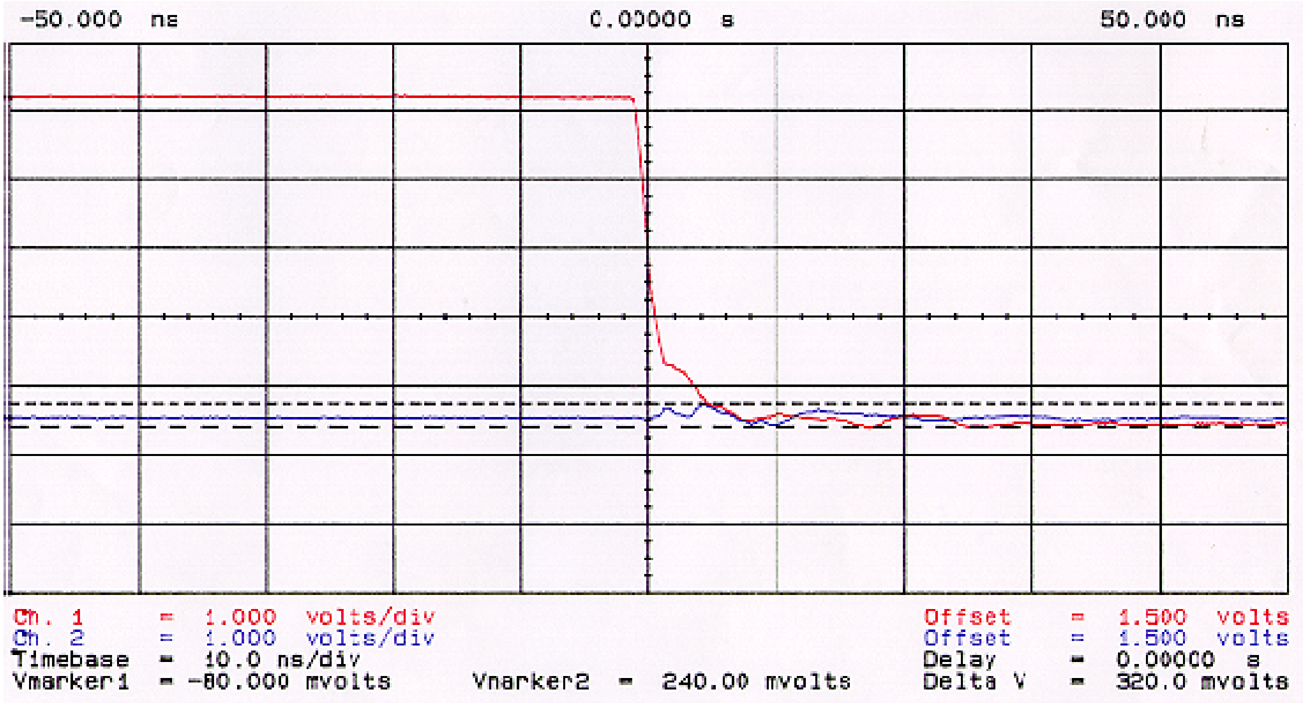


Figure 9. Simultaneous-Switching Plot for CBT162292 (V_{OLV}, V_{OLP})

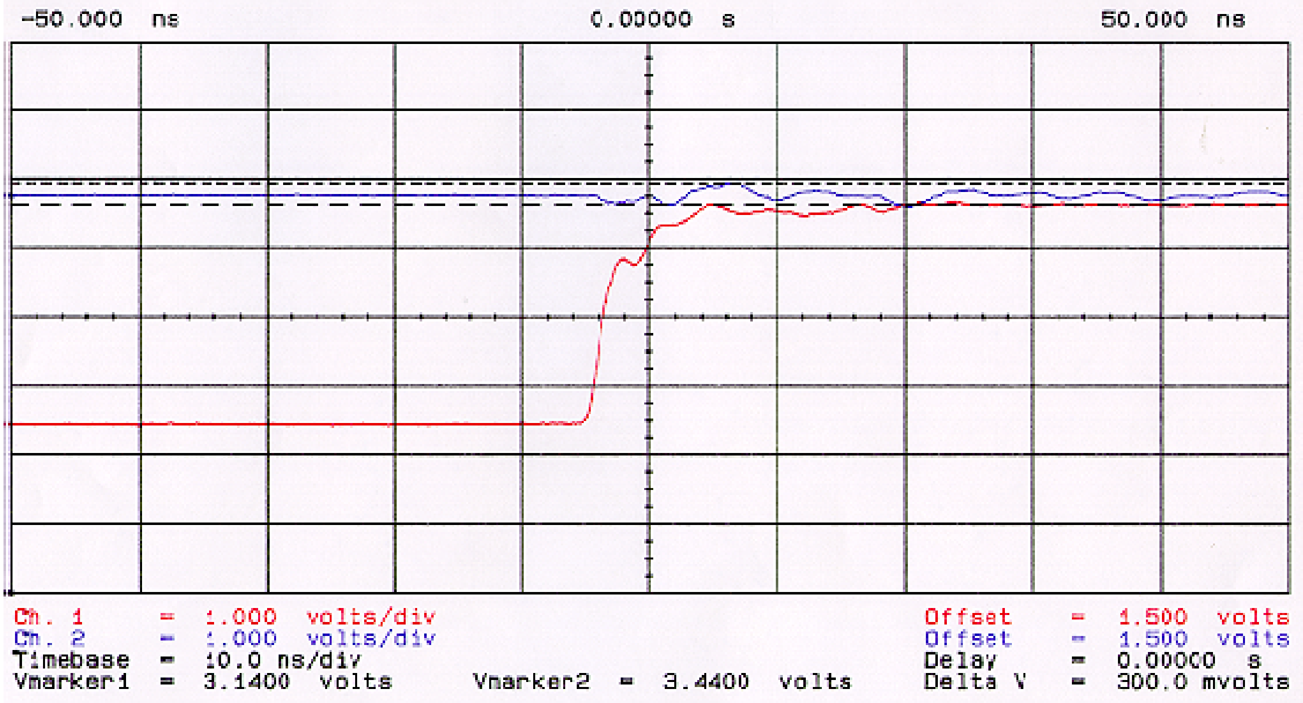
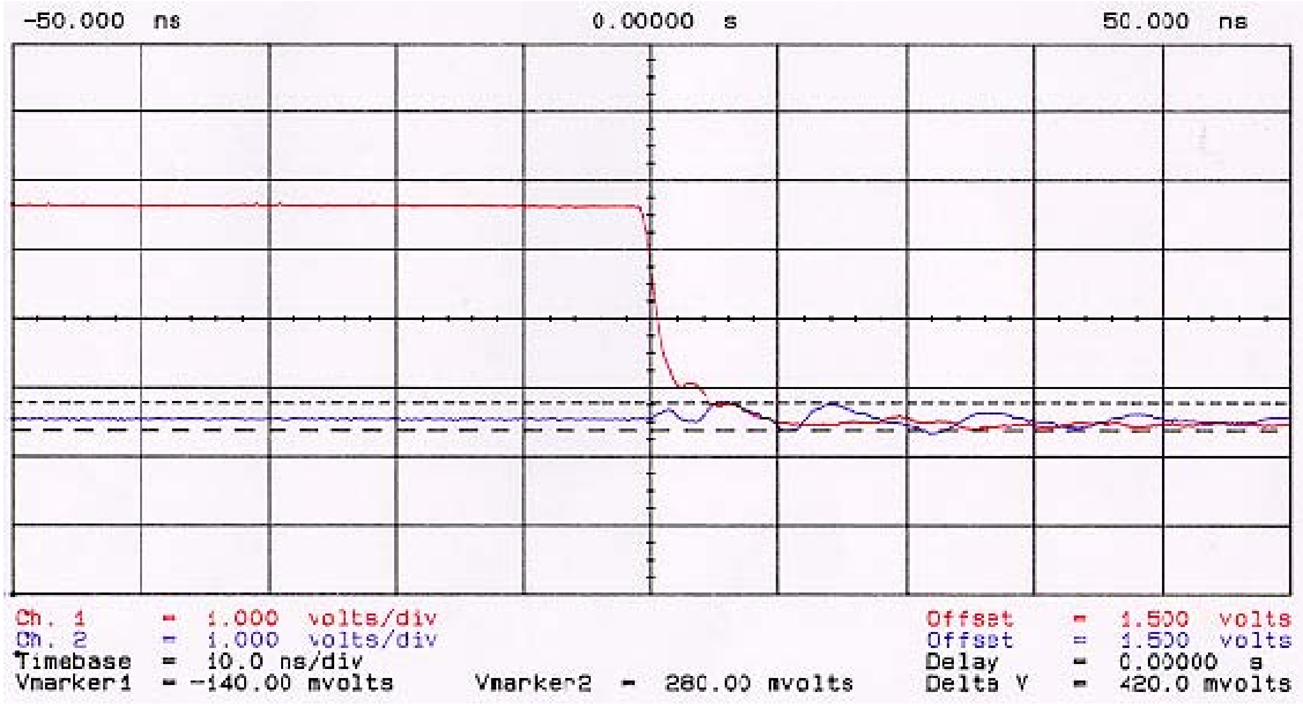
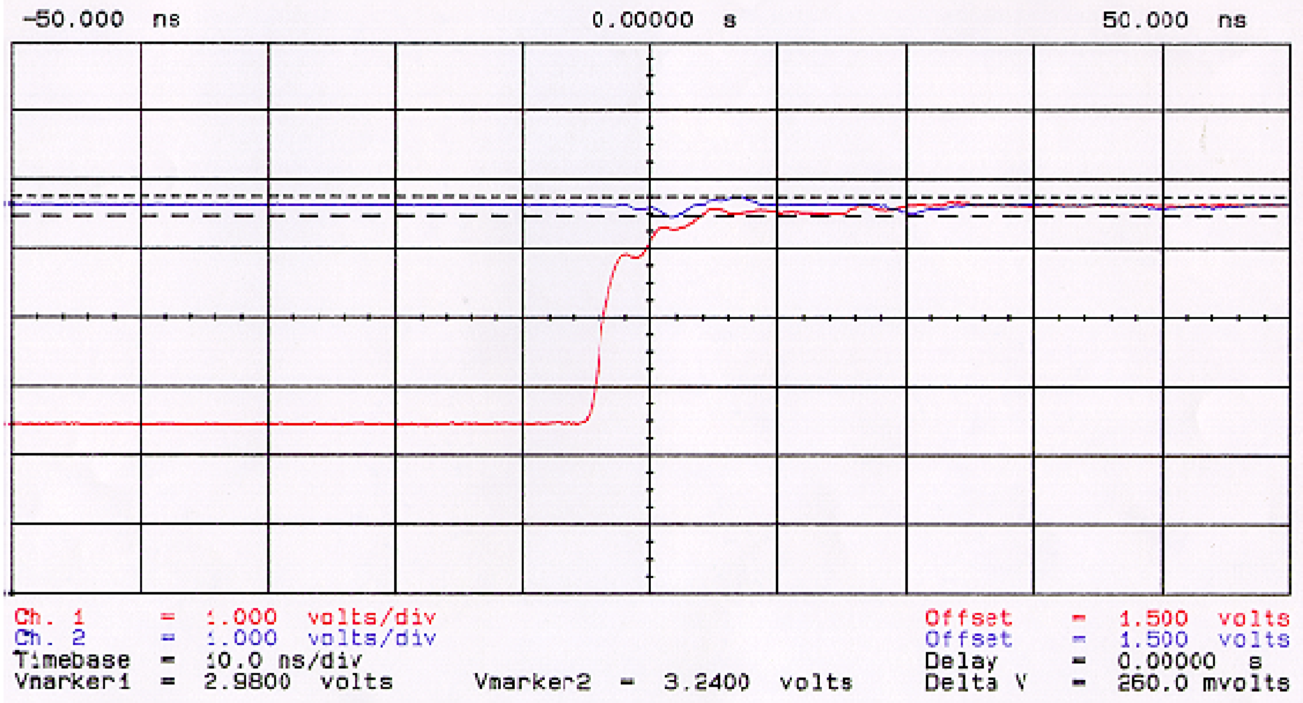


Figure 10. Simultaneous-Switching Plot for CBTLV16292 (V_{OHV}, V_{OHP})



Ch. 1 = 1.000 volts/div
Ch. 2 = 1.000 volts/div
Timebase = 10.0 ns/div
Vmarker1 = −140.00 mvolts
Vmarker2 = 280.00 mvolts
Offset = 1.500 volts
Offset = 1.500 volts
Delay = 0.00000 s
Delta V = 420.0 mvolts

Figure 11. Simultaneous-Switching Plot for CBTLV16292 (V_{OLV}, V_{OLP})



Ch. 1 = 1.000 volts/div
Ch. 2 = 1.000 volts/div
Timebase = 10.0 ns/div
Vmarker1 = 2.9800 volts
Vmarker2 = 3.2400 volts
Offset = 1.500 volts
Offset = 1.500 volts
Delay = 0.00000 s
Delta V = 260.0 mvolts

Figure 12. Simultaneous-Switching Plot for CBTLV162292 (V_{OHV}, V_{OHP})

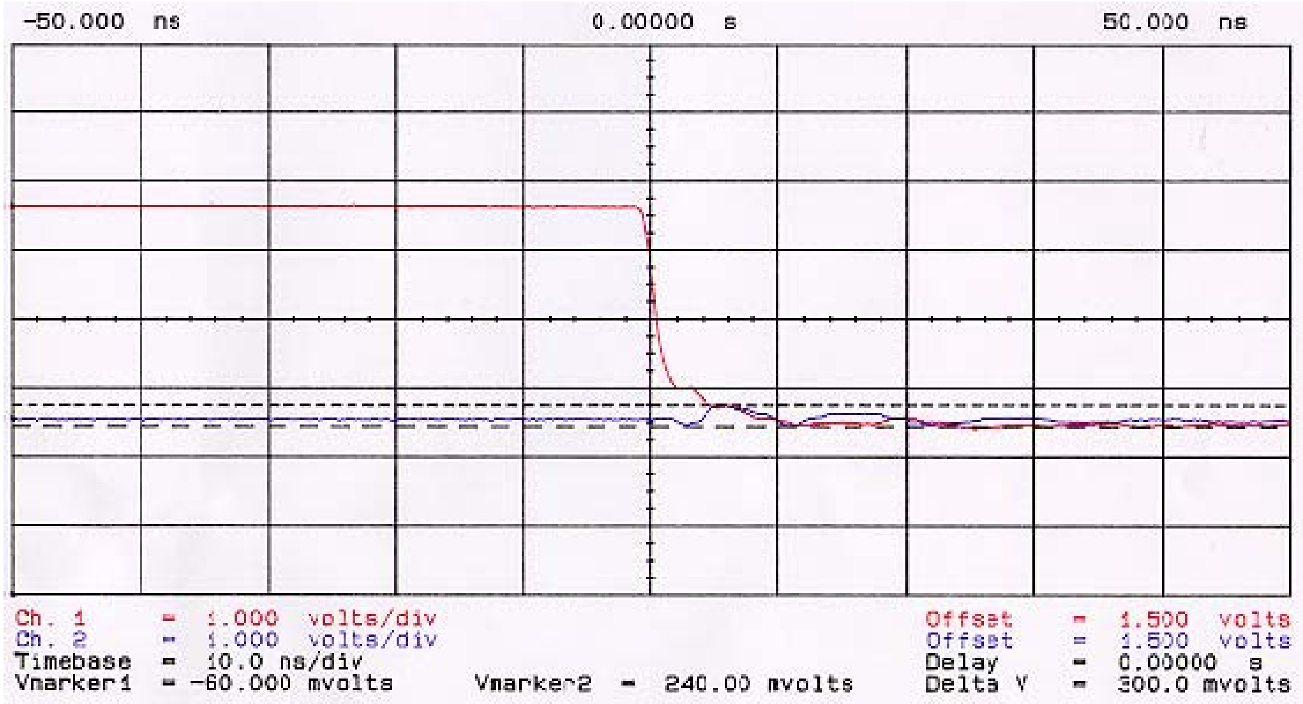


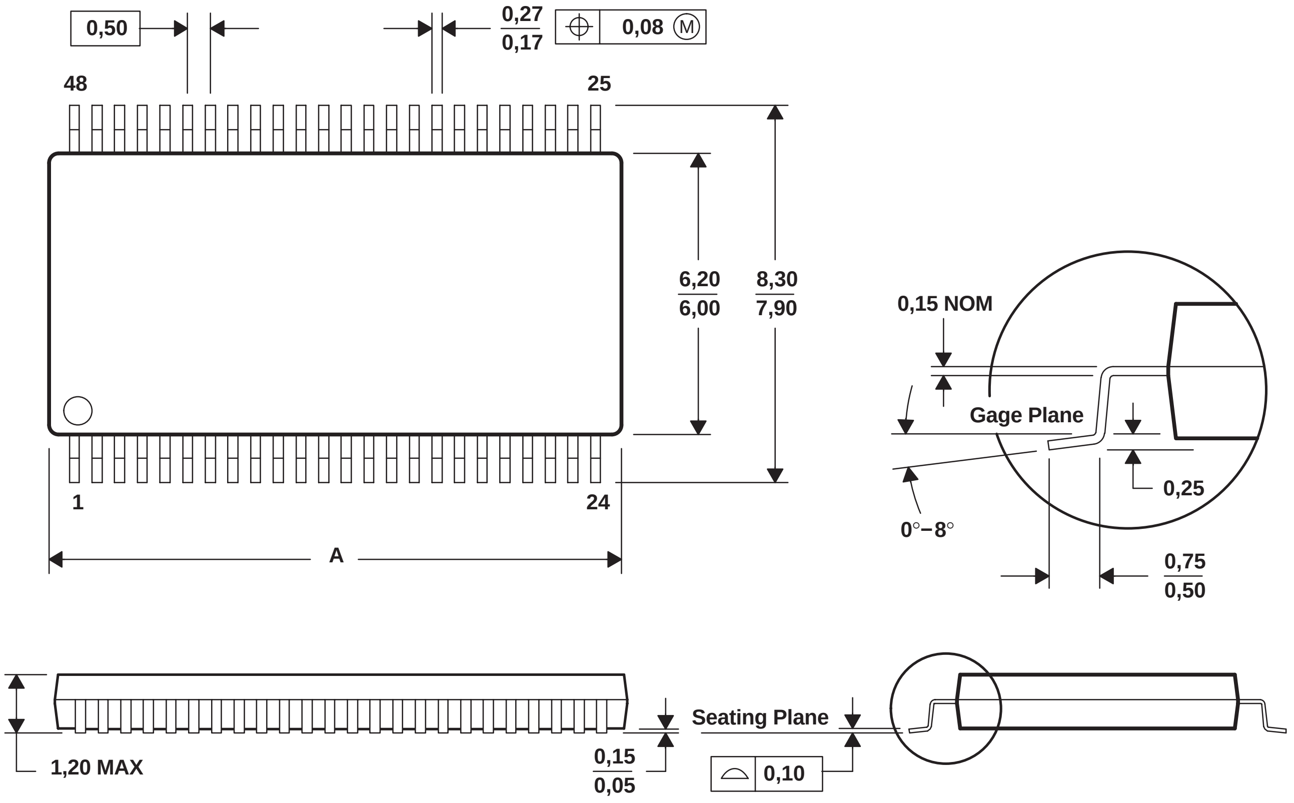
Figure 13. Simultaneous-Switching Plot for CBTLV162292 (V_{OLV}, V_{OLP})

Package Information

All of the devices discussed in this application report are available in the JEDEC-standard TSSOP (DGG) and TVSOP (DGV) packages. The mechanical data are shown in Figures 14 and 15.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN


0,50
0,27
0,17
0,08 M
48
25
6,20
6,00
8,30
7,90
0,15 NOM
Gage Plane
0,25
0°−8°
0,75
0,50
1
24
A
1,20 MAX
0,15
0,05
Seating Plane
0,10

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

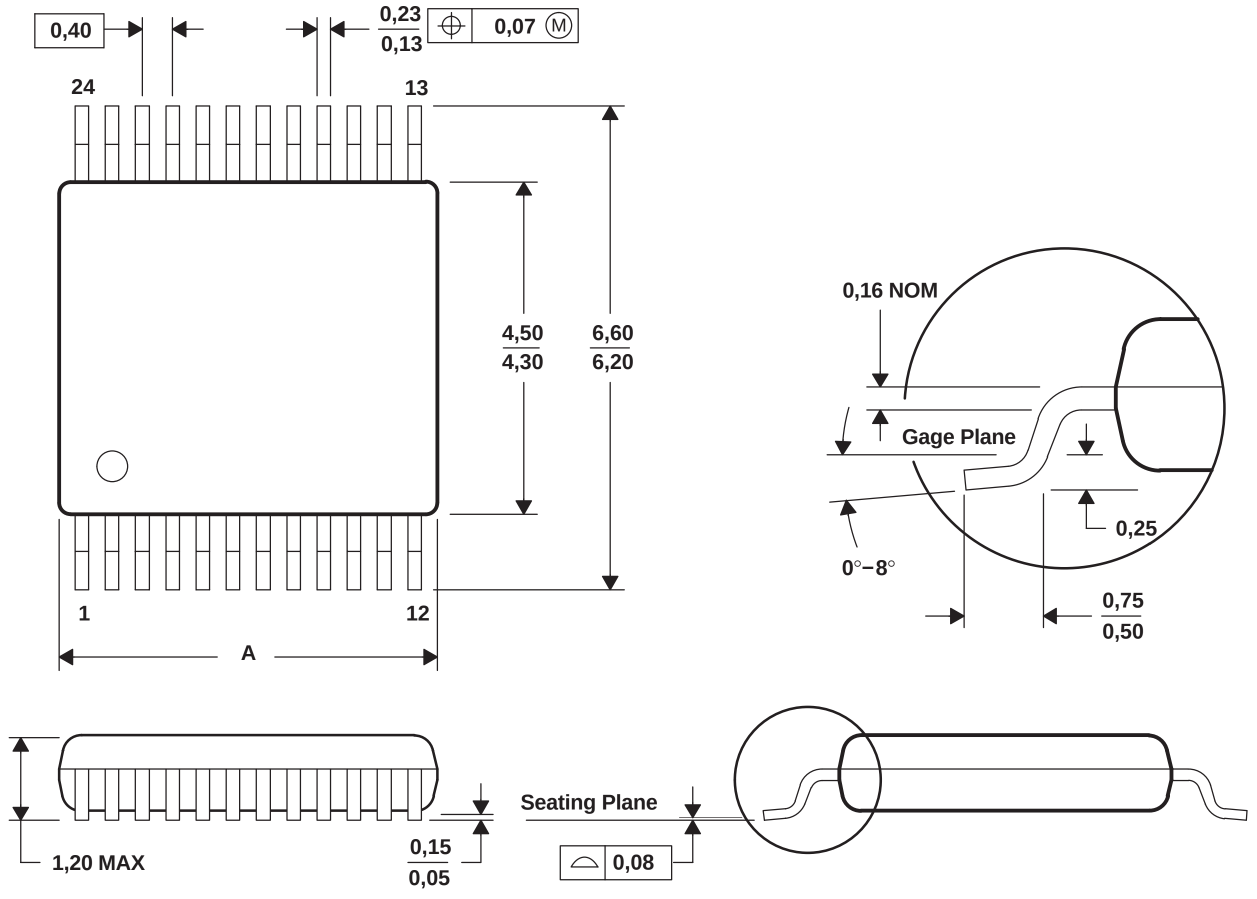
4040078/ F 12/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

Figure 14. Package Outline Diagram (DGG)

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

24 PINS SHOWN


0,40
0,23
0,13
0,07 Ⓜ
24
13
4,50
4,30
6,60
6,20
1
12
A
0,16 NOM
Gage Plane
0,25
0°−8°
0,75
0,50
1,20 MAX
0,15
0,05
Seating Plane
0,08

PINS ** / DIM	14	16	20	24	48	56
A MAX	3,70	3,70	5,10	5,10	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	9,60	11,20

4073251/C 08/98

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins − MO-153
  14/16/20/56 Pins − MO-194

Figure 15. Package Outline Diagram (DGV)

Applications

High-performance desktop computers and servers utilizing Intel Pentium II or Pentium III processors and the 440BX chipset require large amounts of memory support to run complex applications. Currently, with three double-sided DIMMs using 64-Mbit technology, a total memory size of 384 Mbyte is possible. To support 512 Mbytes, a fourth DIMM must be added. The 82443BX integrates a memory controller that supports a 64/72-bit DRAM interface and operates the interface at 66 MHz or 100 MHz, while supporting up to four double-sided DIMMs. To meet the tight 100-MHz timing requirements for a four-DIMM configuration, the CBT16292 bus switch is recommended.

The BX controller supplies two copies of memory address (MA) for effectively driving the address load and optimizing strict timing requirements placed on it by the 100-MHz address bus. The controller also supplies the FET-enable signal (FENA) to enable CBT switches. For the data bus to offset heavy loading to the data-in/data-out (DQ) line with the additional fourth DIMM, the CBT16292 (12-bit to 24-bit mux/demux with internal 500-Ω pulldown resistors) is recommended. This reduces the loading to the data bus. To the memory controller it looks like there are only two DIMMs instead of four. Figure 16 shows the application of the CBT16292. With error correction code (ECC), six devices are needed to buffer the 72-bit signals. This task also can be accomplished by using CBT162292, CBTLV16292, or CBTLV162292 devices.

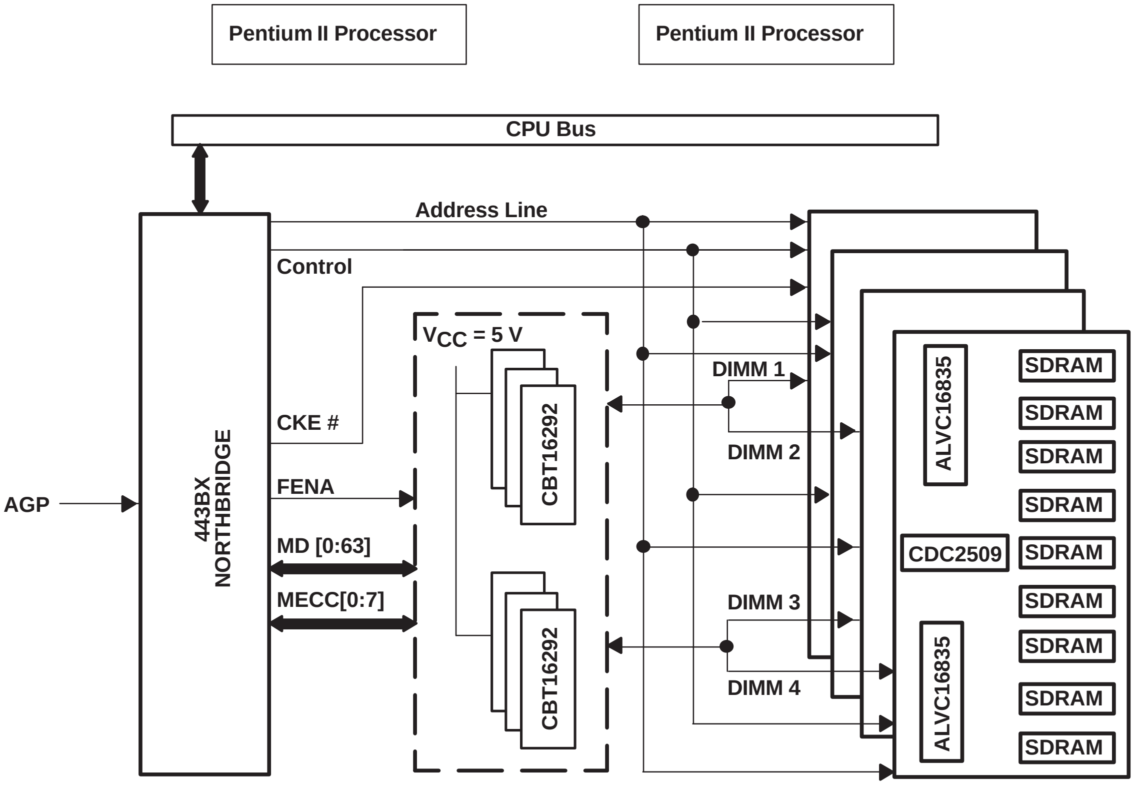

Pentium II Processor
Pentium II Processor
CPU Bus
Address Line
Control
CKE #
FENA
MD [0:63]
MECC[0:7]
AGP
443BX NORTHBRIDGE
V_{CC} = 5 V
CBT16292
CBT16292
DIMM 1
DIMM 2
DIMM 3
DIMM 4
ALVC16835
CDC2509
ALVC16835
SDRAM
SDRAM
SDRAM
SDRAM
SDRAM
SDRAM
SDRAM
SDRAM
SDRAM

Figure 16. CBT16292 in a Four-DIMM Memory-Switching Application

Figure 16 shows that the CBT16292 plays an integral part in the overall memory solution. Layout and routing should be taken into account. Determining the optimal line length depends on different simulation methods that can accommodate strict timing requirements of a 100-MHz bus. Figure 17 is an example of a typical motherboard layout integrating CBT16292 for four DIMMs. This layout also shows that, by using the CBT16292, the design is more effective because there can be equal load distribution, which can minimize skews.

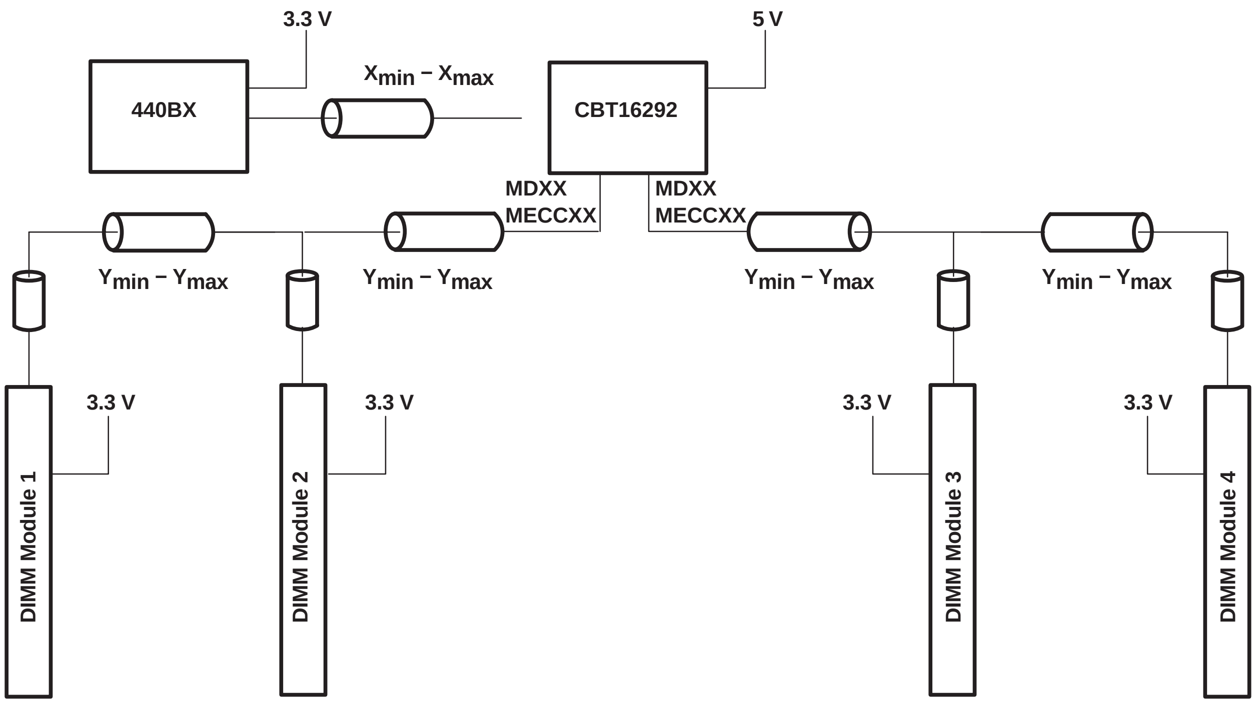

3.3 V
5 V
440BX
Xmin – Xmax
CBT16292
MDXX
MECCXX
MDXX
MECCXX
Ymin – Ymax
Ymin – Ymax
Ymin – Ymax
Ymin – Ymax
3.3 V
3.3 V
3.3 V
3.3 V
DIMM Module 1
DIMM Module 2
DIMM Module 3
DIMM Module 4

Figure 17. Typical Motherboard Layout Using CBT16292

To further optimize the layout and design shown in Figure 17, the CBTLV16292 and CBTLV162292 also are available. By using these 3.3-V FET-switch parts, all three parts of the memory solution are on the same power plane, and performance is not sacrificed.

Conclusion

TI’s CBT16292, CBT162292, CBTLV16292, and CBTLV162292 bus-switch solutions allow successful 100-MHz system integration. TI’s ’16292 solutions reduce loading, increase reliability, and ease overall timing when integrating the devices with Intel’s 440BX chipset.

Acknowledgment

The authors of this application report are Ji Park, Nadira Sultana, and Chris Cockrill.

Glossary

C

CBT	Crossbar technology
CMOS	Complementary metal-oxide semiconductor

D

DIMM	Dual in-line memory module
DRAM	Dynamic random-access memory
DQ	Data-in/data-out line

E

ECC	Error correction code

F

FET	Field-effect transistor
FENA	FET select signal

M

Mbyte	Megabyte
MA	Memory address

P

PC	Personal computer
pF	Picofarad

S

SDRAM	Synchronous dynamic random-access memory

T

TI	Texas Instruments
t_{en}	Enable time
t_{dis}	Disable time
TSSOP	Thin shrink small-outline package
TVSOP	Thin very small-outline package

V

V_{OLP}	Output low peak voltage
V_{OLV}	Output low valley voltage
V_{OHV}	Output high valley voltage
V_{OHP}	Output high peak voltage

Application Report
SCDA007 - APRIL 2000

Texas Instruments Solution for Undershoot Protection for Bus Switches

Nadira Sultana and Chris Graves
Standard Linear & Logic

ABSTRACT

Three solutions for undershoot protection (Schottky diode, charge pump, and active clamp) are discussed. Their advantages and disadvantages are presented, as well as a comparison of significant characteristics of each solution. Laboratory test data confirm the superior performance of the TI device with the active-clamp undershoot-protection feature.

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Introduction

The TI™ CBT/CBTLV bus-switch family has become an indispensable solution in high-performance personal-computer (PC), data-communications, and consumer applications. In some applications, due to various system design techniques, undershoot events occur. This undershoot forces the switch on, intermittently, over a short time interval. When a bus switch is disabled, an input undershoot that exceeds its threshold voltage V_T can turn on the pass transistor. This unwanted condition causes severe data errors on the outputs.

TI has a new, active-clamp undershoot-protection feature in the bus-switch family, designated K, i.e., CBTK. This application report discusses various options for undershoot protection, including their advantages and disadvantages. Laboratory test results demonstrate the superior performance of the new CBTK devices with the undershoot-protection feature.

Background

What Happens to the Bus Switches When Undershoot Occurs

The bus switch consists of a large, but simple, NMOS transistor that passes data. Figure 1 illustrates a simple bus switch. The gate of the NMOS transistor is controlled by an enable signal. When the gate voltage is low, the switch is off.

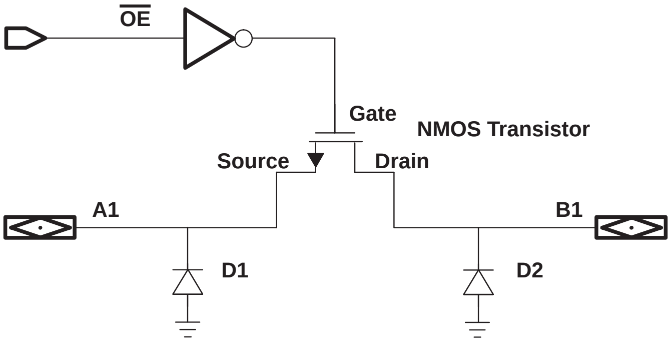

Figure 1. Basic NMOS-Transistor Bus Switch

When the gate voltage is high, the switch is on. The threshold voltage V_T of an NMOS transistor is approximately +650 mV. When V_{GS} (gate-source voltage, $V_G – V_S$) is greater than V_T, the switch is turned on. In the enabled state, undershoot is not a problem. But, when the switch is disabled, a negative voltage on the bus could turn on the switch, causing a data error.

Two different situations can exist when undershoot occurs. The first situation occurs when the source node voltage (V_S) becomes lower than the gate voltage (V_G). Any undershoot on the source node (V_S) greater than or equal to +650 mV creates a positive V_{GS}, which is greater than V_T. This turns on the switch, and the two buses are no longer isolated. Corruption of data is inevitable.

TI is a trademark of Texas Instruments.

In the second situation, a parasitic npn transistor is formed in the NMOS transistor during manufacturing. Figure 2 shows the cross-sectional view of an NMOS transistor. The emitter is the n^+ source/drain implant, the base is the p-type substrate, and the collector is the n^+ source/drain implant. When undershoot below ground occurs on the source node, because the substrate is at 0 V, a positive V_{be} is created on the parasitic npn transistor and causes the transistor to conduct. With β of approximately 10, a small amount of base current generates enough collector current to establish a continuous flow from collector to emitter, i.e., from drain to source. So the switch is on again, instead of being off, creating a major data error.

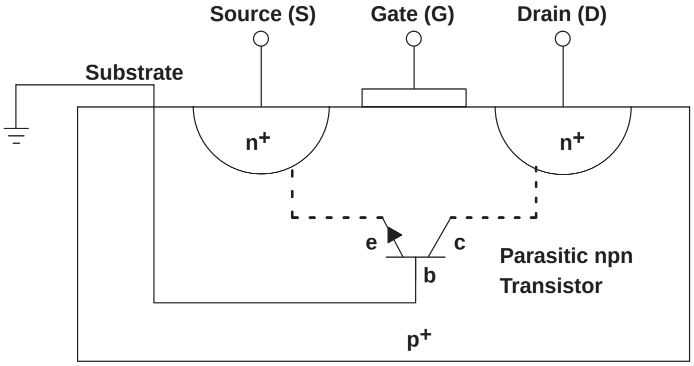

Figure 2. Cross-Sectional View of an NMOS Transistor

Undershoot Event Cases

Termination is an important consideration in signal integrity. Usually, undershoot occurs when a bus is not terminated or is poorly terminated. Signals with very fast edge rates also can degrade signal quality by generating undershoots. Good transmission-line designs can resolve these issues, but some systems, such as a PCI bus, are designed to have a reflected wave. To achieve very high speed using low power, the PCI bus is not terminated. Reflections are not eliminated, by design, but reflections are expected. These reflections can cause severe undershoot conditions that force the bus switch to function improperly.

Techniques for Undershoot Protection

Three main techniques provide undershoot protection: Schottky-diode solution (CBTS), charge-pump solution (none), and active-clamp solution (CBTK). TI, as a world leader in bus-switch technology, designed the CBTK devices to solve undershoot problems. This active clamp feature offers excellent protection against high-current undershoot events. The comparisons in the following paragraphs prove CBTK to be the best solution for undershoot protection.

Schottky-Diode Solution

Figure 3 shows the basic NMOS crossbar switch with Schottky diodes. The n-channel pass-transistor source and drain are connected to two different buses. The gate of the pass transistor is controlled by the $\overline{\text{OE}}$ signal that is generated from the output-enable circuit. When the gate voltage is high, the switch is closed. When the gate voltage is low, the switch is open. The undershoot event does not affect performance of the switch when the switch is on. But, if undershoots occur when the bus switch is off, passing unwanted data can cause a data error. To prevent this, two Schottky diodes are connected from the source and drain to ground. When one of the buses has negative voltage that exceeds the forward turnon voltage of the Schottky diode, the diode turns on and clamps the source or drain voltage of the NMOS switch, keeping the buses isolated.

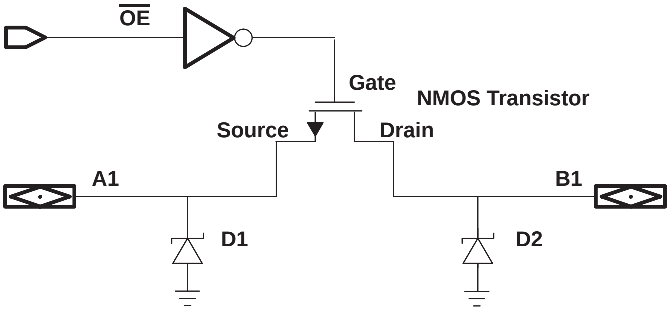

Figure 3. Basic NMOS Switch With Schottky-Diode Clamps

A Schottky diode clamp has the following advantages and disadvantages:

- Advantages
  - Low power requirement
  - Some undershoot protection
  - Bidirectional, both ports protected
- Disadvantages
  - Slow to react to undershoot voltages with fast edge rates. This could cause the n-channel pass transistor to turn on and affect the buses.
  - No effect on the parasitic npn transistor. Because the parasitic transistor’s base is the substrate that is at ground, the undershoot turns on the transistor and a large current corrupts the data.
  - Significant addition of input/output capacitance

Charge-Pump Solution

In this implementation, a charge pump with a negative voltage controls the substrate voltage and the gate voltage of the transistor. During an undershoot event, the charge pump keeps the gate voltage and the substrate voltage negative, so both of them are off.

The advantages and disadvantages of the charge pump are:

- Advantages
  - Excellent undershoot protection
  - Lower input/output capacitance
  - Low I_{off}
  - Bidirectional, both ports protected
- Disadvantages
  - Significantly high I_{CC}
  - Higher cost due to chip size increase for the charge-pump circuit

Active-Clamp Solution

This technology integrates an active-clamp undershoot-protection circuit on both ports. In the active-clamp circuit, a bias generator sets a voltage slightly above ground, which allows the active-clamp pullup voltage to turn on during an undershoot event. This clamp counteracts the undershoot voltage and limits V_{GS}, V_{GD} of the n-channel, and V_{be} of the parasitic npn transistor. Figure 4 shows the basic NMOS switch with active-clamp pullup circuits.

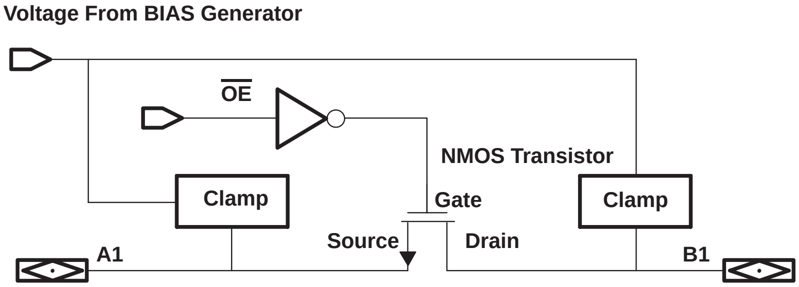

Figure 4. Basic NMOS Switch With Active-Clamp Pullup Circuits

Advantages and one disadvantage of the active-clamp solution are:

- Advantages
  - Excellent undershoot protection
  - Capacitance is low. Minimal capacitance is added.
  - Overvoltage-tolerant I/Os
  - Faster enable/disable switching speed than the Schottky solution
  - Less power required
  - Low I_{off}
  - Both ports protected
- Disadvantage
  - Chip-size increased

Table 1 provides a comparison of significant characteristics of these three undershoot-protection technologies. Different techniques of undershoot protection provide varying degrees of protection with different tradeoffs.

The comparison in Table 1 indicates that the Schottky-diode solution handles only minimal-undershoot events.

The charge-pump solution provides excellent undershoot protection, but has high I_{CC} and high power consumption. Therefore, it is not ideal for mobile and power-consumption-sensitive applications.

The active-clamp solution provides excellent undershoot protection and consumes less power. Moreover, it is overvoltage tolerant, which allows compatible operation in mixed-voltage systems.

Table 1. Comparisons of Undershoot-Protection Technologies

CHARACTERISTICS	SCHOTTKY DIODE (CBTS)	CHARGE PUMP	ACTIVE CLAMP (CBTK)
Undershoot protection	Good. Protection on both ports slows to react with fast edge rates. No effect on parasitic transistor.	Excellent protection on both ports	Excellent protection on both ports
I_{CC}	Low (≤10 µA)	Very high (>100 µA)	Low (≤20 µA)
Capacitance	High (9 pF)	Low (5 pF)	Low (5 pF)
I_{off}	No I_{off} specification	Low (10 µA)	Low (10 µA)
Overvoltage tolerance	No	No	Yes

Laboratory Comparison of Various Device Options

Laboratory testing demonstrated the excellent undershoot-handling capability of the active-clamp circuit (CBTK). Figure 5 shows the test setup. Three devices (CBT6800, CBTS6800, and CBTK6800) were tested with one output switching. A valid high logic level is established on port B by charging a load capacitor on port B to 5.5 V. The bus switch was disabled and an input with an undershoot of −2 V and 20-ns pulse duration was applied. The output of each device was recorded. The standard CBT6800 device turned on as soon as the undershoot event occurred and the capacitor discharged. The Schottky-diode version (CBTS6800) turned on slowly and discharged the capacitor. In contrast, the CBTK effectively clamped the undershoot and maintained excellent signal integrity on port B.

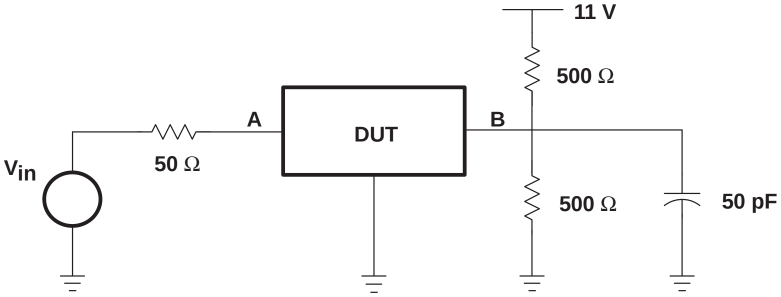

Figure 5. Test Setup for the Undershoot Test

Figure 6 shows the output waveforms from the test. The active-clamp solution performance is much superior compared to the standard product without the clamping feature. The CBTS offers minimal protection. TI provides bus switches with Schottky diodes (CBTS) and active-clamp undershoot-protection (CBTK) features.

Due to an undesirably high $I_{CC,}$ the charge-pump solution is not offered by TI.

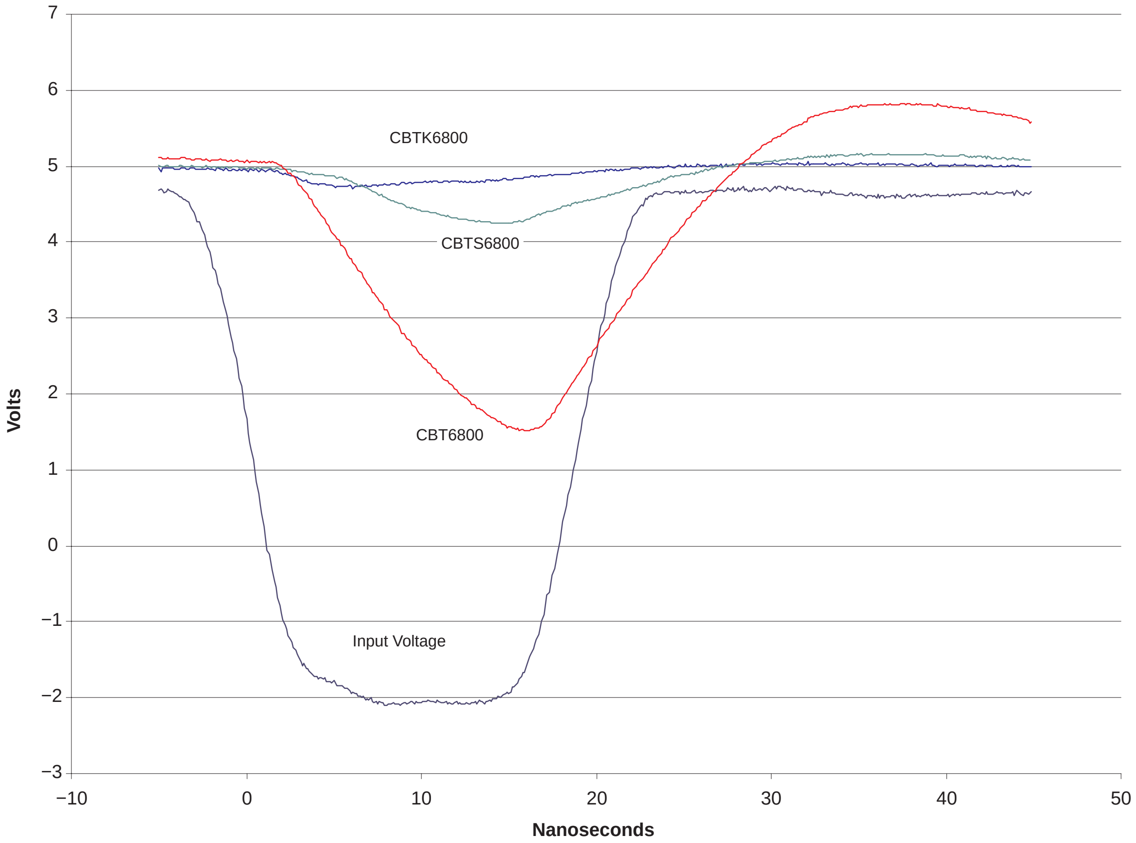

Figure 6. Output Waveforms During Testing of Undershoot Protection of Different Crossbar-Switch Solutions

Conclusion

Systems migrating to lower voltages and improved speeds require bus switches that can prevent unwanted undershoots. Good design techniques can solve problems associated with transmission lines, but systems with an intentionally reflected wave have undershoots.

The TI active-clamp solution provides excellent undershoot protection, while consuming less power, a desirable feature in today’s power-hungry applications. Combined with low power consumption and overvoltage tolerance, the CBTK device is the ultimate solution for undershoot events. TI, as a leading supplier of bus switches, offers innovative functions from multiplexers to simple FET switches in a variety of bit widths. The active-clamp feature, implemented across the majority of functions in 5-V and 3.3-V devices, provides greater flexibility in designing systems.

Glossary

β (beta)	(I_c/I_b) Gain factor of a bipolar junction transistor
CBT	Crossbar technology
CBTLV	Low-voltage crossbar technology
CBTK	Crossbar technology with active-clamp undershoot protection
CBTS	Crossbar technology with Schottky-diode undershoot protection
I_{CC}	Supply current
I_{off}	Input/output power-off leakage current
NMOS	N-channel metal-oxide semiconductor
PC	Personal computer
V_{be}	Difference between base voltage and emitter voltage
V_G	Gate voltage
V_S	Source voltage
V_{GS}	Difference between gate voltage and source voltage
V_{GD}	Difference between gate voltage and drain voltage
V_T	Threshold voltage

TEXAS INSTRUMENTS

Application Report
SCLA015 - February 2001

Bus-Hold Circuit

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Standard Linear & Logic

ABSTRACT

When designing systems that include CMOS devices, designers must pay special attention to the operating condition in which all of the bus drivers are in an inactive, high-impedance condition (3-state). Unless special measures are taken, this condition can lead to undefined levels and, thus, to a significant increase in the device's power dissipation. In extreme cases, this leads to oscillation of the affected components, which has a negative effect on both the reliability − in terms of both functioning and lifetime − and the electromagnetic compatibility of the entire system. This application report addresses a range of circuit design features that minimize these problems. The main purpose of this application report is to present a novel bus-hold circuit that TI™ has integrated into a wide range of modern bus-interface devices. This bus-hold circuit is the ideal way of meeting the demands discussed here, thus helping to ensure the functional reliability of a system.

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1 Introduction

In recent years, CMOS technology has become the technology of choice for development and subsequent production of highly integrated (VLSI) circuits because of the high complexity and low power consumption that can be achieved with these types of circuits. Also, the technology has proved itself with less complex devices, such as the SN74AHC and SN74AC logic families, as well as with the SN74LVC and SN74ALVC logic families developed for use with lower supply voltages. Furthermore, it is possible for important parameters, such as propagation delay time and drive capability, to achieve properties similar to those found in the bipolar circuits that previously dominated this field. In this respect, the particularly powerful SN74ABT and SN74LVT BiCMOS devices, which combine the strengths of CMOS circuits (low power consumption) with those of bipolar circuits (lower propagation delay time and greater drive capability), deserve mention.

When using these integrated CMOS and BiCMOS devices, the designer also must consider certain properties of these devices that the specification sheets deal with only briefly, if at all. This includes, for example, the behavior of the input stages of these components when no defined logic level is established.

2 Behavior of CMOS Input Stages

The input stage of a CMOS circuit consists of an inverter (see Figure 1) that decouples the following internal circuit from the external signal source. Due to the high degree of voltage amplification, this stage regenerates the voltage swing and the rise time of the incoming signal.

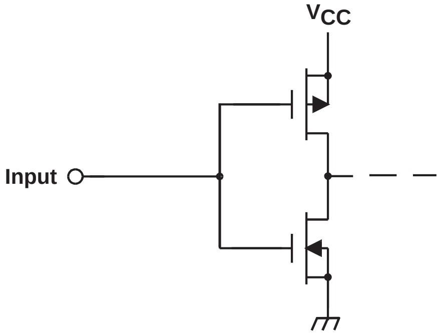

Figure 1. Input Stage of a CMOS Circuit

If there is a valid logic level at the input − the gates of the MOS transistors − of such a circuit, the P-channel transistor conducts if the input is a low level, and the N-channel transistor conducts if the input is a high level. In either case, the complementary transistor is turned off, so that, in both cases, no current flows through the transistors. This is the reason for the low power consumption when CMOS circuits are at rest.

If, on the other hand, an input voltage between these defined logic levels ($V_t < V_i < V_{CC} - V_t$; with V_t = threshold voltage of the transistors) is applied to such an input, both transistors are more or less conducting, leading to an increase in the device’s supply current. Figure 2 shows the supply current in relation to the input voltage for AHC and AC devices. In AHC devices, the supply current reaches a peak value of I_{CC} = 2 mA, while in the faster AC devices, currents of about 5 mA can be expected. Accordingly, the device’s power consumption also increases, so that, with undefined logic levels, the advantages of CMOS circuit technology are not realized.

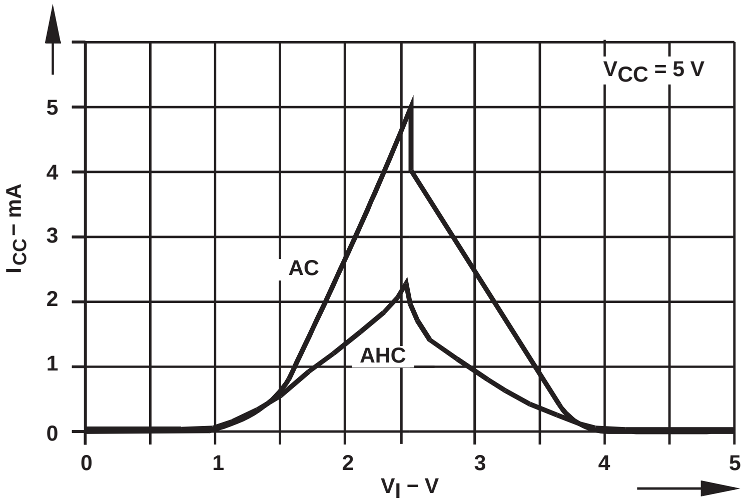

Figure 2. Power Consumption of CMOS Input Stages vs Input Voltage

The effects shown in Figure 2 are typical of all CMOS circuits. Accordingly, this phenomenon also must be taken into account when dealing with VLSI circuits, such as microprocessors or memory devices.

Furthermore, CMOS device data sheets recommend the slowest possible rise time for the input signal to ensure optimum functioning of components. However, slowly rising edges cause fast integrated circuits to malfunction and can, in extreme cases, lead to destruction of the circuit. Figure 3 shows an inverting buffer stage with the parasitic inductances of the package leads (L_P) and the capacitive load (C_L) at the output. If, for example, the input voltage of this kind of circuit rises from low to high, and reaches the threshold voltage, the output switches abruptly from high to low due to the high voltage gain, and discharges C_L. The discharge current causes a voltage drop at the package inductance of the ground terminal, which raises the internal ground potential of the integrated circuit, meaning that the voltage difference between the input and the internal ground potential decreases, giving the appearance of a decrease of the input voltage. If, due to too slow a slew rate, in the meantime, the input voltage has not risen sufficiently, the input stage switches to the opposite state, and the same process repeats, but with the opposite polarity. This process repeats periodically, with the periodicity of the oscillation determined by the device’s propagation delay time. In fast logic circuits, the oscillation is above 50 MHz.

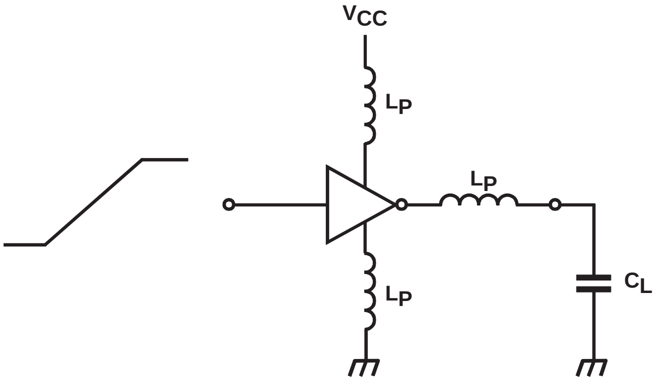

Figure 3. Parasitic Components Causing Circuit Oscillation

Figure 4 shows the oscillation at the output of a CMOS circuit whose input is triggered by a signal with a rise time of t_r = 200 µs. Rise and fall times of this order must be taken into account if, for the operating conditions discussed below, special circuit design techniques are not incorporated to ensure defined signal levels and slew rates.

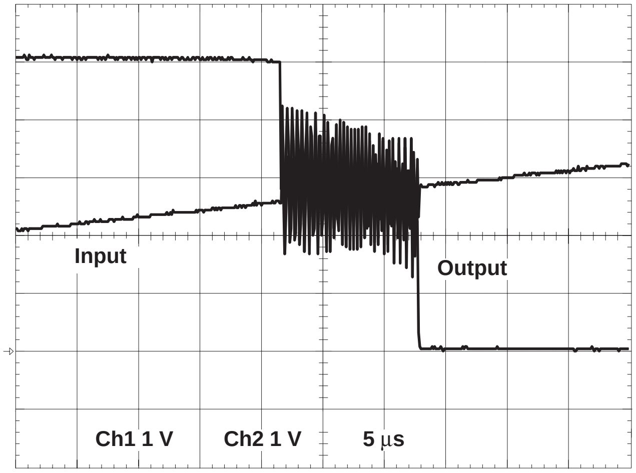

Figure 4. Oscillation at the Output of a CMOS Circuit Whose Input Is Triggered by a Signal With a Rise Time of t_r = 200 ns

In addition to a significant increase in system noise, which compromises the system's electromagnetic compatibility, the circuit's power dissipation rises unacceptably. In MOS circuits, the fact that the transistor's resistance increases as the temperature rises becomes an advantage because this often avoids overloading the circuit. In contrast, with bipolar devices the transistor's current gain increases as the temperature rises. This also applies to BiCMOS devices, such as the SN74ABT and SN74LVT series. Because there are no factors that would reduce power dissipation, these circuits often are overloaded when they oscillate. Experience shows that permanent degradation of devices can be expected if the oscillation lasts for several seconds.

3 Problems Posed by Bus Systems

If only unidirectional transmission lines are involved, the previously mentioned phenomenon of increased power dissipation and oscillation can safely be ignored. With unidirectional transmission lines there is a driver circuit that always is active at one end of the line, thus ensuring defined logic levels (see Figure 5).

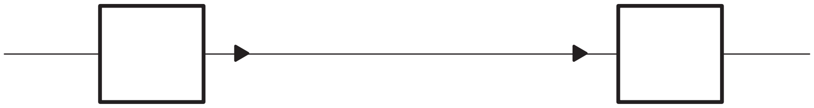

Figure 5. Unidirectional Transmission Line

Bus systems (see Figure 6), in which transmission is bidirectional between individual stations, the operating condition in which all of the 3-state output bus drivers are in an inactive, high-impedance state in a 3-state device must be given special attention. Because there is no driver to impose a defined logic level on the lines, a voltage develops that is determined by the leakage currents of the connected components, thus giving rise to an entirely undefined voltage level. In the literature, this state is described as floating inputs. In the case of Widebus™ circuits with 16 channels and AC technology, with a supply voltage of V_{CC} = 5 V, the supply current rises to $I_{CC} = 16 \times 5$ mA = 80 mA (see Figure 2). Under this condition, the power consumption of this component alone increases to 400 mW, which no longer is low power consumption.

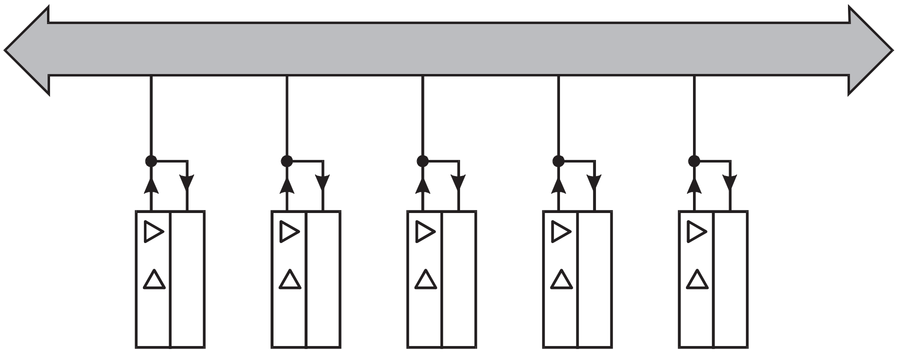

Figure 6. Bidirectional Transmission Line of a Bus System

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4 Avoidance of Undefined Levels in Bus Systems

4.1 Avoidance of Undefined Levels Via Appropriate Bus Control

A simple way to prevent an undefined logic level in bus systems is to ensure, via appropriate control of the bus, that the duration of the inactive state (3-state) is so short that harmful voltages cannot build up. The advantage of this method is that it does not involve any additional costs from using special components.

If we first consider a single device and assume that the maximum leakage current, I_{OZ}, of a 3-state output in the high-impedance state amounts to 10 µA (see Table 1), and that the input and output capacitance, C_S, of the integrated circuit plus the parasitic capacitance of the connection lines (which are related to this particular component) amount to about 20 pF, the voltage on an inactive line drifts away from the defined logic level at a rate that can be calculated using equation 1.

$$\frac{dV}{dt} = \frac{I_{OZ}}{C_S} = \frac{10\ \mu A}{20\ pF} = 0.5\ V/\mu s \qquad (1)$$

If a drift away from the logic level of a maximum of 1 V is permitted, so that the supply current of the affected input stage has not yet risen too sharply (see Figure 2), the bus may remain in an inactive state (3-state) for a maximum of 2 µs. Usually, more than one device is connected to a bus. Where several components are connected to a bus, both their leakage currents and their capacitances are added, and the time constant calculated in equation 1 does not change.

In the data sheets, semiconductor manufacturers give conservative values for the leakage current, I_{OZ}. When determining these values, the leakage current is measured at an ambient temperature of $T_A = 25°C$ and the maximum values to be expected at operating limits are then calculated. However, semiconductor physics predicts a doubling of the leakage current when T_A rises 10°C. Thus, if T_A rises from 25°C to 125°C, the leakage current would rise by a factor of $2^{10} = 1024$. However, this fundamentally correct assumption leads to considerably higher values than are measured in practice. Accordingly, one can assume that typical output leakage currents are smaller than the specification sheet limits by an order of magnitude, or more.

Another method of avoiding undefined logic levels in inactive buses involves the last active bus-interface device remaining active (monitored by suitable control logic) until another bus driver takes over control of the line. The PCI bus uses this method, whereby inactive bus phases of any length can be bridged without the extra cost of adding components.

4.2 Pullup Resistors

Another way of ensuring a defined level during a bus's inactive phase is by tying the lines to the supply voltage or to the ground potential via resistors (R_p in Figure 7). This connection pulls inactive lines to a defined logic level (either high or low).

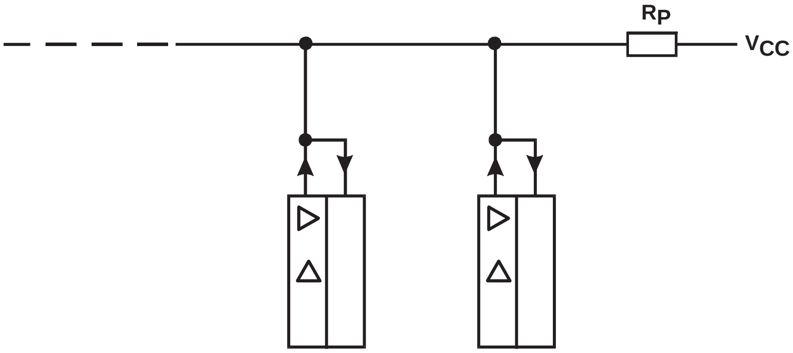


Figure 7. Creating a Defined Level Using Pullup Resistors

Getting the correct impedance for the resistors is not always easy. The resistors should not significantly increase the system's power dissipation; therefore, high-impedance resistors are required (R_p = 10 kΩ to 50 kΩ). The low leakage current of CMOS circuits would permit that. However, it also should be remembered that fast logic circuits need short rise times, t_r, at the inputs to avoid unwanted oscillation which, as mentioned previously, can lead to system malfunction and, possibly, degradation of components. The desired pullup or pulldown resistance, R_p, can be calculated using equation 2:

$$R_p = \frac{t_r}{2.2 \times C_S \times n} \tag{2}$$

Where:

n = number of devices connected to the line

Modern logic circuits and corresponding VLSI circuits demand input signals whose slew rate is $\Delta t/\Delta V < 10$ ns/V. In the case of a supply voltage of $V_{CC} = 5$ V, that corresponds to a signal rise or fall time of $t_{r/f} \approx 50$ ns. Assuming that ten devices, each with a capacitance of $C_S = 20$ pF per component, are connected to the bus, and that the devices require a maximum rise time $t_r = 50$ ns, resistance R_p can be calculated using equation 3.

$$R_p = \frac{50\ \text{ns}}{2.2 \times 20\ \text{pF} \times 10} \approx 110\ \Omega \tag{3}$$

When using modern bus-interface circuits whose advantage is their low quiescent current consumption, this outcome is unacceptable. These resistors consume far more current than the logic circuit itself. After all, many logic circuits are not capable of providing the output current needed for such a low-impedance load.

4.3 Bus-Hold Circuit

A considerably more elegant solution is to ensure a defined level for inactive bus lines via bus-hold circuits (see Figure 8). These circuits feed back the output signal of a noninverting buffer circuit to the input via the resistor R_f. This creates a bistable circuit (latch). To understand the circuit, one first assumes that an active bus driver has switched the line to high level. This means that a high level also exists at the output of the bus-hold circuit buffer. Thus, no current flows via the feedback resistor R_f. The leakage currents of the circuit, which are in the microampere region, determine power consumption of the bus-hold circuit. If the output of the bus driver in question changes to the inactive state, the bus-hold circuit holds the high level via the feedback resistor R_f, so that now, apart from leakage currents, no current flows. Only during the transition of the line from high to low, or vice versa, time current spikes, which are unavoidable in CMOS circuits, occur in the bus-hold circuits. However, the dynamic power dissipation involved is several orders of magnitude less than when using pullup resistors described previously.

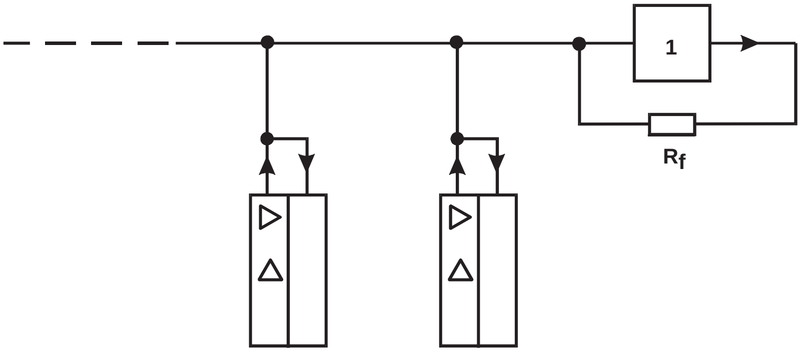


Figure 8. Bus With Bus-Hold Circuit

This kind of circuit can be built simply by using a noninverting buffer circuit, such as the SN74AHCT541, if, as noted previously, the outputs are fed back to the inputs via resistors R_f. The propagation delay time of these components is, in this case, of secondary importance. Whether the CMOS-compatible version (SN74AHC541) or the TTL-compatible version (SN74AHCT541) is used depends on the switching thresholds of the bus-interface device. The impedance of the feedback resistor R_f is decided, taking into account the fact that the voltage drop V_r at the resistor still ensures a sufficient logic level, even at the maximum leakage current I_{OZ} to be expected from the connected devices. Here the number of bus drivers (n) connected to the bus obviously plays a part. In making the calculation it is assumed that, due to its low load, the output voltage of the buffer circuit used in the bus-hold circuit corresponds to the potential of the supply lines (V_{CC} or GND). Thus,

$$R_f \le \frac{V_r}{I_{OZ} \times n} \tag{4}$$

If we assume that ten bus drivers are connected to the bus line and that the output leakage current of the bus drivers is I_{OZ} = 10 µA, and, if we allow a voltage drop of V_r = 1 V at the feedback resistor R_f, the resistance R_f is:

$$R_f \le \frac{1\ \text{V}}{10\ \mu\text{A} \times 10} = 10\ \text{k}\Omega \tag{5}$$

Because with this circuit technique no charging of line capacitance is required, rather only the most recent logic level is held, problems relating to signal rise times no longer are expected. Accordingly, the circuit can be designed with considerably higher impedance, and correspondingly lower power consumption, than with the technology described in paragraph 4.2.

5 Integrated Bus-Hold Circuit

For the reasons given in the previous section, a defined logic level must be ensured on bus lines in the high-impedance state. Thus, it makes sense to integrate bus-hold circuits in the inputs of bus-interface devices. Doing so means designers no longer have to concern themselves with the problem, and additional components are not needed to ensure defined logic levels under all operating conditions, markedly improving the reliability of the whole system.

Inputs of all newly developed bus-interface devices have a bus-hold circuit. The additional letter H in the type designation indicates this feature. An ABT device has no bus-hold circuit, while an ABTH device has the additional bus-hold function. The same applies to LVT and LVC circuits versus ALVTH, LVTH, LVCH, and ALVCH circuits.

The additional cost of the bus-hold function in bus-interface devices is not excessive. Figure 9 shows the simplified input circuit found in the modern CMOS and BiCMOS families. The input signal is amplified in the Q1/Q2 inverter. Simultaneously, this stage decouples the following internal circuit from the exterior of the device. The actual bus-hold circuit consists of transistors Q3 and Q4. The signal, after again being inverted, thus going through 360 degrees total, then returns to the circuit's input. From the resulting feedback the two inverters create a latch that continually tries to reach one of its two stable states − high or low. If there is a high level at the circuit input, the output of the second inverter also is high. Therefore, P-channel transistor Q3 conducts. If the input voltage of the integrated circuit drops for any reason, a current is supplied via this transistor, which counteracts any further drop of the line voltage. If, conversely, there is a low level at the circuit input, N-channel transistor Q4 conducts and compensates for the leakage current of the interface devices connected to the bus.

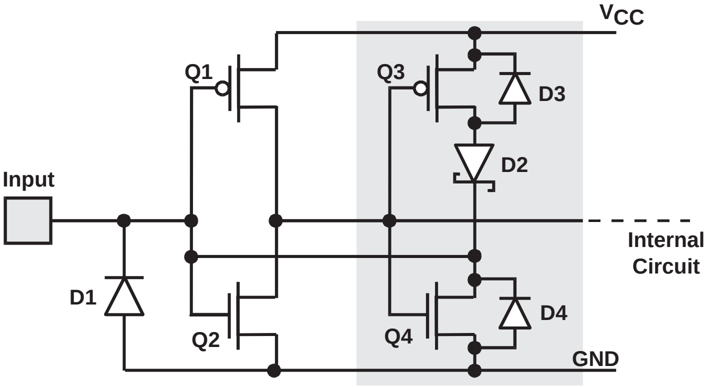


Figure 9. Simplified Circuit Diagram of Bus-Hold Circuits

Transistors Q3 and Q4 in the bus-hold circuit compensate for both their own leakage currents and for those of the connected circuits. Otherwise, they should load the circuit as little as possible, and because of this, these transistors have a comparatively high forward resistance in the on state. (R_{dson} = 5 kΩ). Figure 10 shows the input characteristics of typical bus-interface devices with the bus-hold function.

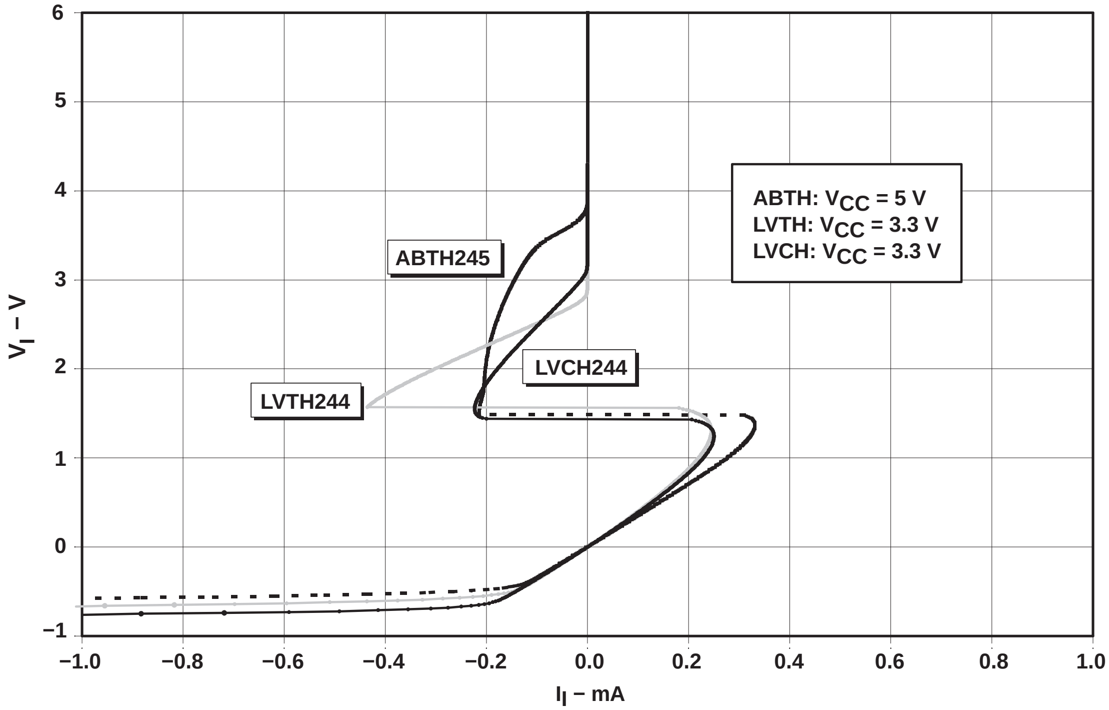


Figure 10. Characteristic Input Curve of Bus-Interface Devices With the Bus-Hold Function

The switching threshold of bus-hold circuits is about 1.5 V in the devices depicted in Figure 10, matching the switching threshold of the appropriate logic circuits. If the input voltage is below this level, N-channel transistor Q4 conducts ($R_{dsontyp}$ = 5 kΩ). This transistor also remains conducting, even when the input voltage falls below 0 V. If the input voltage drops below −0.7 V, clamping diode D1 conducts, which protects the circuit against destruction due to electrostatic discharge and limits negative undershoot stemming from line reflection. Above the cited threshold voltage, P-channel transistor Q3 conducts, pulling the line level to the high potential. Diode D2 in Figure 9 prevents the parasitic diode D3 parallel to transistor Q3 from conducting if the input voltage has a higher positive value than the supply voltage. This last case might occur, for example, when signals with a voltage swing of 5 V control the bus-hold circuit, which is itself operated by a supply voltage of V_{CC} = 3.3 V. This also ensures that the bus-hold circuit remains at the high-impedance state with the supply voltage off. The upper diagram shows the influence of this diode in that the bus-hold circuit already becomes high impedance at markedly less than 3.3 V. In the case of ABTH devices, whose typical high level also is about 3 V despite a supply voltage of 5 V, it would not make sense for the bus-hold circuit to pull the potential significantly above this level. Accordingly, as Figure 10 shows, additional circuit features limit the rise in voltage.

6 Application Information

6.1 Additional Load Caused by Bus-Hold Circuits

The influence of, and the additional load caused by, the bus-hold circuits can be investigated using the example in Figure 11. In this example, a digital signal processor (TMS320C6xx), eight bus-interface devices (SN74LVCH245) with the bus-hold function, and one bus-interface device (SN74AHC245) without the bus-hold function are connected to a system bus. Semiconductor manufacturers still supply devices with 3-state outputs, but without the bus-hold function under discussion. These include, among others, microprocessors, such as digital signal processor TMS320C6xx, or integrated circuit SN74AHC245 used in this example. This leads, in some applications, to a combination of different types of logic circuits. The example illustrated here exemplifies bus systems where circuits with and without the bus-hold function are combined with each other.

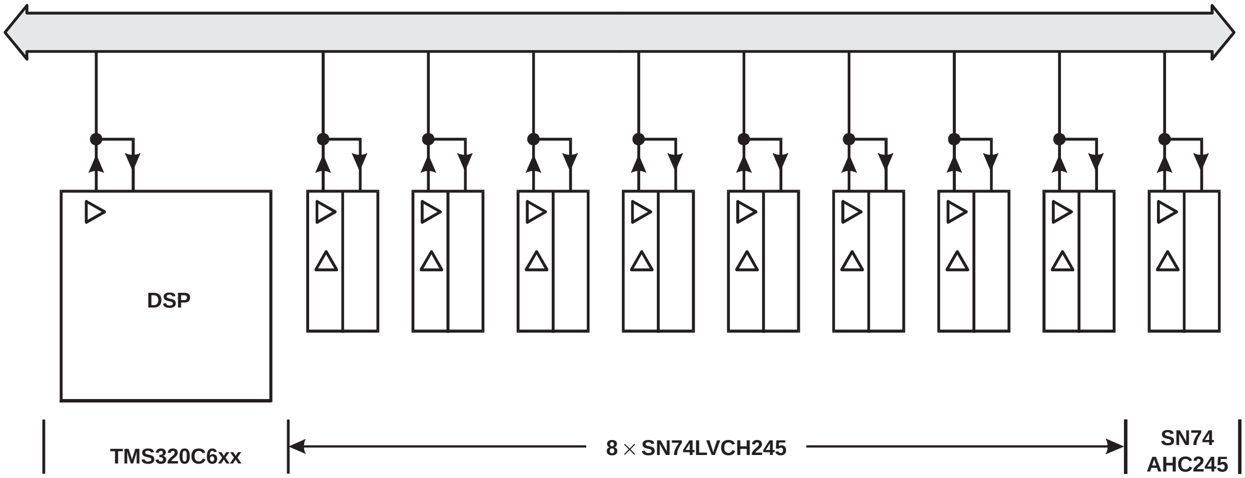


Figure 11. A Simple Bus System

In the data sheets for the SN74LVCH245 and SN74AHC245 devices, and for the digital signal processor TMS320C6201, details of the inputs and outputs are given in Tables 1, 2, and 3.

Table 1. Specifications of the 3-State Outputs With Bus Hold, SN74LVCH245

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	I_{OH} = 12 mA	3 V	2.4		V
V_{OL}	I_{OL} = 12 mA	3 V		0.4	V
$I_{I(hold)}$	V_I = 0.8 V	3 V	75		µA
	V_I = 2 V	3 V	−75		µA
	V_I = 0 to 3.6 V	3.6 V		500	µA

Table 2. Specifications of the 3-State Outputs, SN74AHC245

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	I_{OH} = 4 mA	3 V	2.48		V
V_{OL}	I_{OL} = 4 mA	3 V		0.44	V
I_{OZ}	V_O = V_{CC} or GND	5.5 V		2.5	µA

Table 3. Specifications of the 3-State Outputs, TMS320C6201

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	I_{OH} = 12 mA	3.14 V	2.4		V
V_{OL}	I_{OL} = 12 mA	3.14 V		0.4	V
I_{OZ}	V_O = 0 V or D_{VDD}	3.46 V		10	µA

With respect to sufficient logic levels (V_{IL} < 0.8 V, V_{IH} > 2.0 V), the bus-hold circuit in the SN74LVCH245 device supplies a current of $I_{I(hold)}$ > |75 µA|. Assuming a maximum leakage current of I_{OZmax} = 10 µA for 3-state outputs, a single bus-hold device would almost be capable on its own to compensate the leakage currents of the other nine devices connected to the bus and ensure defined levels on the bus lines. This is all the more so that, in practice, as noted above, none of the integrated circuits show the maximum output leakage currents I_{OZ} given in the data sheets. Due to the large variation of the transistor parameters caused by production variations and changes in supply voltage and temperature, the maximum current $I_{I(hold)}$ might rise to 500 µA (see Figure 10). In the example shown here, a single active output also must be able to charge/discharge the device's capacitance and to switch eight inputs with bus hold. The outputs of the LVCH and AHC devices, and the processor, can supply a current of $8 \times I_{I(hold)max}$ = 4 mA (see Tables 1, 2, and 3).

6.2 Influence on the Circuit's Power Loss

When using bus-hold circuits, a current, $I_{I(hold)}$, flows during signal state transition from low to high and from high to low for the duration of the signal slope, which has an influence on the system's power consumption. The resultant power dissipation can be calculated approximately.

According to Table 1, the maximum current in bus-interface device SN74LVCH245 is $I_{I(hold)max}$ = 500 µA at V_{CCmax} = 3.6 V. Because the current during a signal transition follows a roughly triangular shape, we can derive the power consumption, P_{hold}, caused during signal transitions by the bus-hold circuits:

$$P_{hold} = \frac{1}{2} \times V_{CC} \times I_{I(hold)max} \times t_r \times 2 \times f \times n \qquad (6)$$

Where:

t_r = signal rise or fall time
f = frequency of signal exchange
n = number of inputs with a bus-hold circuit
$I_{I(hold)max}$ = maximum bus-hold circuit input current

For the SN74LVCH245 device, n = 8. If we assume that the mean frequency, f, of signal transitions at the inputs = 10 MHz, the rise time, t_r = 2 ns, yielding:

$$P_{hold} = \frac{1}{2} \times 3.6\ \text{V} \times 500\ \mu\text{A} \times 2\ \text{ns} \times 2 \times 10\ \text{MHz} \times 8 = 0.288\ \text{mW} \qquad (7)$$

Equation 7 predicts that the parameter P_{hold} increases with longer rise times. In contrast, there is the dynamic power dissipation, P_{dyn}, of the circuit, which, taking the power dissipation capacitance C_{pd} = 31 pF given in the device's data sheet, can be calculated:

$$\begin{aligned} P_{dyn} &= C_{pd} \times V_{CC}^2 \times f \times n \\ &= 31\ \text{pF} \times 3.6^2 \times 10\ \text{MHz} \times 8 = 320\ \text{mW} \end{aligned} \qquad (8)$$

Because power consumption P_{hold} caused by the bus-hold circuit is several orders of magnitude less than this, it safely can be disregarded.

6.3 Presetting Logic Levels

Some applications require specific logic levels on certain bus lines during the initialization phase after the supply voltage is switched on. The microprocessor queries this level and makes certain system settings (start vector, etc.) on the basis of the information it reads. In conventional bus-interface devices, the desired level is generated on the lines in question via pullup or pulldown resistors. Because the input resistances of CMOS circuits are very high, high-impedance resistors (10 kΩ to100 kΩ) do this job very well.

When using interface devices with the bus-hold function, however, additional attention has to be paid to this circuit detail. Hold circuits have an inherent tendency to generate a low level when the supply voltage is switched on. As noted previously, this circuit behaves like a latch. A comparatively large capacitance − the interconnect lines and other circuit components − is connected to its set input (the input of the integrated circuit). This capacitance is discharged when the supply voltage is switched on. This is the reason that a low level is generated there when the voltage is switched on. Because the bus-hold circuit still has a very high impedance during the first moment of the power-on phase ($V_{CC} \leq V_t$), a high-impedance pullup resistor (10 kΩ to 100 kΩ), at this point in time, would be able to put the latch into the opposite logic state and generate a high level at the input of the bus-hold circuit. However, this observation does not take into account the fact that other devices connected to this bus might couple charge into the previously mentioned capacitance during supply-voltage startup, thus forcing a different level from the one expected. In this respect, the outputs of the interface devices connected to the bus are more effective than the bus-hold circuit and an associated preset circuit. If the outputs during the power-on phase briefly enter an undesired active state, they force the bus-hold circuit to the output’s state. Then, a high-impedance pullup or pulldown resistor is no longer able to change this state.

Consequently, the only way to force the device to a certain state is to place suitable low-impedance pullup or pulldown resistors. According to the maximum input current to a bus-hold circuit, $I_{I(hold)max}$ = 500 μA. This current flows when a hold-circuit threshold voltage of V_t = 1.5 V is reached (see Figure 10). Taking this figure, the value for pullup resistance, R_p, can be calculated:

$$R_p = \frac{V_{CCmin} - V_t}{I_{I(hold)max}} \tag{9}$$

If an LVCH circuit is connected to the bus, the resistance is calculated as:

$$R_p = \frac{3.0\ \text{V} - 1.5\ \text{V}}{500\ \mu\text{A}} = 3\ \text{k}\Omega \tag{10}$$

If several devices with the bus-hold function are connected to the bus, the resistance value must be reduced accordingly.

7 Summary

This application report addresses the question of how to ensure defined levels on bus lines when all bus drivers are in the inactive high-impedance state (3-state). This is of particular importance in the case of smaller CMOS-based systems where, for technical reasons, the lines cannot be terminated by a resistor network matched to the line impedance. This application report presents various different circuit options, with particular reference to a novel bus-hold circuit that TI integrates into modern bus-interface devices. This additional circuit provides an ideal combination of all the functions needed for a bus system to run properly. These include:

- Ensuring a defined logic level when the bus is in the inactive state (3-state).
- Avoiding excessive supply current due to logic levels that lie outside the limits stipulated in data sheets. To this end, a bus-hold circuit often is a must for battery-operated systems.
- The bus-hold circuit also prevents oscillation of the bus-interface devices provoked by undefined logic levels. Combined with appropriate power consumption, this measure promotes both the reliability and the electromagnetic compatibility of the system.

Insert Tab Here

Insert Tab Here

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as explained in the following example.

EXAMPLE: SN 74CBTLV3245A DGV R

Prefix

SN = Standard prefix
SNJ = Compliant to MIL-PRF-38535 (QML)

Unique Circuit Description

MUST CONTAIN FIVE TO TWELVE CHARACTERS

Examples: 4016B
74CBT1G125
74CBTLVR16292

Package

MUST CONTAIN ONE TO THREE LETTERS

D, DW = plastic small-outline integrated circuit
DB, DBQ, DCT, DL = plastic shrink small-outline package
DBB, DGV = plastic thin very small-outline package
DBV, DCK, DCU = plastic small-outline transistor
DGG, PW = plastic thin shrink small-outline package
FK = leadless ceramic chip carrier
GKE, GQL, GQN, YEA = ball grid array
J, JT = ceramic dual-in-line package
N = plastic dual-in-line package
NS = plastic small-outline package
W, WD = ceramic flatpack

Acquired Harris circuits' packages listed in the data sheets have the following equivalent TI packages:

HARRIS	TI	PIN COUNT
E	N	14, 16, 20
F	J	14, 16, 20
F	JT	24, 28
H	–	Chip only
M†	D	8, 14, 16
SM†	DB	14, 16, 20, 24, 28

† Add the suffix 96 for tape and reel.

NOTE: For order entry for some devices, the package designation must be abbreviated as indicated on the data sheet.

Tape and Reel Packaging

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

MUST CONTAIN ONE LETTER

R = Standard tape and reel (required for DBB, DBQ, DBV, DCK, DCT, DCU, DGG, DGV, GKE, GQL, GQN, PW, YEA, YEP, YZA, YZP, ZKE, ZQL, and ZQN; optional for D, DB, DL, DW, N, and NS packages)

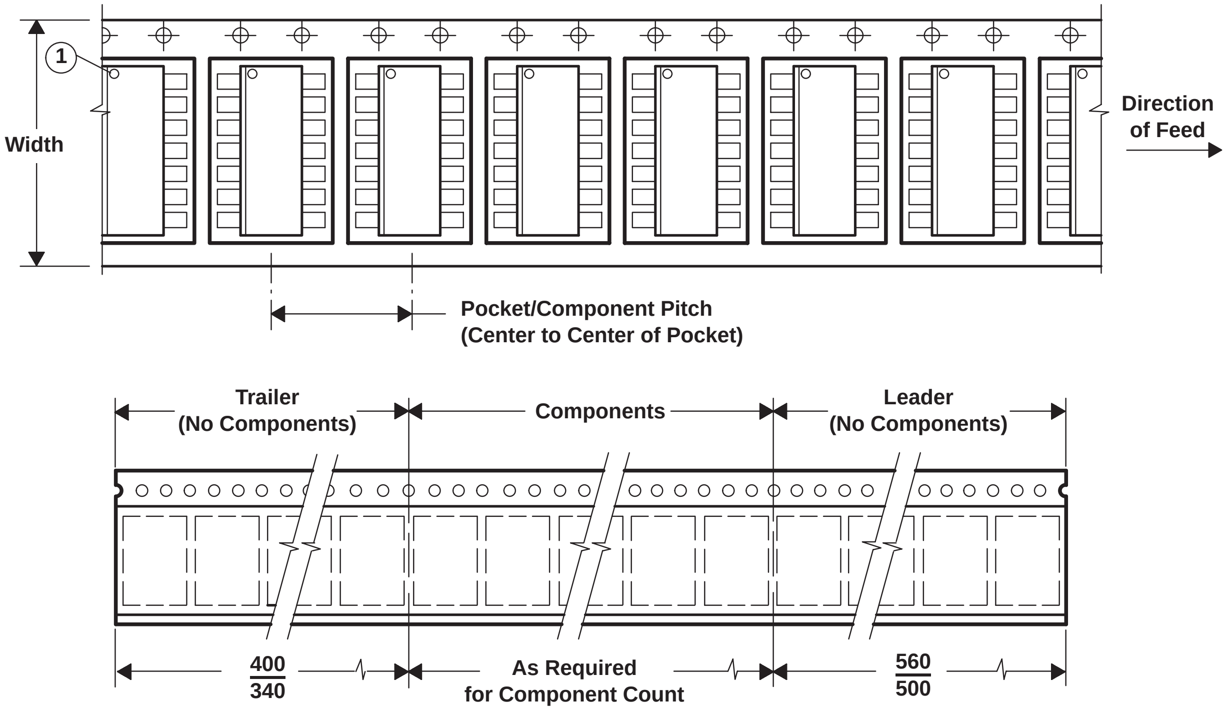
Table 1. Normal Dimensions of Packing Materials

CARRIER-TAPE WIDTH (mm)	COVER-TAPE WIDTH (mm)	REEL WIDTH (mm)	REEL DIAMETER (mm)
8	5.4	9.0	178
12	9.2	12.4	330
16	13.3	16.4	330
24	21.0	24.4	330
32	25.5	32.4	330
44	37.5	44.4	330
56	49.5	56.4	330

All material meets or exceeds industry guidelines for ESD protection.

Dimensions are selected based on package size and design configurations. All dimensions are established to be within the recommendations of the Electronics Industry Association Standard EIA-481-1,2,3.

Common dimensions of particular interest to the end user are carrier-tape width, pocket pitch, and quantity per reel (see Figure 1 and Table 2).



1
Width
Direction of Feed
Pocket/Component Pitch (Center to Center of Pocket)
Trailer (No Components)
Components
Leader (No Components)
400/340
As Required for Component Count
560/500

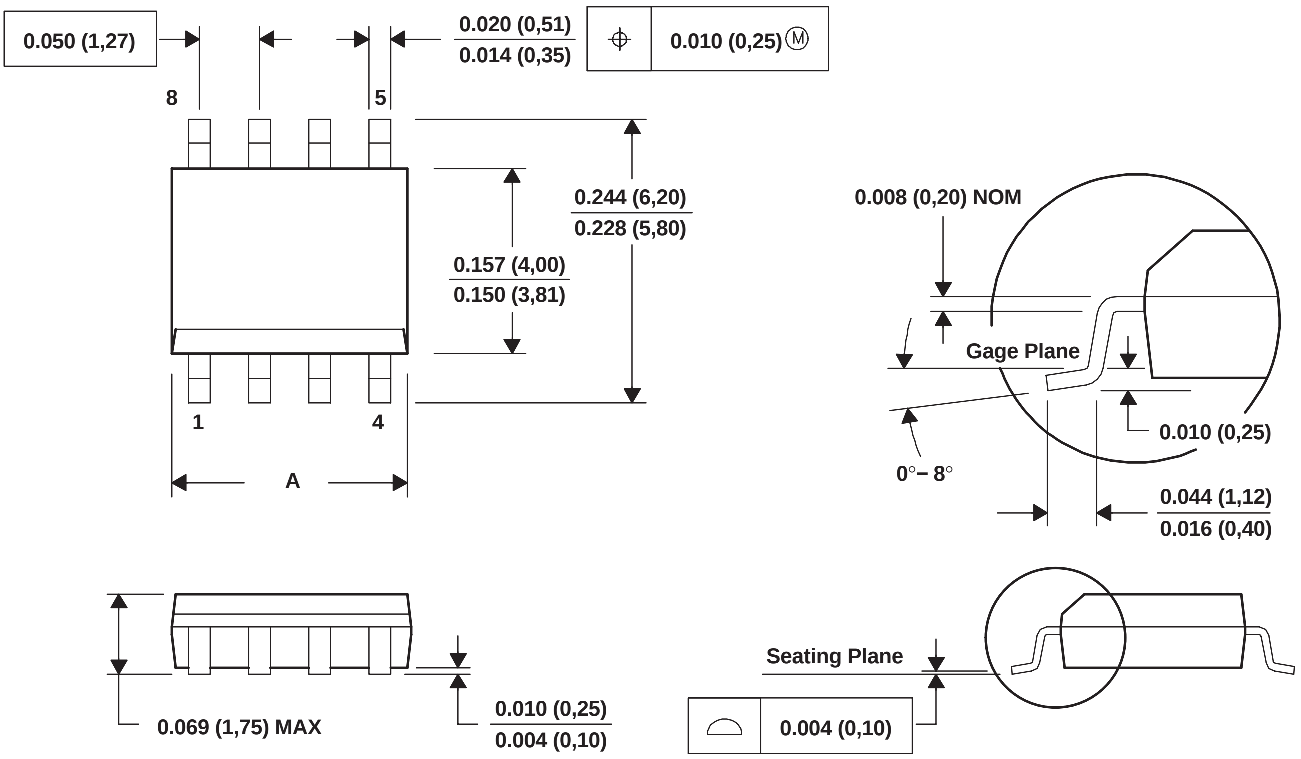
Figure 1. Typical Carrier-Tape Design

Table 2. Selected Tape-and-Reel Specifications

PACKAGE		NO. OF PINS	CARRIER-TAPE WIDTH (mm)	POCKET PITCH (mm)	QTY/REEL
LFBGA	GKE	96	24.00	12.00	1000
SOIC	D	14	16.00	8.00	2500
		16	16.00	8.00	2500
	DW	16	16.00	8.00/12.00	1000
		20	24.00	12.00	1000
SOT	DBV	5	8.00	4.00	3000
	DCK	5	8.00	4.00	3000
SSOP	DB	14	16.00	12.00	2000
		16	16.00	12.00	2000
		20	16.00	12.00	2000
		24	16.00	12.00	2000
	DBQ	16	12.00	12.00	2500
		20	16.00	12.00	2500
		24	16.00	12.00	2500
	DCT	8	12.00	8.00	3000
	DL	48	32.00	16.00	1000
		56	32.00	16.00	1000
TSSOP	DGG	48	24.00	12.00	2000
		56	24.00	12.00	2000
		64	24.00	12.00	2000
	PW	8	12.00	8.00	2000
		14	12.00	8.00	2000
		16	12.00	8.00	2000
		20	16.00	8.00	2000
		24	16.00	8.00	2000
		28	16.00	8.00	2000
TVSOP	DBB	80	24.00	12.00	2000
	DGV	14	16.00	8.00	2000
		16	16.00	8.00	2000
		20	16.00	8.00	2000
		24	16.00	8.00	2000
		48	16.00	8.00	2000
		56	24.00	8.00	2000
VSSOP	DCU	8.00	8.00	8.00	3000

D (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN


0.050 (1,27)
0.020 (0,51)
0.014 (0,35)
0.010 (0,25) Ⓜ
8
5
1
4
0.244 (6,20)
0.228 (5,80)
0.157 (4,00)
0.150 (3,81)
A
0.008 (0,20) NOM
Gage Plane
0.010 (0,25)
0°– 8°
0.044 (1,12)
0.016 (0,40)
Seating Plane
0.069 (1,75) MAX
0.010 (0,25)
0.004 (0,10)
0.004 (0,10)

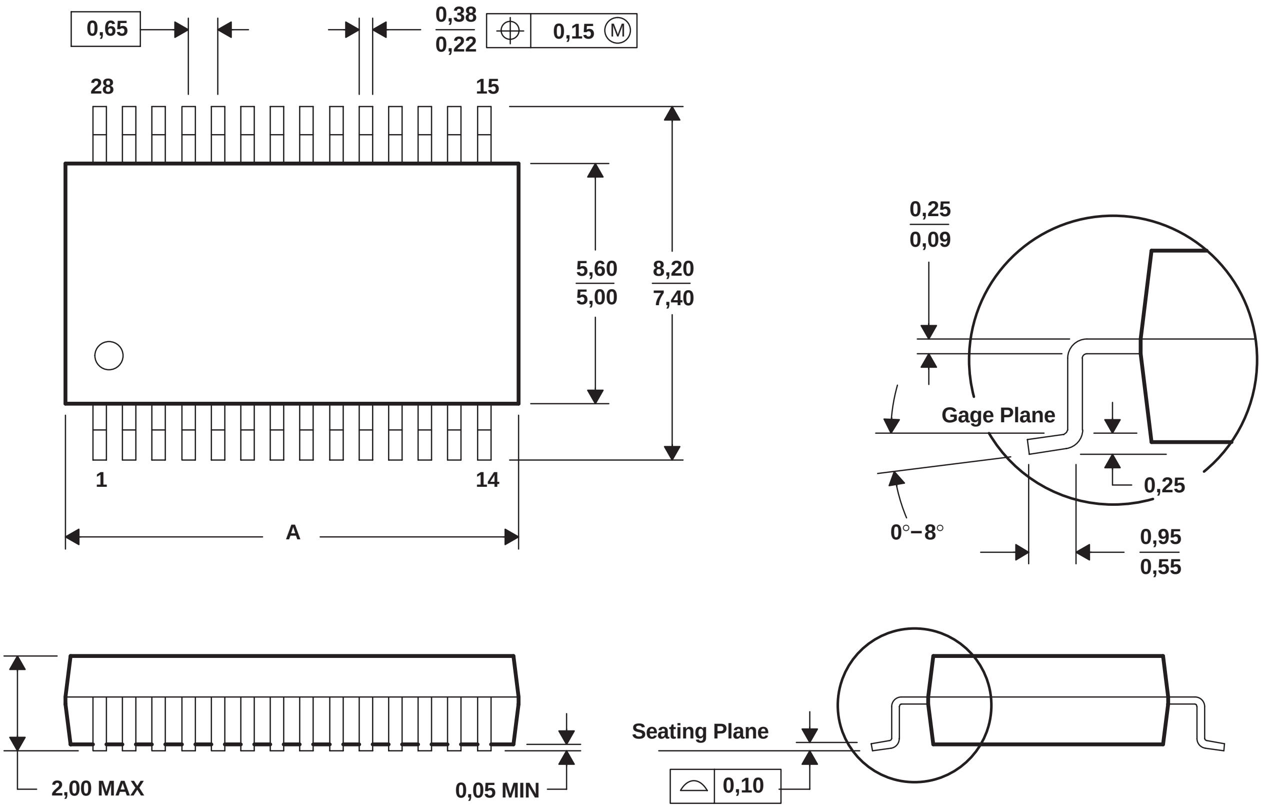
PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN


0,65
0,38
0,22
⌖ 0,15 Ⓜ
28
15
1
14
5,60
5,00
8,20
7,40
A
0,25
0,09
Gage Plane
0,25
0°–8°
0,95
0,55
2,00 MAX
0,05 MIN
Seating Plane
0,10

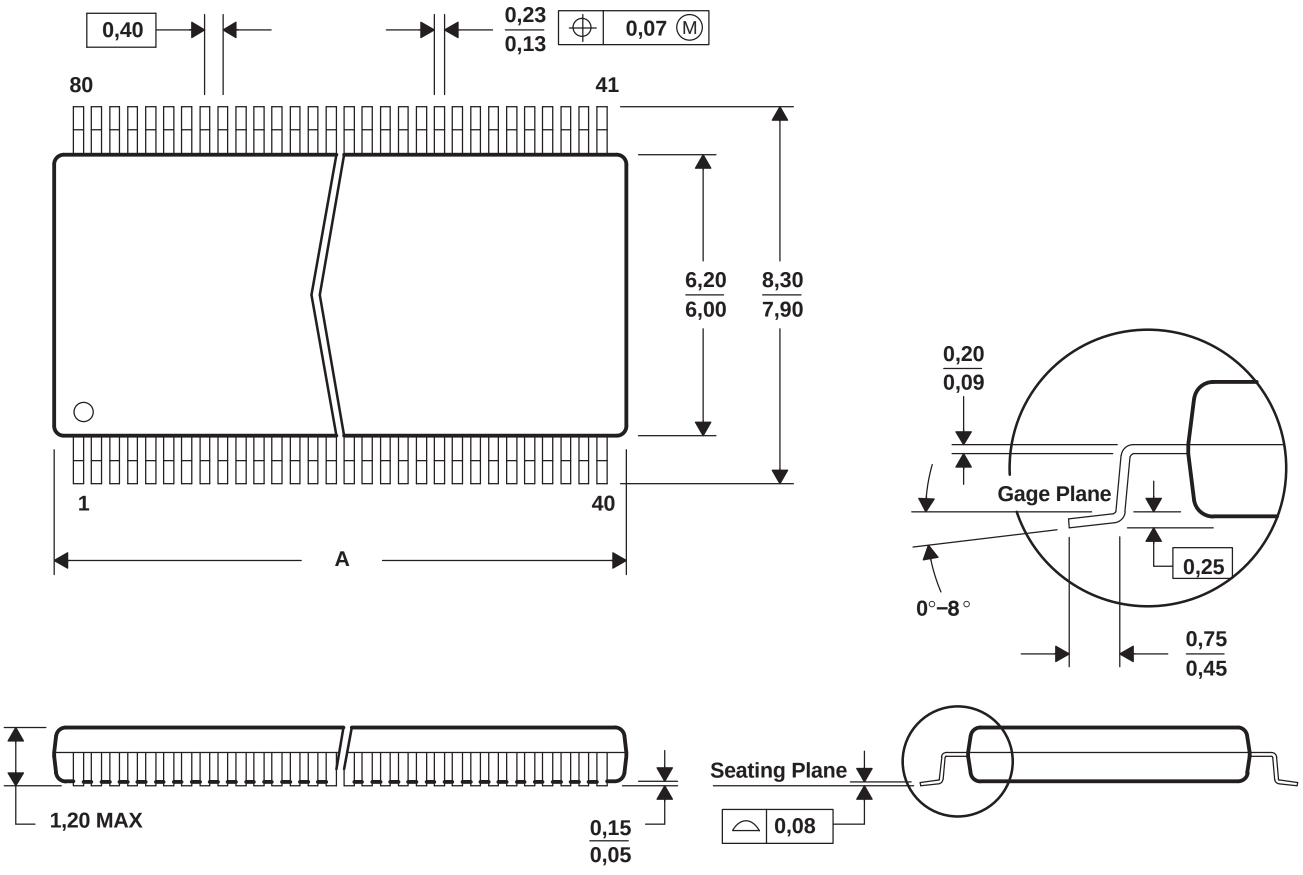
PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065/E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

DBB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

80 PINS SHOWN

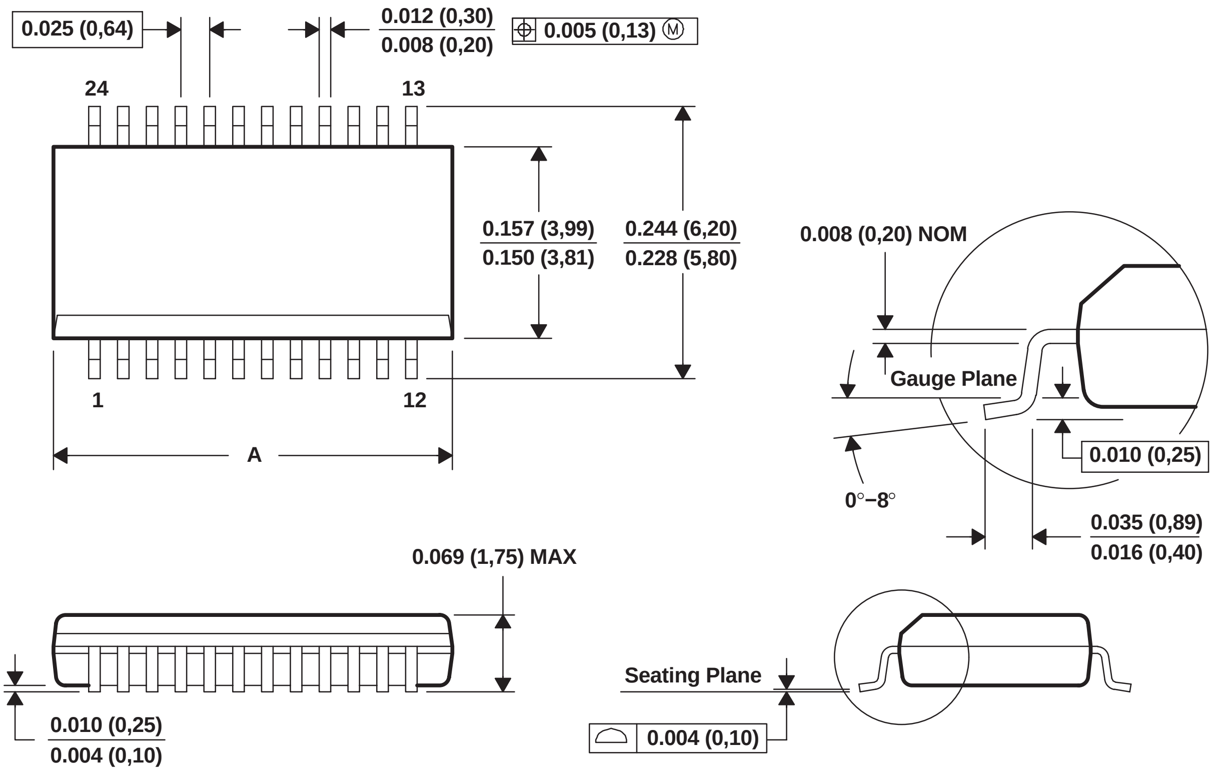

0,40
0,23
0,13
0,07 M
80
41
6,20
6,00
8,30
7,90
0,20
0,09
Gage Plane
0,25
0°–8°
0,75
0,45
1
40
A
1,20 MAX
Seating Plane
0,15
0,05
0,08

PINS** / DIM	80	100
A MAX	17,10	20,90
A MIN	16,90	20,70

4040212/E 03/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC : 80 Pin − MO-153 Variation FF
100 Pin − MO-194 Variation BB

DBQ (R−PDSO−G**) PLASTIC SMALL−OUTLINE PACKAGE

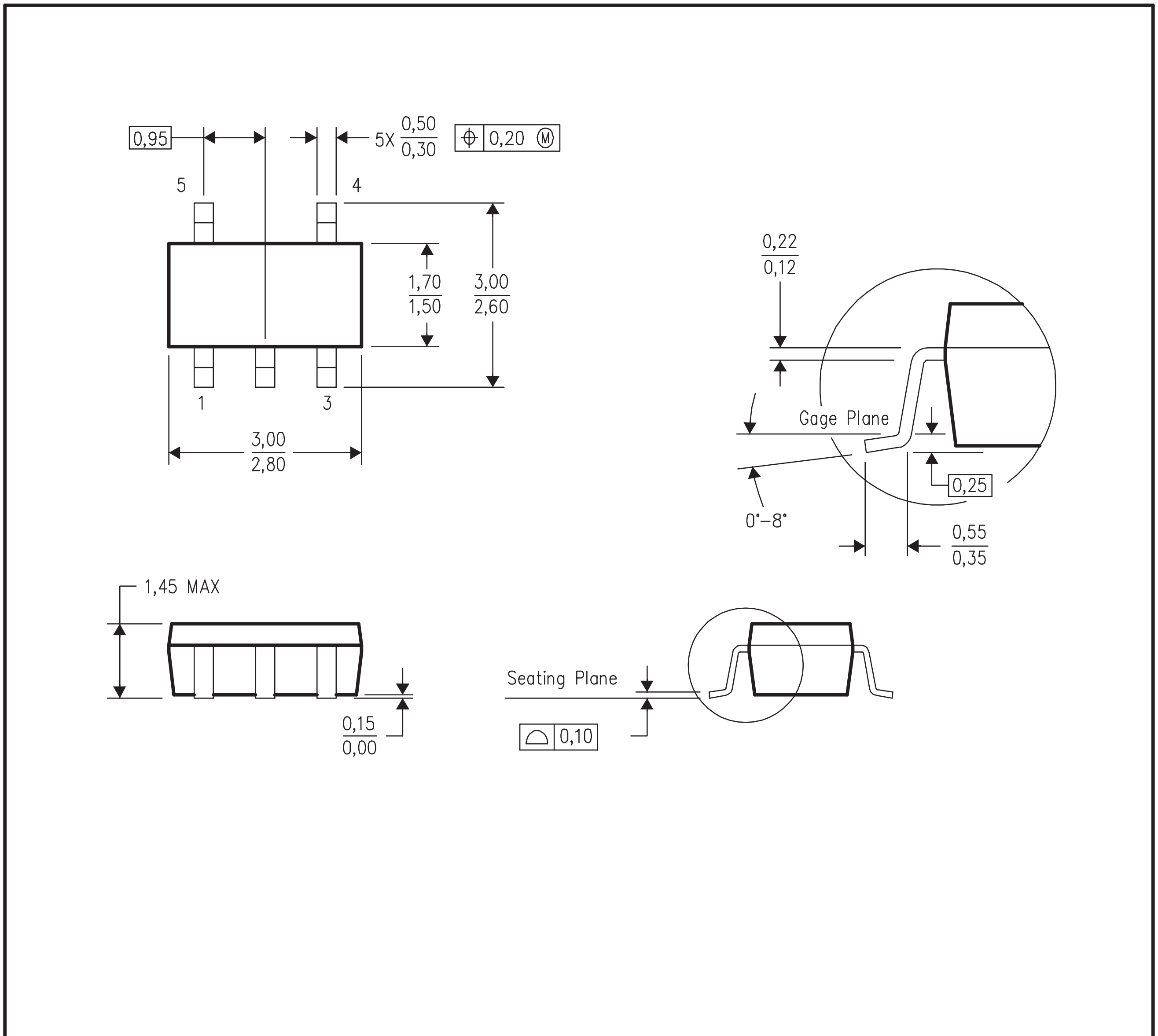

0.025 (0,64)
0.012 (0,30)
0.008 (0,20)
0.005 (0,13) M
24
13
1
12
0.157 (3,99)
0.150 (3,81)
0.244 (6,20)
0.228 (5,80)
A
0.008 (0,20) NOM
Gauge Plane
0.010 (0,25)
0°−8°
0.035 (0,89)
0.016 (0,40)
0.069 (1,75) MAX
0.010 (0,25)
0.004 (0,10)
Seating Plane
0.004 (0,10)

PINS ** / DIM	16	20	24	28
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.189 (4,80)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)
D M0−137 VARIATION	AB	AD	AE	AF

4073301/F 02/02

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO−137.

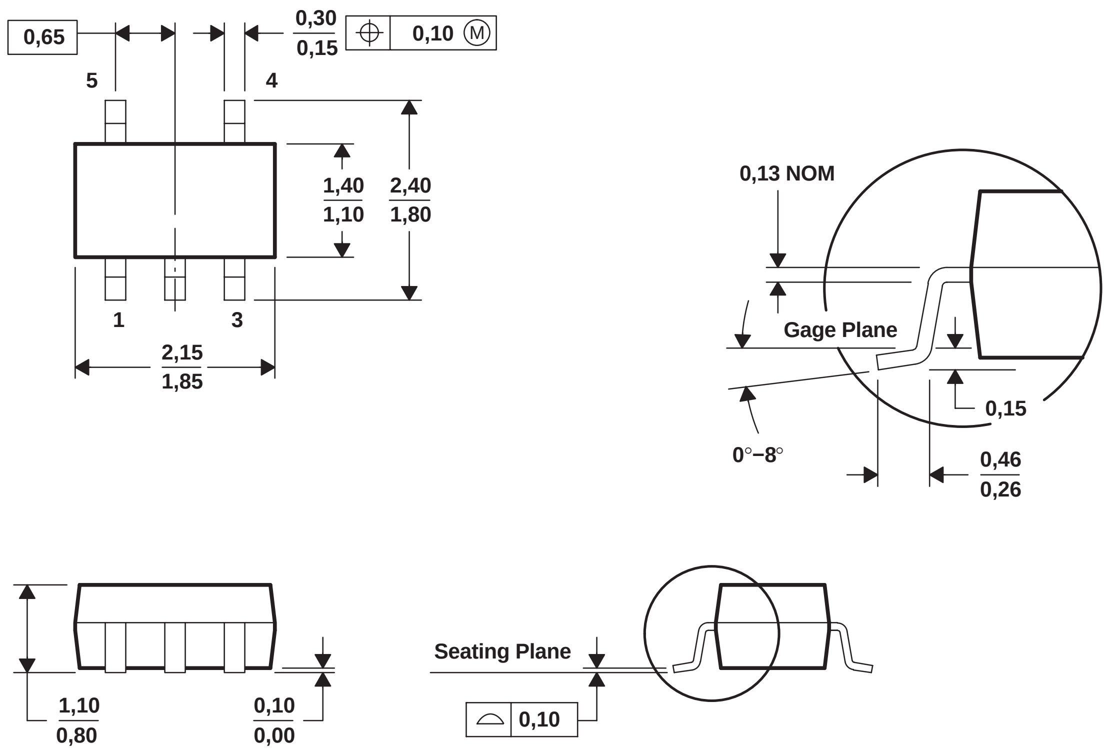
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE


0,95
5X 0,50/0,30
0,20 M
5
4
1
3
1,70/1,50
3,00/2,60
3,00/2,80
0,22/0,12
Gage Plane
0°–8°
0,25
0,55/0,35
1,45 MAX
0,15/0,00
Seating Plane
0,10

4073253-4/H 10/2003

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO–178 Variation AA.

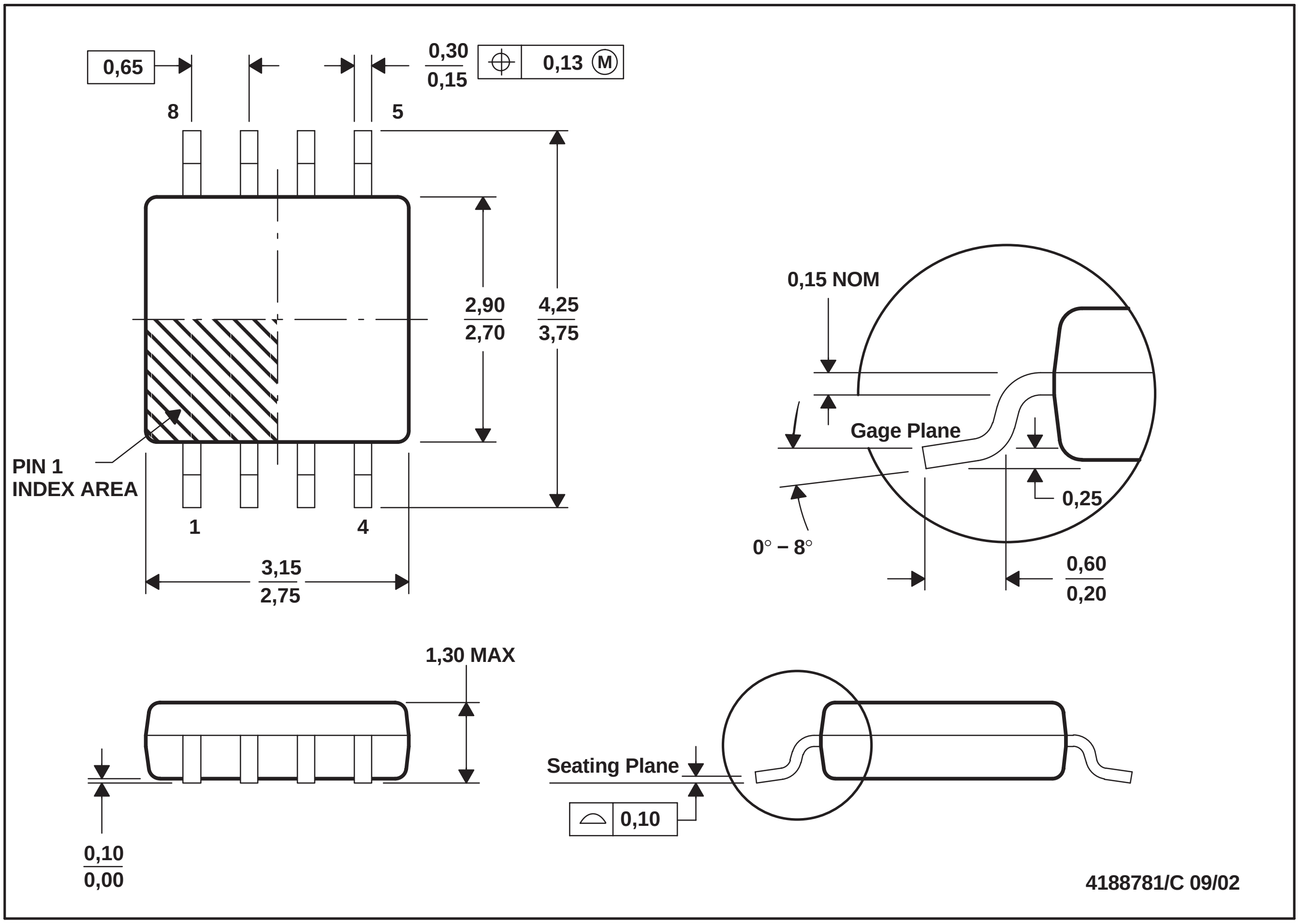
DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE


0,65
0,30
0,15
0,10 Ⓜ
5
4
1,40
1,10
2,40
1,80
1
3
2,15
1,85
0,13 NOM
Gage Plane
0,15
0°–8°
0,46
0,26
Seating Plane
1,10
0,80
0,10
0,00
0,10

4093553-2/D 01/02

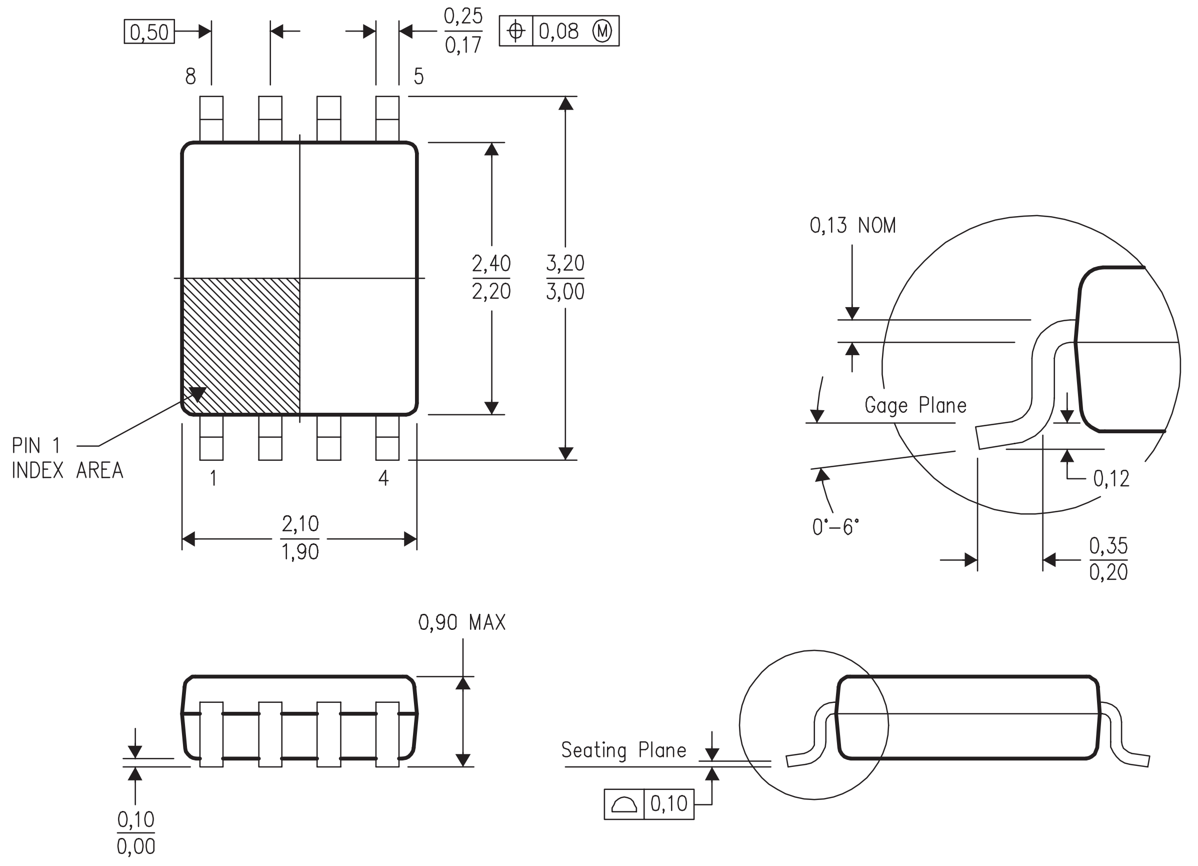
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-203

DCT (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**


0,65
0,30
0,15
0,13 Ⓜ
8
5
2,90
2,70
4,25
3,75
PIN 1
INDEX AREA
1
4
3,15
2,75
0,15 NOM
Gage Plane
0,25
0° – 8°
0,60
0,20
1,30 MAX
Seating Plane
0,10
0,10
0,00
4188781/C 09/02

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. Falls within JEDEC MO-187 variation DA.

DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)

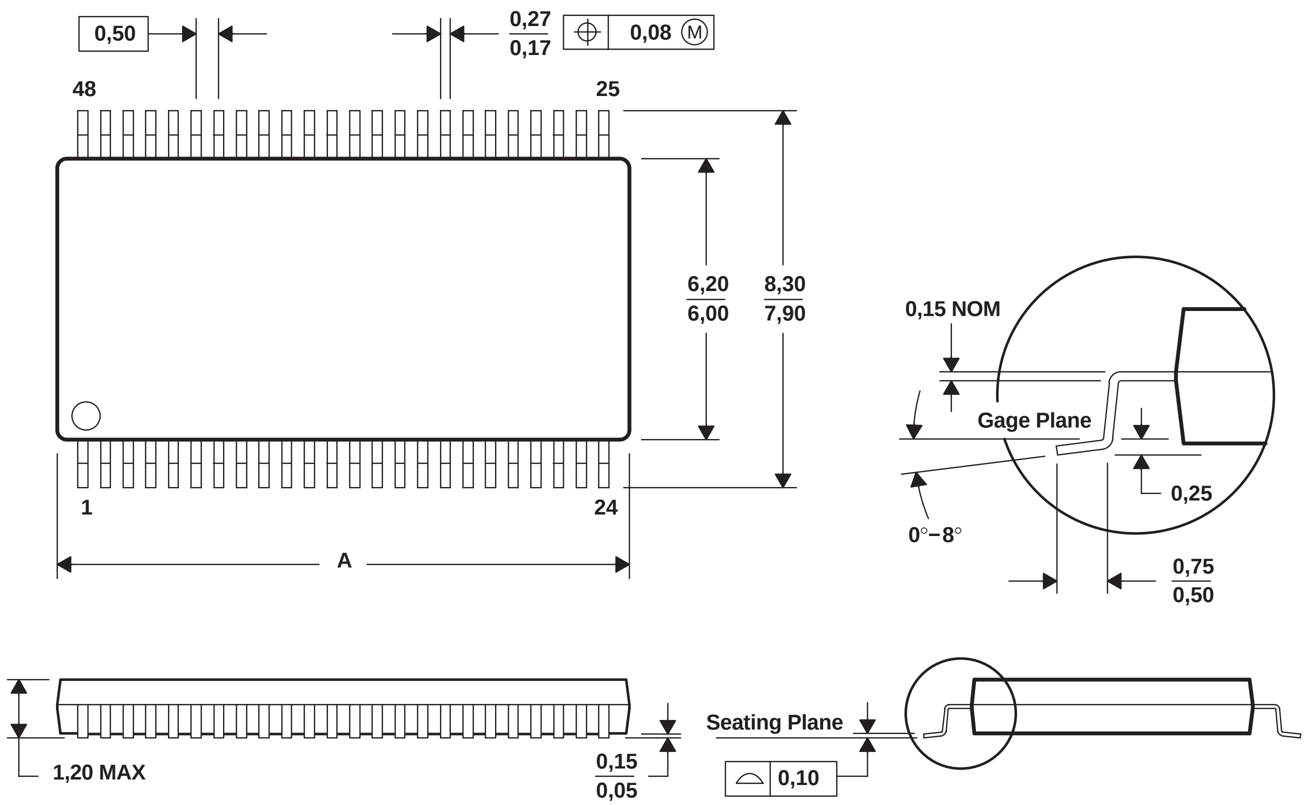

0,50
0,25
0,17
0,08 Ⓜ
8
5
2,40
2,20
3,20
3,00
PIN 1
INDEX AREA
1
4
2,10
1,90
0,13 NOM
Gage Plane
0,12
0°–6°
0,35
0,20
0,90 MAX
Seating Plane
0,10
0,10
0,00

4200503/E 05/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO–187 variation CA.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN


0,50
0,27
0,17
0,08 M
48
25
6,20
6,00
8,30
7,90
0,15 NOM
Gage Plane
0,25
0°–8°
0,75
0,50
1
24
A
1,20 MAX
0,15
0,05
Seating Plane
0,10

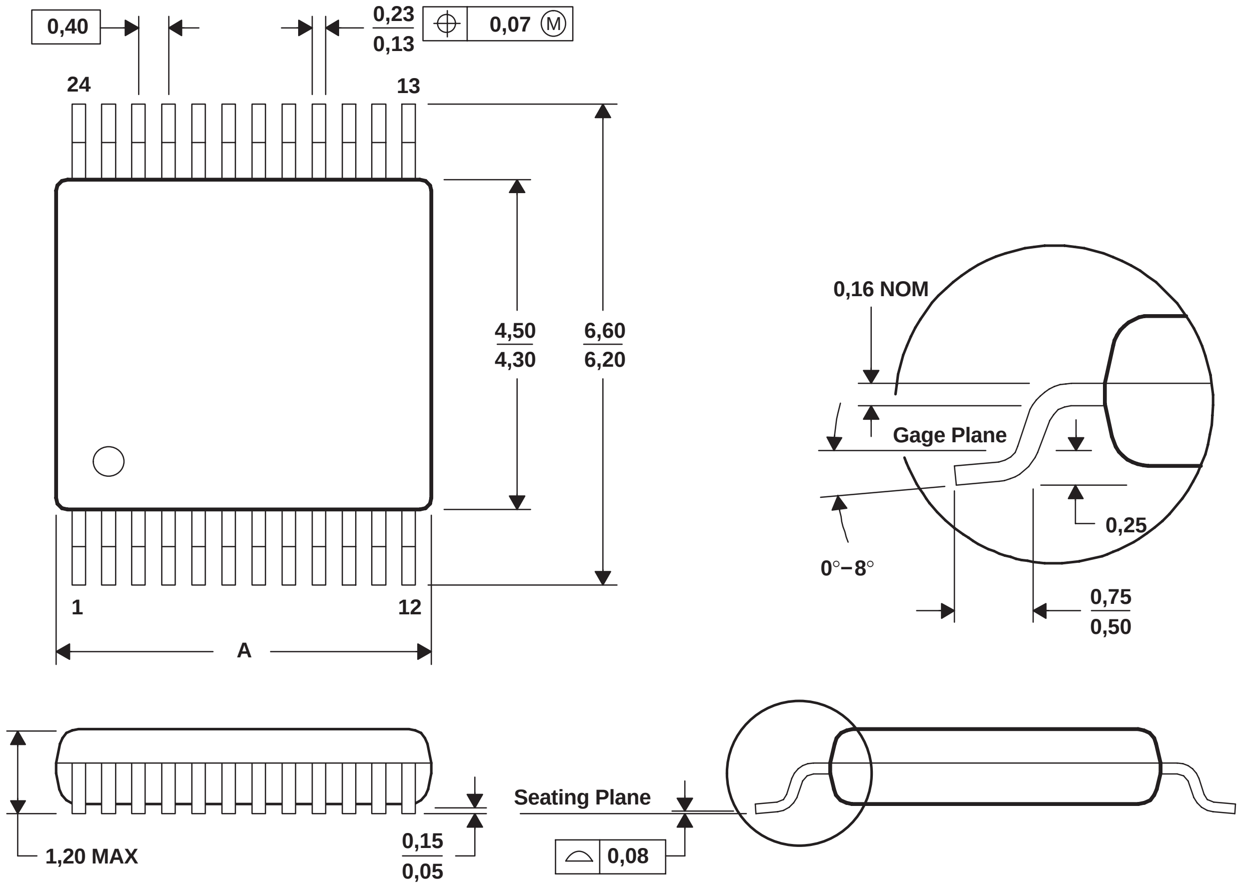
PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/ F 12/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE

24 PINS SHOWN


0,40
0,23
0,13
0,07 M
24
13
4,50
4,30
6,60
6,20
0,16 NOM
Gage Plane
0,25
0°–8°
0,75
0,50
1
12
A
Seating Plane
1,20 MAX
0,15
0,05
0,08

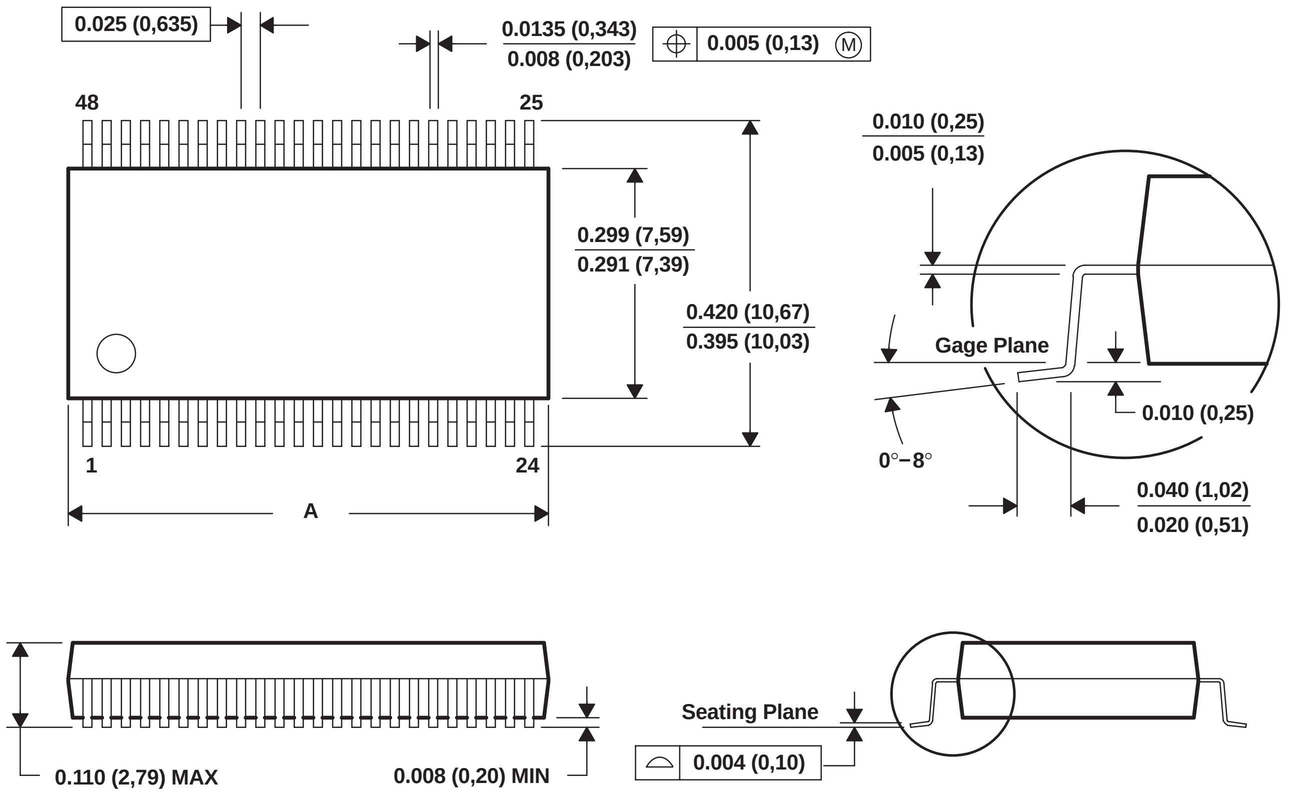
PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins – MO-153
  14/16/20/56 Pins – MO-194

DL (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN


0.025 (0,635)
0.0135 (0,343)
0.008 (0,203)
0.005 (0,13) M
48
25
0.010 (0,25)
0.005 (0,13)
0.299 (7,59)
0.291 (7,39)
0.420 (10,67)
0.395 (10,03)
Gage Plane
0.010 (0,25)
0°–8°
1
24
A
0.040 (1,02)
0.020 (0,51)
Seating Plane
0.004 (0,10)
0.110 (2,79) MAX
0.008 (0,20) MIN

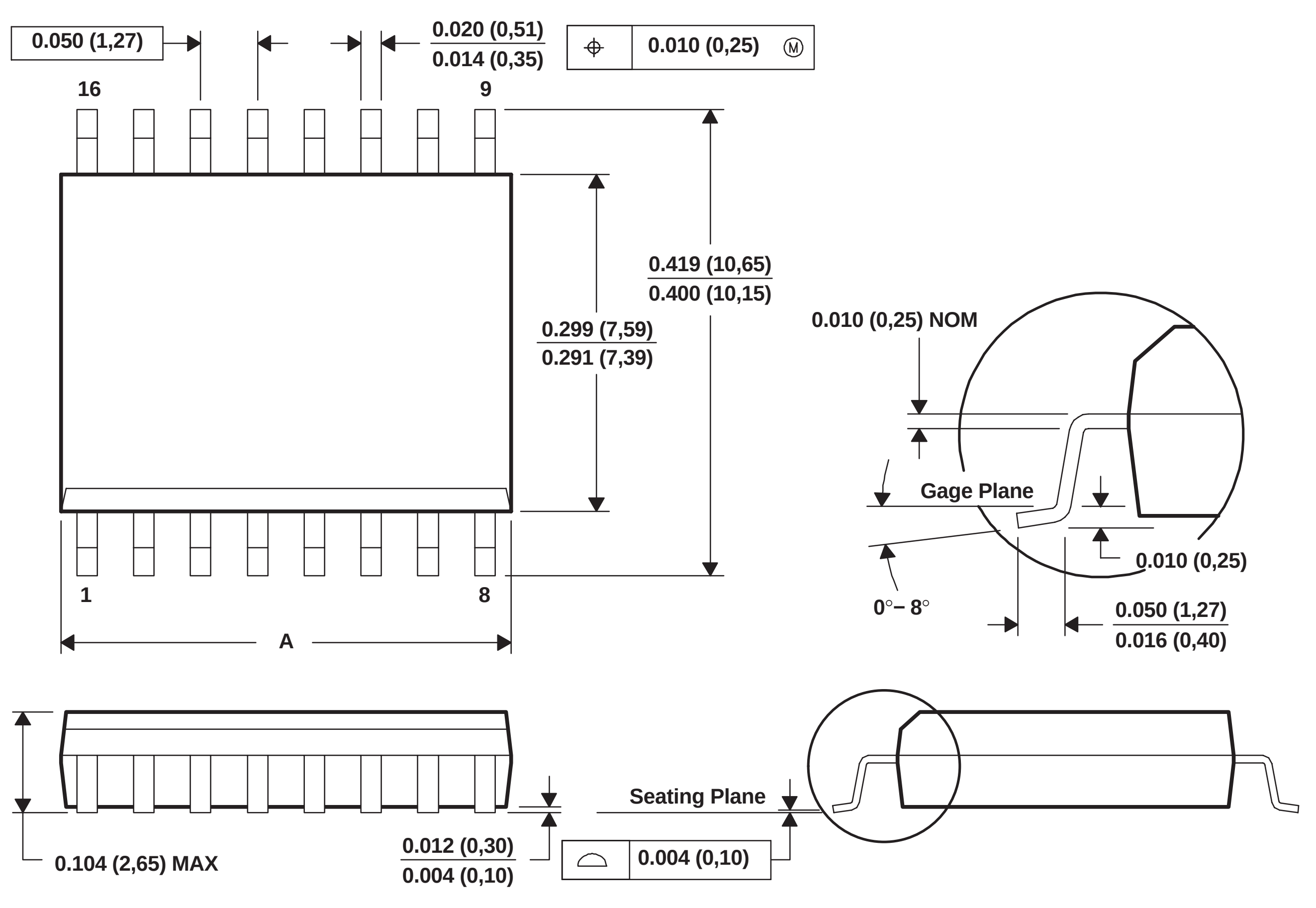
DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/E 12/01

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN


0.050 (1,27)
0.020 (0,51)
0.014 (0,35)
0.010 (0,25) Ⓜ
16
9
1
8
0.419 (10,65)
0.400 (10,15)
0.299 (7,59)
0.291 (7,39)
0.010 (0,25) NOM
Gage Plane
0.010 (0,25)
0°– 8°
0.050 (1,27)
0.016 (0,40)
A
Seating Plane
0.104 (2,65) MAX
0.012 (0,30)
0.004 (0,10)
0.004 (0,10)

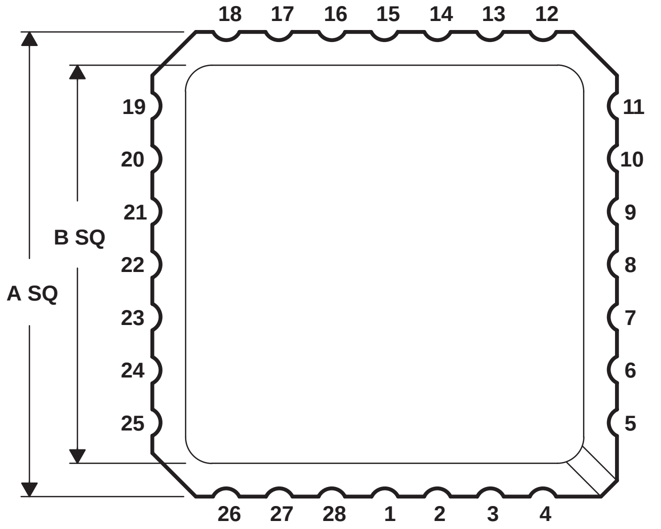
PINS ** / DIM	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/E 08/01

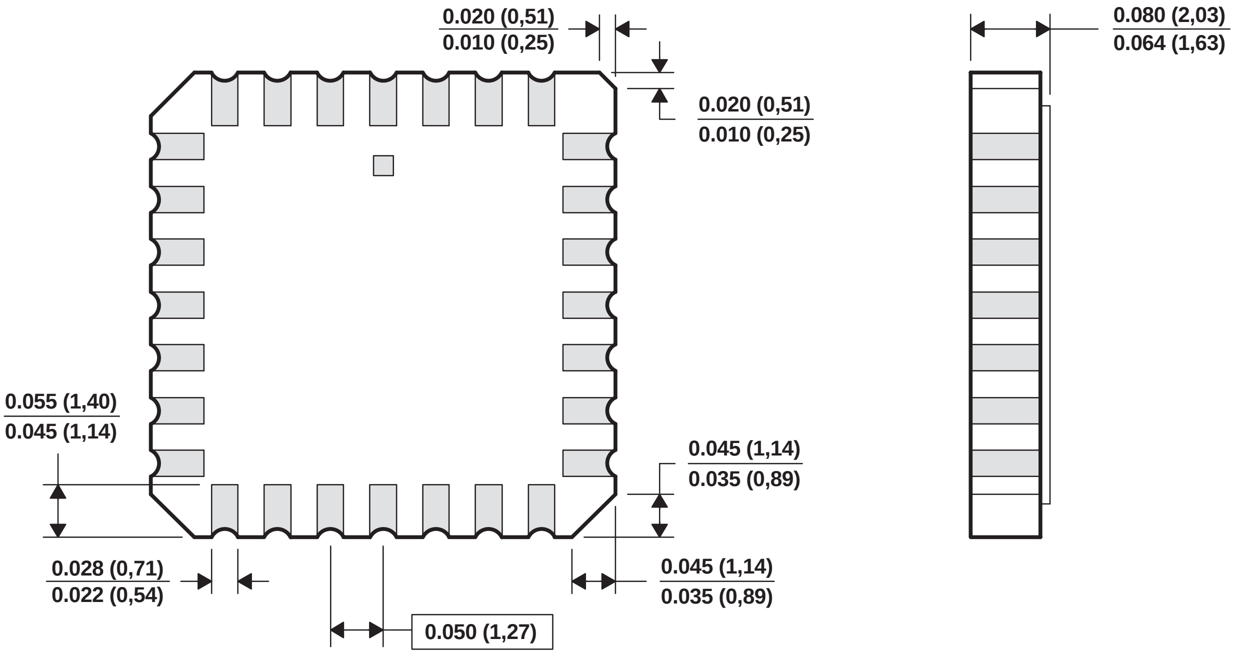
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013

FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINALS SHOWN


18
17
16
15
14
13
12
19
20
21
22
23
24
25
11
10
9
8
7
6
5
26
27
28
1
2
3
4
B SQ
A SQ

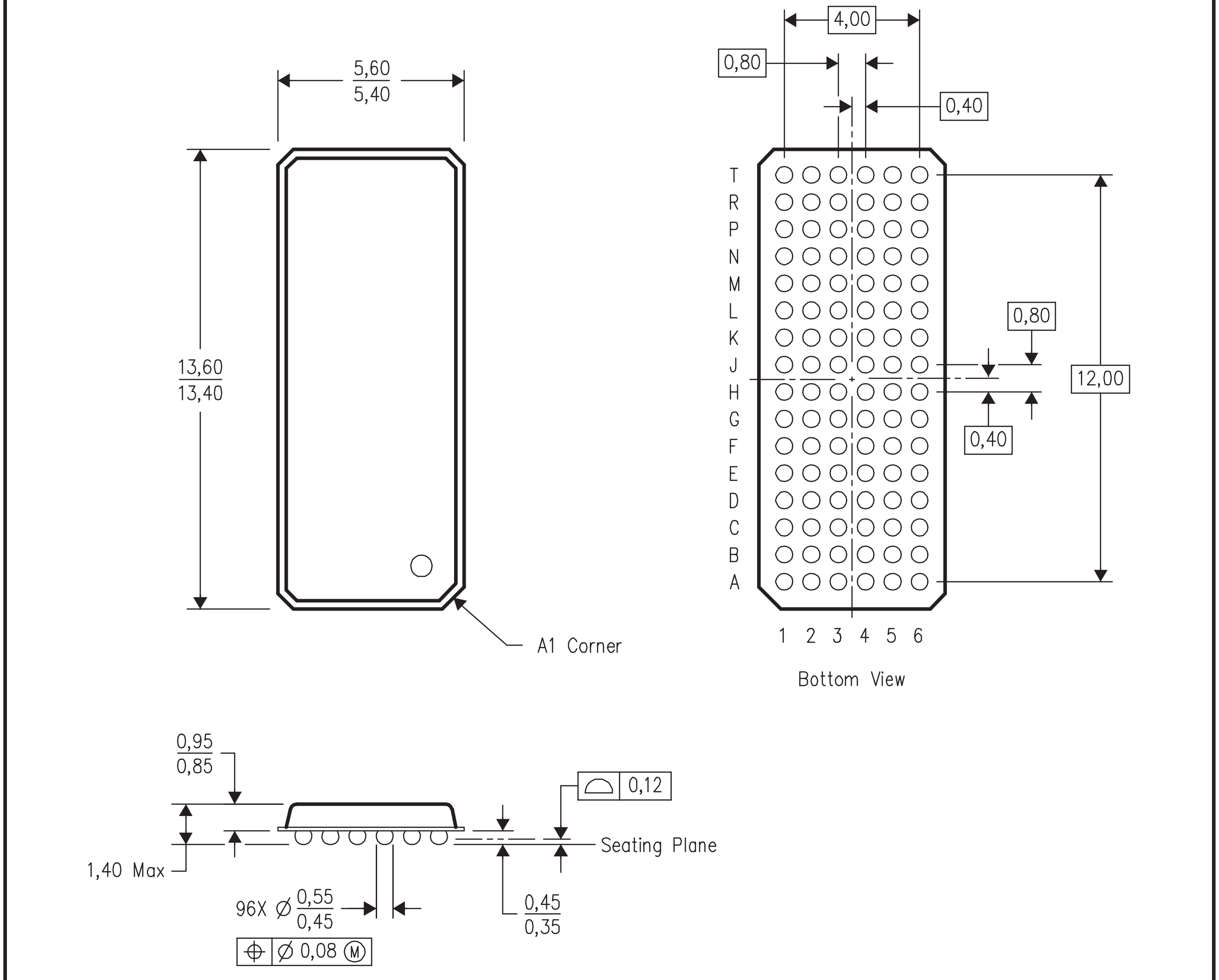
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)


0.020 (0,51)
0.010 (0,25)
0.020 (0,51)
0.010 (0,25)
0.080 (2,03)
0.064 (1,63)
0.055 (1,40)
0.045 (1,14)
0.045 (1,14)
0.035 (0,89)
0.028 (0,71)
0.022 (0,54)
0.045 (1,14)
0.035 (0,89)
0.050 (1,27)

4040140/C 11/95

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold-plated.
- E. Falls within JEDEC MS-004

GKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY

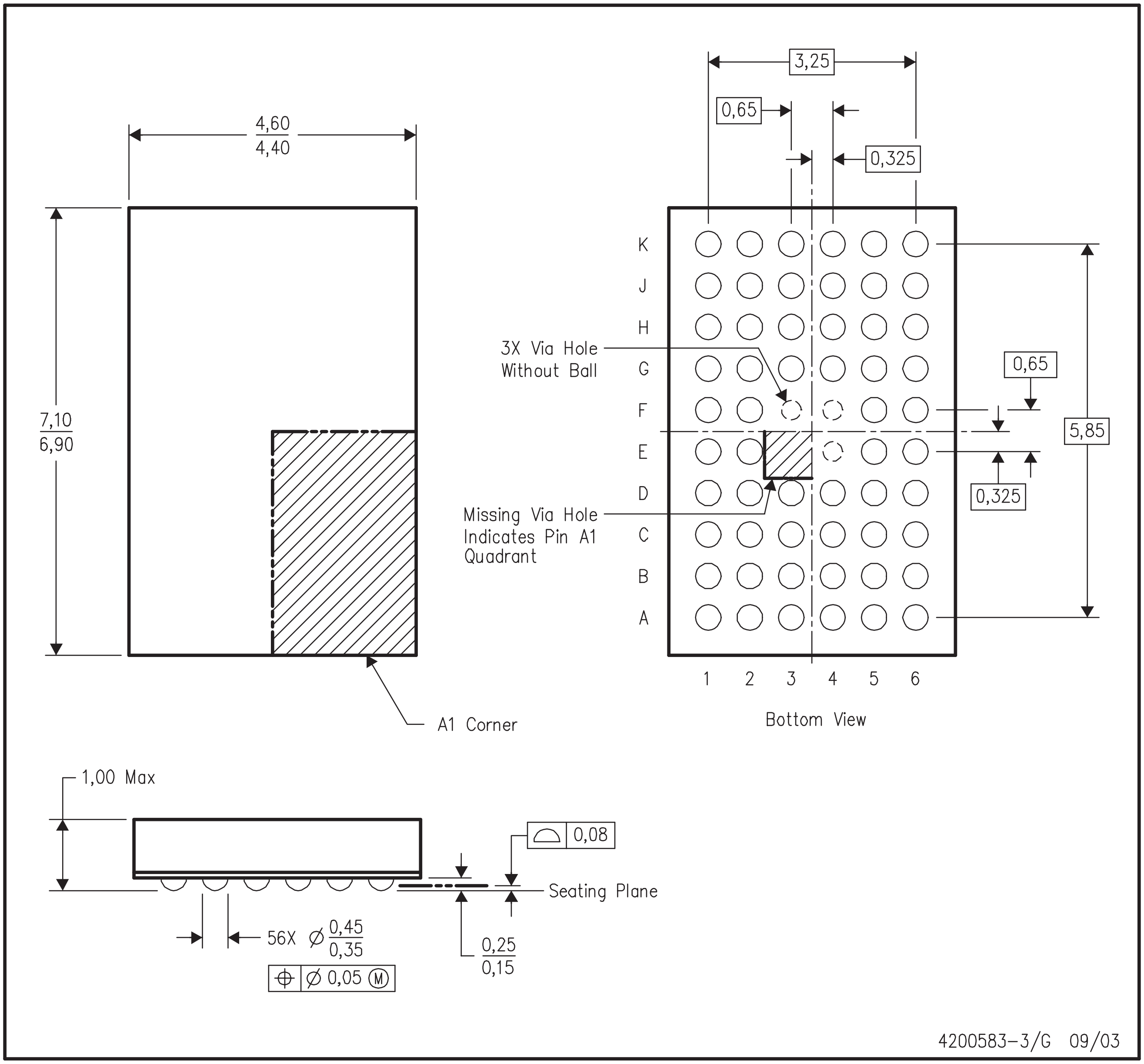

5,60
5,40
13,60
13,40
A1 Corner
4,00
0,80
0,40
T
R
P
N
M
L
K
J
H
G
F
E
D
C
B
A
0,80
12,00
0,40
1 2 3 4 5 6
Bottom View
0,95
0,85
1,40 Max
0,12
Seating Plane
96X Ø 0,55
0,45
Ø 0,08 M
0,45
0,35

4188953/E 06/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar BGA™ configuration
- D. Falls within JEDEC MO–205 variation CC.
- E. This package is tin–lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead–free.

MicroStar BGA is a trademark of Texas Instruments.

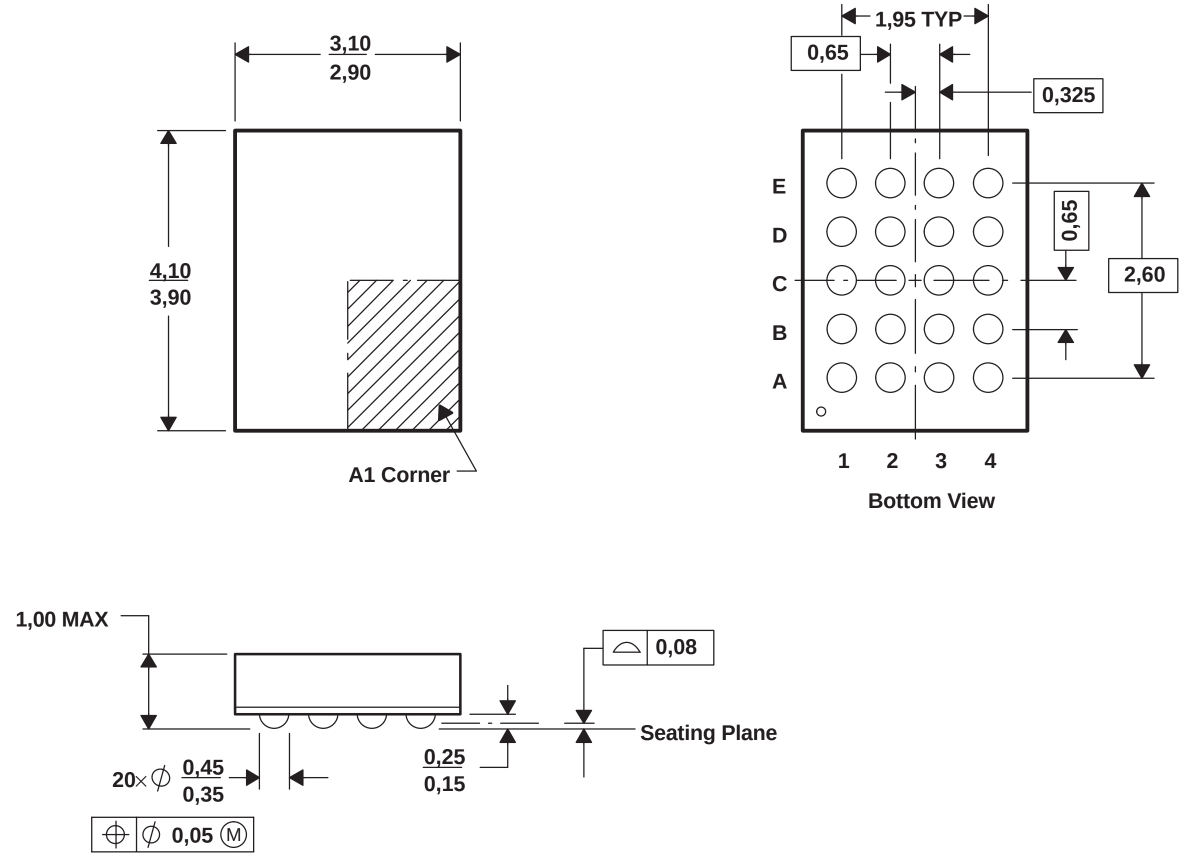
GQL (R-PBGA-N56) PLASTIC BALL GRID ARRAY


4,60
4,40
7,10
6,90
A1 Corner
3,25
0,65
0,325
K
J
H
G
F
E
D
C
B
A
1 2 3 4 5 6
3X Via Hole
Without Ball
Missing Via Hole
Indicates Pin A1
Quadrant
0,65
5,85
0,325
Bottom View
1,00 Max
0,08
Seating Plane
56X ∅ 0,45
0,35
∅ 0,05 Ⓜ
0,25
0,15
4200583-3/G 09/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar Junior™ BGA configuration.
- D. Falls within JEDEC MO-225 variation BA.
- E. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

GQN (R-PBGA-N20) **PLASTIC BALL GRID ARRAY**


3,10
2,90
4,10
3,90
A1 Corner
1,95 TYP
0,65
0,325
0,65
2,60
E
D
C
B
A
1
2
3
4
Bottom View
1,00 MAX
0,08
Seating Plane
20× ∅ 0,45
0,35
0,25
0,15
⌖ ∅ 0,05 Ⓜ

4200704/D 07/2002

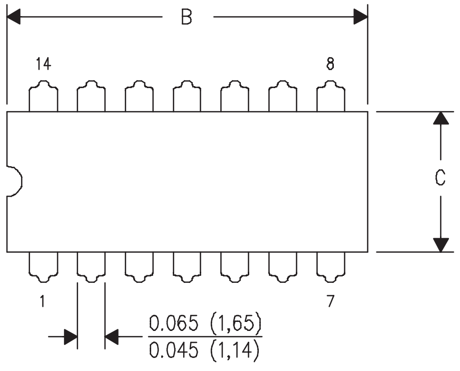
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar Junior™ configuration
- D. Falls within JEDEC MO-225 variation BC.
- E. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

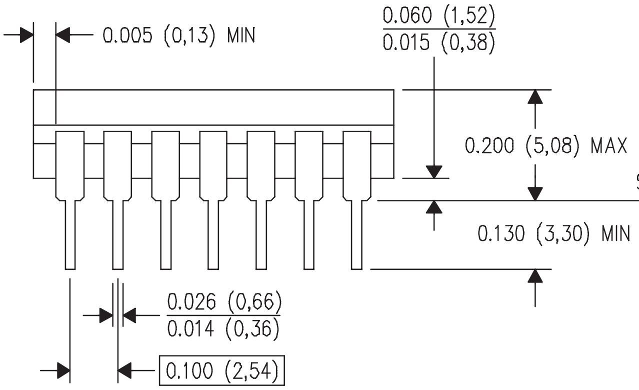
MicroStar Junior is a trademark of Texas Instruments.

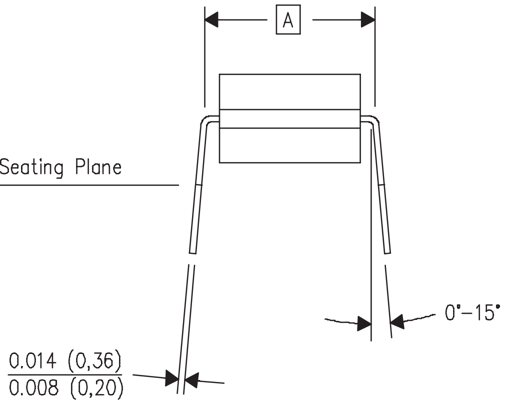
J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN

PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)


B
14
8
C
1
7
0.065 (1,65)
0.045 (1,14)


0.005 (0,13) MIN
0.060 (1,52)
0.015 (0,38)
0.200 (5,08) MAX
Seating Plane
0.130 (3,30) MIN
0.026 (0,66)
0.014 (0,36)
0.100 (2,54)


A
0°–15°
0.014 (0,36)
0.008 (0,20)

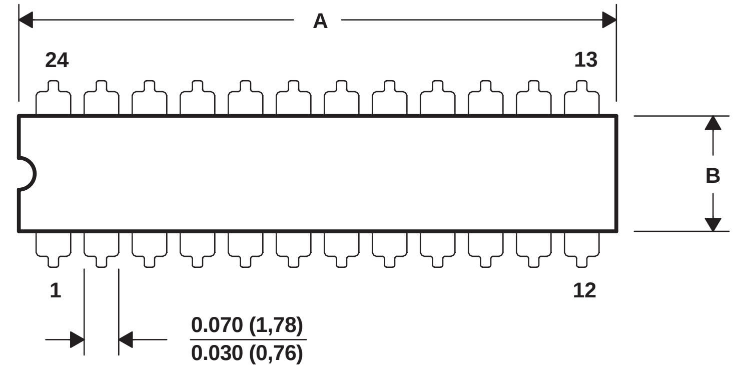
4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

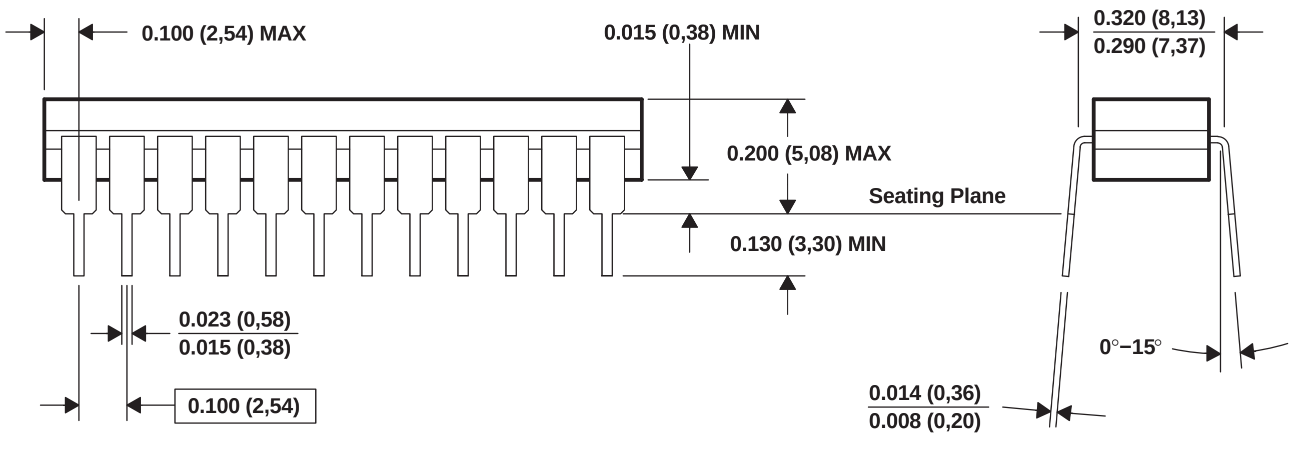
JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN


A
24
13
B
1
12
0.070 (1,78)
0.030 (0,76)

PINS ** / DIM	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)


0.100 (2,54) MAX
0.015 (0,38) MIN
0.320 (8,13)
0.290 (7,37)
0.200 (5,08) MAX
Seating Plane
0.130 (3,30) MIN
0.023 (0,58)
0.015 (0,38)
0°–15°
0.014 (0,36)
0.008 (0,20)
0.100 (2,54)

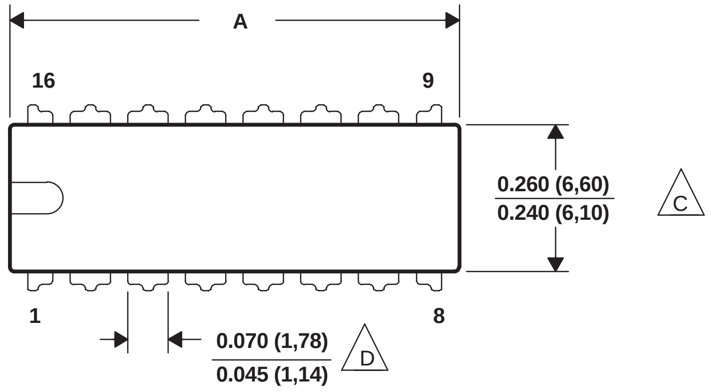
4040110/C 08/96

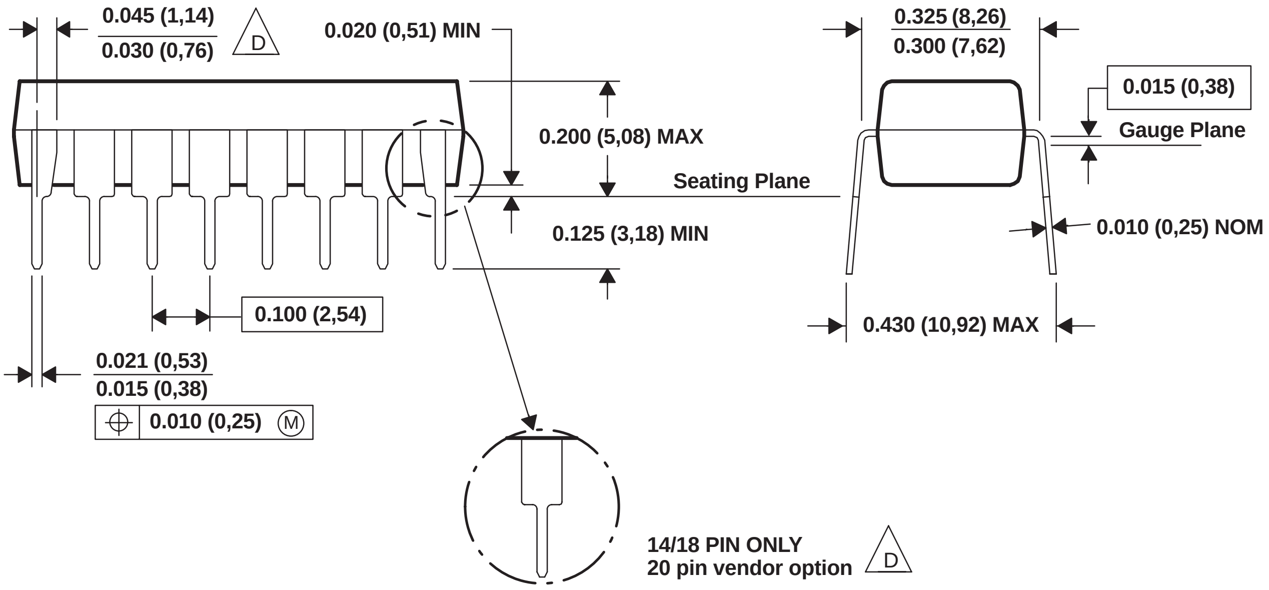
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

N (R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD


A
16
9
1
8
0.260 (6,60)
0.240 (6,10)
C
0.070 (1,78)
0.045 (1,14)
D

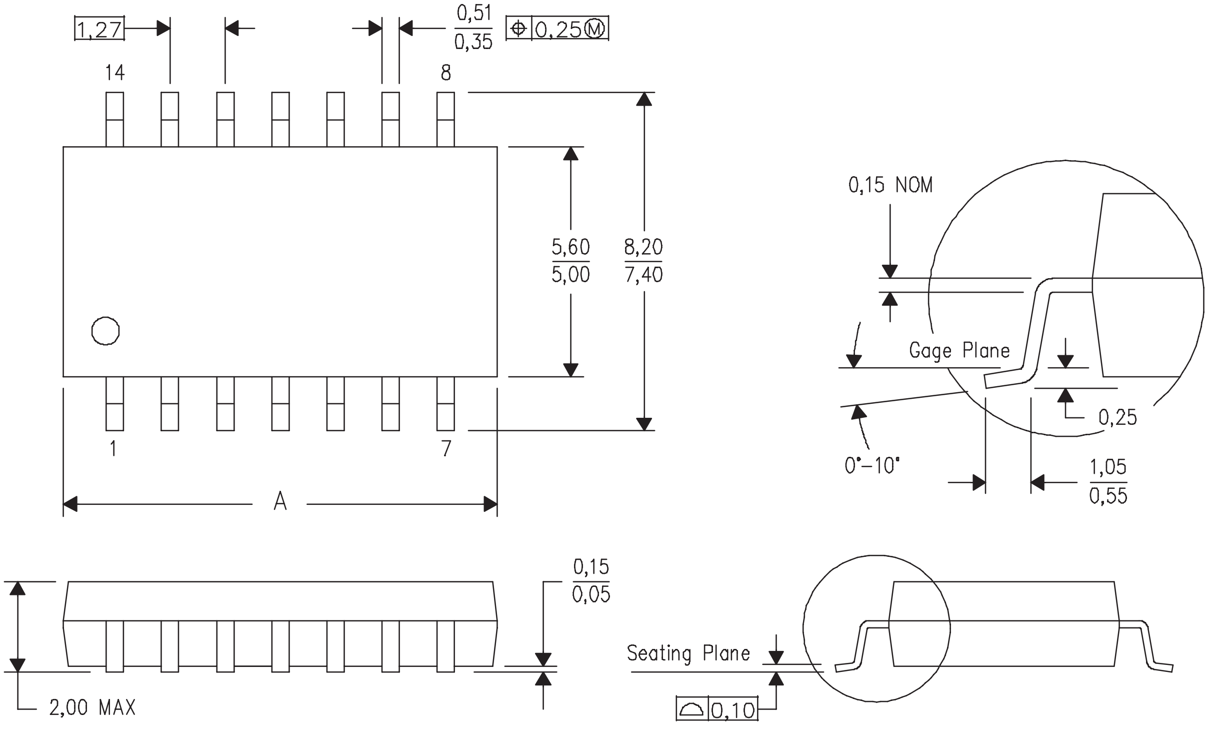

0.045 (1,14)
0.030 (0,76)
D
0.020 (0,51) MIN
0.325 (8,26)
0.300 (7,62)
0.015 (0,38)
Gauge Plane
0.200 (5,08) MAX
Seating Plane
0.125 (3,18) MIN
0.010 (0,25) NOM
0.100 (2,54)
0.430 (10,92) MAX
0.021 (0,53)
0.015 (0,38)
⌖ 0.010 (0,25) Ⓜ
14/18 PIN ONLY
20 pin vendor option
D

4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

NS (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN


1,27
0,51
0,35
⌖ 0,25 Ⓜ
14
8
1
7
5,60
5,00
8,20
7,40
A
0,15 NOM
Gage Plane
0,25
0°–10°
1,05
0,55
0,15
0,05
Seating Plane
⌓ 0,10
2,00 MAX

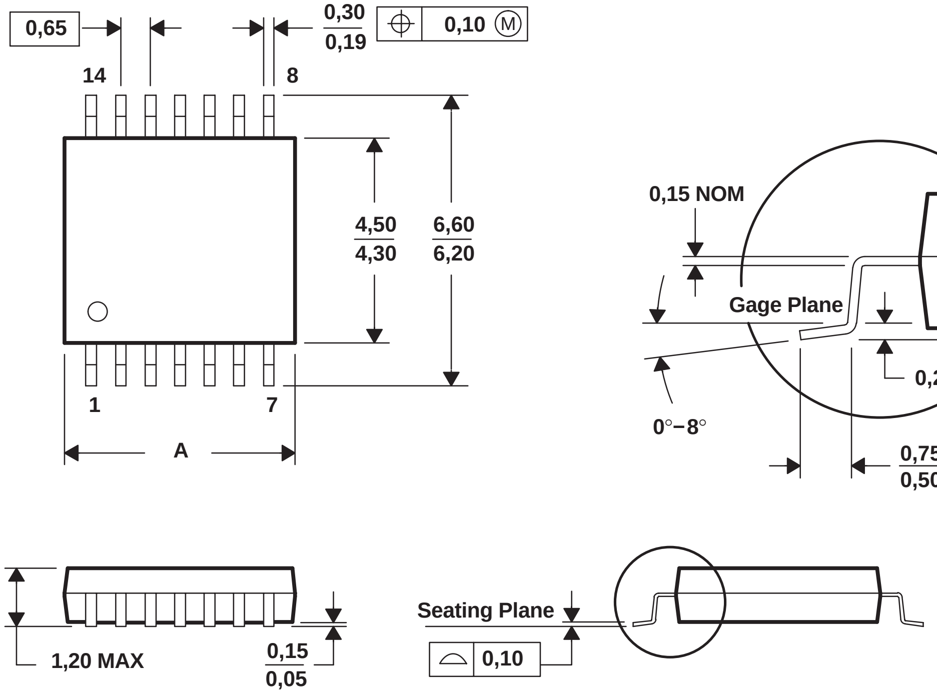
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

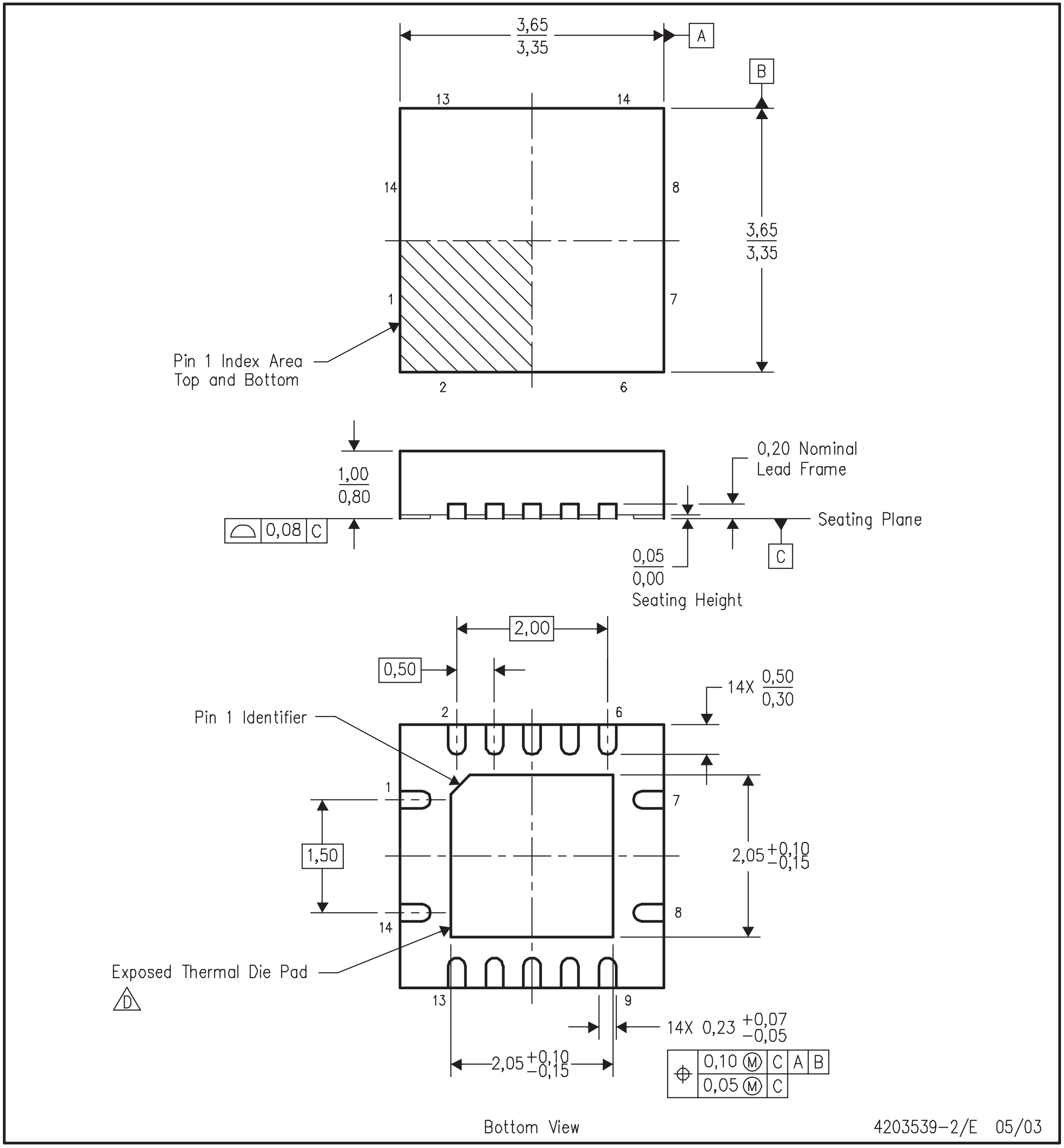

0,65
0,30
0,19
0,10 M
14
8
4,50
4,30
6,60
6,20
1
7
A
0,15 NOM
Gage Plane
0,25
0°−8°
0,75
0,50
1,20 MAX
0,15
0,05
Seating Plane
0,10

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

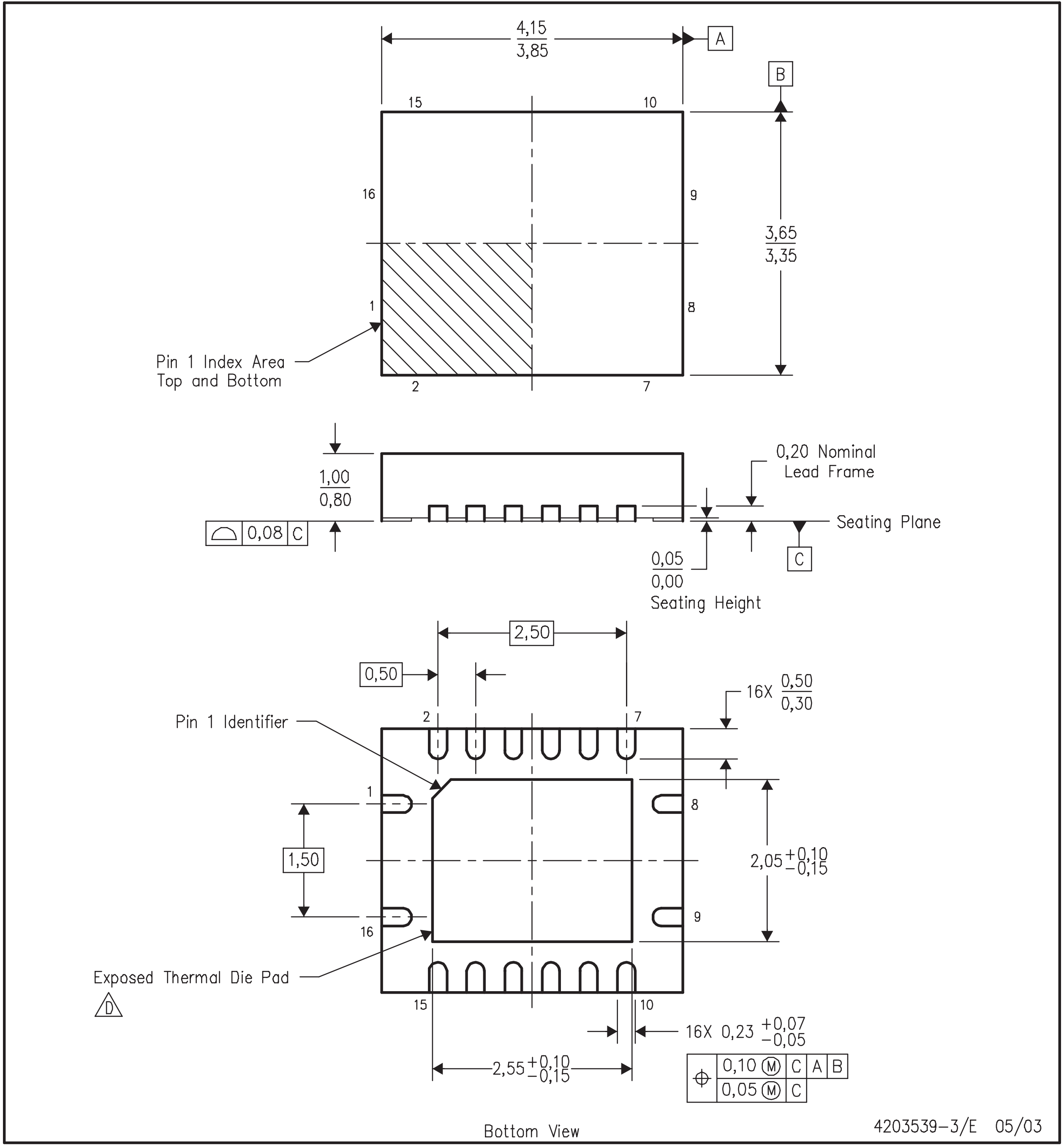
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

RGY (S–PQFP–N14) PLASTIC QUAD FLATPACK


3,65
3,35
A
B
13
14
14
8
3,65
3,35
1
7
Pin 1 Index Area
Top and Bottom
2
6
1,00
0,80
0,08 C
0,20 Nominal
Lead Frame
Seating Plane
C
0,05
0,00
Seating Height
2,00
0,50
14X 0,50
0,30
Pin 1 Identifier
2
6
1
7
1,50
2,05 +0,10 −0,15
8
14
Exposed Thermal Die Pad
D
13
9
14X 0,23 +0,07 −0,05
2,05 +0,10 −0,15
0,10 Ⓜ C A B
0,05 Ⓜ C
Bottom View
4203539–2/E 05/03

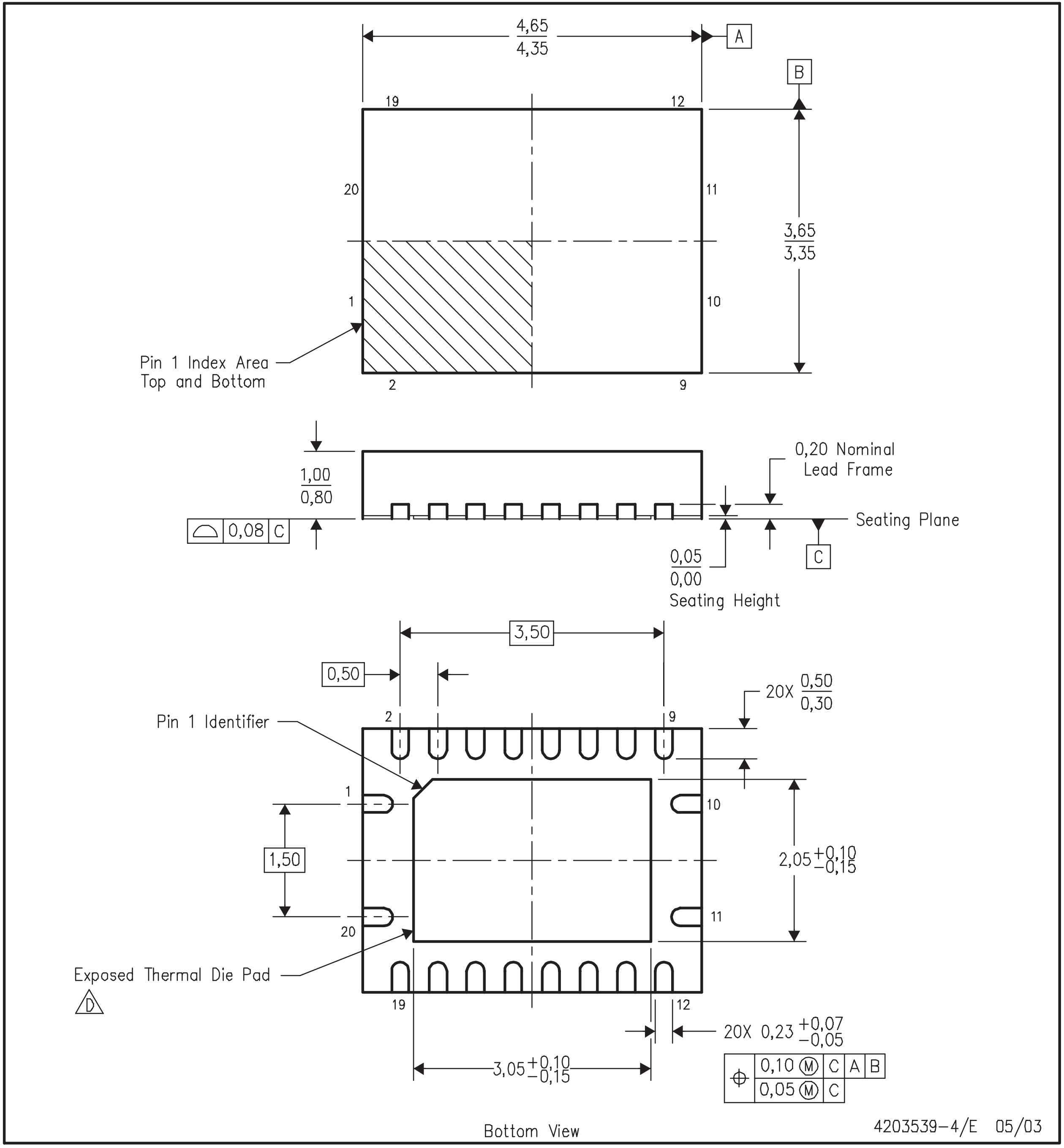
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
- E. Package complies to JEDEC MO–241 variation BA.

RGY (R–PQFP–N16) PLASTIC QUAD FLATPACK


4,15
3,85
A
B
15
10
16
9
1
8
2
7
3,65
3,35
Pin 1 Index Area
Top and Bottom
1,00
0,80
0,08 C
0,20 Nominal
Lead Frame
Seating Plane
C
0,05
0,00
Seating Height
2,50
0,50
16X 0,50
0,30
Pin 1 Identifier
1,50
2,05 +0,10 −0,15
Exposed Thermal Die Pad
D
16X 0,23 +0,07 −0,05
2,55 +0,10 −0,15
0,10 M C A B
0,05 M C
Bottom View
4203539–3/E 05/03

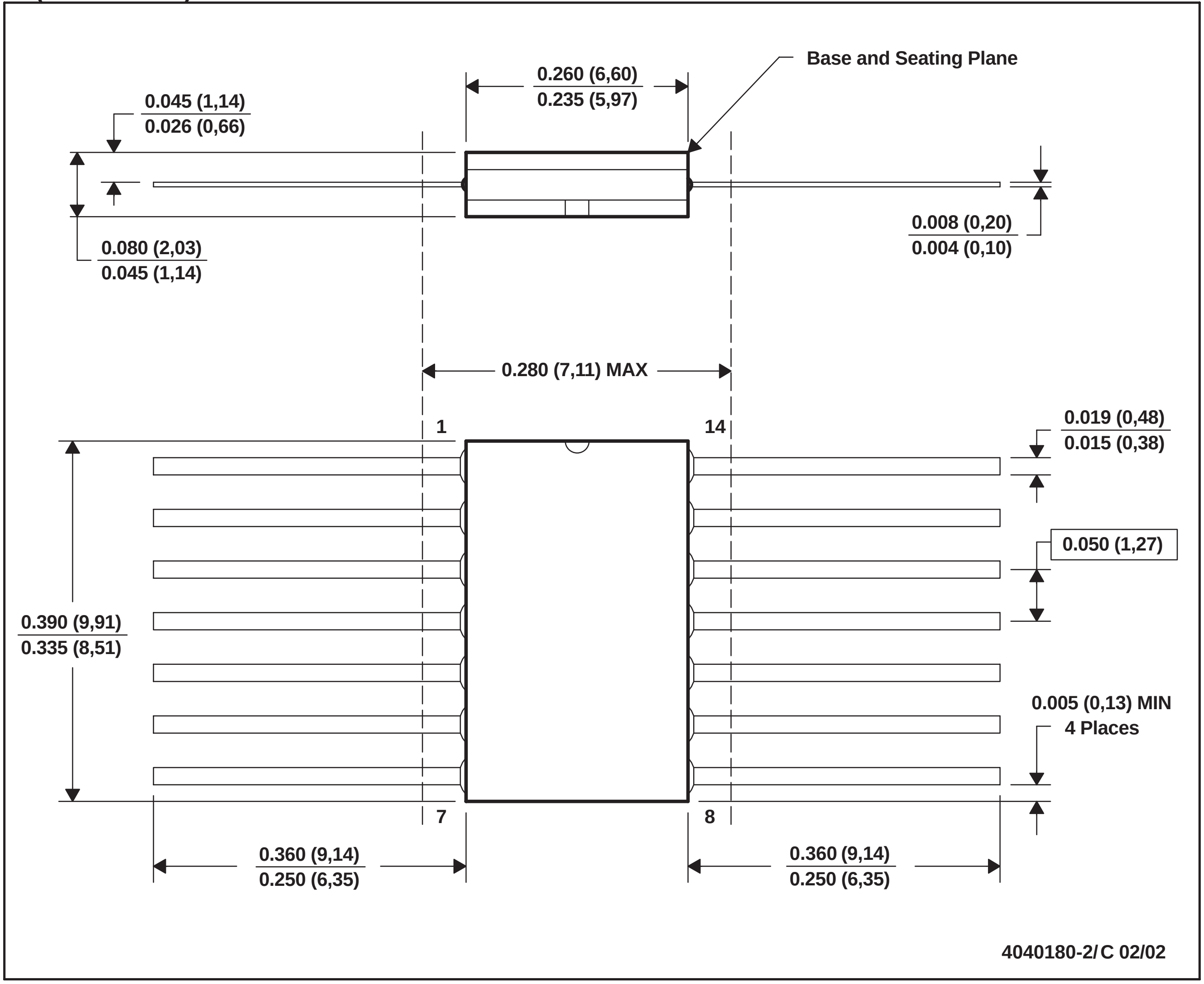
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
- E. Package complies to JEDEC MO–241 variation BB.

RGY (R–PQFP–N20) PLASTIC QUAD FLATPACK


4,65
4,35
A
B
19
12
20
11
3,65
3,35
1
10
Pin 1 Index Area
Top and Bottom
2
9
1,00
0,80
0,08 C
0,20 Nominal
Lead Frame
Seating Plane
C
0,05
0,00
Seating Height
3,50
0,50
20X 0,50 / 0,30
Pin 1 Identifier
2
9
1
10
1,50
2,05 +0,10 −0,15
20
11
Exposed Thermal Die Pad
D
19
12
20X 0,23 +0,07 −0,05
3,05 +0,10 −0,15
0,10 Ⓜ C A B
0,05 Ⓜ C
Bottom View
4203539–4/E 05/03

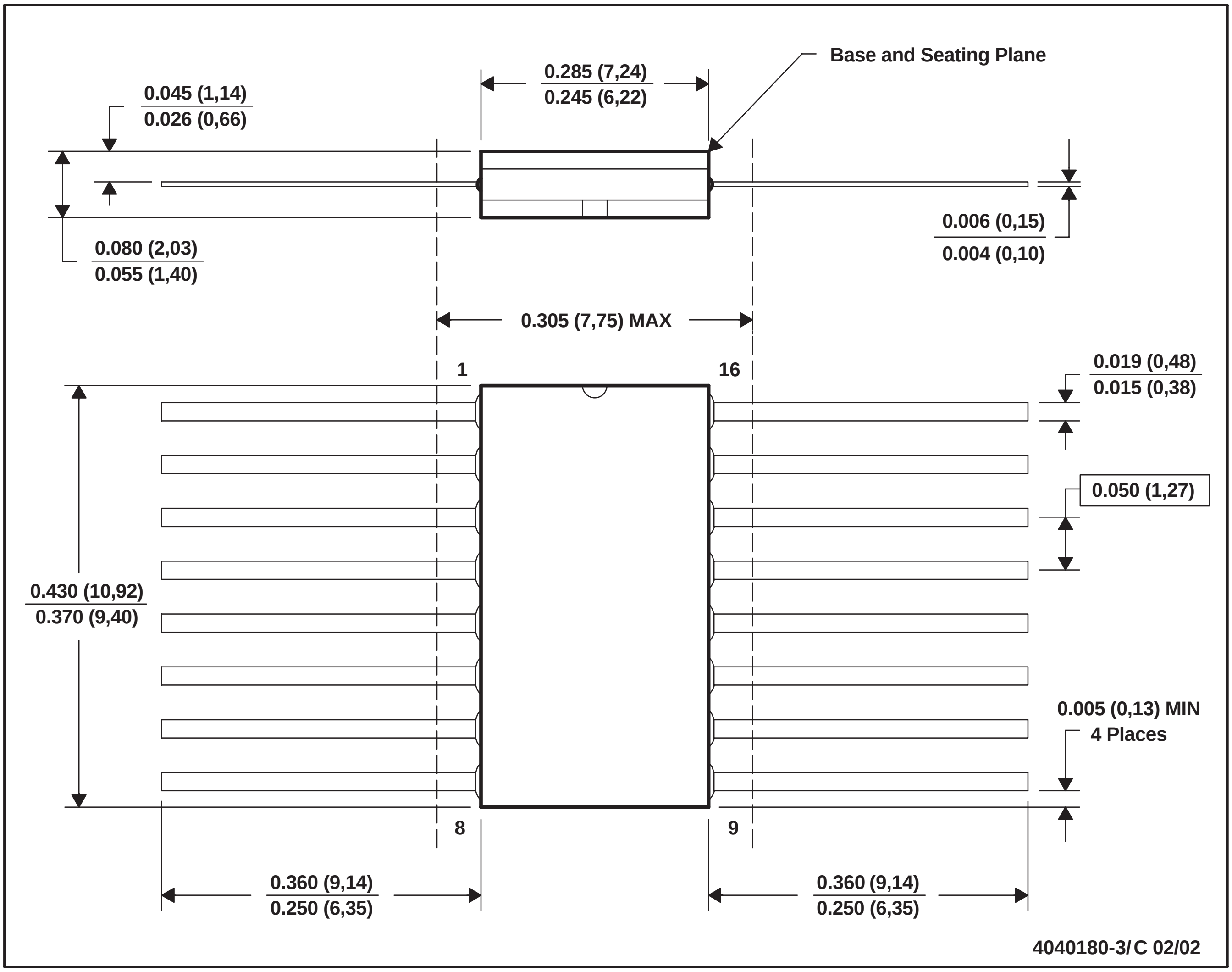
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
- E. Package complies to JEDEC MO–241 variation BC.

W (R-GDFP-F14) **CERAMIC DUAL FLATPACK**


Base and Seating Plane
0.260 (6,60)
0.235 (5,97)
0.045 (1,14)
0.026 (0,66)
0.080 (2,03)
0.045 (1,14)
0.008 (0,20)
0.004 (0,10)
0.280 (7,11) MAX
1
14
0.019 (0,48)
0.015 (0,38)
0.050 (1,27)
0.390 (9,91)
0.335 (8,51)
0.005 (0,13) MIN
4 Places
7
8
0.360 (9,14)
0.250 (6,35)
0.360 (9,14)
0.250 (6,35)
4040180-2/C 02/02

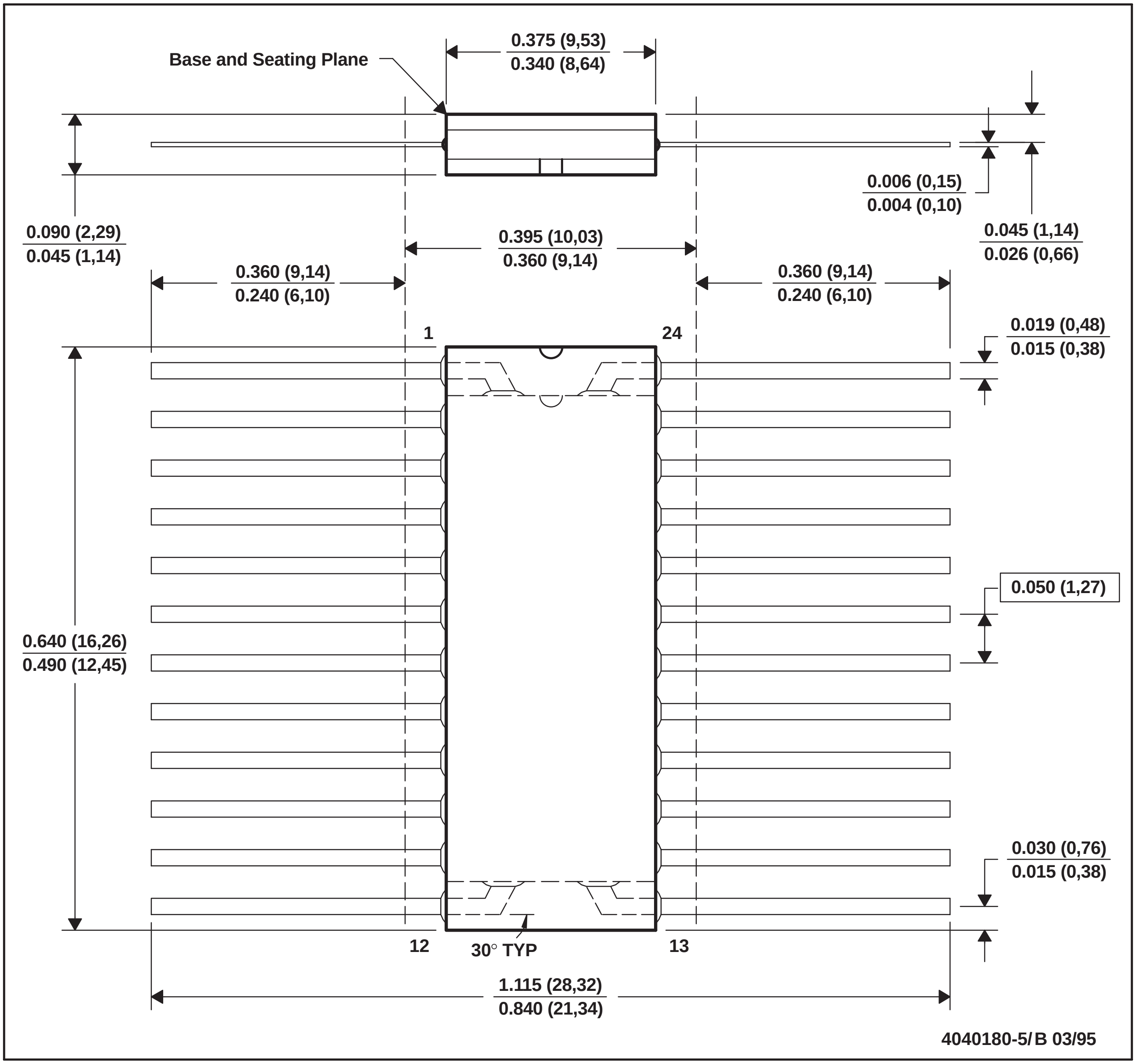
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

W (R-GDFP-F16) **CERAMIC DUAL FLATPACK**


Base and Seating Plane
0.285 (7,24)
0.245 (6,22)
0.045 (1,14)
0.026 (0,66)
0.080 (2,03)
0.055 (1,40)
0.006 (0,15)
0.004 (0,10)
0.305 (7,75) MAX
1
16
8
9
0.019 (0,48)
0.015 (0,38)
0.050 (1,27)
0.430 (10,92)
0.370 (9,40)
0.005 (0,13) MIN
4 Places
0.360 (9,14)
0.250 (6,35)
0.360 (9,14)
0.250 (6,35)
4040180-3/C 02/02

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP-1F16 and JEDEC MO-092AC

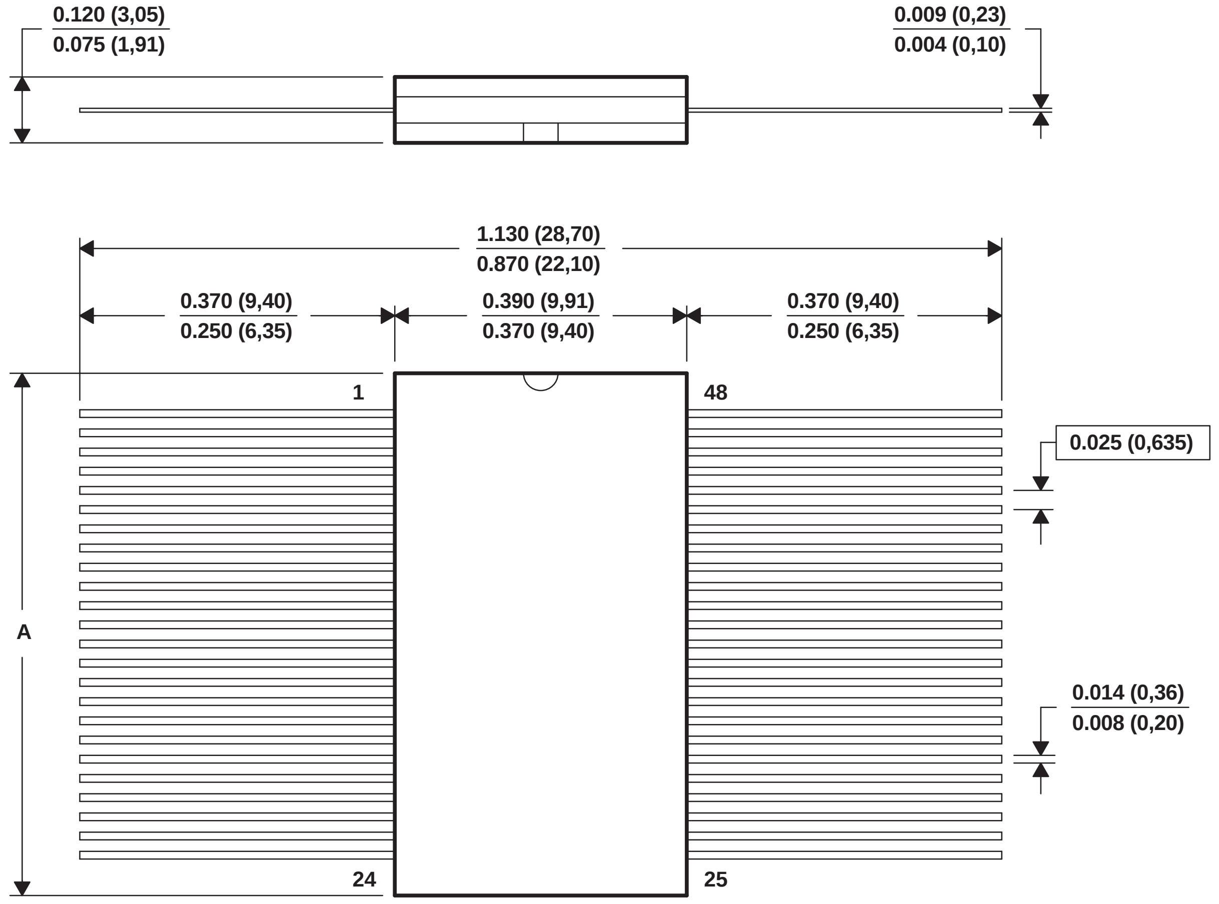
W (R-GDFP-F24) CERAMIC DUAL FLATPACK


Base and Seating Plane
0.375 (9,53)
0.340 (8,64)
0.090 (2,29)
0.045 (1,14)
0.006 (0,15)
0.004 (0,10)
0.045 (1,14)
0.026 (0,66)
0.395 (10,03)
0.360 (9,14)
0.360 (9,14)
0.240 (6,10)
0.360 (9,14)
0.240 (6,10)
1
24
0.019 (0,48)
0.015 (0,38)
0.050 (1,27)
0.640 (16,26)
0.490 (12,45)
0.030 (0,76)
0.015 (0,38)
12
30° TYP
13
1.115 (28,32)
0.840 (21,34)
4040180-5/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
E. Index point is provided on cap for terminal identification only.

WD (R-GDFP-F**) CERAMIC DUAL FLATPACK

48 LEADS SHOWN

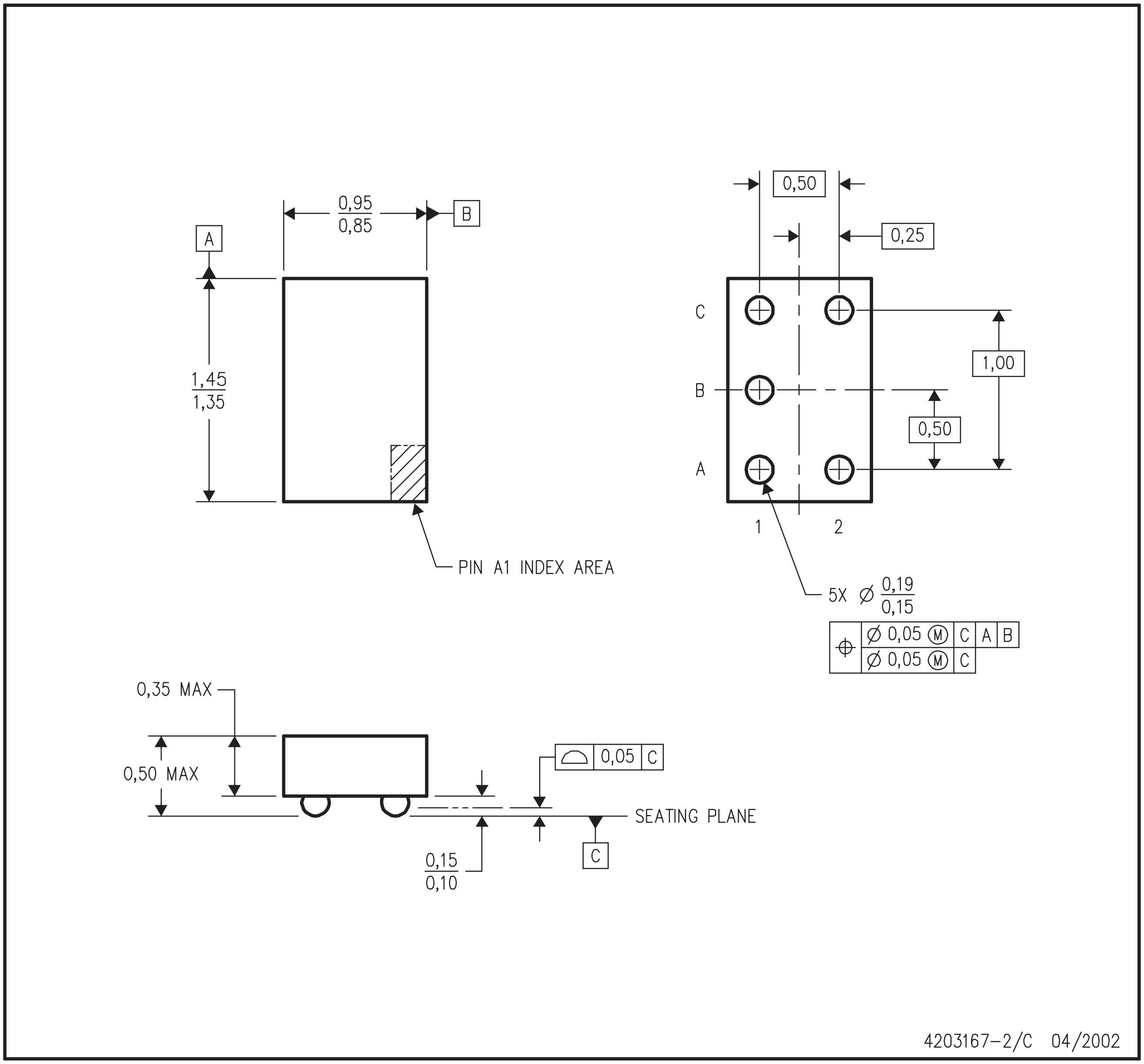

0.120 (3,05)
0.075 (1,91)
0.009 (0,23)
0.004 (0,10)
1.130 (28,70)
0.870 (22,10)
0.370 (9,40)
0.250 (6,35)
0.390 (9,91)
0.370 (9,40)
0.370 (9,40)
0.250 (6,35)
1
48
0.025 (0,635)
A
0.014 (0,36)
0.008 (0,20)
24
25

NO. OF LEADS**	48	56
A MAX	0.640 (16,26)	0.740 (18,80)
A MIN	0.610 (15,49)	0.710 (18,03)

4040176/D 10/97

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only
- E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
  GDFP1-F56 and JEDEC MO-146AB

YEA (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY


0,95
0,85
B
A
1,45
1,35
PIN A1 INDEX AREA
0,50
0,25
C
B
A
1
2
1,00
0,50
5X Ø 0,19
0,15
Ø 0,05 Ⓜ C A B
Ø 0,05 Ⓜ C
0,35 MAX
0,50 MAX
0,05 C
SEATING PLANE
0,15
0,10
C
4203167–2/C 04/2002

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoStar™ package configuration.
- D. Package complies to JEDEC MO–211 variation EA.
- E. This package is tin–lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead–free.

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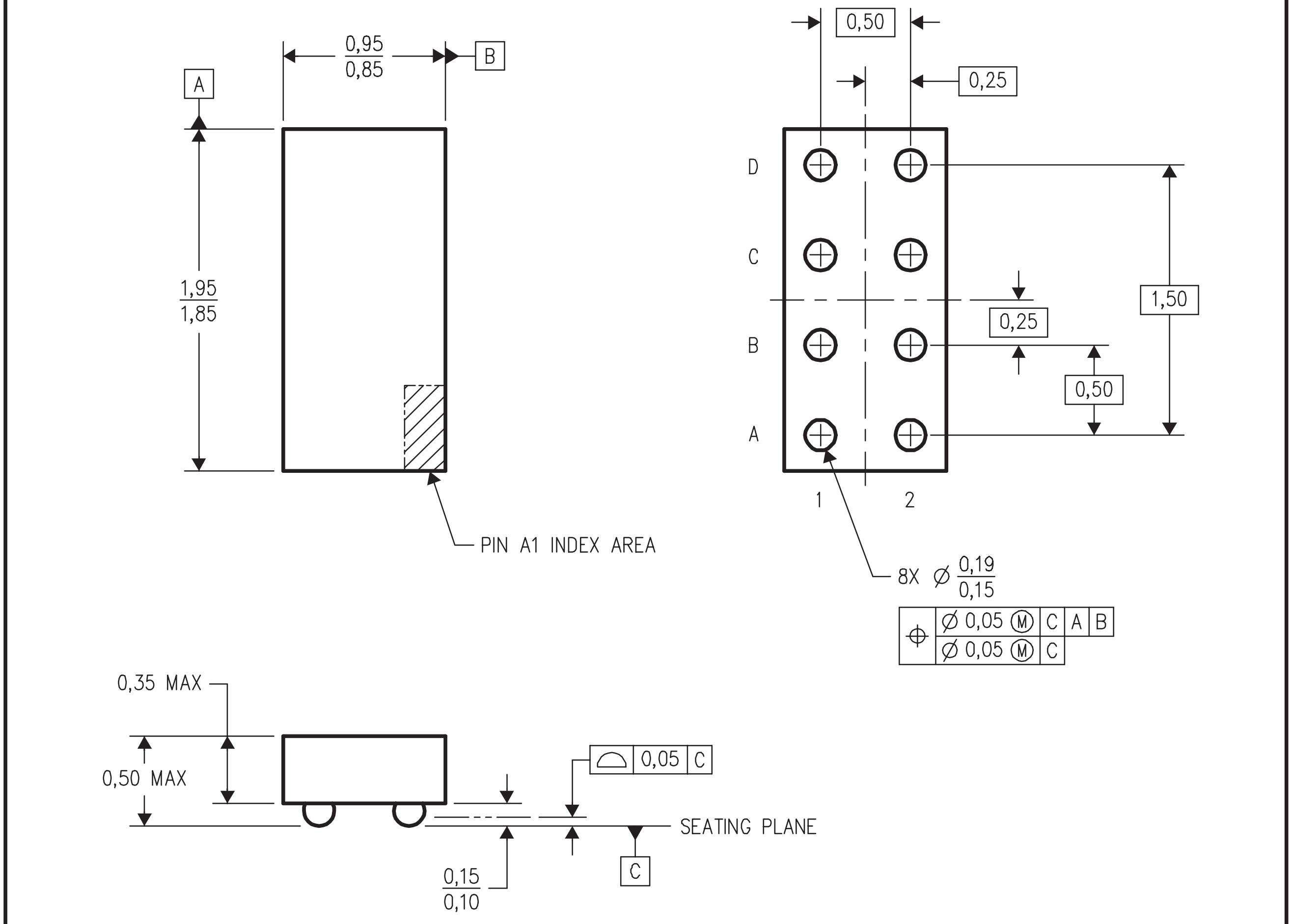
YEA (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY

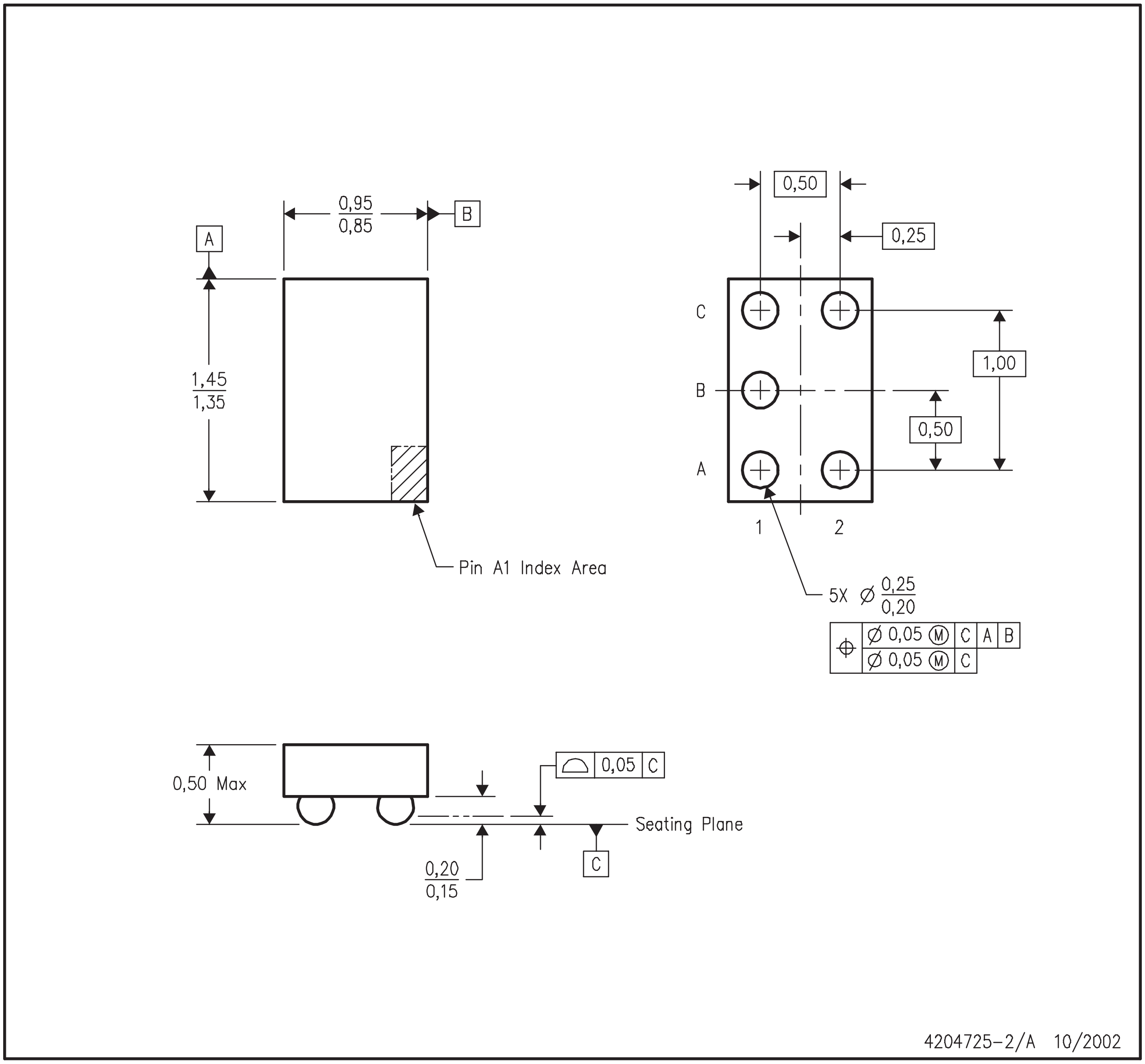

0,95
0,85
B
A
1,95
1,85
PIN A1 INDEX AREA
0,50
0,25
D
C
B
A
1
2
0,25
0,50
1,50
8X Ø 0,19 0,15
Ø 0,05 Ⓜ C A B
Ø 0,05 Ⓜ C
0,35 MAX
0,50 MAX
0,05 C
SEATING PLANE
C
0,15
0,10

4203167–4/C 04/2002

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoStar™ package configuration.
- D. Package complies to JEDEC MO–211 variation EB.
- E. This package is tin–lead (SnPb). Refer to the 8 YZA package (drawing 4204151) for lead–free.

NanoStar is a trademark of Texas Instruments.

YEP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY

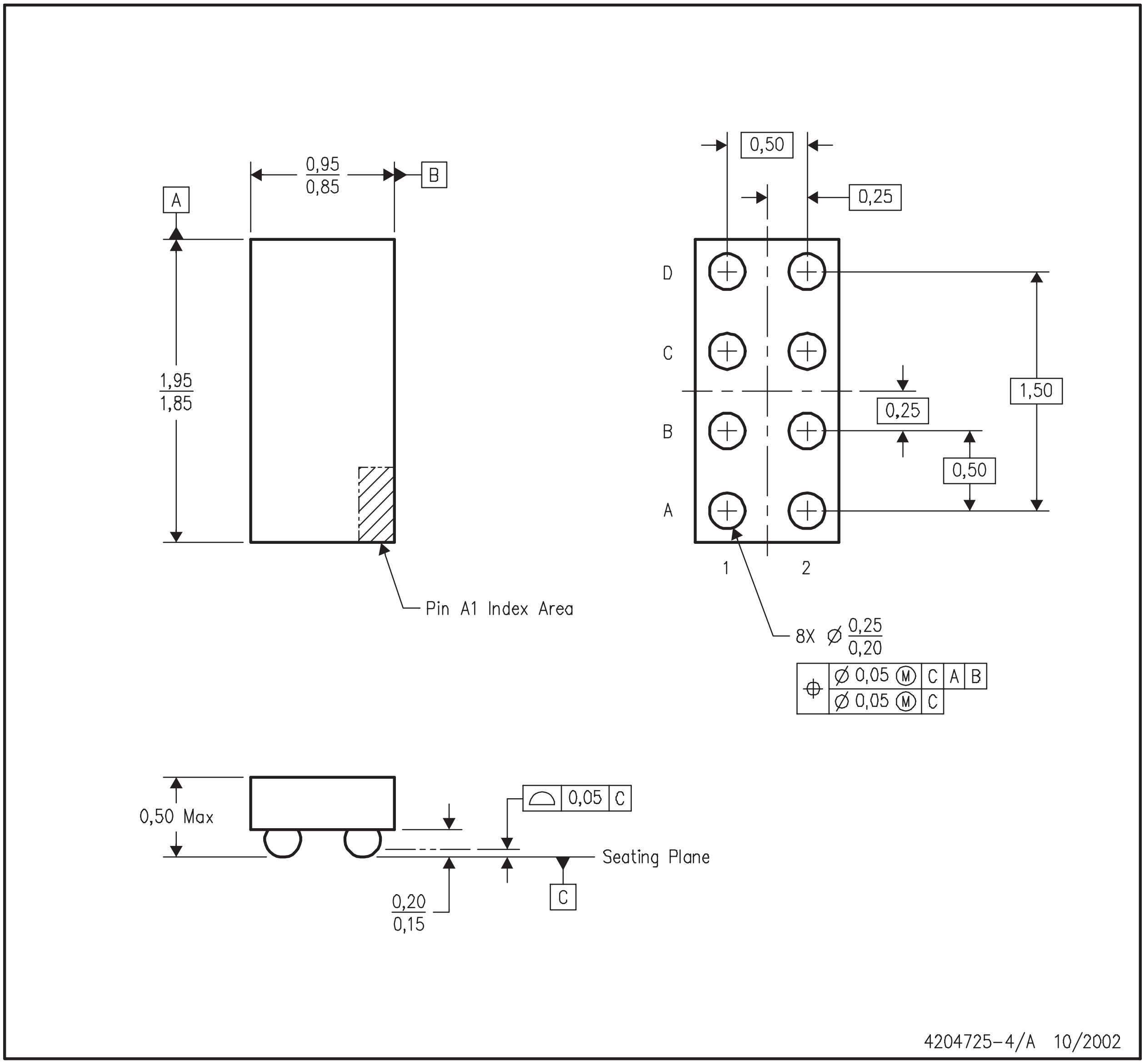


0,95
0,85
B
A
1,45
1,35
Pin A1 Index Area
0,50
0,25
C
B
A
1
2
1,00
0,50
5X Ø 0,25 0,20
Ø 0,05 Ⓜ C A B
Ø 0,05 Ⓜ C
0,50 Max
0,05 C
Seating Plane
C
0,20
0,15
4204725–2/A 10/2002

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoStar™ package configuration.
- D. This package is tin–lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead–free.

NanoStar is a trademark of Texas Instruments.

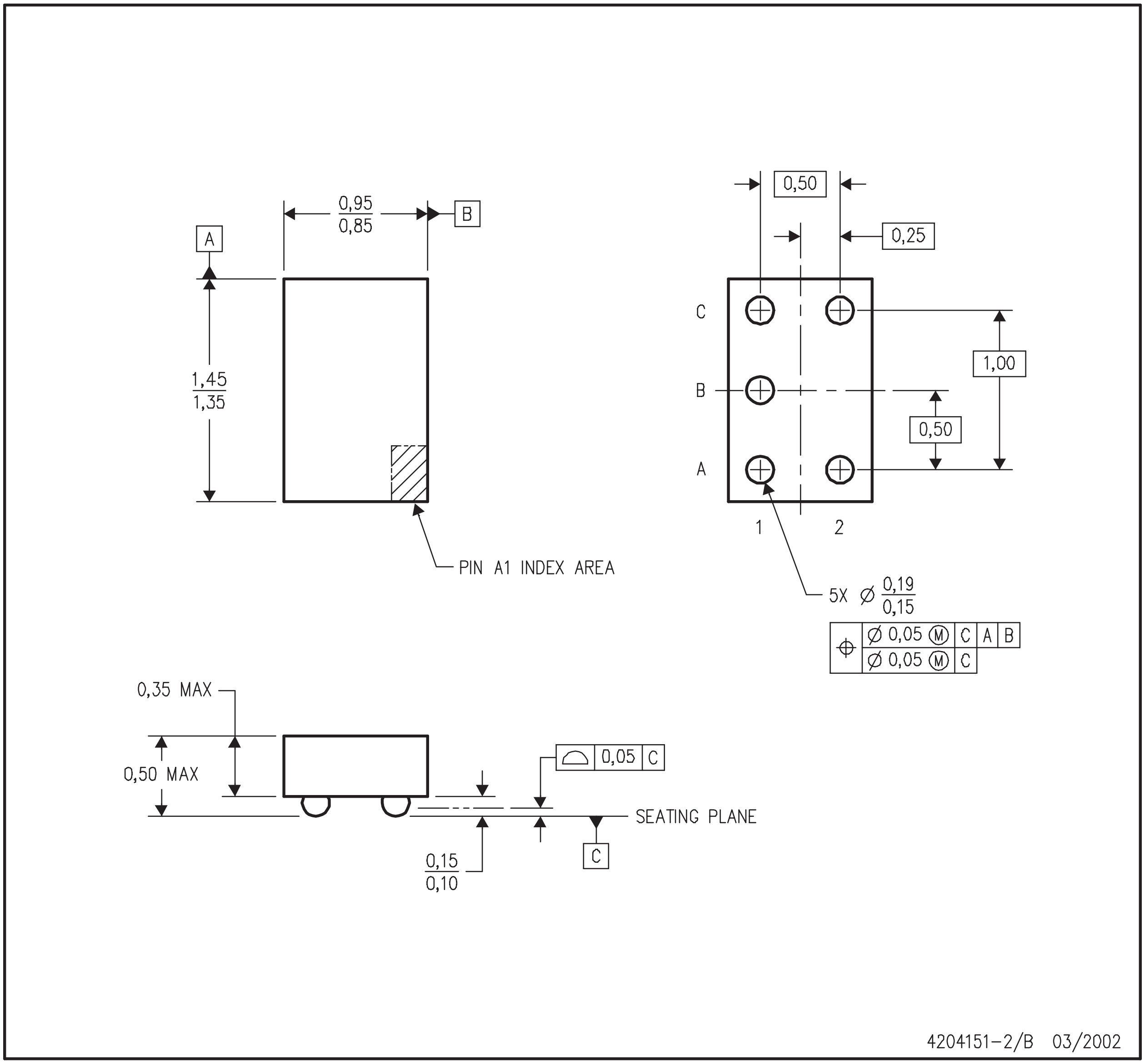
YEP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY


0,95
0,85
B
A
1,95
1,85
Pin A1 Index Area
0,50
0,25
D
C
B
A
1
2
0,25
1,50
0,50
8X Ø 0,25
0,20
Ø 0,05 Ⓜ C A B
Ø 0,05 Ⓜ C
0,50 Max
0,05 C
Seating Plane
C
0,20
0,15
4204725-4/A 10/2002

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoStar™ package configuration.
- D. This package is tin–lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead–free.

NanoStar is a trademark of Texas Instruments.

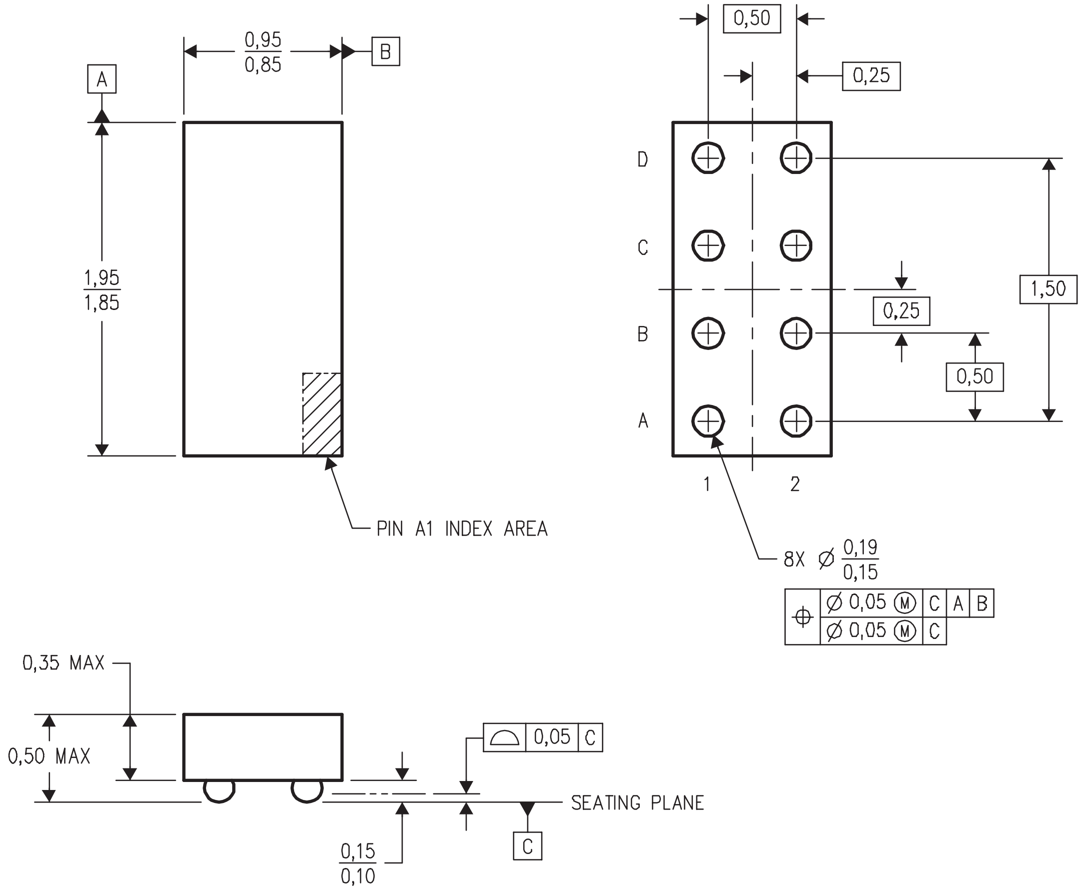
YZA (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY


0,95
0,85
B
A
1,45
1,35
PIN A1 INDEX AREA
0,50
0,25
C
B
A
1
2
1,00
0,50
5X ∅ 0,19
0,15
∅ 0,05 Ⓜ C A B
∅ 0,05 Ⓜ C
0,35 MAX
0,50 MAX
0,05 C
SEATING PLANE
0,15
0,10
C
4204151–2/B 03/2002

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Package complies to JEDEC MO–211 variation EA.
E. This package is lead–free. Refer to the 5 YEA package (drawing 4203167) for tin–lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YZA (R-XBGA-N8) DIE-SIZE BALL GRID ARRAY

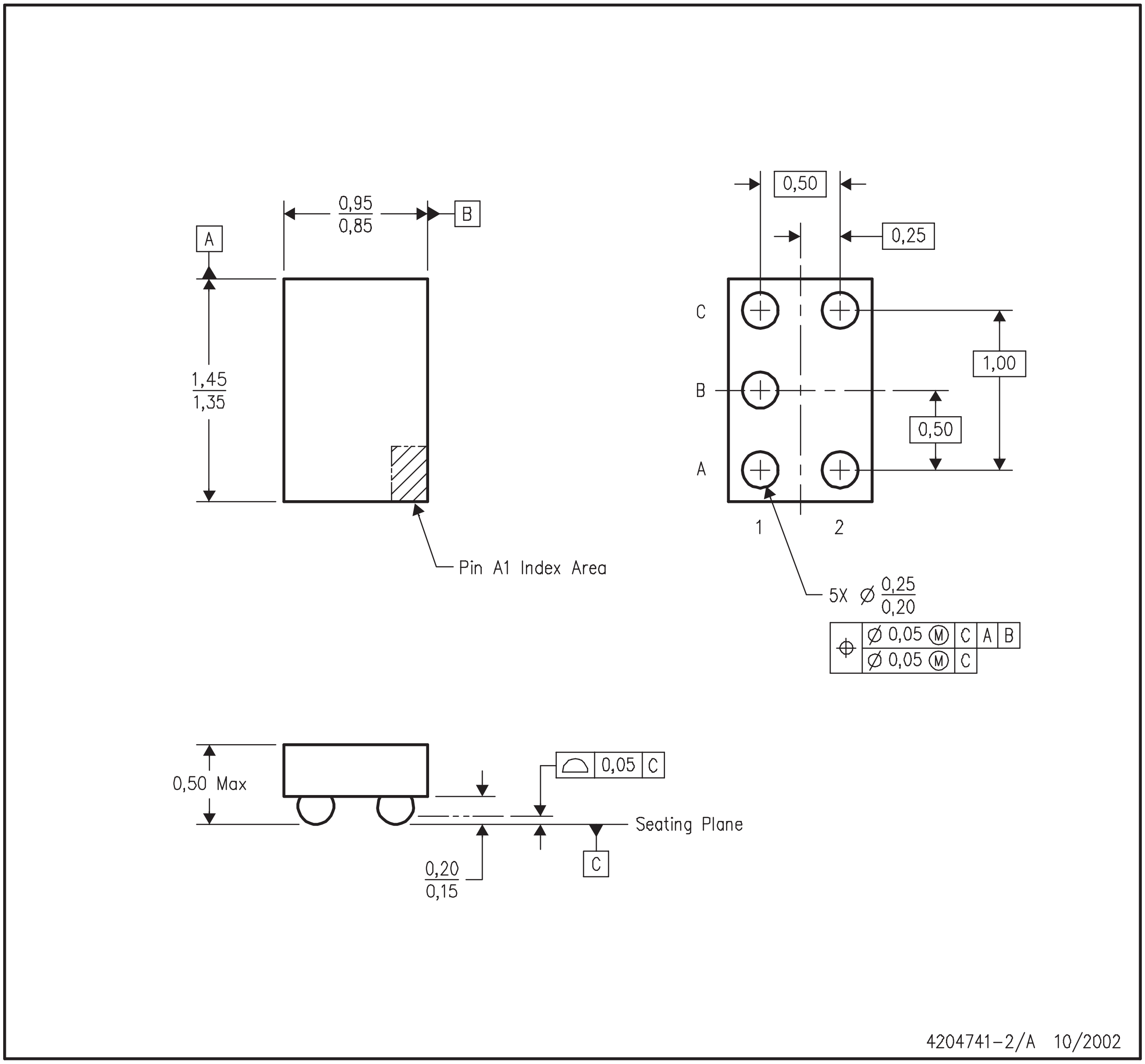

A
0,95
0,85
B
1,95
1,85
PIN A1 INDEX AREA
0,50
0,25
D
C
B
A
1
2
0,25
0,50
1,50
8X Ø 0,19
0,15
Ø 0,05 Ⓜ C A B
Ø 0,05 Ⓜ C
0,35 MAX
0,50 MAX
0,05 C
SEATING PLANE
C
0,15
0,10

4204151-4/B 03/2002

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. Package complies to JEDEC MO-211 variation EB.
- E. This package is lead-free. Refer to the 8 YEA package (drawing 4203167) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YZP (R-XBGA-N5) DIE-SIZE BALL GRID ARRAY

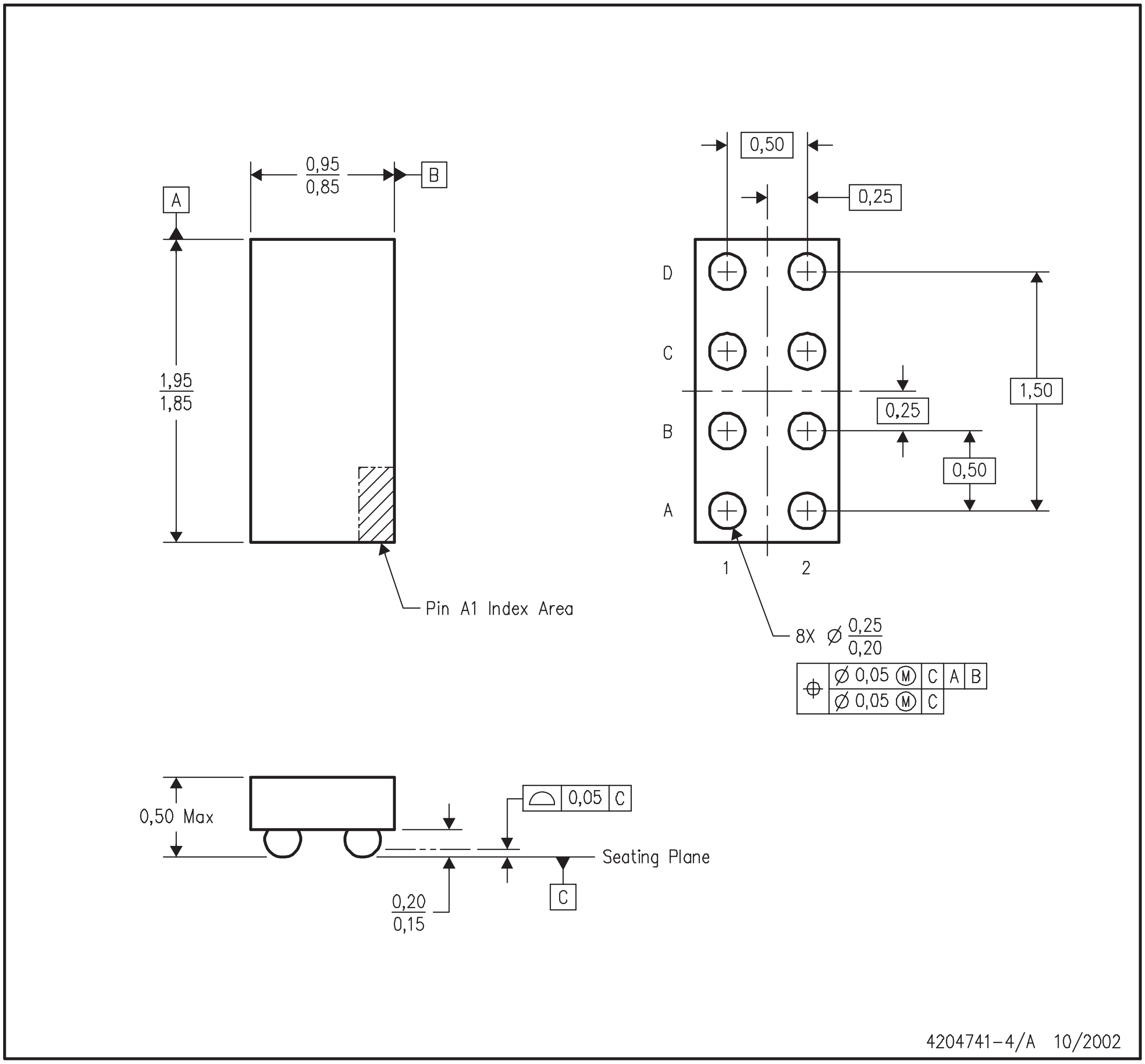


0,95
0,85
B
A
1,45
1,35
Pin A1 Index Area
0,50
0,25
C
B
A
1
2
1,00
0,50
5X Ø 0,25 0,20
Ø 0,05 Ⓜ C A B
Ø 0,05 Ⓜ C
0,50 Max
0,05 C
Seating Plane
0,20
0,15
C
4204741-2/A 10/2002

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

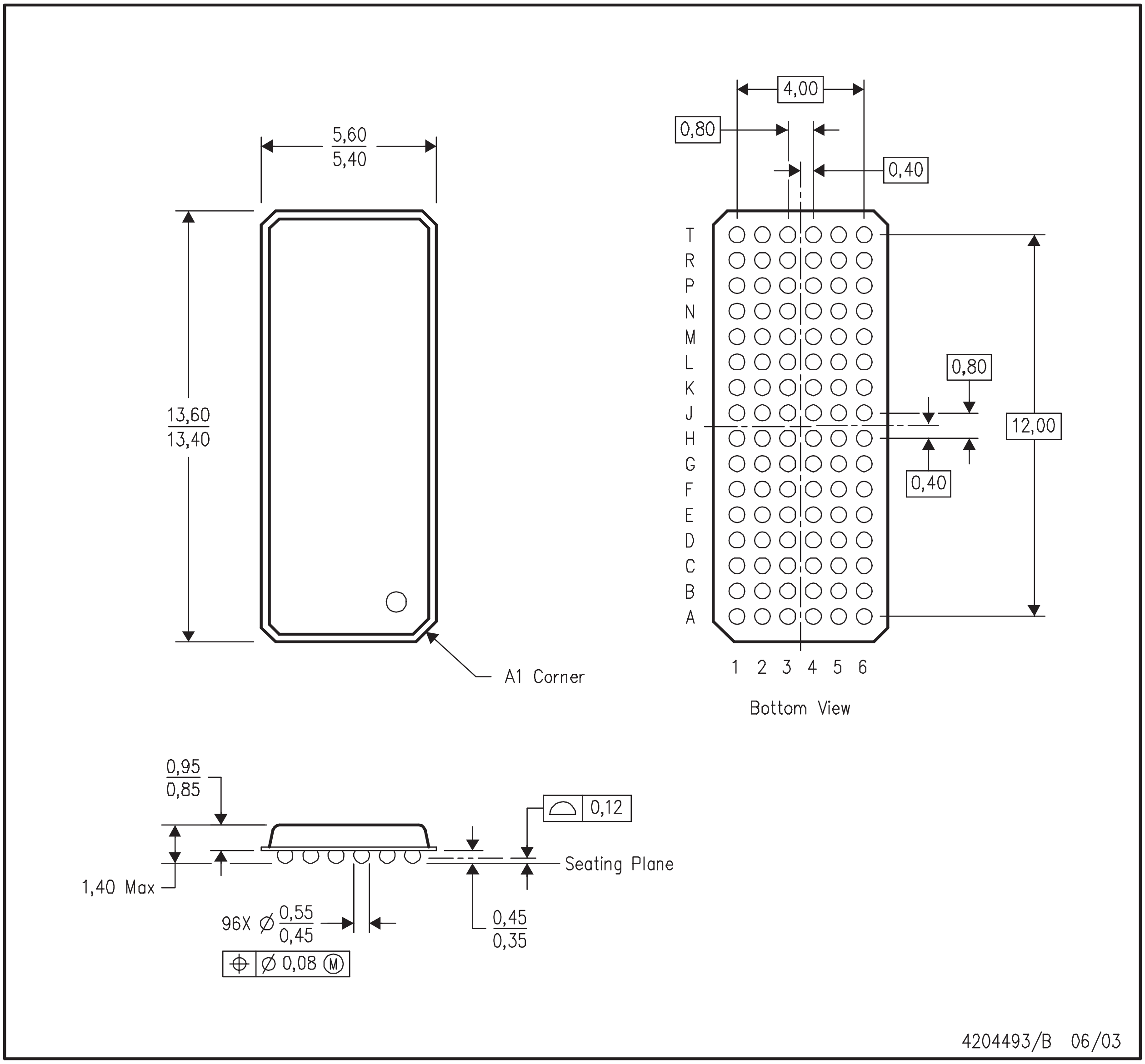
YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY


0,95
0,85
B
A
1,95
1,85
Pin A1 Index Area
0,50
0,25
D
C
B
A
1
2
0,25
1,50
0,50
8X Ø 0,25
0,20
Ø 0,05 Ⓜ C A B
Ø 0,05 Ⓜ C
0,50 Max
0,05 C
Seating Plane
C
0,20
0,15
4204741–4/A 10/2002

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. This package is lead–free. Refer to the 8 YEP package (drawing 4204725) for tin–lead (SnPb).

NanoFree is a trademark of Texas Instruments.

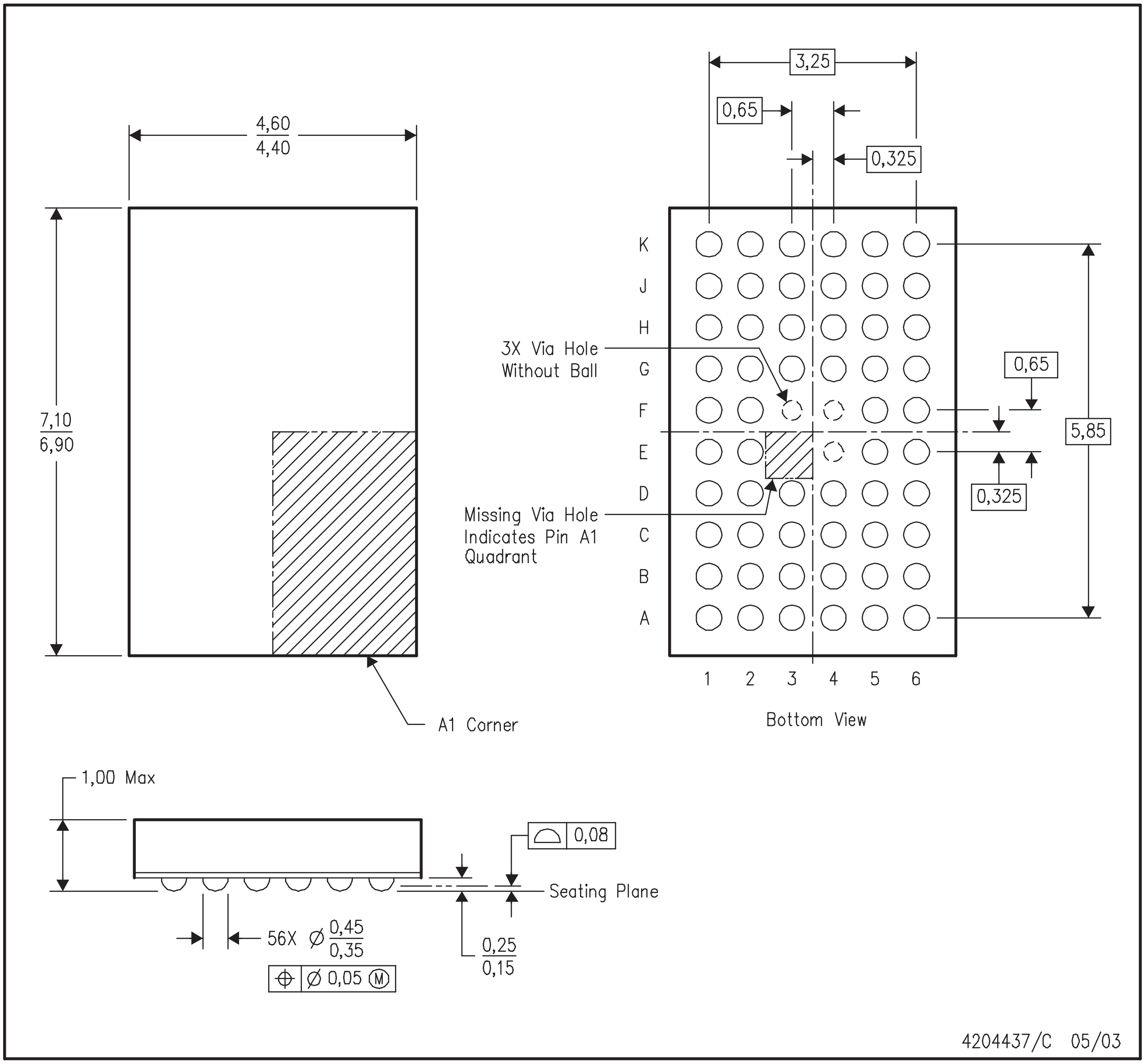
ZKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY


5,60
5,40
13,60
13,40
A1 Corner
4,00
0,80
0,40
T
R
P
N
M
L
K
J
H
G
F
E
D
C
B
A
0,80
12,00
0,40
1 2 3 4 5 6
Bottom View
0,95
0,85
0,12
Seating Plane
1,40 Max
96X Ø 0,55
0,45
0,45
0,35
Ø 0,08 Ⓜ
4204493/B 06/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar BGA™ configuration
- D. Falls within JEDEC MO–205 variation CC.
- E. This package is lead–free. Refer to the 96 GKE package (drawing 4188953) for tin–lead (SnPb).

MicroStar BGA is a trademark of Texas Instruments.

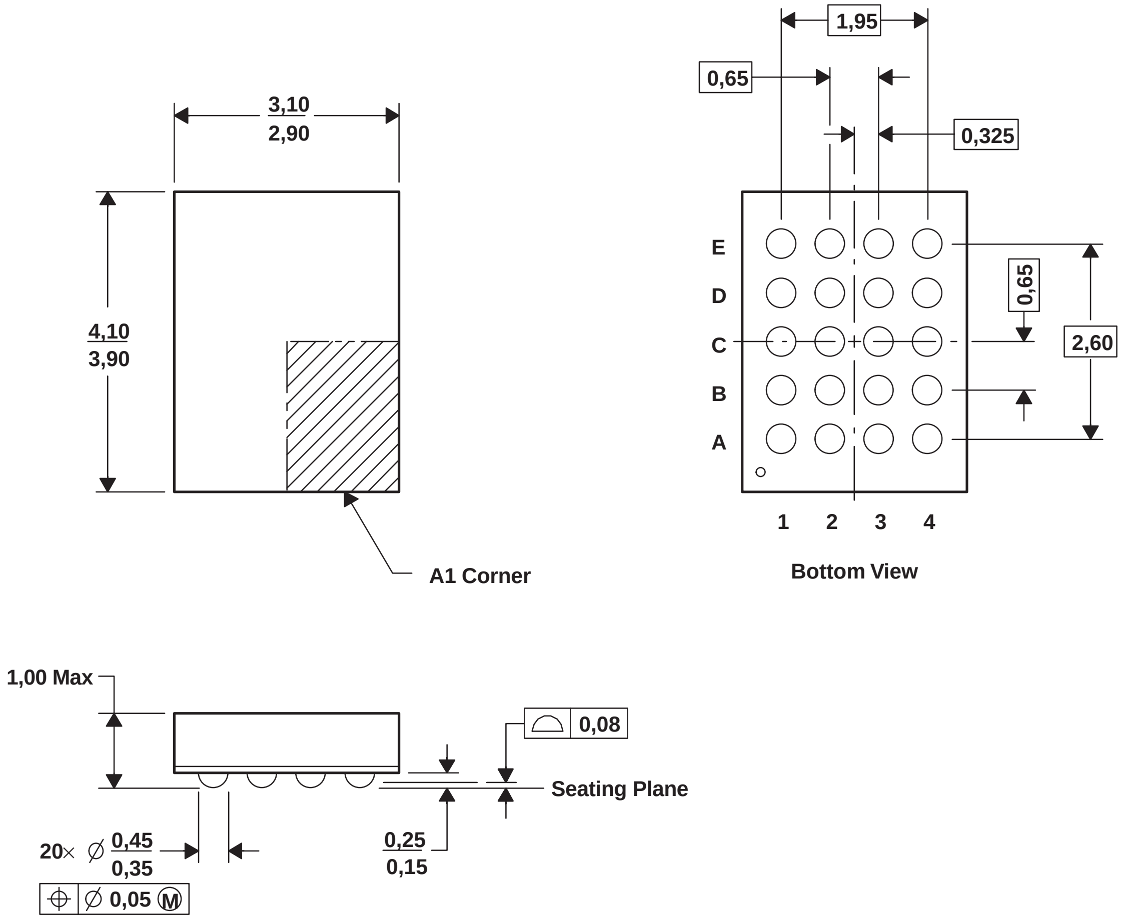
ZQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY


4,60
4,40
7,10
6,90
A1 Corner
3,25
0,65
0,325
K
J
H
G
F
E
D
C
B
A
1 2 3 4 5 6
3X Via Hole Without Ball
Missing Via Hole Indicates Pin A1 Quadrant
0,65
5,85
0,325
Bottom View
1,00 Max
0,08
Seating Plane
56X Ø 0,45
0,35
Ø 0,05 Ⓜ
0,25
0,15
4204437/C 05/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar Junior™ BGA configuration.
- D. Falls within JEDEC MO–225 variation BA.
- E. This package is lead–free. Refer to the 56 GQL package (drawing 4200583) for tin–lead (SnPb).

MicroStar Junior is a trademark of Texas Instruments.

ZQN (R-PBGA-N20) PLASTIC BALL GRID ARRAY


3,10
2,90
4,10
3,90
A1 Corner
1,95
0,65
0,325
E
D
C
B
A
0,65
2,60
1
2
3
4
Bottom View
1,00 Max
0,08
Seating Plane
20× ∅ 0,45
0,35
∅ 0,05 Ⓜ
0,25
0,15

4204492/A 06/2002

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ configuration.
D. Fall within JEDEC MO-225 variation BC.
E. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead)SnPb).

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