Live Insertion

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Abstract

In many current applications, there is a requirement to exchange modules in electronic systems while the supply voltage remains on. This procedure is commonly known as live insertion. To understand this requirement, consider the case of an electronic telephone exchange in which replacing modules for maintenance or repair must be possible at any time without interrupting the operation of the system. To avoid damage to components, and any interruption of operation when changing modules in this way, additional circuitry modifications are necessary.

This report describes the phenomena that occur during live insertion, then presents circuit proposals to solve the potential problems that might otherwise arise.

1 Introduction

For many years, diverse functions and processes have been monitored and controlled successfully by electronic systems. The advantages of electronic controls in such cases (compared with manual or mechanical controls) are lower operating costs and the improved reliability that electronics now provide. However, faults also can arise in such electronic systems, which then require repair. By using modular construction for the equipment, it is possible to quickly exchange a defective module and clear the fault.

With most equipment, it is necessary to switch off the supply voltage during the exchange of the modules to avoid incorrect operation or destruction of components. In many cases–an obvious example is the computer in an office–the exchange of modules while the equipment is turned off is permissible.

In many electronic systems, switching off the equipment to exchange a defective module is unacceptable. Examples include an electronic telephone exchange, the switching control center of an electric utility, or the computer that processes data in the air-traffic control center of an airport. In all of these cases, when a fault is found in a module, exchanging this module in a running system without disturbing or otherwise compromising the rest of the system functions must be possible.

The engineer planning and developing electronic systems for such applications must consider the operating states that can arise and meet these requirements by choosing appropriate components and circuitry layout.

A distinction must be made at this point between two different cases. In the first, it is necessary only to ensure that a module or a part of the installation can be exchanged during operation without switching off the system and without damaging it. In such cases, it can be acceptable (for reasons described later) that the operation of the equipment is disturbed. An example is the installation or exchange of a printer for an operating office computer. The primary requirement is the simple and safe operation of the entire system; in this case, the requirements can be fulfilled by choosing appropriate components for the interfaces.

In the second case, the additional requirement must be met that, during exchange of the modules, the components involved should neither be damaged, nor should the operation be disturbed. To ensure this, beside choosing the appropriate components, the development engineer also must incorporate additional circuit modifications to allow continuous and reliable operation of the system.

This applications report provides the development engineer with suggestions for fulfilling these requirements. The report begins with the choice of the most appropriate components for the application, and continues with a description of circuit modifications that are necessary under the operating conditions described.

2 Internal Construction of Integrated Circuits

Some knowledge of the internal construction of integrated circuits is necessary to develop a system in which successful live insertion during operation is possible. It is less important to have a detailed knowledge of the internal circuit construction of the device than to know what information, in addition to that contained in data sheets, must be considered. In this case, protection circuits at the inputs and outputs are particularly important (for example, those for protection against destruction as a result of electrostatic discharge), together with the parasitic diodes in these parts of the circuit. The latter are determined by the internal construction of the circuits and by the characteristics that result from the production process.

In general, the structure of integrated circuits can be represented as shown in Figure 1. This simplified representation shows basic features of integrated circuits. An understanding of these features is necessary for proper understanding of the problems discussed in this report.

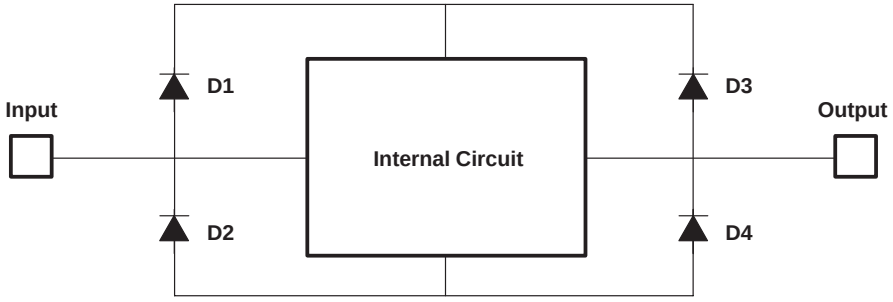

Figure 1. Diodes in the Inputs and Outputs of Integrated Circuits

The diodes shown in Figure 1 have the following functions:

- D1: This diode is integrated into most CMOS circuits for ESD protection. It is intended to limit positive voltages at the input of the circuit. This diode is not included in ABT, LVT, LVC, or AHC/AHCT devices.
- D2: This is a parasitic diode that is predetermined as a result of the internal construction of the semiconductor circuit. With digital circuits, an additional (lower-resistance) diode is intentionally integrated into the chip to limit undershoot of the input signals arising from line reflections. This diode also provides some protection from an electrostatic discharge.
- D3: This diode protects CMOS circuits against destruction as a result of electrostatic discharges. Most bipolar devices have a parasitic diode at this point as a result of the internal construction of the semiconductor. An exception is bipolar devices with an open-collector or 3-state output. With these devices, special modifications to the circuit ensure that this diode is not present and that this current path always remains at a high resistance.
- D4: This diode is present in all digital circuits. In most cases, it is the collector-substrate or drain-substrate diode of the lower-output transistor. With bipolar devices, an additional diode (a Schottky diode) is often integrated into the chip to limit undershoot arising from line reflections. With CMOS circuits, additional ESD-protection diodes are often incorporated.

Table 1. Internal Diodes and Withstanding Voltages of Logic Circuit Inputs and Outputs

	INPUT D1	TOTEM-POLE OUTPUT D3	OPEN-CIRCUIT COLLECTOR OUTPUT D3	3-STATE OUTPUT D3	POWER-UP 3-STATE CIRCUIT
SN7400	5.5 V	7 V	7 V	V_{CC} + 0.5 V	No
SN74LS	7 V	V_{CC} + 0.5 V	7 V	5.5 V	No
SN74S	5.5 V	V_{CC} + 0.5 V	7 V	5.5 V	No
SN74F	7 V	V_{CC} + 0.5 V	7 V	5.5 V	No
SN74ALS	7 V	V_{CC} + 0.5 V	7 V	5.5 V	No
SN74AS	7 V	V_{CC} + 0.5 V	7 V	5.5 V	No
SN74BCT	7 V	–	5.5 V	5.5 V	Yes
SN74ABT	7 V	–	–	5.5 V	Yes
SN74LVT	7 V		–	5.5 V	Yes
SN74HC	V_{CC} + 0.5 V	V_{CC} + 0.5 V	V_{CC} + 0.5 V	V_{CC} + 0.5 V	No
SN74AC	V_{CC} + 0.5 V	V_{CC} + 0.5 V	–	V_{CC} + 0.5 V	No
SN74LV	V_{CC} + 0.5 V	V_{CC} + 0.5 V	V_{CC} + 0.5 V	V_{CC} + 0.5 V	No
SN74LVC	7 V	V_{CC} + 0.5 V	–	5.5 V	No
SN74ALVC	4.6 V	–	–	V_{CC} + 0.5 V	No
SN74AHC	7 V	V_{CC} + 0.5 V	–	V_{CC} + 0.5 V	No
SN74AHCT	7 V	V_{CC} + 0.5 V	–	V_{CC} + 0.5 V	No

When changing modules with the supply voltage switched on, the voltages that are permissible to apply to the input and output components of the interfaces are of particular interest, as well as voltages at the interfaces with the supply voltage switched off. There are a large number of circuit variants and diverse logic functions. Table 1 provides development engineers with an overview of the voltages that can be applied to the terminals of various integrated circuits.

With devices that have diodes D1 and/or D3, a maximum voltage can be applied to the inputs and outputs that are 0.5 V more positive than the instantaneous V_{CC}. In Table 1, this is given as a maximum value of V_{CC} + 0.5 V. At higher voltages, these diodes become conducting. In this case, if there is no current limiting, the possibility of an overload or the destruction of the device must be accepted. If there are no diodes at this point, a voltage can be applied to the appropriate terminal, depending on the breakdown voltage of the transistors in the corresponding part of the circuit, independently of the instantaneous supply voltage. That is, when V_{CC} = 0. The permissible values of voltage are given in Table 1.

BiCMOS circuits also incorporate a power-up 3-state circuit. This circuit consists of a simple voltage-monitoring circuit (see Figure 2) in which V_{CC} is measured by diodes D1 and D2 and with the base-emitter voltage of transistor Q1. Below a certain supply voltage $V_{CC(off)}$ (ABT/BCT: $V_{CC(off)} \approx 2.5$ V; LVT: $V_{CC(off)} \approx 1.8$ V), the output of this circuit is at a high logic state. This signal switches all transistors in the output stage into a high-resistance blocked state (3-state), independently of signals applied to the control inputs of the circuits.

This property of BiCMOS bus-interface devices ensures that a defined behavior can be predicted, even at very low supply voltages where, usually, component behavior is not predictable. Because of power-up 3-state, BiCMOS devices have an advantage over CMOS devices in live-insertion applications.

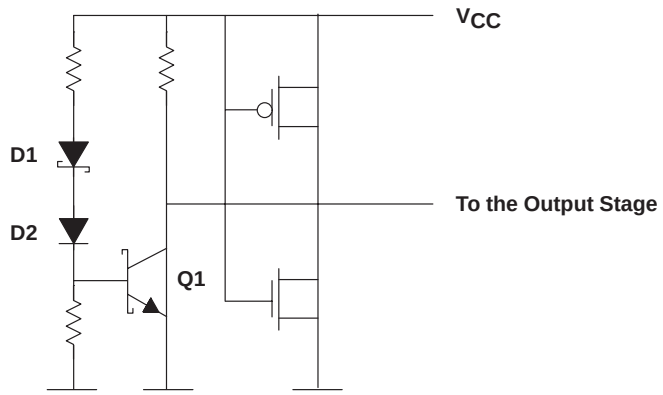

Figure 2. Voltage-Monitoring Circuit in BiCMOS ICs

3 Operating Conditions When Changing Modules With the Supply Voltage On

The previous section describes certain peculiarities of the inputs and outputs of integrated circuits. The operating conditions that can arise when inserting a module in a large system are now examined. The basis for this discussion is the circuit shown in Figure 3. Module 1 is assumed to be connected to the backplane wiring and supplied with voltage from source V1 via the backplane wiring.

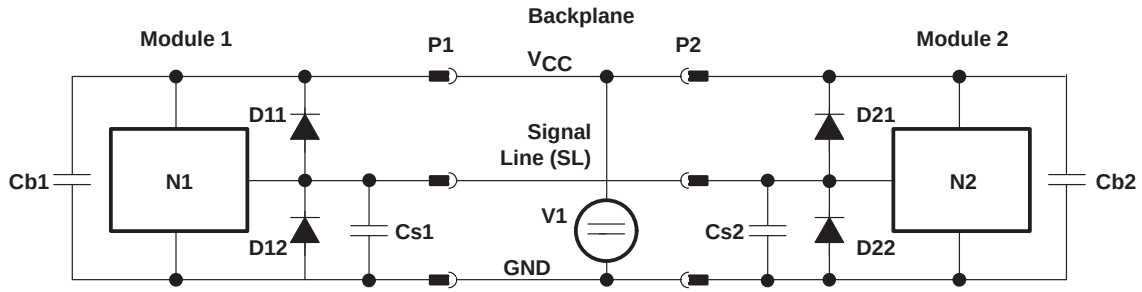

Figure 3. Simplified Circuit to Show Current Paths When Connecting a Module to a System

If Module 2 is inserted into a slot, the contacts of connector P2 make contact in random order as a result of the mechanical tolerances of the guide rails and of the connector. Thus, it is necessary to analyze the various logic states that result.

3.1 GND and the signal line (SL) make contact first; the output of circuit N1 is low

When the module is inserted, a switching capacitance (Cs2 ≈ 20 pF), consisting of the capacitance of the connector P2, the connection to the module, and the input and output capacitance of circuit N2, is charged to the instantaneous logic level (U_{SL} ≈ 0.4 V) of the signal line. Diodes D21 and D22 remain blocking. The signal line is not undesirably influenced. After the connection to V_{CC}, capacitor Cb2 (consisting of the blocking capacitors and the capacitance of the entire circuit) becomes charged, and the circuit on the module that has been inserted commences operation. The disturbances that arise during this switching-on phase, and which result from the initially undefined operation of circuit N2 and from disturbances on V_{CC}, are discussed later in more detail.

3.2 V_{CC} and the signal line (SL) make contact first; the output of circuit N1 is low

When the module is inserted, a connection between the signal line and GND is made via diode D22. The output of circuit N1 first supplies current via this route to the second module until GND also makes contact. This produces severe distortion of the signal on the signal line. As a result of the large equalizing currents that can be expected, an overload of both the output of circuit N1 and diode D22 is likely.

3.3 GND and the signal line (SL) make contact first; the output of circuit N1 is high

When the module is inserted, conditions arise similar to those described in the previous case. The output of circuit N1 supplies current via diode D21, causing an overload of both the output of circuit N1 and of diode D21. Under these circumstances, a defined signal on the signal line cannot be expected.

3.4 V_{CC} and the signal line (SL) make contact first; the output of circuit N1 is high

Assuming that capacitor Cs2 is discharged and that the high level at the output of circuit N1 < V_{CC} , diode D22 conducts and charges capacitor Cb2 to the difference between V_{CC} and the high level at the output of circuit N1. Under these circumstances, the current that flows is negligible as a result of the low level of current supplied by circuit N1. Signal distortion on the signal line is also very small, although the high level is somewhat elevated. This situation is not critical until, after a short time, the output of circuit N1 switches to low, when the state described in section 3.2 is reached.

3.5 V_{CC} and GND make contact first

Under these circumstances, V_{CC} goes to Module 2 before the signal line makes contact. Assuming that the supply voltage to Module 2 has reached an adequate level before the signal line makes contact, and that at the output of circuit N2 a defined (high-resistance) state already has been reached, any disturbance on the signal line can be largely avoided. However, it is possible that the output of circuit N1 is also at a high level, and the switching capacitance Cs2 also must be charged to this level. As shown later, under these circumstances a disturbance of the signal also must be expected.

4 Simple Circuit Modifications

The circuit shown in Figure 3 is so arbitrary that, under the conditions described above, it is impossible to attain definite operating states when inserting a module while the system is operating. The undefined order in which the V_{CC} and GND connections are made is unfavorable. Diodes D21 and D22 also are detrimental, because, in most cases, they open up undesirable current paths, which can then result in faulty operation, if not destruction of components.

The behavior of the circuit can be predicted if the following two requirements are met:

- The connector has one or more leading ground (GND) contacts that make contact before any other contacts are closed.
- For the interface, only integrated circuits without diodes (D11 and D21 in Figure 3) connected to the supply voltage rail, either at the inputs or at the outputs, are used. This requirement applies to all bipolar and BiCMOS circuits with 3-state or open-collector outputs.

The five possible operating states described previously have been reduced to those described in subsections 3.1 and 3.3. Figure 4 shows the changed circuit.

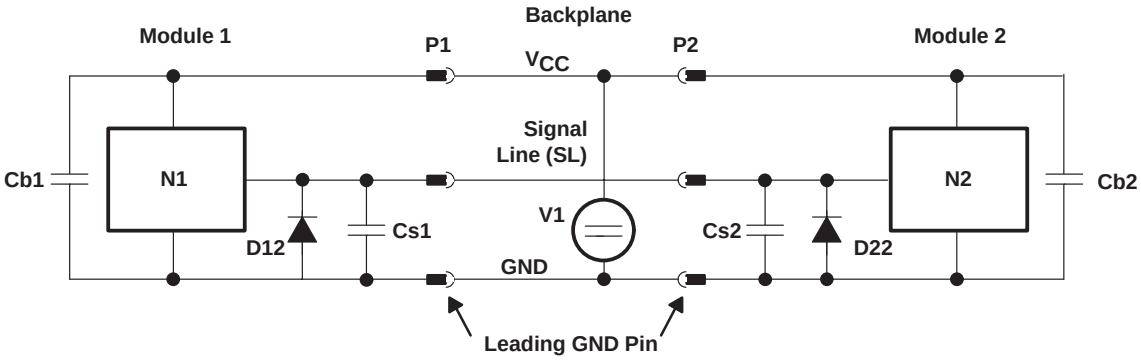

Figure 4. Improved Circuit Using Bipolar or BiCMOS Circuits

When inserting a module into a running system, the ground connection GND makes contact first. This ensures that definite potentials exist between the system and the new module. Diode D22, between the inputs and outputs of the integrated circuits and the ground line, is now operating only in a blocking state. Equalizing currents no longer occur along this path and, to this extent, destruction of the components is prevented.

If contact is made with the signal line before V_{CC}, outputs of the integrated circuits first remain in a high-resistance state. Only after the positive V_{CC} has been connected and the supply voltage to the module has slowly risen, can the outputs of the circuits N2 at the interfaces switch in a more-or-less undefined fashion. At the first instance (charging time of capacitor Cb2), with supply voltages that are still low, neither a definite operation of the enable logic in these bus-interface circuits can be expected, nor is it certain that valid signals will be provided by the controlling circuit to the module that has been inserted.

Using the simple precautions discussed previously can, to a large extent, ensure that a module inserted in an operating system is not damaged. More comprehensive (and costly) precautions are not necessary.

However, there are a number of effects caused by inserting a module that can result in faulty system operation or, in the worst case, can destroy the integrated circuits. For such possibilities, the following phenomena must be considered:

- When inserting a module and before making contact to the signal line, capacitor Cb2 in Figure 4 must be charged. The resulting currents inevitably cause distortion of the signals transmitted through the backplane wiring.
- As mentioned previously, when the supply voltage to the module that has just been inserted ramps up, the outputs of the interface circuits (N2 in Figure 4) can switch on in an uncontrolled fashion. In the simplest case, this can result in short circuiting of the signal, which interferes with the transmission of data in progress. If these bus conflicts continue long enough, thermal overloading of the circuits and destruction of the components can follow, involving not only the module that has just been inserted, but also circuits N1 and N2 in Figure 4.

5 Avoidance of Bus Conflicts

Bus conflicts arise when two or more interface circuits attempt to drive the bus simultaneously, one circuit delivering a high level and the other circuit a low level. Figure 5 shows the simplified typical output characteristics of bipolar bus-interface circuits. The currents that result when a bus conflict occurs are about I_k = 120 mA per output (see Figure 5), determined by the short-circuit current of the circuit that is attempting to supply the high level. The circuit that is trying to generate the low level takes precedence in such a situation. With this circuit, the overload is within acceptable limits. With a low output voltage, V_{OL} < 0.5 V, the total power dissipation P_{dl} of a circuit with n = 8 outputs (for example, the SN74ABT240) can be calculated as follows:

$$P_{dl} = n \times V_{OL} \times I_k = 8 \times 0.5\ V \times 120\ mA = 480\ mW \quad (1)$$

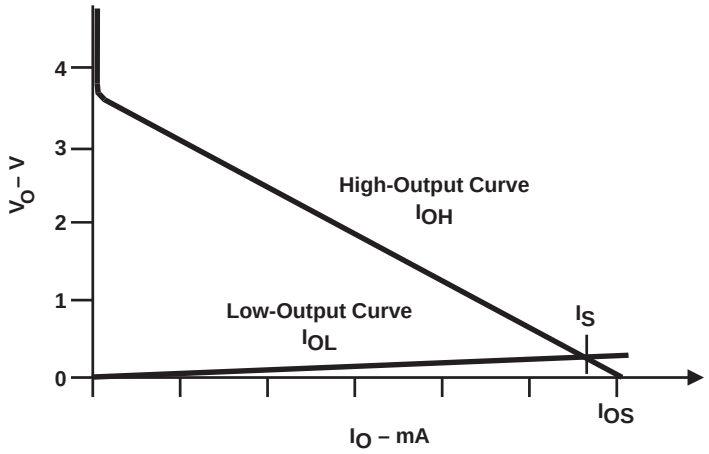

Figure 5. Curve for Calculating the Short-Circuit Currents That Occur With Bus Conflicts

Even with 16-bit Widebus™ circuits, reliability should not be detrimentally affected. The situation is different in the case of the circuit that should deliver the high level. As a result of the short circuit, the voltage drop across the output is about 5 V. With the currents assumed previously, the power dissipation increases to P_{dh} = 5 W (with Widebus circuits, to more than 10 W). Assuming a thermal resistance between the chip and ambient temperature of $R_{\theta JA} \approx 100$ K/W, and a thermal time constant for the silicon chip of $t_\vartheta \approx 1$ ms, in a very short time unacceptably high chip temperatures are reached, and destruction of the integrated circuit (or at least a significant deterioration of its reliability) is likely.

Additional circuit modifications are necessary to prevent an overload of the interface circuits. The simplest way to make the situation less critical consists of using only bus-interface circuits, which are provided with the power-up 3-state circuit, mentioned previously, at any questionable points in the circuit. Assuming that, in the system in question, the other digital circuits on the module that is to be exchanged have been implemented in CMOS technology (which at V_{CC} > 2 V are known to supply defined logic levels), bus conflicts should be avoided.

Unfortunately, in many cases it cannot be assumed that the logic circuits mentioned will also supply defined levels at higher supply voltages, keeping the bus-interface circuits in an inactive state. These logic circuits usually are controlled by VLSI circuits, e.g., by the microprocessor on this module. Last, control circuits do not necessarily supply valid output signals at very low supply voltages and during the initialization phase. The development engineer must use additional circuits that ensure, under all circumstances, that the circuits switch into 3-state.

A circuit proposal is shown in Figure 6. The heart of this circuit consists of the supply voltage supervision and initialization integrated circuit TLC7705. A component of this kind in the module is usually necessary to ensure correct initialization of the circuit (RESET) when switching on the supply voltage. Additionally, the outputs of this circuit are taken to the enable inputs of the bus-interface circuit in order, during the initialization phase, to keep the bus-interface circuits, under every condition, in an inactive high-resistance state. For this purpose, it is advantageous to use bus-interface devices having two enable inputs of equal priority, such as the SN74ABT541. With this device, one of the inputs is connected to the output of the monitor circuit, while the other input is connected to the part of the circuit that normally releases the outputs of the bus-interface circuits. If two independent enable inputs are not available, as with the SN74ABT245, the required function must be performed with an additional gate, for example, the SN74AC32. In some cases, the resulting increase in delay time is unacceptable. Faster bipolar circuits, such as the gate SN74F00, can remedy the delay-time problem. With these single-stage logic circuits, it is possible to ensure, even at very low supply voltages of 2 to 4.5 V, that a low level at an input will result in a high state at the output. However, under these circumstances, an adequate voltage level cannot be guaranteed. For this reason, as shown in Figure 6, a resistor should be provided at the output of this gate to pull the output up to a sufficiently high level.

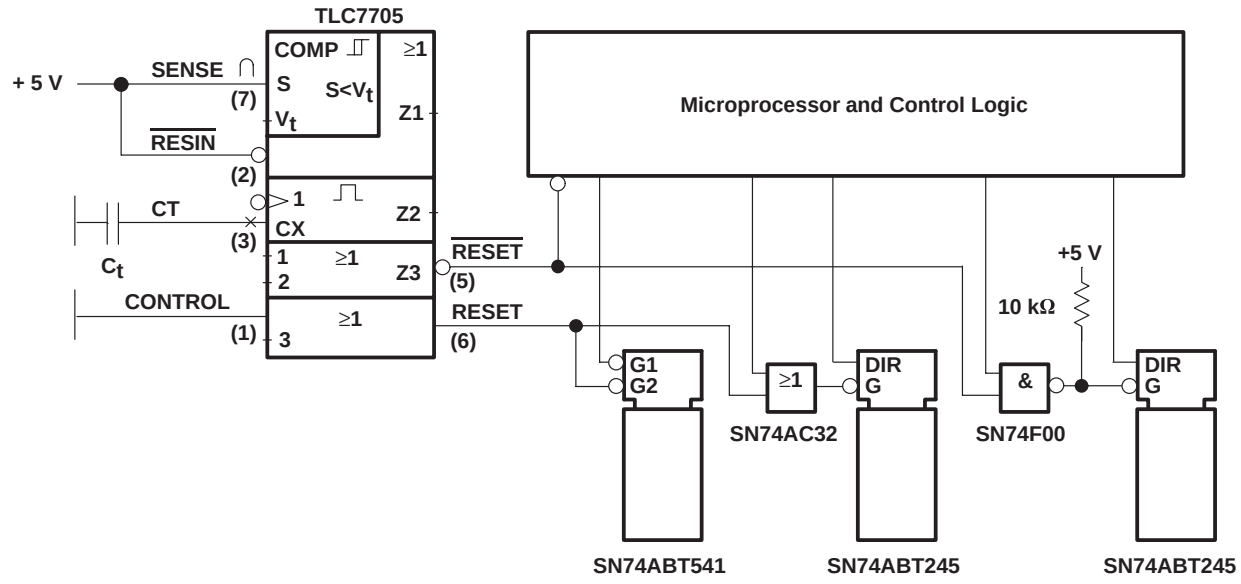

Figure 6. Monitoring Bus-Interface Circuits

6 Avoidance of Disturbances on the System Bus

When inserting a new module in an operating system, the switching capacitance (Cs2 in Figure 3) of the individual signal lines at the interface must be charged to the instantaneous voltage on the corresponding bus line. These additional currents distort the signal that is being transmitted at that instant. Figure 7 shows the equivalent circuit that describes this situation. This involves switching a capacitor (Cs2 = 20 pF) into the middle of a bus line. The inductance of the connector contact (L_c = 30 nH) is in series with this capacitor. The line has an impedance (Z_O = 30 Ω) with a signal propagation time (t_p = 10 ns). It is terminated at both ends with resistors (R_t = 100 Ω) such that, in the quiescent state, a high level (V_h = 3 V) results. The circuit arrangement shown here conforms to conditions typically found with backplane wiring systems that are driven by TTL levels.

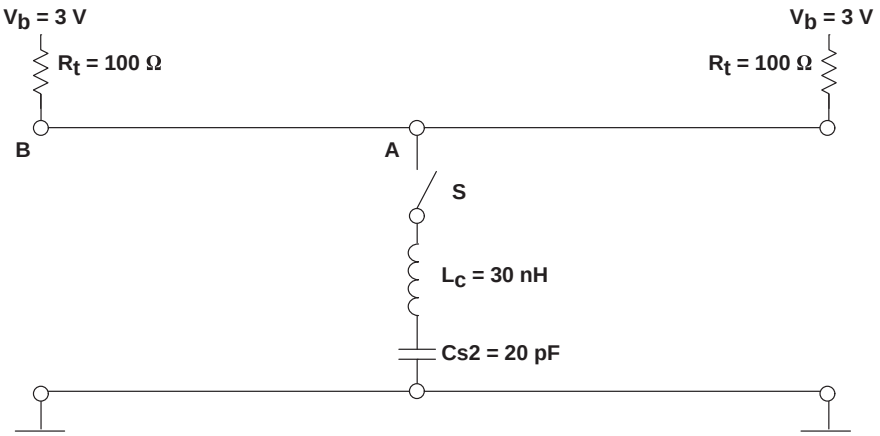

Figure 7. Connecting a Capacitor to a Line

Using the SPICE simulation program, the voltage waveform on the line was simulated at points A and B when closing switch S. Figure 8 shows the result. As expected, connecting capacitor Cs2 to the line at point A generates a voltage peak, which is already close to the threshold voltage (V_t = 1.5 V) of the receiver to which it is connected. The situation is even more critical at B (the end of the line). As a result of intentional mismatching at this point by the terminating resistors (R_t = 100 Ω), the amplitude of the disturbance increases such that the threshold voltage of the circuits at this point may be significantly exceeded. Considering the short response time of modern logic circuits (the delay time of the inverter in the bus-interface circuits is only a few hundred picoseconds), faulty operation of the circuits connected to the bus must be expected.

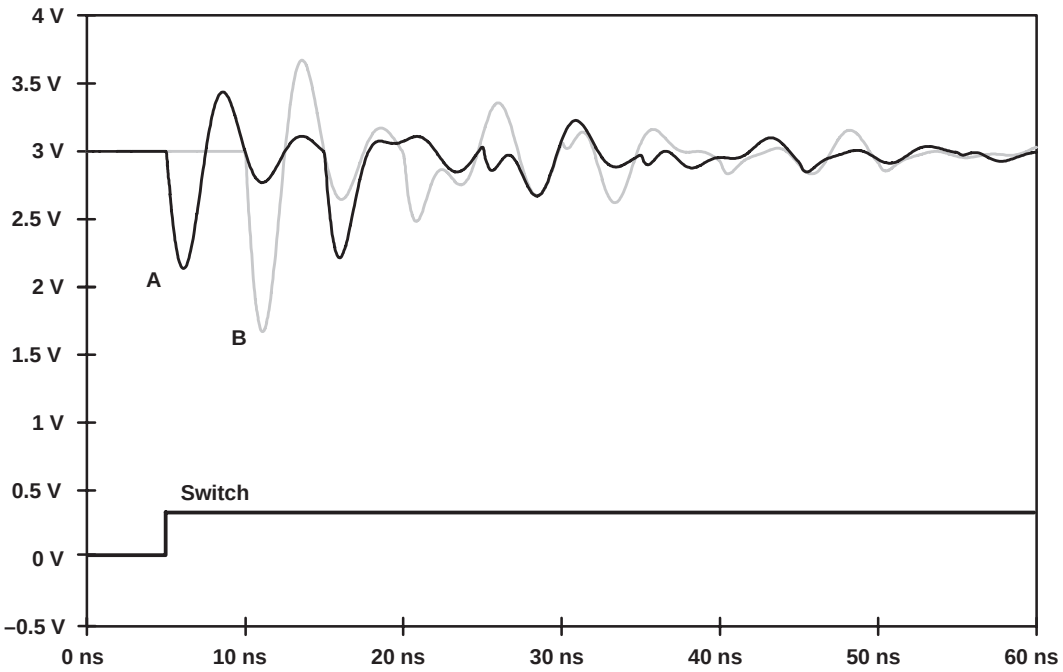

Figure 8. Voltage Peaks When Making Contacts to Signal Lines (Without Voltage Bias)

The amplitude of the interference voltage peaks can be reduced considerably if capacitor Cs2 is charged to the threshold voltage of the circuit via a high-value series resistor R_p (in the simulated circuit, R_p = 10 kΩ) before making contact. Cs2 is charged from an auxiliary voltage source ($V_{p)}$ that corresponds approximately to the threshold voltage of the receiving circuits, i.e., typically V_p = 1.5 V. Figure 9 shows the corresponding circuit and Figure 10 shows that the interference voltage peaks have significantly reduced amplitude.

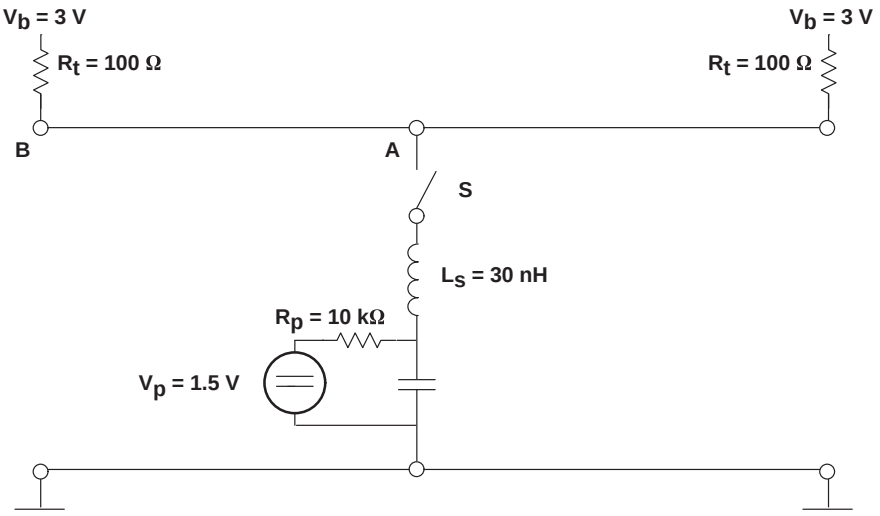

Figure 9. Connection of a Capacitor to a Line (With Voltage Bias)

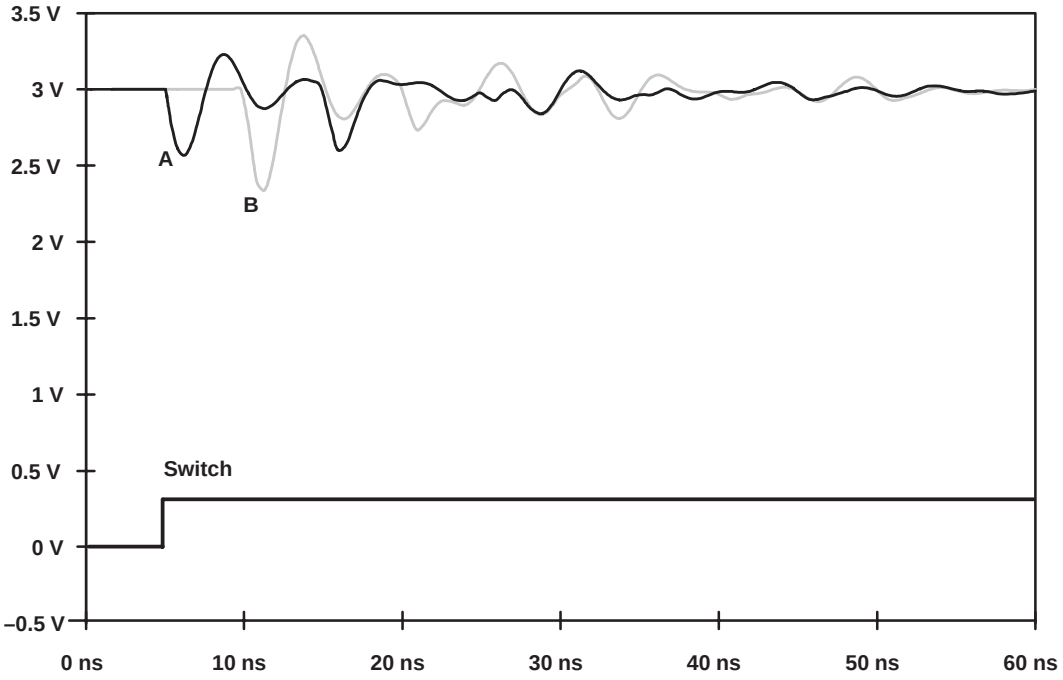

Figure 10. Voltage Peaks When Making Contacts to Signal Lines (With Voltage Bias)

Resistor R_p should have as high a value as possible to keep the loading of the bus during the module-insertion process as low as possible. However, the maximum value of the resistance is determined by the leakage current I_{off} of the circuit to be charged. This leakage current flowing through resistor R_p causes a voltage drop that must be added to the value of the voltage bias.

In practice, in addition to the leading ground contact on the connector, a leading supply-voltage contact must be provided. Figure 11 shows a circuit proposal for such an interface. The following parts of the circuit in the module are initially supplied via the leading ground connection (GND) and the supply voltage connection (V_{CC1}):

- The reference voltage supply D1 for generating the voltage bias on the signal lines
- Switch U3 (for example, SN74CBT3244), which switches the voltage bias to the signal lines during the switch-on phase via series resistor R_p
- Voltage-monitoring circuit U1, which keeps bus-interface circuits U2 in an inactive state during the switch-on phase and, as previously described, controls the initialization of the module.

To avoid a voltage collapse on the supply line of the backplane wiring, which could arise from the sudden charging of blocking capacitor C1, a current-limiting resistor R3 should be connected in series with the V_{CC1} contact on the connector. Because the current consumption of the part of the circuit supplied via this contact is only a few milliamperes, and because it places no excessive demands on the stability of the voltage, the current limiting can be implemented with a simple resistor. A similar filter must also be provided in the V_{CC2} line. However, because this line has considerably higher currents, a significantly more complicated arrangement is necessary. A suitable circuit is described in the next section.

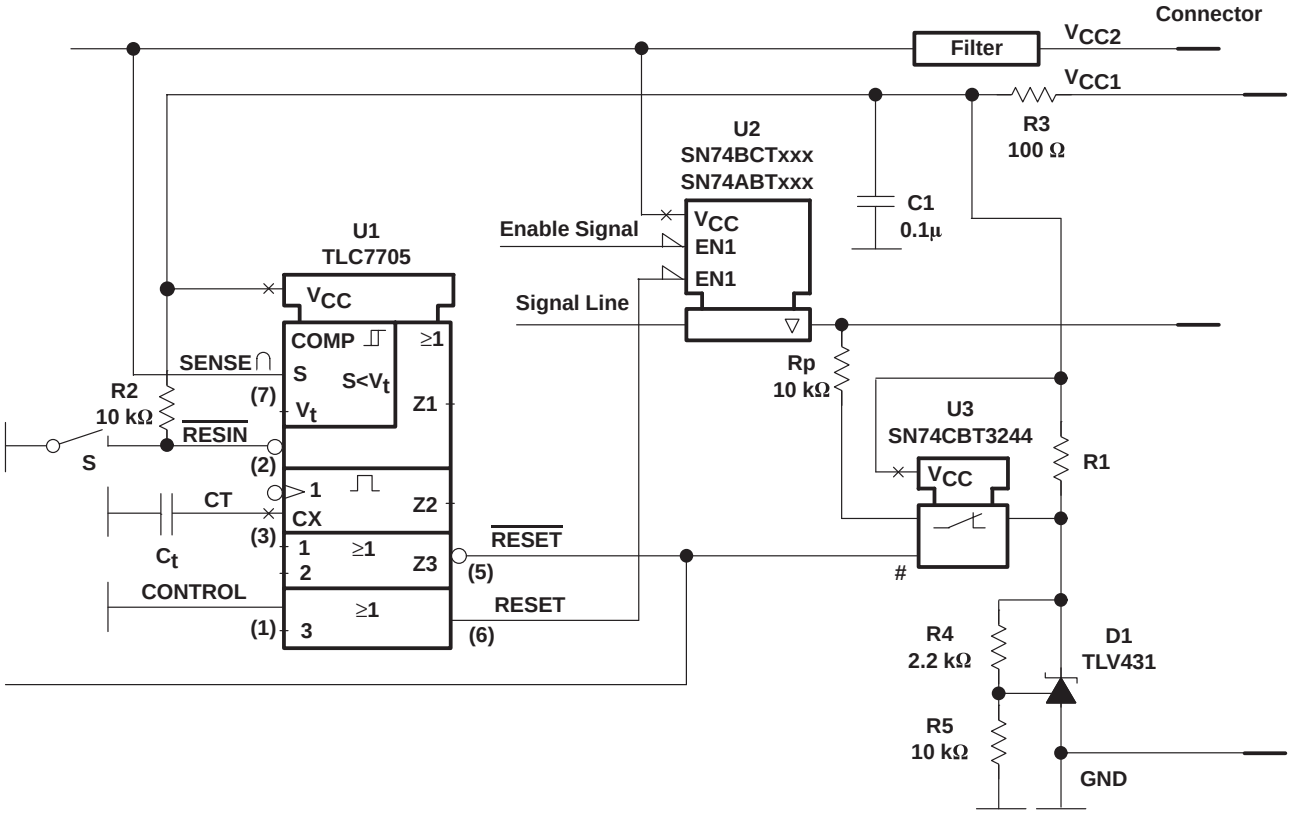

Figure 11. Generation of the Voltage Bias and Control of the Interface

Because supply voltage V_{CC2}, which must power the bus-interface circuits and all other circuits on the module, has not been applied at this instant, outputs of monitor circuit U1 are active, i.e., the voltage at its SENSE input is ≈ 0 V. The RESET output holds the bus-interface circuit U2 in an inactive state via enable input EN1. Simultaneously, the RESET signal closes the switch in circuit U3, so that the voltage bias supplied by the zener diode D1 via the decoupling resistor is applied to the signal lines. In addition, the RESET signal and, if necessary, the noninverting RESET signal, as well, are supplied to the other parts of the circuit on the module that need to be initialized when switching on. When the signal lines make contact as the module is inserted further, signal distortion on the system bus remains very low (see Figure 10). After V_{CC2} makes contact, the other parts of the circuit on the module are supplied with current. In the same way the potential at the SENSE input of circuit U1 rises to 5 V. After the elapsed time determined by timing capacitor C_t, the logic circuits on this module are in a defined initial state and can start operating. At this moment, switch U3 is again opened to avoid an additional loading of the signal lines by the resistors (R_s).

It is advantageous to make the signals delivered by voltage-monitoring circuit U1 independent of V_{CC1} and V_{CC2}. As a result of the contacts bouncing on the connector when inserting a module, undefined operating states can arise. For this reason, switch S at the inverting RESIN input of circuit U1 is provided, which is coupled with the mechanical interlock of the module. When a module is removed, unlatching this interlock automatically switches off logic circuits in the module. In this way, bus-interface circuits U2 also are immediately switched into an inactive state. Conversely, these circuits are held in an inactive state when inserting a new module until the interlock has been mechanically latched, and thus the correct mechanical insertion and defined contacting of the connector is ensured.

7 Special Bus-Interface Circuits

Integrating voltage bias, switches, and resistors into bus-interface circuits allows a significant reduction in the circuit complexity. This feature has been implemented in the enhanced transceiver logic (ETL), series SN74ABTE, and backplane transceiver logic (BTL), series SN74FB. The ETL circuits have been specified by the VITA working group, which has been concerned with the VME bus (ANSI/IEEE Standard 1014), while the BTL circuits are used in the FutureBus+ (IEEE Standard 896), among other applications.

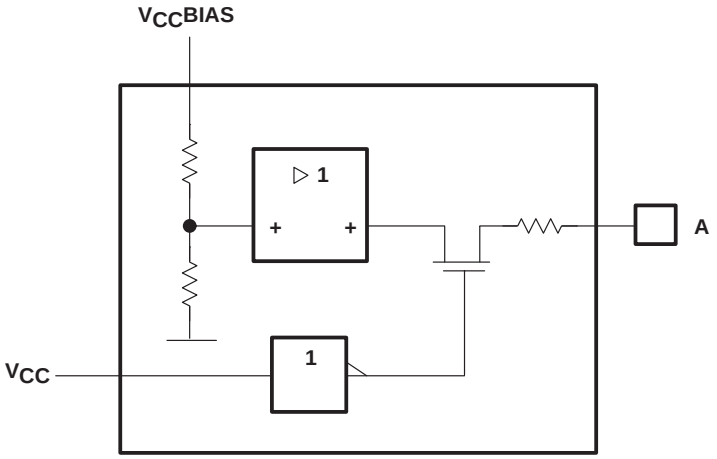

Figure 12. Generation of the Voltage Bias and Control in the SN74ABTE16245

The ETL circuits (for example, SN74ABTE16245) have an additional supply voltage connection (V_{CC}BIAS). This feeds the circuit, which generates the voltage bias mentioned above and, together with the V_{CC} connection, controls the switching on and off of the voltage bias. Figure 12 shows the simplified circuit diagram of this part of the circuit. It does not include the power-up 3-state circuit (see Figure 2), which also is contained in these bus-interface circuits, and which switches all outputs into the high-impedance state (3-state) at a supply voltage below about 2.5 V.

Figure 13 shows a bus interface with ETL circuits. At the moment the module is inserted, and after the connection of the V_{CC1}– and GND contacts, the generation of the voltage bias in the bus interface circuit U3 becomes effective. Voltage-monitoring circuit U1 is simultaneously switched on, which, via OR gate U2, switches the OE input of bus driver U3 to high; when the outputs of this circuit are inactive, this is the 3-state. Thus, the circuit remains in an inactive high-impedance state until initialization of the module has been completed. This also is the case after the V_{CC2} connector makes contact and this supply voltage has increased to the point that the power-up 3-state circuit in bus-interface circuit U3 is no longer effective. It also is advisable to control the end of the initialization phase by means of switch S, which should be coupled to the mechanical interlock of the module.

Before removing the module from a running system, this circuit must be brought to a definite inactive state. This also is performed with switch S, which closes when the module interlock is released. Thus, the outputs of bus-interface circuit U3 are automatically switched into the 3-state by circuits U1 and U2.

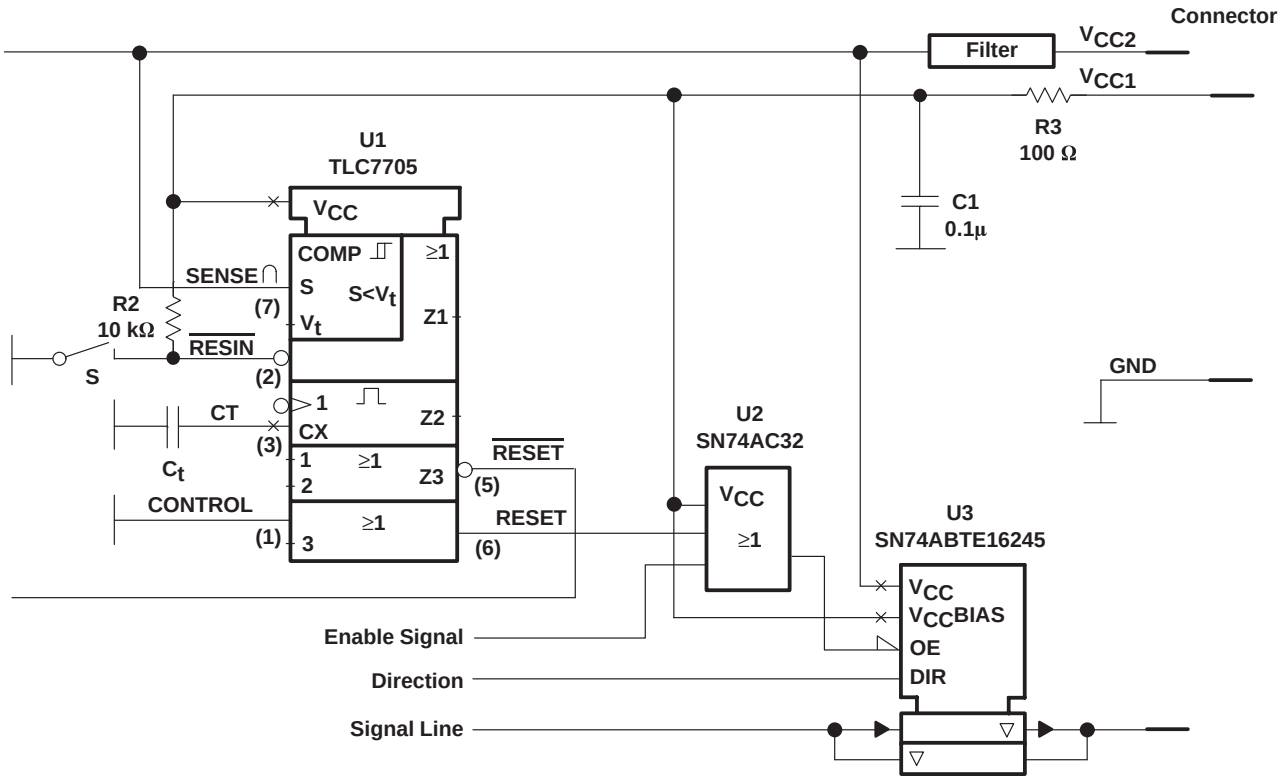

Figure 13. Bus-Interface Control in ETL Circuits

Additional circuit features are found in BTL circuits, which support the use of these components in the applications discussed here. As shown in Figure 12, these bus-interface circuits contain a voltage-bias generator, which is supplied with voltage via the BIASV_{CC} terminal. When inserting the module, this part of the circuit must thus be supplied with voltage (V_{CC1} in Figure 14). In addition, a power-up 3-state circuit also has been integrated, which holds the A and B outputs in an inactive high-impedance state (3-state), until the voltage at the V_{CC}– connections is < 2.5 V. The circuit design is simplified in that several of the BTL circuits for the control of the B outputs, which are taken to the backplane wiring, are provided with two enable inputs. One of the two inputs is monitored by the bus control, while the other input is controlled by the voltage-monitoring circuit. By eliminating an additional OR gate (U2 in Figure 13) the component complexity is reduced. It is more important that, because of the delay time of this gate, about 5 ns are saved.

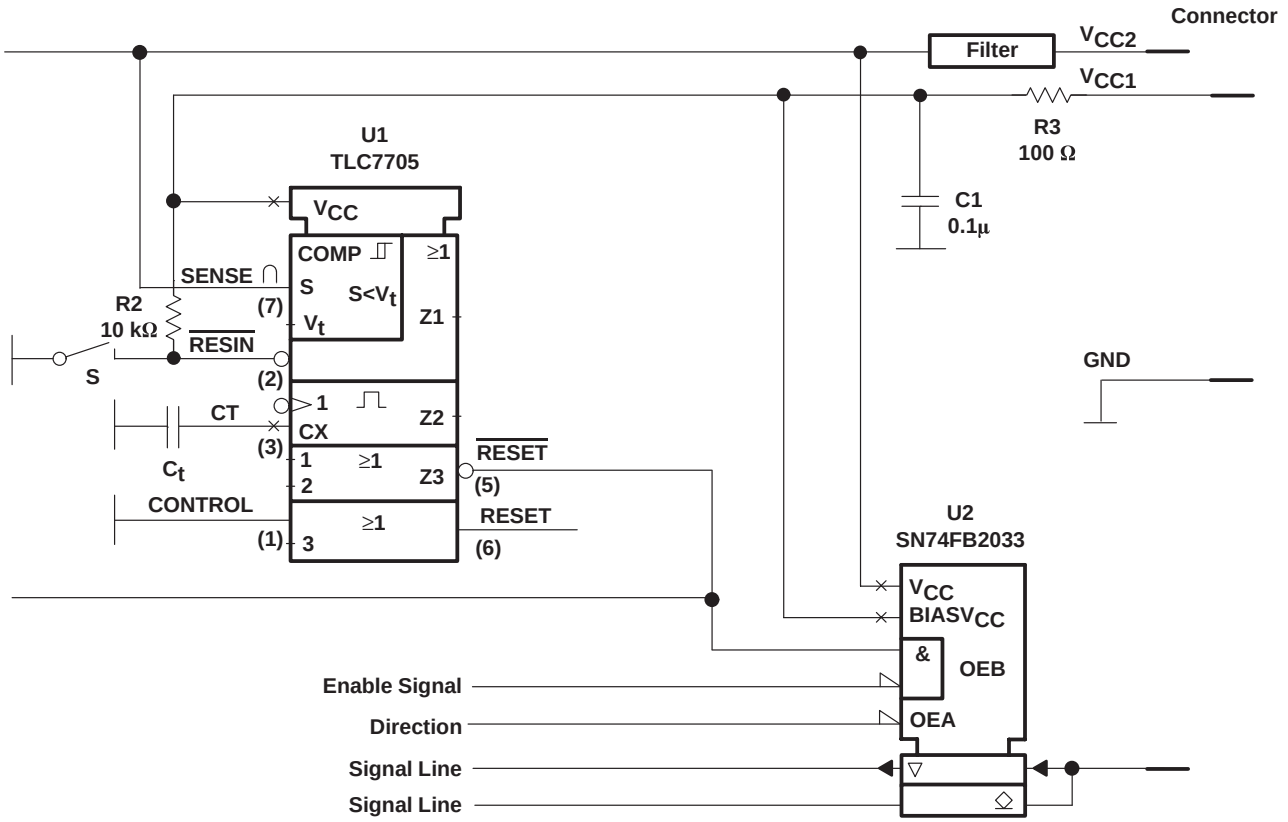

Figure 14. Bus-Interface Control With BTL Circuits

8 Avoidance of Disturbances to the Supply Voltage

Disturbances on the supply voltage lines of a system can occur as a result of charging the line capacitance in the same way as when switching the signal lines to the bus. When a module is inserted in a slot, the large capacitance of this circuit must first be charged. This capacitance is dictated primarily by the blocking capacitor on the circuit board where values of several tens to hundreds of µF are used. Another source of interference is the load on the module, which causes a considerable change of current, and hence voltage, when switching on the supply voltage. This problem is easily solved with the leading supply-voltage connector (V_{CC1} in Figures 13 and 14). Because the part of the circuit fed via this connector has a current consumption of only a few milliamperes, it is easy to implement current limiting at switch on with resistor R3 in Figures 13 and 14. Minor reductions of voltage are acceptable because the CMOS circuits in question can operate over a wide range of supply voltage.

The only question to be answered here is, what is the time constant ($t_d = R3 \times C1$)?, for example, see Figure 14. This time constant determines the rise time of V_{CC1}, and this voltage must have reached its nominal value before the lagging connections are made to V_{CC2}. The time that is available for the build up of V_{CC1} should be estimated. For this purpose, assume that the insertion distance of a module in a module carrier is $D_m = 15$ cm, that the leading contacts protrude by $D_c = 1.5$ mm, and that the time during which the module is being inserted is $t_i = 0.1$ s. Under these conditions, the leading contacts make contact about 1 ms before the subsequent ones. As shown by the applicable mechanical factors, these times are much longer than the time constant of the previously mentioned R/C network.

For the filter of the connection to V_{CC2}, a significantly more complicated arrangement is necessary. The current of several amperes, which flows at this point, makes it impossible to achieve current limiting with a simple resistor. A solution is an inductance in the V_{CC2} line. These components have a high ac impedance, but a very low dc resistance. When designing such a filter, care must be taken that the resonant circuit formed by the L/C element is damped sufficiently to ensure that oscillation does not occur when switching on the supply voltage (the meeting of the contacts on the connector) or when the load changes. A simplified representation of the current supply to a module is shown in Figure 15. After switch S closes (the connector makes contact), capacitor C_b (blocking capacitor in the module) is charged via inductance L. Resistor R_L, together with diodes D1 and D2 connected in series, represents the load that is formed by the electronic circuit in the module. Semiconductors have notoriously nonlinear characteristics, and these are also evident in the current supply path. To account for nonlinearity, the equivalent circuit of the integrated circuits in the module is represented by a resistor and two diodes.

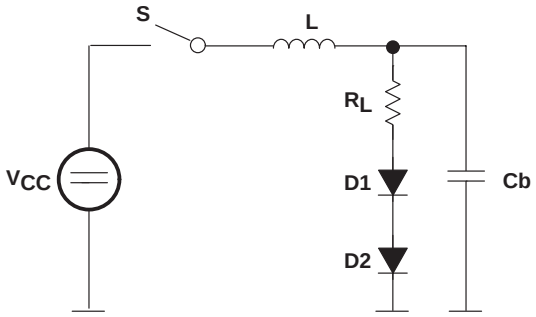

Figure 15. Equivalent Circuit of the Current Supply to a Module

Optimum results (short ramp-up time, no overshoot of the supply voltage) occur when this network is dimensioned such that critical damping is achieved. In this case, the following applies:

$$2 \times R_L = \sqrt{\frac{L}{C_b}} \quad \textbf{(2)}$$

The inductance can be calculated as follows:

$$L = 4 \times R_L^2 \times Cb \quad \textbf{(3)}$$

With a load resistor of $R_L = 1\ \Omega$ and a capacitor $C_b = 50$ mF, this expression applies:

$$L = 4 \times 1^2\Omega^2 \times 50\ \mu F = 200\ \mu H \quad \textbf{(4)}$$

Figure 16 shows the waveform of the supply voltage with various degrees of damping. It shows the following situations:

- Overshoot ($Q > 1$) : $L < 4 \times R_L^2 \times C_b$ ($R_L = 1\ \Omega$, $C_b = 50\ \mu F$, $L = 50\ \mu H$)
- Critical damping ($Q = 1$) : $L = 4 \times R_L^2 \times C_b$ ($R_L = 1\ \Omega$, $C_b = 50\ \mu F$, $L = 200\ \mu H$)
- Overdamping ($Q < 1$) : $L > 4 \times R_L^2 \times C_b$, ($R_L = 1\ \Omega$, $C_b = 50\ \mu F$, $L = 800\ \mu H$)

In the above calculations, the diodes in series with resistor R_L are ignored. This results in the curve (shown in Figure 16 as a case of critical damping) still showing a slight overshoot. In practice, this simplification of the calculations is permissible because the differential resistance of the diodes is usually small compared to resistor R_L. In addition, to avoid an overshoot of the supply voltage, inductance L is made sufficiently large to ensure that, in the worst case, overdamping occurs. In many applications, a problem is then presented by the mechanical dimensions of inductance L, which must be designed to carry high currents.

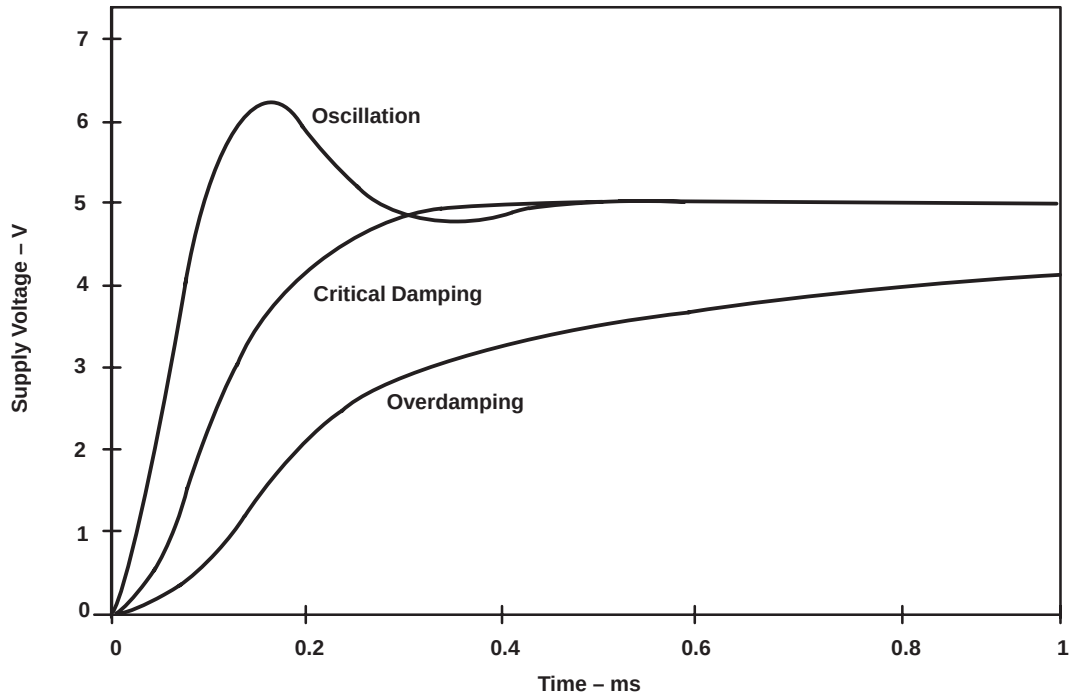

Figure 16. Transient Behavior of the Supply Voltage at Switch On, With Various Degrees of Damping

Another way to limit the switch-on current when inserting a module consists of inserting a semiconductor switch, which switches on slowly, in the supply line. Figure 17 shows such an arrangement. In this case, P-channel MOS transistor Q is used as a switch, an R/C network (R1, Cd) in the gate circuit of this transistor, ensuring that the latter switches on slowly. Diode D ensures that the capacitor discharges rapidly when the module is withdrawn.

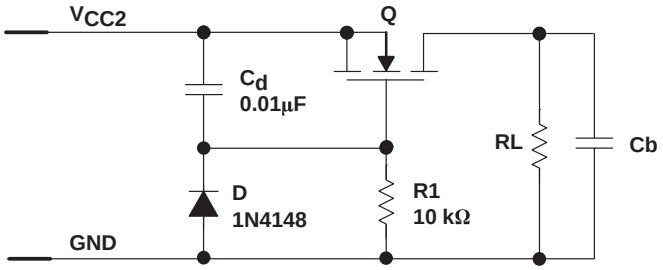

Figure 17. Switch-On Delay Circuit Using a MOS Transistor

When considering transistor Q, one with a low on-resistance (R_{DSon}) should be chosen to avoid an excessive voltage drop across this component. It may be necessary to use several transistors in parallel. Because the power dissipation is exceptionally low when in operation (as a result of the low voltage drop), transistors in the SO package, such as the TPS1101PW, also are suitable at this point in the circuit.

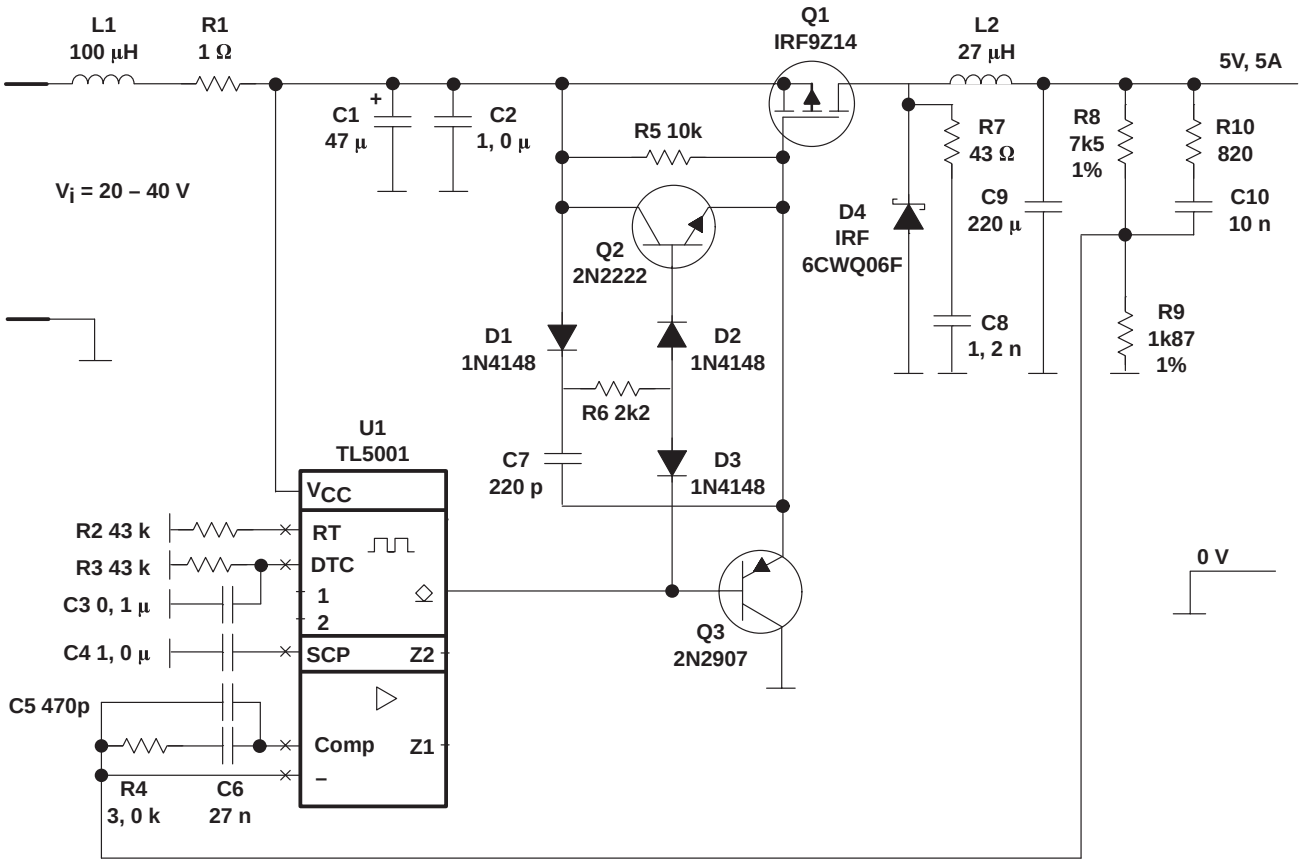

Figure 18. Decentralized Power Supply With Limiting of Switch-On Current

In equipment where it is required to change modules with the supply voltage switched on, a decentralized power supply is often used. An unstabilized voltage of several tens of volts is applied to all modules. Stabilization of the operating voltage is performed by a switching regulator or voltage converter on each module. However, even in this case, limiting of the switch-on current also should be provided to avoid unacceptable voltage drops on the common ground line (GND). The requirements of these parts of the circuit can, however, be achieved more simply. Voltage drops across inductances are not so significant, because these can be compensated by subsequent voltage regulators; therefore, a considerably smaller inductance can be used. Operating the filter in a region in which overshoot of the voltage at the input to the regulator occurs is acceptable.

Figure 18 shows a proposed circuit for a decentralized current supply of this kind. The switch-on current limiting is again performed with the help of the inductance L1 at the input. Damping of the switch-on process is implemented with resistor R1 in series with the inductor. Integrated circuit TL5001 is used as the switching regulator. More detailed information regarding the use of this component can be found in the corresponding data sheets and application reports.

9 Summary

When exchanging modules in electronic equipment whose supply voltage must remain switched on, the development engineer must make circuit modifications to avoid damage to the circuit and to prevent disturbances in the operation of the equipment.

The first requirement (avoiding damage) can be met comparatively easily. In this case, it is necessary only to ensure that, when a module is inserted, no undefined currents flow into the integrated circuits at the interfaces. In addition, the destruction of the interface circuits as a result of undefined states when the circuits are switched on (bus conflicts) must be prevented and can be achieved with the following precautions:

- Leading ground contacts (GND) on the connector
- Use of interface circuits that remain at a high resistance when the supply voltage is switched off. All circuits in the bipolar and BiCMOS logic families meet this requirement (see Table 1).
- Appropriate circuit modifications must be made to prevent undefined states at the outputs of the interface circuits (bus conflicts) when the supply voltage is switched on. Bus-interface circuits from the series ABT, BCT, and LVT are provided with a power-up 3-state circuit, which, in many cases, provides adequate protection. It is safer to switch the interface circuits during the start-up phase so that they are forced into an inactive state (see Figure 6), by means of an additional voltage-monitoring circuit on the module being inserted. Experience has shown that it is advisable to take this precaution, not only when modules must be inserted while the supply voltage is switched on, but because bus conflicts also arise when the system is switched on under normal conditions.

If there is the additional requirement that an operating system not be disturbed when a module is removed or inserted (live insertion), circuit design is much more complicated and the following requirements must be met:

- Leading supply voltage contacts (GND and V_{CC}) on the connector
- Exclusive use of interface circuits that are provided with a power-up 3-state circuit [series ABT, BCT, and LVT (see Table 1)]. These circuits ensure that, even with supply voltages < 2 V, the bus-interface circuits remain in an inactive high-resistance state.
- With suitable circuit modifications, undefined states of the outputs of the interface circuits (bus conflicts) must be avoided when the supply voltage is further increased. A supply-voltage monitoring circuit on the module being inserted is essential to maintain the interface circuits in an inactive high-impedance state during the switch-on phase.
- Control both the enabling and the deactivation of the circuit on the module (including the bus-interface circuits) with a switch that is coupled to the mechanical interlocking of the module.
- Ensure by suitable circuit modifications that, before making contact, the signal lines of the module being inserted are charged to a voltage (pre-charge) that lies approximately halfway between the high and low logic levels on the backplane wiring. This avoids disturbances on the system bus. Bus-interface circuits from the series BTL and ETL are provided with such integrated pre-charge circuits.
- Ensure a slow rise of the supply current when a module is inserted to prevent the rapid charging (giving the effect of a short-circuit) of the capacitors in a module when the module is inserted. This precaution ensures that no unacceptable interference voltages (ground bounce) arise on the ground line (GND) of the backplane wiring and a collapse of the voltage on the power-supply line of the system also is avoided.

If modules must be exchanged while the supply voltage remains on (live insertion), the engineer developing the system must account for a number of operating states, particularly during insertion. If suitable precautions are taken and the correct components are chosen, it is possible to not only prevent damage to parts of the circuit, but, more significantly, operation of the system is not adversely affected by removing or inserting modules.

The precautions that isolate a module from the system logic when the module is removed and reinserted in the system have not been covered in this report. Results of these tasks must be controlled by the operating system of the computer, a discussion that is far beyond the scope of this application report.

Acknowledgment

Eilhard Haseloff is the author of this application report.