CDC339 Clock Driver with 3-State Outputs

1 Features

- Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications
- TTL-Compatible Inputs and Outputs
- Distributes One Clock Input to Eight Outputs
  - Four Same-Frequency Outputs
  - Four Half-Frequency Outputs
- Distributed V_{CC} and Ground Pins Reduce Switching Noise
- High-Drive Outputs (−48-mA I_{OH}, 48-mA I_{OL})
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages

2 Applications

- Data center switch and server motherboard

3 Description

The CDC339 is a high-performance, low-skew clock driver. It is specifically designed for applications requiring synchronized output signals at both the primary clock frequency and one-half the primary clock frequency. The four Y outputs switch in phase and at the same frequency as the clock (CLK) input. The four Q outputs switch at one-half the frequency of CLK.

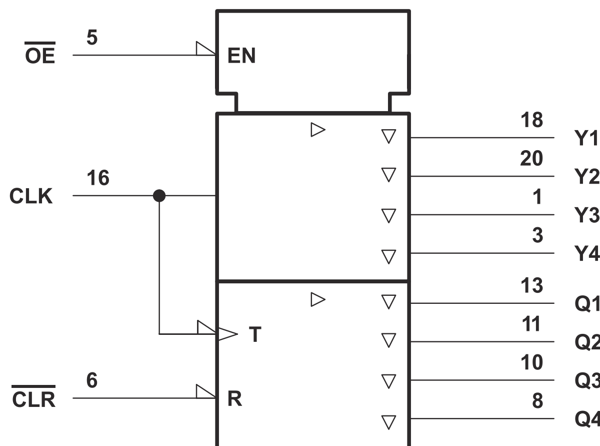
When the output-enable ($\overline{OE}$) input is low and the clear ($\overline{CLR}$) input is high, the Y outputs follow CLK and the Q outputs toggle on low-to-high transitions of CLK. Taking $\overline{CLR}$ low asynchronously resets the Q outputs to the low level. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The CDC339 is characterized for operation from −40°C to 85°C.

Device Information

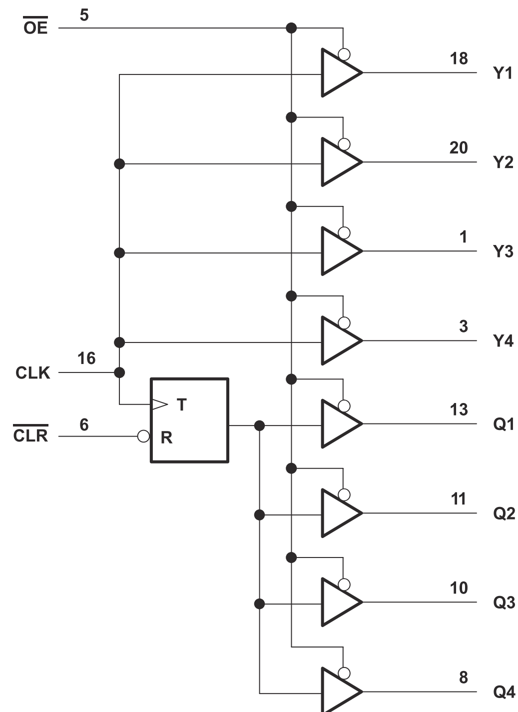
PART NUMBER	PACKAGE[(1)]	BODY SIZE (NOM)
CDC339DW	SOIC (20)	132 mm² 12.8 x 10.3
CDC339DB	SSOP (20)	38 mm² 5.3 x 7.2

(1) For all available packages, see the orderable addendum at the end of the data sheet.



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Logic Symbol



Logic Diagram (Positive Logic)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 1994) to Revision A (May 2020)	Page
• Updated to new TI standard	1
• Added Application bullet	1

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5 Pin Configuration and Functions

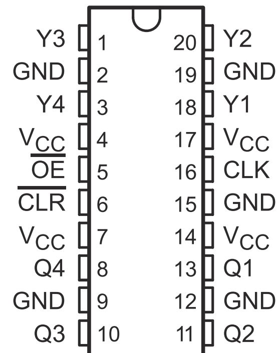

Figure 5-1. DB OR DW PACKAGE (TOP VIEW)

Function Table

INPUTS			OUTPUTS	
$\overline{OE}$	$\overline{CLR}$	CLK	Y1−Y4	Q1−Q4
H	X	X	Z	Z
L	L	L	L	L
L	L	H	H	L
L	H	L	L	Q_0 (1)
L	H	↑	H	$\overline{Q}_0$ (1)

(1) The level of the Q outputs before the indicated steady-state input conditions were established.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range[(2)]		–0.5	7	V
V_O	Voltage range applied to any output in the disabled or power-off state		–0.5	5.5	V
I_O	Current into any output in the low state			96	mA
I_{IK} ($V_{I < 0}$)	Input clamp current			–18	mA
I_{OK} ($V_{O < 0}$)	Output clamp current			–50	mA
	Maximum power dissipation at T_A = 55°C (in still air)[(3)]	DB Package		0.6	W
		DW Package		1.6	W
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		–48	mA
I_{OL}	Low-level output current		48	mA
f_{clock}	Input clock frequency		80	MHz
T_A	Operating free-air temperature	–40	85	°C

(1) Unused pins (input or I/O) must be held high or low.

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6.3 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V	I_I = –18 mA				−1.2	V
V_{OH}	V_{CC} = 4.75 V	I_{OH} = − 48 mA		2			V
V_{OL}	V_{CC} = 4.75 V	I_{OL} = 48 mA				0.5	V
I_{IH}	V_{CC} = 5.25 V	V_I = 2.7 V				50	µA
I_{IL}	V_{CC} = 5.25 V	V_I = 0.5 V				−50	µA
I_{OZ}	V_{CC} = 5.25 V	V_O = 2.7 V or 0.5 V				±50	µA
I_O (2)	V_{CC} = 5.25 V	V_O = 2.5 V		−50		−180	mA
I_{CC}	V_{CC} = 5.25 V V_I = V_{CC} or GND	I_O = 0	Outputs high			70	mA
			Outputs low			85	
			Outputs disabled			70	
C_i	V_I = 2.5 V or 0.5 V				3		pF
C_o	V_O = 2.5 V or 0.5 V				8		pF

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

6.4 Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency			80	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		ns
		CLK low	4		
		CLK high	4		
t_{su}	Setup time	$\overline{CLR}$ inactive before CLK↑	2		ns
	Clock duty cycle		40%	60%	

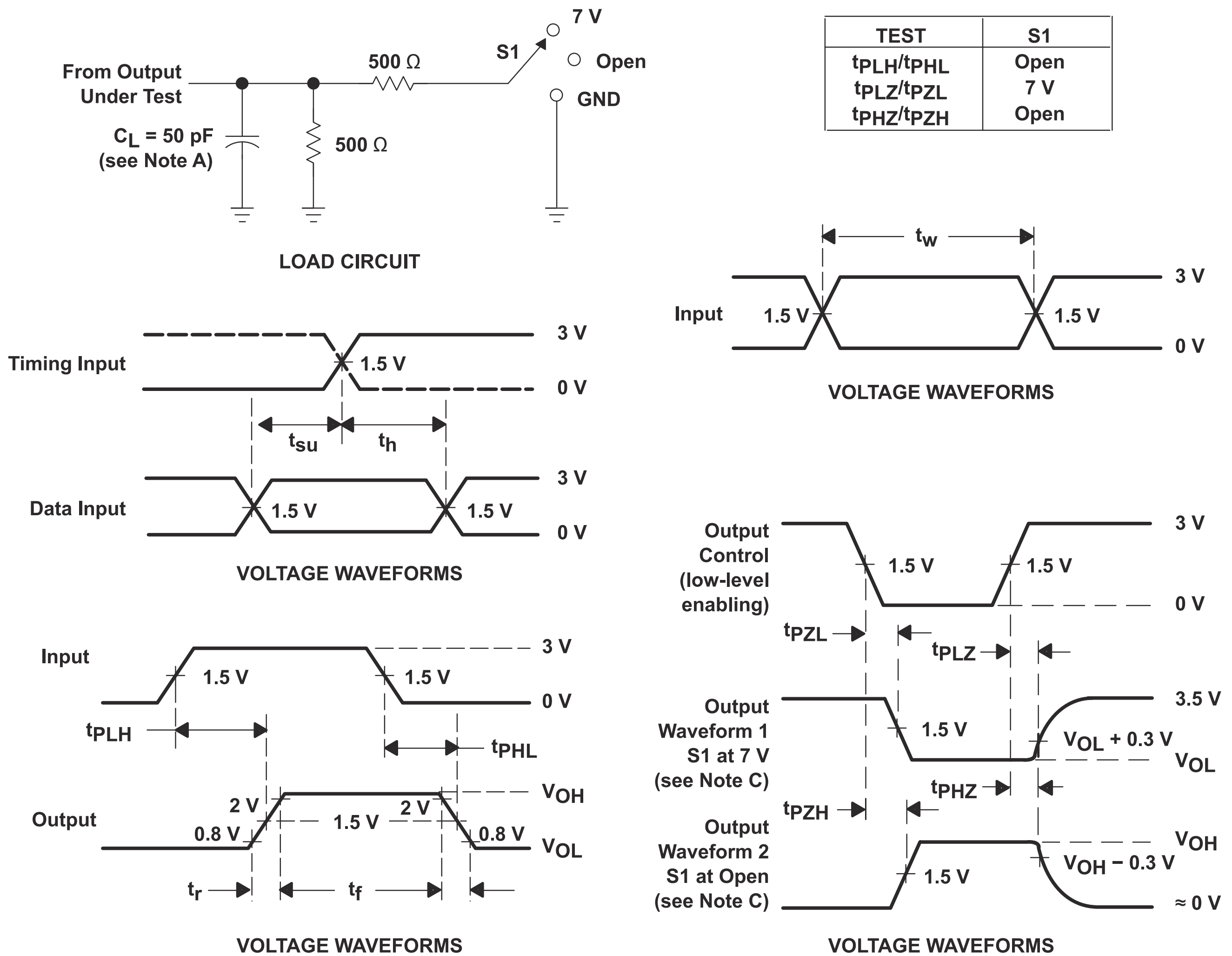
6.5 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (see Figure 6-1 and Figure 6-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
f_{max}			80			MHz
t_{PLH}	CLK	Any Y or Q	3		9	ns
t_{PHL}			3		9	
t_{PHL}	$\overline{CLR}$	Any Q	4		9	ns
t_{PZH}	$\overline{OE}$	Any Y or Q	2		7	ns
t_{PZL}			3		7	
t_{PHZ}	$\overline{OE}$	Any Y or Q	2		7	ns
t_{PLZ}			2		7	
$t_{sk(o)}$	CLK↑	Y↑			0.75	ns
		Q↑			0.9	
		Y↑ and Q↑			0.9	
t_r				0.9		ns
t_f				0.7		ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

7 Parameter Measurement Information



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	7 V
tPHZ/tPZH	Open

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 7-1. Load Circuit and Voltage Waveforms

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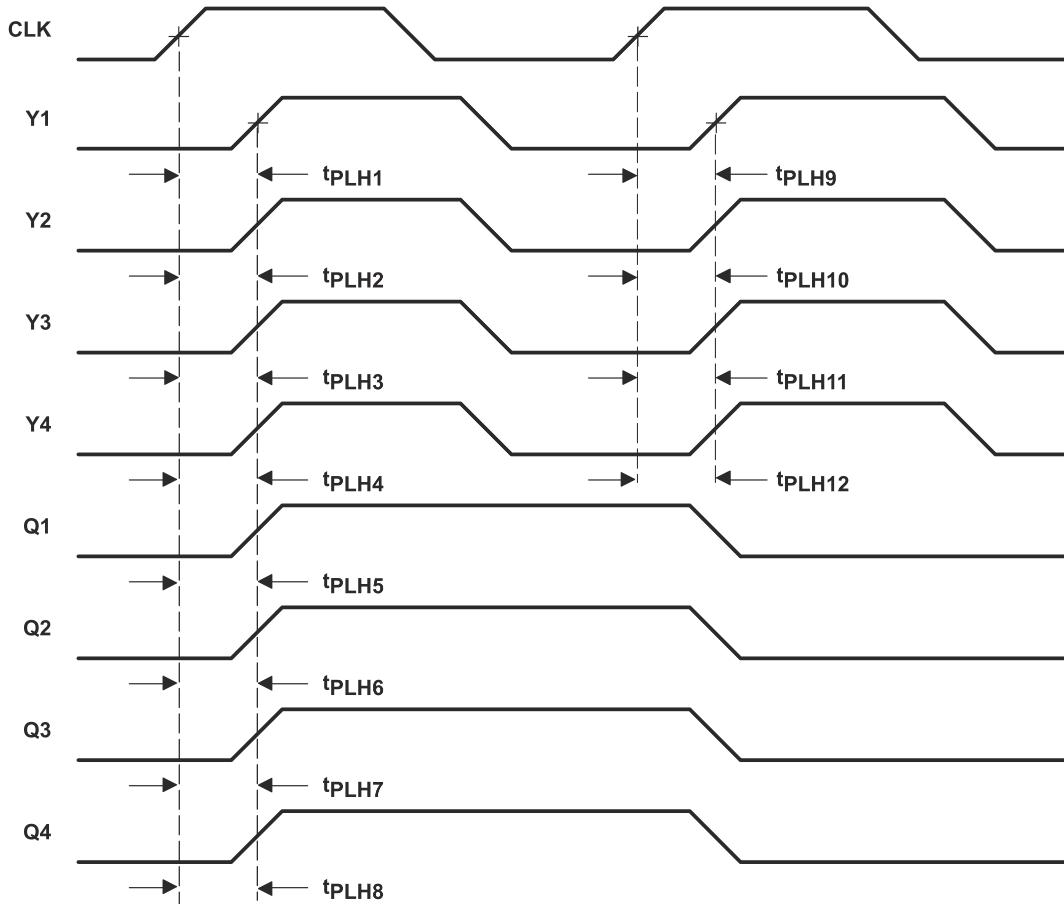

NOTES: A. Output skew, $t_{sk(o)}$, from CLK↑ to Y↑, is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4) or t_{PLHn} (n = 9, 10, 11, 12).

B. Output skew, $t_{sk(o)}$, from CLK↑ to Q↑, is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} (n = 5, 6, 7, 8).

C. Output skew, $t_{sk(o)}$, from CLK↑ to Y↑ and Q↑ , is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} (n=1,2, . . . ,8).

Figure 7-2. Skew Waveforms and Calculations

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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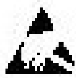
8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

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9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDC339DB	ACTIVE	SSOP	DB	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK339	Samples
CDC339DBG4	ACTIVE	SSOP	DB	20	70	TBD	Call TI	Call TI	-40 to 85		Samples
CDC339DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC339	Samples
CDC339DWG4	ACTIVE	SOIC	DW	20	25	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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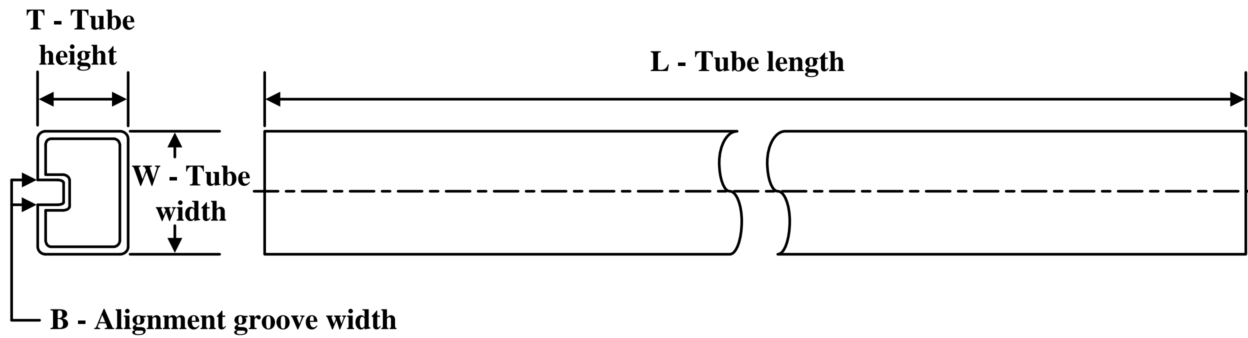
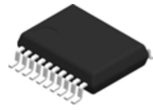
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDC339DB	DB	SSOP	20	70	530	10.5	4000	4.1
CDC339DW	DW	SOIC	20	25	507	12.83	5080	6.6



PACKAGE OUTLINE

SSOP - 2 mm max height

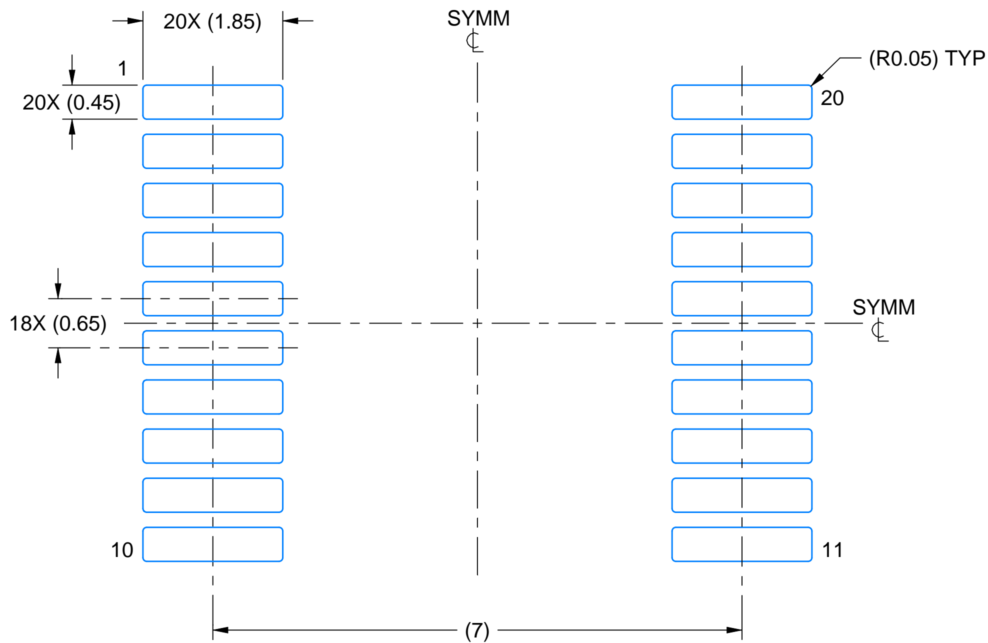
SMALL OUTLINE PACKAGE

A
8.2
7.4 TYP
PIN 1 INDEX AREA
1
10
20
11
18X 0.65
2X 5.85
7.5
6.9
NOTE 3
20X 0.38
0.22
0.1 Ⓜ C A B
B
5.6
5.0
NOTE 4
C
0.1 C
SEATING PLANE
SEE DETAIL A
(0.15) TYP
0.25
GAGE PLANE
2 MAX
0° -8°
0.95
0.55
0.05 MIN
DETAIL A
TYPICAL

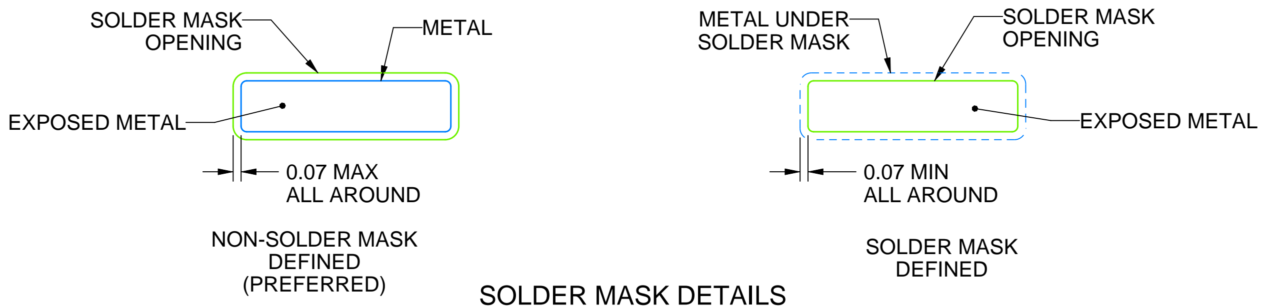
4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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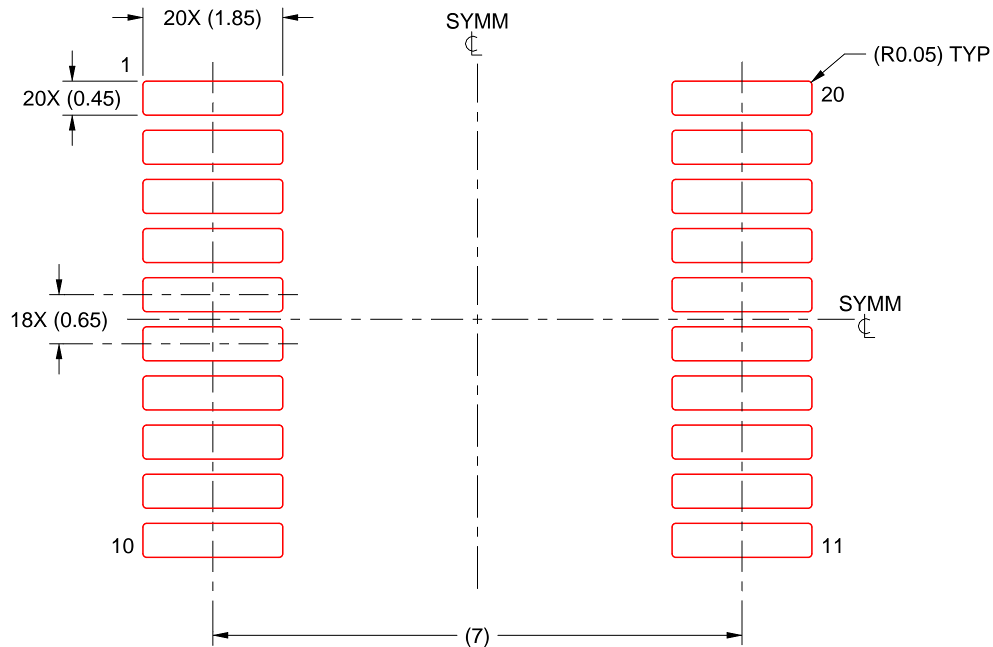
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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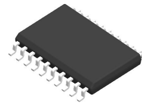
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
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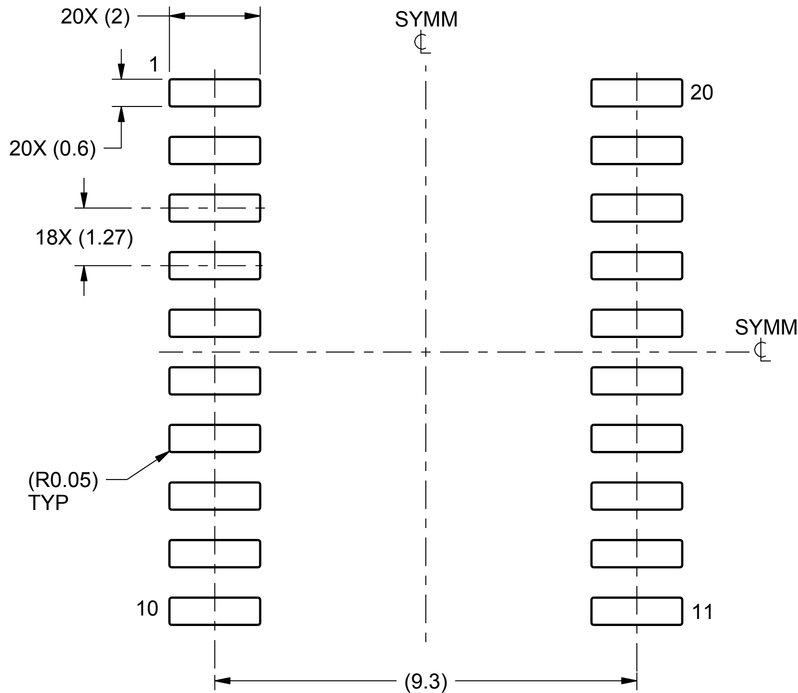
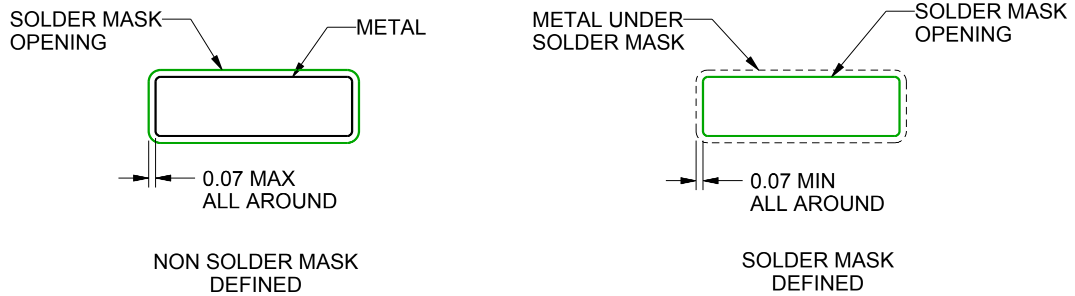
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

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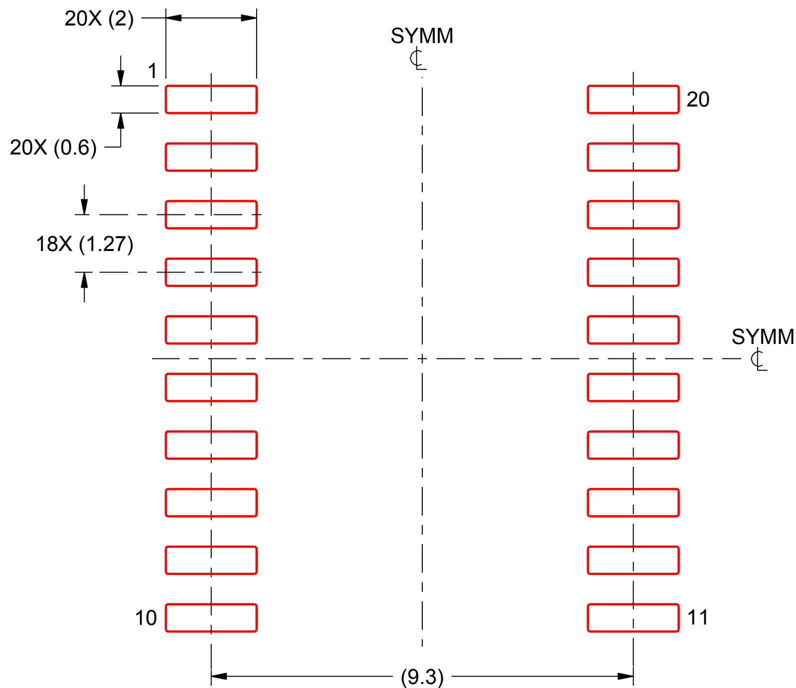
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

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9. Board assembly site may have different recommendations for stencil design.

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