# A General Guideline: How to Use the CDCF5801 for Phase Alignment/Adjustment

*Firoj Kabir* *CDC/HPA*

**ABSTRACT**

Unlike regular PLLs, the CDCF5801 has an extra phase aligner. Using this extra phase aligner, the CDCF5801 can align two different clock phases, even with different frequencies. Examples of where phase alignment may be useful include:

- Applications where two clock buffers' outputs need to be aligned
- Applications that require data synchronization with SERDES
- Applications that require static or dynamic phase adjustment

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## 1 Introduction

The CDF5801 is a low jitter clock multiplier (x1, x2, x4, and x8) with phase alignment/adjustment capability. The CDF5801 covers a wide input frequency range (12.5 MHz to 240 MHz) and output frequency range (25 MHz to 280 MHz). The CDF5801 has one single-ended input (with high sensitivity to accept LVPECL swing as well) and a differential output (it can be configured as LVTTL, LVPECL, HSTL, and LVDS signaling level). The CDCF5801 is characterized for operation over free-air temperatures of –40°C to 85°C. The CDCF5801 has two unique input pins for its phase aligner and using these pins the output clock phase can be controlled precisely.

### 1.1 Working Principal of the Phase Aligner

The CDCF5801 provides clock multiplication from a reference clock (REFCLK) signal with the unique capability to delay or advance the CLKOUT/CLKOUTB with steps of only 1.3 mUI through a phase aligner. For every rising edge on the DLYCTRL pin, the output clock is delayed by a 1.3 mUI or better step size as long as the LEADLAG input detects a low signal at the time of the DLYCTRL rising edge. Similarly, for every rising edge on the DLYCTRL pin, the output clock is advanced by a 1.3 mUI or better step size as long as the LEADLAG pin is high during the transition. This unique capability allows the CDF5801 to align phases (zero delay) between input and output clock, two clocks from different buffers, and even data and clock in some situations. It also provides the capability to program a fixed delay by providing the proper number of edges on the DLYCTRL pin, while strapping the LEADLAG pin to dc high or low.

## 2 Applications

The CDCF5801 can be configured in different ways to meet the specific requirements.

### 2.1 CDCF5801 as a Clock Multiplier

The CDCF5801 can be used a simple clock multiplier (x2, x4, and x8) without an external feedback. In this situation, the output clock has a phase delay with respect to the input clock. The input clock may come from an oscillator.

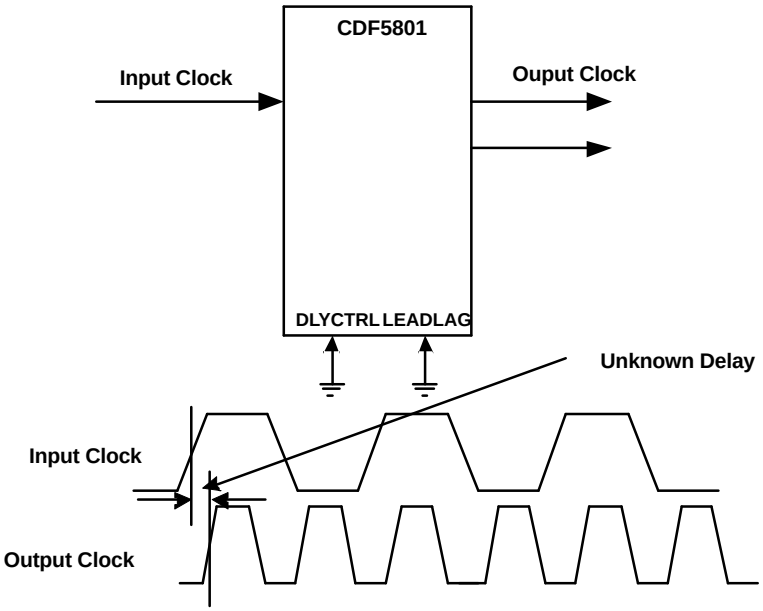


**Figure 1. A Simple Clock Multiplier and the Waveform**

### 2.2 CDCF5801 as a Zero Delay Clock Multiplier

Using the two inputs (LEADLAG and DLYCTRL) of the phase aligner and matching the line length, the CDCF5801 can be used as a zero delay clock multiplier. In this situation, the input clock and output clock are connected to the DLYCTRL and LEADLAG pins, respectively.

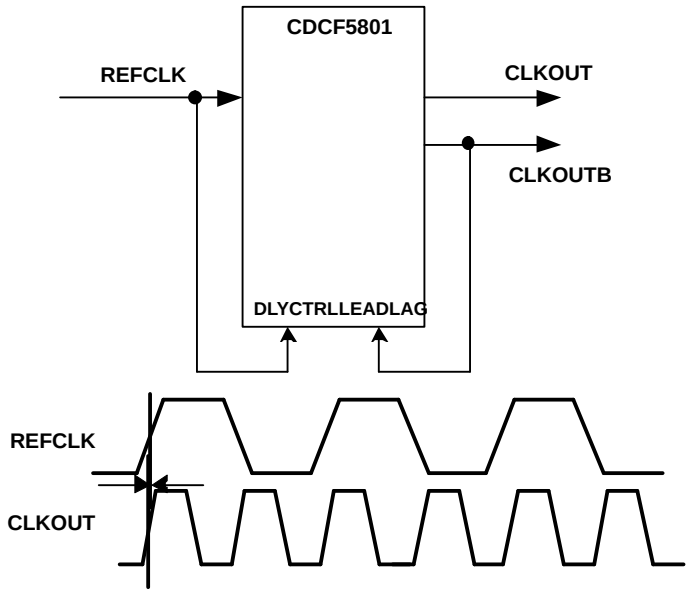


**Figure 2. Zero Delay Clock Multiplier and Waveform (Feedback from CLKOUTB)**

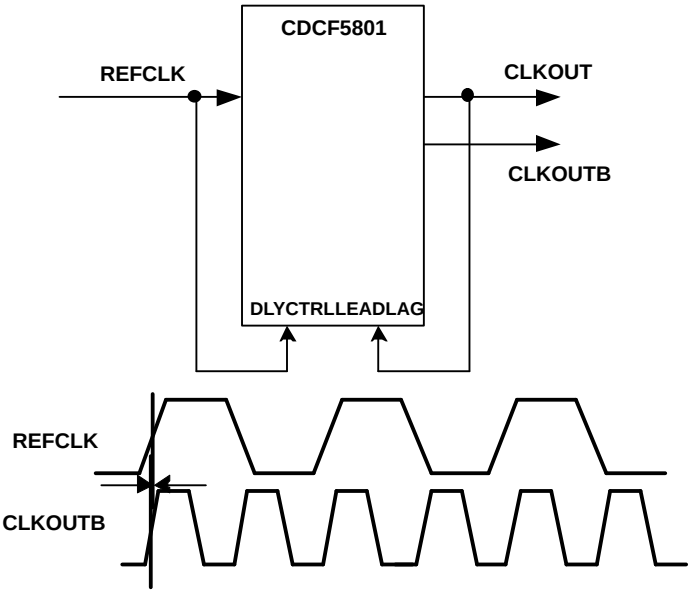


**Figure 3. Zero Delay Clock Multiplier and Waveform (Feedback from CLKOUT)**

## *2.3 Phase Aligning of the Outputs of Two Different Clock Drivers*

The CDCF5801 can also align the phases of two independent clock buffers. This function becomes necessary when two clock buffers are used in parallel with an input-to-output delay uncertainty exceeding the application's requirements.

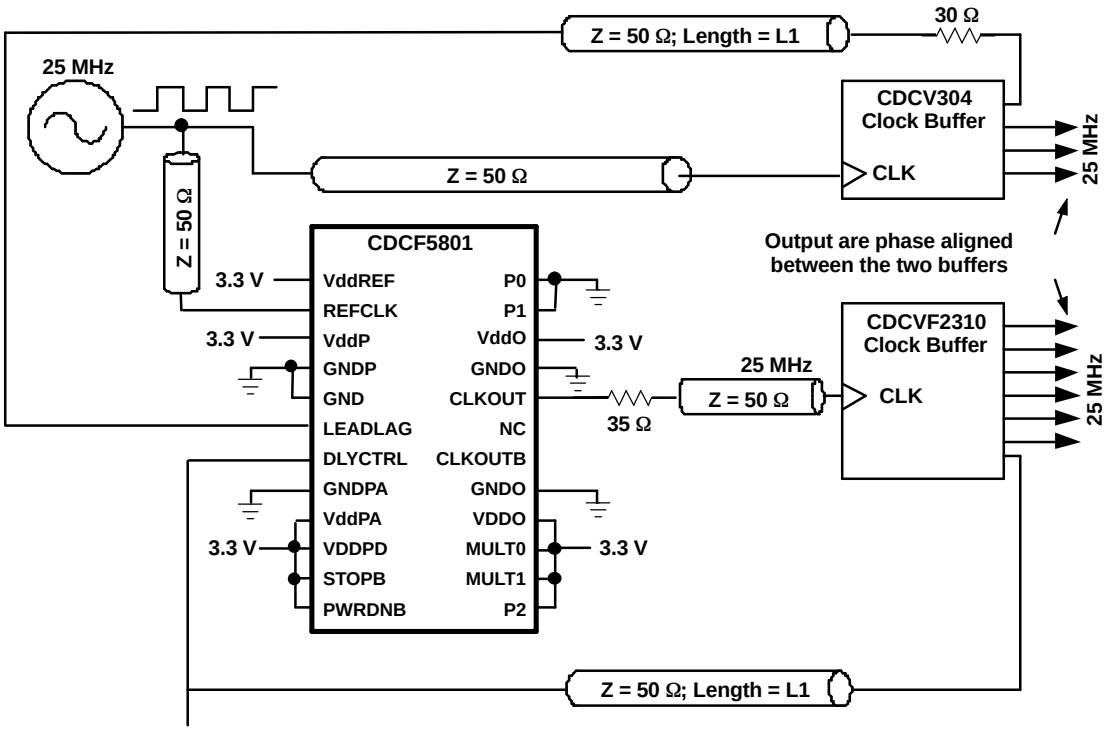


**Figure 4. Aligning Two Clock Buffers' Output Phases**

In Figure 4, the CDCV304 and CDCVF2310 are the two different clock buffers running in parallel. The phase aligner of the CDCF5801 (using LEADLAG and DLYCTRL inputs) compares the two phases' positions and advances or delays the output phase of the CDCF5801 (input of the CDCVF2310) and as a result, the two clock buffers' outputs are phase aligned. The advantage of using the CDCF5801 to align the phases is that the CDCF5801 can handle a relatively long length in its phase aligner inputs.

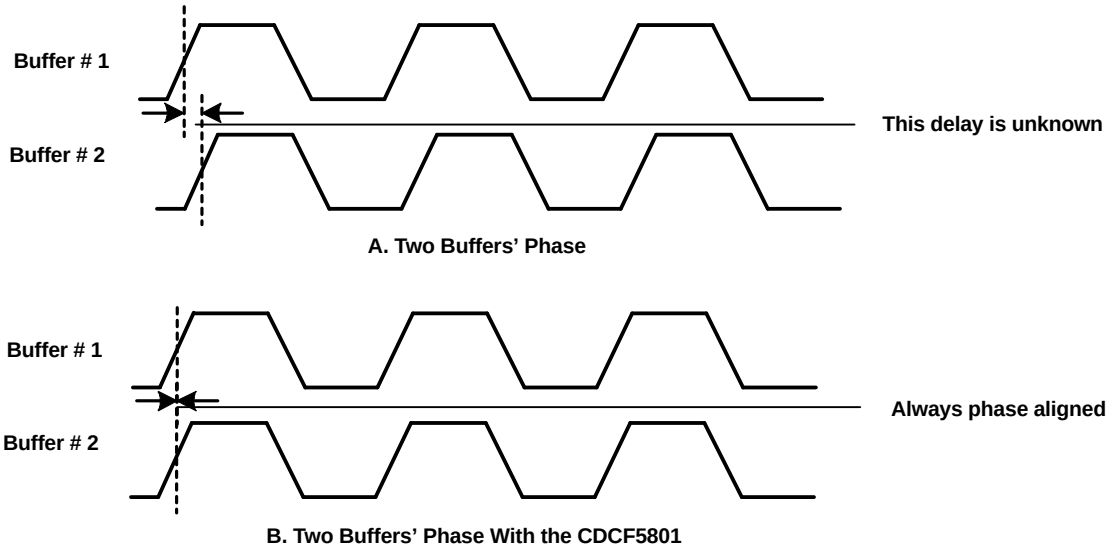


**Figure 5. Waveform Without and With Using the CDCF5801**

In Figure 4, a 25-MHz clock source has been shown and both buffers are using the same clock source. The CDCF5801 can also align the clock buffer outputs when the clock source for each buffer is

independent. In such case, the ppm frequency variation between the two clocks must be low. The frequency of the two clock signals at DLYCTRL and LEADLAG can also be an integer multiple of each other. If the DCF5801 is used as a multiplier, then the buffer output driven by the CDCF5801 (in the above example CDCVF2310) must be divided down to maintain the same or lower frequency than the signal frequency of the LEADLAG pin and then be connected to the DLYCTRL pin.

## 2.4 Advancing or Delaying the Clock Phase

After power up, the delay between the input and the output clock is unknown. However, the clock output phase can be advanced or delayed precisely with respect to its initial output clock phase position. Using a simple microcontroller, a required number of clock pulses can be generated to move the output clock phase. For example, if someone requires advancing the output clock phase by 90 degree (1/4$^{th}$ of the clock period) with respect to its initial position, the microcontroller needs to generate 198 clock pulses (assuming application is x1 and 200 MHz clock frequency; see Table 1 in the CDCF5801 data sheet) for the DLYCTRL pin and HIGH for the LEADLAG pin. The step size depends on the clock output frequency and the device's operating mode.

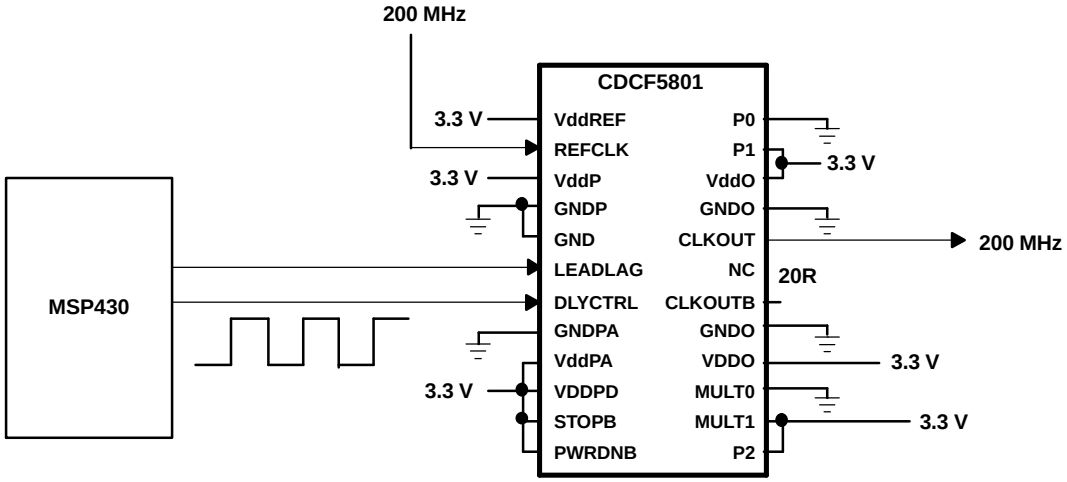


**Figure 6. CDCF5801 With a Microcontroller**

After sending the required the pulses, no reset is required.

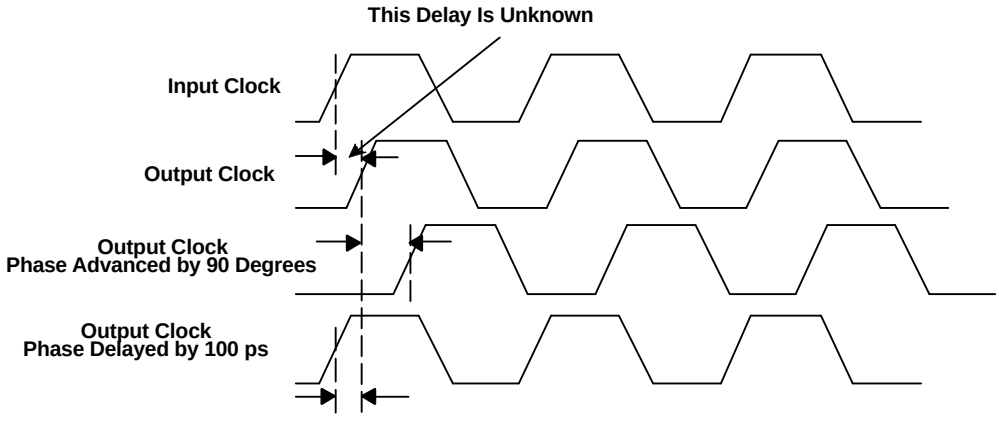


**Figure 7. CDCF5801 Output Phase Position With Respect to the Initial Output Phase**

## 2.5 Synchronizing Data and Clock

In many applications, FPGA drives SERDES (serilalizer and deserializer) and it often requires clean clocks to drive SERDES running the system properly.

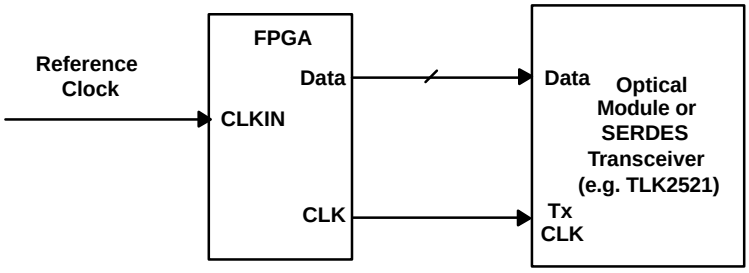


**Figure 8. Driving SERDES With FPGA Clock**

Figure 8 would be perfect if the SERDES did not require a clean clock or if FPGA could generate a clean clock. In real applications, switching noise from FPGA and long transmission line jitter impacts the SERDES TXCLK, resulting in transmit eye degradation.

Practically, the clock generated by FPGA is too noisy to drive SERDES. So, to get the lowest bit error operation from the SERDES, either we need to clean the FPGA clock or to bypass this FPGA clock and provide a clean clock from another source. If we use two separate ICs for data and clock, the real challenge is to synchronize the data and clock at the SERDES end. Using the phase aligning capability of the CDCF5801, we can easily solve the synchronization issue.

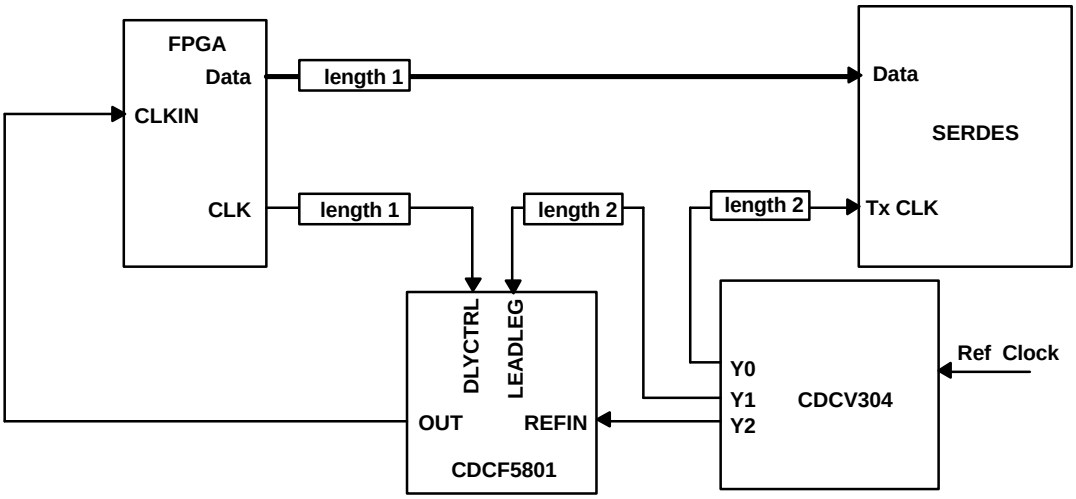


**Figure 9. Driving SERDES With an External Clean Clock and Data and Clock Synchronization**

In Figure 9, the CDCV304 (a simple clock buffer with low additive jitter) provides a clean clock to SERDES. The CDCF5801 synchronizes the data and clock at SERDES end by matching the line length. The clocks at LEADLAG and DLYCTRL pins are always aligned by the phase aligning action of the CDCF5801. The data line length (from FPGA to SERDES) and clock line length (from FPGA to DLYCTRL) are equal and clock lengths (from the CDCV304 to LEADLAG and TXCLK) are the same; therefore the data and clock at SERDES end will be synchronized.

In many applications, expensive skew controlled clocks are used. The jitter specifications of this type of clock often do not meet the SERDES requirements and as output skew is fixed by the static programming, it can not respond correctly when the delay between CLKIN and CLK of FPGA is changed due to temperature, supply voltage, or process variations.

The CDCF5801 synchronizes the data and clock phase dynamically; any delay variation is adjusted when it is required.

If there is a noisy system and the clock needs to be multiplied up, a PLL based jitter cleaner (the CDC7005 with an external clean VCXO) can provide the required clock (multiplication and low phase noise clock) for SERDES.

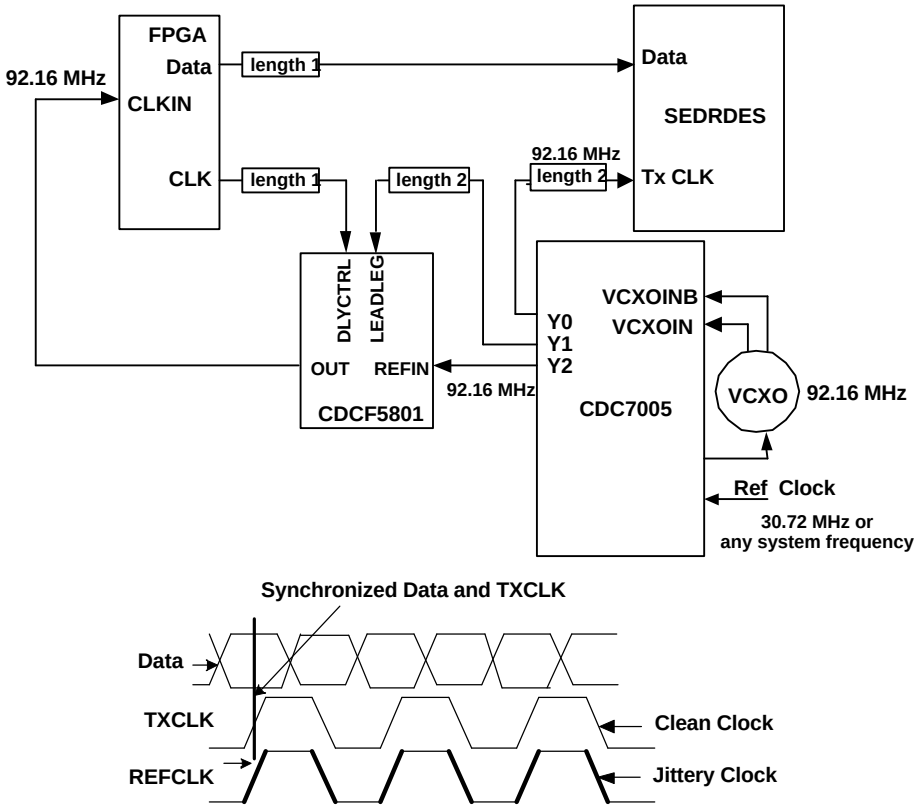


**Figure 10. Cleaning Jitter and Driving SERDES With External Clock and Waveform**

## 3 Configuring the CDCF5801 Outputs

The output of the CDCF5801 is differential. These outputs are complementary, not true differential. So, the outputs can be configured as LVCMOS (CLKOUT is 180 degrees out of phase with CLKOUTB), LVPECL, LVDS, or any other signaling level.

The following figures show how we typically achieve the different signaling levels and common-mode voltages using simple resistors.

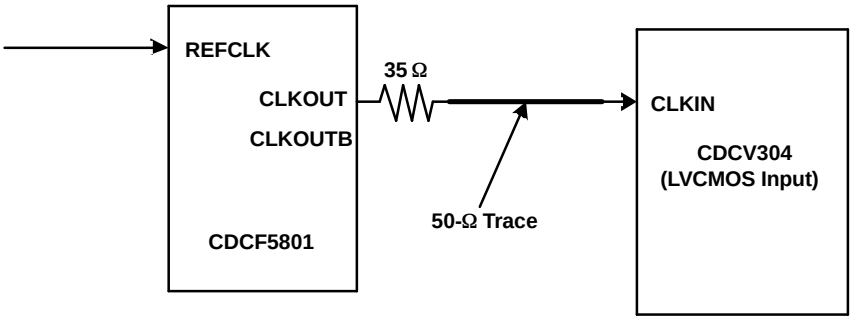


**Figure 11. Driving the LVCMOS/LVTTL Receiver by the CDCF5801**

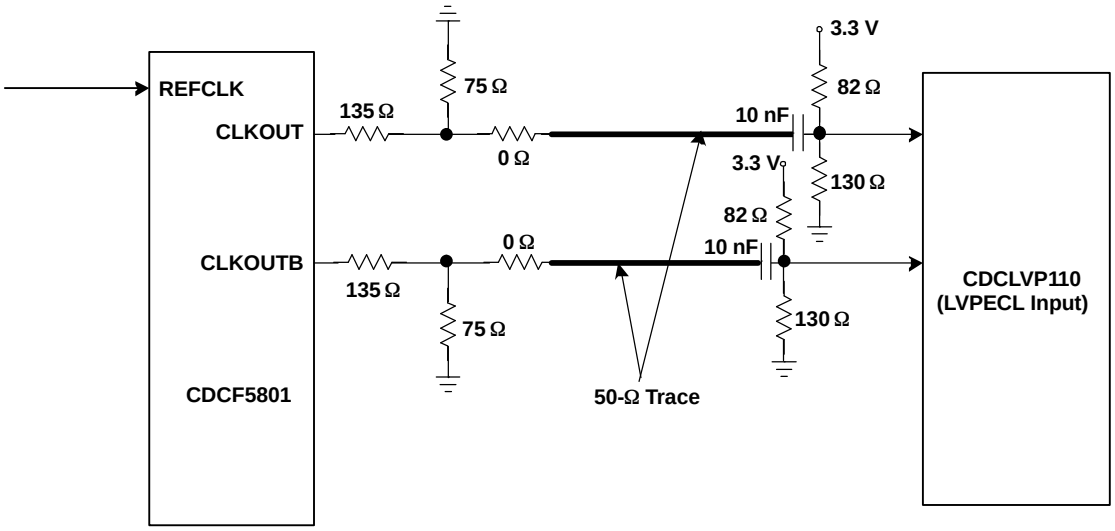


**Figure 12. Driving the LVPECL Receiver by the CDCF5801**

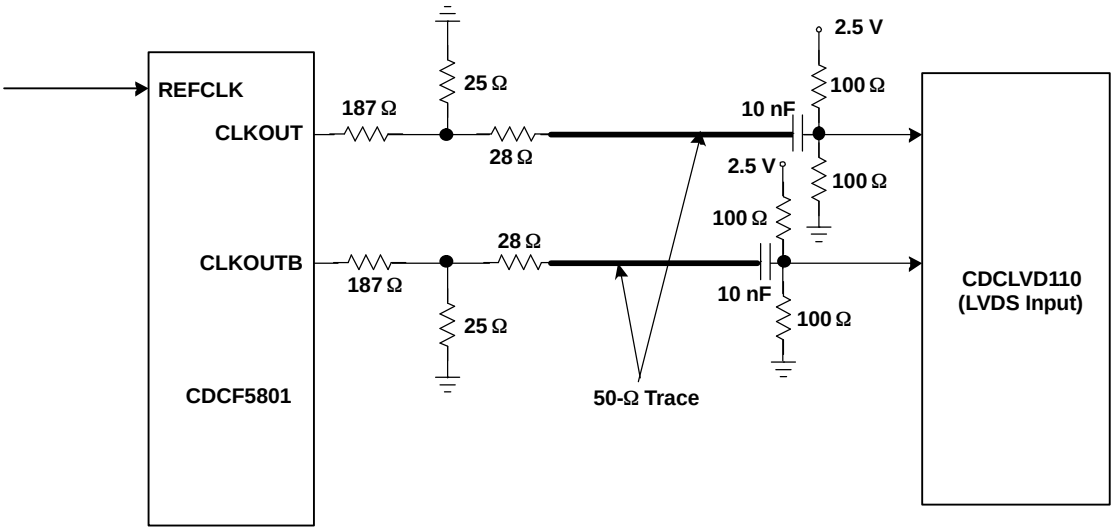


**Figure 13. Driving the LVDS Receiver by the CDCF5801**

In order to meet the receiver's requirements (signal swing, common-mode voltage, etc.), it may be required to change the value of the divider resistors. Proper termination is required to avoid any signal integrity problem issue.

## 4 Decoupling Power Supply

PLL based clock drivers and generators are sensitive to noise on the power supply. Noise on the power supply can dramatically increase the jitter of the PLL. It is required to reduce noise from the system power supply, especially when jitter is critical to applications.

Filter capacitors are used to eliminate the low frequency noise from power supply, where as, the bypass capacitors provide the low impedance path for high frequency noise and guard the power supply system against the induced fluctuations. Inserting a ferrite bead between the board power supply and analog VCC isolates the high frequency switching noises generated the clock driver by preventing them from interrupting the board supply. The digital power supply (VCC) should be decoupled with a filter capacitor. Figure 14 shows a general a recommendation for decoupling the analog power supply.

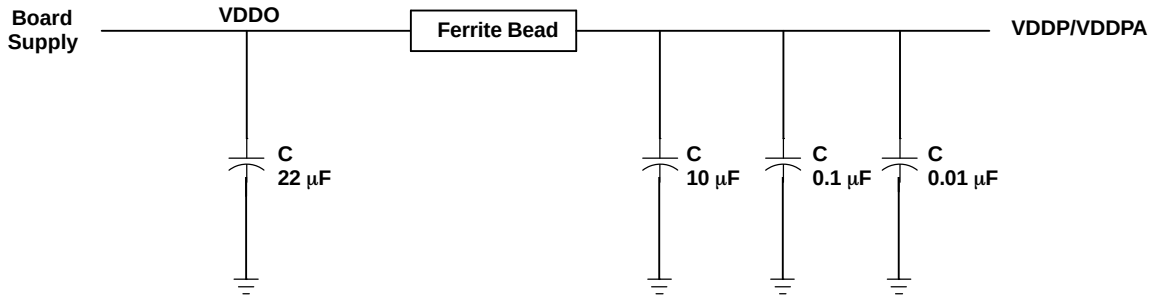


**Figure 14. Example of Decoupling for Analog Power Supply**

## 5 Conclusion

The CDCF5801 offers more flexibility and can be configured many ways in order to fit into certain applications. The dynamic phase alignment capability of the CDCF5801 is especially unique, which could be an attractive solution for many applications.

The CDC5801 is a similar kind of device with phase aligning/adjustment capability. The CDC5801 is optimized for higher frequency applications.

## 6 References

1. *CDCF5801 Clock Multiplier With Delay Control and Phase Alignment* data sheet, Texas Instruments, (SCAS643)
2. *CDC5801 Low Jitter Clock Multiplier and Divider With Programmable Delay and Phase Alignment* data sheet, Texas Instruments, (SCAS682)

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