

# CDCLVP111-SP Low-Voltage 1:10 LVPECL With Selectable Input Clock Driver

## 1 Features

- Distributes One Differential Clock Input Pair LVPECL to 10 Differential LVPECL
- Fully Compatible With LVECL and LVPECL
- Supports a Wide Supply Voltage Range From 2.375 V to 3.8 V
- Selectable Clock Input Through CLK\_SEL
- Low-Output Skew (Typical 15 ps) for Clock-Distribution Applications
  - Additive Jitter Less Than 1 ps
  - Propagation Delay Less Than 355 ps
  - Open Input Default State
  - LVDS, CML, SSTL input Compatible
- $V_{BB}$  Reference Voltage Output for Single-Ended Clocking
- Frequency Range From DC to 3.5 GHz
- **Supports Defense, Aerospace, and Medical Applications**
  - Controlled Baseline
  - One Assembly and Test Site
  - One Fabrication Site
  - Available in Military (–55°C to 125°C) Temperature Range <sup>(1)</sup>
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability

## 2 Applications

- Designed for Driving 50-Ω Transmission Lines
- High-Performance Clock Distribution
- Engineering Evaluation (/EM) Samples Are Available <sup>(2)</sup>

- (1) Custom temperature ranges available.
- (2) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (that is, no burn-in, and so forth) and are tested to a temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing, or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C operating life.

## 3 Description

The CDCLVP111-SP clock driver distributes one differential clock pair of LVPECL input, (CLK0, CLK1) to ten pairs of differential LVPECL clock (Q0, Q9) outputs with minimum skew for clock distribution. The CDCLVP111-SP can accept two clock sources into an input multiplexer. The CDCLVP111-SP is specifically designed for driving 50-Ω transmission lines. When an output pin is not used, leaving it open is recommended to reduce power consumption. If only one of the output pins from a differential pair is used, the other output pin must be identically terminated to 50 Ω.

The  $V_{BB}$  reference voltage output is used if single-ended input operation is required. In this case, the  $V_{BB}$  pin should be connected to  $\overline{\text{CLK0}}$  and bypassed to GND via a 10-nF capacitor.

For high-speed performance, the differential mode is strongly recommended.

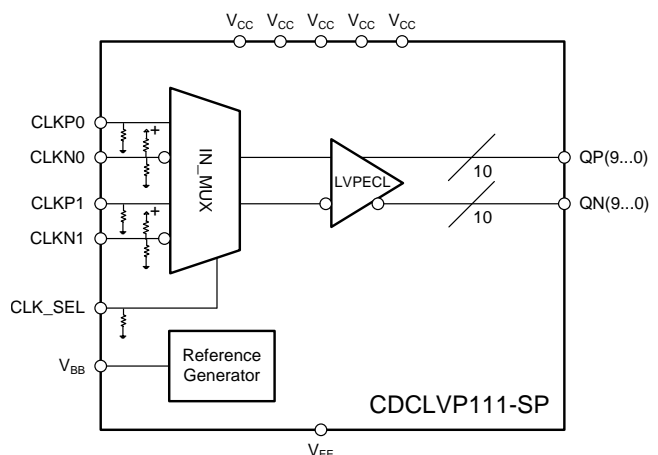
The CDCLVP111-SP is characterized for operation from –55°C to 125°C.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCLVP111-SP	HFG (36)	9.08 mm x 9.08 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Functional Block Diagram



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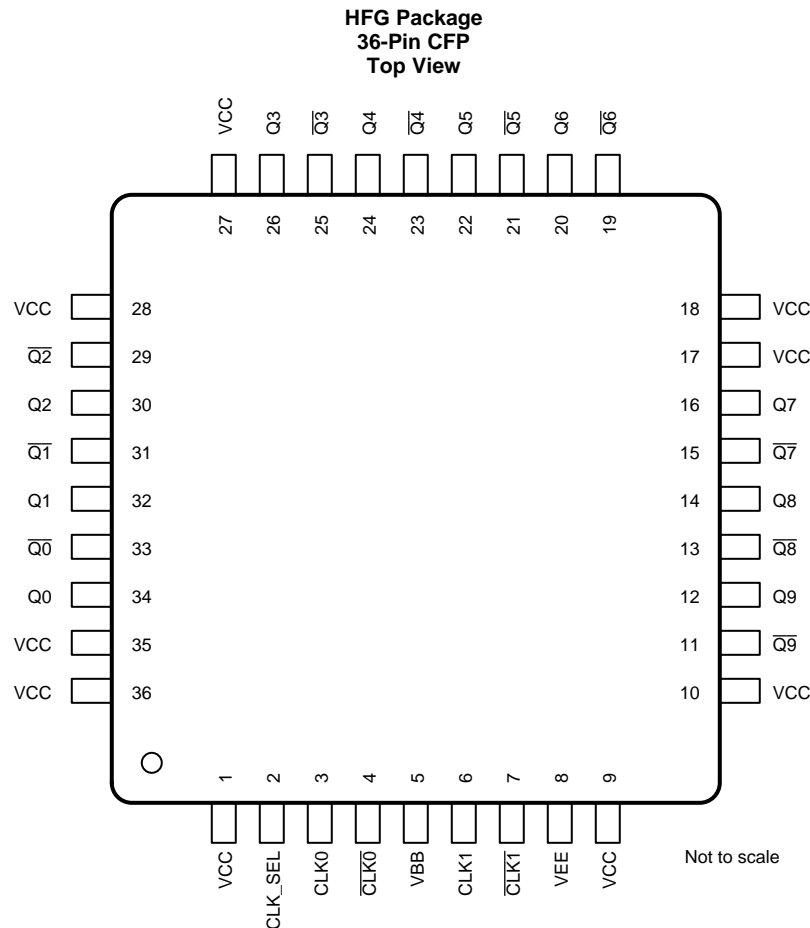
## 4 Revision History

### Changes from Original (November 2016) to Revision A

Page

- Added engineering evaluation samples bullet and footnote to the *Applications* section..... **1**

## 5 Pin Configuration and Functions



**Pin Functions<sup>(1)</sup>**

PIN		TYPE	DESCRIPTION
NAME	NO.		
CLK_SEL	2	Input	Clock select. Used to select between CLK0 and CLK1 input pairs. LVTTTL/LVCMOS functionality compatible.
CLK0, $\overline{\text{CLK0}}$	3, 4	Input	Differential LVECL/LVPECL input pair.
CLK1, $\overline{\text{CLK1}}$	6, 7	Input	
Q[9:0]	12, 14, 16, 20, 22, 24, 26, 30, 32, 34	Output	LVECL/LVPECL clock outputs, these outputs provide low-skew copies of CLKn.
$\overline{\text{Q}}[9:0]$	11, 13, 15, 19, 21, 23, 25, 29, 31, 33	Output	LVECL/LVPECL complementary clock outputs, these outputs provide copies of $\overline{\text{CLKn}}$ .
V <sub>BB</sub>	5	Power	Reference voltage output for single-ended input operation.
V <sub>CC</sub>	1, 9, 10, 17, 18, 27, 28, 35, 36	Power	Supply voltage.
V <sub>EE</sub>	8	Power	Device ground or negative supply voltage in ECL mode.

(1) CLKn, CLK\_SEL pull down resistor = 75 kΩ;  $\overline{\text{CLKn}}$  pull up resistor = 37.5 kΩ;  $\overline{\text{CLKn}}$  pull down resistor = 50 kΩ.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

see <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage (relative to V <sub>EE</sub> )	−0.3	4.6	V
V <sub>I</sub>	Input voltage	−0.3	V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	Output voltage	−0.3	V <sub>CC</sub> + 0.5	V
I <sub>IN</sub>	Input current		±20	mA
V <sub>EE</sub>	Negative supply voltage (relative to V <sub>CC</sub> )	−4.6	0.3	V
I <sub>BB</sub>	Sink/source current	−1	1	mA
I <sub>O</sub>	DC output current	−50		mA
T <sub>J</sub>	Maximum operating junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage (relative to V <sub>EE</sub> )	2.375	2.5/3.3	3.8	V
T <sub>J</sub>	Operating junction temperature	−55		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		CDCLVP111-SP	UNIT
		HFG (CFP)	
		36 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2)</sup>	107.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	33.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	98.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	29.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	91.36	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	13.4	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

- (2) According to JESD 51-7 standard.

## 6.5 LVECL DC Electrical Characteristics

V<sub>supply</sub>: V<sub>CC</sub> = 0 V, V<sub>EE</sub> = –2.375 V to –3.8 V over operating temperature range T<sub>J</sub> = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>EE</sub>	Supply internal current Absolute value of current	–55°C, 25°C, 125°C	30	85	mA
I <sub>CC</sub>	Output and internal supply current All outputs terminated 50 Ω to V <sub>CC</sub> – 2 V	–55°C, 25°C		385	mA
		125°C		405	
I <sub>IN</sub>	Input current Includes pullup and pulldown resistors, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = V <sub>CC</sub> – 2 V	–55°C, 25°C, 125°C	–150	150	μA
V <sub>BB</sub>	Internally generated bias voltage For V <sub>EE</sub> = –3 V to –3.8 V, I <sub>BB</sub> = –0.2 mA	–55°C, 25°C, 125°C	–1.45	–1.3	V
	V <sub>EE</sub> = –2.375 V to –2.75 V, I <sub>BB</sub> = –0.2 mA	–55°C, 25°C, 125°C	–1.3	–1.25	
V <sub>IH</sub>	High-level input voltage (CLK_SEL)	–55°C, 25°C, 125°C	–1.165	–0.88	V
V <sub>IL</sub>	Low-level input voltage (CLK_SEL)	–55°C, 25°C, 125°C	–1.81	–1.475	V
V <sub>ID</sub>	Input amplitude (CLK <sub>n</sub> , CLK <sub>n</sub> ) Difference of input, see <sup>(1)</sup> ,  V <sub>IH</sub> – V <sub>IL</sub>	–55°C, 25°C, 125°C	0.5	1.3	V
V <sub>CM</sub>	Common-mode voltage (CLK <sub>n</sub> , CLK <sub>n</sub> ) DC offset relative to V <sub>EE</sub>	–55°C, 25°C, 125°C	V <sub>EE</sub> + 1	–0.3	V
V <sub>OH</sub>	High-level output voltage I <sub>OH</sub> = –21 mA	–55°C	–1.26	–0.85	V
		25°C	–1.2	–0.85	
		125°C	–1.15	–0.8	
V <sub>OL</sub>	Low-level output voltage I <sub>OL</sub> = –5 mA	25°C	–1.85	–1.425	V
		–55°C, 125°C	–1.85	–1.25	
V <sub>OD</sub>	Differential output voltage swing Terminated with 50 Ω to V <sub>CC</sub> – 2 V, see Figure 4	–55°C, 25°C, 125°C	350		mV

(1) V<sub>ID</sub> minimum and maximum is required to maintain AC specifications, actual device function tolerates a minimum V<sub>ID</sub> of 100 mV.

## 6.6 LVPECL DC Electrical Characteristics

V<sub>supply</sub>: V<sub>CC</sub> = 2.375 V to 3.8 V, V<sub>EE</sub> = 0 V over operating temperature range T<sub>J</sub> = –55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN			TYP			MAX			UNIT
I <sub>EE</sub>	Supply internal current	Absolute value of current		–55°C, 25°C, 125°C			30			85			mA
I <sub>CC</sub>	Output and internal supply current	All outputs terminated 50 Ω to V <sub>CC</sub> – 2 V		–55°C, 25°C						385			mA
				125°C						405			
I <sub>IN</sub>	Input current	Includes pullup and pulldown resistors V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = V <sub>CC</sub> – 2 V		–55°C, 25°C, 125°C			–150			150			μA
V <sub>BB</sub>	Internally generated bias voltage	V <sub>CC</sub> = 3 V to 3.8 V, I <sub>BB</sub> = –0.2 mA		–55°C, 25°C, 125°C			V <sub>CC</sub> – 1.45		V <sub>CC</sub> – 1.3		V <sub>CC</sub> – 1.125		V
		V <sub>CC</sub> = 2.375 V to 2.75 V, I <sub>BB</sub> = –0.2 mA		–55°C, 25°C, 125°C			V <sub>CC</sub> – 1.3		V <sub>CC</sub> – 1.25		V <sub>CC</sub> – 1.1		
V <sub>IH</sub>	High-level input voltage (CLK_SEL)			–55°C, 25°C, 125°C			V <sub>CC</sub> – 1.165			V <sub>CC</sub> – 0.88			V
V <sub>IL</sub>	Low-level input voltage (CLK_SEL)			–55°C, 25°C, 125°C			V <sub>CC</sub> – 1.81			V <sub>CC</sub> – 1.475			V
V <sub>ID</sub>	Input amplitude (CLK <sub>n</sub> , CLK <sub>n</sub> )	Difference of input, see <sup>(1)</sup> ,  V <sub>IH</sub> – V <sub>IL</sub>		–55°C, 25°C, 125°C			0.5			1.3			V
V <sub>CM</sub>	Common-mode voltage (CLK <sub>n</sub> , CLK <sub>n</sub> )	DC offset relative to V <sub>EE</sub>		–55°C, 25°C, 125°C			1			V <sub>CC</sub> – 0.3			V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = –21 mA		–55°C			V <sub>CC</sub> – 1.26			V <sub>CC</sub> – 0.85			V
				25°C			V <sub>CC</sub> – 1.2			V <sub>CC</sub> – 0.85			
				125°C			V <sub>CC</sub> – 1.15			V <sub>CC</sub> – 0.8			
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = –5 mA		25°C			V <sub>CC</sub> – 1.85			V <sub>CC</sub> – 1.425			V
				–55°C, 125°C			V <sub>CC</sub> – 1.85			V <sub>CC</sub> – 1.25			
V <sub>OD</sub>	Differential output voltage swing	Terminated with 50 Ω to V <sub>CC</sub> – 2 V, see Figure 4		–55°C, 25°C, 125°C			350						mV

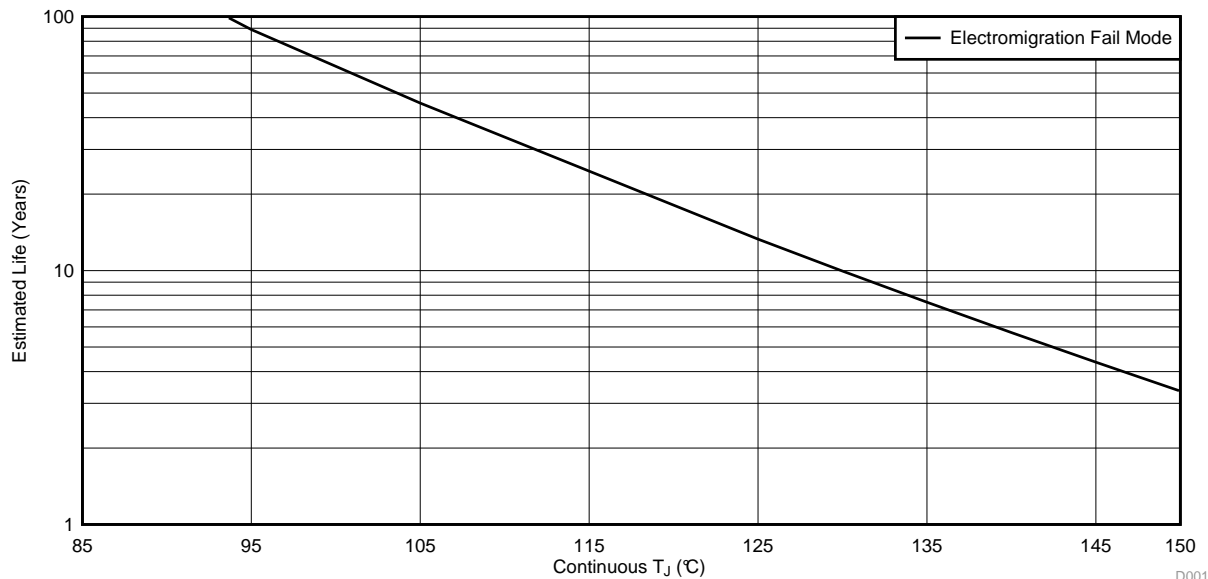
(1) V<sub>ID</sub> minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V<sub>ID</sub> of 100 mV.

## 6.7 AC Electrical Characteristics

V<sub>supply</sub>: V<sub>CC</sub> = 2.375 V to 3.8 V, V<sub>EE</sub> = 0 V or LVECL/LVPECL input V<sub>CC</sub> = 0 V, V<sub>EE</sub> = –2.375 V to –3.8 V over operating temperature range T<sub>J</sub> = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>pd</sub>	Differential propagation delay CLK <sub>n</sub> , CLK <sub>n</sub> to all Q0, Q0... Q9, Q9	See note D in <a href="#">Figure 2</a>	100	355	ps
t <sub>sk(o)</sub>	Output-to-output skew	See notes A and D in <a href="#">Figure 2</a>	15	50	ps
t <sub>sk(pp)</sub>	Part-to-part skew	See notes B and D in <a href="#">Figure 2</a>	70		ps
t <sub>aj</sub>	Additive phase jitter <sup>(1)</sup>	Integration bandwidth of 20 kHz to 20 MHz, f <sub>out</sub> = 200 MHz at 25°C	0.125	0.8	ps
f <sub>(max)</sub>	Maximum frequency <sup>(1)</sup>	Functional up to 3.5 GHz, see <a href="#">Figure 4</a>		3500	MHz
t <sub>r</sub> /t <sub>f</sub>	Output rise and fall time (20%, 80%)	See note D in <a href="#">Figure 2</a>		240	ps

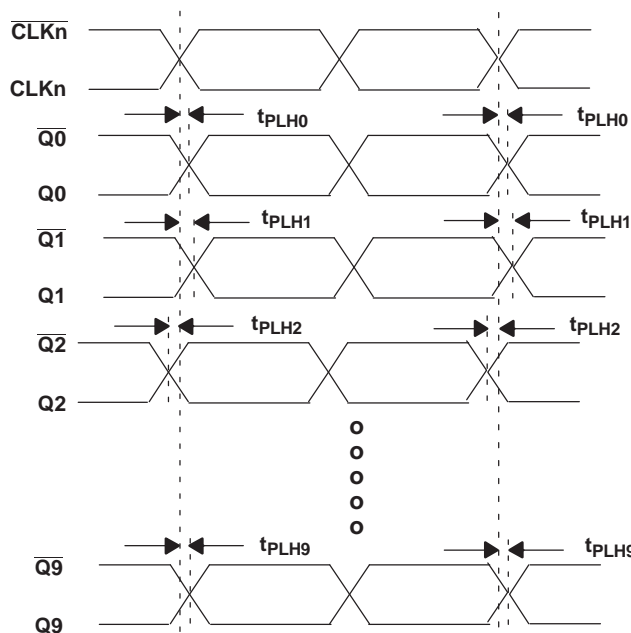
(1) Specified by bench characterization and is not tested in production.



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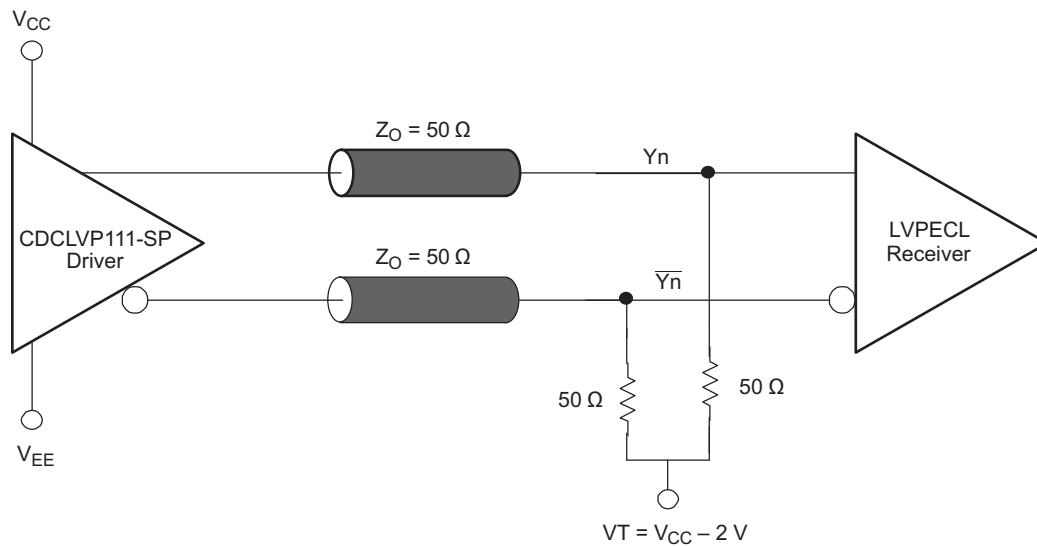
- (1) See data sheet for absolute maximum and minimum recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

**Figure 1. CDCLVP111-SP Operating Life Derating Chart**



- A. Output skew is calculated as the greater of: the difference between the fastest and the slowest  $t_{PLHn}$  ( $n = 0, 1, \dots, 9$ ) or the difference between the fastest and the slowest  $t_{PHLn}$  ( $n = 0, 1, \dots, 9$ ).
- B. Part-to-part skew, is calculated as the greater of: The difference between the fastest and the slowest  $t_{PLHn}$  ( $n = 0, 1, \dots, 9$ ) across multiple devices or the difference between the fastest and the slowest  $t_{PHLn}$  ( $n = 0, 1, \dots, 9$ ) across multiple devices.
- C. Typical value measured at ambient when clock input is 155.52 MHz for an integration bandwidth of 20 kHz to 5 MHz.
- D. Input conditions:  $V_{CM} = 1$  V,  $V_{ID} = 0.5$  V and  $F_{IN} = 1$  GHz.

**Figure 2. Waveform for Calculating Both Output and Part-to-Part Skew**

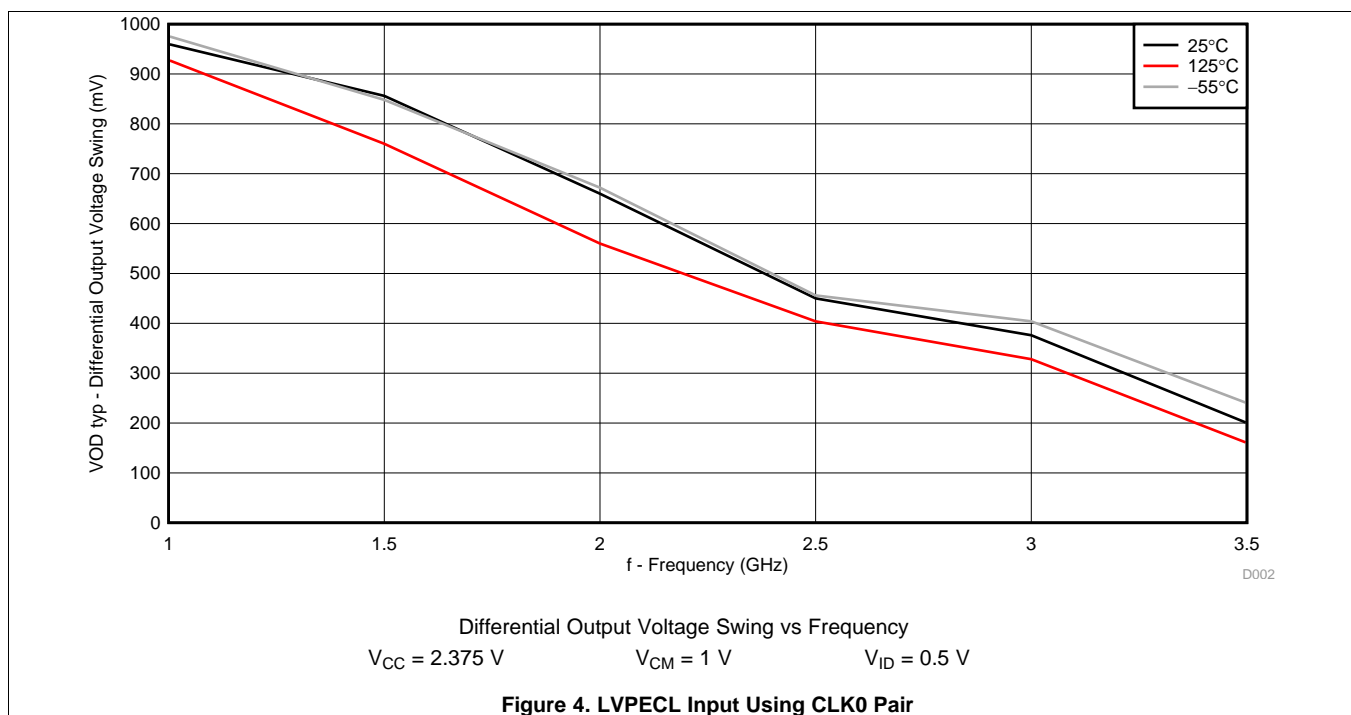


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See *Interfacing Between LVPECL, LVDS, and CML* (SCAA056).

### Figure 3. Typical Termination for Output Driver

## 6.8 Typical Characteristics



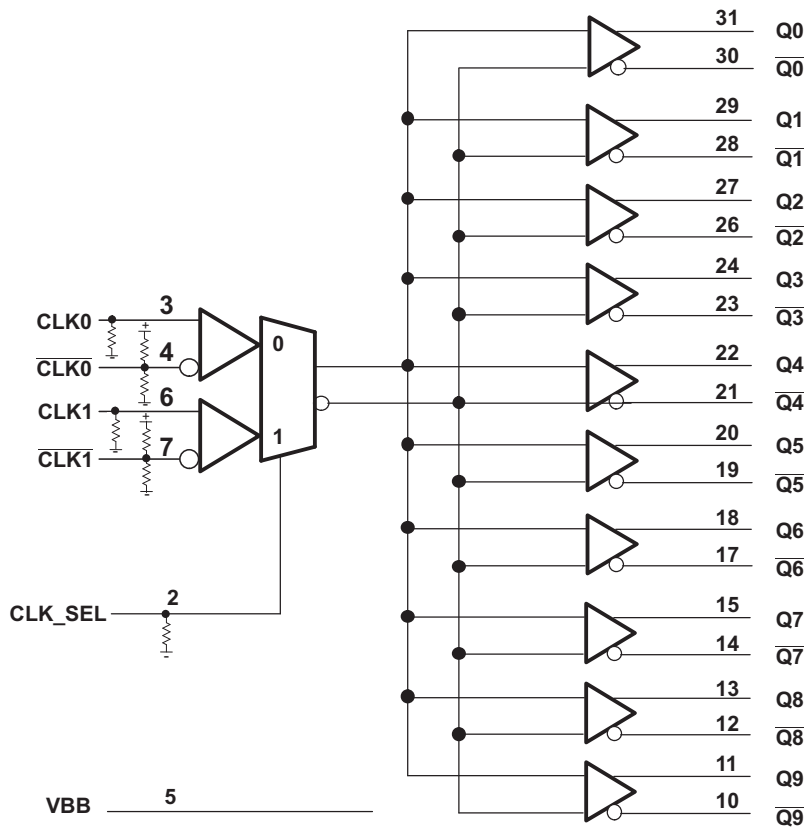


## 7 Detailed Description

### 7.1 Overview

The CDCLVP111-SP is an open emitter for LVPECL outputs. Therefore, proper biasing and termination are required to ensure correct operation of the device and to minimize signal integrity. The proper termination for LVPECL outputs is  $50\ \Omega$  to  $(V_{CC} - 2)$ , but this DC voltage is not readily available on PCB. Therefore, a Thevenin equivalent circuit is worked out for the LVPECL termination in both direct-coupled (DC) and AC-coupled configurations. These configurations are shown in [Figure 6](#) (a and b) for  $V_{CC} = 2.5\text{ V}$  and [Figure 7](#) (a and b) for  $V_{CC} = 3.3\text{ V}$ , respectively. TI recommends to place all resistive components close to either the driver end or the receiver end. If the supply voltage for the driver and receiver is different, AC coupling is required.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The CDCLVP111-SP is a low-additive jitter universal to LVPECL fan out buffer with 2 selectable inputs. The small package, low-output skew, and low-additive jitter make for a flexible device in demanding applications.

## 7.4 Device Functional Modes

Select input terminal by CLK\_SEL pin.

**Table 1. Function Table**

CLK_SEL	ACTIVE CLOCK INPUT
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$

The two inputs of the CDCLVP111-SP are internally mixed together and can be selected through the control pin. Unused inputs and outputs can be left floating to reduce overall component cost. Both AC and DC coupling schemes can be used with the CDCLVP111-SP to provide greater system flexibility.

## 8 Application and Implementation

### NOTE

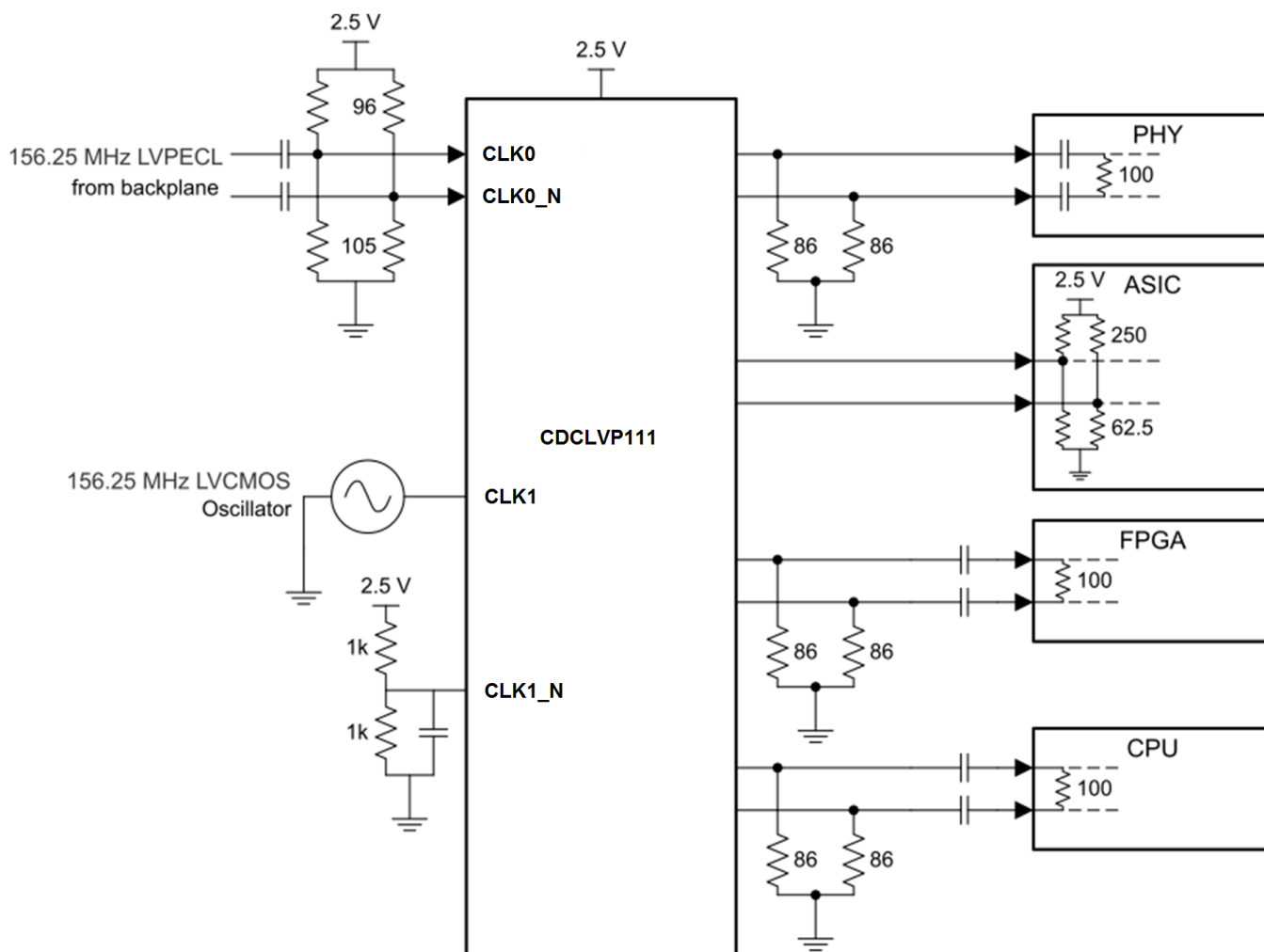
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The CDCLVP111-SP is a low-additive jitter LVPECL fanout buffer that can generate 5 copies of 2 selectable LVDS, CML or SSTL inputs. The CDCLVP111-SP can accept reference clock frequencies up to 3.5 GHz while providing low-output skew.

### 8.2 Typical Application

#### 8.2.1 Fanout Buffer for Line Card Application



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**Figure 5. CDCLVP111-SP Block Diagram**

## Typical Application (continued)

### 8.2.1.1 Design Requirements

The CDCLVP111-SP shown in [Figure 5](#) is configured to be able to select 2 inputs, a 156.25-MHz LVPECL clock from the backplane, or a secondary 156.25-MHz LVCMOS 2.5-V oscillator. Either signal can be then fanned out to desired devices, as shown.

The configuration example is driving 4 LVPECL receivers in a line card application with the following properties:

- The PHY device has internal AC coupling and appropriate termination and biasing. The CDCLVP111-SP will need to be provided with 86- $\Omega$  emitter resistors near the driver for proper operation.
- The ASIC is capable of DC coupling with a 2.5-V LVPECL driver such as the CDCLVP111-SP. This ASIC features internal termination so no additional components are needed.
- The FPGA requires external AC coupling but has internal termination. Again, 86- $\Omega$  emitter resistors are placed near the CDCLVP111-SP and a 0.1-uF are placed to provide AC coupling. Similarly, the CPU is internally terminated and requires external AC coupling capacitors.

### 8.2.1.2 Detailed Design Procedure

Unused outputs can be left floating.

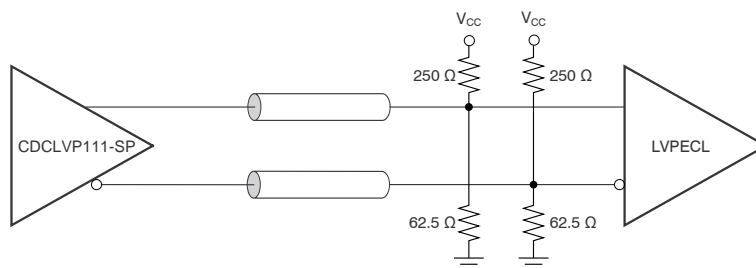
In this example, the PHY, ASIC, and FPGA/CPU require different schemes. Power-supply filtering and bypassing is critical for low-noise applications.

See [Figure 16](#) for recommended filtering techniques.

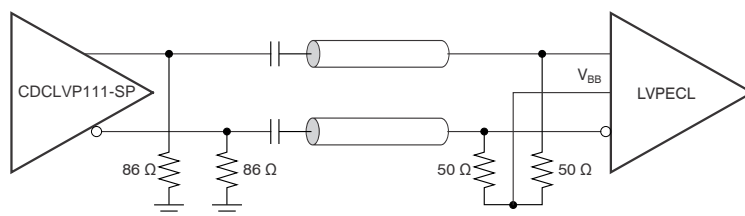
## Typical Application (continued)

### 8.2.1.2.1 LVPECL Output Termination

Refer to [Figure 6](#) for output termination schemes depending on the receiver application.



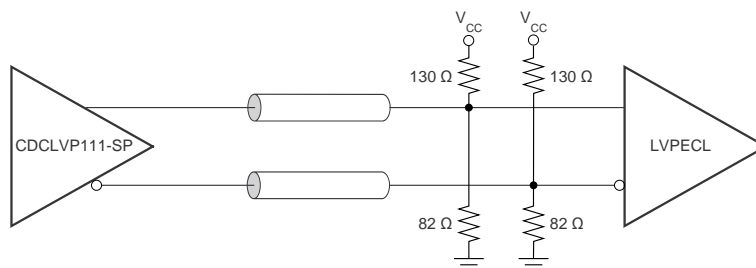
(a) Output DC Termination



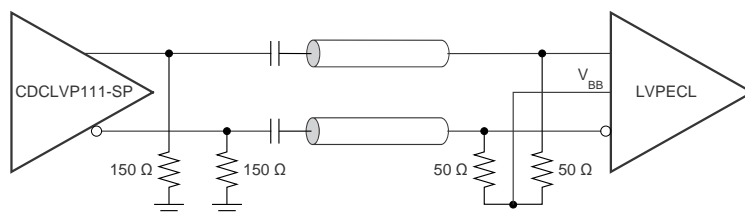
(b) Output AC Termination

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**Figure 6. LVPECL Output DC and AC Termination for  $V_{CC} = 2.5$  V**



(a) Output DC Termination



(b) Output AC Termination

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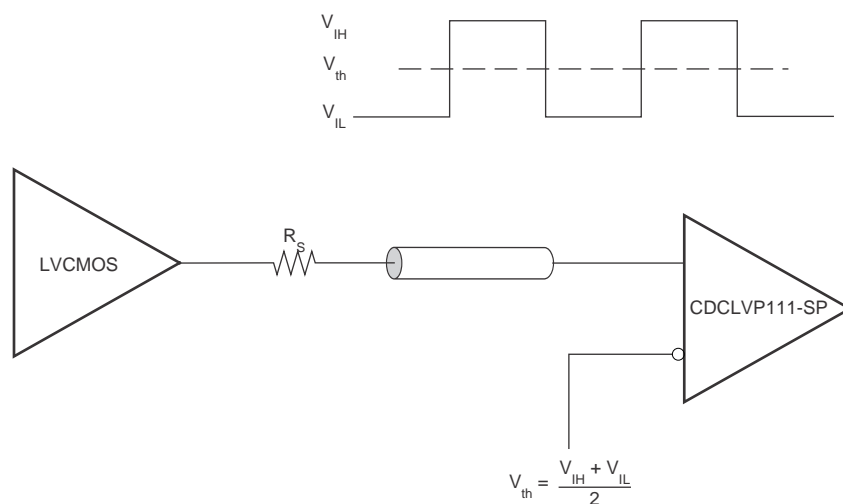
**Figure 7. LVPECL Output DC and AC Termination for  $V_{CC} = 3.3$  V**

## Typical Application (continued)

### 8.2.1.2.2 Input Termination

The CDCLVP111-SP inputs can be interfaced with LVPECL, LVDS, or LVCMOS drivers. [Figure 8](#) illustrates how to DC couple an LVCMOS input to the CDCLVP111-SP. The series resistance ( $R_S$ ) should be placed close to the LVCMOS driver; the value is calculated as the difference between the transmission line impedance and the driver output impedance.

Refer to [Figure 8](#) for proper input terminations, dependent on single ended or differential inputs.

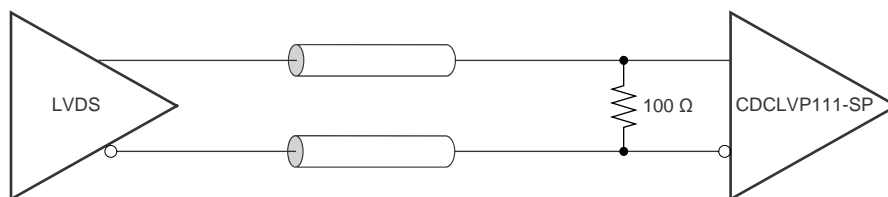


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**Figure 8. DC-Coupled LVCMOS Input to CDCLVP111-SP**

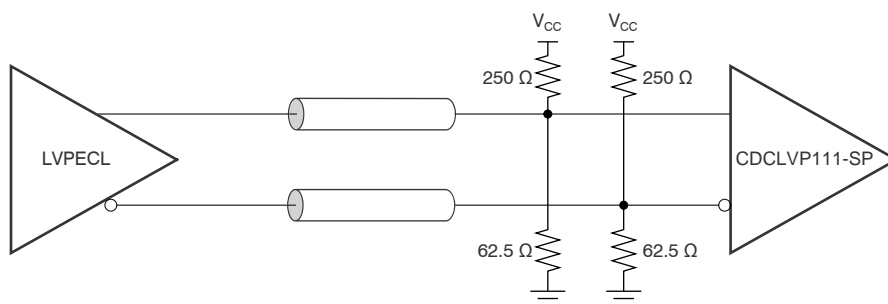
## Typical Application (continued)

Figure 9 shows how to DC couple LVDS inputs to the CDCLVP111-SP. Figure 10 and Figure 11 describe the method of DC coupling LVPECL inputs to the CDCLVP111-SP for  $V_{CC} = 2.5\text{ V}$  and  $V_{CC} = 3.3\text{ V}$ , respectively.



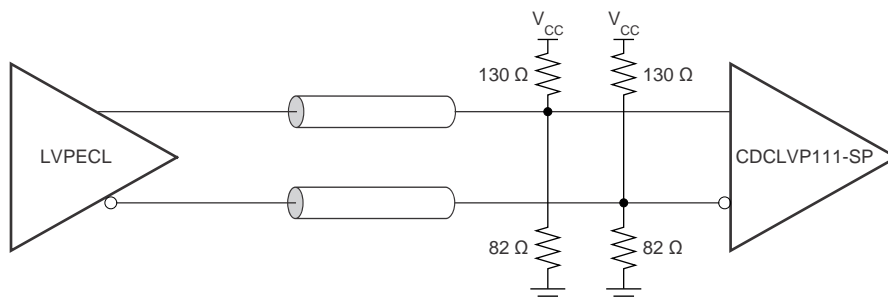
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**Figure 9. DC-Coupled LVDS Inputs to CDCLVP111-SP**



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**Figure 10. DC-Coupled LVPECL Inputs to CDCLVP111-SP ( $V_{CC} = 2.5\text{ V}$ )**

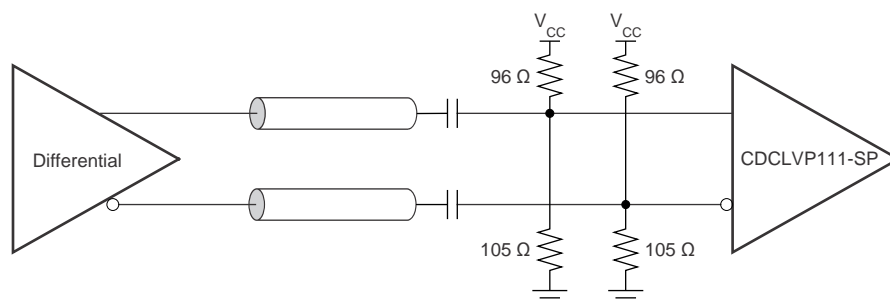


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**Figure 11. DC-Coupled LVPECL Inputs to CDCLVP111-SP ( $V_{CC} = 3.3\text{ V}$ )**

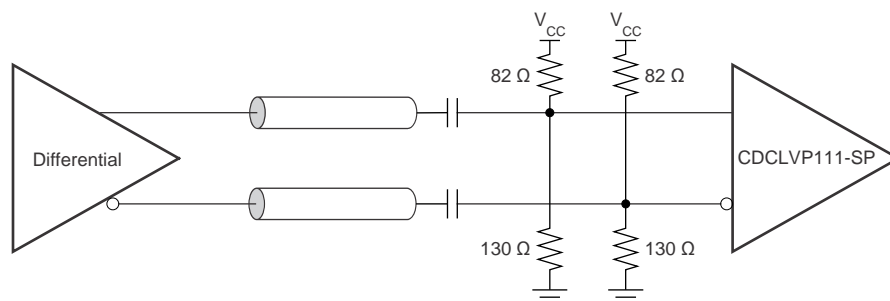
## Typical Application (continued)

Figure 12 and Figure 13 show the technique of AC coupling differential inputs to the CDCLVP111-SP for  $V_{CC} = 2.5\text{ V}$  and  $V_{CC} = 3.3\text{ V}$ , respectively. TI recommends to place all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, AC coupling is required.



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**Figure 12. AC-Coupled Differential Inputs to CDCLVP111-SP ( $V_{CC} = 2.5\text{ V}$ )**



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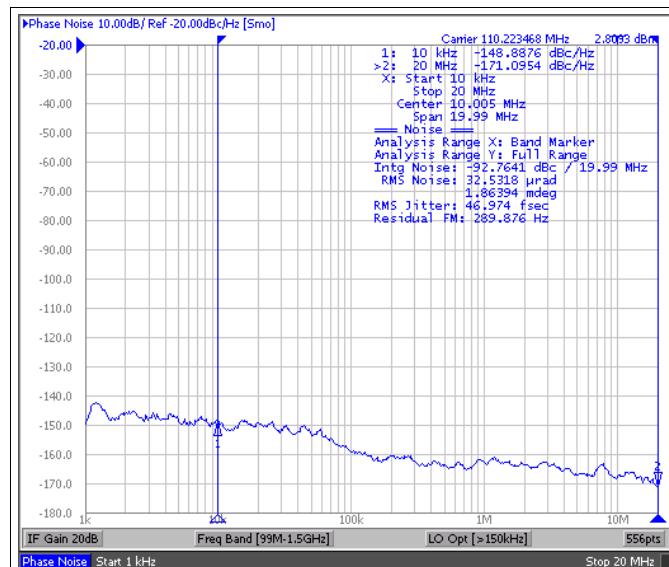
**Figure 13. AC-Coupled Differential Inputs to CDCLVP111-SP ( $V_{CC} = 3.3\text{ V}$ )**



## Typical Application (continued)

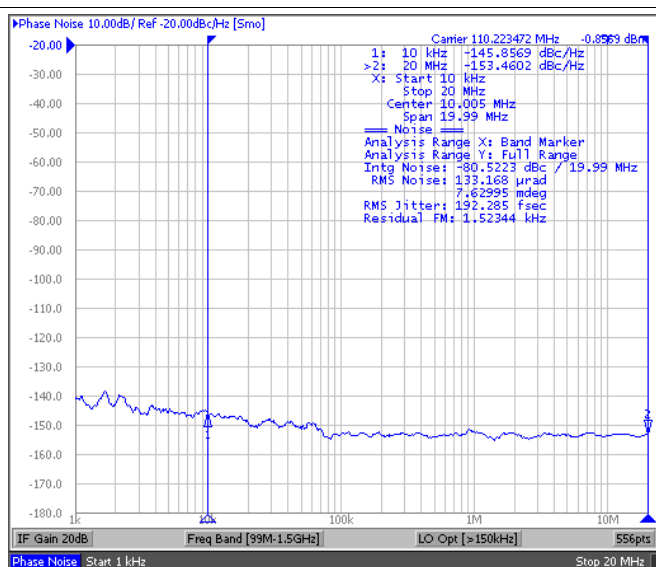
### 8.2.1.3 Application Curves

The CDCLVP111-SP low-additive noise can be shown in this line card application. The low-noise, 110.22-MHz signal with 47-fs RMS jitter drives the CDCLVP111-SP, resulting in 192-fs RMS when integrated from 10 kHz to 20 MHz. The resultant-additive jitter is a low 186-fs RMS for this configuration.



Reference signal is low noise signal generator

**Figure 14. CDCLVP111-SP Reference Phase Noise  
47-fs RMS  
(10 kHz to 20 MHz)**



**Figure 15. CDCLVP111-SP Output Phase Noise  
192-fs RMS  
(10 kHz to 20 MHz)**

## 9 Power Supply Recommendations

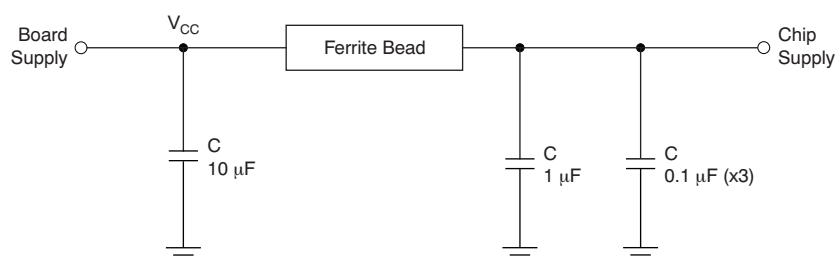
### 9.1 Power-Supply Filtering

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter and phase noise are very critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low-impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply terminals and laid out with short loops to minimize inductance. TI recommends to add as many high-frequency (for example, 0.1- $\mu$ F) bypass capacitors as there are supply terminals in the package.

TI recommends, but does not require, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 16 illustrates this recommended power-supply decoupling method.



**Figure 16. Power-Supply Decoupling**

## 10 Layout

### 10.1 Layout Guidelines

Differential outputs should be length matched and impedance controlled with  $50\ \Omega$  to  $(V_{CC} - 2)$  or  $100\text{-}\Omega$  differential with proper endpoint LVPECL termination. Clock inputs should be biased near device pins.

### 10.2 Layout Example

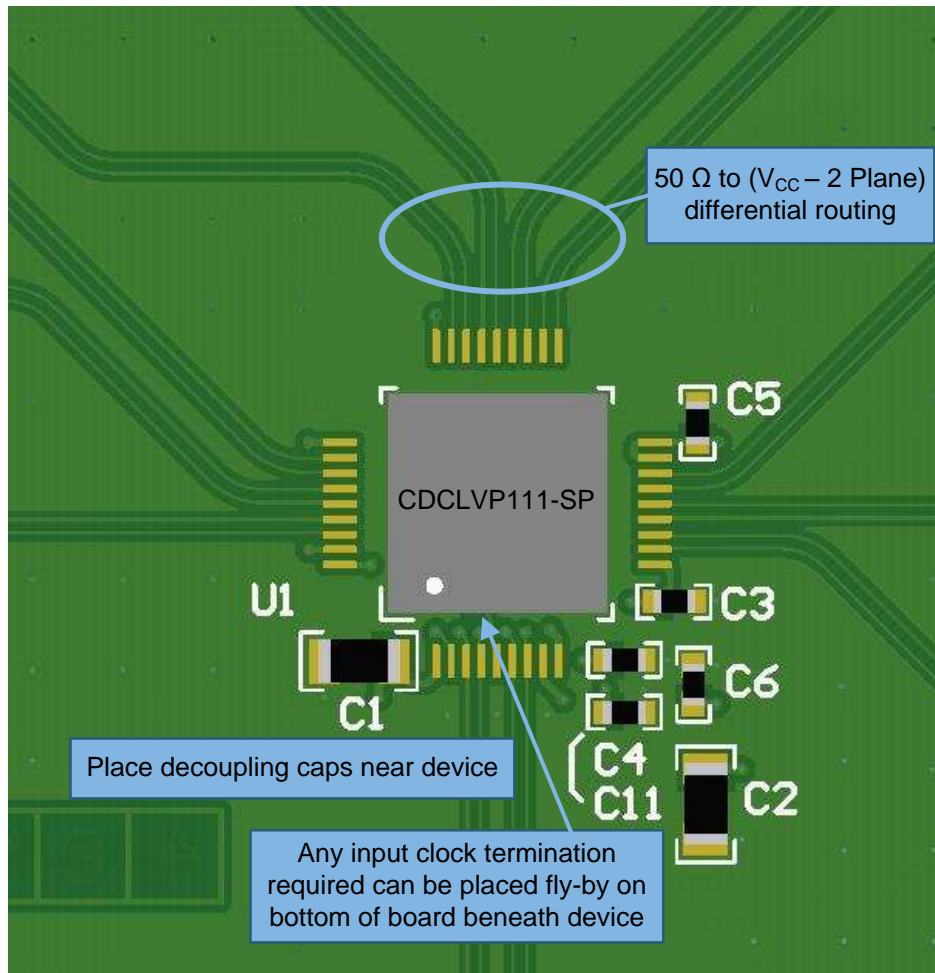


Figure 17. CDCLVP111-SP Layout Example

## 11 Device and Documentation Support

### 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1620701VXC	ACTIVE	CFP	HFG	36	1	RoHS-Exempt & Green	Call TI	N / A for Pkg Type	-55 to 125	5962-1620701VXC CDCLVP111HFG-V	<a href="#">Samples</a>
CDCLVP111HFG/EM	ACTIVE	CFP	HFG	36	1	RoHS-Exempt & Green	Call TI	N / A for Pkg Type	25 to 25	CDCLVP111HFG/EM EVAL ONLY	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

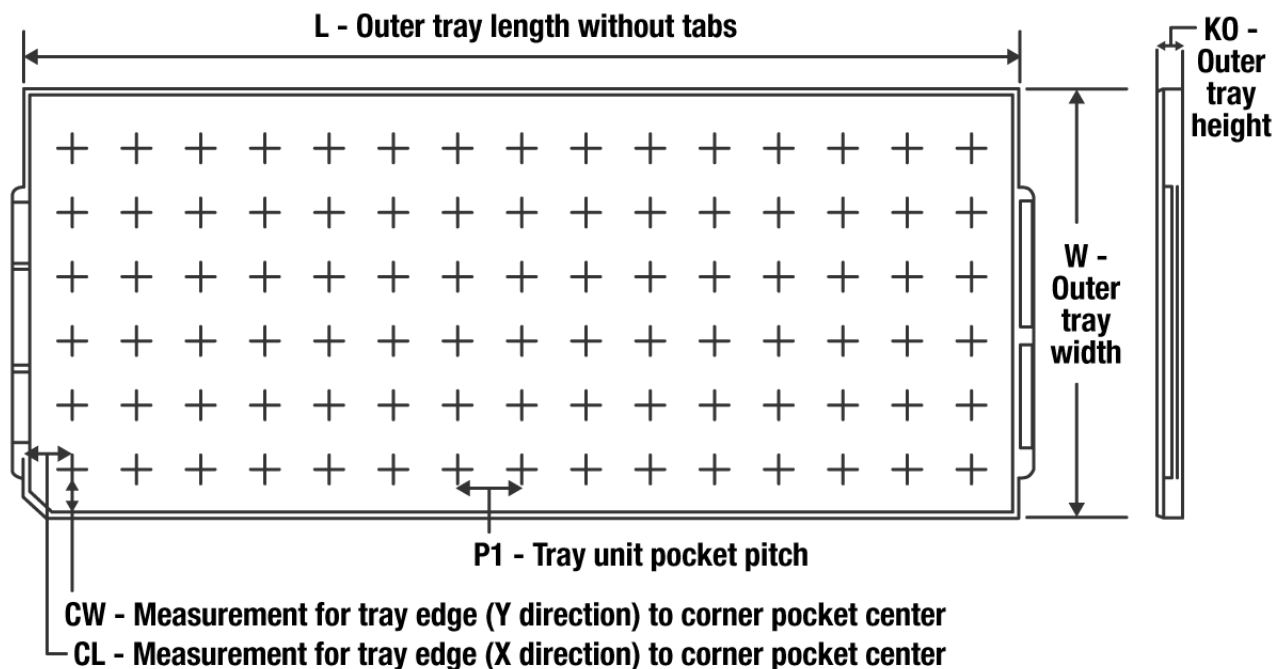
**OTHER QUALIFIED VERSIONS OF CDCLVP111-SP :**

- Catalog : [CDCLVP111](#)
- Enhanced Product : [CDCLVP111-EP](#)

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
5962-1620701VXC	HFG	CFP	36	1	2 x 5	75	315	135.9	13000	60.96	35.58	37.47
CDCLVP111HFG/EM	HFG	CFP	36	1	2 x 5	75	315	135.9	13000	60.96	35.58	37.47

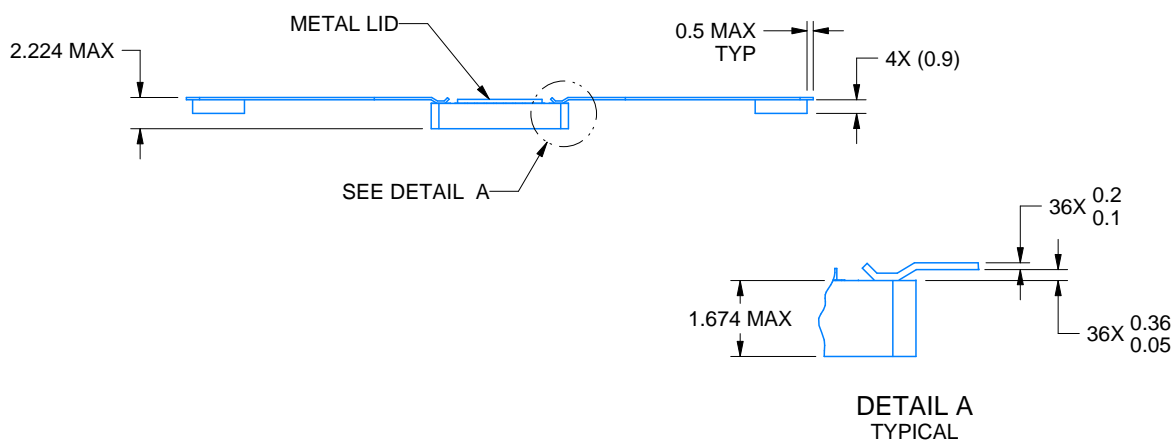


**CFP - 2.224 mm max height**

Technical drawing of a square metal lid with dimensions and labels. The drawing shows a square frame with four corner brackets. A central square area is labeled "METAL LID". Dimensions are provided in inches and millimeters.

Dimensions and labels:

- Top edge: 4X (3.429)
- Right edge: 2X 41.051, 40.231
- Bottom edge: 4X 5.08
- Left edge: 36X 0.248, 0.148
- Central square: 36, 28, 27, 19, 18, 10, 9
- Central square label: METAL LID
- Central square dimensions: 9.278, 8.878, 24.38, 23.88
- Bottom edge label: 32X 0.635



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The lid is connected to Pin 8.
5. The leads are gold plated and can be solder dipped.
6. The leads on the top of the package near the lid are showing.



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