DDR2 Memory Interface Clocks and Registers – Overview

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ABSTRACT

This application report gives an overview of the existing JEDEC DDR2 Register and PLL Buffer specifications and compliant TI devices.

Contents

List of Figures

List of Tables

1 DDR2 Buffer Components for RDIMM

On DDR2 Registered Dual Inline Memory Modules (RDIMM) PLLs and registers are used to buffer the Clock, Command, Control, and Address signals coming from the memory controller.

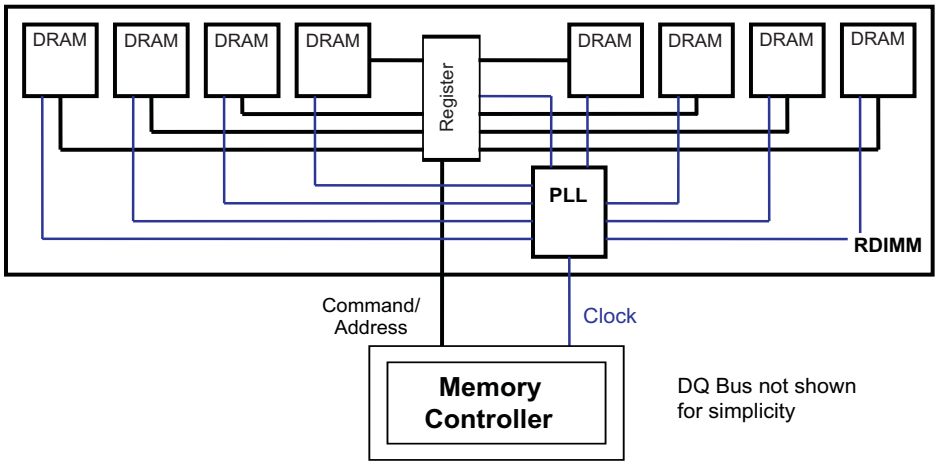

Figure 1. Usage of Register and PLL Buffer on RDIMM

1.1 JEDEC Compliance

The register and PLL devices for DDR2 RDIMM are standardized and specified by the JEDEC community. Over the lifetime of DDR2, several generations of those specifications have evolved. Later generations have tighter specifications for performance parameters (e.g., jitter, t_{PDM}) to support higher speed nodes.

All of TI's DDR2 interface devices are compliant to their corresponding JEDEC standards.

1.2 DDR2 PLL

A PLL is used to buffer the clock signals on DDR2 RDIMM. The input clock is copied to several output clock (e.g., a 1:10 buffer copies one input clock to 10 output clocks). DDR2 PLLs are used as zero delay clock buffers. For more information, review the application report *Application Examples for the CDCUx877X PLL Family* (SCAA087).

1.3 DDR2 Register

A synchronously latched register is used to buffer the Command, Address and Control signals on DDR2 RDIMM.

1.3.1 1:1 and 1:2 Modes

Depending on the type of register, it can be used as a 1:1 or a 1:2 buffer. The 1:1 buffer means that each input has one output copy. The 1:2 buffer means that each input has two output copies.

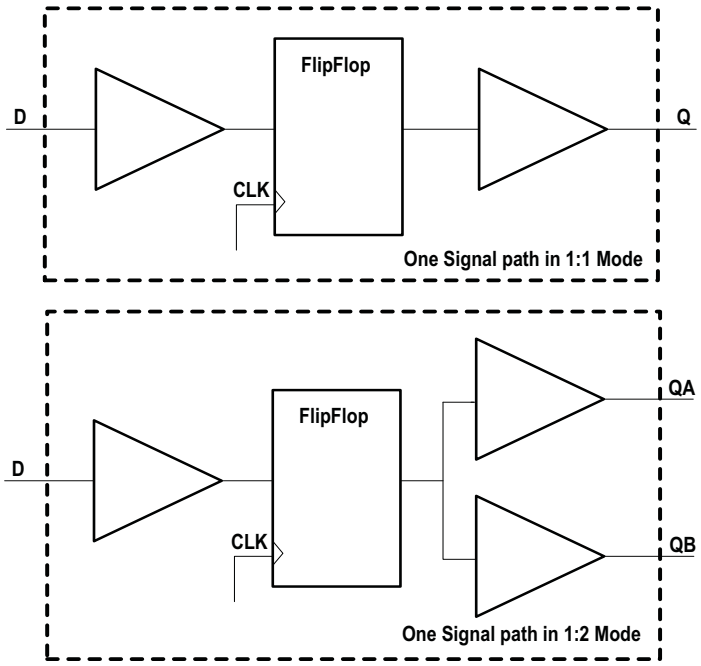

Figure 2. 1:1 and 1:2 Buffer Mode Example

1.3.2 Cascading of Registers

If the bit width of a register is insufficient (e.g., 28 signals need to be buffered, but the register only has 14 inputs), two devices have to be cascaded or a different type of register must be chosen.

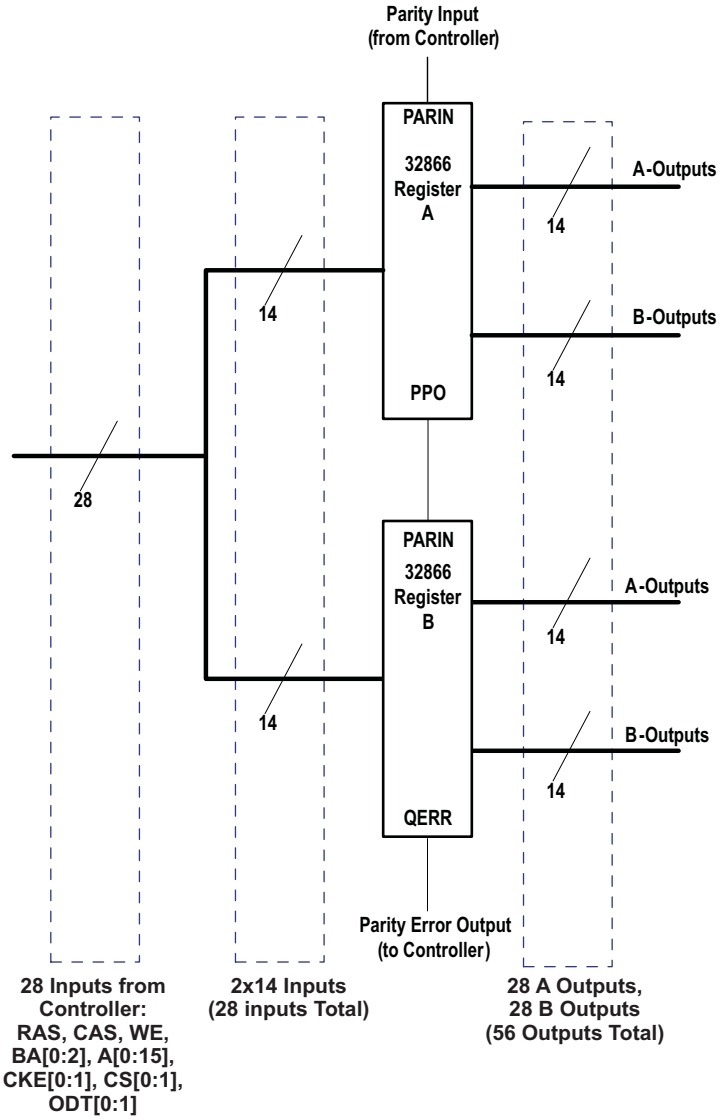

Figure 3. 28-Bit 1:2 Buffering Using Two Cascaded SSTUx32866 Registers

1.3.3 Mirror Mode

Some registers have the possibility to mirror their input ball-out. This can be used to optimize layout if two registers are used. It allows mounting the registers back to back, one on each side of the DIMM.

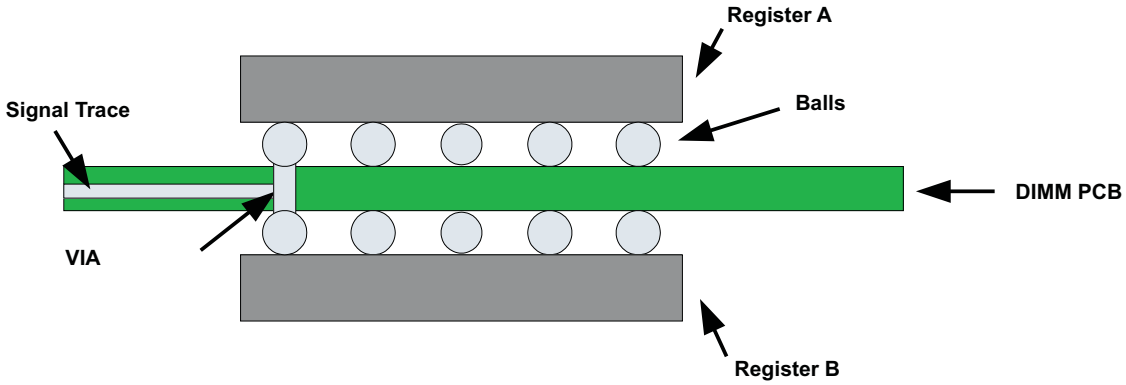

Figure 4. Back-to-Back Mounting of Two Registers With Mirror Ball-Out

1.3.4 Parity Check

Most of the register devices also offer a parity check feature. Those devices compare the parity checksum of all Command and Control signals to a parity signal. It has to be provided by the memory controller one cycle after the corresponding Command and Control signals are latched in. In case the parity does not match, the register output ERROUT is pulled low. Usually the system freezes in that case to prevent any corruption of data.

1.4 Package Options

DDR2 registers and PLLs are available in several package options. Each package has a individual 3-letter designator, which is part of the orderable part number.

Example for a complete part number: ***SN74SSTUB32866ZWLR***

SN74SSTUB32866:	Device Name
ZWL:	3-letter Package Designator
R:	Packing option (T=Tray, R=Reel)

Table 1 is listing all the available packages and a short description.

Table 1. TI DDR2 Interface Devices Package Overview

Designator(1)	Type	Balls/Pads	Devices	RoHs Compliant(2)	Green Compliant(3)	Comment
GKE	LFBGA	96	SSTU32864 SSTU32864C SSTU32864D SSTU32864E SSTU32866	No	No	
ZKE	LFBGA	96	SSTU32864 SSTU32864C SSTU32864D SSTU32864E SSTUB32864 SSTUB32864A SSTU32866 SSTU32866A SSTUB32866 SSTUB32866A	Yes	Yes	Same as GKE, but fully green compliant
ZWL	LFBGA	96	SSTUB32866 SSTEB32866	Yes	Yes	Improved signal Integrity
ZJB	TFBGA	160	SSTUB32865 SSTUB32865A	Yes	Yes	
ZRH	NFBGA	176	SSTUB32868 SSTUB32868A	Yes	Yes	
GQL	BGA	52	CDCU877 CDCU877A	No	No	
ZQL	BGA	52	CDCU877 CDCU877A CDCU877B CDCUA877 CDCU2A877	Yes	Yes	Same as GQL, but fully green compliant
RTB	QFN	40	CDCU877 CDCU877A	No	No	
RHA	QFN	40	CDCU877 CDCU877A	Yes	Yes	Same as RTB, but fully green compliant

(1) Click on Links to open package drawings
(2) Device does not contain restricted RoHs 6 substances (Cadmium, hexavalent Chromium, Lead, Mercury, PBBs, PBDEs).
(3) RoHs compliant and also free of Halogens (Bromine and Chlorine). For more information, see the Eco-Info page on the TI Web site.

2 Register Overview

The register is used to buffer the Command-, Control- and Address-signals on DDR2 RDIMM.

2.1 SSTUx32864

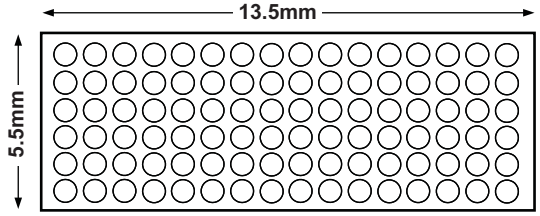

Figure 5. SSTUx32864 Package (96-Ball LFBGA)

2.1.1 General Information

- 25-bit 1:1 or 14-bit to 28-bit 1:2 configuration possible
- Able to cascade with a second SSTUx32864
- No parity check
- Configurable ball-out (mirror function)
- First DDR2 register specified by JEDEC (JESD82-7)

Table 2. Available SSTUx32864-Compliant Devices From TI

SN74SSTU32864 Package Options: GKE, ZKE	– First generation, supports DDR2-400 and DDR2-533 – Propagation delay t_{pdm} 1.4 ns–2.5 ns – Top marking: SU864
SN74SSTU32864C Package Options: GKE, ZKE	– First generation, supports DDR2-400 and DDR2-533 – Propagation delay t_{pdm} 1.4 ns–2.4 ns – Top marking: S864C
SN74SSTU32864D Package Options: GKE, ZKE	– First generation, supports DDR2-400 and DDR2-533 – Propagation delay t_{pdm} 1.4 ns–2.15 ns – Top marking: SU864D
SN74SSTU32864E Package Options: GKE, ZKE	– First generation, supports DDR2-400 and DDR2-533 – Propagation delay t_{pdm} 1.4 ns–2.15 ns – Improved signal integrity compared to previous versions – Top marking: S864E
SN74SSTUB32864 Package Options: ZKE	– Third generation, supports DDR2-400/533/667/800 – Propagation delay t_{pdm} 1.1 ns–1.5 ns – Improved signal integrity compared to previous versions – Fully backward-compatible – Supports industrial temperature range (-40°C–85°C) – Recommended solution for most new designs – Top marking: SB864
74SSTUB32864A Package Options: ZKE	– Third generation, supports DDR2-400/533/667/800 – Propagation delay t_{pdm} 1.1 ns–1.5 ns – Supports industrial temperature range (-40°C–85°C) – Basically same as SN74SSTUB32864, but with higher slew rate – Top marking: SB864A

2.2 SSTUx32866

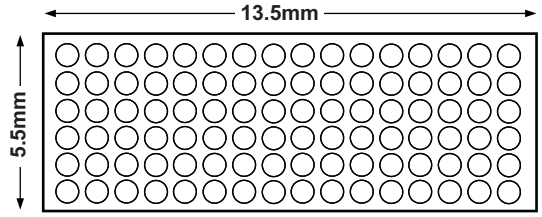

Figure 6. SSTUx32866 Package (96-Ball LFBGA)

2.2.1 General Information

- 25-bit 1:1 or 14-bit to 28-bit 1:2 configuration possible
- Able to cascade with a second SSTUx32866
- Same as SSTUx32864, but additionally with parity check of Command and Address signals
- Configurable ball-out (mirror function)
- JEDEC specifications:
  - SSTU32866 (JESD82-10)
  - SSTUA32866 (JESD82-16)
  - SSTUB32866 (JESD82-25)

Table 3. Available SSTUx32866-Compliant Devices From TI

SN74SSTU32866 Package Options: GKE, ZKE	– First generation, supports DDR2-400 and DDR2-533 – Propagation delay t_{pdm} 1.4 ns–2.5 ns – Top marking: SU866
SN74SSTU32866A Package Options: ZKE	– First generation, supports DDR2-400 and DDR2-533 – Propagation delay t_{pdm} 1.4 ns–2.15 ns – Top marking: SU866A
SN74SSTUB32866 Package Options: ZKE, ZWL	– Third generation, supports DDR2-400/533/667/800 – Propagation delay t_{pdm} 1.1 ns–1.5 ns – Improved signal integrity compared to previous versions – Fully backward-compatible – Parity input pulldown resistor of 150 kΩ allows usage on typical SSTUx32864 applications – Supports industrial temperature range (-40°C–85°C) – ZWL package option further improves signal integrity – Recommended solution for most new designs – Top marking: SB866
74SSTUB32866A Package Options: ZKE	– Third generation, supports DDR2-400/533/667/800 – Propagation delay t_{pdm} 1.1 ns–1.5 ns – Supports industrial temperature range (-40°C–85°C) – Basically same as SN74SSTUB32866 but with higher slew rate – Top marking: SB866A
SN74SSTEB32866 (1) Package Options: ZWL	– Same as SN74SSTUB32866, but supports VDD voltage range 1.425 V–1.9 V

(1) At present, engineering samples for this device are available. Release to market is planned for June 2009.

2.3 SSTUx32865

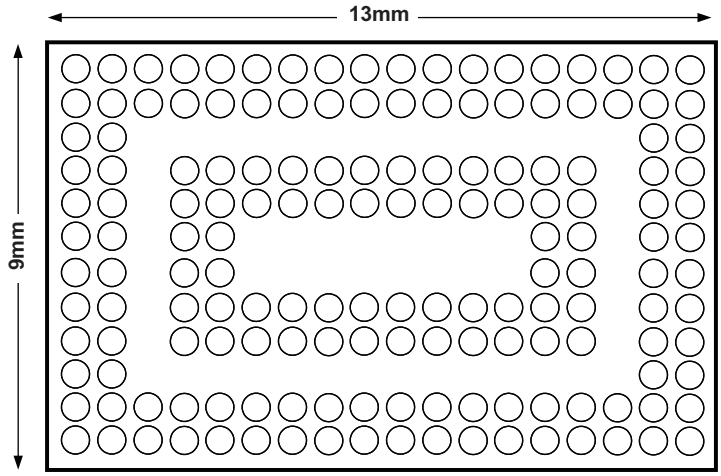

Figure 7. SSTUx32865 Package (160-Ball TFBGA)

2.3.1 General Information

- 28-bit to 56-bit 1:2 configuration
- With parity check of Command and Address signals
- Integrates the functionality of two SSTUx32866 into a single device
- No mirror function
- Fits on VLP DIMMs
- JEDEC Specifications:
  - SSTU32868 (JESD82-9)
  - SSTUA32S865/SSTUA32D865 (JESD82-19)
  - SSTUB32868 (JESD82-24)

Table 4. Available SSTUx32865-Compliant Devices From TI

74SSTUB32865 Package Options: ZJB	– Third generation, supports DDR2-400/533/667/800 – Propagation delay t_{pdm} 1.1 ns– 1.5 ns – Fully backward-compatible – Supports industrial temperature range (-40°C–85°C) – Top marking: SB865
74SSTUB32865A Package Options: ZJB	– Same as 74SSTUB32865 but with higher drive strength and slew rate – Top marking: SB865A

2.4 SSTUx32868

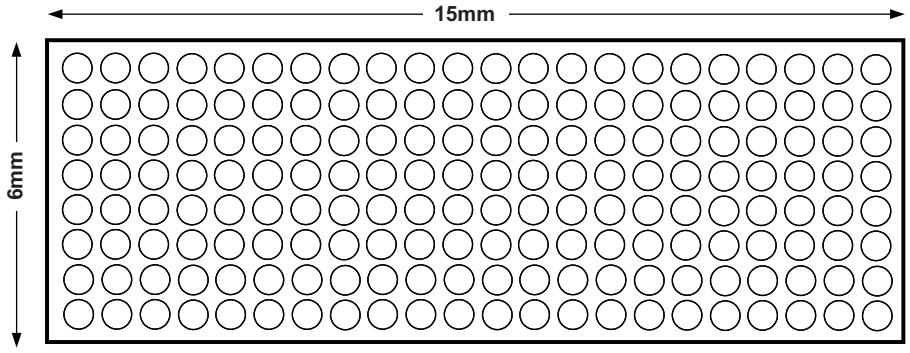

Figure 8. SSTUx32868 Package (176-Ball NFBGA)

2.4.1 General Information

- 28-bit to 56-bit 1:2 configuration
- With parity check of Command and Address signals
- Integrates the functionality of two SSTUx32866 into a single device
- Configurable ball-out (mirror function)
- JEDEC Specifications:
  - SSTU32868 (JESD82-14)
  - SSTUA32S868/SSTUA32D868 (JESD82-17)
  - SSTUB32868 (JESD82-26)

Table 5. Available SSTUx32868-Compliant Devices From TI

74SSTUB32868 Package Options: ZRH	– Third generation, supports DDR2-400/533/667/800 – Propagation delay t_{pdm} 1.1 ns–1.5 ns – Fully backward-compatible – Supports industrial temperature range (-40°C–85°C) – Top marking: SB868
74SSTUB32868A Package Options: ZRH	– Same as 74SSTUB32868 but with higher drive strength and slew rate – Top marking: SB868A

2.5 SSTUx32869

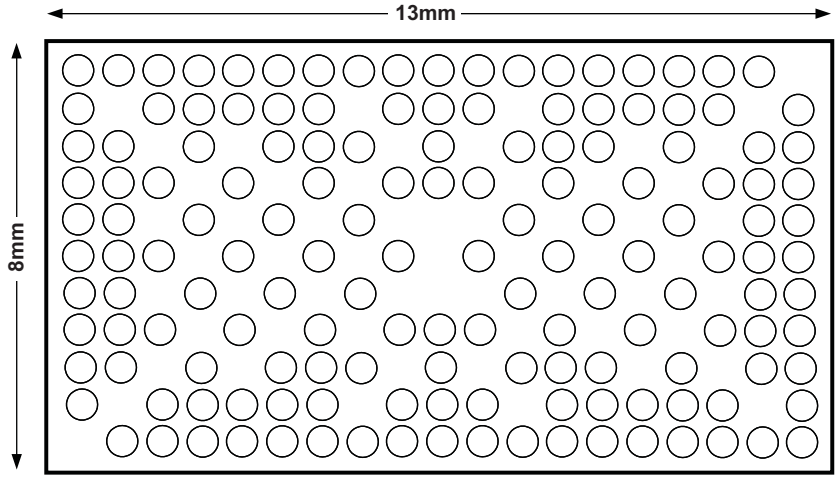

Figure 9. SSTUx32869 Package (150-Ball TFBGA)

2.5.1 General Information

- 14-bit to 28-bit 1:2 configuration (no 1:1 mode available)
- With parity check of Command and Address signals
- Same as SSTUx32866, but with 50% more dynamic drive strength
- No mirror function
- Fits on VLP DIMMs
- JEDEC Specifications:
  - SSTU32S869/SSTU32D869 (JESD82-12)
  - SSTUB32869 (JESD82-27)

3 PLL Overview

3.1 CUx877

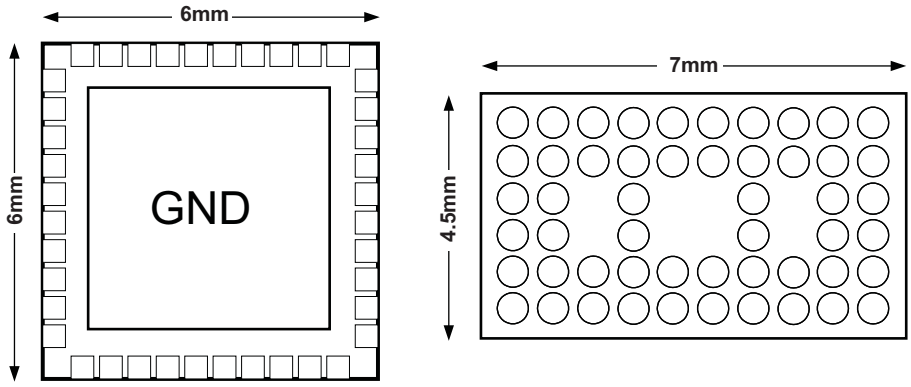

Figure 10. CUx877 Package (40-Pad QFN and 52-Ball BGA)

3.1.1 General Information

- 1:10 PLL clock buffer
- External feedback loop for synchronizing outputs to inputs (zero delay, See application report SCAA087)
- Two package options specified
- JEDEC specifications
  - CU877 (JESD82-8)
  - CUA877/CU2A877 (JESD82-18)

Table 6. Available CUx877-Compliant Devices From TI

CDCU877 Package Options: RHA, RTB, GQL, ZQL	– First generation, supports DDR2-400 and DDR2-533 – Supports industrial temperature range (-40°C–85°C) – Top marking: CDCU877
CDCU877A Package Options: RHA, RTB, GQL, ZQL	– Basically same as CDCU877 – Only difference: VOX is on average 30 mV lower compared to CDCU877 (for the same application) – Top marking: CDCU877A
CDCU877B Package Options: ZQL	– Supports DDR2-400/533/667 – Supports industrial temperature range (-40°C–85°C) – Top marking: CDCU877B
CDCUA877 Package Options: ZQL	– Supports DDR2-400/533/667/800 – Supports industrial temperature range (-40°C–85°C) – Top marking: CDCUA877
CDCU2A877 Package Options: ZQL	– Same as CDCUA877, but with higher output drive – Top marking: CDCUA877

4 Recommendations for New RDIMM Designs

Table 7. Buffer Recommendations for New RDIMMs

					Recommended PLL Buffer	Recommended Register Buffer		
RawCard	**Organization**	**Number of SD-RAMs**	**Form Factor**	**Parity**	**DDR2-400 DDR2-533 DDR2-667 DDR2-800**	**DDR2-400 DDR2-533**	**DDR2-667**	**DDR2-800**
A	1Rx8	9 (planar)	LP	No	CDCUA877	SSTUB32864 SSTUB32866(1)	SSTUB32864 SSTUB32866(1)	SSTUB32864 SSTUB32866(1)
B	2Rx8	18 (planar)	LP	No	CDCUA877	SSTUB32864 SSTUB32866(1)	SSTUB32864 SSTUB32866(1)	SSTUB32864 SSTUB32866(1)
C	1Rx4	18 (planar)	LP	No	CDCUA877	SSTUB32864 SSTUB32866(1)	SSTUB32864 SSTUB32866(1)	SSTUB32864 SSTUB32866(1)
D	2Rx4	36 (stacked)	LP	Yes	CDCUA877 CDCU2A877(2)	SSTUB32865 SSTUB32865A(2)	SSTUB32865 SSTUB32865A(2)	SSTUB32865 SSTUB32865A(2)
E	2Rx4	36 (stacked)	LP	Yes	CDCUA877 CDCU2A877(2)	SSTUB32866		
F	1Rx8	9 (planar)	LP	Yes	CDCUA877	SSTUB32866	SSTUB32866	SSTUB32866
G	2Rx8	18 (planar)	LP	Yes	CDCUA877	SSTUB32866	SSTUB32866	SSTUB32866
H	1Rx4	18 (planar)	LP	Yes	CDCUA877	SSTUB32866	SSTUB32866	SSTUB32866
J	2Rx4	36 (planar)	LP	Yes	CDCUA877 CDCU2A877(2)	SSTUB32866	SSTUB32866	
K	2Rx4	36 (stacked)	LP	Yes	CDCUA877 CDCU2A877(2)	SSTUB32868	SSTUB32868 SSTUB32868A	SSTUB32868 SSTUB32868A(2)
L	2Rx4	36 (planar)	LP	Yes	CDCUA877 CDCU2A877(2)	SSTUB32868	SSTUB32868 SSTUB32868A	SSTUB32868 SSTUB32868A(2)
M	4Rx4	72 (stacked)	LP	Yes	CDCU2A877	SSTUB32868A	SSTUB32868A	
N	4Rx8	36 (planar)	LP	Yes	CDCUA877 CDCU2A877(2)	SSTUB32866 SSTUB32866A(2)	SSTUB32866 SSTUB32866A(2)	
P	2Rx4	36 (stacked)	LP	Yes	CDCUA877 CDCU2A877(2)	SSTUB32868A	SSTUB32868A	
R	1Rx8	9 (planar)	VLP	Yes	CDCUA877	SSTUB32866	SSTUB32866	SSTUB32866
T	2Rx8	18 (planar)	VLP	Yes	CDCUA877	SSTUB32866	SSTUB32866	SSTUB32866
U	1Rx4	18 (planar)	VLP	Yes	CDCUA877	SSTUB32866	SSTUB32866	SSTUB32866
V	1Rx4	18 (planar)	VLP	Yes	CDCUA877	SSTUB32865	SSTUB32865	
Y	2Rx4	36 (stacked)	VLP	Yes	CDCUA877 CDCU2A877(2)	SSTUB32865 SSTUB32865A(2)		

(1) SSTUB32866 has on on-die pulldown resistor for parity input. Therefore it can be used on RawCards which are designed for SSTUB32864 as well.
(2) Proposed if DRAM input capacitance is on higher end of the specification for improved Signal Integrity

5 References

Register Data Sheets

1. SN74SSTU32864, 25-Bit Configurable Registered Buffer With SSTL_18 Inputs and Outputs (SCES434)
2. SN74SSTU32864C, 25-Bit Configurable Registered Buffer With SSTL_18 Inputs and Outputs (SCES542)
3. SN74SSTU32864D, 25-Bit Configurable Registered Buffer With SSTL_18 Inputs and Outputs (SCES623)
4. SN74SSTU32864E, 25-Bit Configurable Registered Buffer VWith SSTL_18 Inputs and Outputs (SCAS802)
5. SN74SSTUB32864, 25-Bit Configurable Registered Buffer (SCAS791)
6. 74SSTUB32864A, 25-Bit Configurable Registered Buffer (SCAS838)
7. SN74SSTU32866, 25-Bit Configurable Registered Buffer With Address-Parity Test (SCES564)
8. SN74SSTU32866A, 25-Bit Configurable Registered Buffer With Address-Parity Test (SCAS803)
9. SN74SSTUB32866 25-Bit Configurable Registered Buffer With Address-Parity Test (SCAS792)
10. 74SSTUB32866A, 25-Bit Configurable Registered Buffer With Address-Parity Test (SCAS837)
11. 74SSTUB32865, 28-Bit to 56-Bit Registered Buffer with Address-Parity Test (SLAS537)
12. 74SSTUB32865A, 28-Bit to 56-Bit Registered Buffer With Address-Parity Test (SLAS562)
13. 74SSTUB32868, 28-Bit to 56-Bit Registered Buffer With Address-Parity Test (SCAS835)
14. 74SSTUB32868A, 28-Bit to 56-Bit Registered Buffer With Address-Parity Test (SCAS846)

PLL Data Sheets

1. CDCU877/CDCU877A, 1.8-V Phase Lock Loop Clock Driver (SCAS688)
2. CDCU877B, 1.8-V Phase Lock Loop Clock Driver (SCAS801)
3. CDCUA877, 1.8-V Phase Lock Loop Clock Driver (SCAS769)
4. CDCU2A877, 1.8-V Phase Lock Loop Clock Driver (SCAS827)

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