Application Report
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Configuring and Optimizing On-Chip PLL of the DAC348x

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ABSTRACT

A phase-locked loop (PLL), is a chief component used in telecommunication applications. This application report discusses the use of the DAC348x family's on-chip PLL to generate a high-frequency digital-to-analog converter (DAC) sample clock from a lower-frequency reference clock. The PLL in the DAC348x acts as a frequency multiplier, easing the system and board level design associated with the higher frequency DAC sample clock. The system designers can accomodate the higher data speeds needed for modern communication applications while relaxing the cost and design requirements of the high speed clock generators or synthesizer. One tradeoff, however, is that the on-chip PLL may have jitter and spur performance limitations when compared to other high-performance clocking solutions. To aid designers with the DAC348x's on-chip PLL configuration and optimization, this report discusses ways to mitigate phase-noise performance degradation and phase-frequency detector (PFD or PD) spur occurrence, by adjusting PLL parameters such as divider ratios and PFD frequencies. This application note also shows ways to minimize the impact of phase noise and PFD spurs in some of the common communication signals.

Contents

1 Introduction

A PLL is a feedback control system that uses the phase difference between a reference and the output to synchronize and generate clocking signals. It has many important applications in digital communications. For example, a PLL can be used as a FM demodulator to extract the original content of a modulated signal. It is also used for carrier synchronization and recovery to remove frequency or phase offsets that might exist between the transmitter and receiver of a system. The PLL application discussed in this report is frequency multiplication, which is the functionality used within the Texas Instruments (TI) DAC348x family. This functionality of the on-chip PLL can ease design and lower the cost of clock distribution in a system, allowing the use of a lower frequency clock signal to generate the DAC sample clock needed for many systems. Additionally, some applications may require the DAC to oversample in order to extend the DAC Nyquist zone. Having this extended frequency range allows images to be pushed further apart and minimize the occurrence of the image fold-back. The PLL allows the DAC to run at a faster update rate at the output to provide flexible frequency planning and filtering requirement.

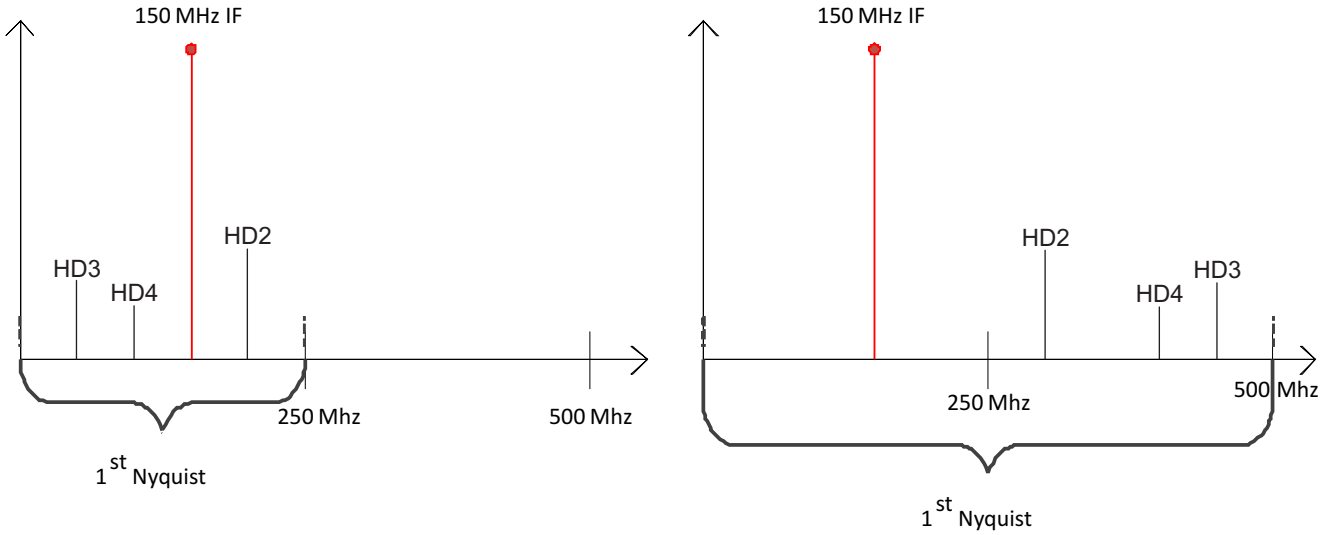

Figure 1. Spectrum Comparison: F_{DAC} = 500 MHz, Nyquist Zone = 250 MHz vs. F_{DAC} = 1 GHz, Nyquist Zone = 500 MHz

Figure 1 shows two spectrum plots of a 150MHz tone sampling at 500 MHz and 1 GHz, respectively. The plots also show up to four harmonic distortions (HD), and any harmonic distortion frequency exceeding the first Nyquist zone will fold back around $F_{DAC}/2$. The higher DAC sampling speed allows the Nyquist zone expansion, which decreases the amount of image and harmonic distortion fold-back showing on the DAC output spectrum. To simplify the design and implementation of the DAC348x PLL functionality, this application note will give an overview of the PLL architecture, the tradeoffs associated with using a PLL for clock generation, and the results of the PLL performance of the DAC3484 EVM.

2 PLL Architecture Overview

The ultimate goal of frequency multiplication is to take in a lower frequency and multiply it to output a higher frequency. F_{REF} is a low, fixed frequency that serves as the system clock provided to the DAC. The F_{REF} needs a multiplier to get to the desired frequency at F_{DAC}. To achieve the desired DAC sample rate, F_{DAC}, the PLL is used to implement the multiplying function. A PLL consists of four main parts; a phase-frequency detector (PFD), charge pump (CP), a loop filter, and a voltage-controlled oscillator (VCO). Along with these components are the dividers (N and M) and a prescaler (P), which are added for programmability and optimization of the frequency manipulation. The DAC348x PLL block diagram is shown in Figure 2.

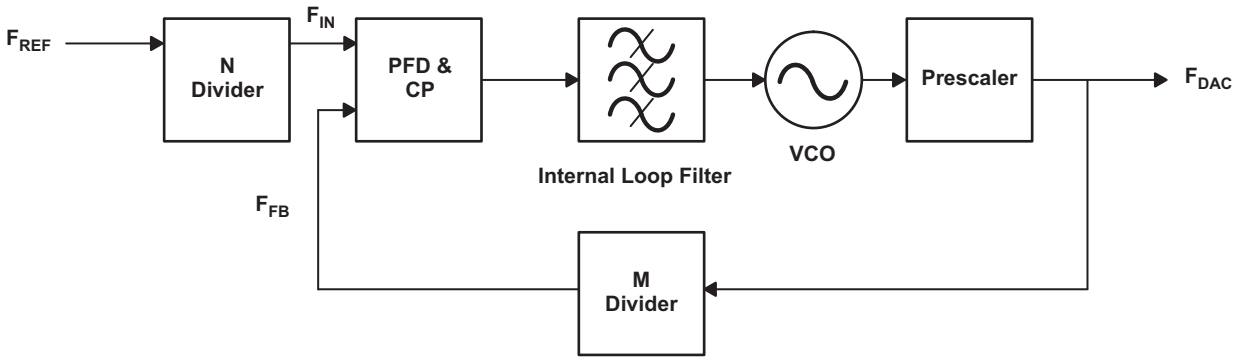

Figure 2. Full PLL in the DAC348x

The M and N dividers are programmable integers added to the loop. They give the user more flexibility in selecting PLL settings. Without the dividers and the closed loop, the VCO frequency would essentially be equal to F_{REF}, and no multiplication would take place. Adding the dividers allows for flexible output frequency control. In the feedforward path, the N divider takes in the reference frequency and converts it to the PFD frequency per the programmed divider value. In the feedback path, the M divider provides a divided down feedback signal based on the VCO frequency. The PFD takes in the feedforward N divider frequency and the feedback M divider frequency and converts the difference between them into an error signal that is sent to the CP. Next, the CP takes the error signal and converts it to a current that is fed to the low-pass filter, integrating the error current and generating a control voltage to bias the VCO.

In summary, an error between the two PFD input frequencies causes a change in the VCO frequency, affecting the feedback frequency, F_{FB}, to create a closed-loop system. The VCO converges to a stable point when F_{IN} and F_{FB} are aligned. The feedback path tracks the input signal going into the PFD so the frequency at the oscillator is adjusted to match the frequencies of the input reference and feedback signal. When the error in phase is zero, the PLL is then locked. Furthermore, the prescaler, P, is added to the loop to divide the higher VCO frequency to a lower DAC update frequency, allowing for an extended frequency range that the PLL can output.

If we treat the core components (PFD, CP, LPF and VCO) as a single black box of a control loop, we can evaluate the signal going into the PFD and coming out of the VCO to understand how these dividers combine to form the needed frequency multiplier for the desired output frequency. From control theory, the loop reaches steady-state only if the input and feedback signal are equal. In the PLL loop the input and feedback frequencies should match to make the phase error zero. Following the math equations in Equation 1, setting the frequency going into the PFD, F_{in}, equal to F_{FB} and solving for F_{DAC}, we find that the multiplier becomes a factor of M and N. This allows F_{DAC} to operate at fractional multiples of F_{REF} instead of integer multiples.

See *Fractional/Integer-N PLL Basics* (SWRA029) for a more detailed explanation on how PLLs work.

$$F_{in} = \frac{F_{REF}}{N} \quad \text{(feed forward path of PFD)}$$

$$F_{FB} = \frac{F_{DAC}}{M} \quad \text{(feed back path of PFD)}$$

$$\frac{F_{REF}}{N} = \frac{F_{DAC}}{M} \quad \text{(closed loop system and error in phase is zero)}$$

$$F_{DAC} = \frac{M}{N} \times F_{REF} \tag{1}$$

3 Configuring the On-Chip PLL of the DAC348x

To program the onboard PLL of the DAC348x, P should be chosen first based on the fixed VCO range of the part and the desired DAC sample rate. For the DAC348x family, the VCO is designed to operate between 3.3 GHz and 4.0 GHz. For the DAC34SH84, the VCO range is designed to operate between 2.7 GHz to 3.3 GHz. The product of P and the desired DAC clock are used to adjust the VCO center frequency within this range, as shown in Equation 2. Refer to the DAC3484 data sheet, Figure 56, to see the relationship between the VCO center frequency and DAC tuning bits. P must be an integer and is selected based on the range of the tuning bits. It is used in conjunction with the VCO frequency to generate any frequency needed for the DAC (see Table 5 in datasheet).

$$F_{VCO} = P \times F_{DAC} \tag{2}$$

Once the prescaler is chosen, M and N are selected based on the PFD frequency options for the system using Equation 3:

$$F_{PFD} = \frac{F_{DAC}}{M} = \frac{F_{REF}}{N} \leq 155 \text{ MHz} \tag{3}$$

The N divider is any integer between 1 and 16 and it determines the step size of the reference frequency allowing the PFD to operate at lower frequencies than the reference frequency. The M divider is between 4 and 254 and it controls the multiplier and creates the feedback frequency. Adding this divider allows the VCO frequency to be increased above the reference frequency. The M and N dividers determine the frequency going into the PFD and CP. For peak operation the M and N dividers should keep the PFD

frequency below 155 MHz. One thing to note for the DAC3484 is the overall divide ratio, or PxM, which must be kept within the range of 24 to 480. When the divide ratio is less than 120, the internal loop filter is sufficient to keep the loop locked and stable. When the ratio is above 120, an external loop filter or the double charge pump feature can be used to ensure stability. The double CP option is selected by setting config24, bit(7:6) to *b11*. The double CP feature has shown better phase-noise performance in band, as opposed to the external loop filter and is demonstrated in Section 4.

The recommended external loop filter (highlighted in Figure 57 in the datasheet) resistor is used to adjust the loop bandwidth of the PLL. However, because the LPF node does not have a switch separating one filter from the other, the resistor is limited to 5 kΩ. Increasing R will increase the bandwidth of the loop, but anything larger than 5 kΩ will have minimal impact to the loop bandwidth. For low offset frequencies, this will decrease the phase noise contribution from the VCO to the PLL output. For optimal phase margin of the loop, the ratio of C1/C2 remains 100. Decreasing the ratio will allow for smaller phase margin and possibly faster settling time of the PLL. This is less of a concern for applications operating at constant frequencies versus frequency hopping, however, changes to the recommended external loop filter are not guaranteed to display better phase-noise performance than the single or double CP options. Further characterization of the VCO will lead to more concise loop filter calculations, but is not currently available.

3.1 Summary

Here is a quick summary for configuring the on-chip PLL:

1. Select P based on desired output frequency and required VCO frequency range.
2. Select N for desired input frequency and select M for optimal PFD frequency.
3. Adjust M and N accordingly based on external reference frequency options for increased phase-noise performance. M and N optimization is discussed throughout the rest of this report.
4. The PFD frequency may be limited if the DAC348x is configured in Dual Synchronization Sources Mode. See the relevant DAC348x datasheet for details.

4 PLL Phase Noise Analysis (RMS JITTER)

All of the following plots were taken with nominal supply voltage, F_{DAC} = 1228.8 MHz and 983.04 MHz, 4X interpolation, NCO disabled, QMC disabled, coarse mixer at Fs/4, constant input, Integration bandwidth IF > 99 MHz: 10 Hz - 40 MHz, IF < 99 MHz: 10 Hz – 20 MHz (unless otherwise stated).

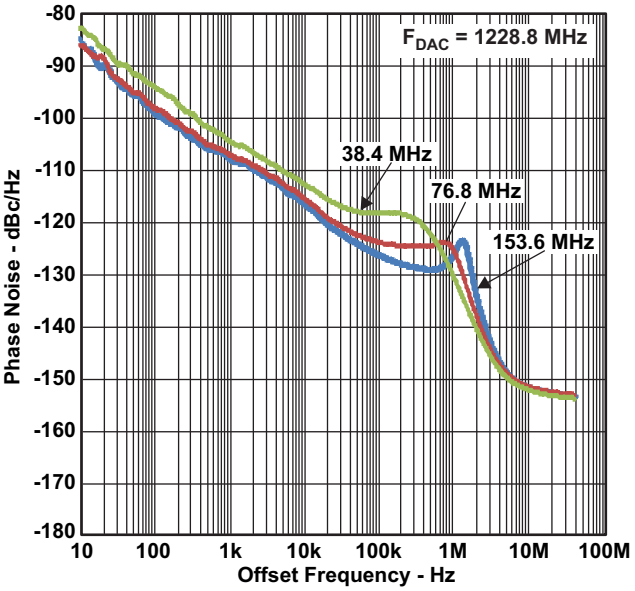

Figure 3. Phase Noise vs. PFD Freq (MHz), F_{DAC} = 1228.8 MHz

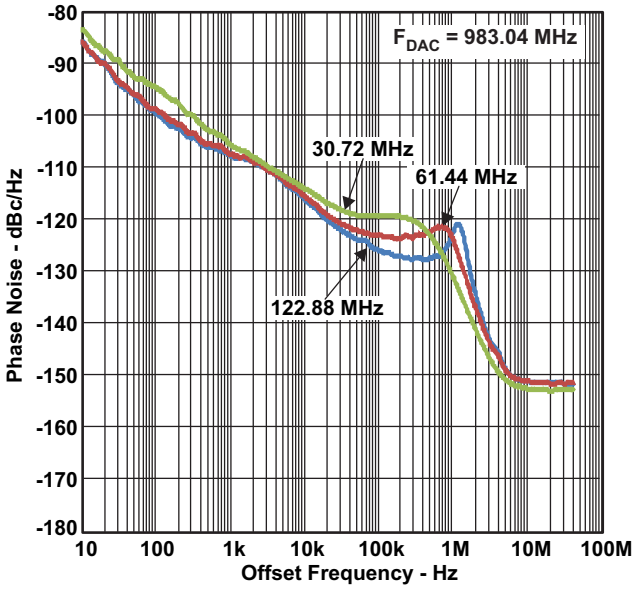

Figure 4. Phase Noise vs. PFD Freq (MHz), F_{DAC} = 983.04 MHz

Figure 3 and Figure 4 show the phase-noise curves for various PFD frequencies with the DAC output at 1228.8 MHz and 983.04 MHz respectively. In both cases, the phase-noise performance is better where the PFD frequency is higher and consequently the RMS jitter is less as seen in Table 1. At higher PFD frequencies, the control loop of the PLL is updating faster, allowing for quicker error correction from the feedback frequency. This results in better jitter performance.

Table 1. RMS Jitter Between High and Low PFD Frequencies (N divider = 1, external reference frequency and PFD frequency are equal)

DAC Frequency (MHz)	PFD Frequency (MHz)	RMS Jitter (fsec)
1228.8	153.6	556.2
1228.8	76.8	582.8
1228.8	38.4	677.8
983.04	122.88	652.4
983.04	61.44	661.4
983.04	30.72	724.3

When limited to low PFD frequencies, such as the case in synchronizing multiple DACs, the jitter performance is improved by using a higher reference frequency. Figure 5 and Figure 6 show the phase noise results for low PFD frequencies with varying external reference and N dividers. While the phase noise curves are very close together and follow the same shape, with a higher external reference and increased N divider, the RMS jitter is improved by almost 100 fsecs for these test cases, as seen in Table 2.

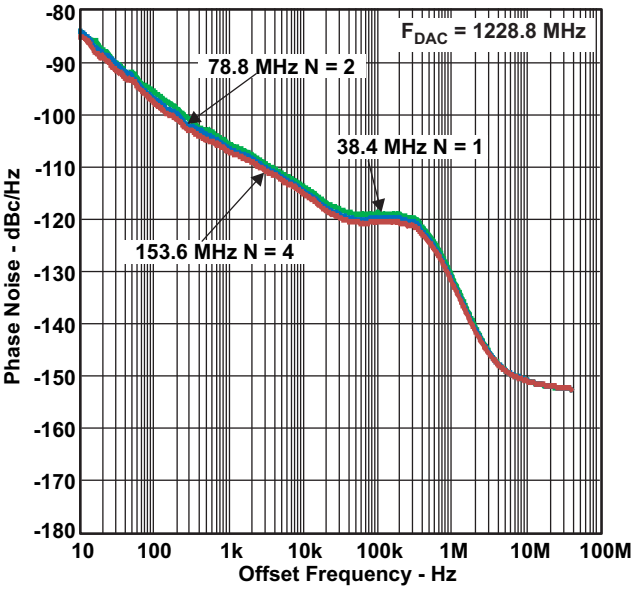

Figure 5. Phase Noise vs. External Ref (MHz), F_{DAC} = 1228.8 MHz, PFD = 38.4 MHz

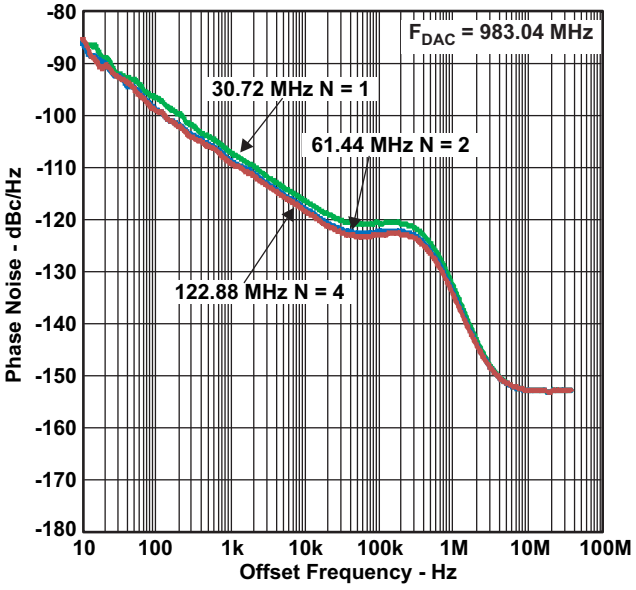

Figure 6. Phase Noise vs. External Ref (MHz), F_{DAC} = 983.04 MHz, PFD = 30.72 MHz.

Table 2. RMS Jitter with Increased N Divider and Higher External Reference Clock

DAC Frequency (MHz)	PFD Frequency (MHz)	External Reference Frequency (MHz)	N	RMS Jitter (fsec)
1228.8	38.4	38.4	1	677.8
1228.8	38.4	76.8	2	610.3
1228.8	38.4	153.6	4	580.1
1228.8	76.8	76.8	1	582.8
1228.8	76.8	153.6	2	526.5
983.04	30.72	30.72	1	724.3
983.04	30.72	61.44	2	613.3
983.04	30.72	122.88	4	579.8
983.04	61.44	61.44	1	661.4
983.04	61.44	122.88	2	528.9

For applications with low PFD frequencies, the double CP feature has been added to the DAC348x family. As mentioned, when the divide ratio (PxM) is greater than 120, the single CP feature cannot guarantee loop stability. However, the external loop filter can be used to stabilize the loop and it shows a significant decrease in phase noise. As an alternative, the double CP option allows for better phase-noise performance and loop stability as shown in Figure 7. Currently, changes to the external loop filter are limited as discussed in the configuration section. Upon completion of the VCO characterization, loop filter calculations are possible. Typically the double CP will show better phase noise than the single charge pump with external filter. The single CP option without external filter should be used for best phase-noise performance when PxM is less than 120.

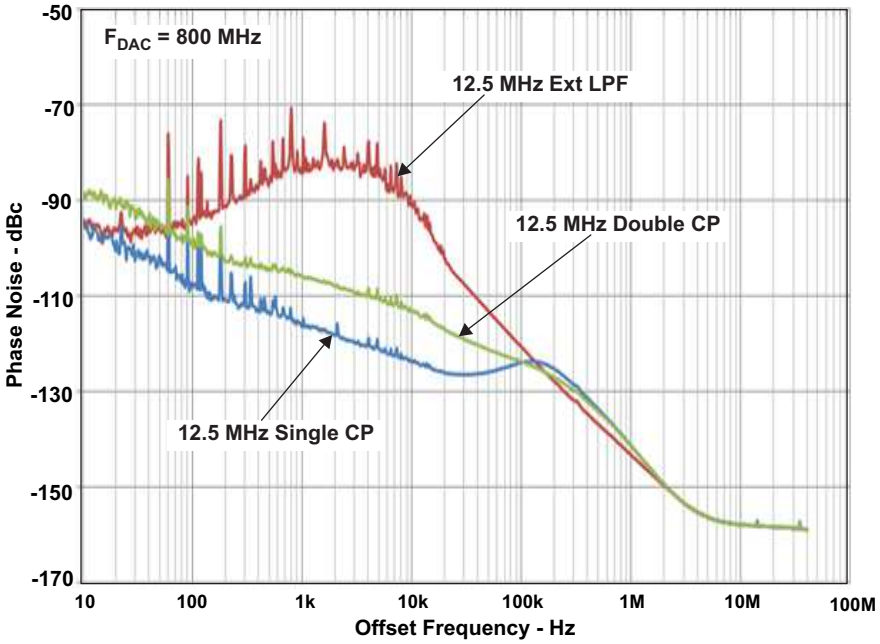

Figure 7. Phase Noise for Single CP, Double CP, and External-Loop Filter PFD frequency = 12.5 MHz, F_{DAC} = 800 MHz, NCO enabled = 100 MHz IF, Integration bandwidth = 10 Hz-40 MHz

Summary: Higher PFD frequencies result in better jitter and phase-noise performance because the control loop of the PLL is updating much faster, allowing for more error correction from the feedback frequency. If the application requires lower PFD frequency, the use of a higher external reference frequency and large N divider can help improve phase noise. Additionally, the double charge pump feature can help maintain stability and phase noise for the low PFD configuration.

5 PFD Spurs and Performance

All plots were taken with nominal supply voltage, F_{DAC} = 1228.8 MHz, 4X interpolation, NCO enabled at Fs/4, QMC disabled (unless otherwise stated).

Figure 8 and Figure 9 show the spectrums for a high PFD frequency of 153.6 MHz and a low PFD frequency of 38.4 MHz respectively, with the N divider equal to one in both cases. For PLL configurations with high PFD frequency, the number of spurs seen in band is less than the case with lower PFD frequency. However, the amplitudes of the spurs in the high frequency PFD configuration are higher than the amplitudes of the spurs in the low frequency PFD configuration. To relate this result to the real world application, Section 6 shows the investigation of the performance with modulated signals (LTE and WCDMA) and the impact of PFD spur amplitude on overall performance.

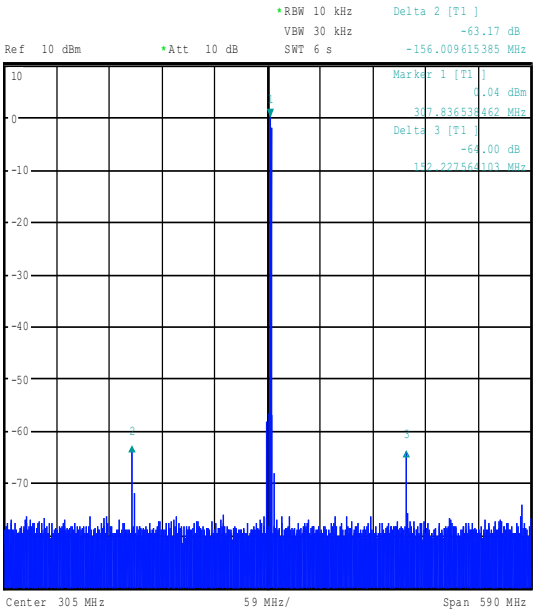

Figure 8. PFD Spurs for PFD Frequency = 153.6 MHz, Worst Spur Amplitude Measured at –64 dB

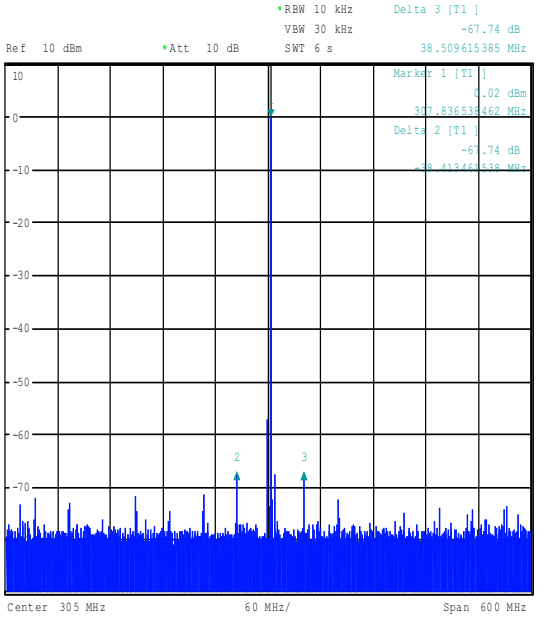

Figure 9. PFD Spurs for PFD Frequency = 38.4 MHz, Worst Spur Amplitude Measured at –67.74 dB

Particularly concerning applications that are limited to low PFD frequencies, using a higher external clock not only results in lower RMS jitter but it also reduces the amplitude of the prominent PFD spurs in the spectrum as seen in Figure 10 and Figure 11. In Figure 11, the external reference frequency is twice the PFD frequency and the N divider is increase to 2. Notice the prominent PFD spurs are no longer 38 MHz from the carrier, with the worst spur having an amplitude of -70.1 dB. Where the external reference frequency and PFD frequency equal at 38.4 MHz, the prominent PFD spurs are seen at that PFD frequency and the highest amplitude at 67.7 dB. Note the plots only observe PFD spurs. Other distortions such as HD2 and HD3 behave similarly between PLL on vs PLL off since the harmonic distortions are caused by analog artifacts alone.

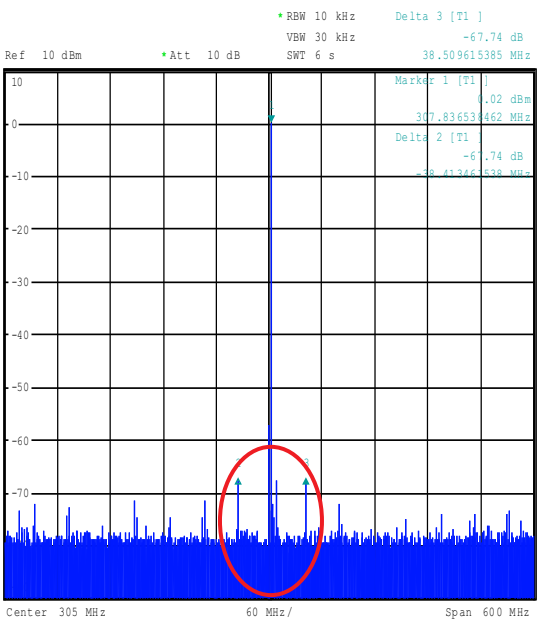

Figure 10. PFD Spurs for PFD Frequency = 38.4 MHz, External Reference = 38.4 MHz, N = 1, Worst Spur Amplitude Measured at –67.7 dB

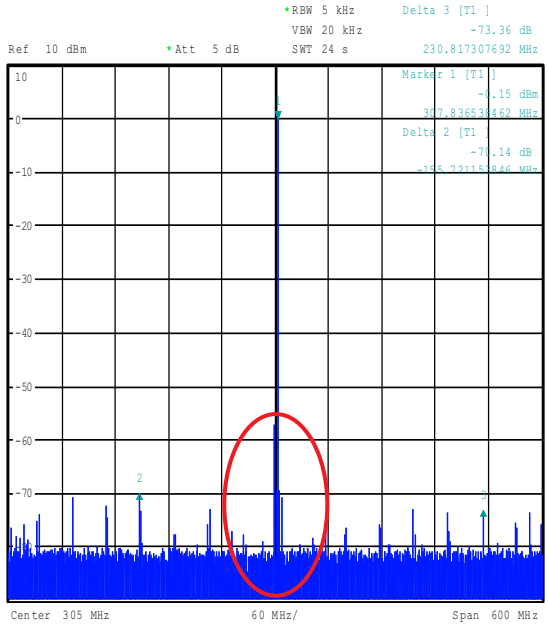

Figure 11. PFD Spurs for PFD Frequency = 38.4 MHz, External Reference = 76.8 MHz, N = 2, Worst Spur Amplitude Measured at –70.1 dB

Summary: PFD spurs resulting from higher PFD frequencies are spaced further out and may be located outside the bandwidth of interest. Both the PFD frequency and external reference frequency contribute to spur performance. The higher external reference frequency can increase both spur performance as well as phase noise.

6 Modulated Signal Results and Analysis

Now that the PFD spur and phase noise behaviors have been examined, another important factor is the impact of on-chip PLL to communication signals for radio applications. Examining both LTE and WCDMA standards and a carrier of Fs/4, Table 3 highlights the error vector magnitude (EVM) measurements of the specified signal with the PLL disabled compared to the PLL enabled with the various PFD settings that have been discussed above. EVM measures the error between the measured symbol location versus the ideal location on a constellation plot, which is affected by many factors. Phase noise and jitter can create a distribution cloud around the ideal constellation point. The more jitter and phase noise present, the larger the cloud becomes, leading to larger EVM measurements.

Table 3. EVM Measurements for Multiple PLL Settings and PLL Disabled at IF = Fs/4

PFD Freq (MHz)	LTE 10 MHz 3.1 (%)	LTE 5 MHz 3.1 (%)
1228.8 (PLL OFF)	0.31	0.640
983.04 (PLL OFF)	0.30	0.674
153.6	0.29	0.718
76.8 76.8, Ext = 153.6	0.31 0.29	0.615 0.614
38.4 38.4, Ext = 76.8 38.4, Ext = 153.6	0.29 0.28 0.29	0.605 0.654 0.673
122.88	0.30	0.674
61.44 61.44, Ext = 122.88	0.30 0.31	0.612 0.658
30.72 30.72, Ext = 61.44 30.72, Ext = 122.88	0.29 0.30 0.29	0.572 0.618 0.622

As shown in Table 3, minimal degradation in the EVM is seen between the PLL disabled versus the PLL enabled cases, demonstrating that if the phase noise is below the inherent signal performance the EVM is not significantly increased. If the phase noise falls below the carrier inherent signal performance, it will not largely affect the EVM measurement.

Equally important is the adjacent-channel power ratio (ACPR) performance of these signals. ACPR is the ratio of total power of the in-band modulated signal and the adjacent band's power. It is a merit of the likelihood for that channel to cause interference in other adjacent channels. In Figure 12, the LTE signals are shown for PLL disabled with DAC output frequency of 1228.8 MHz. Figure 13 and Figure 14 examine the ACPR for PFD frequencies of 153.6 MHz and 38.4 MHz, respectively.

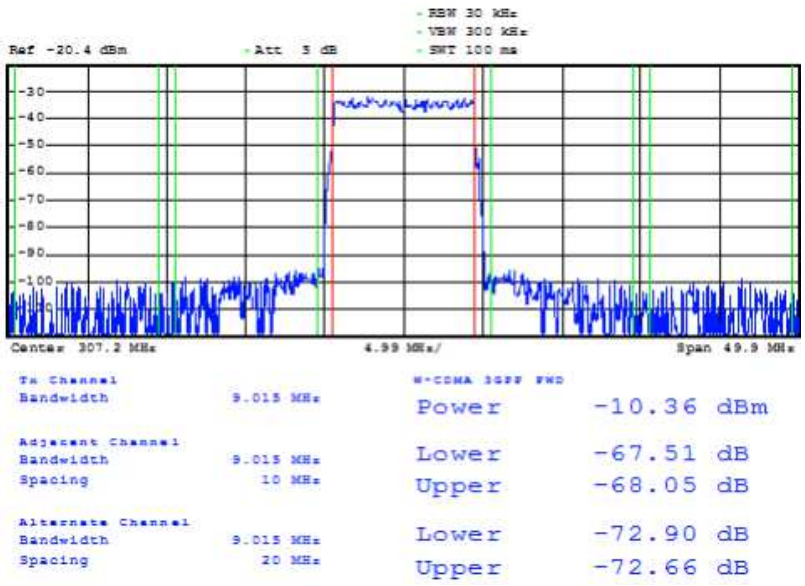

Figure 12. LTE 10 MHz 3.1; PLL Disabled, F_{DAC} = 1228.8 MHz

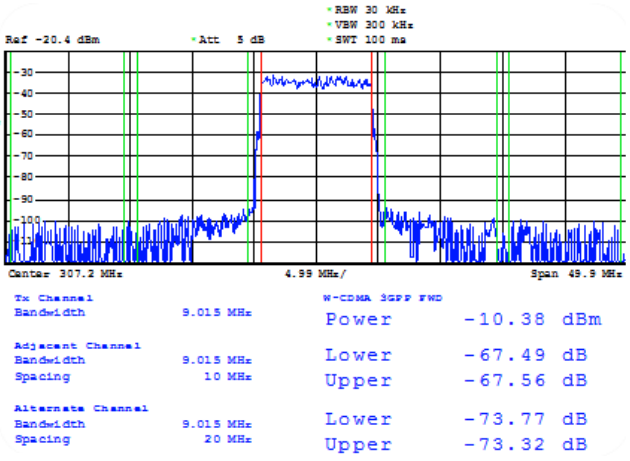

Figure 13. LTE 10 MHz 3.1; PLL Enabled, F_{DAC} = 1228.8 MHz, N = 1, PFD Frequency = 153.6 MHz

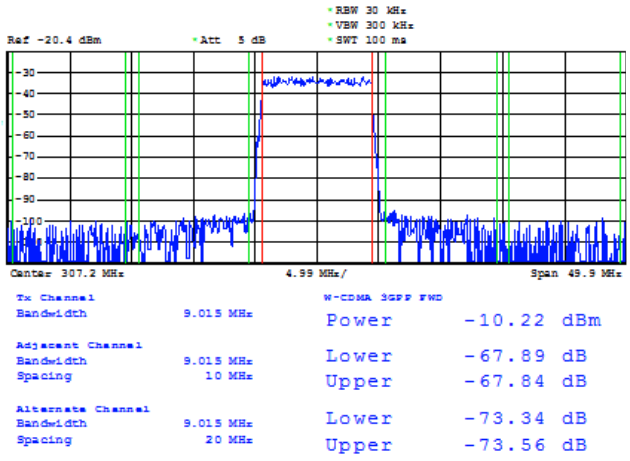

Figure 14. LTE 10 MHz 3.1; PLL enabled, F_{DAC} = 1228.8 MHz, N = 1, PFD frequency = 38.4 MHz

The spurious performance discussed in Section 5 can affect the spectral performance of the modulated signal. However, if the PFD spurs are low in amplitude and far away enough, the spurs can be filtered out in order to meet the emission mask requirement. Although there are more spurs for PLL enabled mode, the alternate and adjacent cahnnel leakage performance remain similar between PLL enabled mode and PLL disabled mode.

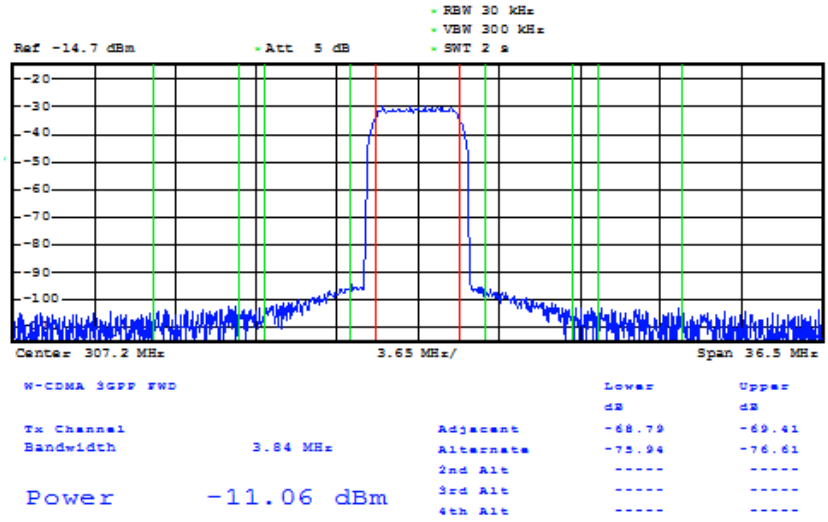

Figure 15. WCDMA; PLL disabled, F_{DAC} = 1228.8 MHz

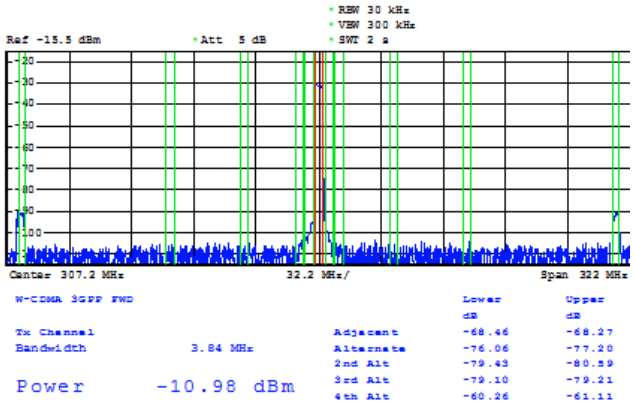

Figure 16. WCDMA; PLL enabled, F_{DAC} = 1228.8 MHz, IF = Fs/4, N = 1, PFD frequency = 153.6 MHz

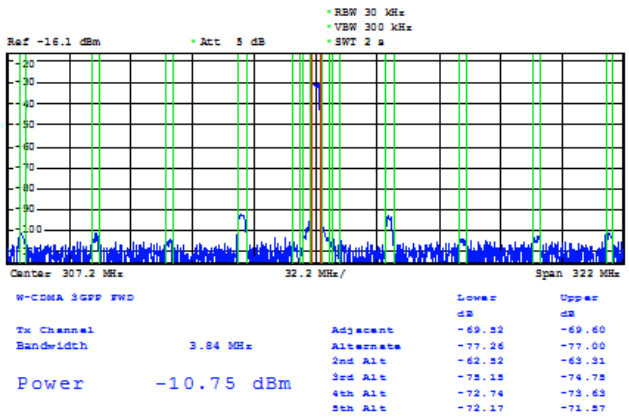

Figure 17. WCDMA 10 MHz; PLL enabled, F_{DAC} = 1228.8 MHz, IF = Fs/4, N = 1, PFD frequency = 38.4 MHz

Figure 16 and Figure 17 show the modulated WCDMA signal with a high PFD frequency, 153.6 MHz, and a low PFD frequency, 38.4 MHz, respectively. As previously mentioned, the high PFD frequency system has less spurs and the images are pushed further out from the carrier to relax filter requirements.

Summary: If the phase noise is below the noise floor in band of the carrier, the inherent signal performance is not hindered because the noise falls below the carrier bandwidth SNR. This results in comparable EVM measurements with the PLL enabled or disabled. Spectral performance is minimally affected with higher PFD setting because the amplitude of the PFD spurs remain low and far away enough to meet the emission mask requirement when properly filtered.

Table 4. Summary of ACPR measurements for LTE and WCDMA signals (Figures 13–18)

Signal type	PFD (MHz)	Tx Channel Power (dBm)	Adjacent Channel Power Lower (dB)	Adjacent Channel Power Upper (dB)	Alternate Channel Power Lower (dB)	Alternate Channel Power Upper (dB)
LTE 10 MHz TM3.1	Disabled	-10.36	-67.51	-68.05	-72.90	-72.66
LTE 10 MHz TM3.1	153.6	-10.38	-67.49	-67.56	-73.77	-73.32
LTE 10 MHz TM3.1	38.4	-10.22	-67.89	-67.84	-73.34	-73.56
WCDMA TM1	Disabled	-11.06	-68.79	-69.41	-75.94	-76.61
WCDMA TM1	122.88	-10.98	-68.46	-68.27	-76.06	-77.20
WCDMA TM1	30.74	-10.75	-69.52	-69.60	-77.26	-77.00

7 Conclusions/Recommendations

Using the on-chip PLL for the DAC348x family provides an oversampling feature with some tradeoffs to jitter performance. However, measurement results have indicated that the on-chip PLL performance may still be able to meet the requirements of most communication systems if the PFD frequency and F_{DAC} are planned accordingly. Mitigating solutions presented in this paper can effectively improve phase-noise performance. The optimal recommendation is to utilize a high PFD frequency while in single CP mode. This configuration results in the best phase-noise performance when the PLL is enabled, and less PFD spurs are observed. For systems that are limited to low PFD frequencies, such as in the case of synchronizing multiple DACs, the DAC must be supplied with a higher external reference and increased N-divider. Doing so will optimize performance and will also push the most prominent PFD spurs further away from the IF tone. Additionally, for the case of using lower PFD frequencies, the double CP mode has been added to provide an additional option to improve phase-noise performance as opposed to using the external loop filter.

Below is a summary of the recommendations presented in this report:

1. Use higher PFD frequencies in single CP mode for best phase-noise performance.
2. For low PFD frequencies, choose higher external reference and an increased N divider, when possible.
3. For low PFD frequencies, double CP mode offers better performance than using the external loop filter.

It is shown that the PLL does not degrade performance of communication signals such as LTE and WCDMA. While spurious performance may affect the spectral emission, the PFD spur can be adjusted by the M and N dividers to farther locations to relax the filtering requirement. EVM measurement can be attributed to phase-noise performance but if the phase noise is below the inherent signal performance the EVM is not significantly increased. Measurement results have indicated that enabling the PLL does not significantly diminish ACPR performance and the EVM measurements of the LTE and WCDMA signals. This application note shows that using the on-chip PLL is a viable option and the tradeoffs in performance can be alleviated with the suggestions discussed.

8 References

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