Ready to make the jump to JESD204B?

Thomas Neu
Systems Engineer,
High-Speed Data Converters
Texas Instruments

What you need to know when transitioning to JESD204B

There is a lot of buzz about a new interface standard called JESD204B that addresses the digital interconnect between high-speed data converters and the digital processor. It uses a high-speed serial interface to transfer the digital data as opposed to the traditional, lower speed CMOS or LVDS interfaces. While this new interface promises many benefits, such as reduced overall design complexity, board space and cost savings, the system designer needs to carefully consider various design aspects when making the switch to the JESD204B interface.

This paper examines the system implications around the JESD204B interface (**Figure 1**). Besides the sampling rate and AC performance specifications, there are several new parameters that influence the selection of the analog-to-digital (ADCs) or digital-to-analog converters (DACs).

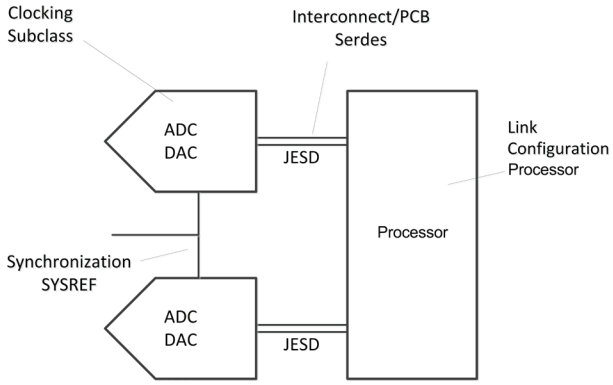


Figure 1. *System considerations concerning the JESD204B interface.*

Some of the most important parameters include support for different JESD204B subclasses (important in multi-channel applications) and harmonic clocking using an internal clock divider. For latency-sensitive industrial and military applications, the total data link latency may be the primary decision factor.

Other new key specifications include the maximum supported serial interface speed, which drives the digital processing solution and determines the processor (DSP or FPGA) class and cost, as well as the supported JESD204B link configurations.

The JESD204B standard provides great freedom for the link configuration, but it's up to the system designer to ensure compatibility between the transmitting and receiving device.

Clocking the converter

In the JESD204B-based system, the data converter clock takes on two additional responsibilities (**Figure 2**). Since the sampling clock is a low-jitter clock, it is also used to generate the high-speed clock for the ADC's serializer and DAC's deserializer.

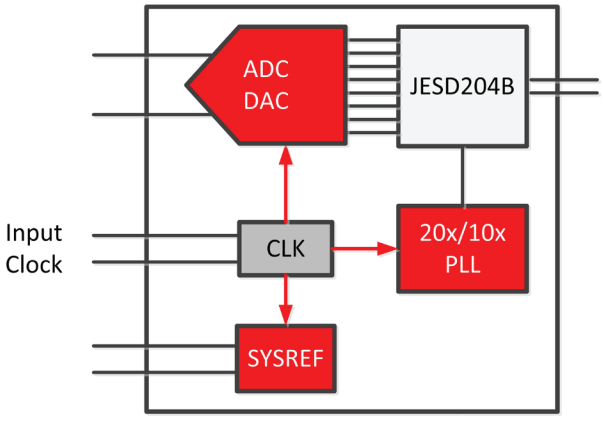


Figure 2. *Sampling clock gets additional responsibilities in JESD204B-based data converters.*

JESD204B employs 8b/10b encoding, which encodes 8-bit data into a 10-bit word (or 16-bit data into two 10-bit words) with 20 percent extra overhead. This encoding ensures that even if a static 0 or 1 pattern is sent, there are sufficient transitions present in the transmitted data so that the phase-locked loop (PLL) of the de-serializer can still recover the embedded clock.

With 8b/10b encoding, for example, an ADC with 16-bit resolution transmits 20 bits for each captured sample. The output data is then transmitted at 20 times the sampling rate using a single differential pair or alternatively a slower data rate using more lanes, such as 10 times the sampling rate using two lanes.

Modern data converters, like the ADC16DX370 – the industry's first dual-channel, 16-bit, 370-MSPS ADC – offer more flexibility and support different JESD204B link configurations. The system engineer can choose to save board area and minimize the number of gigabit transceivers in a processor, thus, he can operate the ADC16DX370 using a single lane per ADC at 7.4 Gbps. Or, he can choose to configure it to using two lanes per ADC at 3.7 Gbps and potentially use a lower-cost processor.

Secondly, the input clock is used to capture the synchronization input signal, which resets the internal reference clock or local multi-frame clock (LMFC). Multi-channel synchronization, as required in a MIMO configuration, can be established by phase-aligning the device clocks of multiple data converters and latching in this synchronization signal simultaneously (**Figure 3**).

Accurate management of clock timing and synchronization play an important role and will be examined in more detail later. Most commonly, a single device, such as the LMK04828 JESD204B clock jitter cleaner, is used to distribute both the data converter sampling clock and the synchronization signal to minimize skew between devices.

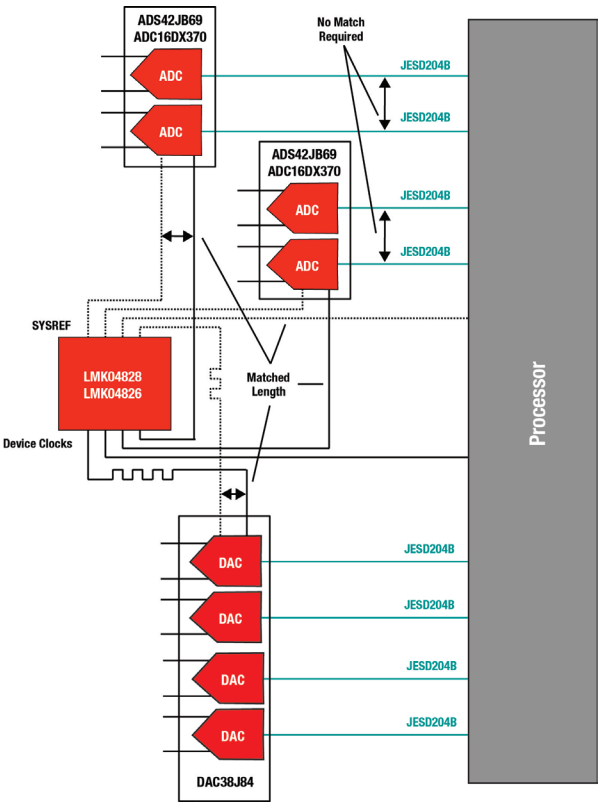


Figure 3. *Clocking a JESD204B-based system.*

Furthermore, the JESD204B standard also introduced the harmonic clocking feature, which eliminates the need to provide the exact sampling clock frequency to each device in the system. By distributing only a single, higher order multiple (2, 4, 8 times and so on) of the base sampling rate, the system clock tree can be simplified. Then each individual data converter can generate its required clock frequency using an internal clock divider.

Subclass 0, 1 or 2?

The JESD204B standard contains three different subclasses (0, 1 and 2), which primarily impact multi-chip synchronization. They also support the deterministic latency feature. A data converter may support one, two or all three subclasses (such as the ADS42JB69 a dual, 16-bit, 250-MSPS ADC). Depending on the application, the support of a specific subclass can be an important factor in data converter selection.

Subclass 0 supports the added features of JESD204 revision B, like higher line rates up to 12.5 Gbps, while still maintaining backward compatibility with JESD204A. Subclass 0 may be sufficient for many applications, but only subclass 1 and 2 support the deterministic latency feature. Deterministic latency establishes a fixed latency digital link between the JESD204B transmitter and receiver.

The data transmission start is tied to the internal reference clock, called the local multi-frame clock (LMFC). By aligning the LMFC clock across multiple devices using the synchronization signal, multi-chip synchronization can be greatly simplified. In subclass 1, the deterministic latency feature is implemented using an external SYSREF signal as the synchronization signal, while subclass 2 uses the SYNCb signal (**Table 1**).

Among system designers, subclass 1 is often preferred because a single clocking device can be used to distribute the sampling clock and the SYSREF signal. This allows for very accurate phase alignment and minimum skew across devices.

Subclass	0	1	2
Deterministic Latency Support	No	Yes	Yes
External Signal	—	SYSREF	SYNCb

Table 1. *Subclass comparison of the JESD204B standard.*

What is deterministic latency?

One of the more desirable features introduced by JESD204B is the deterministic latency of the link between a logic device and a data converter. It promises to greatly simplify multi-chip synchronization, including spanning across the transmit-and-receive boundary. A data converter contains various blocks that may operate in different clock domains, as well as have a propagation delay that is sensitive to process, temperature and supply voltage variation. Therefore, the latency across multiple transmitter and receiver links may vary.

In JESD204B, a common device clock can be distributed to all data converters, which is then used to generate the internal clocks inside each device. If an internal clock divider is used to generate the desired sampling rate, additional phase ambiguity is incurred. Depending on start-up condition, a divide-by-two block, for example, generates the half-rate clock with either 0° or 180° phase, which causes additional uncertainty.

As illustrated earlier, there are two subclasses defined in the JESD204B standard that govern how to achieve deterministic latency across different links between transmit and receive devices. Subclass 1 uses an external SYSREF, and subclass 2 uses the SYNCb signal as the synchronization signal.

As defined in the JESD204B standard, deterministic latency ensures a known, repeatable latency between the JESD204B transmitter and receiver, which does not vary between power or link re-synchronization cycles.

The synchronization signal (SYSREF or SYNCb) is used to reset all internal blocks (such as an input clock divider) to a known state. It aligns the phase of the internal reference clock or local multi-frame clock (LMFC) to the edge of the device clock where the synchronization signal is sampled. However, this assumes that all external synchronization signals, as well as device clocks to various devices, are matched in length amongst each other.

The system engineer needs to ensure the external synchronization signal meets the setup and hold time of the device clock. However, data converters like the ADS42JB69 provide a programmable delay buffer at the SYSREF input, for example. This is very helpful for exact timing alignment, especially with higher frequency device clocks.

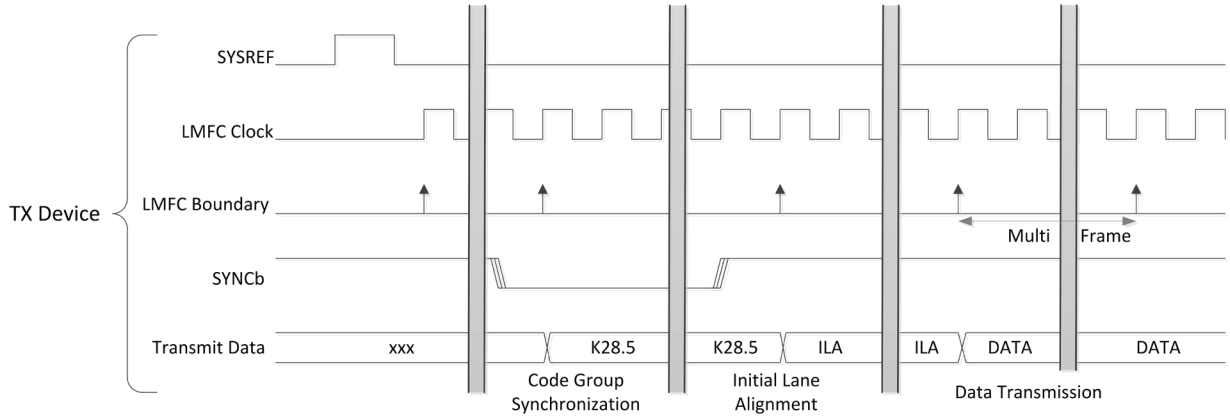


Figure 4. *ILA sequence of the JESD204B transmitting device.*

Achieving deterministic latency

The deterministic latency procedure is decribed in the example below using subclass 1 and illustrated in **Figure 4**. Subclass 2 is very similar, except it uses the SYNCb signal instead of the SYSREF signal to align the LMFCs.

1. The SYSREF signal is distributed and aligns the LMFCs across all devices. SYSREF can be a one-shot, gapped periodic or a periodic signal. In case of periodic or gapped periodic configuration, the period of the SYSREF signal must be an integer multiple of the LMFC in order to avoid a SYSREF pulse in the middle of a multi-frame. Since a periodic SYSREF signal acts like a sub-harmonic clock of the data converter sampling clock, it may have a spurious effect on the data converter performance. Thus, it often gets turned off during normal operation after synchronization has been achieved.
2. After the link is established, the receiving device requests code group synchronization (CGS) by driving the SYNCb signal low.
3. Once the receiver successfully decodes the K28.5 characters, it drives the SYNCb signal high, which starts the initial lane alignment (ILA) sequence simultaneously on all JESD204B links at the next LMFC boundary.
4. The elastic FIFO in the receiving device buffers the incoming data from all lanes in order to account for the skew across the various physical links. The size of elastic buffer must be large enough to store all the data arriving between the earliest possible instant of data arrival on the receiver (RX) buffer input to the next release opportunity.

   The release opportunity occurs after a fixed number of frame cycles, called receiver buffer delay (RBD), following an LMFC boundary. The value of RBD must be chosen such that the data from all lanes arrive in the elastic buffers before the next release opportunity. The RBD value must be set between 1 and K, but often it is set equal to K so that the deterministic latency is equal to a full multi-frame period.

   While RBD can be set to a much lower value in order to minimize latency, there are practical limits, such as timing skew across devices (for example, from internally registering SYSREF and distributing it). Latency from blocks, like 8b/10b encoding, must also be accounted for (**Figure 5**).

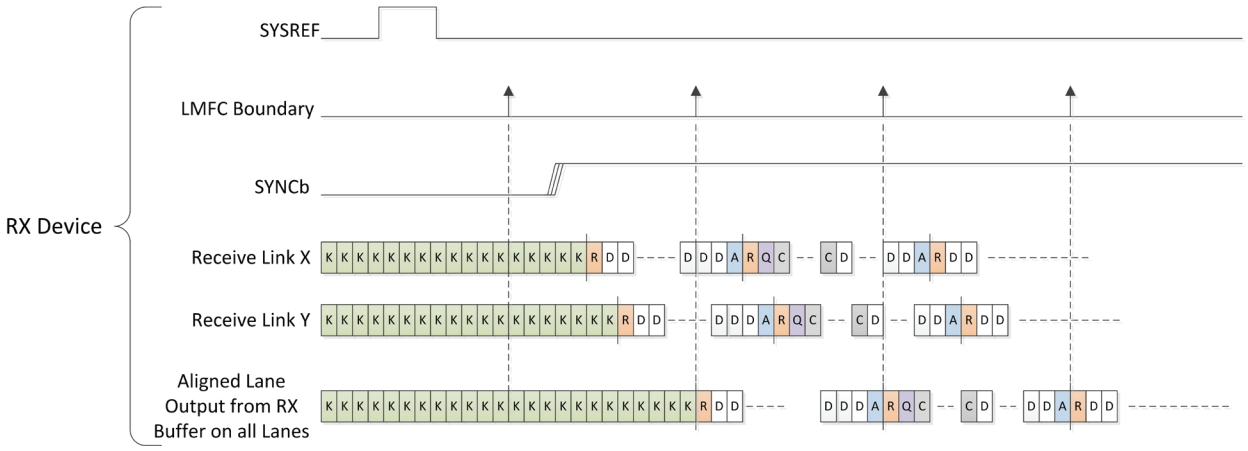


Figure 5. *Achieving deterministic latency in JESD204B receiving device.*

Serial Interface

Modern processors, such as the 66AK2L06, which integrates JESD204B and a digital front end, and high-speed data converters, such as the ADC16DX370, mostly employ a voltage-mode (VML) or current-mode logic (CML) serializer/deserializer (SerDes) transmitter (**Figure 6**). In CML, the two switching transistors are used to steer a constant current through the termination resistor, causing a differential voltage drop at the receiver.

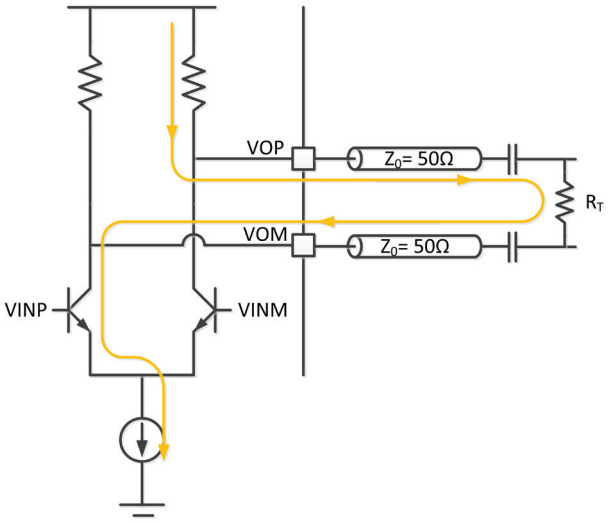


Figure 6. *Illustration of a CML transmitter.*

As next-generation high-speed data converters are moving towards more advanced CMOS processes, the inherent faster transistor switching speed enables higher data rates. On the other hand, the lower-geometry CMOS processes also drastically reduce the digital power consumption of the SerDes block, making the overall digital interface design very power efficient.

For example, the ADC16DX370 can transmit the sampled data over a single serial link at 7.4 Gbps to minimize board space and transmitter power consumption. Alternatively, it can use two serial links at 3.7 Gbps to trade board space for a potentially lower-cost processor.

Eye Diagram

System designers typically examine the quality of the serial link by looking at the eye diagram at the receiving device. It is obtained by overlaying the individual bits sent from the transmitter using a fast oscilloscope.

The eye diagram (**Figure 7**) is used to determine the receiver's ability to extract the correct information from the incoming data stream.

The eye amplitude illustrates how much loss is on the transmission channel. The larger the vertical eye opening, the easier it is for the receiver to determine the correct logic level.

The jitter specifies the deviation from the ideal switching point when the signal crosses through 0V (zero crossing point). A smaller jitter number translates to more timing margin when the receiver determines if the input signal is logic high or low.

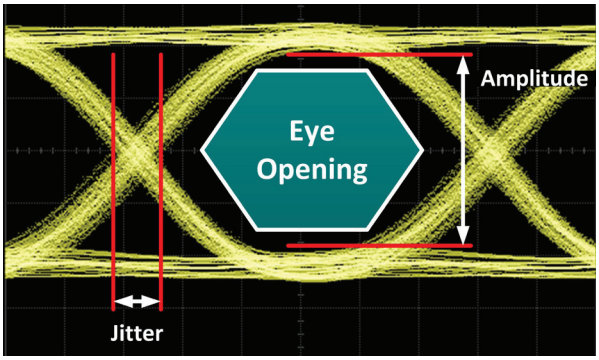


Figure 7. Eye diagram of a serial data link.

Since jitter has such a big impact on the link quality, the JESD204B standard specifies the jitter requirements for both transmitter (TX) and RX. The transmitter jitter is measured directly at the output. It documents how much the transmitter itself degrades the eye diagram prior to going into the transmission channel. The receive jitter is a measure of the jitter tolerance requirement. It indicates how much jitter the receiver has to tolerate while still extracting the correct information from the incoming data stream. The TX and RX jitter requirements are specified for three different max data rates, ranging from up to 3.125, up to 6.25 and up to 12.5 Gbps (**Figure 8**).

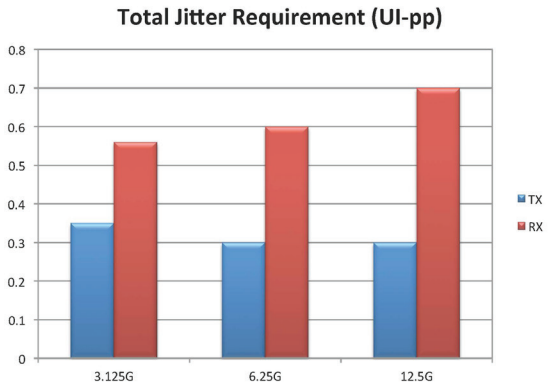


Figure 8. Jitter requirement comparison based on maximum link data rate.

Active Equalization Techniques

The serial link quality primarily depends on how well the receiver can recover the incoming data. A larger transmission distance causes more signal attenuation and shrinks the eye opening. The lossy PCB material essentially acts like a low-pass filter. One of the most efficient ways to counter the insertion loss is to add a high-pass filter in the form of either transmit pre- or de-emphasis or equalization in the SerDes receiver. Pre-emphasis adds extra output current to improve the signal rise and fall times, which boosts the amplitude of the higher order harmonics. De-emphasis, on the other hand, decreases the signal amplitude when no bit transitions happen (essentially attenuating lower frequency range). Hence, pre-emphasis and de-emphasis have about the same effect when trying to compensate the channel insertion loss (**Figure 9**).

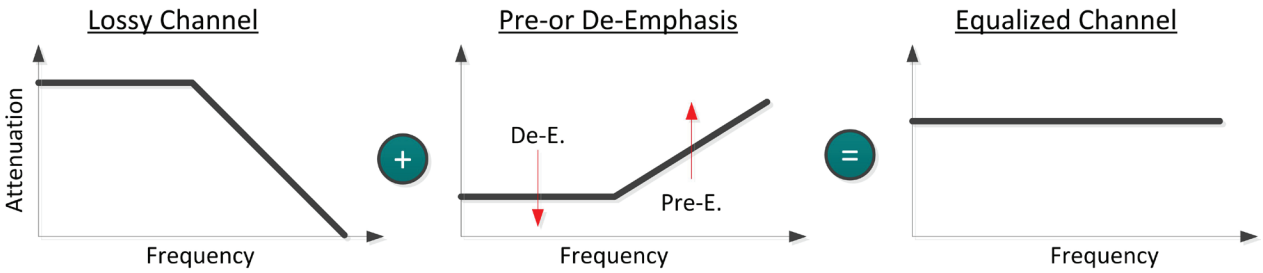
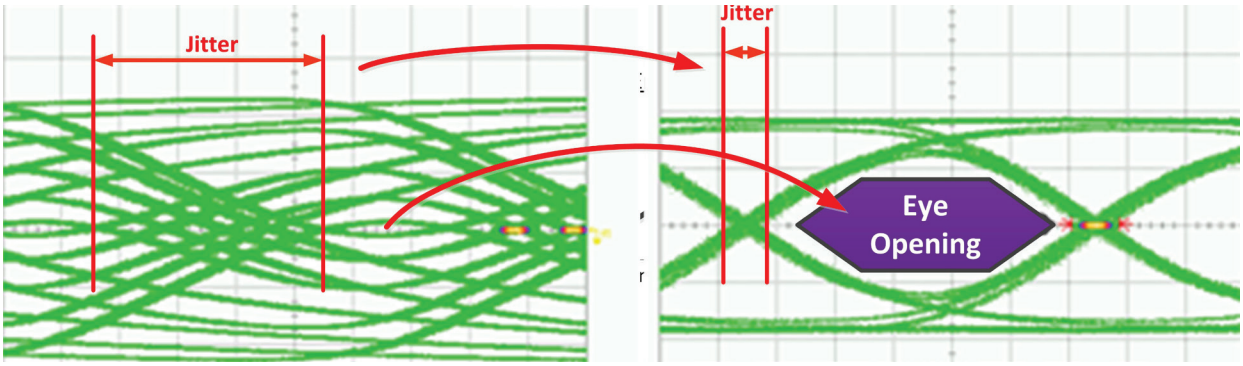


Figure 9. Equalization of a lossy transmission channel.



(a) *Before de-emphasis* ***(b)*** *After de-emphasis*

Figure 10. *Eye diagram after 20 inches of FR4 using ADC16DX370 @ 7.4 Gbps.*

The ADC16DX370 provides several different amounts of de-emphasis and output amplitude levels, which can be tuned to closely match different channel loss profiles. The SerDes receiver in the DAC38J84, a 4-channel, 16-bit, 2.5-GSPS DAC, provides full adaptive equalization, which automatically compensates the channel insertion loss. This is achieved by adjusting the placement of a transfer function zero-based on the received data, which also minimizes inter-symbol interference. Additionally, its receiver includes built-in eye scan and equalization analysis functions to determine if the transmit partner is applying more or less equalization than necessary. The advantage of the pre- and de-emphasis becomes quite apparent when examining the eye diagram at the receiver with and without de-emphasis (**Figure 10**).

Link Configuration

To ensure that the receiving device can reconstruct the transmitted data correctly, both TX and RX need to be set to the same link configuration. The JESD204B standard provides several different parameters, but it is up to the system designer to ensure that the transmitting and receiving device are set to the same configuration.

L = number of lanes per converter device

M = number of converters per device

F = number of octets per frame

S = samples per frame transmitted per single converter per frame cycle

For example, a data converter-to-a processor link can be configured using two lanes in two different configurations that are not compatible with each other. The link on the left side (LMFS = 2111) is configured to fill each converter sample across both lanes, consecutively, as it arrives. The link on the right side (LMFS = 2221) processes two samples at a time and assigns one sample across two octets (**Table 2**).

	LMFS = 2111					LMFS = 2221			
Lane 1	A_0[15:8]	A_1[15:8]	A_2[15:8]	A_3[15:8]		A_0[15:8]	A_0[7:0]	A_2[15:8]	A_2[7:0]
Lane 2	A_0[7:0]	A_1[7:0]	A_2[7:0]	A_3[7:0]		A_1[15:8]	A_1[7:0]	A_3[15:8]	A_3[7:0]

Table 2. *Comparison of two different JESD204B serial link configurations for one ADC.*

Octet	0	1	2	3	4	5	6	7
Lane 0	A_0[11:0]		A_8[11:0]	A_{16}[11:0]		A_{24}[11:0]	A_{32}[11:0]	TTTT
Lane 1	A_1[11:0]		A_9[11:0]	A_{17}[11:0]		A_{25}[11:0]	A_{33}[11:0]	TTTT
Lane 2	A_2[11:0]		A_{10}[11:0]	A_{18}[11:0]		A_{26}[11:0]	A_{34}[11:0]	TTTT
Lane 3	A_3[11:0]		A_{11}[11:0]	A_{19}[11:0]		A_{27}[11:0]	A_{35}[11:0]	TTTT
Lane 4	A_4[11:0]		A_{12}[11:0]	A_{20}[11:0]		A_{28}[11:0]	A_{36}[11:0]	TTTT
Lane 5	A_5[11:0]		A_{13}[11:0]	A_{21}[11:0]		A_{29}[11:0]	A_{37}[11:0]	TTTT
Lane 6	A_6[11:0]		A_{14}[11:0]	A_{22}[11:0]		A_{30}[11:0]	A_{38}[11:0]	TTTT
Lane 7	A_7[11:0]		A_{15}[11:0]	A_{23}[11:0]		A_{31}[11:0]	A_{39}[11:0]	TTTT

Table 3. *JESD204B link configuration for ADC12J4000.*

The JESD204B standard also provides the option to break up samples across multiple octets and lanes (**Table 3**). For example, two 12-bit samples can be transmitted using three octets. This feature is very beneficial when using data converters with lower resolution but very high sampling rates, such as the ADC12J4000.

The ADC12J4000 outputs 12 bits at 4 Gbps. It uses eight serial lanes to transmit 40 samples in one frame, then fills up the last octet with four tail bits. The LMFS configuration is LMFS = 8885.

Inside the processor firmware, the user typically specifies the L, F and K parameters. The designer then maps the output of the JESD block data to the desired logic, since one knows how many converters are involved. During the initial lane alignment procedure, key parameters (L, F, K, M, subclass and more) about the JESD link configuration are also transmitted, which are then verified against what is specified inside the receiving device.

Typically data converters are also equipped with several test pattern options (clock, ramp, custom pattern), which speed up the debug process during the initial bring-up phase.

Texas Instruments high-speed ADCs and DACs can be used with the 66AK2Lx processor family, as well as FPGAs from Altera and Xilinx. An example code is available upon request. However, IP licensing is needed in order to compile the code. **Table 4** lists TI high-speed data converters and wideband receivers and processors that support JESD204B.

ADC	Sampling Rate (Msps)	Resolution (bit)	Channels	Max SerDes Speed (Gbps)
ADC3k family	50 to 160	12/14	2/4	3.2
ADS42JB46	160	14	2	3.2
ADS42JB69	250	16	2	3.2
ADS42JB49	250	14	2	3.2
ADC16DX370	370	16	2	7.4
ADC12J1600	1600	12	1	4.0
ADC12J2700	2700	12	1	6.75
ADC12J4000	4000	12	1	10.0
Wideband Receiver	**Sampling Rate (Msps)**	**Resolution (bit)**	**Channels**	**Max Serdes Speed (Gbps)**
LM97937	370	9	2	7.4
LM15851	4000	12	1	10.0
DAC	**Sampling Rate (Msps)**	**Resolution (bit)**	**Channels**	**Max Serdes Speed (Gbps)**
DAC37J82	1600	16	2	12.5
DAC37J84	1600	16	4	12.5
DAC38J82	2500	16	2	12.5
DAC38J84	2500	16	4	12.5
SoC	**Cumulative Sampling Rate**	**Streams and Channels**	**Max SerDes Speed**	**Signal Processing**
66AK2L06	368 MSPS TX 368 MSPS RX	4 + 4 streams 24 + 24 channels	4 x 7.36 Gbps	16 to 24-bit datapaths Programmable FIR filter, CIC & farrow filter Numerically-controlled oscillator (NCO)/mixer Automatic gain control (AGC) Real-complex conversion, FFT

Table 4. *TI products that support the JESD204B interface.*

Summary

The JESD204B interface delivers a cleaner and more flexible digital interface compared to the traditional parallel interconnect. It reduces PCB area while addressing some of the more demanding system challenges, such as multi-chip synchronization. When transitioning to this new interface, the system designer needs to consider several aspects, such as clocking or synchronization, as outlined in this document.

Texas Instruments is fully committed to this new interface standard and offers a compelling data converter roadmap with state-of-the-art devices to support it. The applications staff at TI is prepared to help with all aspects of the design.

References

- Enabling Larger Phased-Array Radars With JESD204B, RF Globalnet, August 2, 2013
- Why JESD204B may solve a lot of your system design headaches, EDN, November 19 2013
- Tips & Tricks: JESD204B simplifies multi-chip synchronization, EDN, November 2, 2013
- JESD204B blog series, including topics such as deterministic latency, subclasses and link configuration
- When is the JESD204B interface the right choice, Surenna Gupta, Texas Instruments Analog Application Journal, 1Q 2014

Here's more information about:

JESD204B

ADCs

DACs

SerDes

Clocks

Processor

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265