Digital RF Power Control for Power Amplifier Protection in Wireless Base-Stations

ABSTRACT

In a wireless base-station (BS), when the output power of an RF power amplifier (PA) exceeds predefined limits, the antenna and other sensitive electronic components can be permanently damaged. This can lead to frequent and costly maintenance of BS equipment. Also very high PA output power causes neighboring BS cells to experience higher than normal interference. This is especially critical where code-division multiple access is used (that is, in W-CDMA systems). Multiple BS share the same frequency spectrum so signals from one BS appear as noise to another BS. Thus power control is important to keep the in-band noise level low and achieve reasonable carrier to noise ratio. Power control is also important in systems using frequency division multiple access to achieve a high frequency reuse factor.

In the SNWA003, a technique to control the RF power is introduced. It uses a directional coupler to sense the RF power, an LMV232 RF power detector to compute the mean square power, a control circuit and an attenuator to adjust the RF power. Figure 1 shows this approach.

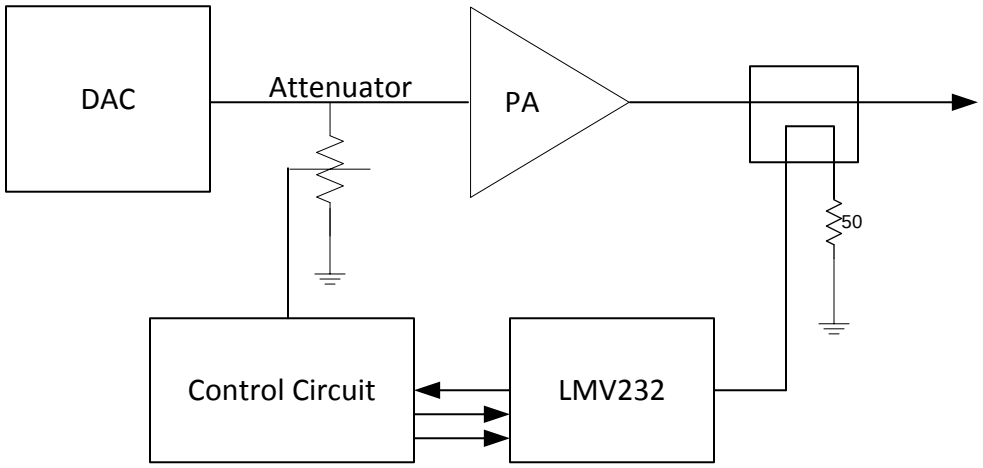

Figure 1. RF Power Control with LMV232

A digital based alternative to SNWA003 is discussed here and the block diagram is shown in Figure 2. It is referred to as Power Amplifier Protection (PAP). The PAP block monitors continuously the running average of the input signal magnitude and compares it to a programmable threshold. If the running average exceeds the threshold, a control signal from the PAP block to an attenuator is triggered which causes the output power to reduce gradually to zero. Digital to analog converters like DAC38J8x and DAC38RF8x devices integrate this approach so that RF power control can be achieved with no extra external components.

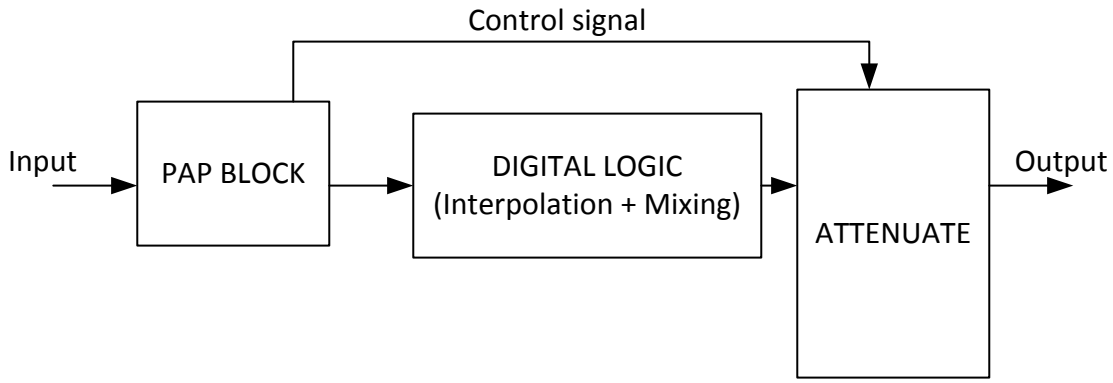

Figure 2. Digital RF Power Control (PAP Block)

1 State Transitions of PAP Block

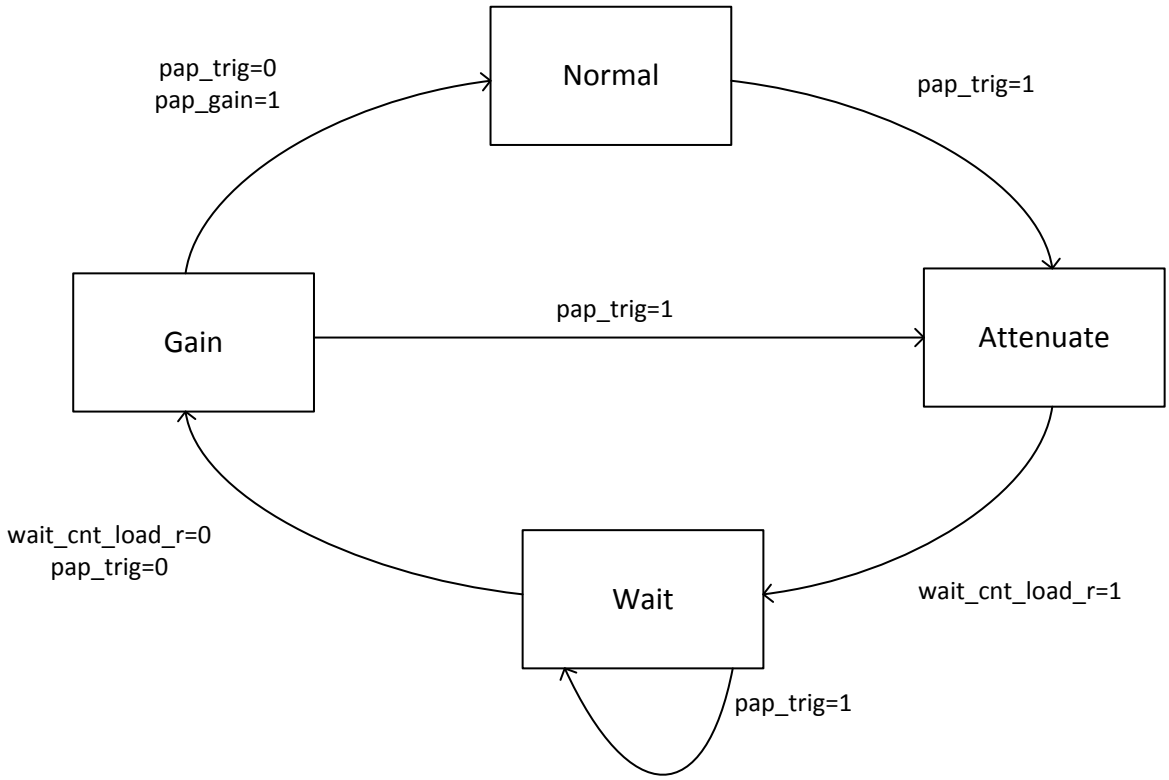

Figure 3. State Diagram of PAP block

1.1 NORMAL State

This is the normal operating condition for the PAP block. Input and output data of PAP block are the same.

1.2 ATTENUATE State

When the PAP block detects an error condition (or when the average power exceeds a pre-defined threshold) it sets the pap_trig signal to '1' causing a state transition from NORMAL operation to ATTENUATE. In the ATTENUTATE state the data path gain (*pap_gain*) is scaled from 1 down to 0 by an attenuator with programmable step size. Each clock cycle (16 samples) the gain is stepped down until the*pap_gain* is 0.

1.3 WAIT State

After the *pap_trig* is 0, the state machine transitions to the WAIT state. Here a programmable counter counts down to allow the condition causing the *pap_trig* to be asserted to be fixed. The number of clock cycles the counter counts is programmable. Once the counter equals zero and *pap_trig* = '0', the state machine transitions to the GAIN state.Figure 4 shows the effect of different wait times when transitioning to the GAIN state. If the wait counter equals 0 but *pap_trig* still equals '1' then the state machine stays in the WAIT state until *pap_trig* = '0'.

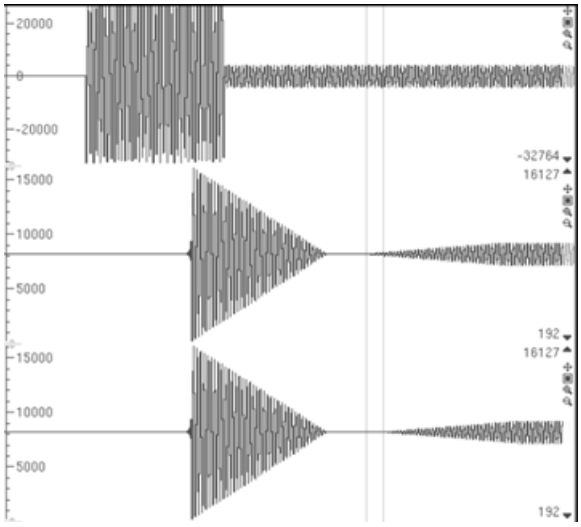

Figure 4. PAP output showing effect of wait time on ATTENUATE to GAIN transition

1.4 GAIN State

The attenuation that was applied in the ATTENUATE state is reversed to restore full signal power. In this state, the data path gain is ramped up from 0 to 1.

Table 1 summarizes the configurable parameters of the PAP block.

Table 1. Configurable Parameters

PARAMETER	DESCRIPTION	ACRONYM
Threshold	Sets the average power threshold	mem_threshold
Step size	Step size of the attenuator and gain blocks	mem_pap_gain_step
Wait	Minimum clock cycles to wait between attenuate and gain state	mem_pap_wait
Length	Number of samples used to compute the average power. Available options are 32, 64 or 128	mem_length

2 Implementation and IIR Filter Model

A section of the PAP block is shown in Figure 5. The input to the PAP block consists of the MSB byte (or bits 15:8) of eight consecutive 16-bit samples (this is denoted as x[7:0][15:8] in Figure 5). The absolute value of the input data is found before summing. The summer output is fed into the positive input of an accumulator and a delayed version of the summer output is also fed to the accumulators negative input. The summers output is delayed by an amount specified by the parameter *mem_length*. The other positive input to the accumulator comes from the previous accumulator output (y[n-1]). A comparator compares the current accumulator output value (y[n]) with the parameter *mem_threshold* and generates a *pap_trig* signal if y[n] is greater than *mem_threshold*.

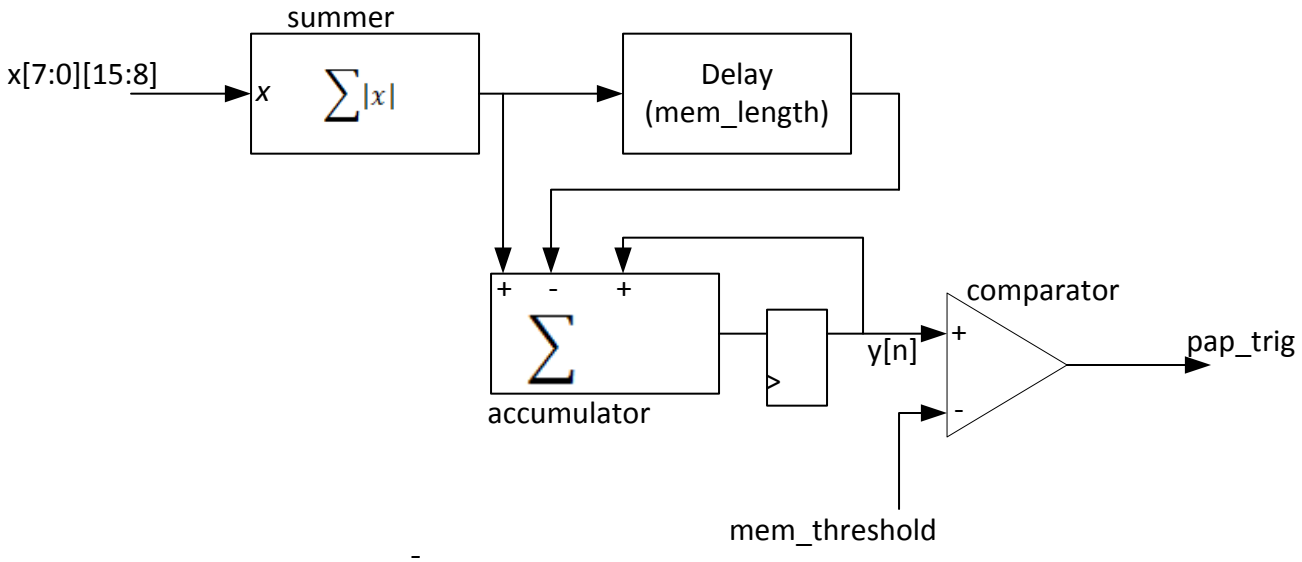

Figure 5. Block Diagram of Power Amplifier Protection (PAP)

Consequently, the output of the accumulator in PAP block can be modeled by the following IIR filter Equation 1.

$$y[n] = y[n-1] + \left(x[n] - x\right)^{\left\lfloor \left(\frac{n - mem\_length}{8}\right) \right\rfloor}_{\left(\frac{mem\_length}{16}\right)} \quad (1)$$

Where:

y[n] → output of PAP accumulator block (*mem_threshold* is compared to y[n]).

x[n] → sum of absolute values of MSB byte of 8 consecutive 16-bits input.

mem_length → Length of moving average filter.

An example script written in MATLAB to compute the output of the accumulator is given in Figure 6. The input (x[n]) is 16-bits sine wave with two amplitude values that differ by ¼ (Figure 7). The output of the accumulator (y[n]) for this input for the three different *mem_length* settings (32, 64 and 128) is shown in Figure 8.

```
%------Generate input signal to PAP block-------%
N=2^16; % number of samples
Fs=200e6; %sampling frequency
fin=10e6; %input frequency
t=0:1/Fs:(N-1)/Fs; % time vector
x=2^15*sin(2*pi*fin*t)'; %16bits 10MHz sine wave
x=[x(1:N/2);0.25*x(1+N/2:N)];

 %------compute absolute value of MSB byte of 8 consecutive samples and sum-------%
msb_sel=x(:,1)/256;
sum_abs=sum(abs(reshape(msb_sel,8,[])));

%------Generate the accumulator output-------%
accm_out_32=filter([1,0,0,0,-1]/2,[1,-1],sum_abs(1:end));% implements the difference equation: y(n)=y(n-1)+[x(n)-x(n-4)]/2
accm_out_64=filter([1,0,0,0,0,0,0,0,-1]/4,[1,-1],sum_abs(1:end));% implements the diff equation: y(n)=y(n-1)+[x(n)-x(n-8)]/4
accm_out_128=filter([1,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,-1]/8,[1,-1],sum_abs(1:end));% implements the diff equation: y(n)=y(n-1)+[x(n)-x(n-16)]/8

plot(accm_out_32,'b')
hold on
plot(accm_out_64,'r')
plot(accm_out_128,'g')
hold off
```

Figure 6. Example MATLAB Script to Compute Accumulator Output of PAP Block

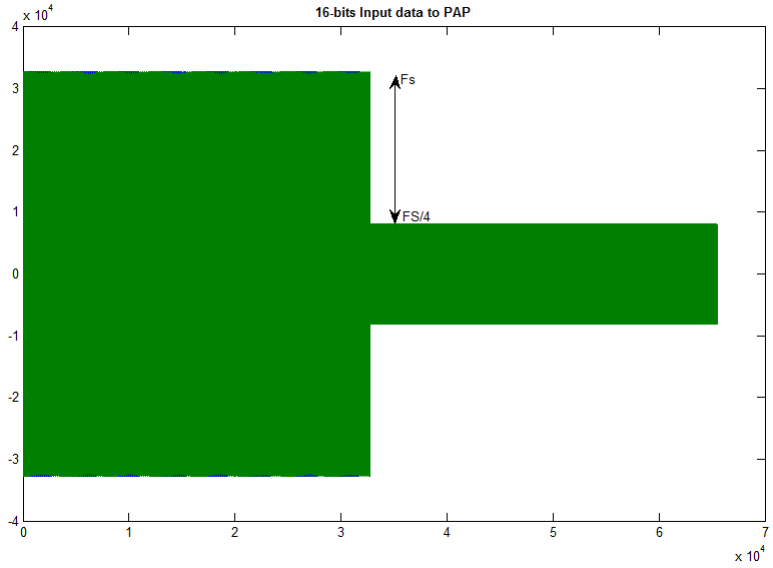

Figure 7. Two-Level Sine Wave Input to PAP Block

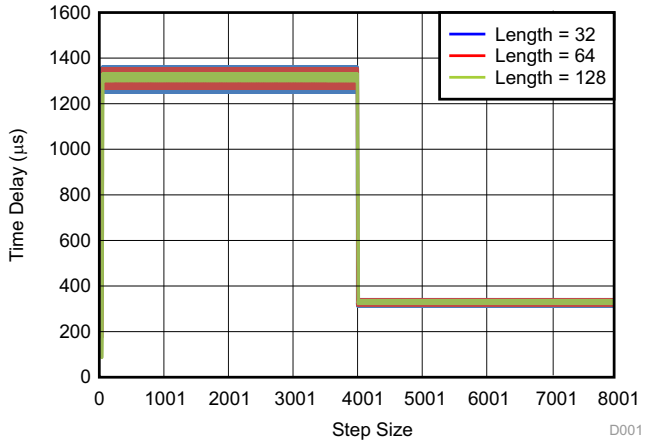

Figure 8. Accumulator Output of 2-Level Sine Wave Input

Based on the 2-level sine wave input to the PAP block in Figure 7 and the resulting accumulator output in Figure 8, when the parameter *mem_threshold* is set to 1000, the final output of the PAP block is as shown in Figure 9. The state machine transitions through all the four states: ATTENUATE (A), WAIT (B), GAIN (C) and NORMAL (D).

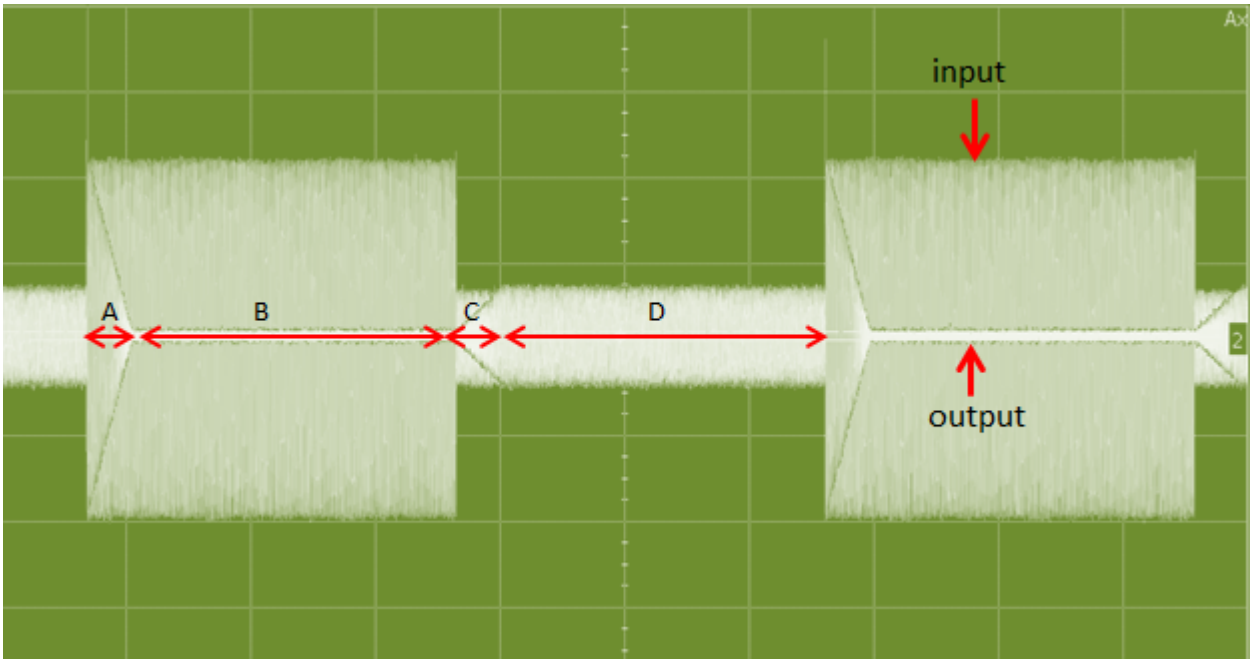

Figure 9. Output of PAP Block for a 2-Level Sine Wave Input and *mem_threshold* = 1000.

3 Step Size and Response Time

The response time is defined as the time the PAP state machine stays in either the ATTENUATE state (state A in Figure 9) or GAIN state (state C in Figure 9).

The response time is inversely proportional to the step size (*mem_pap_gain_step*) and at high step size, it is also directly proportional to the length parameter (*mem_length*). This is illustrated in Figure 10 and Figure 11.

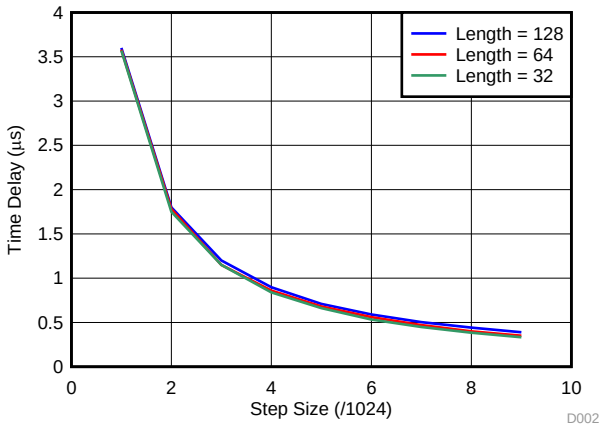

Figure 10. Response Time vs Step Size (Low Step Size)

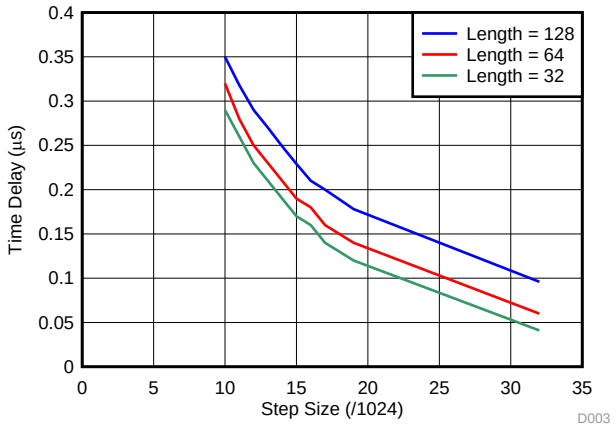

Figure 11. Response Time vs Step Size (High Step Size)

4 Power Amplifier Protection in DAC38RF8x Devices

The DAC38RF8xx is a family of 9 GSPS digital to analog converters that integrate the PAP block discussed in the previous sections. This enables system designers to easily control the RF output power below a specified threshold without the need for extra external components or data processing. The DAC38RF8x EVM (Evaluation module) and the accompanying graphical user interface (GUI) can be used to test the functionality of the DAC and all its features including the PAP. The user interface of the PAP block is shown in Figure 12 and Table 2 describes the functions of all the controls and indicators on the interface.

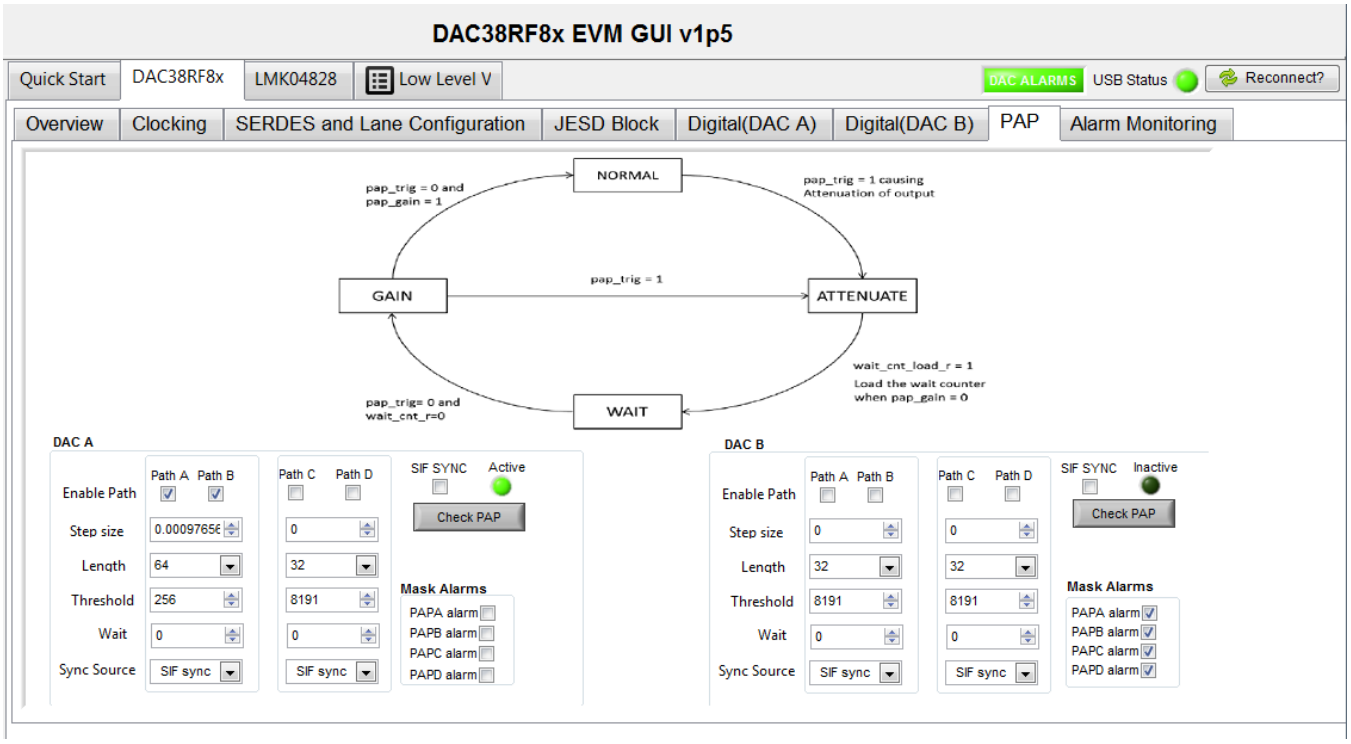

Figure 12. Graphic User Interface of PAP Block in DAC38RF8x Devices

Table 2. Description of GUI Controls/Indicators of PAP block

CONTROL/INDICATORS	FUNCTION
Enable Path	Enables the power amplifier protection (PAP) logic
Step size	Gain attenuation step size for the PAP logic
Length	Controls the moving average length
Threshold	Threshold used to trigger PAP logic
Wait	# of clock cycles to wait between ATTENUATE and GAIN states
Sync Source	used to sync the PAP logic
SIF SYNC	used to trigger a sync event when SIF SYNC is selected as the SYNC SOURCE
Active	Indicates when the PAP logic is triggered.
	ACTIVE = bright green, INACTIVE = dull green
Check PAP	Used to read back the current state of the PAP logic.
	If PAP logic is triggered, the Active LED will turn bright green and cannot be reset to dull green by clicking on this LED
	Note: If PAP logic is not triggered, ACTIVE LED can be toggled between bright and dull green by clicking on the LED

For a 2 x 20 MHz LTE signal centered at 1.79 GHz, the output spectra with and without the PAP in DAC38RF8x enabled is shown in Figure 12. When the PAP is enabled, threshold = 256, Length = 64 and step size = 1/1024.

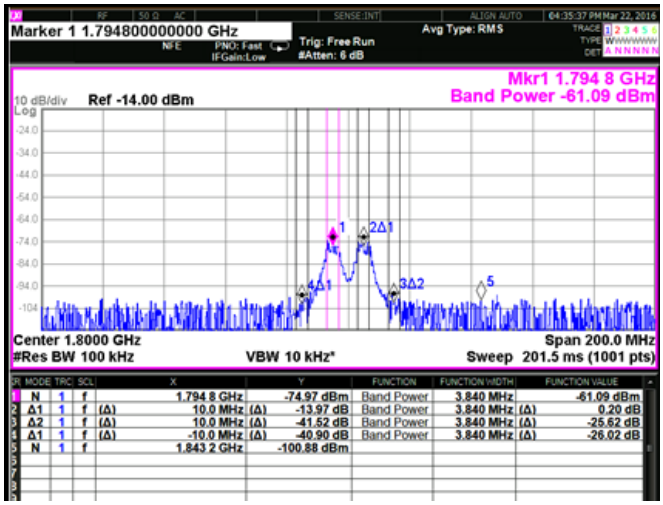

Figure 13. Spectrum With PAP Enabled

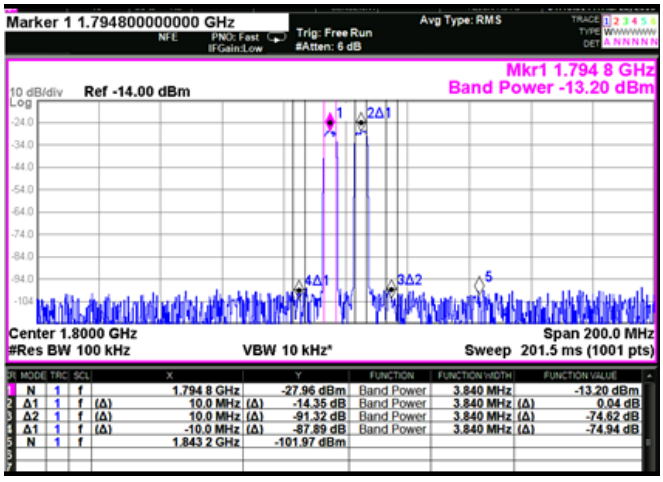

Figure 14. Spectrum With PAP Disabled

5 References

1) AN-1433 Base Station Closed-Loop RF Power Control with LMV232 Crest-Fac, Application report, SNWA003.

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