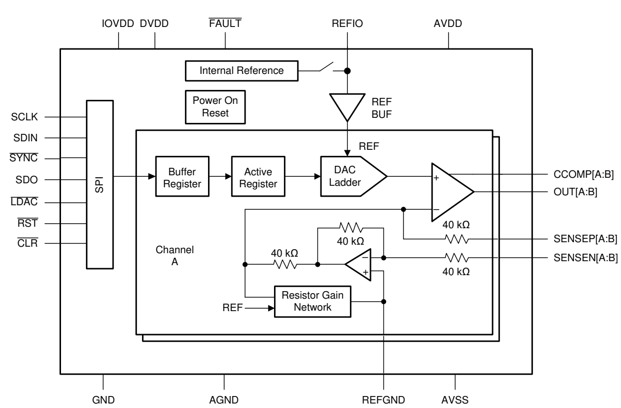
DACx1402 Dual, 16-Bit and 12-Bit, High-Voltage-Output DACs With Internal Reference

1 Features

- Performance:
  - Specified monotonic at 16-bit resolution
  - INL: ±1 LSB maximum at 16-bit resolution
  - TUE: ±0.05% FSR, maximum
- Integrated output buffer
  - Full-scale output voltage: ±5 V, ±10 V, ±20 V, 5 V, 10 V, 20 V, 40 V
  - High drive capability: ±15 mA
  - Per channel sense pins
- Integrated 2.5-V precision reference
  - Initial accuracy: ±2.5 mV, maximum
  - Low drift: 10 ppm/°C, maximum
- Reliability features:
  - CRC error check
  - Short-circuit limit
  - Fault pin
- 50-MHz, SPI-compatible serial interface
  - 4-wire mode, 1.7-V to 5.5-V operation
  - Readback and daisy-chain operations
- Temperature range: –40°C to +125°C
- Package: 5-mm × 5-mm, 32-pin QFN

2 Applications

- Servo drive control module
- Analog output module
- Lab and field Instrumentation
- Data acquisition (DAQ)
- Semiconductor test



Functional Block Diagram

3 Description

The 16-bit DAC81402 and 12-bit DAC61402 (DACx1402) are pin-compatible, dual-channel, buffered, high-voltage-output, digital-to-analog converters (DACs). These devices include a low-drift, 2.5-V internal reference that eliminates the need for an external precision reference in most applications. The devices are specified monotonic and provide high linearity of ±1 LSB INL. Additionally, the devices implement per channel sense pins that eliminate IR drops and sense up to ±12 V of ground bounce.

A user-selectable output configuration enables full-scale bipolar output voltages of ±20 V, ±10 V, and ±5 V; and full-scale unipolar output voltages of 40 V, 20 V, 10 V and 5 V. The full-scale output range for each DAC channel is independently programmable. The integrated DAC output buffers can sink or source up to 15 mA, thus limiting the need for additional operational amplifiers.

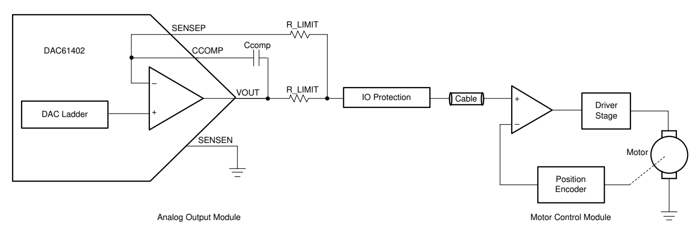
The DACx1402 incorporate a power-on-reset circuit that connects the DAC outputs to ground at power up. The outputs remain in this mode until the device is properly configured for operation. The devices include additional reliability features such as a CRC error check, short-circuit protection, and a thermal alarm.

Communication to the devices is performed through a 4-wire serial interface that supports operation from 1.7 V to 5.5 V.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
DAC81402	VQFN (32)	5.00 mm × 5.00 mm
DAC61402		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Motor Drive Application

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4 Revision History

Changes from Revision * (November 2020) to Revision A (May 2021) — **Page**

- Added DAC81402 and associated content........1

5 Device Comparison Table

DEVICE	RESOLUTION
DAC81402	16-Bit
DAC61402	12-Bit

6 Pin Configuration and Functions

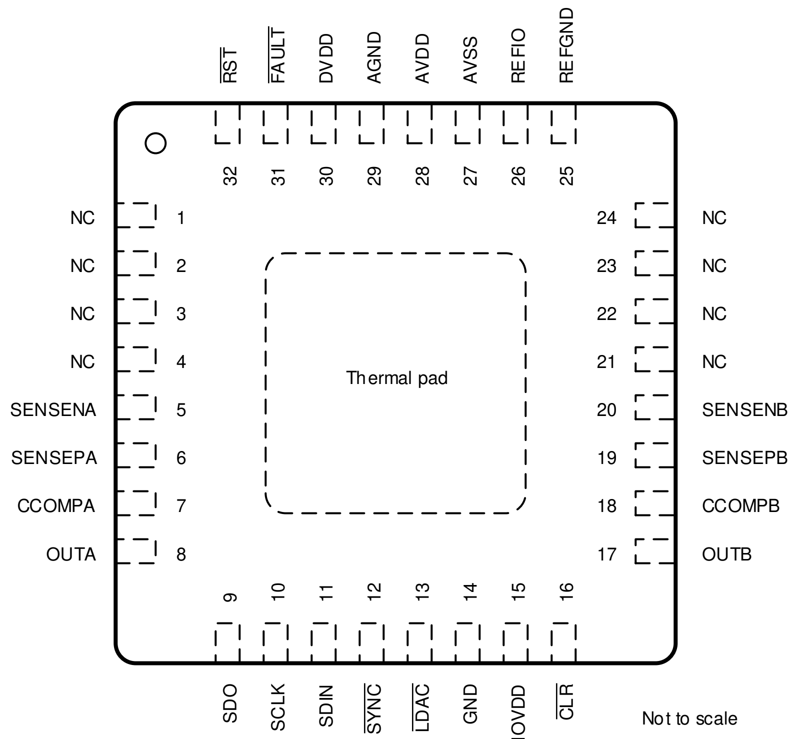


Figure 6-1. RHB (32-pin VQFN) Package, Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	NC	—	No connection.
2	NC	—	No connection.
3	NC	—	No connection.
4	NC	—	No connection.
5	SENSENA	Input	Channel-A sense pin for the negative voltage output load connection.
6	SENSEPA	Input	Channel-A sense pin for the positive voltage output load connection.
7	CCOMPA	Input	Channel-A external compensation capacitor connection pin. The addition of an external capacitor improves the output buffer stability with high capacitive loads at the OUTA pin by reducing the bandwidth of the output amplifier at the expense of increased settling time.
8	OUTA	Output	Channel-A analog output voltage.
9	SDO	Output	Serial interface data output. The SDO pin must be enabled before operation by setting the SDO-EN bit. Data are clocked out of the input shift register on either rising or falling edges of the SCLK pin as specified by the FSDO bit (rising edge by default).
10	SCLK	Input	Serial interface clock.
11	SDIN	Input	Serial interface data input. Data are clocked into the input shift register on each falling edge of the SCLK pin.

Table 6-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
12	$\overline{SYNC}$	Input	Active low serial data enable. This input is the frame synchronization signal for the serial data. The serial serial interface input shift register is enabled when $\overline{SYNC}$ is low.
13	$\overline{LDAC}$	Input	Active low synchronization signal. The DAC outputs of those channels configured in synchronous mode are updated simultaneously when the $\overline{LDAC}$ pin is low. Connect to IOVDD if unused.
14	GND	Ground	Digital ground reference point.
15	IOVDD	Power	IO supply voltage. This pin sets the digital I/O operating voltage for the device.
16	$\overline{CLR}$	Input	Active-low clear input. Logic low on this pin clears all outputs to their clear code. Connect to IOVDD if unused.
17	OUTB	Output	Channel-B analog output voltage.
18	CCOMPB	Input	Channel-B external compensation capacitor connection pin. The addition of an external capacitor improves the output buffer stability with high capacitive loads at the OUTB pin by reducing the bandwidth of the output amplifier at the expense of increased settling time.
19	SENSEPB	Input	Channel-B sense pin for the positive voltage output load connection.
20	SENSENB	Input	Channel-B sense pin for the negative voltage output load connection.
21	NC	—	No connection.
22	NC	—	No connection.
23	NC	—	No connection.
24	NC	—	No connection.
25	REFGND	Ground	Ground reference point for the internal reference.
26	REFIO	Input/Output	Reference input to the device when operating with an external reference. Reference output voltage pin when using the internal reference. Connect a 150-nF capacitor to ground.
27	AVSS	Power	Output buffers negative supply voltage.
28	AVDD	Power	Output buffers positive supply voltage.
29	AGND	Ground	Analog ground reference point.
30	DVDD	Power	Digital and analog supply voltage.
31	$\overline{FAULT}$	Output	$\overline{FAULT}$ is an open-drain, fault-condition output. An external 10-kΩ pullup resistor to a voltage no higher than IOV_{DD} is required.
32	$\overline{RST}$	Input	Active-low reset input. Logic low on this pin causes the device to issue a power-on-reset event.
Thermal Pad	Thermal pad	—	The thermal pad is located on the package underside. The thermal pad should be connected to any internal PCB ground plane through multiple vias for good thermal performance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
	Supply voltage	DV_{DD} to GND	–0.3	6	V
		IOV_{DD} to GND	–0.3	6	
		AV_{DD} to GND	–0.3	44	
		AV_{SS} to GND	–22	0.3	
		AV_{DD} to AV_{SS}	–0.3	44	
	Pin voltage	V_{OUTX} to GND	AV_{SS} – 0.3	AV_{DD} + 0.3	V
		$V_{SENSEPX}$ to GND	AV_{SS} – 0.3	AV_{DD} + 0.3	
		$V_{SENSENX}$ to GND	AV_{SS} – 0.3	AV_{DD} + 0.3	
		V_{REFIO} to GND	–0.3	DV_{DD} + 0.3	
		V_{REFGND} to GND	–0.3	+0.3	
		Digital inputs to GND	–0.3	IOV_{DD} + 0.3	
		SDO to GND	–0.3	IOV_{DD} + 0.3	
		$\overline{FAULT}$ to GND	–0.3	6	
	Input current	Current into any digital pin	–10	10	mA
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–60	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Supply voltage	DV_{DD} to GND	4.5		5.5	V
		IOV_{DD} to GND	1.7		5.5	
		AV_{DD} to GND	4.5		41.5	
		AV_{SS} to GND	–21.5		0	
		AV_{DD} to AV_{SS}	4.5		43	
	Pin voltage	$V_{SENSENX}$ to GND	–12		12	V
T_A	Ambient temperature		–40		125	°C

7.4 Thermal Information

THERMAL METRIC[(1)]		DACx1402 RHB (VQFN) 32 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	29.3	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	17.0	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	9.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.5	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

all minimum/maximum specifications at T_A = –40°C to +125°C and all typical specifications at T_A = 25°C, AV_{DD} = 4.5 V to 41.5 V, AV_{SS} = –21.5 V to 0 V, DV_{DD} = 5.0 V, internal reference enabled, IOV_{DD} = 1.7 V, $V_{SENSENX}$ = 0 V, C_{COMPX} floating, DAC outputs unloaded, and digital inputs at IOV_{DD} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution	DAC81402	16			Bits
		DAC61402	12			
INL	Relative accuracy[1]	DAC81402. All ranges, except 0-V to 40-V and overranges	–1		1	LSB
		DAC81402. 0-V to 40-V range	–2		2	
		DAC61402	–1		1	
DNL	Differential nonlinearity[1]		–1		1	LSB
TUE	Total unadjusted error[1]	Unipolar ranges, AV_{SS} = 0 V	–0.07		0.07	%FSR
		Unipolar ranges, AV_{SS} = 0 V, 0°C ≤ T_A ≤ 50°C	–0.05		0.05	
		Bipolar ranges, –21.5 V ≤ AV_{SS} < 0 V	–0.05		0.05	
	Offset error[1]	Unipolar ranges, AV_{SS} = 0 V Bipolar ranges, –21.5 V ≤ AV_{SS} < 0 V	–0.05		0.05	%FSR
	Offset error temperature coefficient	Unipolar ranges, AV_{SS} = 0 V Bipolar ranges, –21.5 V ≤ AV_{SS} < 0 V		±2		ppmFSR/°C
	Zero-code (negative full scale) error	All unipolar ranges, AV_{SS} = 0 V			0.15	%FSR
		All bipolar ranges, –21.5 V ≤ AV_{SS} < 0 V			0.05	
	Zero-code (negative full scale) error temperature coefficient	All unipolar ranges, AV_{SS} = 0 V All bipolar ranges, –21.5 V ≤ AV_{SS} < 0 V		±2		ppm of FSR/°C
	Full-scale error[2]		–0.06		0.06	%FSR
	Full-scale error temperature coefficient[2]			±3		ppm of FSR/°C
	Gain error[1]		–0.06		0.06	%FSR
	Gain error temperature coefficient			±2		ppm of FSR/°C
	Bipolar-zero (midscale) error	All bipolar ranges, –21.5 V ≤ AV_{SS} < 0 V	–0.03		0.03	%FSR
	Bipolar-zero (midscale) error temperature coefficient	All bipolar ranges, –21.5 V ≤ AV_{SS} < 0 V		±2		ppm of FSR/°C
	Output voltage drift over time	T_A = 40°C, DAC code = full scale, 1000 hours		±6		ppm FSR

7.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and all typical specifications at T_A = 25°C, AV_{DD} = 4.5 V to 41.5 V, AV_{SS} = –21.5 V to 0 V, DV_{DD} = 5.0 V, internal reference enabled, IOV_{DD} = 1.7 V, $V_{SENSENX}$ = 0 V, C_{COMPX} floating, DAC outputs unloaded, and digital inputs at IOV_{DD} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage		0		5	V
		20% overrange	0		6	
			0		10	
		20% overrange	0		12	
			0		20	
		20% overrange	0		24	
			0		40	
			-5		5	
		20% overrange	-6		6	
			–10		10	
		20% overrange	–12		12	
			–20		20	
	Output voltage headroom and footroom	to AV_{SS} and AV_{DD} −10 mA ≤ load current ≤ 10 mA	1.25			V
		to AV_{SS} and AV_{DD}, 5.5 V < AV_{DD} ≤ 41.5 V, −15 mA ≤ load current ≤ 15 mA	1.5			
	Short circuit current[(3)]	Full-scale output shorted to AV_{SS}		40		mA
		Zero-scale output shorted to AV_{DD}, 5.5 V < AV_{DD} ≤ 41.5 V,		40		
		Zero-scale output shorted to AV_{DD}, 4.5 V ≤ AV_{DD} ≤ 5.5 V		25		
	Load regulation	DAC at midscale, −15 mA ≤ load current ≤ 15 mA		50		µV/mA
C_L	Capacitive load[(4)]	R_{LOAD} = open, C_{COMPX} pin left floating	0		2	nF
		R_{LOAD} = open, C_{COMPX} = 500 pF ± 10% to V_{OUTX}			1	µF
	Load current[(4)]	5.5 V < AV_{DD} ≤ 41.5 V			15	mA
		4.5 V ≤ AV_{DD} ≤ 5.5 V			10	
	V_{OUT} dc output impedance	DAC code at midscale, DAC unloaded		0.05		Ω
		DAC code at full scale, DAC unloaded		0.05		
		DAC code at negative full scale, DAC unloaded		25		
	V_{SENSEP} dc output impedance	DAC code at midscale, 10-V span		55		kΩ
		DAC disabled		45		
	V_{SENSEN} dc output impedance	DAC code at midscale, 10-V span		45		kΩ
		DAC disabled		45		

7.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and all typical specifications at T_A = 25°C, AV_{DD} = 4.5 V to 41.5 V, AV_{SS} = –21.5 V to 0 V, DV_{DD} = 5.0 V, internal reference enabled, IOV_{DD} = 1.7 V, $V_{SENSENX}$ = 0 V, C_{COMPX} floating, DAC outputs unloaded, and digital inputs at IOV_{DD} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE						
	Output voltage settling time	5-V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2 LSB		7		µs
		10-V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2 LSB		8		µs
		20-V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2 LSB		12		µs
		40-V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2 LSB		22		µs
		5-V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2 LSB, C_L = 1 µF, C_{COMPX} = 500 pF to V_{OUTX}		0.6		ms
		10-V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2 LSB, C_L = 1 µF, C_{COMPX} = 500 pF to V_{OUTX}		0.6		ms
		20-V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2 LSB, C_L = 1 µF, C_{COMPX} = 500 pF to V_{OUTX}		0.6		ms
		40-V span, 1/4 to 3/4 scale and 3/4 to 1/4 scale, settling time to ±2 LSB, C_L = 1 µF, C_{COMPX} = 500 pF to V_{OUTX}		1.2		ms
	Slew rate	0-V to 5-V range (10% to 90% of full-scale range)		0.8		V/µs
		All other output ranges except 40-V span (10% to 90% of full-scale range)		4		V/µs
		0-V to 5-V range, C_L = 1 µF, C_{COMPX} = 500 pF to V_{OUTX}		0.04		V/µs
		All other ranges, C_L = 1 µF, C_{COMPX} = 500 pF to V_{OUTX}		0.04		V/µs
	Power-on glitch magnitude	AV_{SS} and AV_{DD} ramped symmetrically, ramp rate = 18 V/ms, output unloaded, internal reference		0.1		V
	Output enable glitch magnitude	AV_{SS} and AV_{DD} ramped, output unloaded, internal reference, gain = 1x		0.35		V
	Output noise	0.1 Hz to 10 Hz, DAC code at midscale, 5-V span, external reference = 2.5 V, output unloaded		25		$µV_{PP}$
		0.1 Hz to 10 Hz, DAC code at midscale, 5-V span, internal reference = 2.5 V, output unloaded		30		$µV_{PP}$
	Output noise density	1 kHz, DAC code at midscale, 5-V span, output unloaded, external reference		115		nV/√Hz
		10 kHz, DAC code at midscale, 5-V span, output unloaded, external reference		105		nV/√Hz
THD	Total harmonic distortion	1-kHz sine wave on V_{OUTX}, output unloaded, DAC update rate = 400 kHz		88		dB
PSRR-AC	Power supply ac rejection ratio	V_{OUTX} = 0 V (midscale), output unloaded, ±10-V output, frequency = 60 Hz, amplitude 200 mV_{PP}, superimposed on AV_{DD}, DV_{DD} or AV_{SS}		75		dB

7.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and all typical specifications at T_A = 25°C, AV_{DD} = 4.5 V to 41.5 V, AV_{SS} = –21.5 V to 0 V, DV_{DD} = 5.0 V, internal reference enabled, IOV_{DD} = 1.7 V, $V_{SENSENX}$ = 0 V, C_{COMPX} floating, DAC outputs unloaded, and digital inputs at IOV_{DD} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR-DC	Power supply dc rejection ratio	V_{OUTX} = 0 V (midscale), ±10-V output, DV_{DD} = 5 V, AV_{DD} = 15 V ± 20%, AV_{SS} = –15 V, output unloaded		5		µV/V
		V_{OUTX} = 0 V (midscale), ±10-V output, DV_{DD} = 5 V, AV_{DD} = 15 V, AV_{SS} = –15 V ± 20%, output unloaded		10		
		V_{OUTX} = 0 V (midscale), ±10-V output, DV_{DD} = 5 V ± 5%, AV_{DD} = 15 V, AV_{SS} = –15 V, output unloaded		0.2		mV/V
	Code change glitch impulse	1-LSB change around midscale, 0-V to 5-V range, output unloaded		1		nV-s
		1-LSB change around midscale, 0-V to 10-V range, output unloaded		2		
		1-LSB change around midscale, –5-V to +5-V range, output unloaded		2		
		1-LSB change around midscale, –10-V to +10-V range, output unloaded		4		
	Code change glitch amplitude	1-LSB change around midscale, 0-V to 5-V, 0-V to 10-V, –5-V to +5-V and –10-V to +10-V ranges, output unloaded		±10		mV
	Channel-to-channel ac crosstalk	10-V span, full-scale swing on all other channel, measured channel at midscale, output unloaded		1		nV-s
	Channel-to-channel dc crosstalk	10-V span, full-scale swing on all other channel, measured channel at midscale, output unloaded		1		LSB
	Digital crosstalk	10-V span, full-scale swing on all other input buffer, measured channel at midscale, output unloaded		1		nV-s
	Digital feedthrough	DAC code at midscale, f_{SCLK} = 1 MHz, output unloaded		1		nV-s

7.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and all typical specifications at T_A = 25°C, AV_{DD} = 4.5 V to 41.5 V, AV_{SS} = –21.5 V to 0 V, DV_{DD} = 5.0 V, internal reference enabled, IOV_{DD} = 1.7 V, $V_{SENSENX}$ = 0 V, C_{COMPX} floating, DAC outputs unloaded, and digital inputs at IOV_{DD} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL REFERENCE INPUT						
V_{REFIO}	Reference input voltage		2.49	2.5	2.51	V
	Reference input current			50		µA
	Reference input impedance			50		kΩ
	Reference input capacitance			90		pF
INTERNAL REFERENCE						
	Reference output voltage	T_A = 25°C	2.4975		2.5025	V
	Reference output drift			5	10	ppm/°C
	Reference output impedance			0.15		Ω
	Reference output noise	0.1 Hz to 10 Hz		12		$µV_{PP}$
	Reference output noise density	10 kHz, V_{REFIO} = 10 nF		240		nV/√Hz
	Reference load current			5		mA
	Reference load regulation	Source		120		µV/mA
	Reference line regulation			100		µV/V
	Reference output drift over time	T_A = 40°C, 1000 hours		±300		µV
	Reference thermal hysteresis	First cycle		±125		µV
		Additional cycle		±25		
DIGITAL INPUTS AND OUTPUTS						
V_{IH}	Input high voltage		0.7 × IOV_{DD}			V
V_{IL}	Input low voltage				0.3 × IOV_{DD}	V
	Input current			±2		µA
	Input pin capacitance			2		pF
V_{OH}	SDO, high-level output voltage	SDO load current = 0.2 mA	IOV_{DD} – 0.2			V
V_{OL}	SDO, low-level output voltage	SDO load current = 0.2 mA			0.4	V
	$\overline{FAULT}$, low-level output voltage	$\overline{FAULT}$ load current = 10 mA			0.4	V
	Output pin capacitance			5		pF

7.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and all typical specifications at T_A = 25°C, AV_{DD} = 4.5 V to 41.5 V, AV_{SS} = –21.5 V to 0 V, DV_{DD} = 5.0 V, internal reference enabled, IOV_{DD} = 1.7 V, $V_{SENSENX}$ = 0 V, C_{COMPX} floating, DAC outputs unloaded, and digital inputs at IOV_{DD} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER REQUIREMENTS						
AI_{DD}	AV_{DD} supply current(5)	Normal mode, internal reference			8	mA
		Normal mode, external reference			7	mA
		Power-down mode			10	µA
DI_{DD}	DV_{DD} supply current(5)	Digital interface static			8	mA
AI_{SS}	AV_{SS} supply current(5)	Normal mode, internal reference	–8			mA
		Normal mode, external reference	–7			mA
		Power-down mode	–10			µA
I_{IOVDD}	IOV_{DD} supply current(5)	SCLK toggling at 1 MHz			100	µA

(1) End point fit between codes. 16-bit: 512 to 65024 for AV_{DD} ≥ 5.5 V, 512 to 63488 for AV_{DD} ≤ 5.5 V, 0.2-V headroom between V_{REFIO} and AV_{DD}; 12-bit: 32 to 4064 for AV_{DD} ≥ 5.5 V, 32 to 3968 for AV_{DD} ≤ 5.5 V, 0.2-V headroom between V_{REFIO} and AV_{DD}.
(2) Full-scale code written to the DAC for AV_{DD} ≥ 5.5 V. 16-bit: code 63488 written to the DAC for AV_{DD} ≤ 5.5 V; 12-bit: code 3968 written to the DAC for AV_{DD} ≤ 5.5 V.
(3) Temporary overload condition protection. junction temperature can be exceeded during current limit. operation above the specified maximum junction temperature may impair device reliability.
(4) Specified by design and characterization, not production tested.
(5) AV_{DD} = +15 V, AV_{SS} = –15 V, DV_{DD} = 5 V, SPI static, 10-V output span, all DAC at full scale, V_{OUTX} unloaded.

7.6 Timing Requirements: Write, IOV_{DD}: 1.7 V to 2.7 V

all specifications at T_A = –40°C to +125°C, input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of ($V_{IL} + V_{IH}$) / 2, SDO loaded with 20 pF, 1.7 V ≤ IOV_{DD} < 2.7 V

PARAMETER		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			25	MHz
$t_{SCLKHIGH}$	SCLK high time	20			ns
$t_{SCLKLOW}$	SCLK low time	20			ns
t_{SDIS}	SDIN setup	10			ns
t_{SDIH}	SDIN hold	10			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup	30			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	10			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time	50			ns
$t_{DACWAIT}$	Sequential DAC update wait time	2.4			µs
$t_{BCASTWAIT}$	Broadcast DAC update wait time	4			µs
t_{LDACAL}	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge	80			ns
t_{LDACW}	$\overline{\text{LDAC}}$ low time	20			ns
t_{CLRW}	$\overline{\text{CLR}}$ low time	20			ns
t_{RSTW}	$\overline{\text{RST}}$ low time	20			ns

7.7 Timing Requirements: Write, IOV_{DD}: 2.7 V to 5.5 V

all specifications at T_A = –40°C to +125°C, input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of ($V_{IL} + V_{IH}$) / 2, SDO loaded with 20 pF, 2.7 V ≤ IOV_{DD} ≤ 5.5 V

PARAMETER		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			50	MHz
$t_{SCLKHIGH}$	SCLK high time	10			ns
$t_{SCLKLOW}$	SCLK low time	10			ns
t_{SDIS}	SDIN setup	5			ns
t_{SDIH}	SDIN hold	5			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup	15			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	5			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time	25			ns
$t_{DACWAIT}$	Sequential DAC update wait time	2.4			µs
$t_{BCASTWAIT}$	Broadcast DAC update wait time	4			µs
t_{LDACAL}	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge	40			ns
t_{LDACW}	$\overline{\text{LDAC}}$ low time	20			ns
t_{CLRW}	$\overline{\text{CLR}}$ low time	20			ns
t_{RSTW}	$\overline{\text{RST}}$ low time	20			ns

7.8 Timing Requirements: Read and Daisy Chain, FSDO = 0, IOV_{DD}: 1.7 V to 2.7 V

all specifications at T_A = –40°C to +125°C, input signals are specified with t_R = t_F = 1 ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2, SDO loaded with 20 pF, 1.7 V ≤ IOV_{DD} < 2.7 V

PARAMETER		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			12.5	MHz
$t_{SCLKHIGH}$	SCLK high time	33			ns
$t_{SCLKLOW}$	SCLK low time	33			ns
t_{SDIS}	SDIN setup	10			ns
t_{SDIH}	SDIN hold	10			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup	30			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	10			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time	50			ns
t_{SDOZ}	SDO driven to tri-state mode	0		30	ns
t_{SDODLY}	SDO output delay from SCLK rising edge	0		30	ns

7.9 Timing Requirements: Read and Daisy Chain, FSDO = 1, IOV_{DD}: 1.7 V to 2.7 V

all specifications at T_A = –40°C to +125°C, input signals are specified with t_R = t_F = 1 ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2, SDO loaded with 20 pF, 1.7 V ≤ IOV_{DD} < 2.7 V

PARAMETER		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			25	MHz
$t_{SCLKHIGH}$	SCLK high time	20			ns
$t_{SCLKLOW}$	SCLK low time	20			ns
t_{SDIS}	SDIN setup	10			ns
t_{SDIH}	SDIN hold	10			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup	30			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	10			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time	50			ns
t_{SDOZ}	SDO driven to tri-state mode	0		30	ns
t_{SDODLY}	SDO output delay from SCLK rising edge	0		30	ns

7.10 Timing Requirements: Read and Daisy Chain, FSDO = 0, IOV_{DD}: 2.7 V to 5.5 V

all specifications at T_A = –40°C to +125°C, input signals are specified with t_R = t_F = 1 ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2, SDO loaded with 20 pF, 2.7 V ≤ IOV_{DD} ≤ 5.5 V

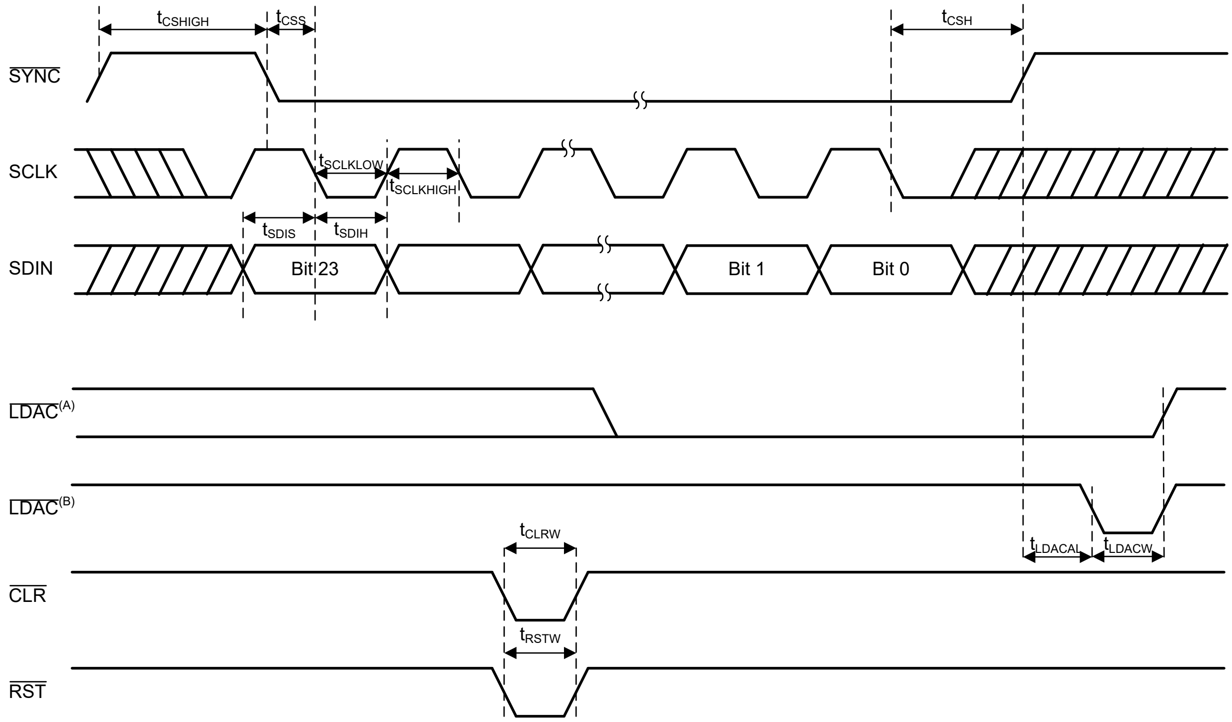
PARAMETER		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			20	MHz
$t_{SCLKHIGH}$	SCLK high time	25			ns
$t_{SCLKLOW}$	SCLK low time	25			ns
t_{SDIS}	SDIN setup	5			ns
t_{SDIH}	SDIN hold	5			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup	20			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	5			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	25			ns
t_{SDOZ}	SDO driven to tri-state mode	0		20	ns
t_{SDODLY}	SDO output delay from SCLK rising edge	0		20	ns

7.11 Timing Requirements: Read and Daisy Chain, FSDO = 1, IOV_{DD}: 2.7 V to 5.5 V

all specifications at T_A = –40°C to +125°C, input signals are specified with t_R = t_F = 1 ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2, SDO loaded with 20 pF, 2.7 V ≤ IOV_{DD} ≤ 5.5 V

PARAMETER		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			35	MHz
$t_{SCLKHIGH}$	SCLK high time	14			ns
$t_{SCLKLOW}$	SCLK low time	14			ns
t_{SDIS}	SDIN setup	5			ns
t_{SDIH}	SDIN hold	5			ns
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup	20			ns
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge	5			ns
t_{CSHIGH}	$\overline{SYNC}$ high time	25			ns
t_{SDOZ}	SDO driven to tri-state mode	0		20	ns
t_{SDODLY}	SDO output delay from SCLK rising edge	0		20	ns

7.12 Timing Diagrams



A. Asynchronous update.
B. Synchronous update.

Figure 7-1. Serial Interface Write Timing Diagram

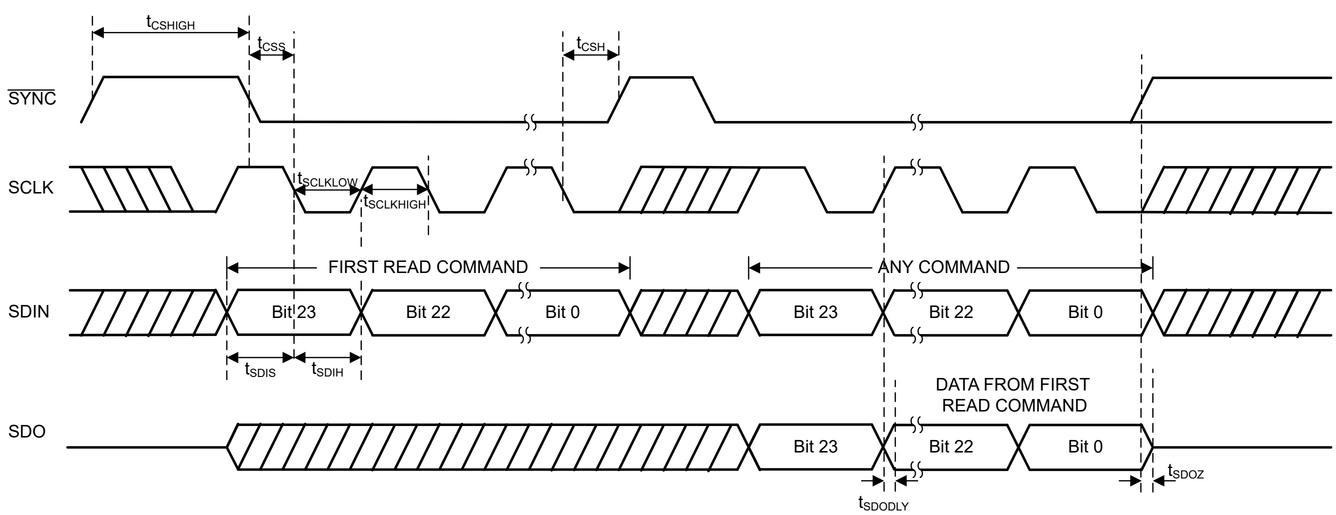


Figure 7-2. Serial Interface Read Timing Diagram

7.13 Typical Characteristics

at T_A = 25°C, DV_{DD} = 5.0 V, IOV_{DD} = 1.8 V, internal reference enabled, unipolar ranges: AV_{SS} = 0 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

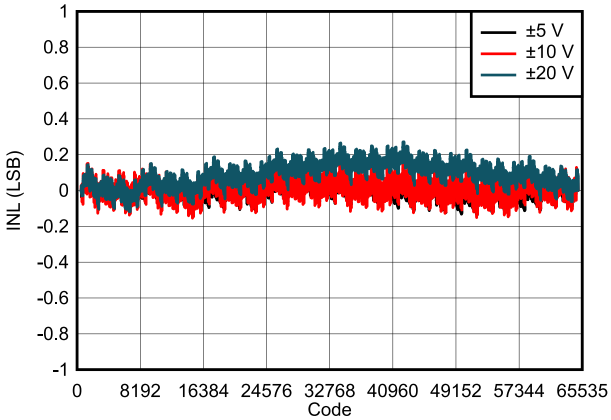


Figure 7-3. DAC81402 INL vs Digital Input Code (Bipolar Outputs)

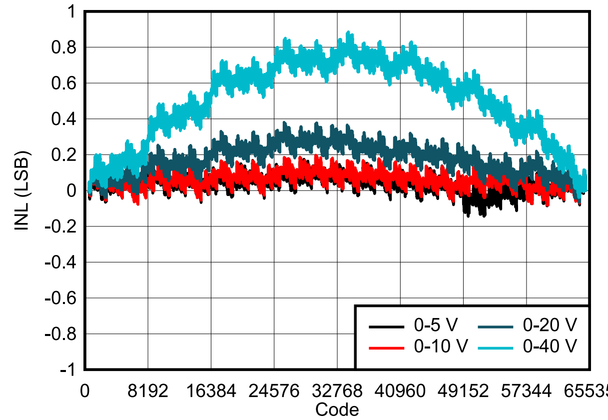


Figure 7-4. DAC81402 INL vs Digital Input Code (Unipolar Outputs)

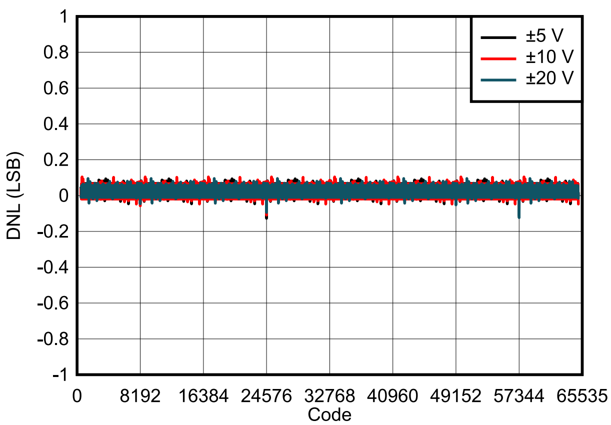


Figure 7-5. DAC81402 DNL vs Digital Input Code (Bipolar Outputs)

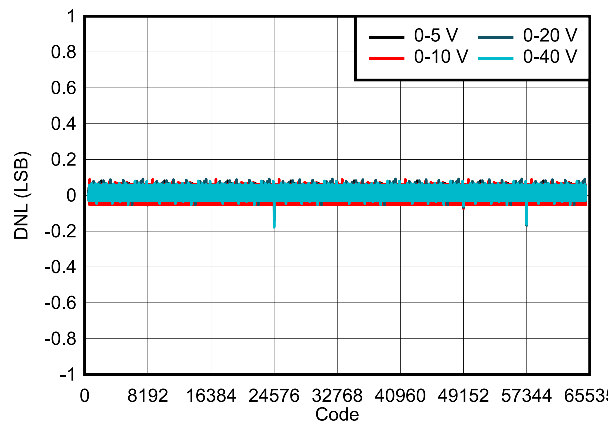


Figure 7-6. DAC81402 DNL vs Digital Input Code (Unipolar Outputs)

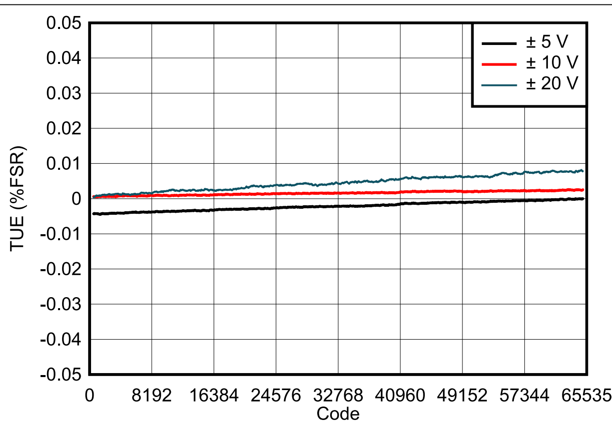


Figure 7-7. DAC81402 TUE vs Digital Input Code (Bipolar Outputs)

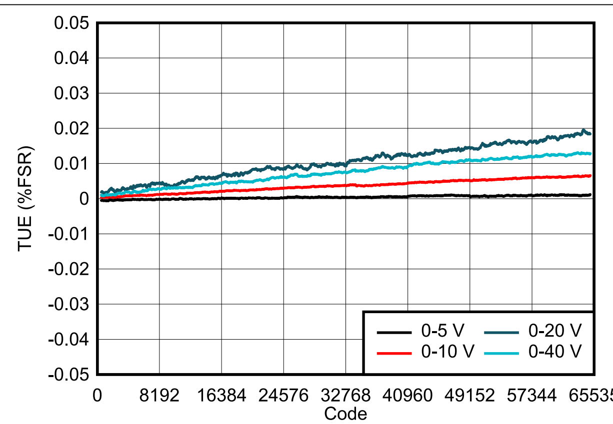


Figure 7-8. DAC81402 TUE vs Digital Input Code (Unipolar Outputs)

7.13 Typical Characteristics (continued)

at T_A = 25°C, DV_{DD} = 5.0 V, IOV_{DD} = 1.8 V, internal reference enabled, unipolar ranges: AV_{SS} = 0 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

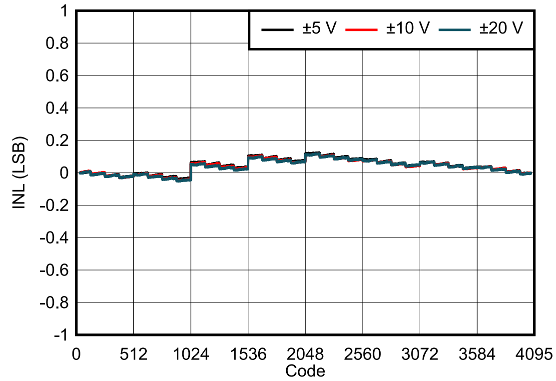


Figure 7-9. DAC61402 INL vs Digital Input Code (Bipolar Outputs)

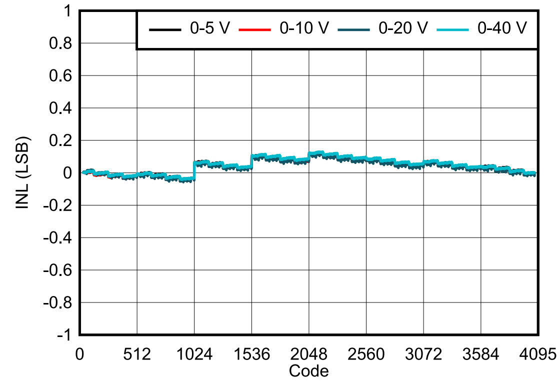


Figure 7-10. DAC61402 INL vs Digital Input Code (Unipolar Outputs)

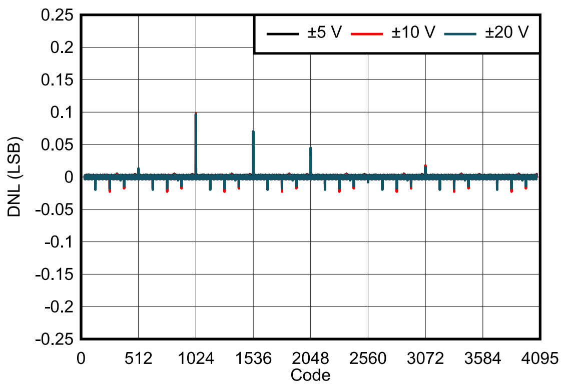


Figure 7-11. DAC61402 DNL vs Digital Input Code (Bipolar Outputs)

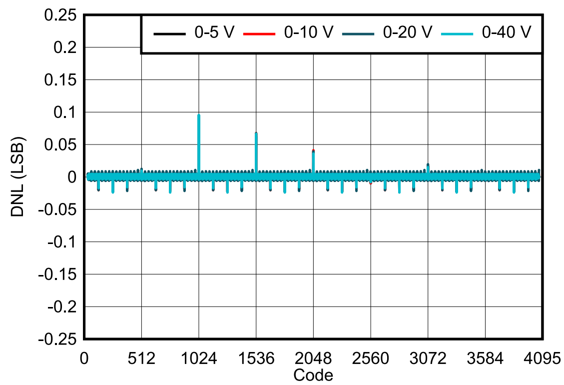


Figure 7-12. DAC61402 DNL vs Digital Input Code (Unipolar Outputs)

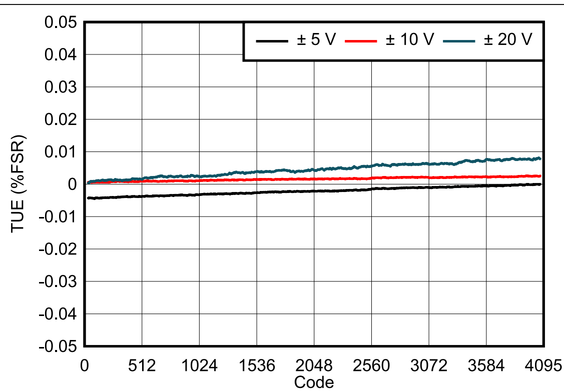


Figure 7-13. DAC61402 TUE vs Digital Input Code (Bipolar Outputs)

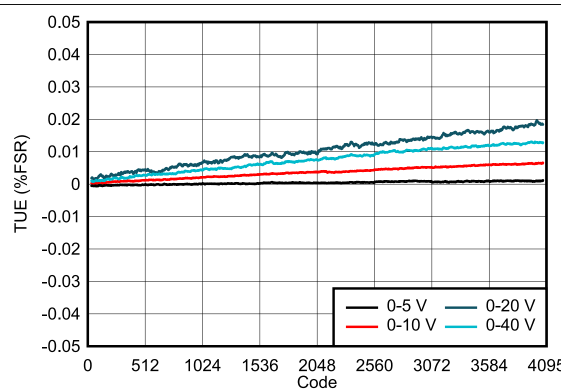


Figure 7-14. DAC61402 TUE vs Digital Input Code (Unipolar Outputs)

7.13 Typical Characteristics (continued)

at T_A = 25°C, DV_{DD} = 5.0 V, IOV_{DD} = 1.8 V, internal reference enabled, unipolar ranges: AV_{SS} = 0 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

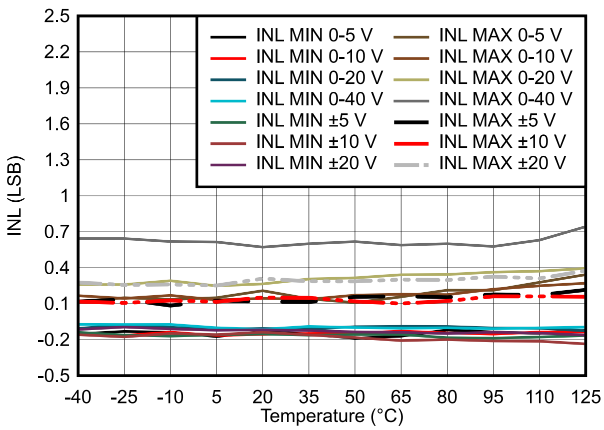


Figure 7-15. DAC81402 INL vs Temperature

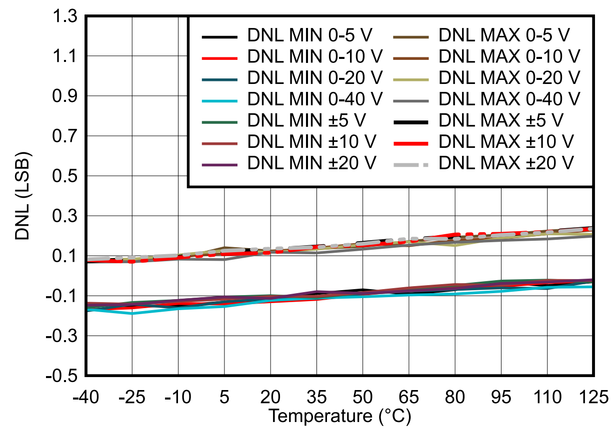


Figure 7-16. DAC81402 DNL vs Temperature

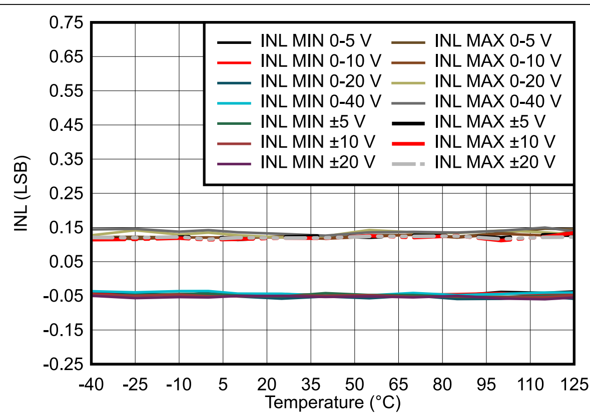


Figure 7-17. DAC61402 INL vs Temperature

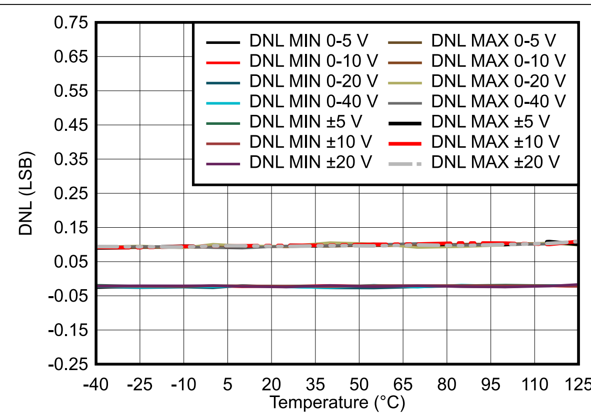


Figure 7-18. DAC61402 DNL vs Temperature

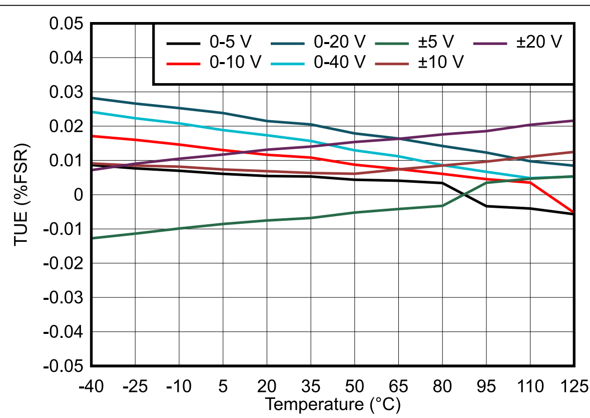


Figure 7-19. TUE vs Temperature

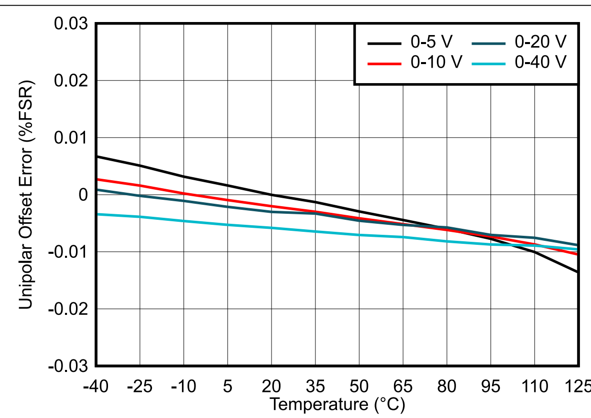


Figure 7-20. Unipolar Offset Error vs Temperature

7.13 Typical Characteristics (continued)

at T_A = 25°C, DV_{DD} = 5.0 V, IOV_{DD} = 1.8 V, internal reference enabled, unipolar ranges: AV_{SS} = 0 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

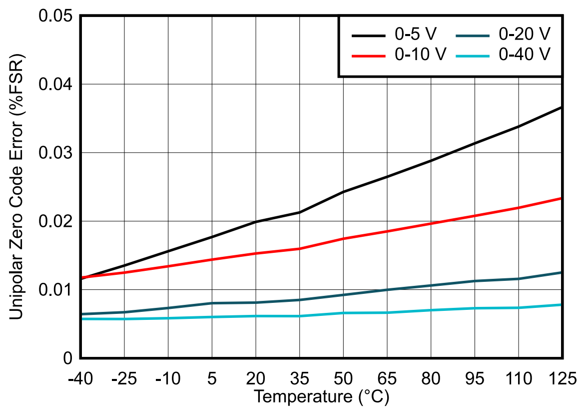


Figure 7-21. Unipolar Zero Code Error vs Temperature

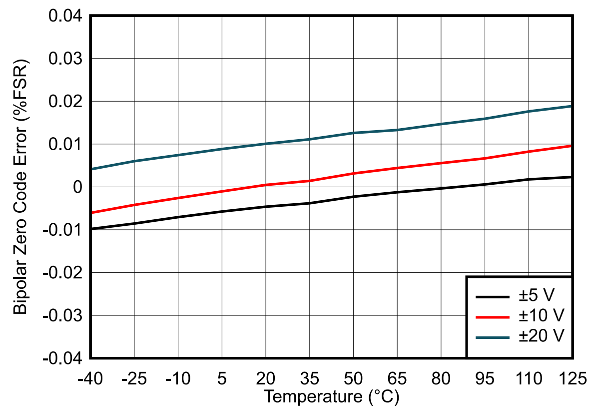


Figure 7-22. Bipolar Zero Code Error vs Temperature

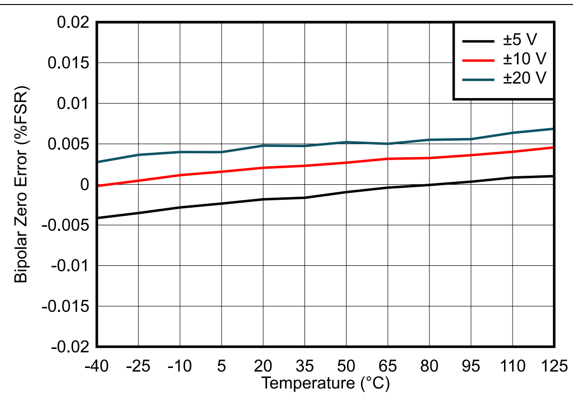


Figure 7-23. Bipolar Zero Error vs Temperature

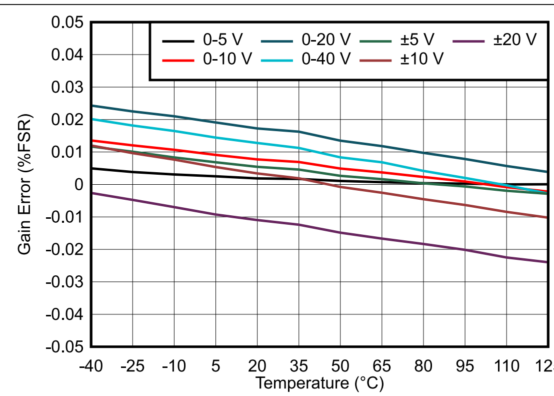


Figure 7-24. Gain Error vs Temperature

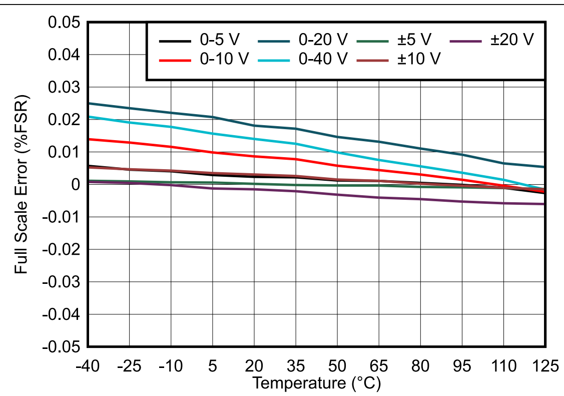


Figure 7-25. Full-Scale Error vs Temperature

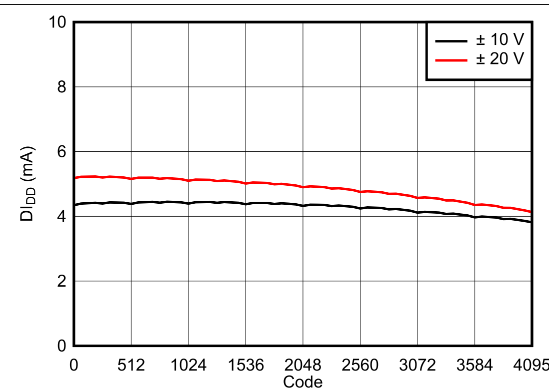


Figure 7-26. Supply Current (DI_{DD}) vs Digital Input Code

7.13 Typical Characteristics (continued)

at T_A = 25°C, DV_{DD} = 5.0 V, IOV_{DD} = 1.8 V, internal reference enabled, unipolar ranges: AV_{SS} = 0 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

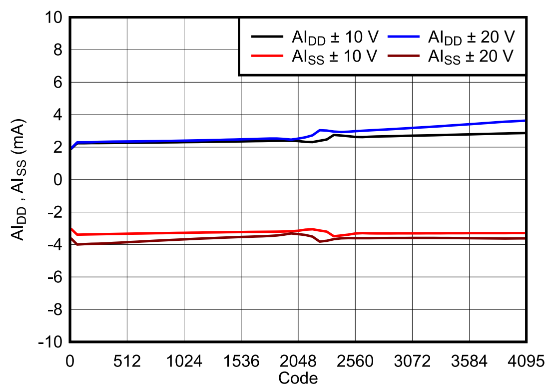


Figure 7-27. Supply Current (AI_{DD}, AI_{SS}) vs Digital Input Code

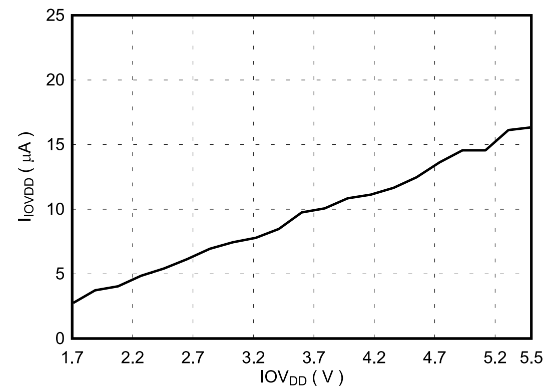
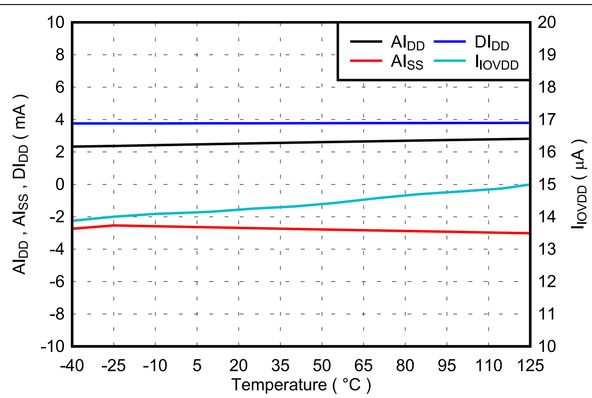
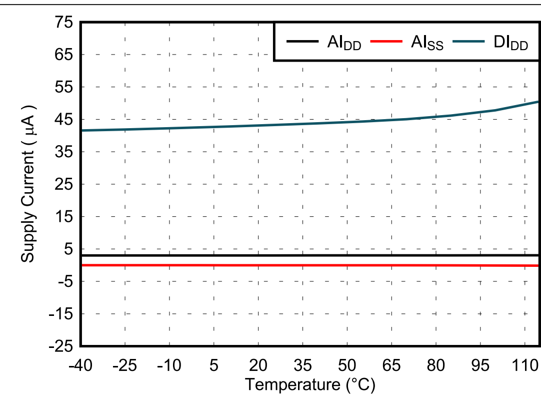


Figure 7-28. Supply Current (I_{IOVDD}) vs Supply Voltage



DAC range: ±20 V

Figure 7-29. Supply Current vs Temperature



DAC range: ±20 V

Figure 7-30. Power-Down Current vs Temperature

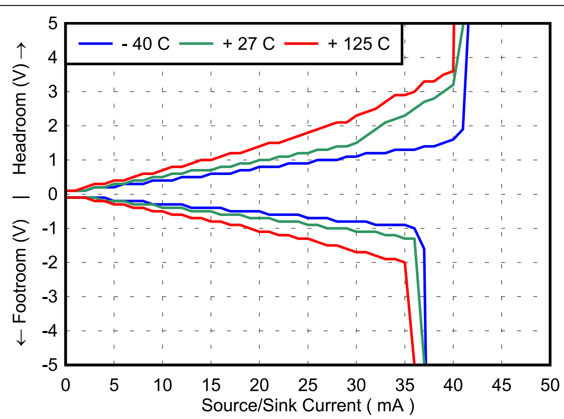


Figure 7-31. Headroom and Footroom from Supply vs Output Current

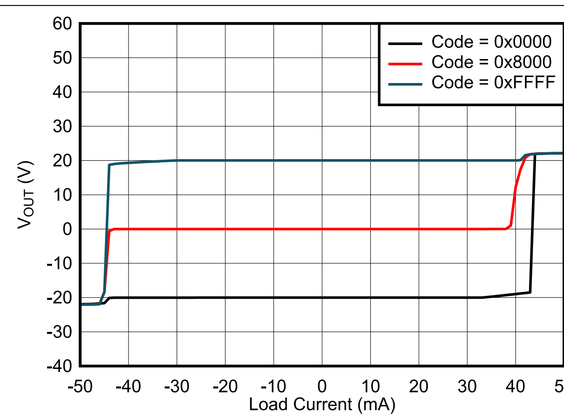
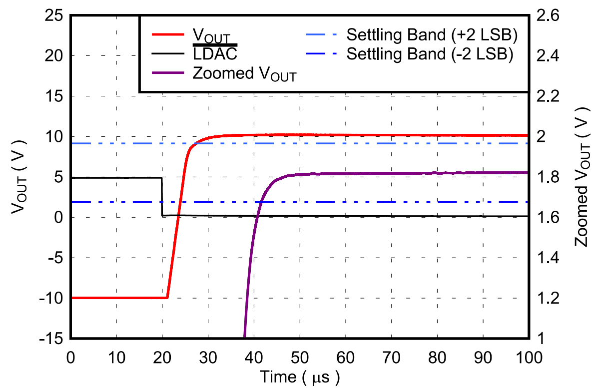


Figure 7-32. Source and Sink Capability

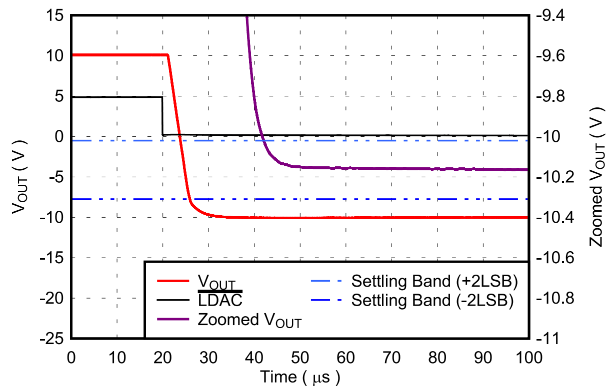
7.13 Typical Characteristics (continued)

at T_A = 25°C, DV_{DD} = 5.0 V, IOV_{DD} = 1.8 V, internal reference enabled, unipolar ranges: AV_{SS} = 0 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)



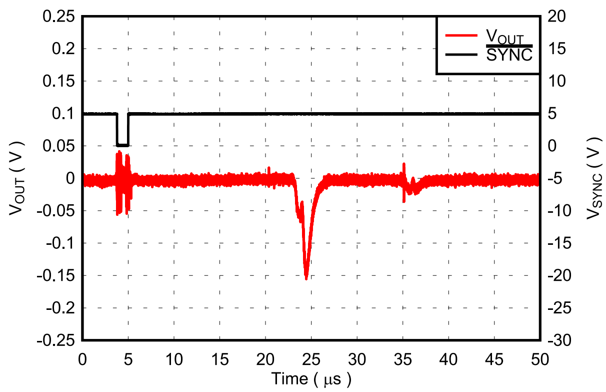
DAC range: ±10 V

Figure 7-33. Full-Scale Settling Time, Rising Edge



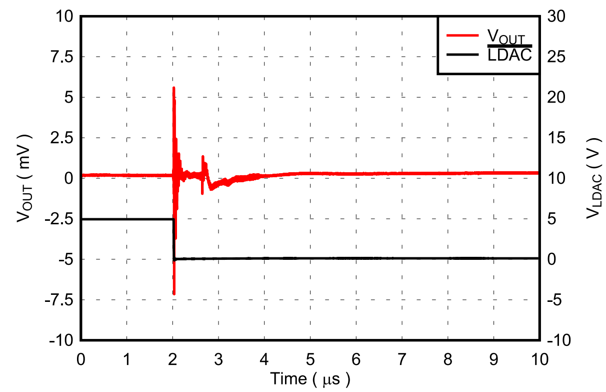
DAC range: ±10 V

Figure 7-34. Full-Scale Settling Time, Falling Edge



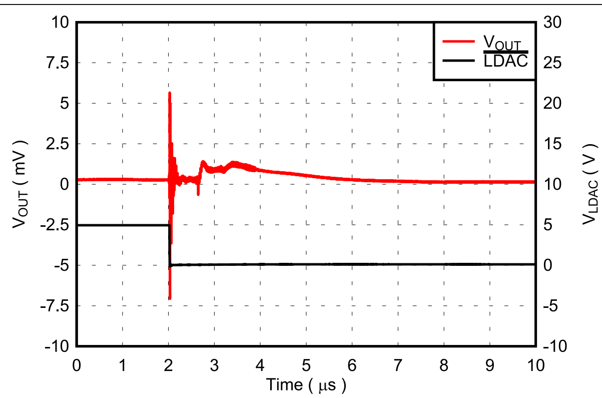
DAC range: ±20 V

Figure 7-35. DAC Output Enable Glitch



DAC range: ±10 V

Figure 7-36. Glitch Impulse, 1 LSB Step, Rising Edge



DAC range: ±10 V

Figure 7-37. Glitch Impulse, 1 LSB Step, Falling Edge

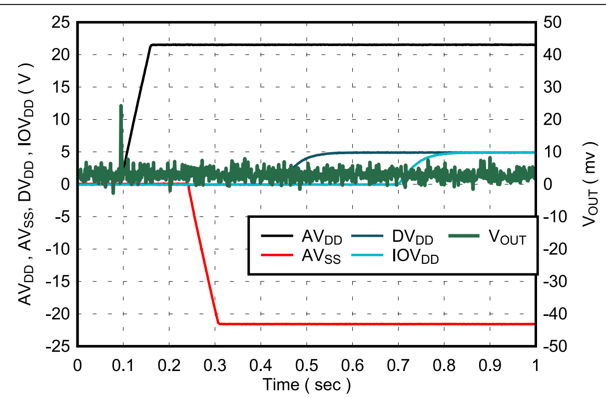


Figure 7-38. Power-Up Response

7.13 Typical Characteristics (continued)

at T_A = 25°C, DV_{DD} = 5.0 V, IOV_{DD} = 1.8 V, internal reference enabled, unipolar ranges: AV_{SS} = 0 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

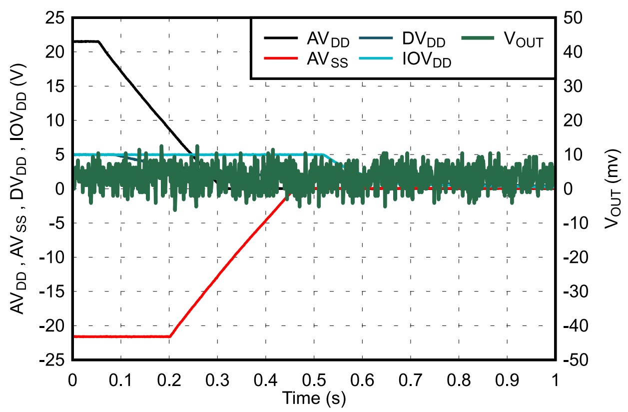
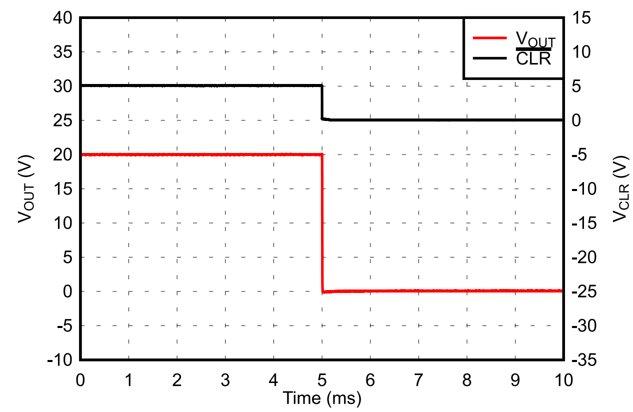
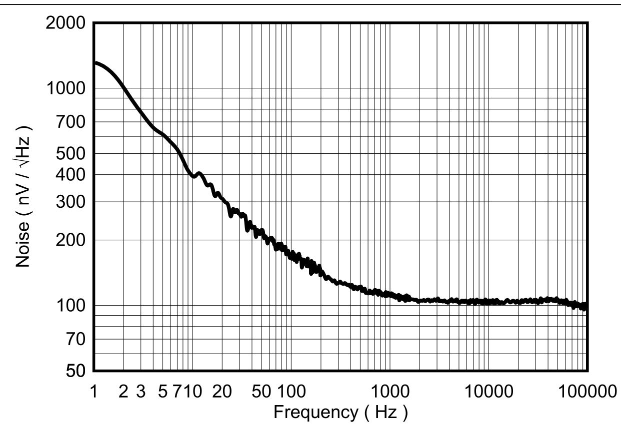


Figure 7-39. Power-Down Response



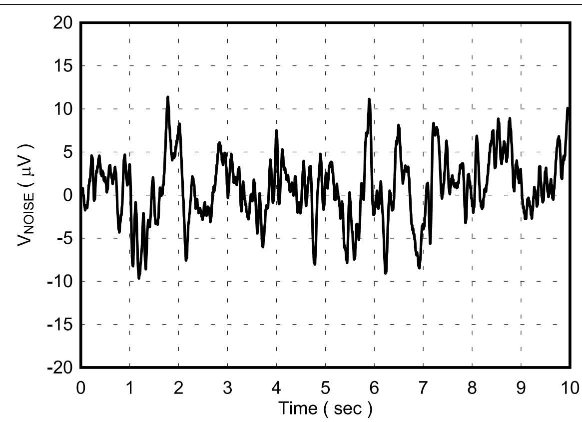
DAC range: ±20 V

Figure 7-40. Clear Command Response



DAC range: 0 V to 5 V, midscale code

Figure 7-41. DAC Output Noise Density vs Frequency



DAC range: 0 V to 5 V, midscale code

Figure 7-42. DAC Output Noise

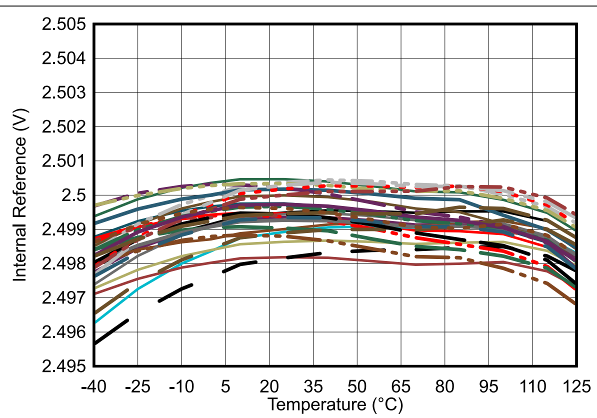


Figure 7-43. Internal Reference Voltage vs Temperature

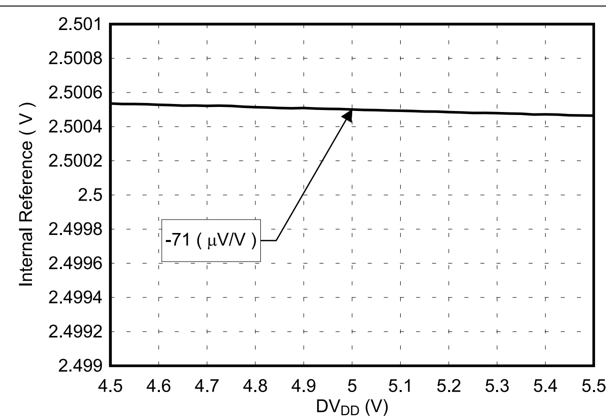


Figure 7-44. Internal Reference Voltage vs Supply Voltage

7.13 Typical Characteristics (continued)

at T_A = 25°C, DV_{DD} = 5.0 V, IOV_{DD} = 1.8 V, internal reference enabled, unipolar ranges: AV_{SS} = 0 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $AV_{SS} \leq V_{MIN}$ − 1.5 V and $AV_{DD} \geq V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

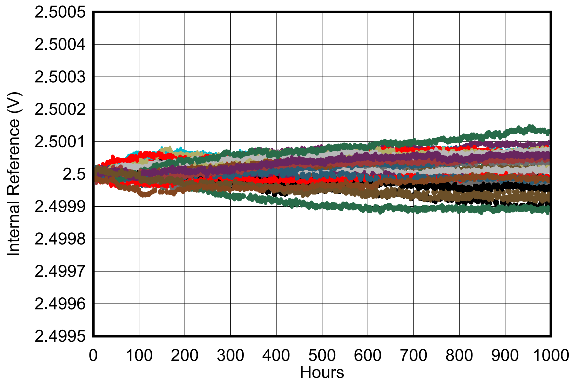


Figure 7-45. Internal Reference Voltage vs Time

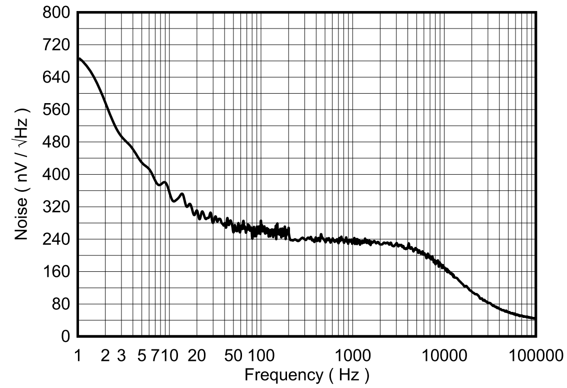


Figure 7-46. Internal Reference Noise Density vs Frequency

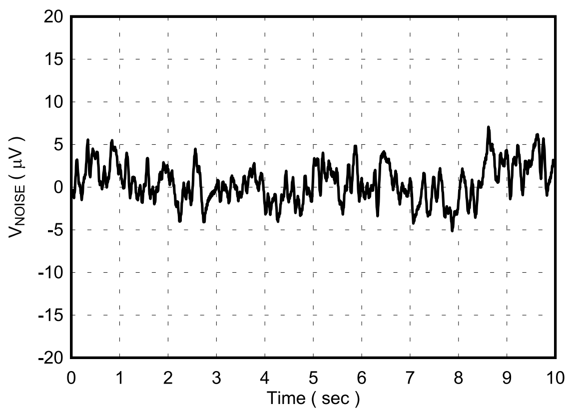


Figure 7-47. Internal Reference Noise

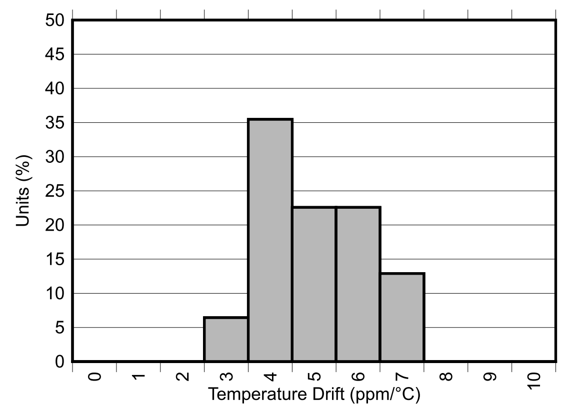


Figure 7-48. Internal Reference Temperature Drift Histogram

8 Detailed Description

8.1 Overview

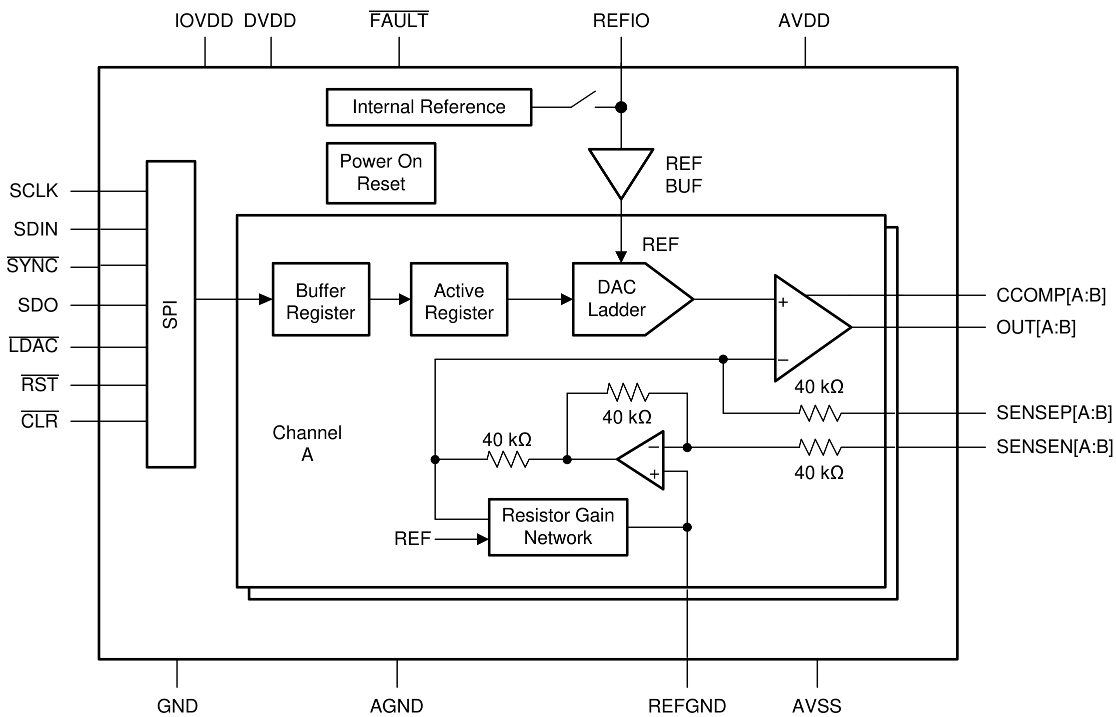
The 16-bit DAC81402 and 12-bit DAC61402 (DACx1402) are pin-compatible, dual-channel, high-voltage-output digital-to-analog converters (DACs). The DACx1402 consist of an R-2R based ladder followed by an output buffer. These devices also include a precision reference and a reference buffer. The R-2R-based ladder is production trimmed to provide monotonicity and a linearity of ±1 LSB. The devices are also optimized to reduce the code-to-code change glitch to less than 2 nV-s.

The DACx1402 output amplifier provides bipolar voltage outputs up to ±20 V, and unipolar voltage outputs up to 40 V. Each output channel includes sense pins that eliminate the IR drop across load connections and sense a difference of up to ±12 V between the load and DAC grounds. Alternatively, the sense pins can also be used for output offset adjustment. An external capacitor compensation pin is also provided to stabilize the output amplifier for high capacitive loads.

Communication to the DACx1402 is performed through a 4-wire serial interface that supports stand-alone and daisy-chain operation. An optional frame-error check provides added robustness to the device serial interface.

The DACx1402 incorporate a power-on-reset circuit that connects the DAC outputs to ground at power up. The outputs remain in this mode until the device is properly configured for operation. The devices include additional reliability features such as short-circuit protection and a thermal alarm.

8.2 Functional Block Diagram



8.3 Feature Description

Each output channel in the device consists of an R-2R ladder digital-to-analog converter (DAC) with dedicated reference and ground buffers, and an output buffer amplifier capable of rail-to-rail operation. The device also includes an internal 2.5-V reference. Figure 8-1 shows a simplified diagram of the device architecture.

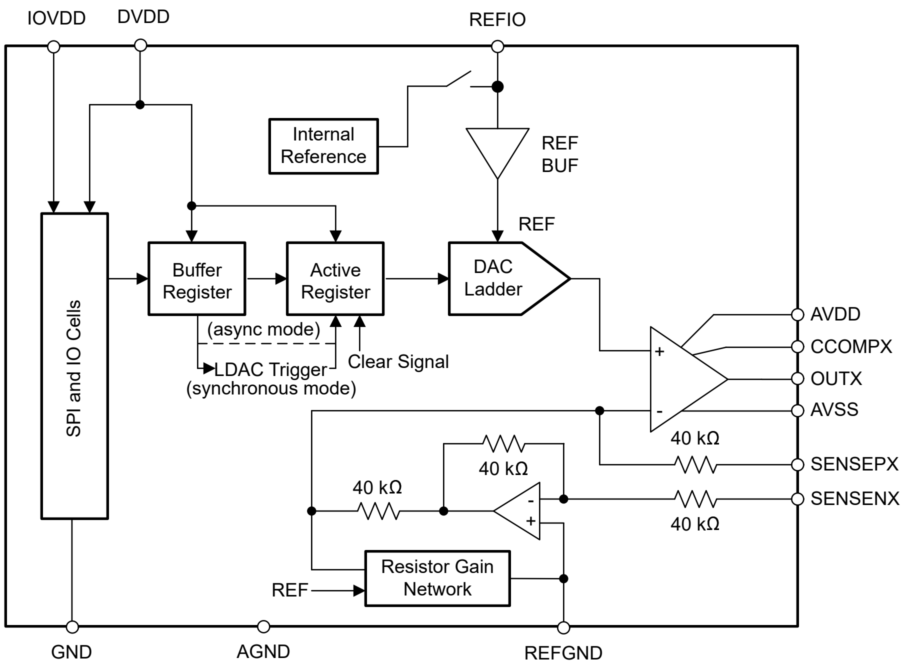


Figure 8-1. Device Architecture

8.3.1 R-2R Ladder DAC

The DAC architecture consists of a voltage-output, segmented, R-2R ladder as shown in Figure 8-2. The device incorporates a dedicated reference buffer per output channel that provides constant input impedance with code at the REFIO pin. The output of the reference buffers drives the R-2R ladders. A production trim process provides excellent linearity and low glitch.

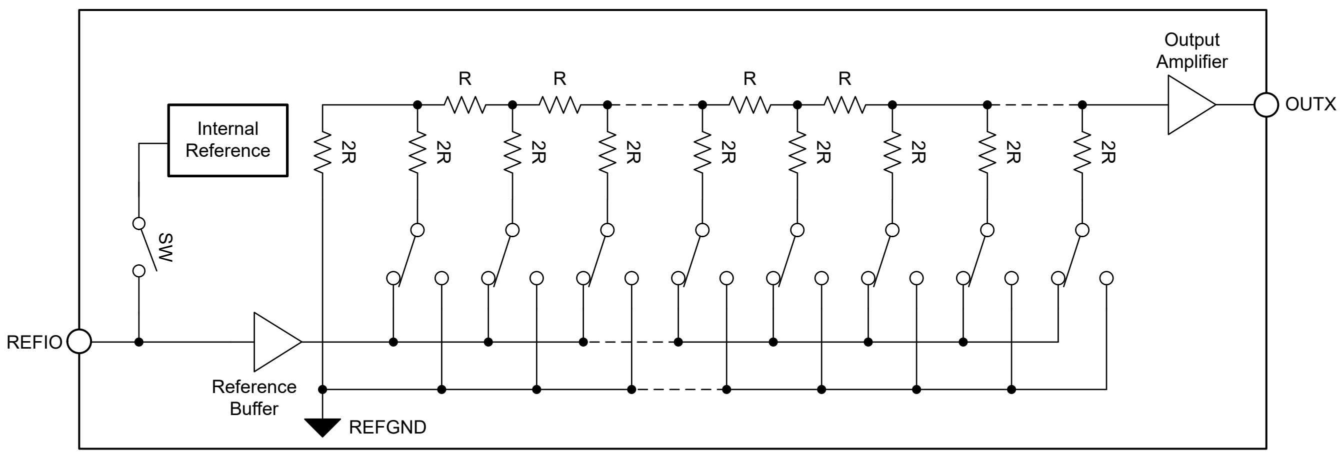


Figure 8-2. R-2R Ladder

8.3.2 Programmable-Gain Output Buffer

The voltage output stage as conceptualized in Figure 8-3 provides the voltage output according to the DAC code and the output range setting.

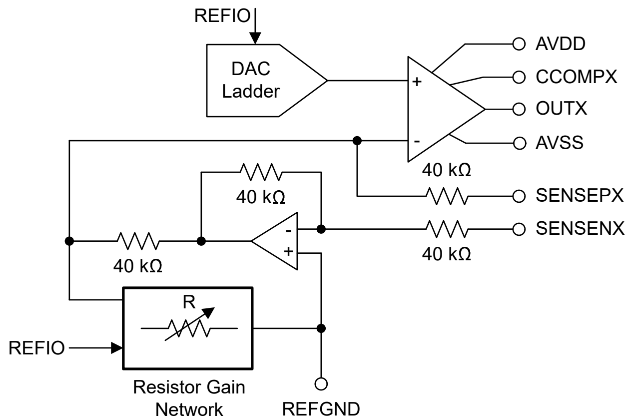


Figure 8-3. Voltage Output Buffer

For unipolar output mode, the output range can be programmed as:

- 0 V to 5 V
- 0 V to 10 V
- 0 V to 20 V
- 0 V to 40 V

For bipolar output mode, the output reange can be programmed as:

- ±5 V
- ±10 V
- ±20 V

In addition, 20% overrange is available on all ranges except for 0 V to 40 V and ±20 V.

The input data are written to the individual DAC data registers in straight-binary format for all output ranges. The output voltage (V_{OUTX}) can be expressed as Equation 1 and Equation 2.

For unipolar output mode

$$V_{OUTX} = V_{REFIO} \times GAIN \times \frac{CODE}{2^N} \quad (1)$$

For bipolar output mode

$$V_{OUTX} = V_{REFIO} \times GAIN \times \frac{CODE}{2^N} - GAIN \times \frac{V_{REFIO}}{2} \quad (2)$$

where:

- CODE is the decimal equivalent of the binary code loaded to the DAC data register.
- N is the DAC resolution in bits.
- V_{REFIO} is the reference voltage (internal or external).
- GAIN is the gain factor assigned to each output voltage output range as shown in Table 8-1.

Table 8-1. Voltage Output Range vs Gain Setting

MODE	VOLTAGE OUTPUT RANGE	GAIN
Unipolar	5 V	2.0
	6 V (20% overrange)	2.4
	10 V	4.0
	12 V (20% overrange)	4.8
	20 V	8.0
	24 V (20% overrange)	9.6
	40 V	16.0
Bipolar	±5 V	4.0
	±6 V (20% overrange)	4.8
	±10 V	8.0
	±12 V (20% overrange)	9.6
	±20 V	16.0

The output amplifiers can drive up to ±15 mA with 1.5-V supply headroom while maintaining the specified TUE specification for the device. The output stage has short-circuit current protection that limits the output current to 40 mA. The device is able to drive capacitive loads up to 1 µF. For loads greater than 2 nF, an external compensation capacitor must be connected between the CCOMPx and OUTx pins to keep the output voltage stable, but at the expense of reduced bandwidth and increased settling time.

8.3.2.1 Sense Pins

The SENSEPx pins are provided to enable sensing of the load by connecting to points electrically closer to the load. This configuration allows the internal output amplifier to make sure that the correct voltage is applied across the load, as long as headroom is available on the power supply. The SENSEPx pins are used to correct for resistive drops on the system board, and are connected to V_{OUTX} at the pins. In some cases, both V_{OUTX} and $V_{SENSEPX}$ are brought out through separate lines and connected remotely together at the load. In such cases, if the $V_{SENSEPX}$ line is cut, then the amplifier loop is broken; use a 5-kΩ resistor between the OUTx and SENSEPx pins to maintain proper amplifier operation.

The SENSENx pins are provided as remote ground sense reference outputs from the internal V_{OUTX} amplifier. The output swing of the V_{OUTX} amplifier is relative to the voltage seen at these pins. The voltage difference between $V_{SENSENX}$ and the device ground must be lower than ±12 V.

At device start up, the power-on-reset circuit makes sure that all registers are at default values. The voltage output buffer is in a Hi-Z state; however, the SENSEPx pins connect to the amplifier inputs through an internal 40-kΩ feedback resistor (Figure 8-3). If the OUTx and SENSEPx pins are connected together, the OUTx pins are also connected to the same node through the feedback resistor. This node is protected by internal circuitry and settles to a value between GND and the reference input.

8.3.3 DAC Register Structure

Data written to the DAC data registers is initially stored in the DAC buffer registers. The transfer of data from the DAC buffer registers to the active registers can be configured to occur immediately (asynchronous mode) or be initiated by a DAC trigger signal (synchronous mode). After the active registers are updated, the DAC outputs change to the new values.

After a power-on or reset event, all DAC registers set to zero code, the DAC output amplifiers power down, and the DAC outputs connect to ground.

8.3.3.1 DAC Output Update

The DAC double-buffered architecture enables data updates without disturbing the analog outputs. Data updates can be performed either in synchronous or asynchronous mode. The device offers both software and hardware data update control.

The update mode for each DAC channel is determined by the status of the corresponding SYNC-EN bit. In both update modes, a minimum wait time of 2.4 µs is required between DAC output updates.

8.3.3.1.1 Synchronous Update

In synchronous mode, writing to the DAC data register does not automatically update the DAC output. Instead the update occurs only after a trigger event. A DAC trigger signal is generated eigher through the SOFT-LDAC bit or by the $\overline{\text{LDAC}}$ pin. The synchronous update mode enables simultaneous update of multiple DAC outputs.

8.3.3.1.2 Asynchronous Update

In asynchronous mode, a DAC data register write results in an immediate update of the DAC active register and DAC output on a $\overline{\text{SYNC}}$ rising edge.

8.3.3.2 Broadcast DAC Register

The DAC broadcast register enables a simultaneous update of multiple DAC outputs with the same value with a single register write.

Each DAC channel can be configured to update or remain unaffected by a broadcast command by setting the corresponding DAC-BRDCAST-EN bit. A register write to the BRDCAST-DATA register forces those DAC channels that have been configured for broadcast operation to update their DAC buffer registers to this value. The DAC outputs update to the broadcast value according to their synchronous mode configuration.

8.3.3.3 Clear DAC Operation

The DAC outputs are set in clear mode either through the $\overline{\text{CLR}}$ pin or the SOFT-CLR bit. In clear mode, each DAC data register is set to either zero code (if configured for unipolar range operation) or midscale code (if set for bipolar range operation). A clear command forces all DAC channels to clear the contents of their buffer and active registers to the clear code regardless of their synchronization setting.

8.3.4 Internal Reference

The device includes a precision 2.5-V band-gap reference with a maximum temperature drift of 10 ppm/°C. The internal reference is in power-down mode by default.

The internal reference voltage is available at the REFIO pin and can source up to 5 mA. To filter noise, place a minimum 150-nF capacitor between the reference output and ground.

External reference operation is also supported. The external reference is applied to the REFIO pin. If using an external reference, power down the internal reference.

8.3.5 Power-On Reset (POR)

The device incorporates a power-on-reset function. After the supplies reach their minimum specified values, a POR event is issued. Additionally, a POR event can be initiated by the $\overline{\text{RST}}$ pin or a SOFT-RESET command.

A POR event causes all registers to initialize to default values, and communication with the device is valid only after a 1 ms POR delay. After a POR event, the device is set to power-down mode, where all DAC channels and internal reference are powered down and the DAC outputs are connected to ground through a 10-kΩ internal resistor.

8.3.5.1 Hardware Reset

A device hardware reset event is initiated by a minimum 20-ns logic low on the $\overline{\text{RST}}$ pin.

8.3.5.2 Software Reset

The device implements a software reset feature. A device software reset is initiated by writing reserved code 0x1010 to SOFT-RESET in the TRIGGER register. The software reset command is triggered on the $\overline{\text{SYNC}}$ rising edge of the instruction.

8.3.6 Thermal Alarm

The device incorporates a thermal shutdown that is triggered when the die temperature exceeds 140°C. A thermal shutdown sets the TEMP-ALM bit, and causes all DAC outputs to power-down; however, the internal reference remains powered on. The $\overline{\text{FAULT}}$ pin can be configured to monitor a thermal shutdown condition by setting the TEMPALM-EN bit. After a thermal shutdown is triggered, the device stays in shutdown even after the device temperature lowers.

The die temperature must fall to less than 140°C before the device can be returned to normal operation. To resume normal operation, the thermal alarm must be cleared through the ALM-RESET bit while the DAC channels are in power-down mode.

8.4 Device Functional Modes

8.4.1 Power-Down Mode

The device output amplifiers and internal reference power-down status can be individually configured and monitored though the PWDWN registers. Setting a DAC channel in power-down mode disables the output amplifier and clamps the output pin to ground through an internal 10-kΩ resistor.

The DAC data registers are not cleared when the DAC goes into power-down mode. Therefore, upon return to normal operation, the DAC output voltages return to the same respective voltages prior to the device entering power-down mode. The DAC data registers can be updated while in power-down mode, which allows for changing the power-on voltage, if required.

After a power-on or reset event, all the DAC channels and the internal reference are in power-down mode. The entire device can be configured into power-down or active modes through the DEV-PWDWN bit.

8.5 Programming

The device is controlled through an SPI-compatible, flexible, four-wire, serial interface. The interface provides access to the device registers, and can be configured to daisy-chain multiple devices for write operations. The device incorporates an optional error-checking mode to validate SPI data communication integrity in noisy environments.

8.5.1 Stand-Alone Operation

A serial interface access cycle is initiated by asserting the $\overline{\text{SYNC}}$ pin low. The serial clock, SCLK, can be a continuous or gated clock. SDIN data are clocked on SCLK falling edges. A regular serial interface access cycle is 24 bits long with error checking disabled and 32 bits long with error checking enabled. Therefore, the $\overline{\text{SYNC}}$ pin must stay low for at least 24 or 32 SCLK falling edges. The access cycle ends when the $\overline{\text{SYNC}}$ pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. If the access cycle contains more than the minimum clock edges, only the first 24 or 32 bits are used by the device. When $\overline{\text{SYNC}}$ is high, the SCLK and SDIN signals are blocked, and SDO is in a Hi-Z state.

Table 8-2 describes the format for an error-checking-disabled access cycle (24-bits long). The first byte input to SDIN is the instruction cycle. The instruction cycle identifies the request as a read or write command and the 6-bit address that is to be accessed. The last 16 bits in the cycle form the data cycle.

Table 8-2. Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
23	RW	Identifies the communication as a read or write command to the address register: R/W = 0 sets a write operation. R/W = 1 sets a read operation
22	x	Don't care bit
21-16	A[5:0]	Register address — specifies the register to be accessed during the read or write operation
15-0	DI[15:0]	Data cycle bits: If a write command, the data cycle bits are the values to be written to the register with address A[5:0] If a read command, the data cycle bits are don't care values

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. The output data format is shown in Table 8-3. Data are clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit.

Table 8-3. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	RW	Echo RW from previous access cycle
22	x	Echo bit 22 from previous access cycle
21-16	A[5:0]	Echo address from previous access cycle
15-0	DO[15:0]	Readback data requested on previous access cycle

8.5.2 Daisy-Chain Operation

For systems that contain several devices, the SDO pin can be used to daisy-chain the devices together. Daisy-chain operation is useful in reducing the number of serial interface lines.The SDO pin must be enabled by setting the SDO-EN bit before initiating daisy-chain operation.

The first falling edge on the $\overline{\text{SYNC}}$ pin starts the operation cycle (see Figure 8-4). If more than 24 clock pulses are applied while the $\overline{\text{SYNC}}$ pin is kept low, the data ripple out of the shift register and are clocked out on the SDO pin, either on the falling edge or rising edge of SCLK according to the FSDO bit. By connecting the SDO output of the first device to the SDIN input of the next device in the chain, a multiple-device interface is constructed.

Each device in the daisy-chain system requires 24 clock pulses. As a result the total number of clock cycles must be equal to 24 × N, where N is the total number of devices in the daisy chain. When the serial transfer to all devices is complete, the $\overline{\text{SYNC}}$ signal is taken high. This action transfers the data from the SPI shift registers to the internal register of each device in the daisy chain, and prevents any further data from being clocked into the input shift register.

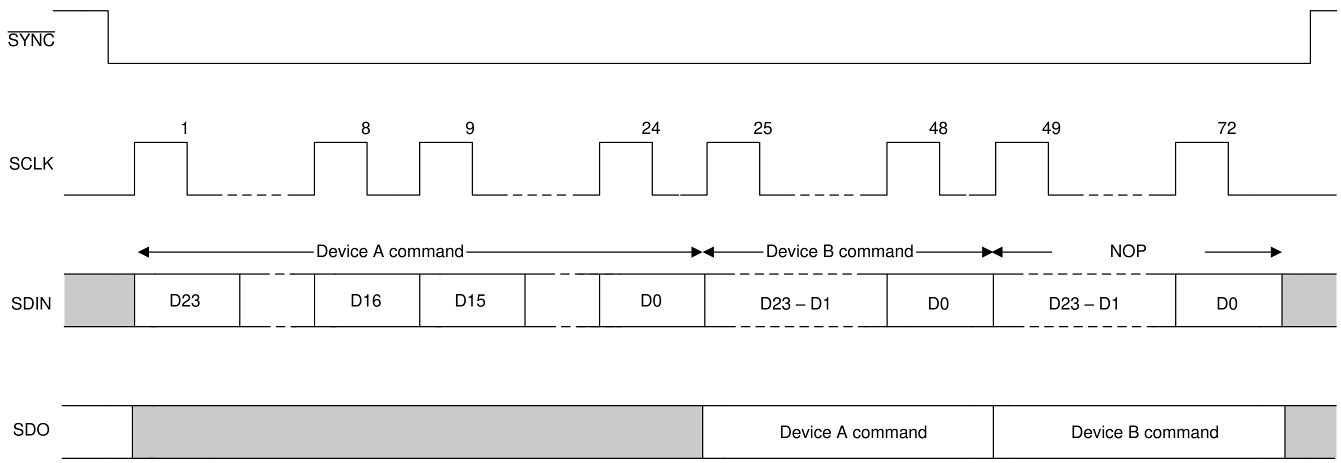


Figure 8-4. Serial Interface Daisy-Chain Write Cycle

8.5.3 Frame Error Checking

If the device is used in a noisy environment, error checking can be used to check the integrity of SPI data communication between the device and the host processor. This feature is enabled by setting the CRC-EN bit.

The error checking scheme is based on the CRC-8-ATM (HEC) polynomial: $x^8 + x^2 + x + 1$ (that is, 100000111). When error checking is enabled, the serial interface access cycle width is 32 bits. The normal 24-bit SPI data are appended with an 8-bit CRC polynomial by the host processor before feeding the data to the device. In all serial interface readback operations, the CRC polynomial is output on the SDO pin as part of the 32-bit cycle.

Table 8-4. Error Checking Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
31	RW	Identifies the communication as a read or write command to the address register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.
30	CRC-ERROR	Reserved bit. Set to zero.
29-24	A[5:0]	Register address. Specifies the register to be accessed during the read or write operation.
23-8	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[5:0]. If a read command, the data cycle bits are don't care values.
7-0	CRC	8-bit CRC polynomial.

The device decodes the 32-bit access cycle to compute the CRC remainder on $\overline{\text{SYNC}}$ rising edges. If no error exists, the CRC remainder is zero and data are accepted by the device.

A write operation failing the CRC check causes the data to be ignored by the device. After the write command, a second access cycle can be issued to determine the error checking results (CRC-ERROR bit) on the SDO pin.

If there is a CRC error, the CRC-ALM bit of the status register is set to 1. The $\overline{\text{FAULT}}$ pin can be configured to monitor a CRC error by setting the CRCALM-EN bit.

Table 8-5. Write Operation Error Checking Cycle

BIT	FIELD	DESCRIPTION
31	RW	Echo RW from previous access cycle (RW = 0).
30	CRC-ERROR	Returns a 1 when a CRC error is detected; otherwise, returns a 0.
29-24	A[5:0]	Echo address from previous access cycle.
23-8	DO[15:0]	Echo data from previous access cycle.
7-0	CRC	Calculated CRC value of bits 31:8.

A read operation must be followed by a second access cycle to get the requested data on the SDO pin. The error check result (CRC-ERROR bit) from the read command is output on the SDO pin.

As in the case of a write operation failing the CRC check, the CRC-ALM bit of the status register is set to 1, and the $\overline{\text{ALMOUT}}$ pin, if configured for CRC alerts, is set low.

Table 8-6. Read Operation Error Checking Cycle

BIT	FIELD	DESCRIPTION
31	RW	Echo RW from previous access cycle (RW = 1).
30	CRC-ERROR	Returns a 1 when a CRC error is detected; otherwise, returns a 0.
29-24	A[5:0]	Echo address from previous access cycle.
23-8	DO[15:0]	Readback data requested on previous access cycle.
7-0	CRC	Calculated CRC value of bits 31:8.

8.6 Register Map

Table 8-7 lists the memory-mapped registers for the device. All register addresses not listed should be considered as reserved locations and the register contents should not be modified.

Table 8-7. Register Map

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	NOP	W	0000	NOP[15:0]															
01	DEVICEID	R	0A70(1) or 0930(2)	DEVICEID[13:0]														VERSIONID[1:0]	
02	STATUS	R	0000	RESERVED													CRC-ALM	DAC-BUSY	TEMP-ALM
03	SPICONFIG	R/W	0AA4	RESERVED				TEMPALM-EN	DACBUSY-EN	CRCALM-EN	RESERVED			DEV-PWDWN	CRC-EN	RSVD	SDO-EN	FSDO	RSVD
04	GENCONFIG	R/W	4000	RSVD	REF-PWDWN	RESERVED													
05	BRDCONFIG	R/W	000F	RESERVED												RSVD	DACB-BRDCAST-EN	DACA-BRDCAST-EN	RSVD
06	SYNCCONFIG	R/W	0000	RESERVED												RSVD	DACB-SYNC-EN	DACA-SYNC-EN	RSVD
09	DACPWDWN	R/W	FFFF	RESERVED												RSVD	DACB-PWDWN	DACA-PWDWN	RSVD
0A	DACRANGE	W	0000	RESERVED				DACB-RANGE[3:0]				DACA-RANGE[3:0]				RESERVED			
0E	TRIGGER	R/W	0000	RESERVED						SOFT-CLR	ALM-RESET	RESERVED			SOFT-LDAC	SOFT-RESET[3:0]			
0F	BRDCAST	W	0000	BRDCAST-DATA[15:0]															
11	DACA	W	0000	DACA-DATA[15:0]															
12	DACB	W	0000	DACB-DATA[15:0]															

(1) Reset code for DAC81402.
(2) Reset code for DAC61402.

8.6.1 NOP Register (address = 00h) [reset = 0000h]

Return to Register Map.

Figure 8-5. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP[15:0]															
W-0000h															

Table 8-8. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOP[15:0]	W	0000h	No operation. Write 0000h for proper no-operation command.

8.6.2 DEVICEID Register (address = 01h) [reset = 0A70h or 0930h]

Return to Register Map.

Figure 8-6. DEVICEID Register

15	14	13	12	11	10	9	8
DEVICEID[13:6]							
R							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DEVICEID[5:0]						VERSIONID[1:0]	
R						R-0h	

Table 8-9. DEVICEID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	DEVICEID[13:0]	R	029Ch	DAC81402 device ID.
			024Ch	DAC61402 device ID.
1-0	VERSIONID[1:0]	R	0h	Version ID. Subject to change.

8.6.3 STATUS Register (address = 02h) [reset = 0000h]

Return to Register Map.

Figure 8-7. STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-00h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CRC-ALM	DAC-BUSY	TEMP-ALM
R-00h					R-0h	R-0h	R-0h

Table 8-10. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0000h	Reserved for factory use
2	CRC-ALM	R	0h	CRC-ALM = 1 indicates a CRC error.
1	DAC-BUSY	R	0h	DAC-BUSY = 1 indicates DAC registers are not ready for updates.
0	TEMP-ALM	R	0h	TEMP-ALM = 1 indicates die temperature is over 140°C. A thermal alarm event forces the DAC outputs to go into power-down mode.

8.6.4 SPICONFIG Register (address = 03h) [reset = 0AA4h]

Return to Register Map.

Figure 8-8. SPICONFIG Register

15	14	13	12	11	10	9	8
RESERVED				TEMPALM-EN	DACBUSY-EN	CRCALM-EN	RESERVED
R-0h				R/W-1h	R/W-0h	R/W-1h	R-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		DEV-PWDWN	CRC-EN	RESERVED	SDO-EN	FSDO	RESERVED
R-1h	R-0h	R/W-1h	R/W-0h	R-0h	R/W-1h	R/W-0h	R-0h

Table 8-11. SPICONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved for factory use
11	TEMPALM-EN	R/W	1h	When set to 1, a thermal alarm triggers the $\overline{\text{FAULT}}$ pin.
10	DACBUSY-EN	R/W	0h	When set to 1, the $\overline{\text{FAULT}}$ pin is set between DAC output updates. Contrary to other alarm events, this alarm resets automatically.
9	CRCALM-EN	R/W	1h	When set to 1, a CRC error triggers the $\overline{\text{FAULT}}$ pin..
8-6	RESERVED	R	2h	Reserved for factory use
5	DEV-PWDWN	R/W	1h	DEV-PWDWN = 1 sets the device in power-down mode. DEV-PWDWN = 0 sets the device in active mode.
4	CRC-EN	R/W	0h	When set to 1, frame error checking is enabled.
3	RESERVED	R	0h	Reserved for factory use
2	SDO-EN	R/W	1h	When set to 1, the SDO pin is operational.
1	FSDO	R/W	0h	Fast SDO bit (half-cycle speedup). When 0, SDO updates on SCLK rising edges. When 1, SDO updates on SCLK falling edges.
0	RESERVED	R	0h	Reserved for factory use

8.6.5 GENCONFIG Register (address = 04h) [reset = 4000h]

Return to Register Map.

Figure 8-9. GENCONFIG Register

15	14	13	12	11	10	9	8
RESERVED	REF-PWDWN	RESERVED					
R-0h	R/W-1h	R-00h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-00h							

Table 8-12. GENCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved for factory use
14	REF-PWDWN	R/W	1h	REF-PWDWN = 1 powers down the internal reference. REF-PWDWN = 0 activates the internal reference.
13-0	RESERVED	R	0000h	Reserved for factory use

8.6.6 BRDCONFIG Register (address = 05h) [reset = 000Fh]

Return to Register Map.

Figure 8-10. BRDCONFIG Register

15	14	13	12	11	10	9	8
RESERVED							
R-00h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED	DACB-BRDCAST-EN	DACA-BRDCAST-EN	RESERVED
R-0h				R-1h	R/W-1h	R/W-1h	R-1h

Table 8-13. BRDCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	000h	Reserved for factory use
3	RESERVED	R	1h	Reserved for factory use
2	DACB-BRDCAST-EN	R/W	1h	When set to 1, the corresponding DAC is set to update the output to the value set in the BDCAST register. When cleared to 0, the corresponding DAC output remains unaffected by a BRDCAST command.
1	DACA-BRDCAST-EN	R/W	1h	
0	RESERVED	R	1h	Reserved for factory use

8.6.7 SYNCCONFIG Register (address = 06h) [reset = 0000h]

Return to Register Map.

Figure 8-11. SYNCCONFIG Register

15	14	13	12	11	10	9	8
RESERVED							
R-00h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED	DACB-SYNC-EN	DACA-SYNC-EN	RESERVED
R-0h				R-0h	R/W-0h	R/W-0h	R-0h

Table 8-14. SYNCCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	000h	Reserved for factory use
3	RESERVED	R	0h	Reserved for factory use
2	DACB_SYNC_EN	R/W	0h	When set to 1, the corresponding DAC is set to update in response to an LDAC trigger (synchronous mode). When cleared to 0, the corresponding DAC output is set to update immediately on $\overline{SYNC}$ rising edge (asynchronous mode).
1	DACA_SYNC_EN	R/W	0h	
0	RESERVED	R	0h	Reserved for factory use

8.6.8 DACPWDWN Register (address = 09h) [reset = FFFFh]

Return to Register Map.

Figure 8-12. DACPWDWN Register

15	14	13	12	11	10	9	8
RESERVED							
R-FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RESERVED	DACB-PWDWN	DACA-PWDWN	RESERVED
R-Fh				R-1h	R/W-1h	R/W-1h	R-1h

Table 8-15. DACPWDWN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	FFFh	Reserved for factory use
3	RESERVED	R	1h	Reserved for factory use
2	DACB-PWDWN	R/W	1h	When set to 1, the corresponding DAC is in power-down mode, and the output is connected to ground through a 10-kΩ internal resistor.
1	DACA-PWDWN	R/W	1h	
0	RESERVED	R	1h	Reserved for factory use

8.6.9 DACRANGE Register (address = 0Ah) [reset = 0000h]

Return to Register Map.

Figure 8-13. DACRANGE Register

15	14	13	12	11	10	9	8
RESERVED				DACB-RANGE[3:0]			
W-0h				W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DACA-RANGE[3:0]				RESERVED			
W-0h				W-0h			

Table 8-16. DACRANGE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	W	0h	Reserved for factory use
11-8	DACB-RANGE[3:0]	W	0h	Sets the output range for the corresponding DAC. 0000: 0 V to 5 V 1000: 0 V to 6 V 0001: 0 V to 10 V 1001: 0 V to 12 V 0010: 0 V to 20 V 1010: 0 V to 24 V 0011: 0 V to 40 V 0101: –5 V to +5 V 1101: –6 V to +6 V 0110: –10 V to +10 V 1110: –12 V to +12 V 0111: –20 V to +20 V All others: invalid
7-4	DACA-RANGE[3:0]	W	0h	
3-0	RESERVED	W	0h	Reserved for factory use

8.6.10 TRIGGER Register (address = 0Eh) [reset = 0000h]

Return to Register Map.

Figure 8-14. TRIGGER Register

15	14	13	12	11	10	9	8
RESERVED						SOFT-CLR	ALM-RESET
W-00h						W-0h	W-0h
7	6	5	4	3	2	1	0
RESERVED			SOFT-LDAC	SOFT-RESET[3:0]			
W-0h			W-0h	W-0h			

Table 8-17. TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	W	00h	Reserved for factory use
9	SOFT-CLR	W	0h	Set this bit to 1 to clear all DAC outputs.
8	ALM-RESET	W	0h	Set this bit to 1 to clear an alarm event. Not applicable for a DAC-BUSY alarm event.
7-5	RESERVED	W	0h	Reserved for factory use
4	SOFT-LDAC	W	0h	Set this bit to 1 to synchronously load the DACs that have been set in synchronous mode in the SYNCCONFIG register.
3-0	SOFT_RESET[3:0]	W	0h	Set these bits to reserved code 1010 to reset the device to the default state.

8.6.11 BRDCAST Register (address = 0Fh) [reset = 0000h]

Return to Register Map.

Figure 8-15. BRDCAST Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRDCAST-DATA[15:0]															
W-0000h															

Table 8-18. BRDCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	BRDCAST_DATA[15:0]	W	0000h	Writing to the BRDCAST register forces the DAC channels that have been set to broadcast in the BRDCONFIG register to update the data register data to BRDCAST-DATA. Data are MSB aligned in straight-binary format: DAC81402: { DATA[15:0] } DAC61402: { DATA[11:0], x, x, x, x } x − Don't care bits

8.6.12 DACn Register (address = 11h to 12h) [reset = 0000h]

Return to Register Map.

Figure 8-16. DACn Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DACn-DATA[15:0]															
W-0000h															

Table 8-19. DACn Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DACn-DATA[15:0]	W	0000h	Stores the data to be loaded to DACn in MSB-aligned, straight-binary format: DAC81402: { DATA[15:0] } DAC61402: { DATA[11:0], x, x, x, x } x − Don't care bits

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The primary applications for the device include motor-drive circuits in industrial environments, and programmable power supplies commonly used in automated test equipment and laboratory power supplies. In these applications, high precision and programmable voltage ranges are important considerations. The excellent device linearity of ±1 LSB INL and inherently monotonic design meets the criteria for these applications.

9.2 Typical Application

In industrial automation and process control applications, voltage and current analog output signals are used to operate control sources such as motors, solenoids and valve based actuators. The DAC provides a voltage output which is then used by control modules to drive industrial motors. Standard analog output ranges provided by these programmable logic control (PLC) systems include: 5 V, 10 V, ± 5 V and ± 12 V.

The end application and user requirements determine the appropriate output range, so software programmability of the output range is a desirable function in many system designs. Furthermore force-sense of the output voltage, capacitive load stability even with long cables at the DAC outputs, and smaller packages which enable multi-channel systems, are all important factors in these applications. Motor drive applications require a high precision voltage output to precisely control the motor movements in factory automations. Figure 9-1 illustrates a simple voltage output module driving motors in an industrial CNC control application

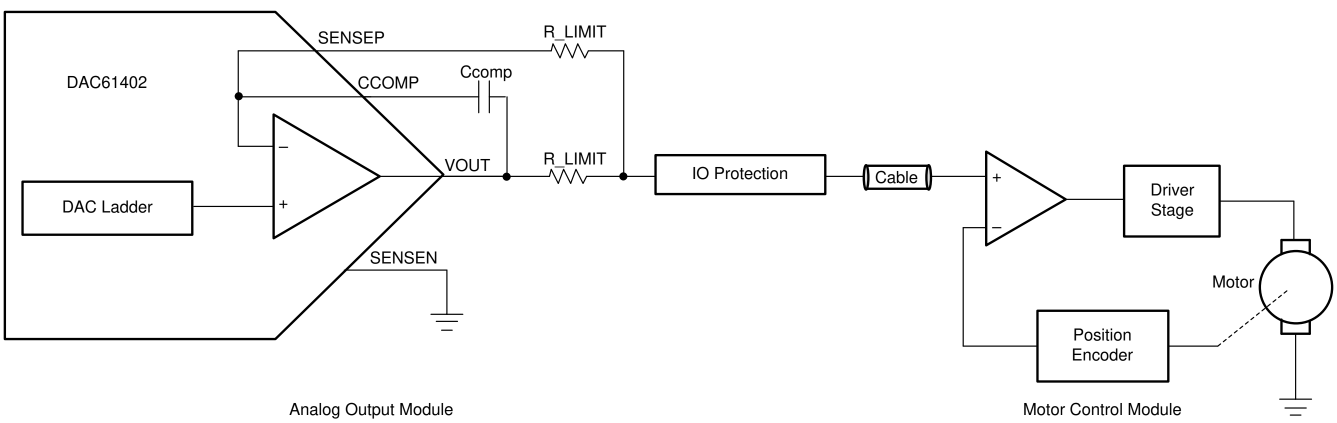


Figure 9-1. Motor Drive Circuit

9.2.1 Design Requirements

- Voltage range: 0 to 5 V, 0 to 10 V, 0 to 40 V, and ± 20 V
- Capacitive load: 1 µF
- Bipolar supply voltage: AV_{DD} = 21 V, AV_{SS} = −21 V
- Unipolar supply voltage: AV_{DD} = 41.5 V, AV_{SS} = 0 V
- EOS protection: Required

9.2.2 Detailed Design Procedure

The DACx1402 are an excellent choice for this application because of their exceptional linearity and programmable output ranges which simplify the drive stage design. Since the maximum output voltage requirements is ±20 V, the AV_{DD} and AV_{SS} supplies should be set to 21 V and −21 V, respectively. In unipolar output range, the AV_{DD} supply should be set to 41 V for a full-scale output voltage of 40 V. In unipolar designs, the AV_{SS} supply can be tied to ground. In all cases, the supply voltages must be selected such that the AV_{DD} − AV_{SS} voltage does not exceed 41.5 V.

The analog output module design includes an external electrical overstress protection circuit for short circuit events. R_LIMIT sets the maximum current flowing into the device in the event of an electrical overstress condition. The design uses a compensation capacitor for driving large cables such as the ones found in industrial environments. A C_{COMP} value of 470 pF is sufficient to drive capacitive loads as large as 1 µF.

Figure 9-2 shows a simplified structure of the device output pins, represented as a pair of clamp-to-rail diodes connected to the AV_{DD} and AV_{SS} supply rails.

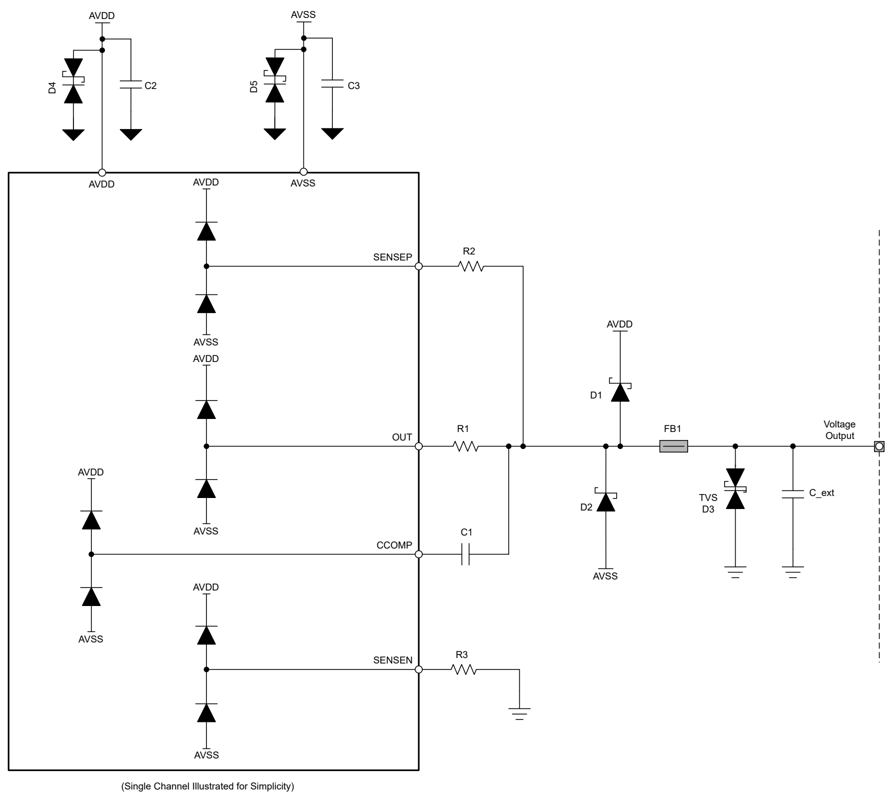


Figure 9-2. Electrical Overstress (EOS) Protection Scheme

If the device output pins are exposed to industrial transient testing without external protection components, the diode structures will become forward biased and conduct current. If the conducted current is large, as is common in high-voltage industrial transient tests, the structures will become permanently damaged and impact the device functionality.

Both attenuation and diversion strategies are implemented to protect the device. Attenuation is realized by the capacitor C_{ext} which forms an RC low-pass filter when interacting with the source impedance of the transient generator. The ferrite bead FB1 also helps attenuate high-frequency currents, along with both AC and DC current limiters realized by the series pass elements R1, R2, and R3.

Diversion is achieved by the transient voltage suppressor (TVS) diode D3 and clamp-to-rail diodes D1 and D2. The combined effects of both strategies effectively limits the current flowing into the device internal diode structures to prevent permanent damage. If we assume the schottky diode clamps V_{OUT} to ±1.5 V from rail, then the peak current entering the device is equal to 80 mA, assuming R1 = 10 Ω and the diode FB is 0.7 V. It is important to also include the TVS diodes D4 and D5 at the AVDD and AVSS nodes in order to provide a discharge path for the energy sent to these nodes through diodes D4, D5, and the internal diode structures. In the abscensce of these diodes when current is diverted to these nodes decoupling capacitors will charge, slowly increasing the voltage at these nodes which can exceed the threshold limits of AVDD and AVSS.

9.2.3 Application Curves

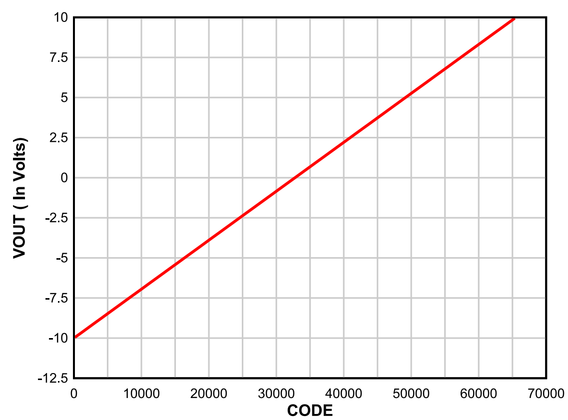


Figure 9-3. Output Voltage vs DAC Code Sweep

10 Power Supply Recommendations

The device requires four power-supply inputs: IOVDD, DVDD, AVDD, and AVSS. A 0.1-μF ceramic capacitor must be connected close to each power-supply pin. In addition, a 4.7-μF or 10-μF bulk capacitor is recommended for each power supply. Tantalum or aluminum types can be chosen for the bulk capacitors.

There is no sequencing requirement for the power supplies. The DAC output range is configurable; therefore, sufficient power-supply headroom is required to achieve linearity at codes close to the power-supply rails. When sourcing or sinking current from or to the DAC output, make sure to account for the effects of power dissipation on the temperature of the device, and ensure the device does not exceed the maximum junction temperature.

11 Layout

11.1 Layout Guidelines

Printed circuit board (PCB) layout plays a significant role in achieving desired ac and dc performance from the device. The device has a pinout that supports easy splitting of the noisy and quiet grounds. The digital and analog signals are available on separate sides of the package for easy layout. Figure 11-1 shows an example layout where the different ground planes have been clearly demarcated, as well as the best position for the single-point shorts between the planes.

For best power-supply bypassing, place the bypass capacitors close to the respective power-supply pins. Provide unbroken ground reference planes for the digital signal traces, especially for the SPI and $\overline{\text{LDAC}}$ signals. The $\overline{\text{RST}}$ and $\overline{\text{FAULT}}$ signals are static lines; therefore these lines can lie on the analog side of the ground plane.

11.2 Layout Example

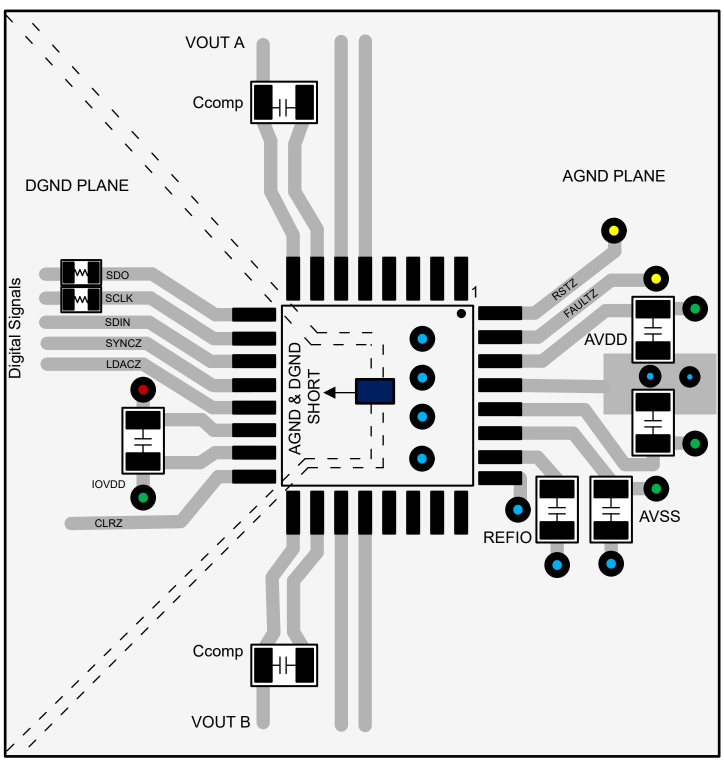


Figure 11-1. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *BP-DAC81404EVM, BP-DAC61402EVM* user's guide

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC61402RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D61402	Samples
DAC61402RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D61402	Samples
DAC81402RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D81402	Samples
DAC81402RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D81402	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

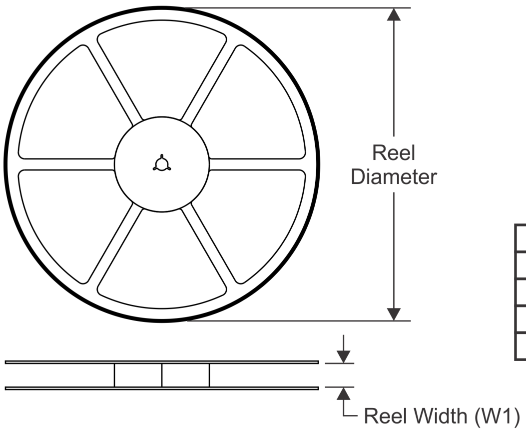
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

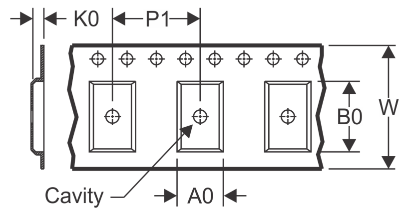
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

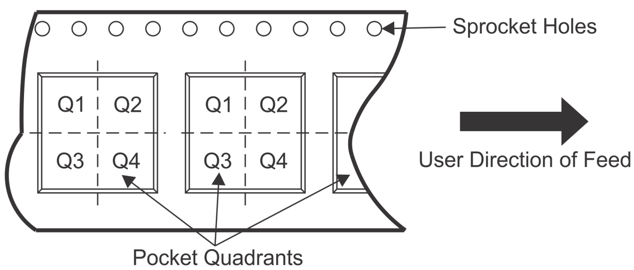


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

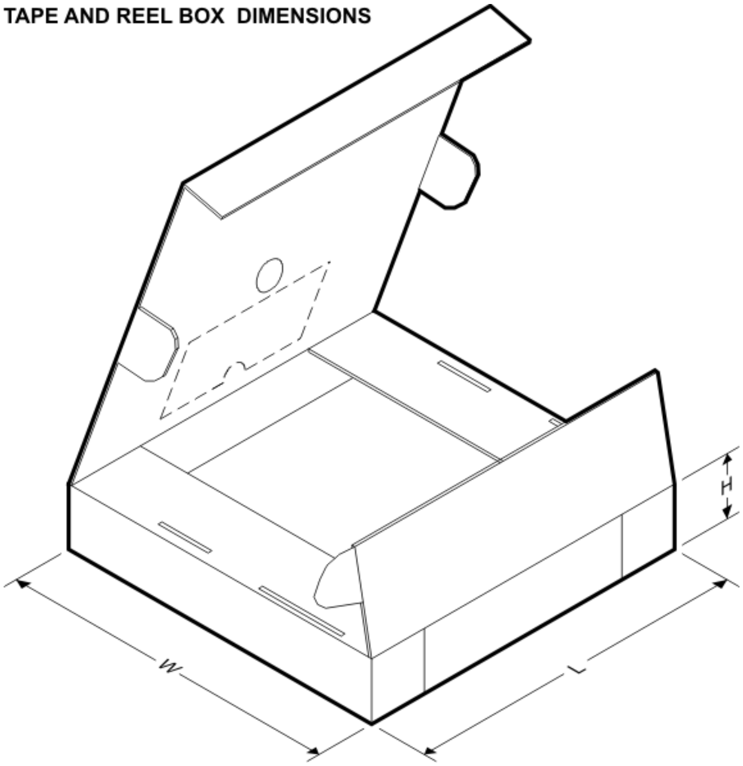
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC61402RHBR	VQFN	RHB	32	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
DAC61402RHBT	VQFN	RHB	32	250	180.0	12.5	5.25	5.25	1.1	8.0	12.0	Q2
DAC81402RHBR	VQFN	RHB	32	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
DAC81402RHBT	VQFN	RHB	32	250	180.0	12.5	5.25	5.25	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

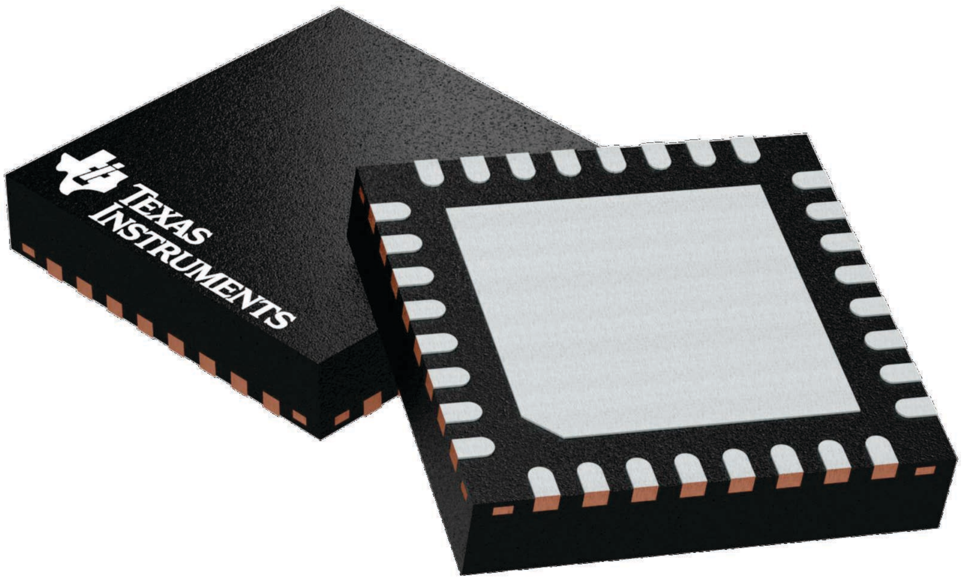
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC61402RHBR	VQFN	RHB	32	3000	338.0	355.0	50.0
DAC61402RHBT	VQFN	RHB	32	250	205.0	200.0	33.0
DAC81402RHBR	VQFN	RHB	32	3000	338.0	355.0	50.0
DAC81402RHBT	VQFN	RHB	32	250	205.0	200.0	33.0

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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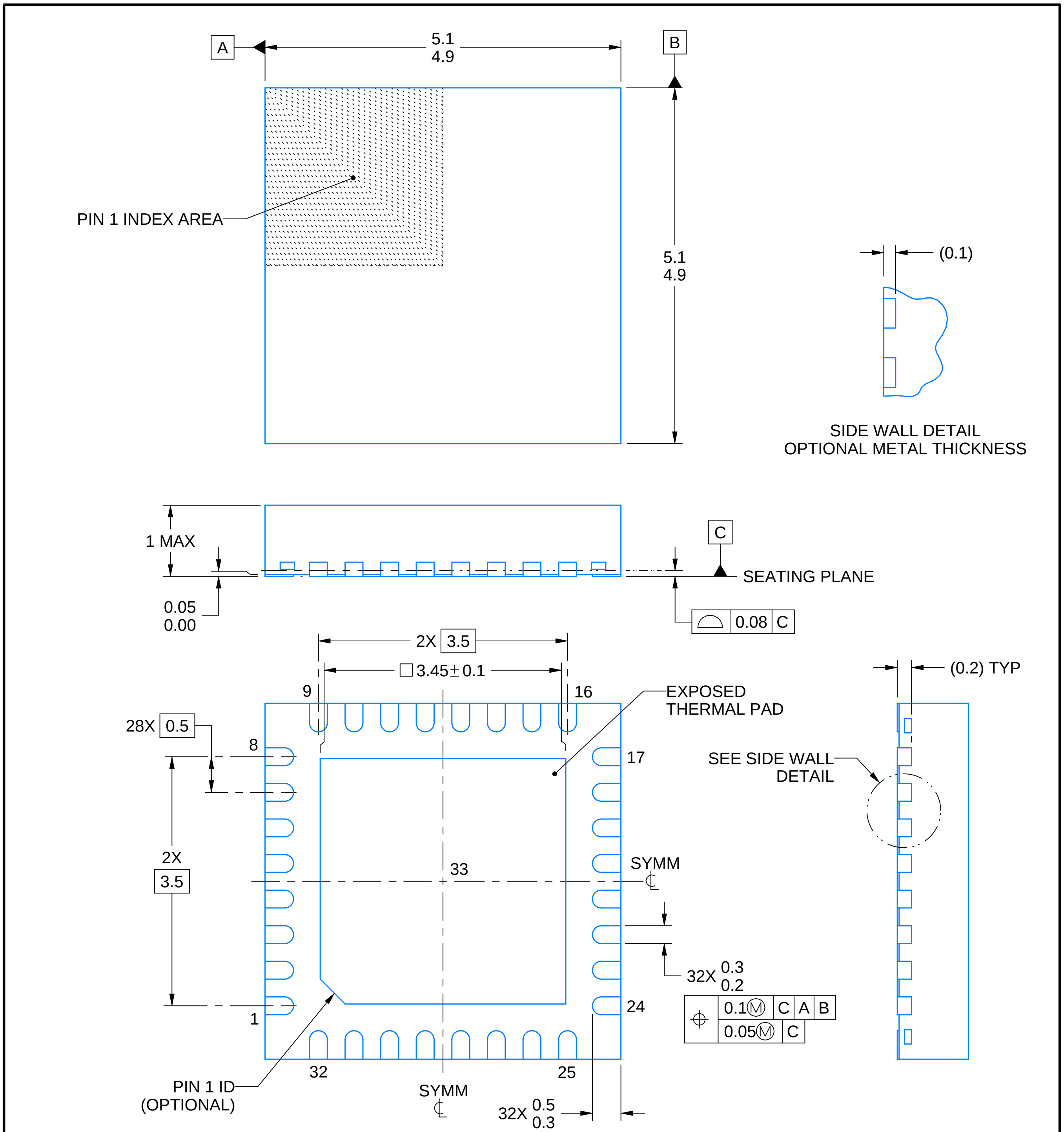
PACKAGE OUTLINE

VQFN - 1 mm max height

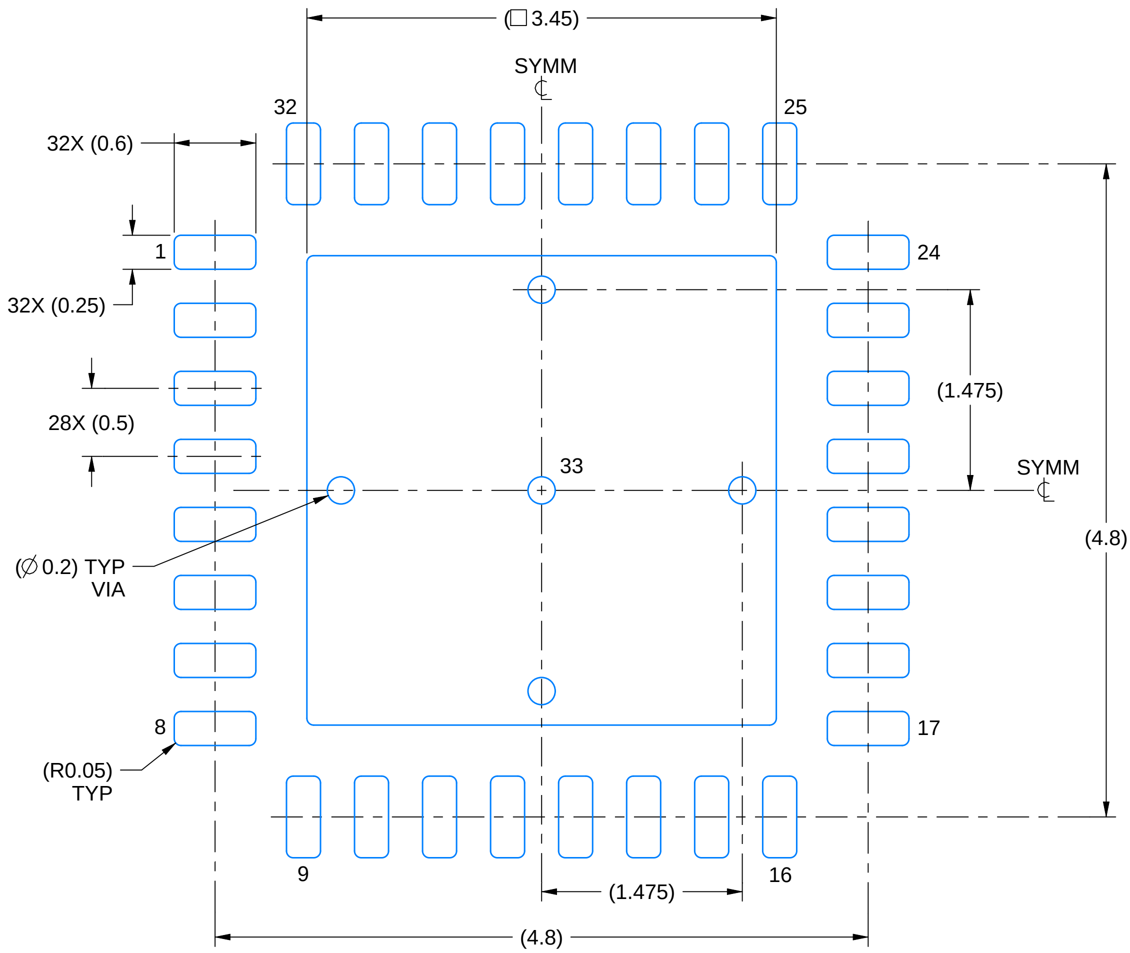
PLASTIC QUAD FLATPACK - NO LEAD



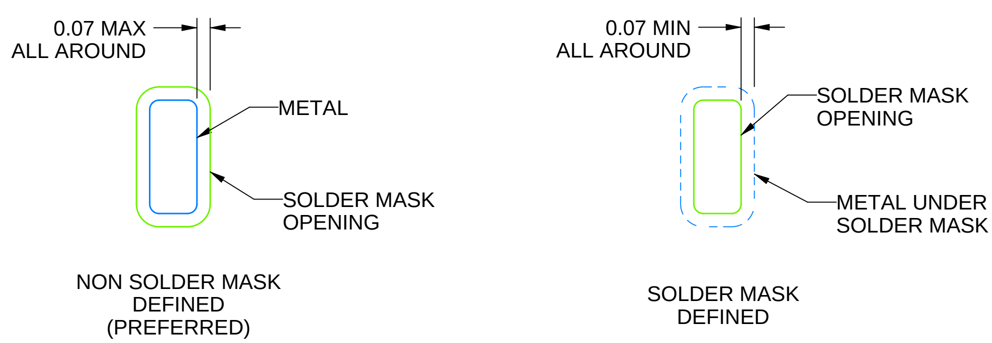
4223442/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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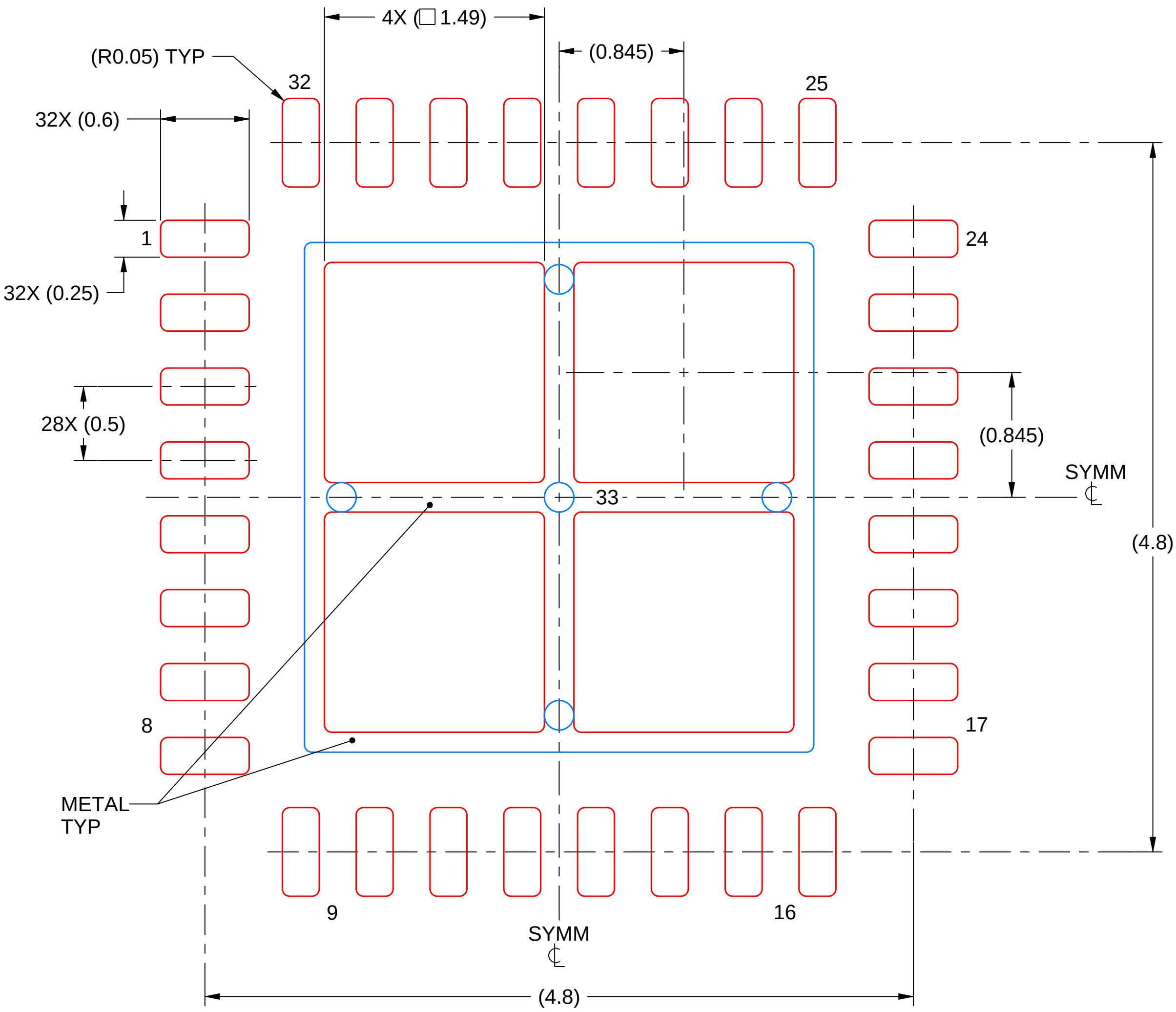
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.