

Implementing HART in PLC Analog Input Modules for Real-Time Communication in 4-20mA Systems

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Introduction

HART enabled field devices are ubiquitous in factory automation and process control applications, allowing bidirectional digital communication over the 4-20mA analog current signal. Often, HART is used to transmit diagnostic or calibration information but can also be used to transmit additional control variables to the PLC. To take full advantage of HART enabled field devices, a HART enabled PLC analog input module (AI) is required to communicate with the field device in real-time. A HART enabled analog input module consists of an ADC and sense resistor to measure the analog current, and a HART modem to modulate and demodulate the HART data.

The [DAC874xH](#) family of devices are standalone modems supporting HART, Foundation Fieldbus, and Profibus PA. These HART certified modems feature SPI/UART interface options, internal filtering, and additional SPI features that add flexibility interfacing with the host MCU, making [DAC874xH](#) an excellent option for analog input module designs requiring HART.

Overview of HART in AI Modules

[Figure 1](#) illustrates a simplified diagram of a HART enabled analog input module. R1 is the sense resistor that both senses the loop current and enables HART communication. The HART physical layer specification requires R1 to be between 230 Ω and 600 Ω . R2 and C1 form a low pass filter to ensure the ADC only measures the DC loop current and the HART modulation is sufficiently attenuated. Depending on the ADC selection, additional filtering can be achieved with the ADC internal digital filter. C2 and C3 AC couple the HART modem input and output to the load resistor.

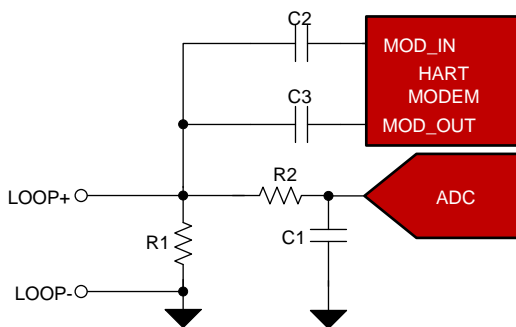


Figure 1. Simplified Analog Input Module with HART

The HART communication protocol is a master/slave communication scheme. The input module acts as the master and sends requests for data to the slave transmitter or field device. The slave transmitter regulates the loop current and transmits HART as a 1mA_{pp} sinusoidal waveform that is converted to a voltage signal by R1 and demodulated by the HART modem at the analog input module. When the analog input module transmits HART it directly couples the voltage signal to the load resistor, creating a HART voltage waveform that is demodulated by the HART modem in the field device.

Design Considerations

When designing an input module with HART it is critical to meet requirements outlined by the HART specification while also meeting the input requirements for the ADC selected. The simplified circuit shown in [Figure 1](#) shows a single load resistor, but it is often more practical to split the load resistor in to three series resistors. At full-scale loop current the voltage at LOOP+ will be outside the range of most precision ADCs if a single resistor is used. This allows flexibility in meeting the input requirements for the ADC while still maintaining the required overall resistive load required for HART. Another advantage of the split load resistor configuration is decreasing the sense resistor value which reduces self heating and drift, minimizing error in the loop current measurement over the current input range.

[Figure 2](#) illustrates a practical example of a HART enabled analog input module that uses separate current sense and HART load resistors. [DAC8740H](#) is the UART interfaced HART modem. [ADS1260](#) is a delta-sigma ADC with internal programmable gain amplifier (PGA) that measures the voltage across the current sense resistor to calculate the DC loop current. The HART signal is modulated and demodulated across the sum of the three resistors. R2 is the current sense resistor and R3 is used to bias the voltage at the negative input of the ADC as the PGA cannot inputs cannot go to ground. The internal PGA allows for use of a smaller current sense resistor reducing self-heating error. For [ADS1260](#) the input requirements arise from the internal PGA headroom requirements. Resistors R3 and R2 must be selected to appropriately set the voltage at both inputs of the ADC. The voltage requirements at the PGA inputs

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