

# DLP3310 0.33 1080p DMD

## 1 Features

- 0.33-inch (8.47-mm) diagonal micromirror array
  - Displays full-HD 1920 × 1080 pixels on the screen
  - 5.4-μm micromirror pitch
  - 17° micromirror tilt (relative to flat surface)
  - Side illumination for optimal efficiency and optical engine size
  - Polarization independent aluminum micromirror surface
- 32-bit subLVDS input data bus
- Dedicated DLPC3437 controller and DLPA3000/DLPA3005 PMIC/LED driver for reliable operation

## 2 Applications

- Mobile smart TVs
- Screenless TVs
- Gaming displays
- Digital signage
- Wearable displays
- Pico projectors
- Interactive displays
- Ultra mobile displays
- Smart home displays
- Virtual assistants

## 3 Description

The [DLP3310](#) digital micromirror device (DMD) is a digitally controlled micro-opto-electromechanical system (MOEMS) spatial light modulator (SLM). When coupled with an appropriate optical system, the DLP3310 DMD displays a very crisp and high quality image or video. DLP3310 is part of the chipset composed of the DLP3310 DMD, [DLPC3437](#) controller, and [DLPA3000/DLPA3005](#) PMIC/LED driver. The compact physical size of the DLP3310 coupled with the controller and the PMIC/LED driver provides a complete system solution that enables small form factor, low power, and full-HD displays.

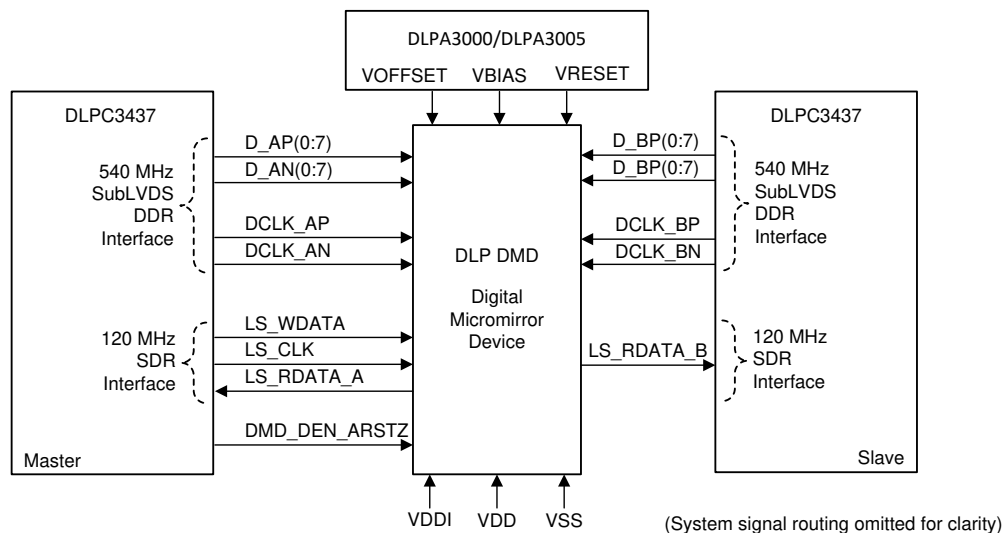
Visit the [getting started with TI DLP®Pico™ display technology](#) page to learn how to get started with the DLP3310.

The DLP3310 ecosystem includes established resources to help the user accelerate the design cycle, which include [production ready optical modules](#), [optical modules manufactures](#), and [design houses](#).

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP3310	FQM (92)	19.25 mm × 7.2 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



### Simplified Application



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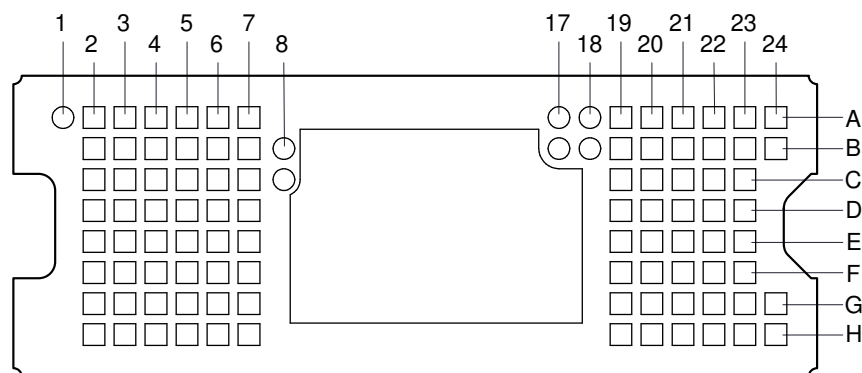
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (April 2022) to Revision C (May 2022)</b> .....	<b>Page</b>
• Updated <i>Micromirror Array Optical Characteristics</i> .....	<b>18</b>
<b>Changes from Revision A (August 2021) to Revision B (April 2022)</b> .....	<b>Page</b>
• This document is updated per the latest Texas Instruments and industry data sheet standards.....	<b>1</b>
• Updated <a href="#">Pin Configuration and Functions</a> .....	<b>3</b>
<b>Changes from Revision * (November 2018) to Revision A (July 2021)</b> .....	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	<b>1</b>
• Updated  T <sub>DELTA</sub>   MAX from 30°C to 15°C.....	<b>7</b>

## 5 Pin Configuration and Functions



**Figure 5-1. FQM Package 92-Pin CLGA Bottom View**

**Table 5-1. Pin Functions – Connector Pins**

PIN <sup>(1)</sup>		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH <sup>(2)</sup> (mm)
NAME	NO.					
DATA INPUTS						
D_AN(0)	C6	I	SubLVDS	Double	Data, negative	2.83
D_AN(1)	D7	I	SubLVDS	Double	Data, negative	4.00
D_AN(2)	D5	I	SubLVDS	Double	Data, negative	1.97
D_AN(3)	F7	I	SubLVDS	Double	Data, negative	4.03
D_AN(4)	F5	I	SubLVDS	Double	Data, negative	1.90
D_AN(5)	G6	I	SubLVDS	Double	Data, negative	3.08
D_AN(6)	H5	I	SubLVDS	Double	Data, negative	2.23
D_AN(7)	H7	I	SubLVDS	Double	Data, negative	3.88
D_AP(0)	C5	I	SubLVDS	Double	Data, positive	2.72
D_AP(1)	D6	I	SubLVDS	Double	Data, positive	3.89
D_AP(2)	D4	I	SubLVDS	Double	Data, positive	1.87
D_AP(3)	F6	I	SubLVDS	Double	Data, positive	3.93
D_AP(4)	F4	I	SubLVDS	Double	Data, positive	1.79
D_AP(5)	G5	I	SubLVDS	Double	Data, positive	2.97
D_AP(6)	H4	I	SubLVDS	Double	Data, positive	2.12
D_AP(7)	H6	I	SubLVDS	Double	Data, positive	3.78
D_BN(0)	C20	I	SubLVDS	Double	Data, negative	2.23
D_BN(1)	D19	I	SubLVDS	Double	Data, negative	3.27
D_BN(2)	D21	I	SubLVDS	Double	Data, negative	1.27
D_BN(3)	F19	I	SubLVDS	Double	Data, negative	3.52
D_BN(4)	F21	I	SubLVDS	Double	Data, negative	1.34
D_BN(5)	G20	I	SubLVDS	Double	Data, negative	2.55
D_BN(6)	H21	I	SubLVDS	Double	Data, negative	1.71
D_BN(7)	H19	I	SubLVDS	Double	Data, negative	3.37
D_BP(0)	C21	I	SubLVDS	Double	Data, positive	2.13
D_BP(1)	D20	I	SubLVDS	Double	Data, positive	3.16
D_BP(2)	D22	I	SubLVDS	Double	Data, positive	1.17
D_BP(3)	F20	I	SubLVDS	Double	Data, positive	3.42
D_BP(4)	F22	I	SubLVDS	Double	Data, positive	1.23
D_BP(5)	G21	I	SubLVDS	Double	Data, positive	2.44

**Table 5-1. Pin Functions – Connector Pins (continued)**

PIN <sup>(1)</sup>		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH <sup>(2)</sup> (mm)
NAME	NO.					
D_BP(6)	H22	I	SubLVDS	Double	Data, positive	1.61
D_BP(7)	H20	I	SubLVDS	Double	Data, positive	3.27
DCLK_AN	E6	I	SubLVDS	Double	Clock, negative	2.56
DCLK_AP	E5	I	SubLVDS	Double	Clock, positive	2.46
DCLK_BN	E20	I	SubLVDS	Double	Clock, negative	2.05
DCLK_BP	E21	I	SubLVDS	Double	Clock, positive	1.95
<b>CONTROL INPUTS</b>						
LS_WDATA	B3	I	LPSDR <sup>(1)</sup>	Single	Write data for low speed interface	1.78
LS_CLK	B5	I	LPSDR	Single	Clock for low-speed interface	1.78
DMD_DEN_ARSTZ	B2	I	LPSDR		Asynchronous reset DMD signal. A low signal places the DMD in reset. A high signal releases the DMD from reset and places it in active mode.	0.85
LS_RDATA_A	B7	O	LPSDR	Single	Read data for low-speed interface	4.19
LS_RDATA_B	B4	O	LPSDR	Single	Read data for low-speed interface	2.18
<b>POWER</b>						
V <sub>BIAS</sub> <sup>(3)</sup>	A6	Power			Supply voltage for positive bias level at micromirrors	
V <sub>BIAS</sub> <sup>(3)</sup>	A22	Power				
V <sub>OFFSET</sub> <sup>(3)</sup>	B21	Power			Supply voltage for HVCMOS core logic. Supply voltage for stepped high level at micromirror address electrodes.	
V <sub>OFFSET</sub> <sup>(3)</sup>	G2	Power			Supply voltage for offset level at micromirrors	
V <sub>RESET</sub>	A5	Power			Supply voltage for negative reset level at micromirrors	
V <sub>RESET</sub>	A23	Power				
V <sub>DD</sub> <sup>(3)</sup>	C2	Power			Supply voltage for LVCMOS core logic. Supply voltage for LPSDR inputs. Supply voltage for normal high level at micromirror address electrodes	
V <sub>DD</sub>	A19	Power				
V <sub>DD</sub>	A20	Power				
V <sub>DD</sub>	A21	Power				
V <sub>DD</sub>	B20	Power				
V <sub>DD</sub>	D2	Power				
V <sub>DD</sub>	D3	Power				
V <sub>DD</sub>	D23	Power				
V <sub>DD</sub>	E2	Power				
V <sub>DD</sub>	F2	Power				
V <sub>DD</sub>	F3	Power				
V <sub>DD</sub>	F23	Power				
V <sub>DDI</sub>	B6	Power			Supply voltage for SubLVDS receivers	
V <sub>DDI</sub>	B19	Power				
V <sub>DDI</sub>	C3	Power				
V <sub>DDI</sub>	C23	Power				
V <sub>DDI</sub>	E3	Power				
V <sub>DDI</sub>	E23	Power				
V <sub>DDI</sub>	G3	Power				
V <sub>DDI</sub>	G23	Power				

**Table 5-1. Pin Functions – Connector Pins (continued)**

PIN <sup>(1)</sup>		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH <sup>(2)</sup> (mm)
NAME	NO.					
V <sub>SS</sub>	A2	Ground			Common return Ground for all power	
V <sub>SS</sub>	A3	Ground				
V <sub>SS</sub>	A4	Ground				
V <sub>SS</sub>	A7	Ground				
V <sub>SS</sub>	A24	Ground				
V <sub>SS</sub>	B22	Ground				
V <sub>SS</sub>	B23	Ground				
V <sub>SS</sub>	B24	Ground				
V <sub>SS</sub>	C4	Ground				
V <sub>SS</sub>	C7	Ground				
V <sub>SS</sub>	C19	Ground				
V <sub>SS</sub>	C22	Ground				
V <sub>SS</sub>	E4	Ground				
V <sub>SS</sub>	E7	Ground				
V <sub>SS</sub>	E19	Ground				
V <sub>SS</sub>	E22	Ground				
V <sub>SS</sub>	G4	Ground				
V <sub>SS</sub>	G7	Ground				
V <sub>SS</sub>	G19	Ground				
V <sub>SS</sub>	G22	Ground				
V <sub>SS</sub>	G24	Ground				
V <sub>SS</sub>	H2	Ground				
V <sub>SS</sub>	H3	Ground				
V <sub>SS</sub>	H23	Ground				
V <sub>SS</sub>	H24	Ground				

- (1) Low speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)*. See [JESD209B](#).
- (2) Net trace lengths inside the package:  
Relative dielectric constant for the FQM ceramic package is 9.8.  
Propagation speed =  $11.8 / \sqrt{9.8} = 3.769$  in/ns.  
Propagation delay =  $0.265$  ns/inch =  $265$  ps/in =  $10.43$  ps/mm.
- (3) The following power supplies are all required to operate the DMD: V<sub>DD</sub>, V<sub>DDI</sub>, V<sub>OFFSET</sub>, V<sub>BIAS</sub>, V<sub>RESET</sub>. All V<sub>SS</sub> connections are also required.

**Table 5-2. Pin Functions – Test Pads**

NUMBER	SYSTEM BOARD
A1	Do not connect.
A17	Do not connect.
A18	Do not connect.
B8	Do not connect.
B17	Do not connect.
B18	Do not connect.
C8	Do not connect.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

see (1)

			MIN	MAX	UNIT
Supply voltage	$V_{DD}$	Supply voltage for LVC MOS core logic <sup>(2)</sup> Supply voltage for LPSDR low speed interface	−0.5	2.3	V
	$V_{DDI}$	Supply voltage for SubLVDS receivers <sup>(2)</sup>	−0.5	2.3	V
	$V_{OFFSET}$	Supply voltage for HVC MOS and micromirror electrode <sup>(2) (3)</sup>	−0.5	11	V
	$V_{BIAS}$	Supply voltage for micromirror electrode <sup>(2)</sup>	−0.5	19	V
	$V_{RESET}$	Supply voltage for micromirror electrode <sup>(2)</sup>	−15	0.5	V
	$ V_{DDI} - V_{DD} $	Supply voltage delta (absolute value) <sup>(4)</sup>		0.3	V
	$ V_{BIAS} - V_{OFFSET} $	Supply voltage delta (absolute value) <sup>(5)</sup>		11	V
	$ V_{BIAS} - V_{RESET} $	Supply voltage delta (absolute value) <sup>(6)</sup>		34	V
Input voltage	Input voltage for other inputs LPSDR <sup>(2)</sup>		−0.5	$V_{DD} + 0.5$	V
	Input voltage for other inputs SubLVDS <sup>(2) (7)</sup>		−0.5	$V_{DDI} + 0.5$	V
Input pins	$ V_{ID} $	SubLVDS input differential voltage (absolute value) <sup>(7)</sup>		810	mV
	$I_{ID}$	SubLVDS input differential current		10	mA
Clock frequency	$f_{clock}$	Clock frequency for low speed interface LS_CLK		130	MHz
	$f_{clock}$	Clock frequency for high speed interface DCLK		620	MHz
Environmental	$T_{ARRAY}$ and $T_{WINDOW}$	Temperature—operational <sup>(8)</sup>	−20	90	°C
		Temperature—non-operational <sup>(8)</sup>	−40	90	°C
	$ T_{DELTA} $	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 <sup>(9)</sup>		30	°C
	$T_{DP}$	Dew point—operating and non-operating		81	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to the ground terminals ( $V_{SS}$ ). The following power supplies are all required to operate the DMD:  $V_{DD}$ ,  $V_{DDI}$ ,  $V_{OFFSET}$ ,  $V_{BIAS}$ , and  $V_{RESET}$ . All  $V_{SS}$  connections are also required.
- (3)  $V_{OFFSET}$  supply transients must fall within specified voltages.
- (4) Exceeding the recommended allowable absolute voltage difference between  $V_{DDI}$  and  $V_{DD}$  may result in excessive current draw.
- (5) Exceeding the recommended allowable absolute voltage difference between  $V_{BIAS}$  and  $V_{OFFSET}$  may result in excessive current draw.
- (6) Exceeding the recommended allowable absolute voltage difference between  $V_{BIAS}$  and  $V_{RESET}$  may result in excessive current draw.
- (7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
- (8) The highest temperature of the active array (as calculated by the [Micromirror Array Temperature Calculation](#)) or of any point along the window edge as defined in [Figure 7-1](#). The locations of thermal test points TP2, TP3, TP4, and TP5 in [Figure 7-1](#) are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
- (9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in [Figure 7-1](#). The window test points TP2, TP3, TP4, and TP5 shown in [Figure 7-1](#) are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

### 6.2 Storage Conditions

applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
$T_{DMD}$	DMD storage temperature	−40	85	°C
$T_{DP-AVG}$	Average dew point temperature (non-condensing) <sup>(1)</sup>		24	°C
$T_{DP-ELR}$	Elevated dew point temperature range (non-condensing) <sup>(2)</sup>	28	36	°C
$CT_{ELR}$	Cumulative time in elevated dew point temperature range		6	Months

- (1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.

- (2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of  $CT_{ELR}$ .

### 6.3 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V

- (1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

### 6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

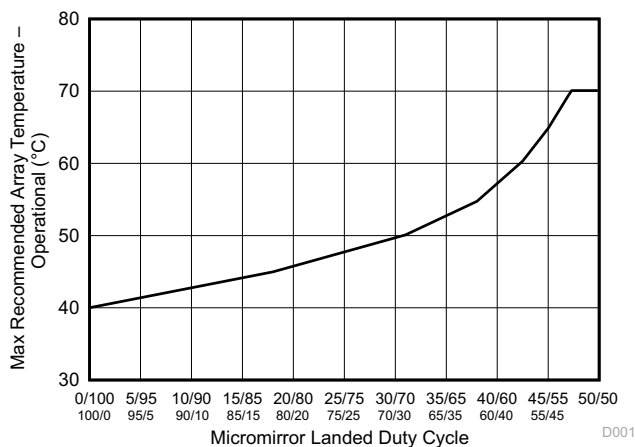
		MIN	NOM	MAX	UNIT
<b>SUPPLY VOLTAGE RANGE<sup>(3)</sup></b>					
$V_{DD}$	Supply voltage for LVC MOS core logic Supply voltage for LP SDR low-speed interface	1.65	1.8	1.95	V
$V_{DDI}$	Supply voltage for SubLVDS receivers	1.65	1.8	1.95	V
$V_{OFFSET}$	Supply voltage for HVC MOS and micromirror electrode <sup>(4)</sup>	9.5	10	10.5	V
$V_{BIAS}$	Supply voltage for mirror electrode	17.5	18	18.5	V
$V_{RESET}$	Supply voltage for micromirror electrode	−14.5	−14	−13.5	V
$ V_{DDI} - V_{DD} $	Supply voltage delta (absolute value) <sup>(5)</sup>			0.3	V
$ V_{BIAS} - V_{OFFSET} $	Supply voltage delta (absolute value) <sup>(6)</sup>			10.5	V
$ V_{BIAS} - V_{RESET} $	Supply voltage delta (absolute value) <sup>(7)</sup>			33	V
<b>CLOCK FREQUENCY</b>					
$f_{clock}$	Clock frequency for low speed interface LS_CLK <sup>(8)</sup>	108		120	MHz
$f_{clock}$	Clock frequency for high speed interface DCLK <sup>(9)</sup>	300		540	MHz
	Duty cycle distortion DCLK	44%		56%	
<b>SUBLVDS INTERFACE<sup>(9)</sup></b>					
$ V_{ID} $	SubLVDS input differential voltage (absolute value). See Figure 6-8, Figure 6-9.	150	250	350	mV
$V_{CM}$	Common mode voltage. See Figure 6-8, Figure 6-9.	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage. See Figure 6-8, Figure 6-9.	575		1225	mV
$Z_{LINE}$	Line differential impedance (PWB/trace)	90	100	110	Ω
$Z_{IN}$	Internal differential termination resistance. See Figure 6-10.	80	100	120	Ω
	100-Ω differential PCB trace	6.35		152.4	mm
<b>ENVIRONMENTAL</b>					
$T_{ARRAY}$	Array temperature – long-term operational <sup>(10) (11) (12) (13)</sup>	0	40 to 70 <sup>(12)</sup>		°C
	Array temperature – short-term operational, 25 hr max <sup>(11) (14)</sup>	−20		−10	°C
	Array temperature – short-term operational, 500 hr max <sup>(11) (14)</sup>	−10		0	°C
	Array temperature – short-term operational, 500 hr max <sup>(11) (14)</sup>	70		75	°C
$T_{WINDOW}$	Window temperature – operational <sup>(15) (16)</sup>			90	°C
$ T_{DELTA} $	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 <sup>(17)</sup>			15	°C
$T_{DP-AVG}$	Average dew point temperature, non-condensing <sup>(18)</sup>			24	°C
$T_{DP-ELR}$	Elevated dew point temperature range, non-condensing <sup>(19)</sup>	28		36	°C
$CT_{ELR}$	Cumulative time in elevated dew point temperature range			6	Months
$ILL_{UV}$	Illumination wavelengths < 420 nm <sup>(10)</sup>			0.68	mW/cm <sup>2</sup>
$ILL_{VIS}$	Illumination wavelengths between 420 nm and 700 nm			Thermally Limited	
$ILL_{IR}$	Illumination wavelengths > 700 nm			10	mW/cm <sup>2</sup>

## 6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		MIN	NOM	MAX	UNIT
ILL <sub>θ</sub>	Illumination marginal ray angle <sup>(16)</sup>			55	°

- (1) The following power supplies are all required to operate the DMD:  $V_{DD}$ ,  $V_{DDI}$ ,  $V_{OFFSET}$ ,  $V_{BIAS}$ , and  $V_{RESET}$ . All  $V_{SS}$  connections are also required.
- (2) The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the *Recommended Operating Conditions*. No level of performance is implied when operating the device above or below the *Recommended Operating Conditions* limits.
- (3) All voltage values are with respect to the ground pins ( $V_{SS}$ ).
- (4)  $V_{OFFSET}$  supply transients must fall within specified max voltages.
- (5) To prevent excess current, the supply voltage delta  $|V_{DDI} - V_{DD}|$  must be less than the specified limit.
- (6) To prevent excess current, the supply voltage delta  $|V_{BIAS} - V_{OFFSET}|$  must be less than the specified limit.
- (7) To prevent excess current, the supply voltage delta  $|V_{BIAS} - V_{RESET}|$  must be less than the specified limit.
- (8) LS\_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
- (9) Refer to the SubLVDS timing requirements in [Timing Requirements](#).
- (10) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination will reduce device lifetime.
- (11) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in [Figure 7-1](#) and the package thermal resistance using the [Micromirror Array Temperature Calculation](#).
- (12) Per [Figure 6-1](#), the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to [Section 7.7](#) for a definition of micromirror landed duty cycle.
- (13) Long-term is defined as the useful life of the device.
- (14) Short-term is the total cumulative time over the useful life of the device.
- (15) The locations of thermal test points TP2, TP3, TP4, and TP5 shown in [Figure 7-1](#) are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, test points should be added to those locations.
- (16) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including Pond of Micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.
- (17) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge shown in [Figure 7-1](#). The window test points TP2, TP3, TP4, and TP5 shown in [Figure 7-1](#) are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
- (18) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
- (19) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of  $CT_{ELR}$ .



**Figure 6-1. Maximum Recommended Array Temperature—Derating Curve**



## 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DLP3310	UNIT
		FQM (LGA)	
		92 PINS	
Thermal resistance	Active area to test point 1 (TP1)	6.0	°C/W

- (1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

## 6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS <sup>(2)</sup>	MIN	TYP	MAX	UNIT
CURRENT						
I <sub>DD</sub>	Supply current: V <sub>DD</sub> <sup>(3) (4)</sup>	V <sub>DD</sub> = 1.95 V			135	mA
		V <sub>DD</sub> = 1.8 V		123.6		
I <sub>DDI</sub>	Supply current: V <sub>DDI</sub> <sup>(3) (4)</sup>	V <sub>DDI</sub> = 1.95 V			35.34	mA
		V <sub>DD</sub> = 1.8 V		32		
I <sub>OFFSET</sub>	Supply current: V <sub>OFFSET</sub> <sup>(5) (6)</sup>	V <sub>OFFSET</sub> = 10.5 V			2.55	mA
		V <sub>OFFSET</sub> = 10 V		2.5		
I <sub>BIAS</sub>	Supply current: V <sub>BIAS</sub> <sup>(5) (6)</sup>	V <sub>BIAS</sub> = 18.5 V			1.25	mA
		V <sub>BIAS</sub> = 18 V		1.2		
I <sub>RESET</sub>	Supply current: V <sub>RESET</sub> <sup>(6)</sup>	V <sub>RESET</sub> = −14.5 V			−2.55	mA
		V <sub>RESET</sub> = −14 V		−2.5		
POWER <sup>(7)</sup>						
P <sub>DD</sub>	Supply power dissipation: V <sub>DD</sub> <sup>(3) (4)</sup>	V <sub>DD</sub> = 1.95 V			263.25	mW
		V <sub>DD</sub> = 1.8 V		222.48		
P <sub>DDI</sub>	Supply power dissipation: V <sub>DDI</sub> <sup>(3) (4)</sup>	V <sub>DDI</sub> = 1.95 V			68.91	mW
		V <sub>DD</sub> = 1.8 V		57.6		
P <sub>OFFSET</sub>	Supply power dissipation: V <sub>OFFSET</sub> <sup>(5) (6)</sup>	V <sub>OFFSET</sub> = 10.5 V			26.78	mW
		V <sub>OFFSET</sub> = 10 V		25		
P <sub>BIAS</sub>	Supply power dissipation: V <sub>BIAS</sub> <sup>(5) (6)</sup>	V <sub>BIAS</sub> = 18.5 V			23.13	mW
		V <sub>BIAS</sub> = 18 V		21.6		
P <sub>RESET</sub>	Supply power dissipation: V <sub>RESET</sub> <sup>(6)</sup>	V <sub>RESET</sub> = −14.5 V			36.98	mW
		V <sub>RESET</sub> = −14 V		35		
P <sub>TOTAL</sub>	Supply power dissipation: Total			361.68	419.05	mW
LPSDR INPUT <sup>(8)</sup>						
V <sub>IH(DC)</sub>	DC input high voltage <sup>(9)</sup>		0.7 × V <sub>DD</sub>	V <sub>DD</sub> + 0.3		V
V <sub>IL(DC)</sub>	DC input low voltage <sup>(9)</sup>		−0.3	0.3 × V <sub>DD</sub>		V
V <sub>IH(AC)</sub>	AC input high voltage <sup>(9)</sup>		0.8 × V <sub>DD</sub>	V <sub>DD</sub> + 0.3		V
V <sub>IL(AC)</sub>	AC input low voltage <sup>(9)</sup>		−0.3	0.2 × V <sub>DD</sub>		V
ΔV <sub>T</sub>	Hysteresis ( V <sub>T+</sub> − V <sub>T−</sub> )	Figure 6-10	0.1 × V <sub>DD</sub>	0.4 × V <sub>DD</sub>		V
I <sub>IL</sub>	Low-level input current	V <sub>DD</sub> = 1.95 V; V <sub>I</sub> = 0 V	−100			nA
I <sub>IH</sub>	High-level input current	V <sub>DD</sub> = 1.95 V; V <sub>I</sub> = 1.95 V			100	nA
LPSDR OUTPUT <sup>(10)</sup>						
V <sub>OH</sub>	DC output high voltage	I <sub>OH</sub> = −2 mA	0.8 × V <sub>DD</sub>			V

## 6.6 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS <sup>(2)</sup>	MIN	TYP	MAX	UNIT
V <sub>OL</sub>	DC output low voltage	I <sub>OL</sub> = 2 mA			0.2 × V <sub>DD</sub>	V
<b>CAPACITANCE</b>						
C <sub>IN</sub>	Input capacitance LPSDR	f = 1 MHz			10	pF
	Input capacitance SubLVDS	f = 1 MHz			20	pF
C <sub>OUT</sub>	Output capacitance	f = 1 MHz			10	pF
C <sub>RESET</sub>	Reset group capacitance	f = 1 MHz; (768 × 344) micromirrors	400		500	pF

- (1) Device electrical characteristics are in [Recommended Operating Conditions](#), unless otherwise noted.  
 (2) All voltage values are with respect to the ground pins (V<sub>SS</sub>).  
 (3) To prevent excess current, the supply voltage delta |V<sub>DDI</sub> – V<sub>DD</sub>| must be less than the specified limit.  
 (4) Supply power dissipation based on non-compressed commands and data.  
 (5) To prevent excess current, the supply voltage delta |V<sub>BIAS</sub> – V<sub>OFFSET</sub>| must be less than the specified limit.  
 (6) Supply power dissipation based on 3 global resets in 200 μs.  
 (7) The following power supplies are all required to operate the DMD: V<sub>DD</sub>, V<sub>DDI</sub>, V<sub>OFFSET</sub>, V<sub>BIAS</sub>, V<sub>RESET</sub>. All V<sub>SS</sub> connections are also required.  
 (8) LPSDR specifications are for pins LS\_CLK and LS\_WDATA.  
 (9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low-Power Double Data Rate (LPDDR)* [JESD209B](#).  
 (10) LPSDR specification is for pin LS\_RDATA.

## 6.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

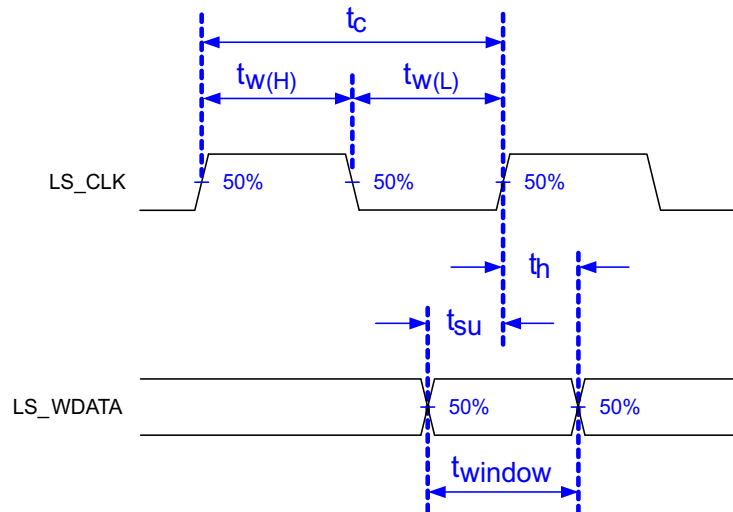
			MIN	NOM	MAX	UNIT
<b>LPSDR</b>						
t <sub>r</sub>	Rise slew rate <sup>(1)</sup>	(30% to 80%) × V <sub>DD</sub> . See <a href="#">Figure 6-3</a> .	1		3	V/ns
t <sub>f</sub>	Fall slew rate <sup>(1)</sup>	(70% to 20%) × V <sub>DD</sub> . See <a href="#">Figure 6-3</a> .	1		3	V/ns
t <sub>r</sub>	Rise slew rate <sup>(2)</sup>	(20% to 80%) × V <sub>DD</sub> . See <a href="#">Figure 6-3</a> .	0.25			V/ns
t <sub>f</sub>	Fall slew rate <sup>(2)</sup>	(80% to 20%) × V <sub>DD</sub> . See <a href="#">Figure 6-3</a> .	0.25			V/ns
t <sub>c</sub>	Cycle time LS_CLK <sub>i</sub>	See <a href="#">Figure 6-2</a> .	7.7	8.3		ns
t <sub>W(H)</sub>	Pulse duration LS_CLK high	50% to 50% reference points. See <a href="#">Figure 6-2</a> .	3.1			ns
t <sub>W(L)</sub>	Pulse duration LS_CLK low	50% to 50% reference points. See <a href="#">Figure 6-2</a> .	3.1			ns
t <sub>su</sub>	Setup time	LS_WDATA valid before LS_CLK ↑. See <a href="#">Figure 6-2</a> .	1.5			ns
t <sub>h</sub>	Hold time	LS_WDATA valid after LS_CLK ↑. See <a href="#">Figure 6-2</a> .	1.5			ns
t <sub>WINDOW</sub>	Window time <sup>(1) (3)</sup>	Setup time + Hold time, <a href="#">Figure 6-2</a>	3			ns
t <sub>DERATING</sub>	Window time derating <sup>(1) (3)</sup>	For each 0.25 V/ns reduction in slew rate below 1 V/ns. See <a href="#">Figure 6-5</a> .		0.35		ns
<b>SubLVDS</b>						
t <sub>r</sub>	Rise slew rate	20% to 80% reference points. See <a href="#">Figure 6-4</a> .	0.7	1		V/ns
t <sub>f</sub>	Fall slew rate	80% to 20% reference points. See <a href="#">Figure 6-4</a> .	0.7	1		V/ns
t <sub>c</sub>	Cycle time DCLK	See <a href="#">Figure 6-6</a> .	1.79	1.85		ns

## 6.7 Timing Requirements (continued)

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

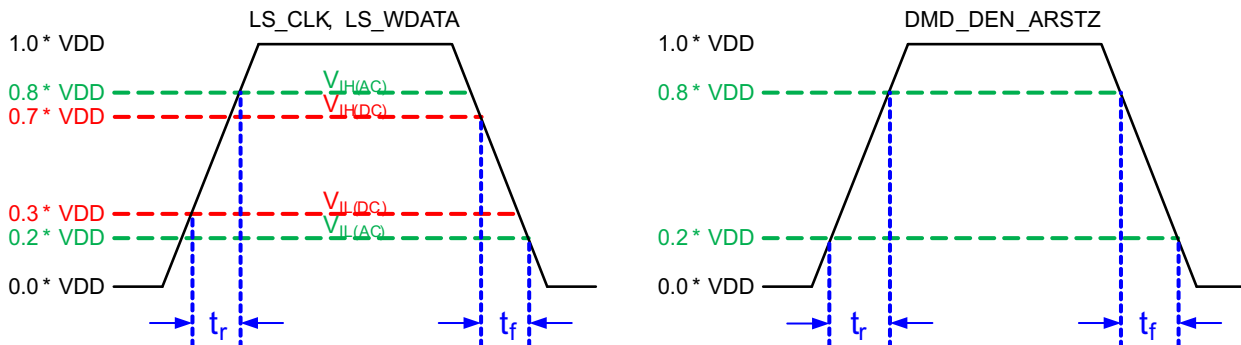
			MIN	NOM	MAX	UNIT
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points. See <a href="#">Figure 6-6</a> .	0.79			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points. See <a href="#">Figure 6-6</a> .	0.79			ns
$t_{su}$	Setup time	D(0:7) valid before DCLK $\uparrow$ or DCLK $\downarrow$ . See <a href="#">Figure 6-6</a> .				
$t_h$	Hold time	D(0:7) valid after DCLK $\uparrow$ or DCLK $\downarrow$ . See <a href="#">Figure 6-6</a> .				
$t_{WINDOW}$	Window time	Setup time + Hold time. See <a href="#">Figure 6-6</a> , <a href="#">Figure 6-7</a> .			3.0	ns
$t_{LVDS-ENABLE+REFGEN}$	Power-up receiver <sup>(4)</sup>				2000	ns

- (1) Specification is for LS\_CLK and LS\_WDATA pins. Refer to LPSDR input rise slew rate and fall slew rate in [Figure 6-3](#).
- (2) Specification is for DMD\_DEN\_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in [Figure 6-3](#).
- (3) Window time derating example: 0.5-V/ns slew rate increases the window time by 0.7 ns, from 3 to 3.7 ns.
- (4) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.



Low-speed interface is LPSDR and adheres to the [Electrical Characteristics](#) and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR) JESD209B*.

**Figure 6-2. LPSDR Switching Parameters**



**Figure 6-3. LPSDR Input Rise and Fall Slew Rate**

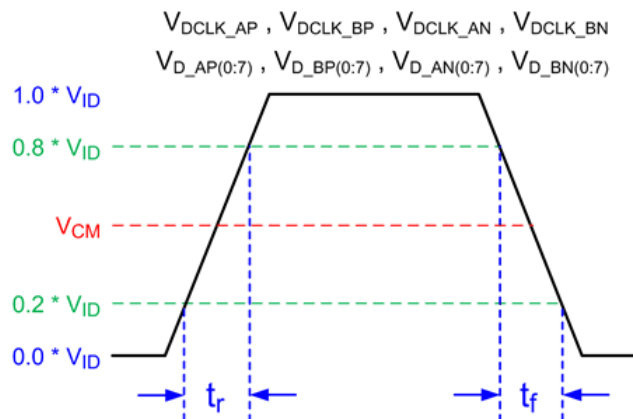


Figure 6-4. SubLVDS Input Rise and Fall Slew Rate

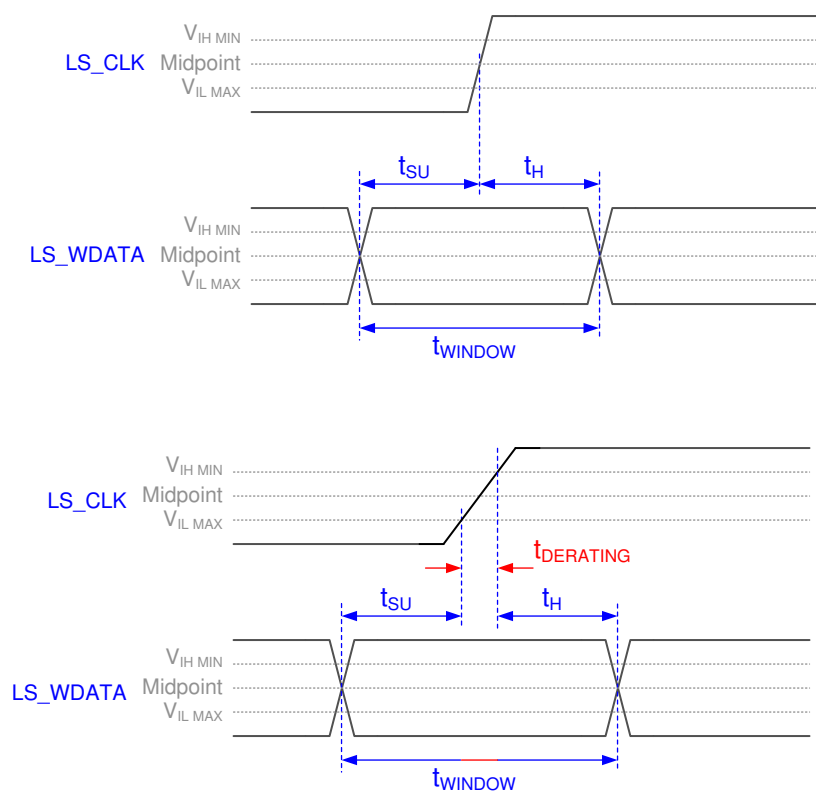
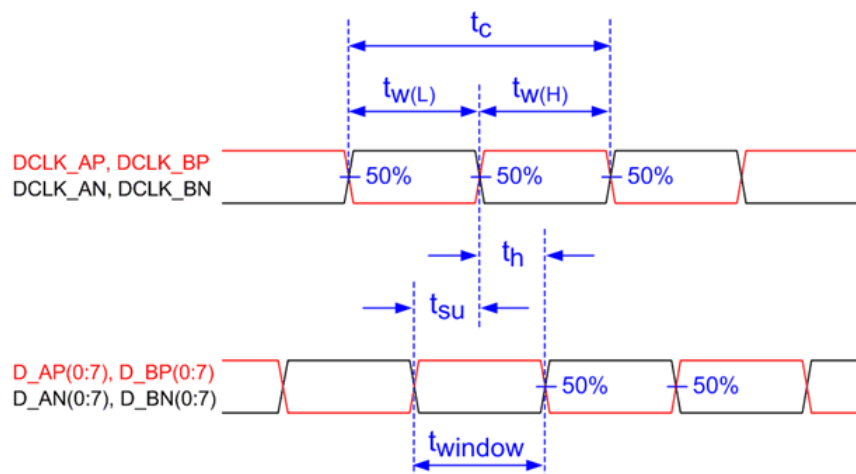
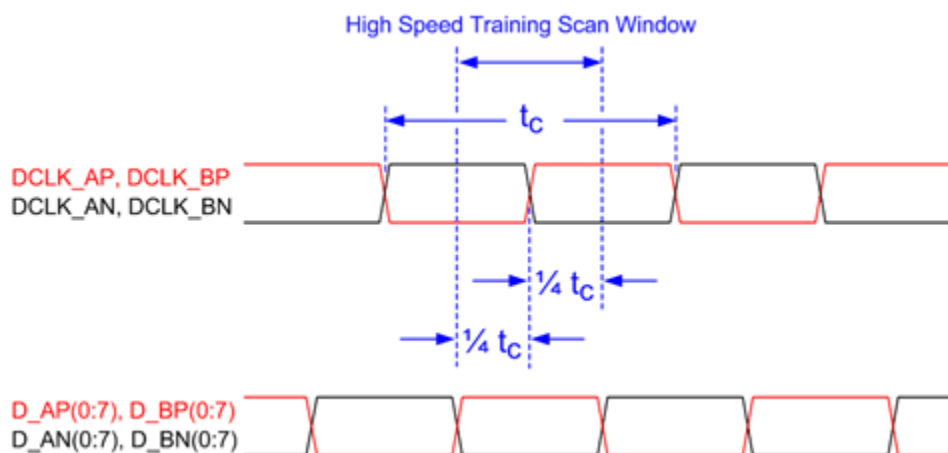


Figure 6-5. Window Time Derating Concept

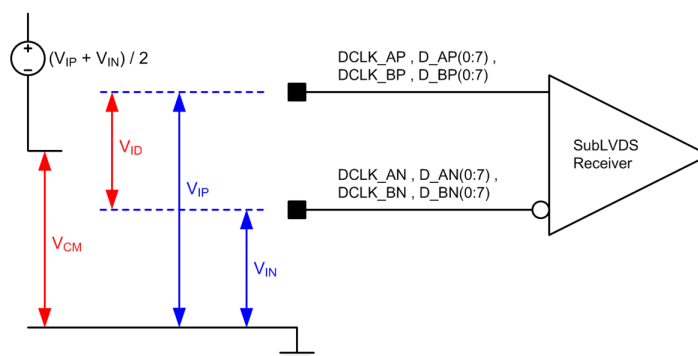


**Figure 6-6. SubLVDS Switching Parameters**



Note: Refer to [High Speed Interface](#) for details.

**Figure 6-7. High-Speed Training Scan Window**



**Figure 6-8. SubLVDS Voltage Parameters**

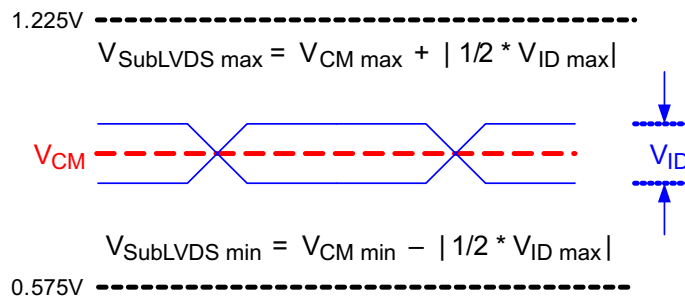


Figure 6-9. SubLVDS Waveform Parameters

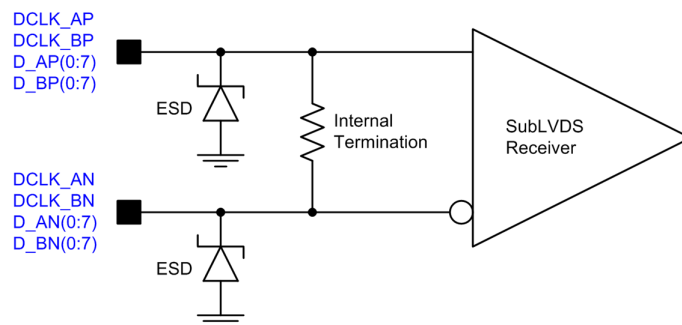


Figure 6-10. SubLVDS Equivalent Input Circuit

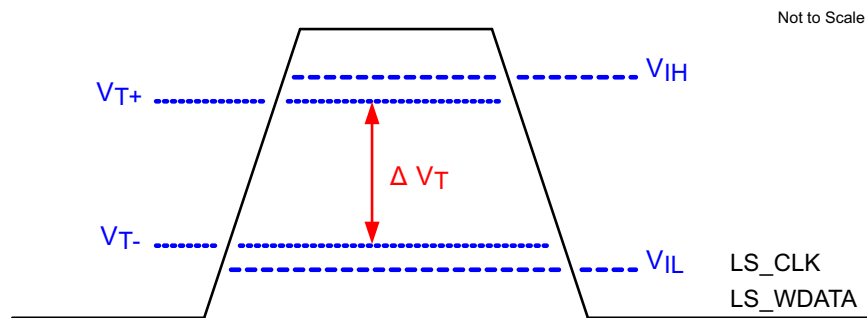


Figure 6-11. LPSDR Input Hysteresis

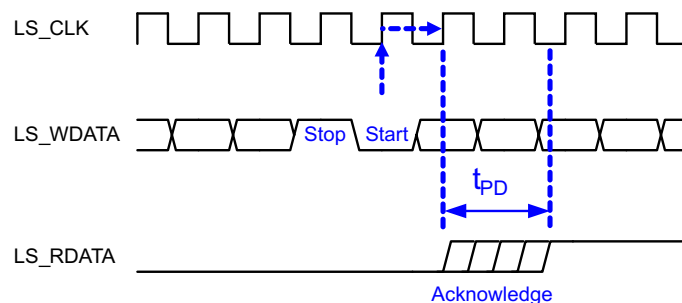
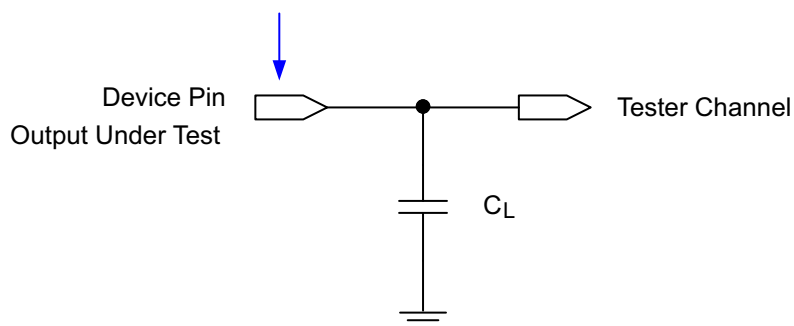


Figure 6-12. LPSDR Read Out

Data Sheet Timing Reference Point



See [Timing](#) for more information.

**Figure 6-13. Test Load Circuit for Output Propagation Measurement**

## 6.8 Switching Characteristics

See<sup>(1)</sup>.

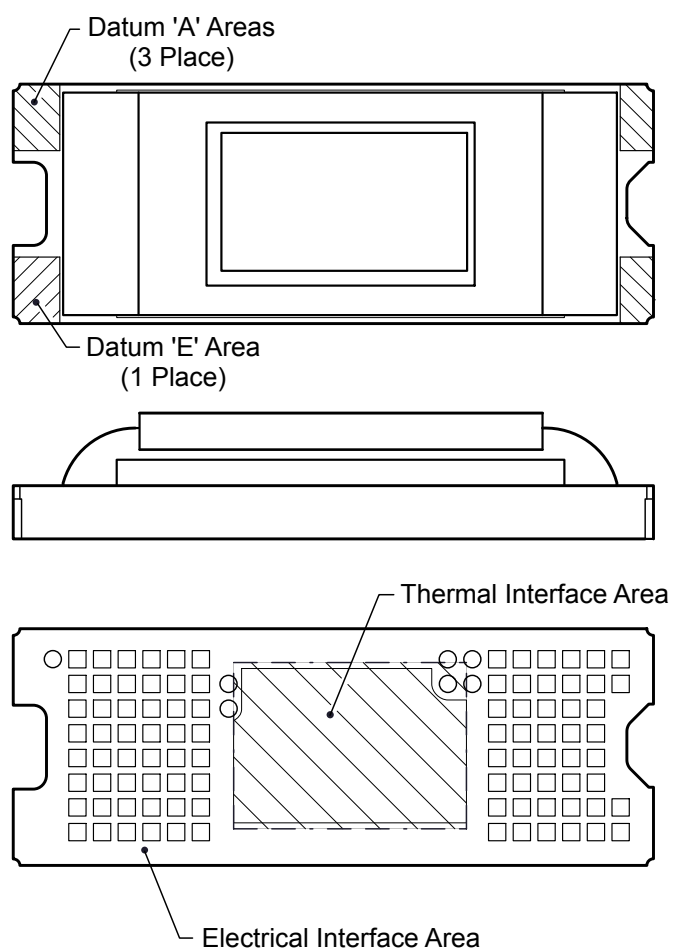
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD}$ Output propagation, clock to Q, rising edge of LS_CLK input to LS_RDATA output (See <a href="#">Figure 6-12.</a> )	$C_L = 45 \text{ pF}$			15	ns
Slew rate, LS_RDATA		0.5			V/ns
Output duty cycle distortion, LS_RDATA		40%		60%	

(1) Device electrical characteristics are over [Recommended Operation Conditions](#) unless otherwise noted.

## 6.9 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:				
• Thermal Interface Area <sup>(1)</sup>			60	N
• Clamping and Electrical Interface Area <sup>(1)</sup>			110	N

(1) Uniformly distributed within area shown in [Figure 6-14.](#)



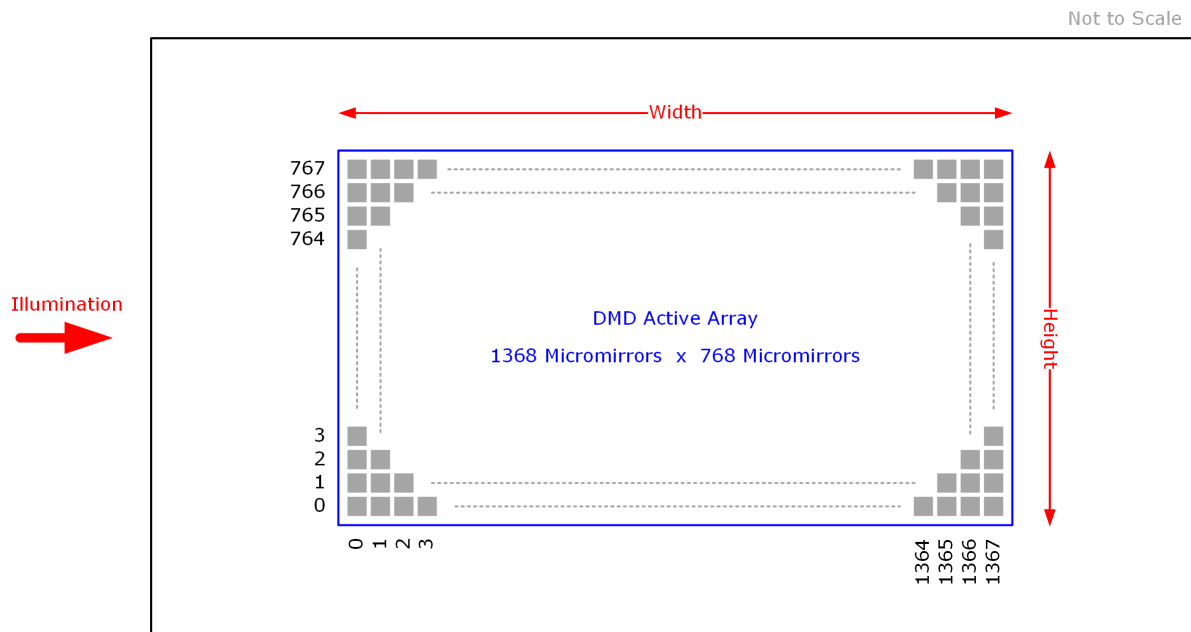
**Figure 6-14. System Interface Loads**



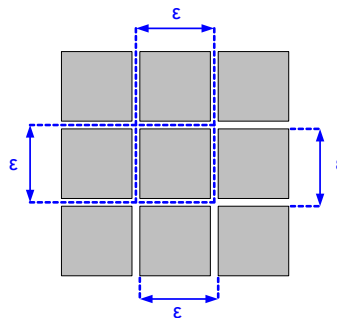
## 6.10 Micromirror Array Physical Characteristics

PARAMETER		VALUE	UNIT
Number of active columns	See <a href="#">Figure 6-15 (2)</a> .	1368	micromirrors
Number of active rows	See <a href="#">Figure 6-15 (2)</a> .	768	micromirrors
Micromirror (pixel) pitch	See <a href="#">Figure 6-16</a> .	5.4	$\mu\text{m}$
Micromirror active array width	Micromirror pitch $\times$ number of active columns; see <a href="#">Figure 6-15</a> .	7.387	mm
Micromirror active array height	Micromirror pitch $\times$ number of active rows; see <a href="#">Figure 6-15</a> .	4.147	mm
Micromirror active border	Pond of micromirror (POM) <sup>(1)</sup>	20	micromirrors/side

- (1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.
- (2) The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enable each micromirror to display two distinct pixels on the screen during every frame, resulting in a full  $1920 \times 1080$  pixel image being displayed.



**Figure 6-15. Micromirror Array Physical Characteristics**



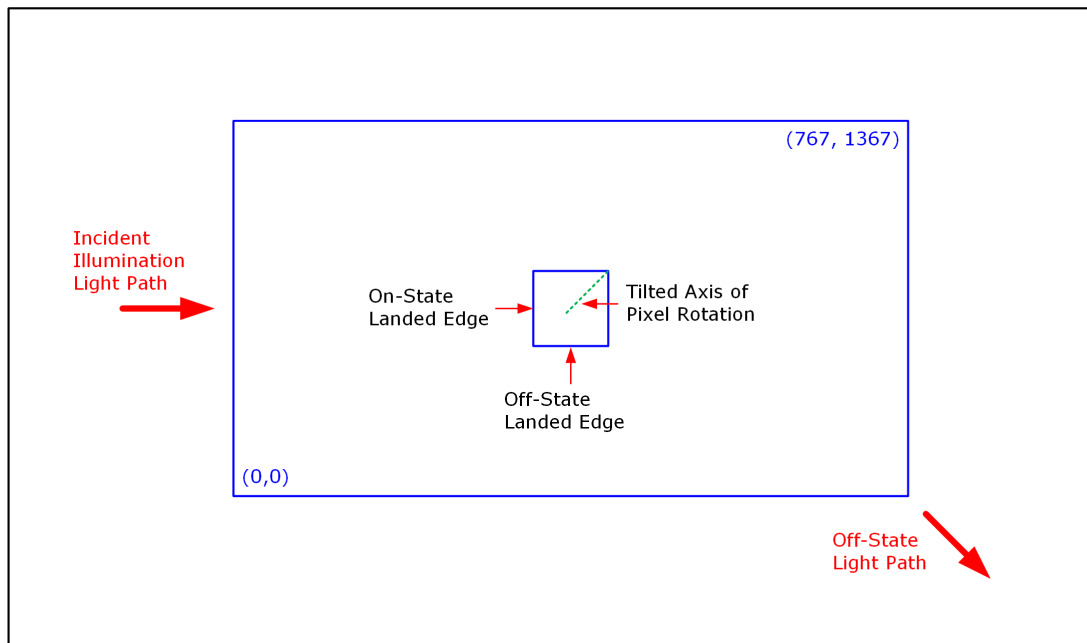
**Figure 6-16. Mirror (Pixel) Pitch**

## 6.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle		DMD landed state <sup>(1)</sup>		17		degree
Micromirror tilt angle tolerance <sup>(2) (3) (4) (5)</sup>			-1.4		1.4	degree
Micromirror tilt direction <sup>(6) (7)</sup>		Landed ON state		180		degree
		Landed OFF state		270		
Micromirror crossover time <sup>(8)</sup>		Typical performance		1	3	μs
Micromirror switching time <sup>(9)</sup>		Typical performance	10			
Image performance <sup>(10)</sup>	Bright pixel(s) in active area <sup>(11)</sup>	Gray 10 Screen <sup>(12)</sup>			0	micromirrors
	Bright pixel(s) in the POM <sup>(13)</sup>	Gray 10 Screen <sup>(12)</sup>			1	
	Dark pixel(s) in the active area <sup>(14)</sup>	White Screen			4	
	Adjacent pixel(s) <sup>(15)</sup>	Any Screen			0	
	Unstable pixel(s) in active area <sup>(16)</sup>	Any Screen			0	

- (1) Measured relative to the plane formed by the overall micromirror array.
- (2) Additional variation exists between the micromirror array and the package datums.
- (3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
- (4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
- (5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
- (6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON state direction. A binary value of 0 results in a micromirror landing in the OFF state direction. See [Figure 6-17](#).
- (7) Micromirror tilt direction is measured as in a typical polar coordinate system: Measuring counter-clockwise from a 0° reference which is aligned with the +X Cartesian axis.
- (8) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
- (9) The minimum time between successive transitions of a micromirror.
- (10) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
  - Test set degamma shall be linear
  - Test set brightness and contrast shall be set to nominal
  - The diagonal size of the projected image shall be a minimum of 20 inches
  - The projections screen shall be 1X gain
  - The projected image shall be inspected from a 38 inch minimum viewing distance
  - The image shall be in focus during all image quality tests
- (11) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
- (12) Gray 10 screen definition: All areas of the screen are colored with the following settings:
  - Red = 10/255
  - Green = 10/255
  - Blue = 10/255
- (13) POM definition: Rectangular border of off-state mirrors surrounding the active area
- (14) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
- (15) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster
- (16) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image

Not to Scale



**Figure 6-17. Landed Pixel Orientation and Tilt**

## 6.12 Window Characteristics

PARAMETER <sup>(1)</sup>		MIN	NOM	MAX	UNIT
Window material		Corning Eagle XG			
Window refractive index	at wavelength 546.1 nm	1.5119			
Window aperture <sup>(2)</sup>				See <sup>(2)</sup>	
Illumination overfill <sup>(3)</sup>				See <sup>(3)</sup>	
Window transmittance, single-pass through both surfaces and glass	Minimum within the wavelength range 420 to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
Window Transmittance, single-pass through both surfaces and glass	Average over the wavelength range 420 to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

(1) See [Section 7.5](#) for more information.

(2) See the package mechanical characteristics for details regarding the size and location of the window aperture.

(3) The active area of the DLP3310 device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to limit light flux incident outside the active array to less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.

## 6.13 Chipset Component Usage Specification

### Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

The DLP3310 is a component of one or more DLP® chipsets. Reliable function and operation of the DLP3310 requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices for operating or controlling a DLP DMD.

## 6.14 Software Requirements

### CAUTION

The DLP3310 DMD has mandatory software requirements. Refer to [Software Requirements for TI DLP®Pico™ TRP Digital Micromirror Devices](#) application report for additional information. Failure to use the specified software will result in failure at power up.

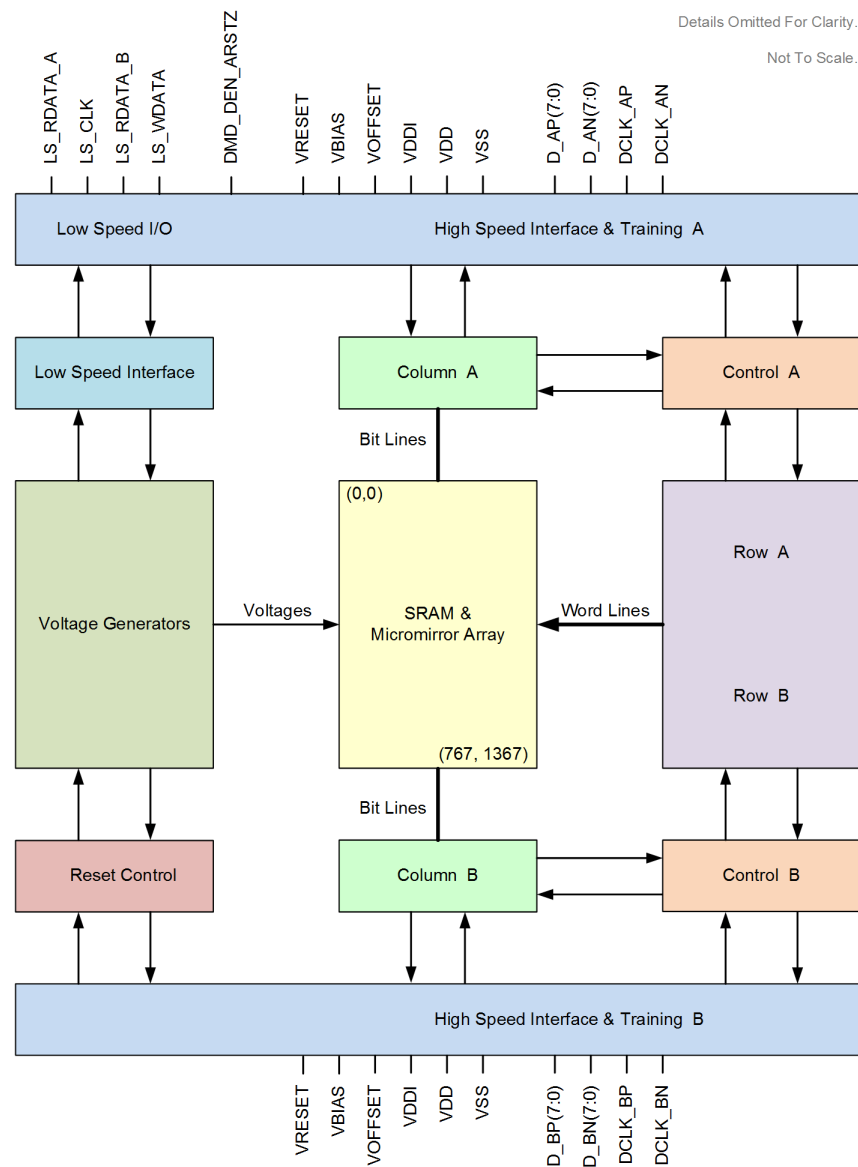
## 7 Detailed Description

### 7.1 Overview

The DLP3310 is a 0.33 inch diagonal spatial light modulator of aluminum micromirrors. Pixel array size is 1368 columns by 768 rows in a square grid pixel arrangement. The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display two distinct pixels on the screen during every frame, resulting in a full 1920 x 1080 pixel image being displayed. The electrical interface is Sub Low Voltage Differential Signaling (SubLVDS) data.

The DLP3310 is part of the chipset composed of the DLP3310 DMD, DLPC3437 controller, and DLPA3000/DLPA3005 PMIC/LED driver. To ensure reliable operation, the DLP3310 DMD must always be used with the DLPC3437 controller and the DLPA3000/DLPA3005 PMIC/LED drivers.

### 7.2 Functional Block Diagram



A. Details omitted for clarity.

## 7.3 Feature Description

### 7.3.1 Power Interface

The power management IC DLPA3000/DLPA3005 contains three regulated DC supplies for the DMD reset circuitry:  $V_{BIAS}$ ,  $V_{RESET}$ , and  $V_{OFFSET}$ , as well as the two regulated DC supplies for the DLPC3437 controller.

### 7.3.2 Low-Speed Interface

The Low Speed Interface handles instructions that configure the DMD and control reset operation. LS\_CLK is the low-speed clock, and LS\_WDATA is the low speed data input.

### 7.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs, with a dedicated clock.

### 7.3.4 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. [Figure 6-13](#) shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

## 7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC3437 controller. For more information, see the [DLPC3437 DLPC3437 Display Controller Data Sheet](#) or contact a TI applications engineer.

## 7.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

### 7.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and/or active area could occur.

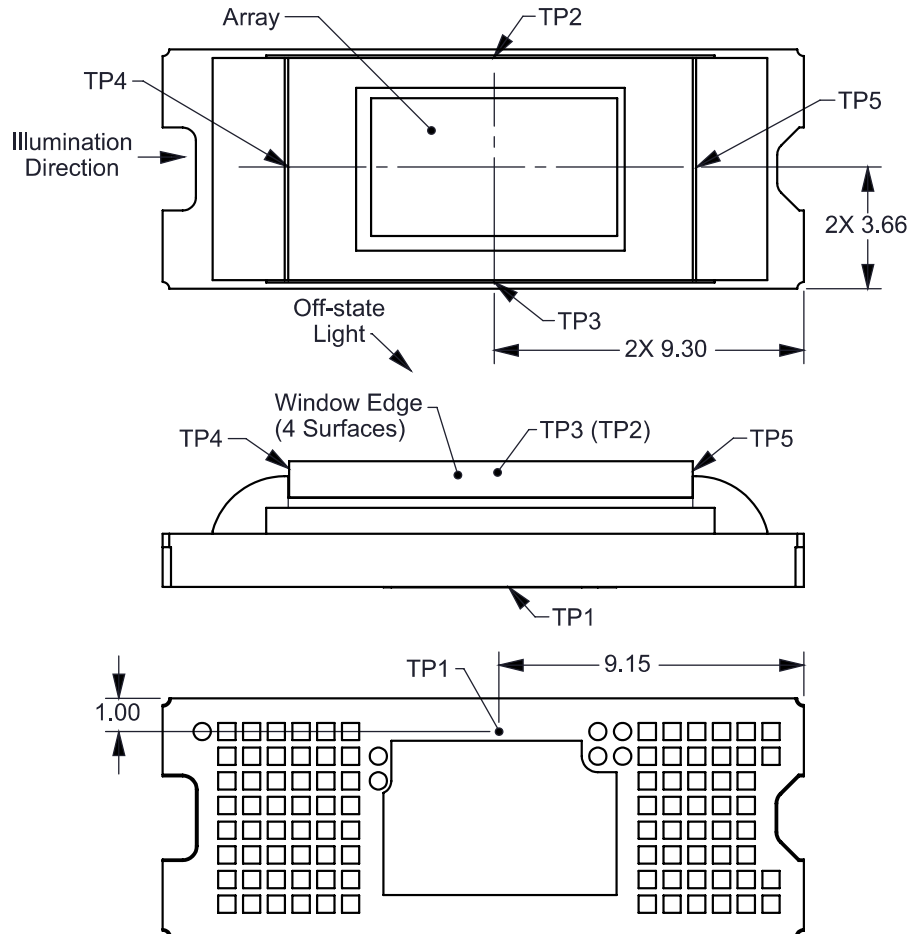
### 7.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

### 7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

### 7.6 Micromirror Array Temperature Calculation



**Figure 7-1. DMD Thermal Test Points**

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1 in [Figure 7-1](#)) is provided by the following equations:

$$T_{\text{ARRAY}} = T_{\text{CERAMIC}} + (Q_{\text{ARRAY}} \times R_{\text{ARRAY-TO-CERAMIC}})$$

$$Q_{\text{ARRAY}} = Q_{\text{ELECTRICAL}} + Q_{\text{ILLUMINATION}}$$

where

- $T_{\text{ARRAY}}$  = computed array temperature ( $^{\circ}\text{C}$ )
- $T_{\text{CERAMIC}}$  = measured ceramic temperature ( $^{\circ}\text{C}$ ) (TP1 location)
- $R_{\text{ARRAY-TO-CERAMIC}}$  = thermal resistance of package specified in [Thermal Information](#) from array to ceramic TP1 ( $^{\circ}\text{C}/\text{Watt}$ )
- $Q_{\text{ARRAY}}$  = Total (electrical + absorbed) DMD power on the array (Watts)
- $Q_{\text{ELECTRICAL}}$  = nominal electrical power
- $Q_{\text{ILLUMINATION}} = (C_{\text{L2W}} \times \text{SL})$
- $C_{\text{L2W}}$  = Conversion constant for screen lumens to power on DMD (Watts/Lumen)
- $\text{SL}$  = measured screen Lumens

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.16 Watts. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a 1-Chip DMD system with projection efficiency from the DMD to the screen of 87%.

The conversion constant  $C_{\text{L2W}}$  is calculated to be 0.00266 W/lm based on array characteristics. It assumes a spectral efficiency of 300 lumens/Watt for the projected light and illumination distribution of 83.7% on the active array, and 16.3% on the array border.

Sample calculations for typical projection application:

$$C_{\text{L2W}} = 0.00266 \text{ W/lm}$$

$$\text{SL} = 450 \text{ lm}$$

$$Q_{\text{ELECTRICAL}} = 0.16 \text{ W}$$

$$T_{\text{CERAMIC}} = 55.0^{\circ}\text{C}$$

$$Q_{\text{ARRAY}} = 0.16 \text{ W} + (0.00266 \text{ W/lm} \times 450 \text{ lm}) = 1.36 \text{ W}$$

$$T_{\text{ARRAY}} = 55.0^{\circ}\text{C} + (1.36 \text{ W} \times 6^{\circ}\text{C}/\text{W}) = 63.2^{\circ}\text{C}$$

## 7.7 Micromirror Landed-On/Landed-Off Duty Cycle

### 7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 75/25 indicates that the referenced pixel is in the ON state 75% of the time and in the OFF state 25% of the time, whereas 25/75 would indicate that the pixel is in the ON state 25% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) nominally add to 100.



### 7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

It is the symmetry and asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

### 7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in [Figure 6-1](#). The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD should be operated at for a given long-term average Landed Duty Cycle.

### 7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the nominal landed duty cycle of a given pixel is determined by the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience very close to a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel will experience very close to a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in [Table 7-1](#).

**Table 7-1. Grayscale  
Value and Landed Duty  
Cycle**

Grayscale Value	Nominal Landed Duty Cycle
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where "color cycle time" is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_}\% \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_}\% \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_}\% \times \text{Blue\_Scale\_Value}) \quad (1)$$

where

Red\_Cycle\_%, Green\_Cycle\_%, and Blue\_Cycle\_% represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point.

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities would be as shown in [Table 7-2](#).

**Table 7-2. Example Landed Duty Cycle for Full-Color Pixels**

Red Cycle Percentage	Green Cycle Percentage	Blue Cycle Percentage	
50%	20%	30%	

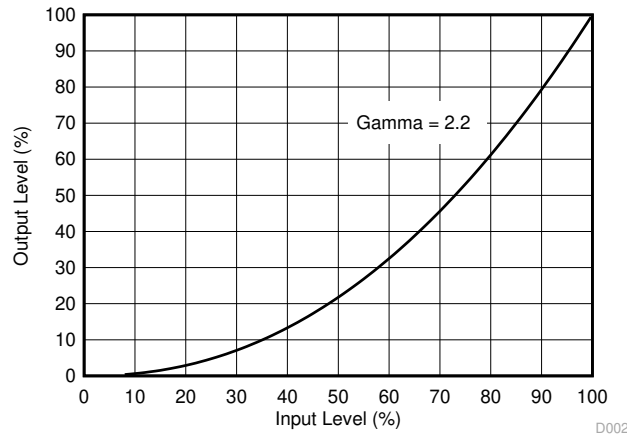
  

Red Scale Value	Green Scale Value	Blue Scale Value	Nominal Landed Duty Cycle
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the Landed Duty Cycle is any applied image processing. Within the DLP Controller DLPC3437, the two functions which affect Landed Duty Cycle are Gamma and IntelliBright™.

Gamma is a power function of the form  $\text{Output\_Level} = A \times \text{Input\_Level}^{\text{Gamma}}$ , where A is a scaling factor that is typically set to 1.

In the DLPC3430/DLPC3435 controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in [Figure 7-2](#).



**Figure 7-2. Example of Gamma = 2.2**

From [Figure 7-2](#), if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value will be 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

The IntelliBright algorithms content adaptive illumination control (CAIC) and local area brightness boost (LABB) also apply transform functions on the gray scale level of each pixel.

But while the amount of gamma applied to every pixel (of every frame) is constant (the exponent, gamma, is constant), CAIC and LABB are both adaptive functions that can apply a different amounts of either boost or compression to every pixel of every frame.

Consideration must also be given to any image processing which occurs before the DLPC3437 controller.

## 8 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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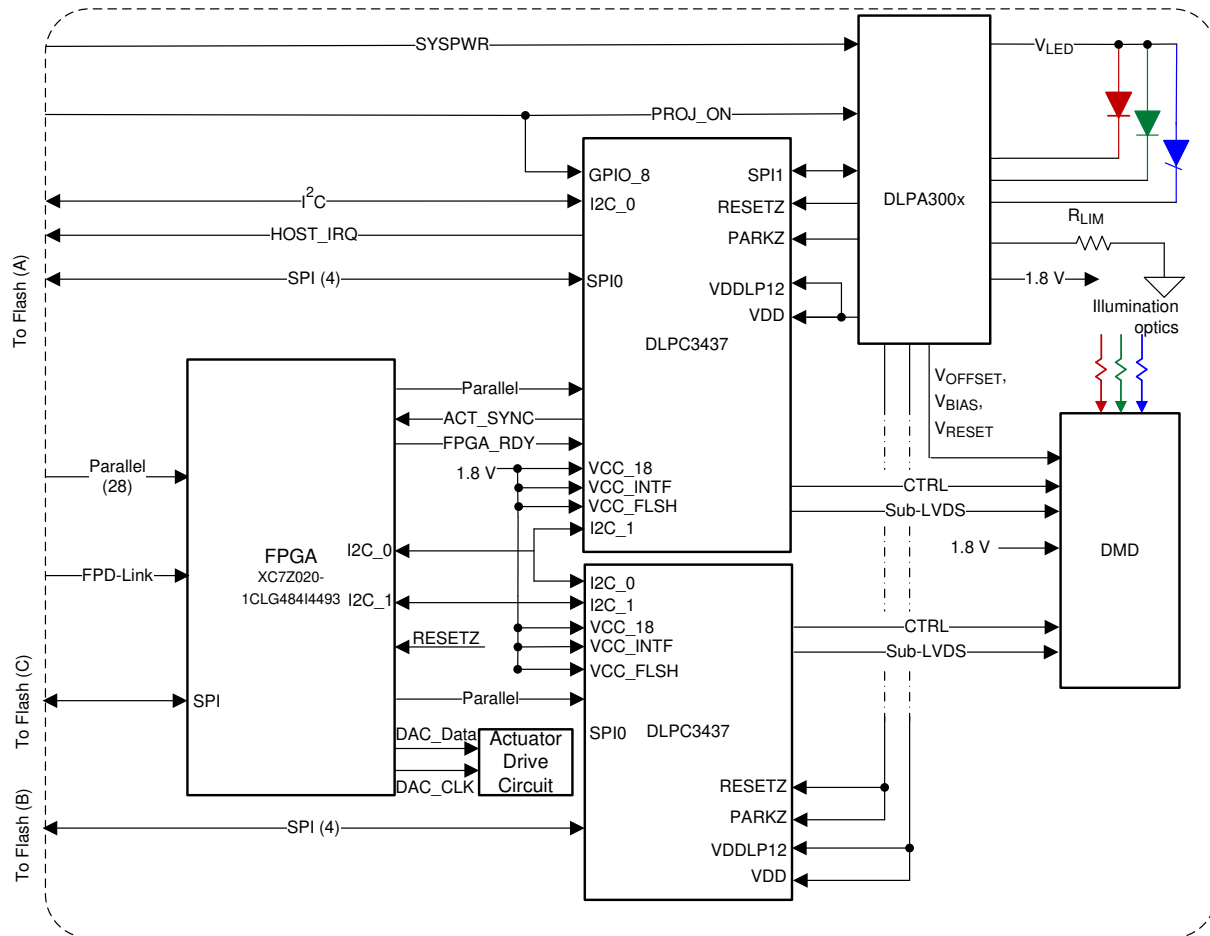
### 8.1 Application Information

The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the dual DLPC3437 controllers. The new high tilt pixel in the side-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness constrained applications. Applications of interest include projection embedded in display devices like battery powered mobile accessory full HD projectors, battery powered smart full HD projectors, digital signage, interactive surface projection, low latency gaming displays, interactive displays, and wearable displays.

DMD power-up and power-down sequencing is strictly controlled by the DLPA3000/DLPA3005. Refer to [Section 9](#) for power-up and power-down specifications. To ensure reliable operation, the DLP3310 DMD must always be used with two DLPC3437 controllers and a DLPA3000/DLPA3005 PMIC/LED driver.

### 8.2 Typical Application

A common application when using a DLP3310 DMD and two DLPC3437s is for creating a pico-projector that can be used as an accessory to a smartphone, tablet or a laptop. The two DLPC3437s in the pico-projector receive images from the XC7Z020-1CLG484I4493 FPGA, which receives images from a multimedia front end within the product as shown in [Figure 8-1](#).



**Figure 8-1. Typical Application Diagram**

### 8.2.1 Design Requirements

A pico-projector is created by using a DLP chip set comprised a DLP3310 DMD, two DLPC3437 controllers, a XC7Z020-1CLG484I4493 FPGA, and a DLPA3000/DLPA3005 PMIC/LED driver. The XC7Z020-1CLG484I4493 FPGA and DLPC3437 controllers do the digital image processing, the DLPA3000/DLPA3005 provides the needed analog functions for the projector, and the DLP3310 DMD is the display device for producing the projected image.

In addition to the three DLP chips in the chip set, other chips are needed. At a minimum a Flash part is needed to store the software and firmware to control the XC7Z020-1CLG484I4493 FPGA, and each of the DLPC3437 controllers.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector.

For connecting the XC7Z020-1CLG484I4493 FPGA to the multimedia front end for receiving images, either a 24-bit parallel interface can be used, or the dual FPD-Link interface can be used. An I<sup>2</sup>C interface should be connected from the multimedia front end for sending commands to one of the DLPC3437 controllers for configuring the chipset for different features.

### 8.2.2 Detailed Design Procedure

For connecting together the XC7Z020-1CLG484I4493 FPGA, the two DLPC3437 controllers, the DLPA3000/DLPA3005, and the DLP3310 DMD, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve a reliable projector.

The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

### 8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is as shown in [Figure 8-2](#). For the LED currents shown, it's assumed that the same current amplitude is applied to the red, green, and blue LEDs.

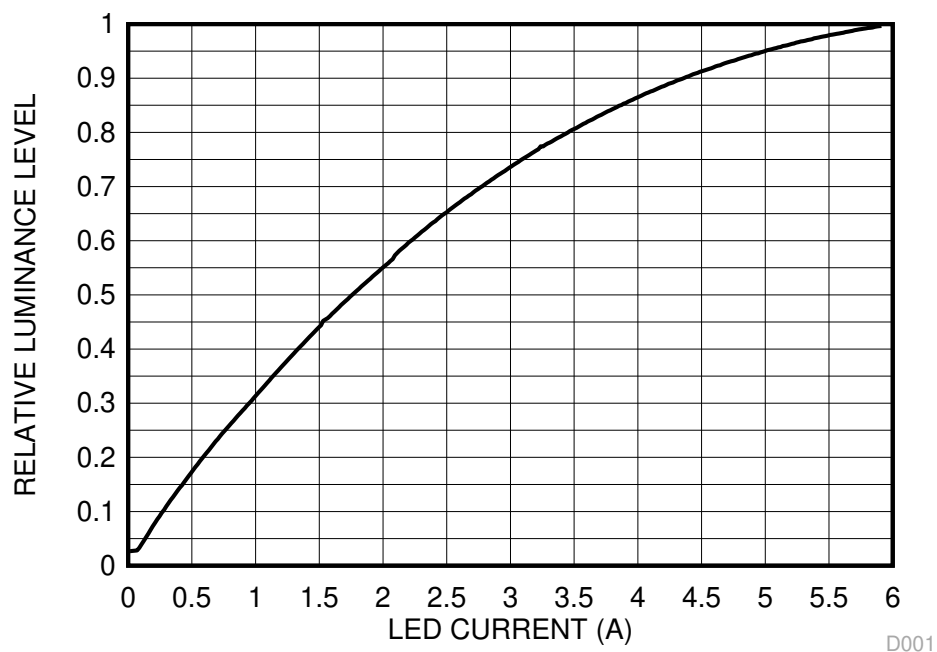


Figure 8-2. Luminance vs Current

D001

## 9 Power Supply Recommendations

The following power supplies are all required to operate the DMD:  $V_{DD}$ ,  $V_{DDI}$ ,  $V_{OFFSET}$ ,  $V_{BIAS}$ , and  $V_{RESET}$ . All  $V_{SS}$  connections are also required. DMD power-up and power-down sequencing is strictly controlled by the DLPA3000/DLPA3005 devices.

### CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.

$V_{DD}$ ,  $V_{DDI}$ ,  $V_{OFFSET}$ ,  $V_{BIAS}$ , and  $V_{RESET}$  power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to [Figure 9-2](#).  $V_{SS}$  must also be connected.

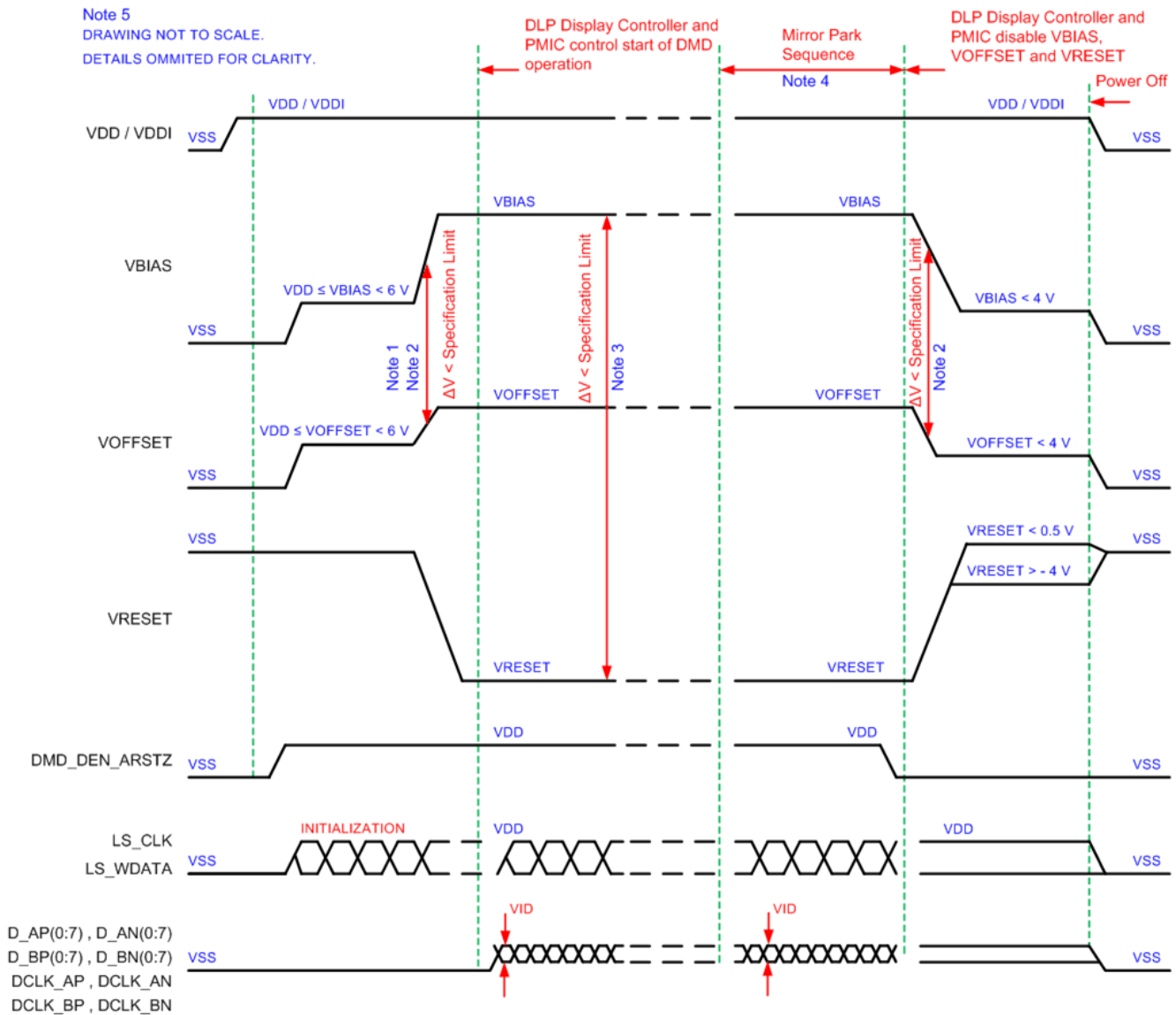
### 9.1 Power Supply Power-Up Procedure

- During power-up,  $V_{DD}$  and  $V_{DDI}$  must always start and settle before  $V_{OFFSET}$ ,  $V_{BIAS}$ , and  $V_{RESET}$  voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between  $V_{BIAS}$  and  $V_{OFFSET}$  must be within the specified limit shown in [Recommended Operating Conditions](#). Refer to [Table 9-1](#) and the [Layout Example](#) for power-up delay requirements.
- During power-up, the DMD's LPSDR input pins shall not be driven high until after  $V_{DD}$  and  $V_{DDI}$  have settled at operating voltage.
- During power-up, there is no requirement for the relative timing of  $V_{RESET}$  with respect to  $V_{OFFSET}$  and  $V_{BIAS}$ . Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed previously and in [Figure 9-1](#).

### 9.2 Power Supply Power-Down Procedure

- Power-down sequence is the reverse order of the previous power-up sequence.  $V_{DD}$  and  $V_{DDI}$  must be supplied until after  $V_{BIAS}$ ,  $V_{RESET}$ , and  $V_{OFFSET}$  are discharged to within 4 V of ground.
- During power-down, it is not mandatory to stop driving  $V_{BIAS}$  prior to  $V_{OFFSET}$ , but it is a strict requirement that the delta between  $V_{BIAS}$  and  $V_{OFFSET}$  must be within the specified limit shown in [Recommended Operating Conditions](#) (Refer to Note 2 for [Figure 9-1](#)).
- During power-down, the DMD's LPSDR input pins must be less than  $V_{DDI}$ , the specified limit shown in [Recommended Operating Conditions](#).
- During power-down, there is no requirement for the relative timing of  $V_{RESET}$  with respect to  $V_{OFFSET}$  and  $V_{BIAS}$ .
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed previously and in [Figure 9-1](#).

### 9.3 Power Supply Sequencing Requirements



- Refer to [Table 9-1](#) and [Figure 9-2](#) for critical power-up sequence delay requirements.
- To prevent excess current, the supply voltage delta  $|V_{BIAS} - V_{OFFSET}|$  must be less than specified in [Recommended Operating Conditions](#). OEMs may find that the most reliable way to ensure this is to power  $V_{OFFSET}$  prior to  $V_{BIAS}$  during power-up and to remove  $V_{BIAS}$  prior to  $V_{OFFSET}$  during power-down. Refer to [Table 9-1](#) and [Figure 9-2](#) for power-up delay requirements.
- To prevent excess current, the supply voltage delta  $|V_{BIAS} - V_{RESET}|$  must be less than specified limit shown in [Section 6.4](#).
- When system power is interrupted, the DLPA3000/DLPA3005 initiates hardware power-down that disables  $V_{BIAS}$ ,  $V_{RESET}$  and  $V_{OFFSET}$  after the Micromirror Park Sequence.
- Drawing is not to scale and details are omitted for clarity.

**Figure 9-1. Power Supply Sequencing Requirements (Power Up and Power Down)**

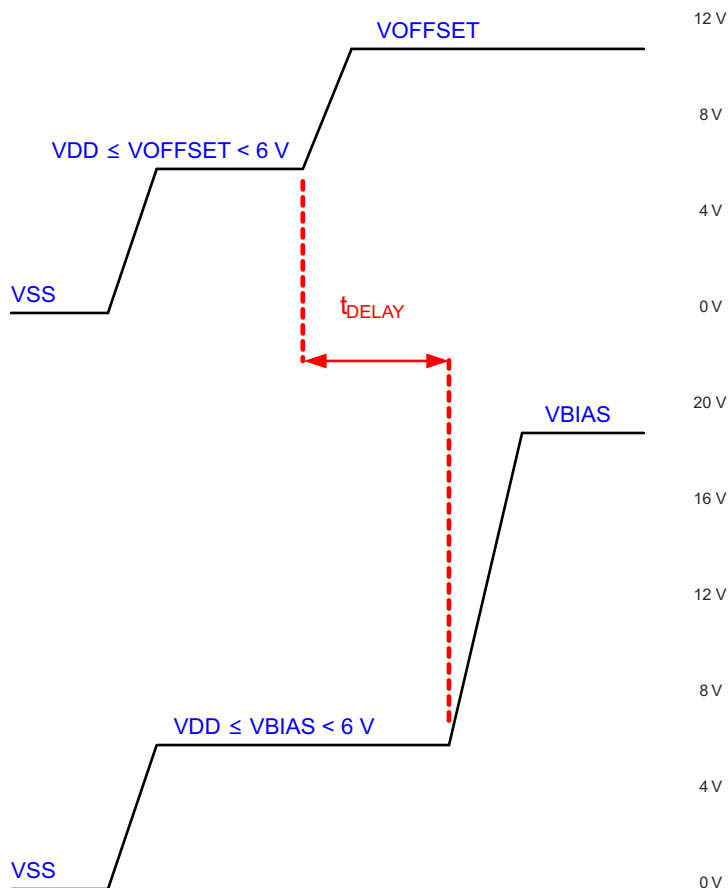
**Table 9-1. Power-Up Sequence Delay Requirement**

PARAMETER		MIN	MAX	UNIT
$t_{DELAY}$	Delay requirement from $V_{OFFSET}$ power up to $V_{BIAS}$ power up	2		ms
$V_{OFFSET}$	Supply voltage level at beginning of power-up sequence delay (see <a href="#">Figure 9-2</a> )		6	V



**Table 9-1. Power-Up Sequence Delay Requirement (continued)**

PARAMETER		MIN	MAX	UNIT
$V_{BIAS}$	Supply voltage level at end of power-up sequence delay (see Figure 9-2)		6	V



Refer to Table 9-1 for  $V_{OFFSET}$  and  $V_{BIAS}$  supply voltage levels during power-up sequence delay.

**Figure 9-2. Power-Up Sequence Delay Requirement**

## 10 Layout

### 10.1 Layout Guidelines

The DLP3310 DMD is connected to a PCB or a Flex circuit using an interposer. For additional layout guidelines regarding length matching, impedance, etc. see the DLPC3437 controller datasheet. For a detailed layout example refer to the layout design files. Some layout guidelines for routing to the DLP3310 DMD are:

- Match lengths for the LS\_WDATA and LS\_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer to [Figure 10-1](#).
- Minimum of two 220-nF (35 V) capacitors - one close to  $V_{BIAS}$  pin. Capacitors C10 and C14 in [Figure 10-1](#).
- Minimum of two 220-nF (35 V) capacitors - one close to each  $V_{RST}$  pin. Capacitors C11 and C13 in [Figure 10-1](#).
- Minimum of two 220-nF (35 V) capacitors - one close to each  $V_{OFS}$  pin. Capacitors C4 and C12 in [Figure 10-1](#).
- Minimum of four 220-nF (10 V) capacitors - two close to each side of the DMD. Capacitors C1, C3, C2, and C5 in [Figure 10-1](#).

### 10.2 Layout Example

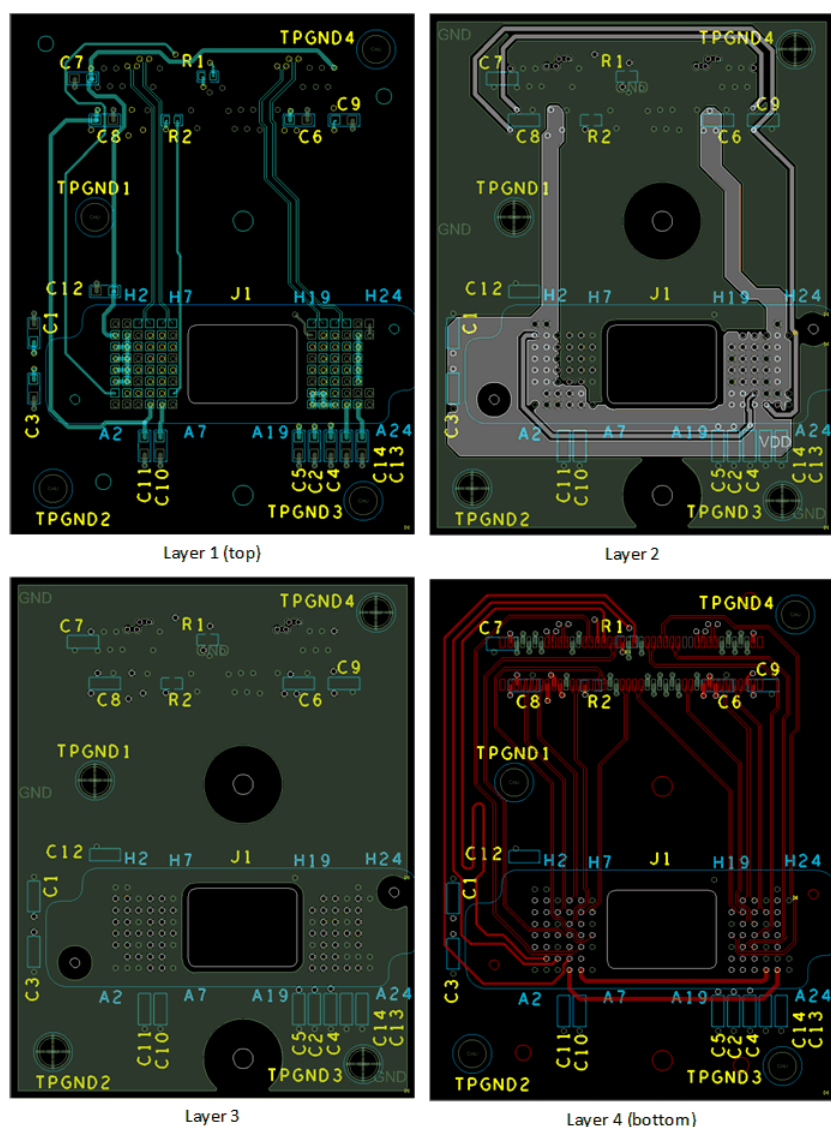


Figure 10-1. Power Supply Connections

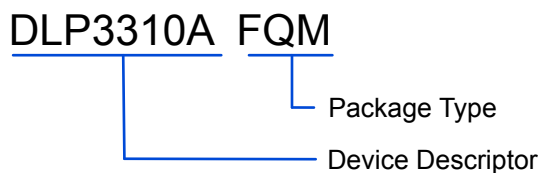
## 11 Device and Documentation Support

### 11.1 Third-Party Products Disclaimer

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### 11.2 Device Support

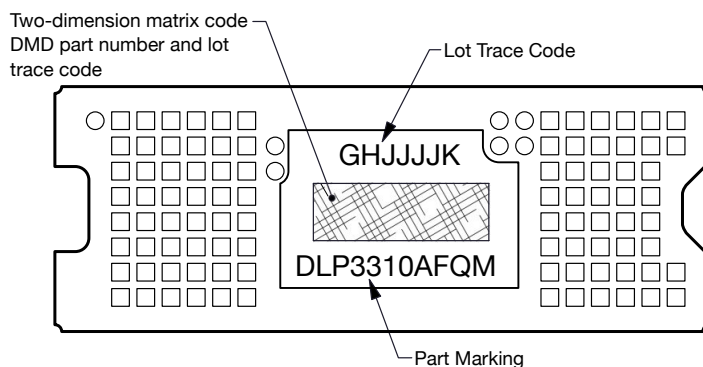
#### 11.2.1 Device Nomenclature



**Figure 11-1. Part Number Description**

#### 11.2.2 Device Markings

The device marking includes the legible character string GHJJJK DLP3310AFQM. GHJJJK is the lot trace code. DLP3310AFQM is the device marking.



**Figure 11-2. DMD Marking**

### 11.3 Documentation Support

#### 11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.5 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 11.6 Trademarks

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IntelliBright™ is a trademark of Texas Instruments.

DLP® is a registered trademark of Texas Instruments.

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### 11.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.8 Glossary

#### [TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

### 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP3310AFQM	ACTIVE	CLGA	FQM	92	100	RoHS & Green	NI/AU	N / A for Pkg Type			<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

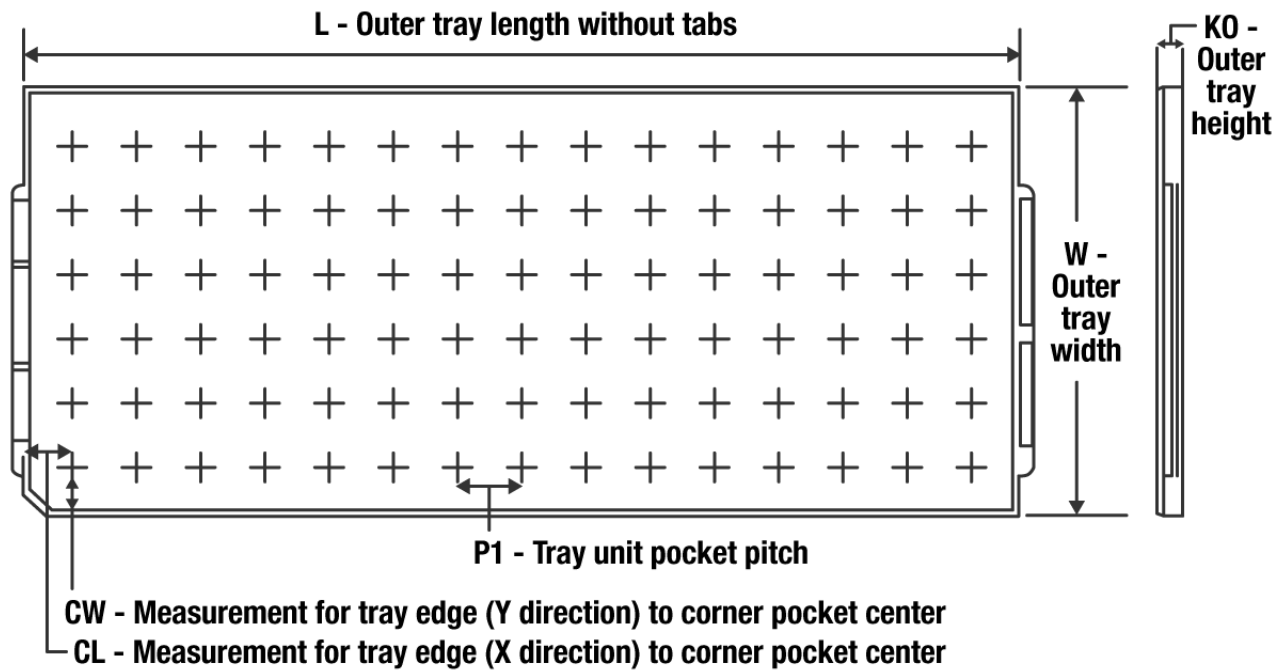
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
DLP3310AFQM	FQM	CLGA	92	100	10 x 10	150	315	135.9	12190	28	31.5	16.2



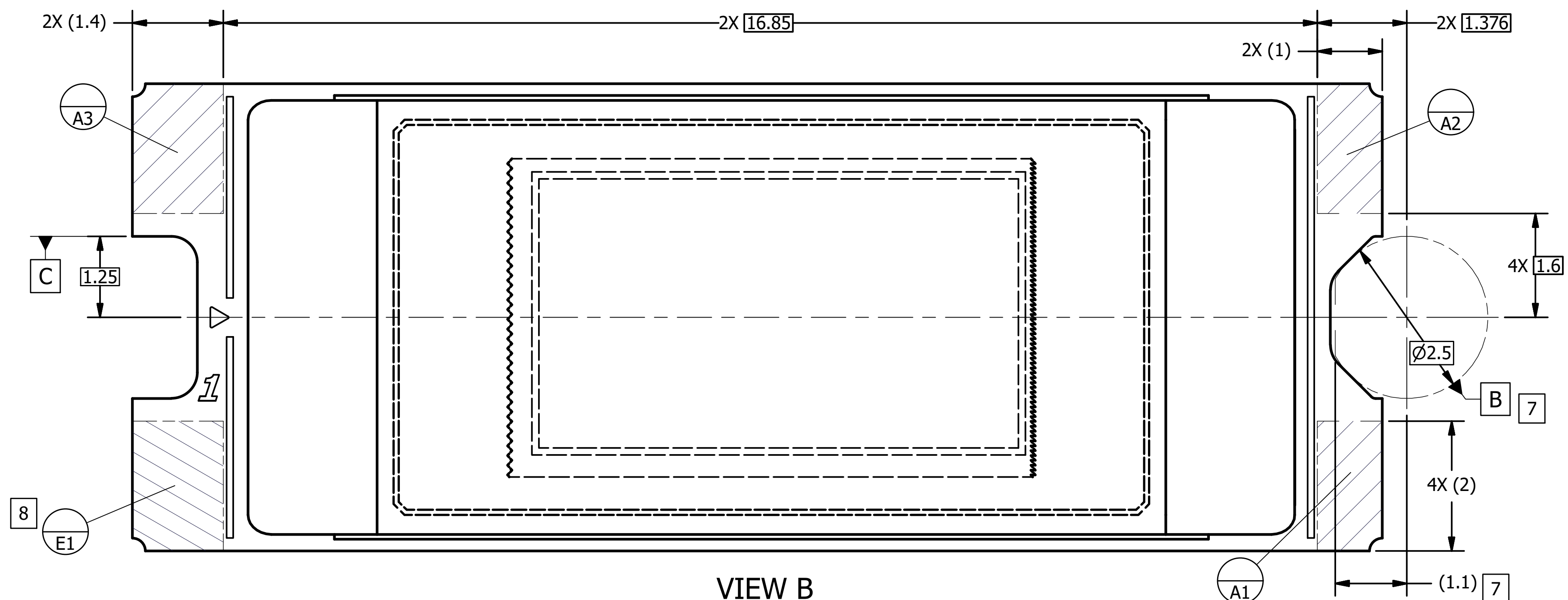


D

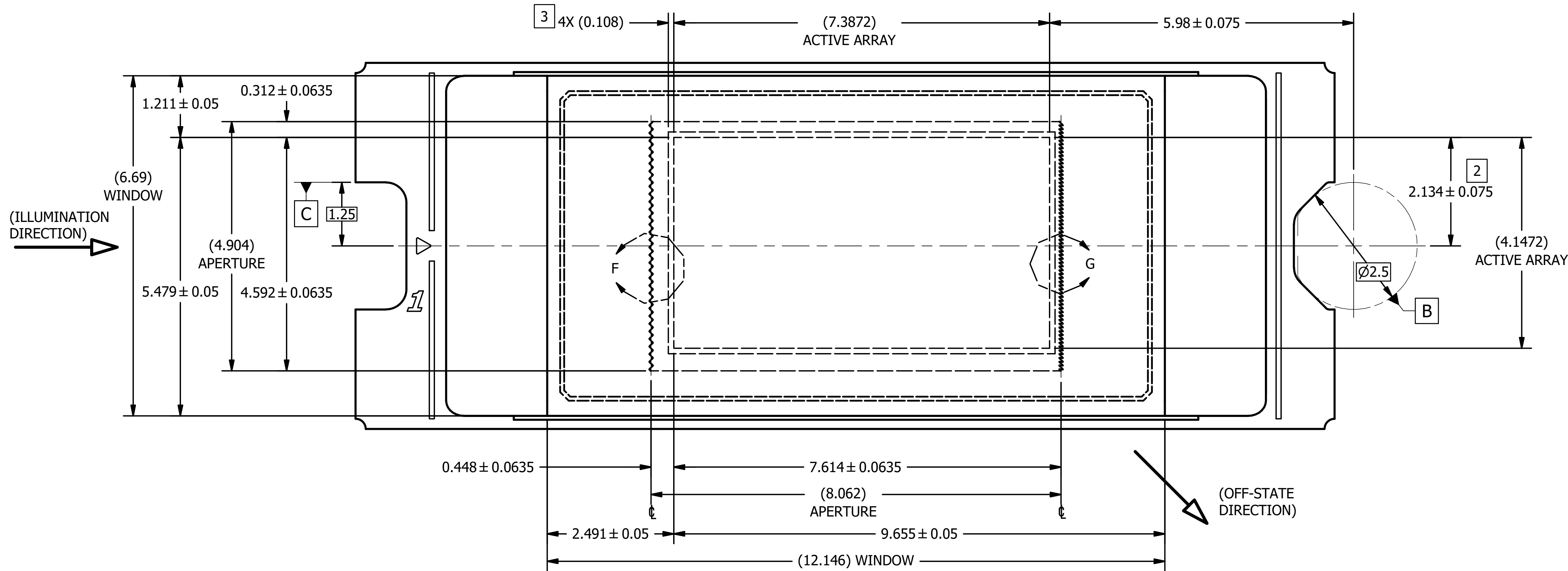
C

B

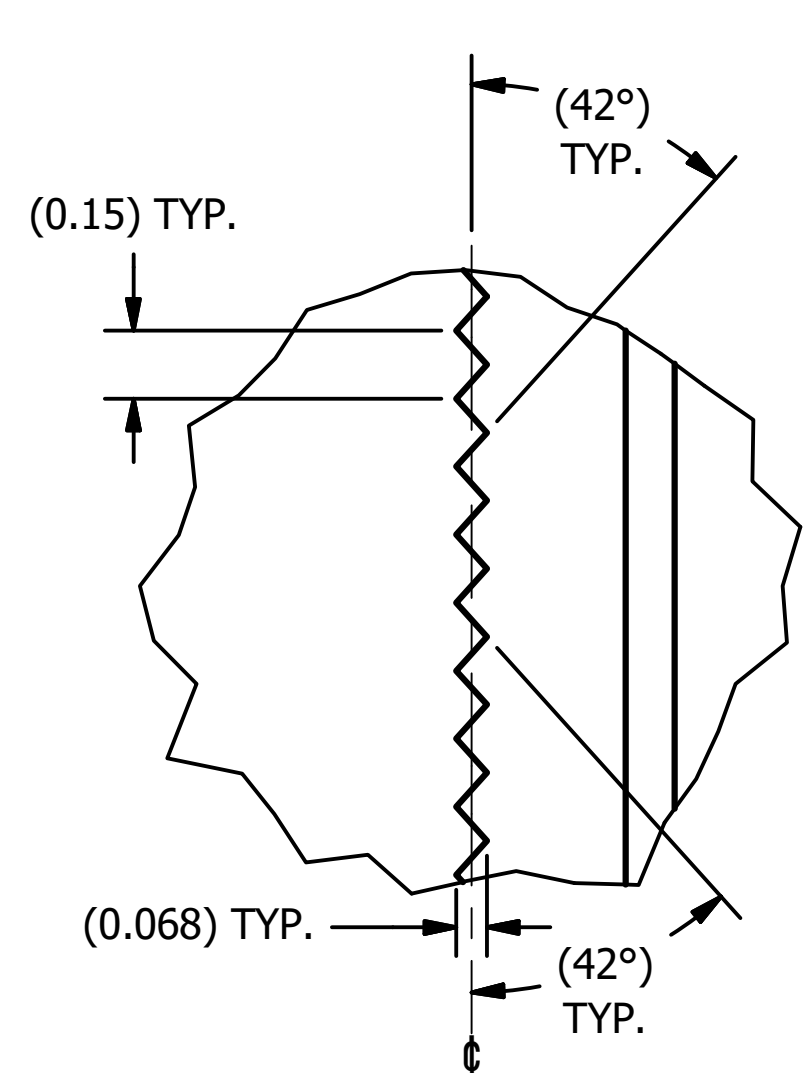
**A**



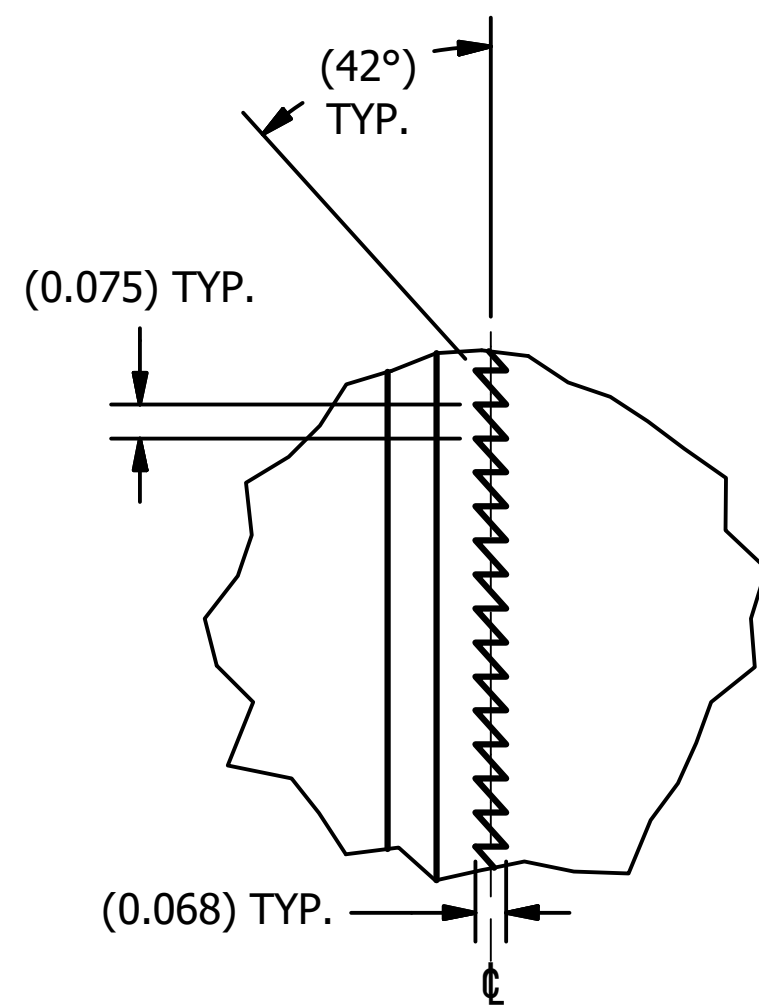




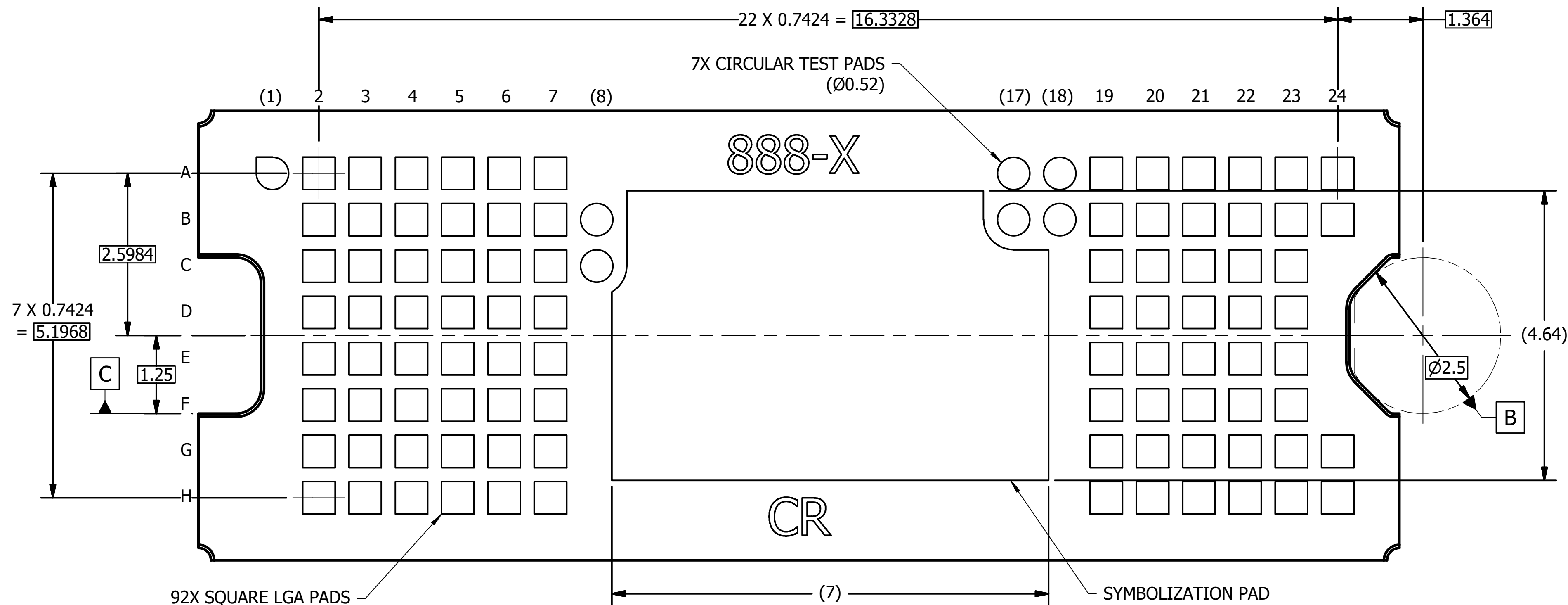
VIEW E  
WINDOW AND ACTIVE ARRAY  
(FROM SHEET 1)



DETAIL F  
APERTURE LEFT EDGE  
SCALE 60 : 1



DETAIL G  
APERTURE RIGHT EDGE  
SCALE 60 : 1



VIEW H-H  
BACK SIDE METALLIZATION  
(FROM SHEET 1)

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