DLP® Products Thermal Design Guide: Focus on High Power NIR Laser Illumination

Application Report

Literature Number: DLPA104
December 2018

Texas Instruments

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1 Trademarks

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Application Report
DLPA104–December 2018

DLP® High-Power NIR Thermal Design Guide

Scott Overmann

2 Introduction

DLP® technology is often used with high power illumination sources for high brightness displays as well as various industrial exposure equipment such as lithography systems, 3D printers, and laser marking machines to name a few. Managing the thermal specifications requires certain DMD temperature calculations. At higher power levels, important cooling techniques need to be incorporated to best control the DMD temperature to maximize performance over time. This application report explains key DMD temperature calculations and cooling best practices when integrating a DMD into a light engine design. The examples provided focus on high power NIR applications in the 950 – 1150 nm range with high incident power and high peak incident irradiance.

3 Digital Micromirror Device (DMD) Temperature Requirements

DLP® DMDs have been shipping commercially for over 20 years. Over the decades, TI has completed extensive amounts of DMD characterization predominantly for display use cases that span 0 – 70 °C array temperature operation. As a result, DMD performance has been found to be extremely robust over this relatively large operating temperature range. However, there is a relationship with extreme temperature conditions that leads to degraded performance. As a result, temperature limits are imposed on critical locations of the DMD for operating and storage conditions, which are specified in each product's datasheet.

3.1 Critical Locations for DMD Temperature Measurements

The critical locations that define the device temperature limits (see Figure 1) are the:

- array micromirrors (cannot be measured directly, must be calculated)
- window glass edges (TP2 – TP5 reference points)
- back of the package (TP1 reference point).

The temperature of the array micromirrors is controlled by conduction through the ceramic header and the heatsink that contacts the ceramic directly beneath the array.

The window glass is cooled primarily through conduction through a glass interposer to the silicon die. The glass window is attached to the glass interposer (spacer) to the silicon die with very thin epoxy bonds and therefore must be kept below specified temperatures to ensure package integrity is maintained.

The window glass temperature rise is primarily due to bulk absorption of the window glass and any absorbed heat load on the window aperture. Therefore, it is recommended that the illumination design be optimized so that direct light loading on the window aperture is eliminated since this will significantly impact window temperature.

For this application report we will use the DLP650LNIR DMD as the example for all subsequent calculations. Refer to the appropriate DMD datasheet for parameters used in the calculations. Figure 1 shows an image of the DLP650LNIR DMD along with the five reference test point (TP) locations for monitoring critical temperatures on the device.

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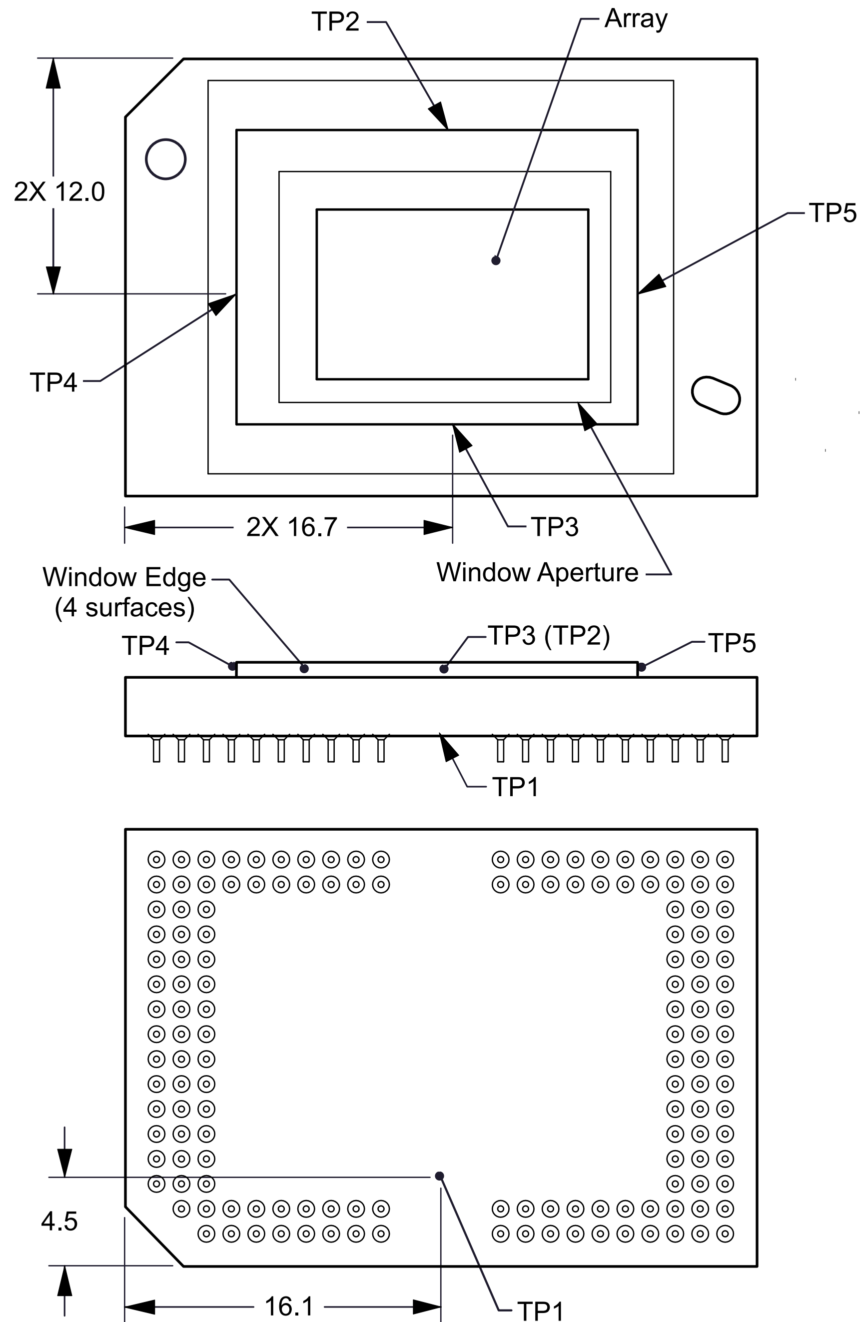

Figure 1. DMD thermal test points

External DMD temperature test points (TP1 – TP5) can be measured by attaching thermocouples to the DMD at locations shown in Figure 1. Recommended thermocouple wire types are T or K with fine gauge (36 gauge) wire. Thermocouple beads and exposed wire should be attached with glue such that the bead and exposed wire is in close contact with the surface being measured. Ultraviolet (UV) cure glue is an effective way to attach thermocouples to the DMD.

Window thermocouples (TP2 –TP5) can be read directly and compared to the appropriate datasheet specification.

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The DMD Micromirror temperature cannot be measured directly, therefore it must be computed analytically from:

- the measurement point on the outside of the package
- the silicon-to-ceramic thermal resistance
- the mirror-to-silicon thermal resistance
- the internally generated electrical power
- and the illumination heat load

The relationship between mirror temperature and the reference ceramic temperature (thermal test TP1 in Figure 1) is provided by the following equations:

$$T_{MIRROR} = T_{CERAMIC} + Delta_T_{SILICON\text{-}TO\text{-}CERAMIC} + Delta_T_{MIRROR\text{-}TO\text{-}SILICON}$$

$$Delta_T_{SILICON\text{-}TO\text{-}CERAMIC} = Q_{SILICON} \times R_{SILICON\text{-}TO\text{-}CERAMIC}$$

$$Delta_T_{MIRROR\text{-}TO\text{-}SILICON} = Q_{MIRROR} \times R_{MIRROR\text{-}TO\text{-}SILICON}$$

$$Q_{SILICON} = Q_{ELECTRICAL} + (\alpha_{DMD} \times Q_{INCIDENT})$$

$$Q_{MIRROR} = Q_{INCIDENT_MIRROR} \times [FF_{OFF\text{-}STATE_MIRROR} \times (1 - MR)] \quad (1)$$

$$\alpha_{DMD} = [FF_{OFF\text{-}STATE_MIRROR} \times (1\text{-}MR)] + [1\text{-}FF_{OFF\text{-}STATE\text{-}MIRROR}] + [2 \times \alpha_{WINDOW}] \quad (2)$$

where:

- T_{MIRROR} = computed micromirror temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature (°C) (TP1 location)
- $Delta_T_{SILICON\text{-}TO\text{-}CERAMIC}$ = temperature rise of silicon above ceramic test point TP1
- $Delta_T_{MIRROR\text{-}TO\text{-}SILICON}$ = temperature rise of an individual mirror above the silicon (°C)
- $R_{SILICON\text{-}TO\text{-}CERAMIC}$ = thermal resistance, silicon die to ceramic TP1 (°C/Watt) as specified in the data sheet
- $R_{MIRROR\text{-}TO\text{-}SILICON}$ = thermal resistance, individual mirror to silicon die (°C/Watt) as specified in the data sheet
- $Q_{SILICON}$ = total DMD power (electrical + absorbed) on the silicon (Watts)
- Q_{MIRROR} = absorbed heat load on a single mirror (Watts)
- $Q_{ELECTRICAL}$ = nominal electrical power (Watts)
- $Q_{INCIDENT}$ = total incident optical power to DMD (Watts)
- $Q_{INCIDENT_MIRROR}$ = Incident optical power on an individual mirror (Watts)
- α_{DMD} = absorptivity of DMD
- α_{WINDOW} = absorptivity of DMD window (single pass)
- $FF_{OFF\text{-}STATE\text{-}MIRROR}$ = DMD off-state mirror fill factor
- MR = DMD mirror reflectivity

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a system operating at 1064 nm with 100% of the illumination contained within the 1280 × 800 active array mirrors. Silicon-to-ceramic thermal resistance assumes the entire active micromirror array is uniformly illuminated.

NOTE: Incident irradiation that concentrates on a subset of the micromirror array, results in an increase in effective package thermal resistance.

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3.1.1 Sample Calculation 1 - Uniform illumination of entire DMD active array

This calculation assumes that the entire DMD active array (1280 × 800) mirrors is uniformly illuminated with zero overfill falling outside the Pond of Mirrors pixel border. The highest DMD temperatures typically occur when the DMD mirrors are in the off-state (–12° landed) position. Therefore, the off-state fill factor calculates the worst case mirror temperature. Calculate the mirror temperatures to assess the viability of the illumination conditions.

- $FF_{OFF\text{-}STATE\text{-}MIRROR}$ = 75.3%
- MR @ 1064 nm = 94%
- α_{WINDOW} @ 1064 nm = 0.7%
- $R_{MIRROR\text{-}TO\text{-}SILICON}$ = 3.39E5 °C/Watt
- $R_{SILICON\text{-}TO\text{-}CERAMIC}$ = 0.5 °C/Watt
- Array Resolution = 1280 × 800
- $T_{CERAMIC}$ = 30.0°C (measured)
- $Q_{INCIDENT}$ = 160 W (measured)
- $Q_{ELECTRICAL}$ = 1.8 W

α_{DMD} = [0.753 × (1-0.94)] + (1 - 0.753) + (2 × 0.007) = 0.31

$Q_{SILICON}$ = 1.8 W + (0.31 × 160 W) = 51.4 W

Q_{MIRROR} = [(160W / (1280 × 800)] × 0.753 × (1 - 0.94) = 7.06E-6 W

$Delta_T_{SILICON\text{-}TO\text{-}CERAMIC}$ = 51.4 W × 0.5°C/W= 25.7°C

$Delta_T_{MIRROR\text{-}TO\text{-}SILICON}$ = 7.06E-6 W × 3.39E5 °C/W= 2.4°C

T_{MIRROR} = 30.0°C + 25.7 + 2.4°C = **58.1°C**

3.1.2 Sample Calculation 2 – Partial DMD active array illumination with non-uniform illumination peak:

This calculation assumes that only a subsection of the DMD active array 960 × 475 pixels in size is (non-uniformly) illuminated. This calculation assumes the illuminated area is in the center of the DMD. Non-centered area can affect the value of $R_{SILICON\text{-}TO\text{-}CERAMIC}$. If the application requires offsetting the illumination on the DMD, contact TI for more information on how to assess $R_{SILICON\text{-}TO\text{-}CERAMIC}$. As in Sample Calculation 1, the off-state fill factor can be used to assess the highest temperatures that can occur. Calculate the mirror temperatures which occur at the highest illumination intensities to assess the viability of the illumination conditions.

- $FF_{OFF\text{-}STATE\text{-}MIRROR}$ = 75.3%
- MR @ 1064 nm = 94%
- α_{WINDOW} @ 1064 nm = 0.7%
- $R_{MIRROR\text{-}TO\text{-}SILICON}$ = 3.39E5 °C/Watt
- $R_{SILICON\text{-}TO\text{-}CERAMIC}$ = 0.9 °C/Watt (higher than previous example due to reduced illumination area)
- Pixel Size = 10.8 µm = 0.00108 cm (square)
- $T_{CERAMIC}$ = 30.0°C (measured)
- $Q_{INCIDENT}$ = 60 W (measured)
- $Q_{ELECTRICAL}$ = 1.8 W
- Peak Irradiance = 500 W/cm^2 (measured)

α_{DMD} = [0.753 × (1 - 0.94)] + (1 - 0.753) + (2 × 0.007) = 0.31

$Q_{SILICON}$ = 1.8 W + (0.31 × 60 W) =20.4 W

$Q_{INCIDENT_MIRROR}$ = Peak Irradiance (W/cm^2) × Pixel Area (cm^2) = [500 W/cm^2 × (0.00108 cm)^2] = 5.832E-4 W

Q_{MIRROR} = 5.832E-4 W × 0.753 × (1 - 0.94) = 2.64E-5 W

$Delta_T_{SILICON\text{-}TO\text{-}CERAMIC}$ = 20.4 W × 0.9°C/W = 18.4°C

$Delta_T_{MIRROR\text{-}TO\text{-}SILICON}$ = 2.64E-5 W × 3.39E5°C/W= 8.9°C

T_{MIRROR} = 30.0°C + 18.4°C + 8.9°C = **57.3°C**

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4 Determining DMD Heat Loads

Properly assessing the heat load on the DMD is critical to determining device temperatures and meeting thermal requirements. Knowing how the heat load is distributed on the package is necessary to accurately assess critical temperatures. Optical modeling can be used to predict the illumination light distribution on the active array and aids in computing the spatial distribution of the thermal load. Thermal load due to the electrical dissipation of the silicon die can be obtained from the appropriate device datasheet.

4.1 Absorbed thermal load on active micromirror array and pond of mirrors (POM)

Light incident to the active micromirror array falls on both the micromirror surface and in the gaps between the micromirrors. Light incident on micromirrors is absorbed at a rate of (1 – mirror reflectivity). The DMD micromirror surface has reflectivity similar to that of polished bulk aluminum. Light falling on the gaps between the mirrors lands on the top of the silicon die which is intentionally designed to absorb most of the light. Fill factor determines the percentage of light on the micromirror surface versus the mirror gaps. The fill factor value is a function of several variables including pixel pitch, mirror state (on or off), illumination angle, and f-number (f/#). When designing a system, it is recommended to consider the worst case or lowest pixel fill factor condition, which is mirrors in the off-state when viewed from the illumination pupil.

The heat loads on the DMD silicon, mirror, and mirror gap are determined from the following:

$Q_{SILICON} = Q_{ELECTRICAL} + Q_{MIRROR} + Q_{MIRROR_GAPS}$

$Q_{MIRROR} = Q_{INCIDENT} \times$ (off-state mirror fill factor $\times$ (1 – mirror reflectivity))

$Q_{MIRROR_GAPS} = Q_{INCIDENT} \times$ (1 – off-state mirror fill factor)

The DMD has a region of mirrors outside of the active array approximately 10 pixels wide that are only addressable to the off-state. This region is called the Pond of Mirrors (POM) (see Figure 2). From a thermal standpoint, POM mirrors can be treated like active array mirrors in the off-state.

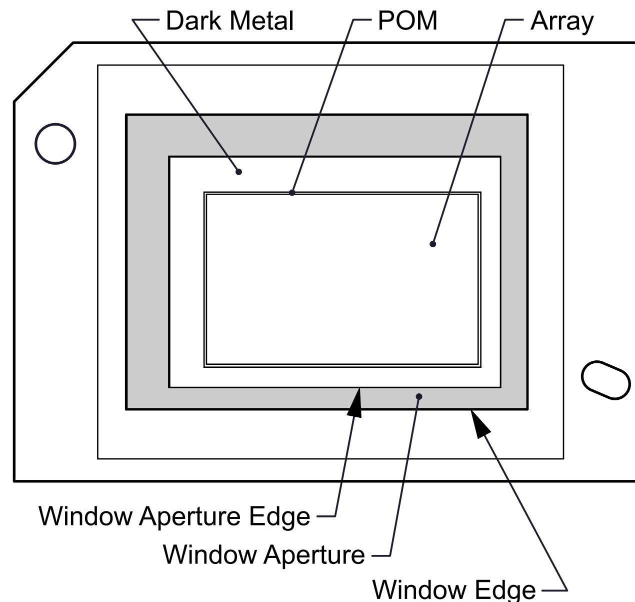

Figure 2. Active Array, POM, Dark Metal, Window Aperture

4.2 Absorbed load on DMD dark metal area and window aperture

A dark metal area exists outside of the POM on a DMD (see Figure 2). The dark metal area is specifically designed to be dark in visible applications and therefore has highly absorptive properties. It is recommended that there be no illumination load on the dark metal area since the absorption will be near 100% and will cause significant heating to the DMD with no benefit to system optical power output. For this reason, it is recommended to slightly under fill the active array so that significant illumination loads are not incident on the dark metal area.

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The DMD also has a dark aperture on the inside of the window glass. This aperture material is also highly absorptive and has a high thermal resistance path to the back of the DMD where a heatsink would be attached. Similar to the dark metal area, it is critical that significant incident light does not fall on the window aperture. If it does, window heating will occur, due to the intense light load and relatively poor thermal path, without providing any benefit to system optical power output.

4.3 Absorbed load in the window glass and forced air window cooling

The DMD window has both reflective and absorptive losses that are wavelength dependent. In the case of the DLP650LNIR at 1064 nm, the absorbed load in the window is nominally 0.7% per pass. This results in window heating that is significant at higher incident power levels.

For higher incident power levels, forced air cooling of the window is required to reduce window temperature and ensure reliable operation of the DLP650LNIR DMD. Forced air window cooling can be accomplished with an air stream from a simple blower-type fan ducted over the front of the window, or clean dry air that may already be available within the system. Since the window glass has relatively low thermal conductivity, but significant surface area, a relatively low flowrate of air provides substantial window cooling.

Please refer to the DLP650LNIR datasheet for incident power and irradiance levels requiring forced air window cooling as well as specific airflow details.

4.4 Dump light heat load and diffraction losses

When the DMD mirrors are in the off-state, incident light not absorbed by the DMD will be directed out of the DMD but not through the projection optics. A dump light absorber is normally used to capture this light. Since the dump light absorber and DMD are usually in close proximity, the dump light absorber should be cooled properly such that parasitic heat conduction from the absorber to the DMD is minimized. The dump light absorber may benefit from liquid cooling or forced airflow from a blower or fan since the heat load on this component will likely be substantial.

The DMD also has diffractive light losses that will not necessarily be directed to the dump light absorber. It is important to consider the location and impact of these optical diffraction orders as their heat loads can be concentrated and potentially cause thermal damage to other parts of the system.

5 DMD thermal resistances

5.1 Silicon-to-Ceramic Thermal Resistance

The silicon-to-ceramic thermal resistance depends on DMD geometry, array size, die attach material, and ceramic header. It is also a function of the heat input area which results in the silicon-to-ceramic thermal resistance increasing when a subset of the array mirrors are illuminated. Thermal resistance provided in the DMD datasheet assumes uniform illumination across the entire active micromirror array surface.

5.2 Mirror-to-Silicon Thermal Resistance

The mirror-to-silicon thermal resistance is the thermal resistance from the micromirror surface to the top of the silicon die. Primary cooling paths include the air gap between the mirror and top of silicon and the metal conductive paths of the micromirrors. This resistance is dependent upon pixel size. DMD datasheets provide mirror-to-silicon thermal resistance.

5.3 System Mounting Interface

The DMD package mounting interface to the system can have a significant effect on the overall cooling of the device. The typical interface consists of an optical housing on the window side and an electrical socket on the back side that connects to an electronics board. Depending on the temperature of these parts relative to the DMD, they act as either a heat sink or a source. If the optical housing and electronics board are cooler than the DMD, then these parts act as heat sinks and will provide some additional cooling benefit beyond the dedicated heatsink. However, sometimes these parts are hotter than the DMD and thermally isolating them from the DMD is preferred.

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A detailed thermal-resistance network of the DMD cooling paths is shown in Figure 3. A simplified thermal-resistance that is defined from the device ceramic test point (TP1) to the external room ambient is shown in Figure 4 below. This simplified resistance is termed the DMD system resistance (R_{sys}) and includes all heat-transfer paths to and from the device. The value of the system resistance (R_{sys}) is that it can be measured easily and used to gauge the effectiveness of the DMD cooling design.

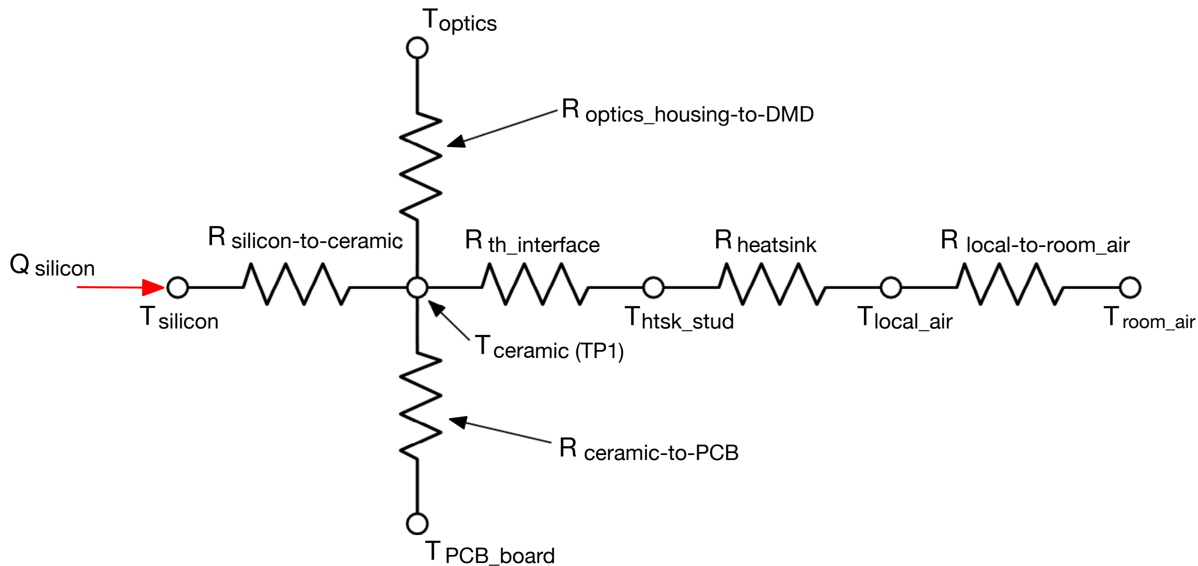
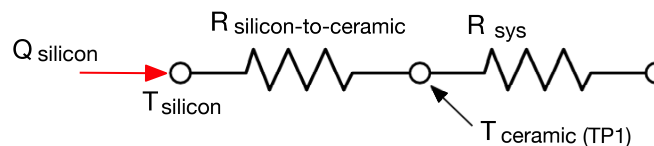


Figure 3. DMD Thermal-Resistance Network



$$R_{sys} = \frac{T_{ceramic} - T_{room_air}}{Q_{silicon}}$$

Figure 4. Simplified DMD Thermal-Resistance Network

5.4 Thermal Interface Resistance

The DMD has a dedicated thermal interface area. Contact to this area with a thermal stud should be maximized to reduce interface resistance. A low thermal resistance interface between the DMD ceramic and attached heatsink stud is critical since it is part of the overall system thermal resistance. Assuming 18.9 x 11.4 mm interface area and thermal grease with a 3 W/m-K thermal conductivity and thickness of 50 µm results in an interface thermal resistance of 0.08 ºC/W.

5.5 DMD Heatsink Resistance

Most applications requiring high power illumination will require a high performance heat sink solution to meet the temperature specification of the DMD. Typical high performance heatsink options include:

- liquid-cooled loops with a cooling stud
- heat pipe assisted heatsinks with an attached fan

In both cases, the liquid loop or the heatpipe only serves to transfer heat from one location to another. Ultimately finned or radiator surface areas are required to reduce heatsink thermal resistance.

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Returning to the DLP650LNIR example of 160W incident power, the calculated total DMD load was 51.4W. Temperature rise through the DMD package was 25.7ºC and additional temperature rise from mirror-to-silicon was 2.4ºC. To maintain an array temperature of 70ºC, the back of the package must be kept at 41.9ºC. Assuming a 20ºC room ambient, this requires a system heatsink resistance of:

R_sys = (41.9ºC – 20ºC) / 51.4 W = 0.43 ºC/W

This resistance includes the thermal interface to the DMD and also any preheating of air that may occur from room ambient temperature to inside a product. However, if a high performance thermal interface material such as a good thermal grease is used, and fresh air is brought in directly from outside the product, then this resistance could be achieved either with a heat pipe heatsink assembly with a fan or with a liquid cooling system.

Figure 5 provides an estimate of heatsink size versus thermal resistance. A 0.35 ºC/W heatsink with an additional 0.08 ºC/W thermal grease interface resistance would achieve the required 0.43 ºC/W in the equation above. It would have a finned volume of approximately 400 cm^3. An example of a heatsink with this resistance is shown in Figure 6.

Passive liquid cooling systems can achieve low heatsink thermal resistance. Active liquid cooling systems have the potential to maintain the heatsink stud at room temperature resulting in a 0 ºC/W heatsink thermal resistance. Care should be taken if heatsink temperatures below ambient air temperature are used because there is risk of condensation if any part of the system is cooler than the dew point of the surrounding air.

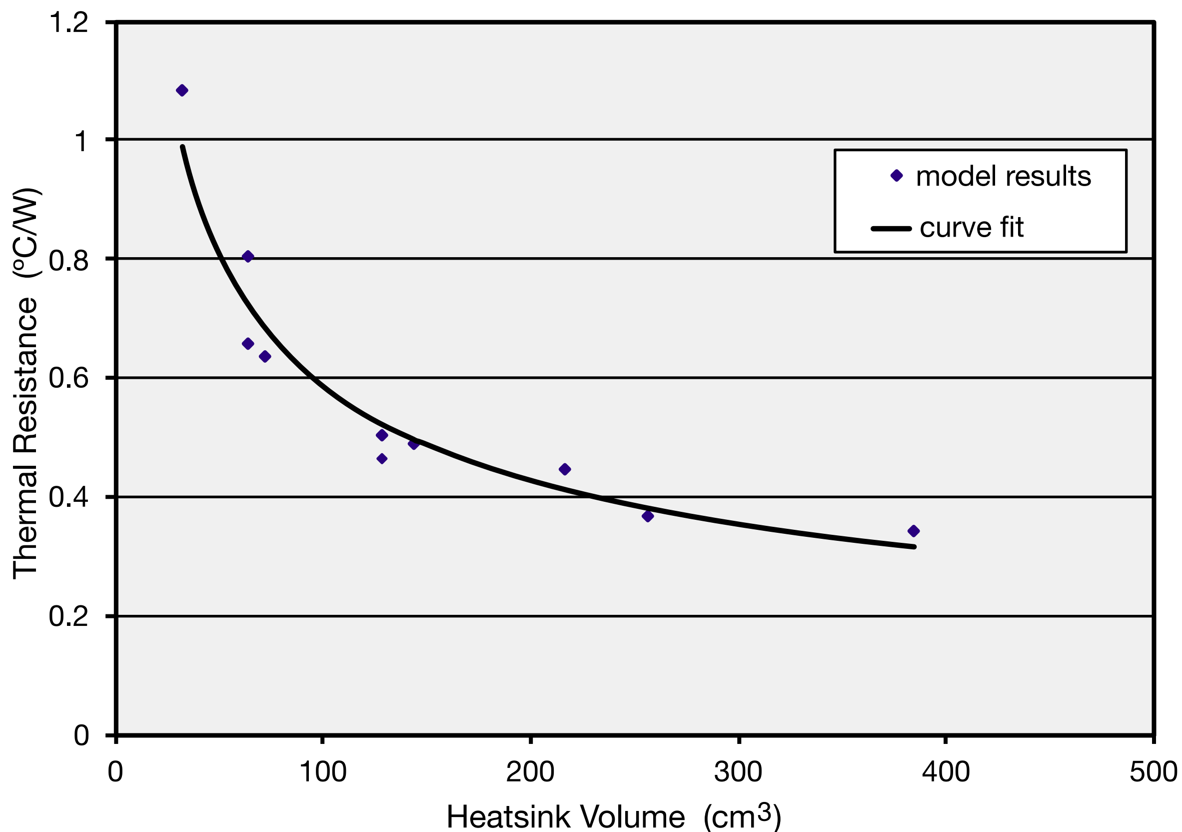

Figure 5. Heat pipe/heatsink and fan thermal resistance vs. heatsink volume

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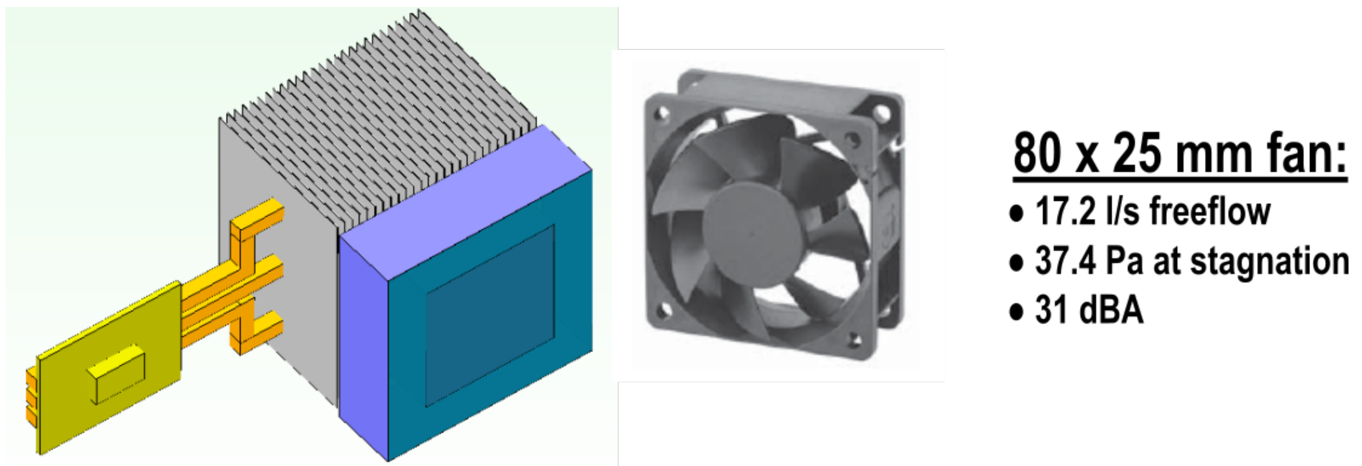

Figure 6. 8 x 8 x 6 cm (384 cm³) heatpipe heatsink with three 6 mm diameter copper water heatpipes and aluminum fins with 80 x 25 mm fan, 0.35 ºC/W thermal resistance (not including thermal grease interface material)

6 Other design considerations and precautions

6.1 Overfill

Controlling the illumination bundle close to the active array size is important to achieving acceptable DMD temperatures. In the case of DLP650LNIR, if optical overfill extends past the 10 pixel POM significant heating will occur since the region outside of the POM is highly absorptive. This will contribute to overall DMD heat load as mentioned earlier. If the illumination bundle is significantly smaller than the 1280 x 800 active array, then the package thermal resistance, Rsilicon-to-ceramic will increase. It is therefore recommended that the 1280 x 800 pixel array be slightly optically under filled to achieve the best thermal performance.

As mentioned earlier, any significant illumination incident on the window aperture can cause substantial window heating. Overfill that extends to the window aperture should be avoided. Stray light that is not part of the primary illumination bundle should also be considered to ensure that very little light is incident on the window aperture.

6.2 Optimal wavelengths

The window transmittance of each DMD depends on the window properties as well as the illumination wavelength being used in a system design. The application note Wavelength Transmittance Considerations for DLP® DMD Window is a good reference for determining DMD window efficiency values for a given wavelength.

The DLP650LNIR DMD is optimized for operation between 950 and 1150 nm. The datasheet explains it has operating capability beyond this range but at lower power levels. Designers must factor in that lower window efficiency in these extended ranges leads to increased heat absorption levels. Care should be taken to ensure all temperature specifications and performance goals are met depending on the desired operating wavelength.

6.3 Illumination uniformity

From a thermal design perspective, the ideal illumination profile across the DMD would be spatially uniform and resemble a “top hat” profile. For applications that have non-uniform illumination, the mirror-to-silicon temperature rise must be calculated based on the highest irradiance or peak intensity. This is because DMD micromirrors are small and the temperature rise of each mirror above the silicon temperature is dependent upon the absorbed heat load of that mirror.

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6.4 Pulsed lasers

The thermal time constant of a 10.8 µm DMD micromirror is very short, on the order of ~30 µs. Therefore, pulsed lasers with low average power but very high peak power can possibly damage the micromirrors since the thermal mass of an individual mirror is low and heating will occur rapidly.

7 Summary

Several thermal considerations must be managed when designing DLP systems using high power illumination. These include determining heat loads, controlling illumination to minimize light outside the active array, minimizing heatsink and thermal interface resistances, and measuring critical temperatures in the system. Equations are provided for designers to perform thermal calculations to ensure the DMD is kept within specified temperature ranges. An example is shown demonstrating that cooling of a 160W incident power system is achievable while maintaining DMD temperature specifications.

8 Related Documents

- DLPS136 DLP650LNIR Data Sheet
- DLPA015 DLP® Series-450 DMD and System Mounting Concepts
- DLPA067 Mounting Hardware and Quick Reference Guide for DLP® Advanced Light Control Digital Micromirror Devices
- DLPA031 Wavelength Transmittance Considerations for DLP® DMD Window

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