Application Report
DLPA092–January 2018

DLPC910, DLPR910A - Advised Continuous Row Command Operation

ABSTRACT

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1 Affected Products

Any DLPC910 controller configured with the DLPR910A programmable read-only memory (PROM).

2 Summary

If the DLPC910 controller is configured using the DLPR910A PROM, when row cycles are sent continuously (no clocks between row cycles) while DVALID is held HIGH continuously, data will be incorrectly sent to the DMD. This includes No-Op row cycles.

This issue affects the DLPC910 controller for the DLP9000X digital micromirror device (DMD) and the DLP6500 DMD when configured with the DLPR910A PROM.

The DLPR910A PROM release (revised from DLPR910) includes modifications to the DLPC910 controller firmware. This DLPR910A update makes the DLPC910 controller compatible with both the original DLP9000X, DLP6500 and DLP9000XB, DLP6500B versions.

A consequence of these modifications is a change to the method of sending row commands continuously.

Figure 1 shows the current timing diagram for DVALID during a row cycle:

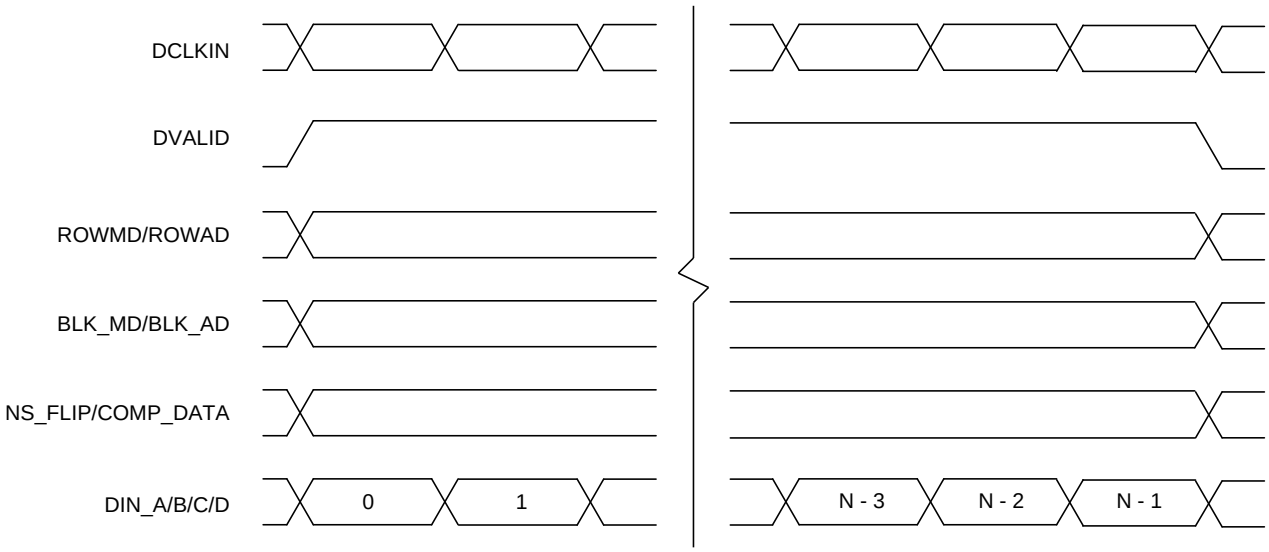

Figure 1. DLPC910 Row Operation (Current)

NOTE: N is the number of clock edges per row cycle for the DMD. This is 40 for the DLP9000X(B) and 64 for the DLP6500(B).

Immediate action: Please see the “TI Recommendations” section (Section 3) of this technical advisory for details.

3 TI Recommendations

TI recommends implementing the solution shown in Figure 2 for all row cycle commands when using the DLPC910 controller configured with the DLPR910A PROM:

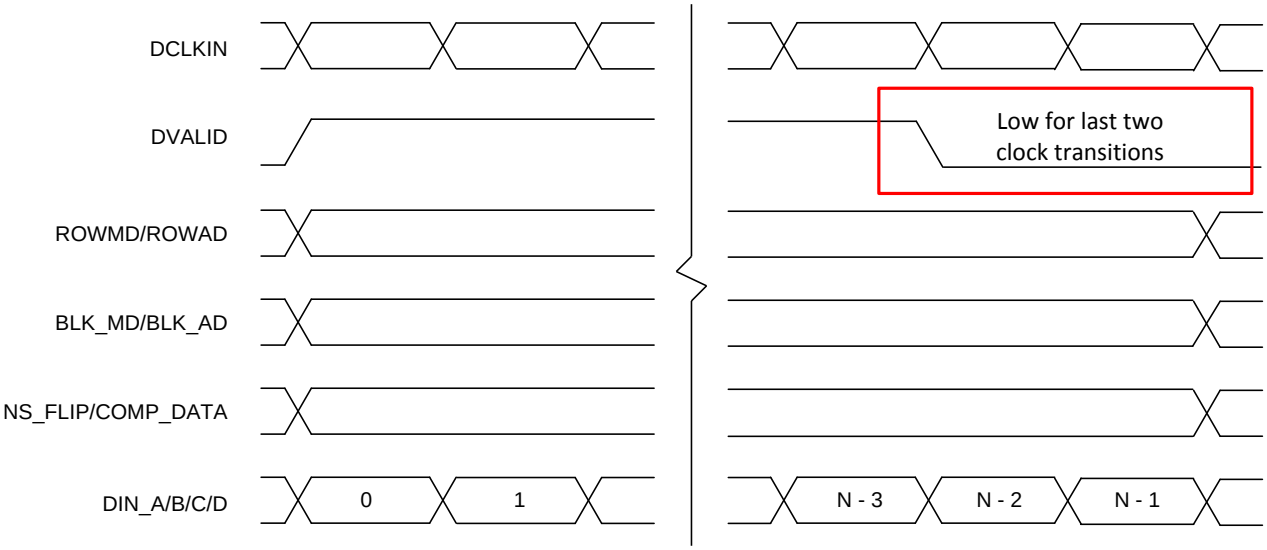

Figure 2. DLPC910 Row Operation (New Implementation)

This implementation requires setting DVALID to LOW for the last two clock transitions (last clock cycle) of each row cycle, which will ensure that the row cycle commands and data are correctly sent to the DMD. This is for all row cycle operations including No-Op row cycles.

NOTE: Setting DVALID to LOW for the last clock cycle does not affect data read in the last two clock transitions. The firmware will finish the correct number of DIN_(A/B/C/D) reads for the specific DMD started by the rising edge of DVALID at the beginning of the row cycle.

In systems that will not send continuous row cycle commands no change is required, but it is recommended.

Further, this change is recommended for all versions of the DLPR910 PROM.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265