Application Report

Optimizing DLP® Pico™ power consumption for Augmented Reality (AR) and power-sensitive applications

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ABSTRACT

This application note investigates the power consumption of three DLP Pico chipsets which offer many benefits for augmented reality (AR) applications. These chipsets, defined in this document to be the DMD and accompanying digital controller, are examined across varying operating conditions, including different sequences, content (images), and the Content Adaptive Illumination Control (CAIC) algorithm. Power measurements on a live system demonstrating the techniques described in this document can be found in the appendix. Copies of the firmware builds used, as well as test images, are also available for users who wish to evaluate DLP technology for their application.

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Trademarks

1 Introduction

Texas Instruments DLP® technology is a micro-electro-mechanical systems (MEMS) technology that modulates light using a digital micromirror device (DMD). Each micromirror on a DMD represents a pixel on the screen and is independently modulated, in sync with color sequential illumination, to create stunning displays. DLP technology powers the displays of products worldwide, from digital cinema projectors to smartphone attachments. In 2014, a new class of DLP Pico™ chipsets based on a breakthrough micromirror technology called DLP TRP (Figure 1-1) was launched. With a smaller pixel pitch of 5.4 µm and increased tilt angle of 17 degrees, TI's DLP TRP chipsets have higher resolutions, lower power consumption, and enhanced image processing features while maintaining the best in class optical efficiency of DLP technology. TRP chipsets are a great fit for any display system that requires high resolution and high brightness at low power in a compact size.

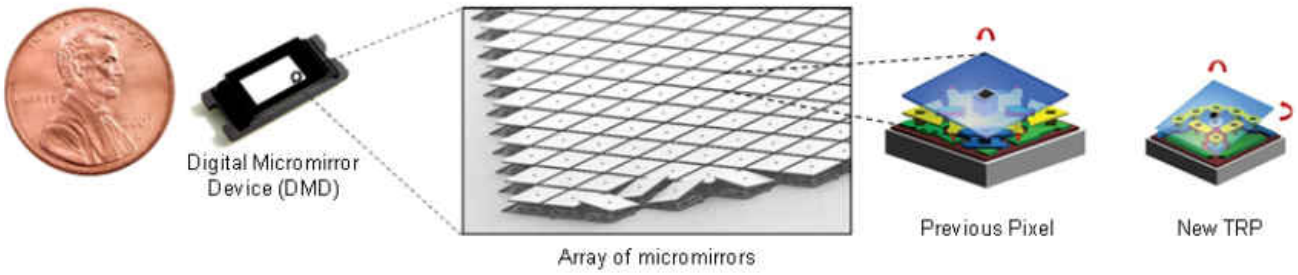

Figure 1-1. Texas Instruments DLP TRP Technology: Smaller, Brighter, Lower Power

2 Concept

2.1 System Design Considerations

Within the context of a power-sensitive application such as AR headsets, there are numerous system design considerations which can take advantage of the speed and efficiency of DLP technology in order to implement quality displays with reduced power consumption and portable form factors. For a formal definition of augmented reality as a use case, please see the DLP® Technology for Near Eye Display application report.

Near-eye display applications, along with other power-sensitive applications such as portable smartphones, tablets, and smart home displays, have requirements unlike traditional fixed projection displays. Near-eye display applications, for instance, have reduced LED brightness requirements as a result of implementing a virtual image directly to the user's eye. DLP chipsets offer methods to take advantage of this gap in brightness requirements with static LED power saving options in addition to dynamic LED dimming options. See Section 3.2 and Section 4.3 for examples.

AR-compatible content is furthermore unlike that of a standard video feed. In many cases, only particular regions of the display are utilized with a particular piece of content. In the example shown in Figure 2, the red car in the augmented reality content only consumes a portion of the total display area while the traditional video always requires the full display resolution. In cases such as this, DLP chipsets feature solutions which allow the user to automatically extract potential power savings from the simpler content. Section 4.1 shows how the DMD can be effectively operated at a reduced capacity to save system power with the right kind of content.

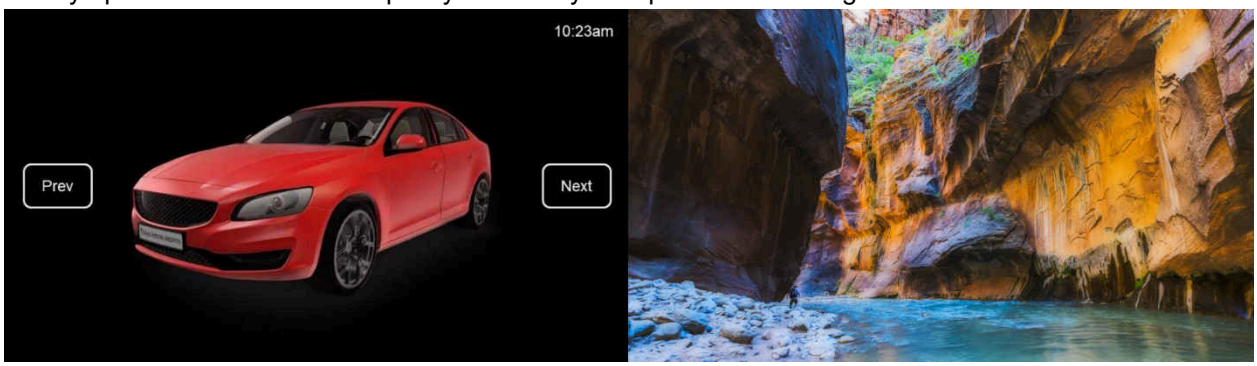

Figure 2-1. Typical AR content (left) versus traditional video content (right)

During runtime, power consumption of particular use cases and system behavior can also be optimized further. Section 3.3, Section 4.2, and Section 5.1 detail the software optimizations that product designers can make during runtime in order to maximize the utility of their DLP chipset. Many of these configuration decisions can be implemented in firmware prior to boot, while some allow for on-the-fly reconfiguration based on the current system operating mode.

2.2 Chipset Selection

DLP Pico technology is a robust projection technology offering a flexible portfolio to provide customers an optimized display solution for a wide variety of applications. DLP Pico products feature many chipsets that are very attractive for AR. These chipsets consume low amounts of power, offer a variety of resolutions, and are able to produce high-quality displays in a small form factor. Recommended chipsets are those supporting the DLP2010 (.2 WVGA), DLP230GP (.23 qHD), and DLP3010 (.3 720p) DMDs. Designing a display system which consumes minimal power is critical for AR applications given the form factors and battery limitations of such devices.

Each of these chipsets creates a unique display solution by taking advantage of different tradeoffs between power consumption and system brightness. Of the three chipsets this Application Note investigates, the DLP2010 chipset provides the smallest form factor and lowest power consumption, but also has the most restrictions on system output brightness. The DLP3010 chipset offers the least restrictions on system brightness, but this consumes the most power and results in the largest system design. Selecting the most appropriate chipset for an AR application considers resolution, frame rate, brightness, power, and size requirements.

Figure 2-2. Overview of DLPC343x single-controller chipsets

Table 2-1. Comparison of DLP augmented reality chipsets

Specification	DLP2010	DLP230GP	DLP3010
Micromirror Array Diagonal	0.2"	0.23"	0.3"
Resolution	854 x 480 (WVGA)	960 x 540 (qHD)	1280 x 720 (HD)
DMD Part Number	DLP2010AFQJ	DLP230GPAFQP	DLP3010AFQK
Controller Part Number	DLPC3430 or DLPC3435	DLPC3432	DLPC3433 or DLPC3438
Power Management IC Part Number	DLPA2000	DLPA2000	DLPA2000

2.3 Terms and Definitions

There are many different factors and system features that impact power consumption, even when analyzing a single DLP Pico chipset. The following list contains concepts examined for each chipset in this application note and an explanation of how DLP Pico chipsets offer a competitive advantage for AR systems:

Sequences – The term “sequence” in a single-chip DLP system represents the order and length of the bursts of light that are shone onto the DMD. When these bursts of light are synchronized with instructions operating the DMD mirrors, the result is a high-quality display that can be projected onto virtually any surface. In this investigation, all three optical modules use red, green and blue LEDs as an illumination source. Sequences control how often the DMD is loaded with image data and how many bursts of each color are shown per frame. Higher rates of DMD activity translate to increased data processing by the DLP chipset and higher power consumption. As such, sequence configuration has a direct impact on the power profile of a DLP-based system. DLP Pico chipsets support a variety of sequences which allows system designers flexibility when optimizing for image quality or power consumption.

Frame Rate – Increasing the frame rate of the system typically increases the number of DMD operations (and bursts of color) within the same period of time. The additional operations cause the system to consume more power. However, this relationship between frame rate and power consumption is not linear, and is highly dependent on software configuration. A DLP-based augmented reality system running at 120 Hz or 240 Hz for AR applications optimizes for image latency. The firmware evaluated in the Appendix characterizes these DLP chipsets at typical frame rates including 60 Hz, 120 Hz, and 240 Hz (240 Hz is not supported by the DLP3010 chipset).

Look – The concept of "looks" combines the concepts of "frame rate" and "sequence" above as they are applied to a software configuration on the chipsets described in this document. A look specifies the duty cycle combination of the red, green, and blue LEDs which are used to illuminate the DMD in a fashion specified by the DMD sequence. A single look contains duty cycle and sequence specifications for all frame rates that are supported by a particular chipset.

Content – As with many displays, the power consumption of a DLP chipset is content dependent. If the content being used possesses high-frequencies of color variance, such as a white noise pattern, more DMD operations are required to load the frame and therefore consume more power. The DLPC343x controller has built in software functions such as compression, sleep mode, and CAIC to make most efficient use of the DLP controller, PMIC, and DMD for each frame of image data. The use and impact of these functions is discussed in the sections below.

3 System Configuration

3.1 DMD Sequence Generation

Within the period of light emission, the DLP controller constructs a procession of color bursts in predefined sequences to build a frame image to be projected through the DMD and LEDs. In a typical system configuration, the emission period consists of the entire frame period (so, 16.67 ms in a 60 Hz frame, or 8.33 ms in a 120 Hz frame). An example sequence for a single color is seen in Figure 3-1, producing a white ramp once all bit planes are accounted for. DLPC343x chipsets replicate this procedure for each color (red, green, and blue) in separate color segments to complete the image frame.

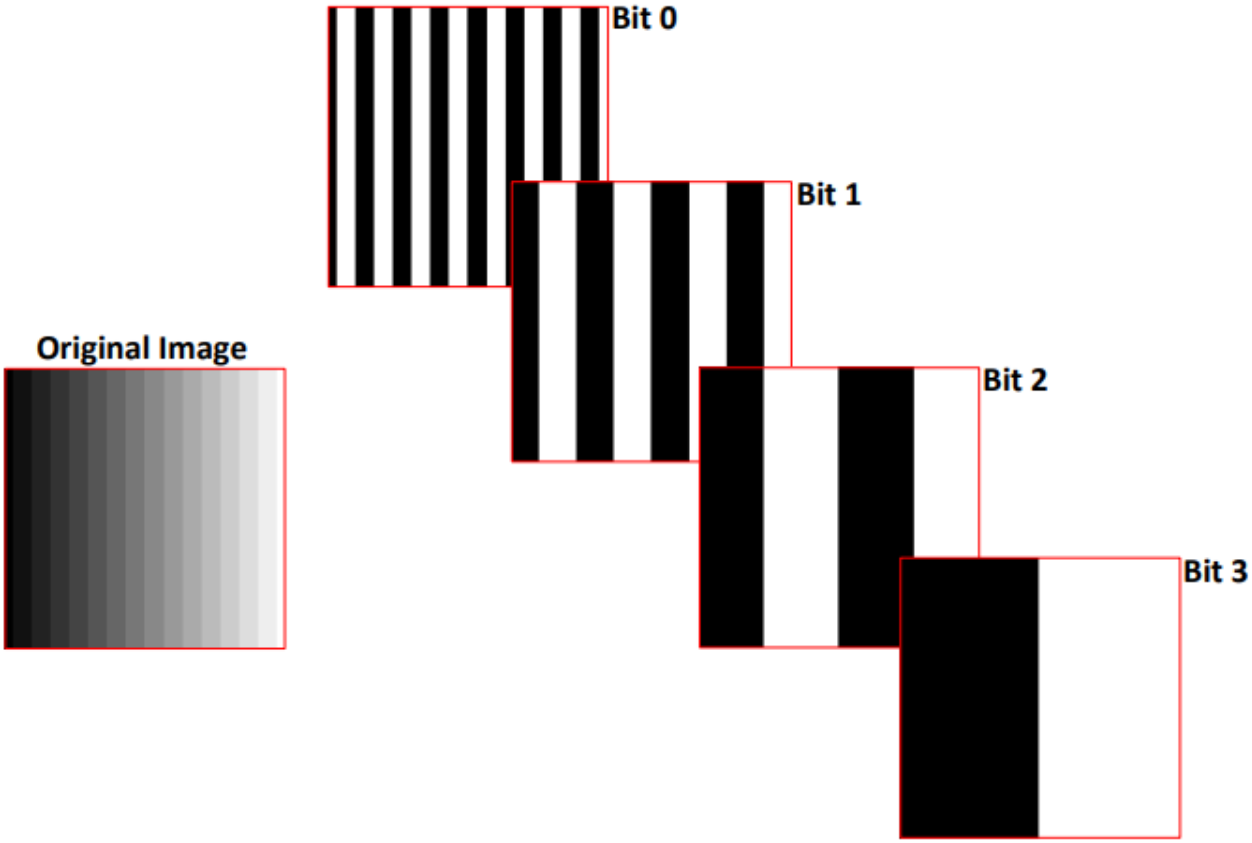

Figure 3-1. Sequence Example Bit Planes

Typical DLPC343x system configurations may feature multiple color cycles which separate the individual color segments into discrete chunks. In display applications, this interleaving of illuminator colors reduces color breakup and thereby improves image quality performance. Due to the increased complexity of system software instructions required to intersperse color segments in this manner, average color cycle count typically drops as frame time drops (or frame rate increases).

Figure 3-2. Example illumination sequence with four color cycles per LED

Using multiple color cycles helps reduce color breakup. Color breakup is the visible separation of red, green, and blue that normally composes a singular image. This non-ideality occurs when a color reaches an observer's eye when the image is past the relevance of the scene in front of the user, leaving a trailing image. Due to the fast switching speed of the micromirrors, DLP technology is able to mitigate this by cycling through the colors more frequently.

3.2 Dark Time

With a strong focus on power consumption and image latency, support for AR applications require a different approach than that of a typical display application (such as the example above). Inclusion of dark time allows for a reduction in the emission time (and thereby ***input latency***), reduction in sequence complexity (increasing ***maximum frame rate*** and reducing ***power consumption***), and a reliable source of image dimming (reducing ***LED power consumption***and ***total system brightness***). Such is possible thanks to the speed at which image data can be rendered by a DLP chipset to the DMD. This type of sequence is made by completing a sequence within a certain percentage of the frame period, leaving the remainder of the frame period without any LED illumination. For example, a Look with 50% dark time at 120 Hz (a 8.33 ms period) has 4.16 ms of emission followed by 4.16 ms without LED illumination. As a result, the images brightness is reduced by roughly 50%.

Figure 3-3. Example illumination sequence with one color cycle per LED, and 50% dark time

By displaying all bit planes for a particular frame within only a fraction of the full frame time, the effective latency of the input content can be reduced. Assuming single buffer mode is enabled with the configuration above, the latency is reduced from 8.33 ms (a typical 120 Hz frame) down to 4.16 ms (as the image is fully displayed in half the time). Taking this further, the same configuration of 50% dark time can yield an image latency of 2.083 ms with a frame rate of 240 Hz (supported by the 0.2” WVGA chipset).

While the full emission time may be desired for maximum brightness, dark time can offer significant power savings as a majority of power in typical DLP chipsets is spent by the LEDs for illumination. Because the LEDs are off during dark time, only the active color cycle segments contribute to the total power consumption of the LEDs. Depending on the amount of dark time employed in a particular AR system design, this can lead to substantial power savings.

In addition to power savings, this illumination scheme also indirectly provides a way to dim the LEDs beyond what is possible with the power management IC (or PMIC) of the DLP chipset. The DLPA2000, for example, supports LED output power from ~0.4 W to 2 W in a typical configuration depending on IDAC current settings. By employing the LED dimming available via dark time, this output power is effectively cut by however much dark time is used (50% in this case). For more information on the PMIC and associated IDAC operation, see the DLPA2000 Datasheet.

Although an image sequence with reduced color cycles (such as in the figure above) presents a possibility of reduced image quality due to image trailing (or ghosting) in typical display applications, it is a strong value proposition for AR systems using DLP technology. In particular, improvements to image latency via dark time are beneficial for head-mounted displays where the user’s head movements otherwise cause noticeable lag in content and loss of image presence.

An upper limit for dark time exists for every chipset and system configuration and is a result of factors such as DMD load time, frame rate, bit depth, color cycles, and hardware. See Section 5.1 for a full table of AR-compatible software configurations available from TI.com.

3.3 Single Buffer Mode

Under default operating conditions, the DLPC343x is configured to feature a double-buffered video processing pipeline. Double-buffering the video input ensures that the video output does not experience image or color tearing, at the cost of requiring an additional frame of latency for video processing.

The DLPC343x controller is capable of disabling this double-buffering scheme and rely on a single video frame buffer, minimizing the video input latency of the system. Note that single buffer mode is only supported when operating with external video input or test patterns. If a splash screen is loaded while single-buffer mode is enabled, the controller automatically enters the standard double-buffered mode. When the input source returns to a test pattern or external video the controller returns to single-buffer mode (assuming the user did not disable it). Image freeze is not supported when Single buffer mode is enabled. Single buffer mode is not supported with 3D video and therefore must be manually disabled.

While there may be some power savings to be had by disabling use of a secondary buffer, the reduced input latency is useful in the context of low latency applications such as Augmented Reality (AR). In particular, head-mounted display applications such as AR benefit from reduced video latency as a means to improve the real-world presence of AR content and reduce motion sickness caused by temporal inconsistency. Combined with dark time sequences (which reduce image latency by reducing the effective display time of a frame to a fraction of the total frame time) and increased frame rate (up to 240 Hz on the 0.2” WVGA chipset), extremely low video latency can be achieved on the DLPC343x family of chipsets.

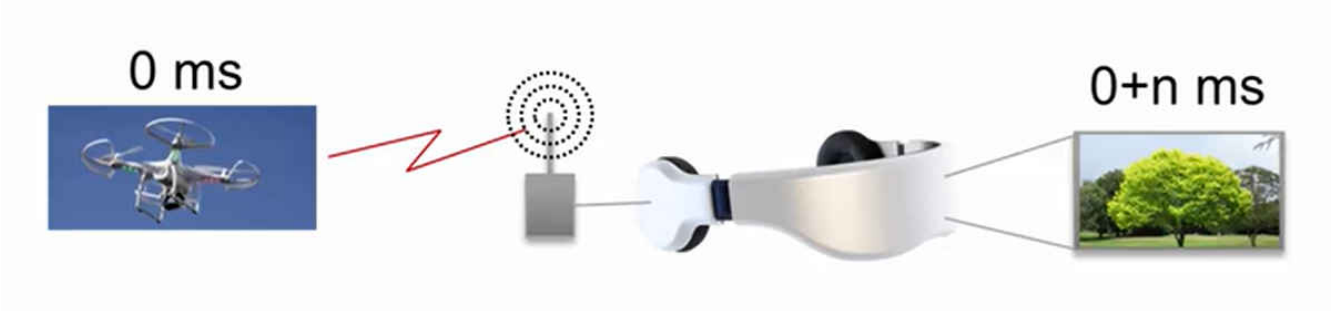

Figure 3-4. Display latency introduced by DLP chipset

4 Software Configuration

4.1 Sleep Mode and DMD Compression

The DLPC343x chipsets can further reduce power consumption from the DMD via use of data compression and sleep modes. The DLPC343x controller features a processing block which compresses the data written to the DMD, resulting in less operations required to load the DMD. Since less memory access instructions are used to load DMD patterns, this process results in reduced power consumption. As such, it is expected that relatively uniform patterns consume less power than non-uniform patterns. This data compression feature is enabled by default in the 0.2” WVGA, 0.23” qHD, and 0.3” HD chipsets. Within the context of AR applications this functionality can be readily taken advantage of thanks to the nature of the content being displayed. Examples such as Figure 4-1 are common in AR video streams, with large regions of the image being empty (and thereby easily compressible).

Figure 4-1. Example of compression-friendly AR content

The DLPC343x may also access its sleep modes depending on input content, as with compression. If entire DMD regions are left blank the DLP controller may detect this and choose to put sections of the chipset to sleep as no new data is being written to the system. Sleep modes automatically toggle different portions of the DLPC343x controller and DMD to save power when certain blocks are not required. Like DMD compression, sleep modes are enabled by default in available DLPC343x controller firmware configurations.

Because the power savings resulting from DMD compression and sleep mode are almost entirely dependent on image content, it is valuable to optimize such input content whenever possible in order to maximize power efficiency of the DLP chipset. Thanks to the immersive nature of augmented reality content, it is uncommon for noisy images that present few chances for power savings to occur.

4.2 Previous Bitplane Compare (PBPC)

Previous Bitplane Compare (PBPC) is a function available on the DLPC343x family of chipsets which can be enabled for specific use cases featuring content which is uniformly white or black. When PBPC is enabled, the DLPC343x controller is able to detect when compatible content is being sent to the DMD (such as a solid white or black raster).

In such cases, the DLPC343x puts the system into a special low-power state which minimizes power consumption caused by transmitting video data from the controller to the DMD. This is possible because these corner cases of content (all white or all black) never requires a change of mirror state within the frame (the array of mirrors on the DMD is never loaded with new data, and is kept at all on or all off). While such images are seldom found during typical display video content, it can ensure that power is not wasted by inefficient DMD addressing during “empty” video content. PBPC can be enabled by issuing the appropriate I^2C command to the DLPC343x during runtime.

4.3 Content Adaptive Illumination Control (CAIC)

Content Adaptive Illumination Control (CAIC) is an optional software function available on the DLPC343x controller which modulates LED power output during runtime based on input video content. When enabled, it consumes a marginal amount of additional power in the controller subsystem while providing the opportunity to save substantial amounts of power on the much larger LED loads being used in the system. As such, the value returned by use of CAIC is very dependent on system design, power profile, brightness settings, and input content. Within the context of this application note, CAIC is considered with regards to its ability to save overall system power in AR applications.

In a typical DLP display system without CAIC enabled, the IDAC controlling the RGB LEDs is set to provide a particular brightness and power output based on the user's preference. When CAIC is enabled, however, control of this setting is automated by the DLPC343x controller itself. The CAIC software algorithm reacts independently to the input content provided on a frame by frame basis to modulate the IDAC values sent to the PMIC. For a general overview of CAIC and other DLPC343x Intellibright Algorithms, see TI DLP® IntelliBright™ Algorithms for the DLPC343x.

While operating in power reduction mode, CAIC provides potential returns to **power, brightness, thermal management, and contrast**. AR content is well suited to this operating mode due to the sparse nature of objects typically found in AR overlays. For example, Figure 4-2 represents content with a relatively low average picture level (APL). In such a case, the IDACs are able to be driven much lower than the nominal value while maintaining white point. In comparison, for full-on content such as a white raster the CAIC algorithm keeps all LEDs running at maximum capacity to preserve the white point of the image. As a result, ongoing execution of the CAIC algorithm and its subsequent LED modulation results in significant power savings during appropriate content, with full-on-full-off (FOFO) contrast improving at the same time:

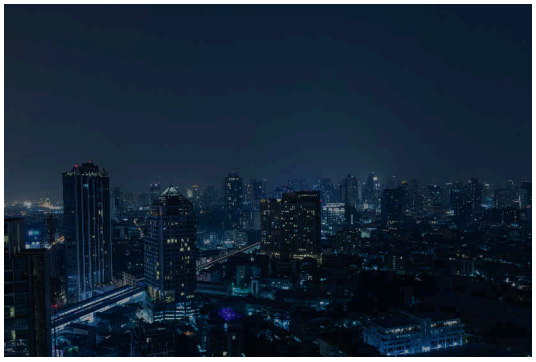

Figure 4-2. Example content with low Average Picture Level (APL)

It is important to note, however, that as CAIC seeks to maintain white point during LED modulation it cannot reduce LED power output if intrusive content skews the APL. Consider an object (such as a logo) in the frame that contains 255:255:255 RGB data (white color). In such a case CAIC keeps all LEDs at the nominal operating value:

Figure 4-3. Example content with high Average Picture Level (APL) due to UI elements

Since CAIC is adaptive to different input content, it functions best when given a wide range of input content on which to operate. For example, if input content varies little and is consistently at a high picture level, the

algorithm itself minimally impacts system performance. In such a case, nominal current settings are maintained regardless of whether or not CAIC is enabled. Similarly, if the average picture level of input content is always low then the LED output power necessarily remains at the minimum state. In this situation, the use of CAIC in the system becomes redundant and the user may simply disable CAIC altogether, opting to instead set the LED IDAC output values to their minimum as a static system configuration. The maximum CAIC LED current set by the user via I2C defines the maximum CAIC LED currents to which CAIC can adjust the RGB color channels. The maximum CAIC LED current for any RGB color channel is restricted to the maximum ratings for the PMIC being used as well as the maximum current handling capability of the LED driving circuitry.

In cases where the input content ***is*** dynamic, Table 4-1 below demonstrates the LED power savings (as well as thermal performance) that one can expect when utilizing the CAIC algorithm for dark-colored content, mixed dark-bright-colored content, and bright-colored content on the DLPC343x chipset. The DLPC3432 is used as an example:

Table 4-1. DLP230GP Chipset Performance with and without CAIC

Specification		Record Player	Woods Trail	Carnival
Content Description		Preference towards darker Colors, lower average intensity	Mixture of bright and dark scenes, good variety of colors	Preference towards brighter colors, higher average intensity
CAIC Disabled	Power	1.72 W	1.72 W	1.72 W
	Surface Temperature	46°C	46°C	46°C
CAIC Enabled	Power	0.96 W	1.16 W	1.49 W
	Surface Temperature	40°C	41°C	44°C
	Power Savings	43.1%	32.5%	15.1%

While darker content with a lower average picture level (APL) results in greater power savings with CAIC, AR systems benefit most from using CAIC to save power and improve contrast dynamically based on the input content over a variety of use cases. For example, it is common within AR applications to consider indoor (low ambient light) and outdoor (high ambient light) use cases to prepare content accordingly for maximum visibility and usability. CAIC ensures that the LED illuminators are used as efficiently as possible.

When operating in conditions with low average picture level, it is important to address the inherent non-linearity of LEDs under strained thermal and lifetime operating conditions. Over time, reduced DAC output from the PMIC may feature non-linearity in color channels that may degrade white point and reduce overall system performance. To manage this variability, it is recommended to properly calibrate the associated lookup tables (LUTs) used by the CAIC algorithm to characterize each LED, and adjust these tables as necessary to reflect the real-world operating conditions of the device. For information on how to calibrate the CAIC LUTs used to drive the software algorithm within a DLPC343x-based chipset, see the Real-Time Color Management for DLPC343x application note.

5 Measurements

5.1 Available Firmware Builds

All looks (operating modes) use 30% red, 50% green, 20% blue duty cycle configuration for LEDs unless otherwise noted for consistent white point performance. Firmware builds are available on TI.com via the TI DLP® Pico™ Firmware Selector Tool.

Table 5-1. DLP2010 (0.2" WVGA) Chipset Configuration Settings (with DLPA2000 and DLPC3430)

Look #	Dark Time (%)	Color Cycles (#)	Frame Rates Supported	DMD Blocks	Notes
0	0%	4+	60, 120, 240 Hz	8	N/A
1	50%	1	60, 120, 240 Hz	8	240 Hz mode runs at reduced brightness
2	25%	2	60, 120 Hz	8	120 Hz mode runs at reduced brightness
3	0%	4+	60, 120, 240 Hz	6	N/A
4	50%	1	60, 120, 240 Hz	6	N/A
5	25%	2	60, 120, 240 Hz	6	240 Hz mode runs at reduced brightness

Table 5-2. DLP230GP (0.23" qHD) Chipset Configuration Settings (with DLPA2000 and DLPC3432)

Look #	Dark Time (%)	Color Cycles (#)	Frame Rates Supported	DMD Blocks	Notes
0	0%	4+	60, 120, 240 Hz	8	N/A
1	50%	1	60, 120, 240 Hz	8	240 Hz mode runs at reduced brightness
2	25%	2	60, 120 Hz	8	N/A
3	0%	4+	60, 120, 240 Hz	6	N/A
4	50%	1	60, 120, 240 Hz	6	240 Hz mode runs at reduced brightness
5	25%	2	60, 120	6	N/A

Table 5-3. DLP3010 (0.3" HD) Chipset Configuration Settings (with DLPA2000 and DLPC3433)

Look #	Dark Time (%)	Color Cycles (#)	Frame Rates Supported	DMD Blocks	Notes
0	0%	4+	60, 120 Hz	8	N/A
1	50%	1	60, 120 Hz	8	N/A
2	25%	2	60 Hz	8	N/A
3	0%	4+	60, 120 Hz	6	N/A
4	50%	1	60, 120 Hz	6	N/A
5	25%	2	60 Hz	6	N/A

5.2 Test Cases

The images used in this application note represent different content that is typically displayed in an AR system. In the list below, each image used is shown with a short description on why the image was used. The images have been made available for public use so the reader can create the measurements with the same settings and content used to collect the reported data.

1. Black Image – The black image was selected to show the power consumption of the system when no content was being displayed (and the system is active).
2. White Image – Alternate case to black image. Highly compressible content with minimum DMD mirror activity.
3. Red Car – The image with a red car and some additional content was selected as a typical AR image. AR content typically has a main object with some smaller features and a black background. The black background is used to allow the system to augment the user's surrounding.
4. White Car - Alternate case to red car image.
5. SMPTE Color Bars – The SMPTE Color Bars is an industry standard pattern, which is used in this application note to provide a potential "common ground" when measuring power and comparing systems.
6. White Noise – The white noise image is the "worst case" pattern for power consumption, as the compression algorithms cannot be used to save power and this pattern contains the most data switching. This pattern can be used to calculate the maximum power consumption of the DLP chipset.

Note that each measurement was made using the image scaled to the native resolution of the DMD. This resulted in different files being used to measure power on each of the three DLP Pico chipsets in this application note. All three resolutions of each image have been made available for the reader to use in their measurements.

The tables shown contain the power measurement data for the three DLP Pico chipsets outlined in this application note. For each chipset, the power profile of the **DMD and the DLPC343x Controller** are first measured across varying frame rates (keeping emission time at 100%), and then across varying levels of emission time (keeping frame rate at 60 Hz). Finally, a third chart is available which demonstrates total chipset power across frame rate and emission time. In this case, power values are the average of typical use case images and excludes extreme cases (such as white noise). **LED power** is not included in this test, as it will vary directly with brightness settings implemented by the system designer.

For all test cases, the following optional system features are enabled:

1. DMD Sleep Mode and Compression
2. Single Buffer Mode
3. Previous Bitplane Compare

The following system features are not enabled:

1. CAIC - Because CAIC only affects dynamic LED power, it is not enabled in these tests. Refer to Section 4.3 for information on the impact of CAIC on LED power efficiency.

5.3 Test Data

All power units are in milliwatts (mW).

Table 5-4. DLP2010 (0.2" WVGA) Chipset Power (Variable Frame Rate, Fixed 0% Dark Time)

Frame Rate	Black Raster	White Raster	Red Car	White Car	SMPTE Color Bars	White Noise
DLP2010 DMD						
60 Hz	62	92	86	87	94	115
120 Hz	64	97	90	92	101	123
240 Hz	66	106	94	95	103	125
DLPC3430 Controller						
60 Hz	119	138	133	134	138	160
120 Hz	144	169	162	163	169	203
240 Hz	197	224	219	221	226	281
Total Power (DLP2010 + DLPC3430)						
60 Hz	181	230	219	221	232	275
120 Hz	208	266	252	255	270	326
240 Hz	263	330	313	316	329	406

Table 5-5. DLP2010 (0.2" WVGA) Chipset Power (Variable Dark Time, 60 Hz Fixed Frame Rate)

Dark Time (%)	Black Raster	White Raster	Red Car	White Car	SMPTE Color Bars	White Noise
DLP2010 DMD						
0%	62	96	86	87	94	115
25%	60	78	73	73	78	87
50%	57	68	66	66	68	75
DLPC3430 Controller						
0%	119	138	133	134	138	160
25%	114	125	123	123	126	143
50%	111	119	118	118	120	135
Total Power (DLP2010 + DLPC3430)						
0%	181	234	219	221	232	275
25%	174	203	196	196	204	230
50%	168	187	184	181	188	210

Table 5-6. DLP2010 (0.2" WVGA) Chipset Power (Average of Typical Use Cases)

Dark Time (%)	60 Hz	120 Hz	240 Hz
0%	214	247	307
25%	191	235	300
50%	180	219	300

Note: "Average of Typical Use Cases" includes all test images except "White Noise", which is an extreme test condition.

Table 5-7. DLP230GP (0.23" qHD) Chipset Power (Variable Frame Rate, Fixed 0% Dark Time)

Frame Rate	Black Raster	White Raster	Red Car	White Car	SMPTE Color Bars	White Noise
DLP230GP DMD						
60 Hz	83	129	116	118	129	156
120 Hz	86	141	123	122	136	170
240 Hz	84	129	117	117	128	152
DLPC3432 Controller						
60 Hz	145	171	165	166	173	202
120 Hz	182	214	207	207	218	265
240 Hz	234	265	265	265	275	247
Total Power (DLP230GP + DLPC3432)						
60 Hz	229	301	282	284	302	358
120 Hz	268	355	330	329	354	436
240 Hz	318	395	382	382	402	499

Table 5-8. DLP230GP (0.23" qHD) Chipset Power (Variable Dark Time, 60 Hz Fixed Frame Rate)

Dark Time (%)	Black Raster	White Raster	Red Car	White Car	SMPTE Color Bars	White Noise
DLP230GP DMD						
0%	83	129	116	118	129	156
25%	78	108	99	99	106	126
50%	73	86	82	82	85	91
DLPC3432 Controller						
0%	146	171	165	166	173	202
25%	139	156	153	153	158	183
50%	131	140	140	140	142	162
Total Power (DLP230GP + DLPC3432)						
0%	229	301	282	284	302	358
25%	217	264	251	252	264	309
50%	204	226	221	222	227	253

Table 5-9. DLP230GP (0.23" qHD) Chipset Power (Average of Typical Use Cases)

Dark Time (%)	60 Hz	120 Hz	240 Hz
0%	280	329	378
25%	252	328	379
50%	221	278	365

Note: "Average of Typical Use Cases" includes all test images except "White Noise", which is an extreme test condition.

Table 5-10. DLP3010 (0.3" HD) Chipset Power (Variable Frame Rate, Fixed 0% Dark Time)

Frame Rate	Black Raster	White Raster	Red Car	White Car	SMPTE Color Bars	White Noise
DLP3010 DMD						
60 Hz	84	126	115	117	123	175
120 Hz	90	138	125	127	137	198
DLPC3433 Controller						
60 Hz	171	196	190	191	196	246
120 Hz	218	252	244	246	251	329
Total Power (DLP3010 + DLPC3433)						
60 Hz	255	322	305	308	319	420
120 Hz	307	390	369	373	387	528

Table 5-11. DLP3010 (0.3" HD) Chipset Power (Variable Dark Time, 60 Hz Fixed Frame Rate)

Dark Time (%)	Black Raster	White Raster	Red Car	White Car	SMPTE Color Bars	White Noise
DLP3010 DMD						
0%	84	126	115	117	123	175
25%	78	91	87	87	90	104
50%	79	91	86	88	90	103
DLPC3433 Controller						
0%	171	196	190	191	196	246
25%	155	167	164	165	167	200
50%	156	168	164	165	167	199
Total Power (DLP3010 + DLPC3433)						
0%	255	322	305	308	319	420
25%	234	258	251	252	257	304
50%	234	259	251	253	256	303

Table 5-12. DLP3010 (0.3" HD) Chipset Power (Average of Typical Use Cases)

Dark Time (%)	60 Hz	120 Hz
0%	333	408
25%	265	346
50%	265	340

Note: "Average of Typical Use Cases" includes all test images except "White Noise", which is an extreme test condition.

5.4 Test Images

Note: All test images are provided with sample firmware on TI.com (via the TI DLP® Pico™ Firmware Selector Tool)

Figure 5-1. Black Raster Test Image

Figure 5-2. White Raster Test Image

Figure 5-3. Red Car Test Image

Figure 5-4. White Car Test Image

Figure 5-5. SMPTE Color Bars Test Image

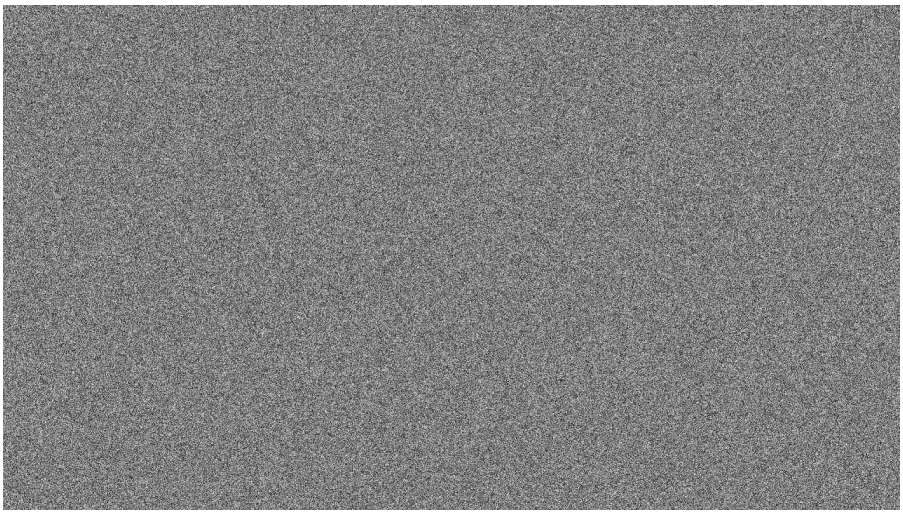

Figure 5-6. White Noise Test Image

6 References

- The following documents are relevant to the topics in this application note and are available at www.ti.com:

  1. DLPC3430 and DLPC3435 Display Controller Datasheet (DLPS038)
  2. DLPC3432 Display Controller Datasheet (DLPS108)
  3. DLPC3433 and DLPC3438 Display Controller Datasheet (DLPS035)
  4. DLPC3430, DLPC3432, DLPC3433, DLPC3435 and DLPC3438 Software Programmer's Guide (DLPU020)
  5. DLP® Technology for Near Eye Display Application Report (DLPA051)

  For assistance, refer to the DLP and MEMS TI E2E™ community support forums.

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