DLPC4422 DLP® Display Controller

1 Features

- Provides Two 30-bit Input Pixel Interfaces or One 60-bit Input Pixel Interface:
  - YUV, YCrCb, or RGB Data Format
  - 8, 9 or 10 Bits per Color
  - Pixel Clock Support Up to 175 MHz for 30-bit and 160 MHz for 60-bit
- Supports 24-30 Hz and 47-120 Hz Frame Rates
- Full Single DLP Controller Support For DMD™s Up to 1920 Pixels Wide
- Dual DLP Controller Support For Up to 4K Ultra High Definition (UHD) Resolution Display Using DLP660TE TRP DMD
- High-Speed, Low Voltage Differential Signaling (LVDS) DMD Interface
- 150 MHz ARM946™ Microprocessor
- Microprocessor Peripherals
  - Programmable Pulse-Width Modulation (PWM) and Capture Timers
  - Three I^2C Ports, Three UART Ports and Three SSP Ports
  - One USB 1.1 Slave Port
- Image Processing
  - Multiple Image Processing Algorithms
  - Frame Rate Conversion
  - Color Coordinate Adjustment
  - Programmable Color Space Conversion
  - Programmable Degamma and Splash
  - Integrated Support for 3-D Display
- On-Screen Display (OSD)
- Integrated Clock Generation Circuitry
  - Operates on a Single 20 MHz Crystal
  - Integrated Spread Spectrum Clocking
- External Memory Support
  - Parallel Flash for Microprocessor and PWM Sequence
  - Optional SRAM
- 516 Pin Plastic Ball Grid Array Package
- Supports Lamp, LED, and Laser Hybrid Illumination Systems

2 Applications

- 4K Ultra High Definition (UHD) Display
- Laser TV
- Digital Signage
- Projection Mapping

3 Description

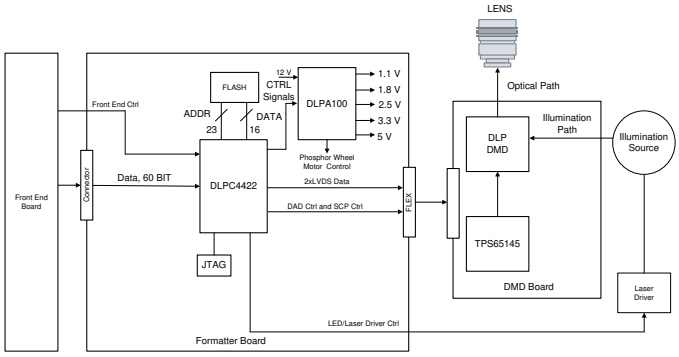
DLPC4422 is a digital display controller for the DLP 4K UHD display chipset. The DLPC4422 display controller, together with the DLP660TE DMD and DLPA100 power management and motor driver device, comprise the chipset. This solution is a great fit for display systems that require high resolution, high brightness and system simplicity. To ensure reliable operation, the DLPC4422 display controller must always be used with the DLP660TE DMD and the DLPA100 power management and motor driver device.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLPC4422	ZPC (516)	27.00 mm × 27.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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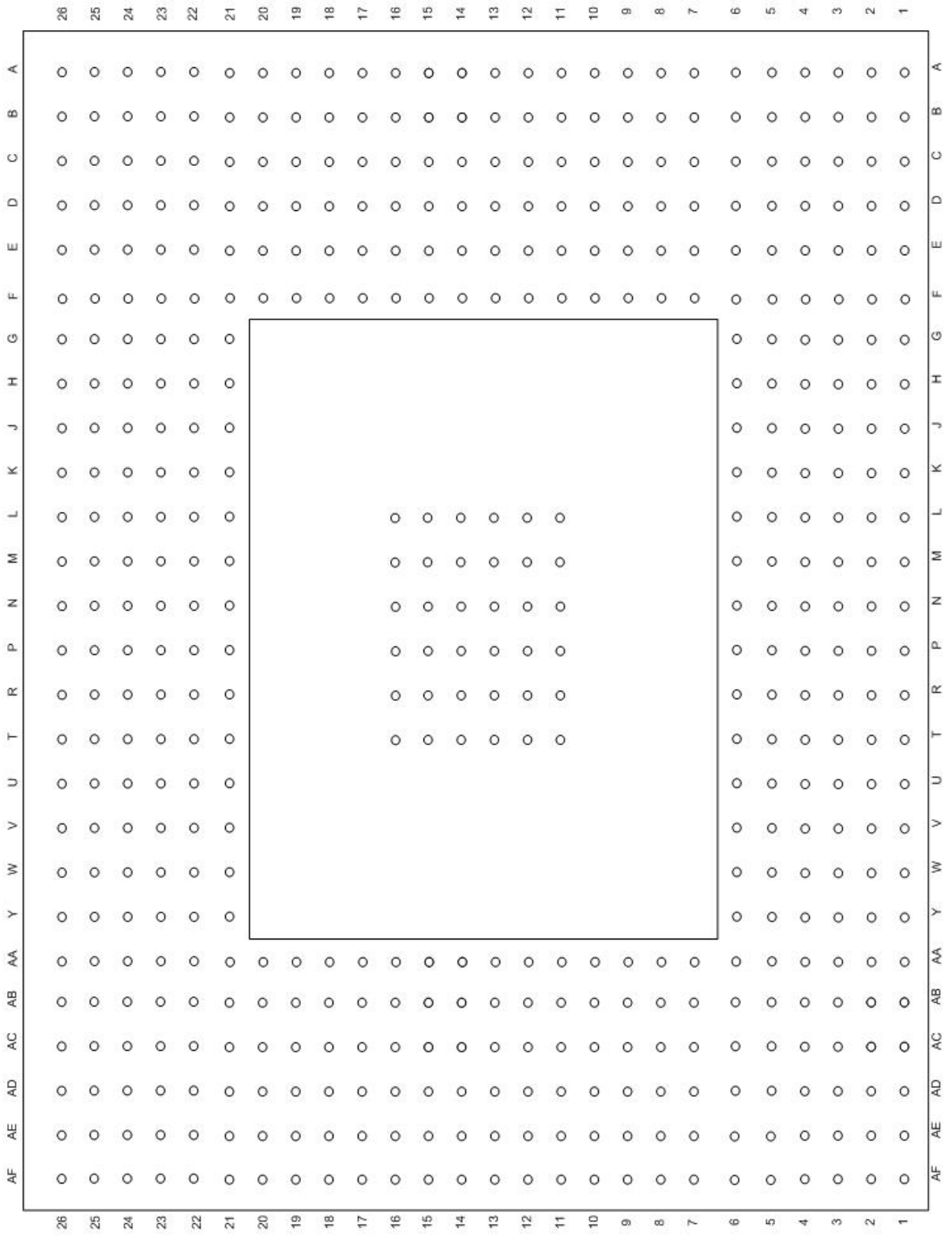
4 Revision History

DATE	REVISION	NOTES
February 2017	*	Initial release.

5 Pin Configuration and Functions

ZPC Package
516-Pin BGA
Bottom View



Pin Configurations and Functions

PIN[1]		I/O[2]	DESCRIPTION
NAME	NO.		
POSENSE	P22	I_4	Power-On Sense, High true, signal provided from an external voltage monitor circuit. This signal should be driven active (high) when all ASIC supply voltages have reached 90% of their specified minimum voltage. This signal should be driven inactive (low) after the falling edge of PWRGOOD as specified.
PWRGOOD	T26	I_4	Power Good, High true, signal from external power supply or voltage monitor. A high value indicates all power is within operating voltage specs and the system is safe to exit its reset state. A transition from high to low is used to indicate that the controller or DMD supply voltage will drop below their rated minimum level. This transition must occur prior to the supply voltage drop as specified. During this interval, POSENSE must remain active high. This is an early warning of an imminent power loss condition. This warning is required to enhance long term DMD reliability. A DMD park followed by a full controller reset is performed by the DLPC4422 controller when PWRGOOD goes low for the specified minimum, protecting the DMD. This minimum de-assertion time is used to protect the input from glitches. Following this the DLPC4422 controller will be held in its reset state as long as PWRGOOD is low. PWRGOOD must be driven high for normal operation. The DLPC4422 controller will acknowledge PWRGOOD as active once it's been driven high for it's specified minimum time. Uses hysteresis.
EXT_ARTZ	T24	O_2	General purpose, LOW true, reset output. This output is asserted low immediately upon asserting power-up reset (POSENSE) low and remains low while POSENSE remains low. EXT_ARSTZ continues to be held low after the release of power-up reset (that is, POSENSE set high) until released by software. EXT_ARSTZ is also asserted low approximately 5µs after the detection of a PWRGOOD or any internally generated reset. In all cases it will remain active for a minimum of 2ms. Note that the ASIC contains a software register that can be used to independently drive this output.
MTR_ARTZ	T25	O_2	Color wheel motor controller, LOW true, reset output. This output is asserted low immediately upon asserting power-up reset (POSENSE) low and remains low while POSENSE remains low. MTR_ARSTZ will continue to be held low after the release of power-up reset (i.e. POSENSE set high) until released by software. MTR_ARSTZ is also optionally asserted low approximately 5 µs after the detection of a PWRGOOD or any internally generated reset. In all cases it will remain active for a minimum of 2 ms. Note that the ASIC contains a software register that can be used to independently drive this output. The ASIC also contains a software register that can be used to disable the assertion of motor reset upon a lamp strike reset..
BOARD LEVEL TEST AND INITIALIZATION[3]			
TDI	N25	I_4	JTAG serial data in
TCK	N24	I_4	JTAG serial data clock
TMS1	P25	I_4	JTAG test mode select
TMS2	P26	I_4	JTAG test mode select
TDO1	N23	O_5	JTAG serial data out
TDO2	N22	O_5	JTAG serial data out
TRSTZ	M23	I_4	JTAG reset. This signal includes an internal pull-up and utilizes hysteresis. This pin should be pulled high (or left unconnected) when the JTAG interface is in use for boundary scan or ARM debug. Connect this pin to ground otherwise. Failure to tie this pin low during normal operation will cause startup and initialization problems.
RTCK	E4	O_2	JTAG Return Clock
ETM_PIPESTAT_2	A4	B_2	ETM Trace Port Pipeline Status. Indicates the pipeline status of the ARM core. These signals include internal pull-downs.
ETM_PIPESTAT_1	B5	B_2	
ETM_PIPESTAT_0	C6	B_2	
ETM_TRACESYNC	A5	B_2	ETM Trace Port Synchronization signal, indicating the start of a branch sequence on the trace packet port. This signal includes an internal pull-down.
ETM_TRACECLK	D7	B_2	ETM Trace Port Clock. This signal includes an internal pull-down.
ICTSEN	M24	I_4	IC Tri-State Enable (active high). Asserting high will Tri-state all outputs except the JTAG interface. This signal includes an internal pull-down however TI recommends an external pull-down for added protection. Uses hysteresis.
TSTPT_7	E8	B_2	Test pin 7 - This signal provides internal pull-downs. Normal Use: reserved for test output. Should be left open or unconnected for normal use.
TSTPT_6	B4	B_2	Test pin 6 - This signal provides internal pull-downs. Normal Use: reserved for test output. Should be left open or unconnected for normal use.
TSTPT_5	C4	B_2	Test pin 5 - This signal provides internal pull-downs. Normal Use: reserved for test output. Should be left open or unconnected for normal use.
TSTPT_4	E7	B_2	Test pin 4 - This signal provides internal pull-downs. Normal Use: reserved for test output. Should be left open or unconnected for normal use.

(1) For instructions on handling unused pins, see *General Handling Guidelines for Unused CMOS-Type Pins*.
(2) I/O Type: I = Input, O = Output, B = Bidirectional, and H = Hysteresis. See Table 1 for subscript explanation.
(3) All JTAG signals are LVTTL compatible.

Pin Configurations and Functions (continued)

PIN[1]		I/O[2]	DESCRIPTION
NAME	NO.		
TSTPT_3	D5	B_2	Test pin 3 - This signal provides internal pull-downs. Normal Use: reserved for test output. Should be left open or unconnected for normal use.
TSTPT_2	E6	B_2	Test pin 2 - This signal provides internal pull-downs. Additionally, TI recommends that jumper options be provided for connecting TSTPT(2:0) to external pull-ups.
TSTPT_1	D3	B_2	Test pin 1 - This signal provides internal pull-downs. Additionally, TI recommends that jumper options be provided for connecting TSTPT(2:0) to external pull-ups.
TSTPT_0	C2	B_2	Test pin 0 - This signal provides internal pull-downs. Additionally, TI recommends that jumper options be provided for connecting TSTPT(2:0) to external pull-ups.
DEVICE TEST			
HW_TEST_EN	M25	I_4	Device manufacturing test enable; This signal includes an internal pull-down and utilizes hysteresis. TI recommends that this signal be tied to an external ground in normal operation for added protection.
ANALOG FRONT END			
AFE_ARSTZ	AC12	O_2	Analog Front End, LOW true, Reset Output. This output is asserted low immediately upon asserting power-up reset (POSENSE) low and remains low while POSENSE remains low. AFE_ARSTZ will continue to be held low after the release of power-up reset (i.e. POSENSE set high) until released by software. AFE_ARSTZ is also asserted low approximately 5µs after the detection of a PWRGOOD or any internally generated reset. In all cases it will remain active for a minimum of 2ms after the reset condition is released by software. Note that the ASIC contains a software register that can be used to independently drive this output.
AFE_CLK	AD12	O_6	Analog Front End External Clock output for video decoder operation. Supports programmable output drive.
AFE_IRQ	AB13	I_4	Analog Front End Interrupt (Active High). This signal includes an internal pull-down and utilizes hysteresis.
PORT1 and PORT 2 CHANNEL DATA and CONTROL [4][5][6][7]			
P_CLK1	AE22	I_4	Input Port Data Pixel Write Clock (selectable as rising or falling edge triggered, and which port it is associated with (A or B or (A and B))). This signal includes an internal pull-down.
P_CLK2	W25	I_4	Input Port Data Pixel Write Clock (selectable as rising or falling edge triggered, and which port it is associated with (A or B or (A and B))). This signal includes an internal pull-down.
P_CLK3	AF23	I_4	Input Port Data Pixel Write Clock (selectable as rising or falling edge triggered, and which port it is associated with (A or B or (A and B))). This signal includes an internal pull-down.
P_DATAEN1	AF22	I_4	Active High Data Enable. Selectable as to which port it is associated with (A or B or (A and B)).This signal includes an internal pull-down.
P_DATAEN2	W24	I_4	Active High Data Enable. Selectable as to which port it is associated with (A or B or (A and B)).This signal includes an internal pull-down.
P1_A_9	AD15	I_4	Port 1 A Channel Input Pixel Data (bit weight 128)
P1_A_8	AE15	I_4	Port 1 A Channel Input Pixel Data (bit weight 64)
P1_A_7	AE14	I_4	Port 1 A Channel Input Pixel Data (bit weight 32)
P1_A_6	AE13	I_4	Port 1 A Channel Input Pixel Data (bit weight 16)
P1_A_5	AD13	I_4	Port 1 A Channel Input Pixel Data (bit weight 8)
P1_A_4	AC13	I_4	Port 1 A Channel Input Pixel Data (bit weight 4)
P1_A_3	AF14	I_4	Port 1 A Channel Input Pixel Data (bit weight 2)
P1_A_2	AF13	I_4	Port 1 A Channel Input Pixel Data (bit weight 1)
P1_A_1	AF12	I_4	Port 1 A Channel Input Pixel Data (bit weight 0.5)
P1_A_0	AE12	I_4	Port 1 A Channel Input Pixel Data (bit weight 0.25)
P1_B_9	AF18	I_4	Port 1 B Channel Input Pixel Data (bit weight 128)
P1_B_8	AB18	I_4	Port 1 B Channel Input Pixel Data (bit weight 64)
P1_B_7	AC15	I_4	Port 1 B Channel Input Pixel Data (bit weight 32)
P1_B_6	AC16	I_4	Port 1 B Channel Input Pixel Data (bit weight 16)
P1_B_5	AD16	I_4	Port 1 B Channel Input Pixel Data (bit weight 8)

(4) Ports 1 and 2 can each be used to support multiple source options for a given product (e.g., AFE & HDMI). To do so, the data bus from both source components must be connected to the same port pins (1 or 2) and control given to the DLPC4422 device to tri-state the "inactive" source. Tying them together like this will cause some signal degradation due to reflections on the tri-stated path. Given the clock is the most critical signal, three Port clocks (1,2,and 3) are provided to provide an option to improve the signal integrity.
(5) Ports 1 and 2 can be used separately as two 30-bit ports, or can be combined into one 60-bit port (typically for high data rate sources) for transmission of two pixels per clock.
(6) The A, B, C input data channels of Ports 1 and 2 can be internally re-configured/ re-mapped for optimum board layout.
(7) Sources feeding less than the full 10-bits per color component channel should be MSB justified when connected to the DLPC4422 controller and the LSBs tied off to zero. For example an 8-bit per color input should be connected to bits 9:2 of the corresponding A, B, C input channel.

Pin Configurations and Functions (continued)

PIN[1]		I/O[2]	DESCRIPTION
NAME	NO.		
P1_B_4	AE16	I_4	Port 1 B Channel Input Pixel Data (bit weight 4)
P1_B_3	AF16	I_4	Port 1 B Channel Input Pixel Data (bit weight 2)
P1_B_2	AF15	I_4	Port 1 B Channel Input Pixel Data (bit weight 1)
P1_B_1	AC14	I_4	Port 1 B Channel Input Pixel Data (bit weight 0.5)
P1_B_0	AD14	I_4	Port 1 B Channel Input Pixel Data (bit weight 0.25)
P1_C_9	AD20	I_4	Port 1 C Channel Input Pixel Data (bit weight 128)
P1_C_8	AE20	I_4	Port 1 C Channel Input Pixel Data (bit weight 64)
P1_C_7	AE21	I_4	Port 1 C Channel Input Pixel Data (bit weight 32)
P1_C_6	AF21	I_4	Port 1 C Channel Input Pixel Data (bit weight 16)
P1_C_5	AD19	I_4	Port 1 C Channel Input Pixel Data (bit weight 8)
P1_C_4	AE19	I_4	Port 1 C Channel Input Pixel Data (bit weight 4)
P1_C_3	AF19	I_4	Port 1 C Channel Input Pixel Data (bit weight 2)
P1_C_2	AF20	I_4	Port 1 C Channel Input Pixel Data (bit weight 1)
P1_C_1	AC19	I_4	Port 1 C Channel Input Pixel Data (bit weight 0.5)
P1_C_0	AE19	I_4	Port 1 C Channel Input Pixel Data (bit weight 0.25)
P1_VSYNC	AC20	B_2	Port 1 Vertical Sync. This signal includes an internal pull-down. While intended to be associated with Port 1, it can be programmed for use with Port 2.
P1_HSYNC	AD21	B_2	Port 1 Horizontal Sync. This signal includes an internal pull-down. While intended to be associated with Port 1, it can be programmed for use with Port 2.
P2_A_9	AD26	I_4	Port 2 A Channel Input Pixel Data (bit weight 128)
P2_A_8	AD25	I_4	Port 2 A Channel Input Pixel Data (bit weight 64)
P2_A_7	AB21	I_4	Port 2 A Channel Input Pixel Data (bit weight 32)
P2_A_6	AC22	I_4	Port 2 A Channel Input Pixel Data (bit weight 16)
P2_A_5	AD23	I_4	Port 1 A Channel Input Pixel Data (bit weight 8)
P2_A_4	AB20	I_4	Port 2 A Channel Input Pixel Data (bit weight 4)
P2_A_3	AC21	I_4	Port 2 A Channel Input Pixel Data (bit weight 2)
P2_A_2	AD22	I_4	Port 2 A Channel Input Pixel Data (bit weight 1)
P2_A_1	AE23	I_4	Port 2 A Channel Input Pixel Data (bit weight 0.5)
P2_A_0	AB19	I_4	Port 2 A Channel Input Pixel Data (bit weight 0.25)
P2_B_9	Y22	I_4	Port 2 B Channel Input Pixel Data (bit weight 128)
P2_B_8	AB26	I_4	Port 2 B Channel Input Pixel Data (bit weight 64)
P2_B_7	AA23	I_4	Port 2 B Channel Input Pixel Data (bit weight 32)
P2_B_6	AB25	I_4	Port 2 B Channel Input Pixel Data (bit weight 16)
P2_B_5	AA22	I_4	Port 2 B Channel Input Pixel Data (bit weight 8)
P2_B_4	AB24	I_4	Port 2 B Channel Input Pixel Data (bit weight 4)
P2_B_3	AC26	I_4	Port 2 B Channel Input Pixel Data (bit weight 2)
P2_B_2	AB23	I_4	Port 2 B Channel Input Pixel Data (bit weight 1)
P2_B_1	AC25	I_4	Port 2 B Channel Input Pixel Data (bit weight 0.5)
P2_B_0	AC24	I_4	Port 2 B Channel Input Pixel Data (bit weight 0.25)
P2_C_9	W23	I_4	Port 2 C Channel Input Pixel Data (bit weight 128)
P2_C_8	V22	I_4	Port 2 B Channel Input Pixel Data (bit weight 64)
P2_C_7	Y26	I_4	Port 2 C Channel Input Pixel Data (bit weight 32)
P2_C_6	Y25	I_4	Port 2 B Channel Input Pixel Data (bit weight 16)
P2_C_5	Y24	I_4	Port 2 C Channel Input Pixel Data (bit weight 8)
P2_C_4	Y23	I_4	Port 2 B Channel Input Pixel Data (bit weight 4)
P2_C_3	W22	I_4	Port 2 C Channel Input Pixel Data (bit weight 2)
P2_C_2	AA26	I_4	Port 2 B Channel Input Pixel Data (bit weight 1)
P2_C_1	AA25	I_4	Port 2 C Channel Input Pixel Data (bit weight 0.5)
P2_C_0	AA24	I_4	Port 2 B Channel Input Pixel Data (bit weight 0.25)
P2_VSYNC	U22	B_2	Port 2 Vertical Sync. This signal includes an internal pull-down. While intended to be associated with Port 2, it can be programmed for use with Port1.
P2_HSYNC	W26	B_2	Port 2 Horizontal Sync. This signal includes an internal pull-down. While intended to be associated with Port 2, it can be programmed for use with Port1.
ALF INPUT PORT CONTROL			
ALF_VSYNC	AF11	I_4	Autolock dedicated vertical sync. This signal includes an internal pull-down and uses hysteresis.

Pin Configurations and Functions (continued)

PIN[1]		I/O[2]	DESCRIPTION
NAME	NO.		
ALF_HSYNC	AD11	I_4	Autolock dedicated horizontal sync. This signal includes an internal pull-down and uses hysteresis.
ALF_CSYNC	AE11	I_4	Autolock dedicated composite sync (sync on green). This signal includes an internal pull-down and uses hysteresis.
DMD RESET and BIAS CONTROL			
DADOEZ	AE7	O_5	DAD1000 / DAD2000 Output Enable (active low)
DADADDR_3	AD6	O_5	DAD1000 / DAD2000 address
DADADDR_2	AE5	O_5	
DADADDR_1	AF4	O_5	
DADADDR_0	AB8	O_5	
DADMODE_1	AD7	O_5	DAD1000 / DAD2000 modes
DADMODE_0	AE6	O_5	
DADSEL_1	AE4	O_5	DAD1000 / DAD2000 select
DADSEL_0	AC7	O_5	
DADSTRB	AF5	O_5	DAD1000 / DAD2000 strobe
DAD_INTZ	AC8	I_4	DAD1000 / DAD2000 interrupt (active low). This signal typically requires an external pull-up and uses hysteresis.
DMD LVDS INTERFACE			
DCKA_P	V4	O_7	DMD, LVDS I/F channel A, differential clock
DCKA_N	V3	O_7	
SCA_P	V2	O_7	DMD, LVDS I/F channel A, differential serial control
SCA_N	V1	O_7	
DDA_P_15	P4	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_15	P3	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_14	P2	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_14	P1	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_13	R4	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_13	R3	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_12	R2	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_12	R1	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_11	T4	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_11	T3	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_10	T2	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_10	T1	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_9	U4	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_9	U3	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_8	U2	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_8	U1	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_7	W4	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_7	W3	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_6	W2	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_6	W1	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_5	Y2	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_5	Y1	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_4	Y4	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_4	Y3	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_3	AA2	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_3	AA1	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_2	AA4	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_2	AA3	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_1	AB2	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_1	AB1	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_P_0	AC2	O_7	DMD, LVDS I/F channel A, differential serial data
DDA_N_0	AC1	O_7	DMD, LVDS I/F channel A, differential serial data
DCKB_P	J3	O_7	DMD, LVDS I/F channel A, differential clock
DCKB_N	J4	O_7	DMD, LVDS I/F channel A, differential clock

Input Bus B Data bit 9.
100-Ω internal LVDS termination

Pin Configurations and Functions (continued)

PIN[1]		I/O[2]	DESCRIPTION
NAME	NO.		
SCB_P	J1	O_7	DMD, LVDS I/F channel A, differential serial control
SCB_N	J2	O_7	DMD, LVDS I/F channel A, differential serial control
DDB_P_15	N1	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_15	N2	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_14	N3	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_14	N4	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_13	M2	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_13	M1	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_12	M3	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_12	M4	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_11	L1	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_11	L2	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_10	L3	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_10	L4	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_9	K1	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_9	K2	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_8	K3	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_8	K4	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_7	H1	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_7	H2	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_6	H3	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_6	H4	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_5	G1	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_5	G2	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_4	G3	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_4	G4	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_3	F1	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_3	F2	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_2	F3	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_2	F4	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_1	E1	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_1	E2	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_P_0	D1	O_7	DMD, LVDS I/F channel B, differential serial data
DDB_N_0	D2	O_7	DMD, LVDS I/F channel B, differential serial data
PROGRAM MEMORY (Flash and SRAM) INTERFACE			
PM_CSZ_0	D13	O_5	Input Bus D Data bit 3. 100-Ω internal LVDS termination.
PM_CSZ_1	E12	O_5	
PM_CSZ_2	A13	O_5	Input Bus D Data bit 5. 100-Ω internal LVDS termination.
PM_ADDR_22 (GPIO 36)	A12	B_5	
PM_ADDR_21 (GPIO 35)	E11	B_5	Input Bus D Data bit 10. 100-Ω internal LVDS termination.
PM_ADDR_20	D12	O_5	
PM_ADDR_19	C12	O_5	Input Bus D Data bit 11. 100-Ω internal LVDS termination.
PM_ADDR_18	B11	O_5	
PM_ADDR_17	A11	O_5	Input Bus D Data bit 12. 100-Ω internal LVDS termination.
PM_ADDR_16	D11	O_5	
PM_ADDR_15	C11	O_5	Input Bus D Data bit 13. 100-Ω internal LVDS termination.
PM_ADDR_14	E10	O_5	
PM_ADDR_13	D10	O_5	Input Bus D Data bit 14. 100-Ω internal LVDS termination.
PM_ADDR_12	C10	O_5	
PM_ADDR_11	B9	O_5	Input Bus D Data bit 15. 100-Ω internal LVDS termination.
PM_ADDR_10	A9	O_5	

Pin Configurations and Functions (continued)

PIN[1]		I/O[2]	DESCRIPTION
NAME	NO.		
PM_ADDR_9	E9	O_5	Output Bus A Data bit 0 to DMD.
PM_ADDR_8	D9	O_5	
PM_ADDR_7	C9	O_5	Output Bus A Data bit 1 to DMD.
PM_ADDR_6	B8	O_5	
PM_ADDR_5	A8	O_5	Output Bus A Data bit 2 to DMD.
PM_ADDR_4	D8	O_5	
PM_ADDR_3	C8	O_5	Output Bus A Data bit 3 to DMD.
PM_ADDR_2	B7	O_5	
PM_ADDR_1	A7	O_5	Output Bus A Data bit 4 to DMD.
PM_ADDR_0	C7	O_5	
PM_WEZ	B12	O_5	Output Bus A Data bit 5 to DMD.
PM_OEZ	C13	O_5	
PM_BLSZ_1	B6	O_5	Output Bus A Data bit 6 to DMD.
PM_BLSZ_0	A6	O_5	
PM_DATA_15	C17	B_5	Output Bus A Data bit 7 to DMD.
PM_DATA_14	B16	B_5	
PM_DATA_13	A16	B_5	Output Bus A Data bit 8 to DMD.
PM_DATA_12	A15	B_5	
PM_DATA_11	B15	B_5	Output Bus A Data bit 9 to DMD.
PM_DATA_10	D16	B_5	
PM_DATA_9	C16	B_5	Output Bus A Data bit 10 to DMD.
PM_DATA_8	E14	B_5	
PM_DATA_7	D15	B_5	Output Bus A Data bit 11 to DMD.
PM_DATA_6	C15	B_5	
PM_DATA_5	B14	B_5	Output Bus A Data bit 12 to DMD.
PM_DATA_4	A14	B_5	
PM_DATA_3	E13	B_5	Output Bus A Data bit 13 to DMD.
PM_DATA_2	D14	B_5	
PM_DATA_1	C14	B_5	Output Bus A Data bit 14 to DMD.
PM_DATA_0	B13	B_5	
PERIPHERAL INTERFACE			
IIC0_SCL	A10	B_8	I2C Bus 0, Clock. This bus support 400 kHz, fast mode operation. This signal requires an external pull-up to 3.3-V. The minimum acceptable pull-up value is 1 kΩ. This input is not 5 V tolerant.
IIC0_SDA	B10	B_8	2C Bus 0, Data. This bus support 400 kHz, fast mode operation. This signal requires an external pull-up to 3.3-V. The minimum acceptable pull-up value is 1 kΩ. This input is not 5 V tolerant.
SSP0_CLK	AD4	B_5	Synchronous Serial Port 0, clock
SSP0_RXD	AD5	I_4	Synchronous Serial Port 0, receive data in
SSP0_TXD	AB7	O_5	Synchronous Serial Port 0, transmit data out
SSP0_CSZ_0	AC5	B_5	Synchronous Serial Port 0, chip select 0 (active low)
SSP0_CSZ_1	AB6	B_5	Synchronous Serial Port 0, chip select 1 (active low)
SSP0_CSZ_2	AC3	B_5	Synchronous Serial Port 0, chip select 2 (active low)
UART0_TXD	AB3	O_5	UART0 transmit data output
UART0_RXD	AD1	O_5	UART0 receive data input
UART0_RTSZ	AD2	O_5	UART0 ready to send hardware flow control output (active low)
UART0_CTSZ	AE2	I_4	UART0 clear to send hardware flow control input (active low)
USB_DAT_N	C5	B_9	USB D- I/O
USB_DAT_P	D6	B_9	USB D+ I/O
PMD_INTZ	AE8	I_4	Interrupt from DLPA100 (active low). This signal requires an external pull-up. Uses hysteresis.
CW_PWM	AD8	O_5	Color wheel control PWM output
CW_INDEX	AF7	O_5	Color wheel index. Uses hysteresis.
LMPCTRL	AC9	O_5	Lamp control output. Lamp enable and synchronization to the ballast.
LMPSTAT	AF8	I_4	Lamp status input. Driven high from the ballast once the lamp is lit.

Pin Configurations and Functions (continued)

PIN[1]		I/O[2]	DESCRIPTION	
NAME	NO.			
GENERAL PURPOSE I/O (GPIO)[8]			Alternate Function 1	Alternate Function 2
GPIO_82	E3	B_5	N/A	N/A
GPIO_81	AB10	B_2	Reserved	N/A
GPIO_80	AD9	B_2	IR_ENABLE (O)	N/A
GPIO_79	AE9	B_2	Reserved	N/A
GPIO_78	AF9	B_2	FIELD_3D_LR (I)	N/A
GPIO_77	AB11	B_2	SAS_INTGTR_EN (O)	SENSE_PWM_OUT (O)
GPIO_76	AC10	B_2	SAS_CSZ (O)	N/A
GPIO_75	AD10	B_2	SAS_DO (O)	SENSE_FREQ_IN (I)
GPIO_74	AE10	B_2	SAS_DI (I)	SENSE_COMP_IN (I)
GPIO_73	AF10	B_2	SAS_CLK (O)	N/A
GPIO_72	K24	B_2	SSP2_DI (I)	N/A
GPIO_71	K23	B_2	SSP2_CLK (B)	N/A
GPIO_70	K22	B_2	SSP2_CSZ_1 (B)	N/A
GPIO_69	J26	B_2	SSP2_CSZ_0 (B)	N/A
GPIO_68	J25	B_2	SSP2_DO (O)	N/A
GPIO_67	J24	B_2	SP_Data_7 (O)	SSP2_CSZ_2 (B)
GPIO_66	J23	B_2	SP_Data_6 (O)	SSP0_CSZ_5 (B)
GPIO_65	J22	B_2	SP_Data_5 (O)	N/A
GPIO_64	H26	B_2	SP_Data_4 (O)	CW_PWM_2 (O)
GPIO_63	H25	B_2	SP_Data_3 (O)	CW_INDEX_2 (I)
GPIO_62	H24	B_2	SP_Data_2 (O)	SP_VC_FDBK (I)
GPIO_61	H23	B_2	SP_Data_1 (O)	N/A
GPIO_60	H22	B_2	SP_Data_0 (O)	N/A
GPIO_59	G26	B_2	SP_WG_CLK (O)	N/A
GPIO_58	G25	B_2	LED_SENSE_PULSE (O)	N/A
GPIO_57	F25	B_2	Reserved	N/A
GPIO_56	G24	B_2	UART2_RXD (O)	N/A
GPIO_55	G23	B_2	UART2_TXD (O)	N/A
GPIO_54	F26	B_2	PROG_AUX_7 (O)	N/A
GPIO_53	E26	B_2	PROG_AUX_6 (O)	N/A
GPIO_52	AB12	B_2	CSP_Data (O)	ALF_CLAMP (O)
GPIO_51	AC11	B_2	CSP_CLK (O)	ALF_COAST (O)
GPIO_50	V23	B_2	Reserved	HBT_CLKOUT (O)
GPIO_49	V24	B_2	Reserved	HBT_DO (O)
GPIO_48	V25	B_2	Reserved	HBT_CLKIN_2 (I)
GPIO_47	V26	B_2	Reserved	HBT_DI_2 (I)
GPIO_46	T22	B_2	Reserved	HBT_CLKIN_1 (I)
GPIO_45	U23	B_2	Reserved	HBT_DI_1 (I)
GPIO_44	U24	B_2	Reserved	HBT_CLKIN_0 (I)
GPIO_43	U25	B_2	Reserved	HBT_DI_0 (I)
GPIO_42	U26	B_2	Reserved	SSP0_CSZ4 (B)
GPIO_41	R22	B_2	Reserved	DASYNC (I)
GPIO_40	T23	B_2	Reserved	FSD12 (O)
GPIO_39	F24	B_2	SW reserved (Boot Hold)	SW reserved (Boot Hold)
GPIO_38	E25	B_2	SW reserved (USB Enumeration Enable)	SW reserved (USB Enumeration Enable)
GPIO_37	G22	B_2	N/A	N/A
GPIO_36	A12	B_2	PM_ADDR_22 (O)	I2C_2 SDA (B)
GPIO_35	E11	B_2	PM_ADDR_21 (O)	I2C_2 SCL (B)
GPIO_34	F23	B_2	SSP1_CSZ_1 (B)	N/A

(8) GPIO signals must be configured by software for input, output, bidirectional, or open-drain. Some GPIOs have one or more alternate use modes, which are also software configurable. The reset default for all optional GPIOs is as an input signal. However, any alternate function connected to these GPIO pins with the exception of general-purpose clocks and PWM generation, are reset. An external pullup to the 3.3-V supply is required for each signal configured as open-drain. External pullup or pulldown resistors may be required to ensure stable operation before software is able to configure these ports.

Pin Configurations and Functions (continued)

PIN[1]		I/O[2]	DESCRIPTION	
NAME	NO.			
GPIO_33	D26	B_2	SSP1_CSZ_0 (B)	N/A
GPIO_32	E24	B_2	SSP1_DO (O)	N/A
GPIO_31	F22	B_2	SSP1_DI (I)	N/A
GPIO_30	D25	B_2	SSP1_CLK (B)	N/A
GPIO_29	E23	B_2	IR1 (I)	SSP2 BC CSZ (B)
GPIO_28	C26	B_2	IR0 (I)	SSP2 BC CSZ (B)
GPIO_27	AB4	B_2	SSP0_CSZ3 (B)	N/A
GPIO_26	D24	B_2	Blue LED enable (O)	UART2 TXD (O)
GPIO_25	C25	B_2	Green LED enable (O)	LAMPSYNC (O)
GPIO_24	B26	B_2	Red LED enable (O)	N/A
GPIO_23	E21	B_2	LED Dual Current Control (O)	N/A
GPIO_22	D22	B_2	LED Dual Current Control (O)	N/A
GPIO_21	E20	B_2	LED Dual Current Control (O)	N/A
GPIO_20	C23	B_2	N/A	N/A
GPIO_19	D21	B_2	N/A	N/A
GPIO_18	B24	B_2	N/A	N/A
GPIO_17	C22	B_2	General Purpose Clock 2 (O)	N/A
GPIO_16	B23	B_2	General Purpose Clock 1 (O)	N/A
GPIO_15	E19	B_2	I2C_1 SDA (B)	N/A
GPIO_14	D20	B_2	I2C_1 SCL (B)	N/A
GPIO_13	C21	B_2	PWM IN_1 (I)	I2C_2 SDA (B)
GPIO_12	B22	B_2	PWM IN_0 (I)	I2C_2 SCL (B)
GPIO_11	A23	B_2	PWM STD_7 (O)	N/A
GPIO_10	A22	B_2	PWM STD_6 (O)	N/A
GPIO_9	B21	B_2	PWM STD_5 (O)	N/A
GPIO_8	A21	B_2	PWM STD_4 (O)	N/A
GPIO_7	A20	B_2	PWM STD_3 (O)	N/A
GPIO_6	C20	B_2	PWM STD_2 (O)	N/A
GPIO_5	B20	B_2	PWM STD_1 (O)	N/A
GPIO_4	B19	B_2	PWM STD_0 (O)	N/A
GPIO_3	A19	B_2	UART1_RTSZ (O)	N/A
GPIO_2	E18	B_2	UART1_CTSZ (I)	N/A
GPIO_1	D19	B_2	UART1_RXD (I)	N/A
GPIO_0	C19	B_2	UART1_TXD (O)	N/A
CLOCK and PLL SUPPORT				
MOSC	M26	I_{10}	System clock oscillator input (3.3-V LVTTL). Note that MOSC must be stable a maximum of 25ms after POSENSE transitions from low to high.	
MOSCN	N26	O_{10}	MOSC crystal return	
OCLKA	AF6	O_5	General purpose output clock A. Targeted for driving the CW motor controller. The frequency is software programmable. Power-up default 787Khz. Note that the output frequency is not affected by non-power-up reset operations (it will hold the last value programmed).	
DUAL CONTROLLER SUPPORT				
SEQ_SYNC	AB9	B_3	Sequence Sync. This signal is used in multi controller configurations only, in which case the SEQSYNC signal from each controller should be connected together with an external pull-up. This signal should either be pulled high or pulled low and not allowed to float for single controller configurations.	
POWER and GROUND				
VDD33	F20, F17, F11, F8, L21, R21, Y21, AA19, AA16, AA10, AA7	POWER	3.3-V I/O Power	
VDD18	C1, F5, G6, K6, M5, P5, T5, W6, AA5, AE1, H5, N6, T6, AA13, U21, P21, H21, F14	POWER	1.8-V Internal DRAM & LVDS I/O Power	
VDD11	F19, F16, F13, F10, F7, H6, L6, P6, U6, Y6, AA8, AA11, AA14, AA17, AA20, W21, T21, N21, K21, G21, L11, T11, T16, L16	POWER	1.1-V Core Power	
VDD_PLLD	L22	POWER	1.1-V DMD clock generator PLL digital power	
VSS_PLLD	L23	GROUND	1.1-V DMD clock generator PLL digital ground	

Pin Configurations and Functions (continued)

PIN[1]		I/O[2]	DESCRIPTION
NAME	NO.		
VAD_PLLD	K25	POWER	1.8-V DMD clock generator PLL analog power
VAS_PLLD	K26	GROUND	1.8-V DMD clock generator PLL analog ground
VDD_PLLM1	L26	POWER	1.1-V Master-LS clock generator PLL digital power
VSS_PLLM1	M22	GROUND	1.1-V Master-LS clock generator PLL digital ground
VAD_PLLM1	L24	POWER	1.8-V Master-LS clock generator PLL analog power
VAS_PLLM1	L25	GROUND	1.8-V Master-LS clock generator PLL analog ground
VDD_PLLM2	P23	POWER	1.1-V Master-HS clock generator PLL digital power
VSS_PLLM2	P24	GROUND	1.1-V Master-HS clock generator PLL digital ground
VAD_PLLM2	R25	POWER	1.8-V Master-HS clock generator PLL analog power
VAS_PLLM2	R26	GROUND	1.8-V Master-HS clock generator PLL analog ground
VAD_PLLS	R23	POWER	1.1-V video-2X clock generator PLL analog power
VAS_PLLS	R24	GROUND	1.1-V video-2X clock generator PLL analog ground
L-VDQPAD_[7:0], R-VDQPAD_[7:0]	B18, D18, B17, E17, A18, C18, A17, D17, AE17, AC17, AF17, AC18, AB16, AD17, AB17, AD18	RESERVED	These should be tied directly to ground for normal operation.
CFO_VDD33	AE26	RESERVED	This should be tied directly to 3.3 I/O power (VDD33) for normal operation.
VTEST1, VTEST2, VTEST3, VTEST4	AB14, AB15, E15, E16	RESERVED	These should be tied directly to ground for normal operation.
LVDS_AVS1, LVDS_AVS2	V5, K5	POWER	These should be tied directly to ground for normal operation.
VPGM	AC6	POWER	This should be tied directly to ground for normal operation.
GROUND	A26, A25, A24, B25, C24, D23, E22, F21, F18, F15, F12, F9, F6, E5, D4, C3, B3, A3, B2, A2, B1, A1 G5, J5, J6, L5, M6, N5, R5, R6, U5, V6, W5, Y5, AA6, AB5, AC4, AD3, AE3, AF3, AF2, AF1, AA9, AA12, AA15, AA18, AA21, AB22, AC23, AD24, AE24, AF24, AE25, AF25, AF26, V21, M21, J21, L15, L14, L13, L12, M16, M15, M14, M13, M12, M11, N16, N15, N14, N13, N12, N11, P16, P15, P14, P13, P12, P11, R16, R15, R14, R13, R12, R11, T15, T14, T13, T12	GROUND	Common ground

Table 1. I/O Type Subscript Definition

SUBSCRIPT	DESCRIPTION	ESD STRUCTURE
2	3.3 LVTTL I/O Buffer with 8 mA drive	ESD diode to VDD33 and GROUND
3	3.3 LVTTL I/O Buffer, with 12 mA drive	ESD diode to VDD33 and GROUND
4	3.3 LVTTL Receiver	ESD diode to VDD33 and GROUND
5	3.3 LVTTL I/O Buffer with 8 mA drive, with Slew Rate Control	ESD diode to VDD33 and GROUND
6	3.3 LVTTL I/O Buffer, with programmable 4 mA, 8 mA, or 12 mA drive	ESD diode to VDD33 and GROUND
7	1.8 LVDS (DMD I/F)	ESD diode to VDD33 and GROUND
8	3.3 V I2C with 3 mA sink	ESD diode to VDD33 and GROUND
9	USB Compatible (3.3 V)	ESD diode to VDD33 and GROUND
10	OSC 3.3 V I/O Compatible LVTTL	ESD diode to VDD33 and GROUND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
ELECTRICAL				
Supply Voltage(2)	V_{DD11} (Core)	–0.30	1.60	V
	V_{DD18} (LVDS I/O and Internal DRAM)	–0.30	2.50	
	V_{DD33} (I/O)	–0.30	3.90	
	VDD_PLLD (1.1V DMD clock generator - Digital)	-0.30	1.60	
	VDD_PLLM1 (1.1V Master - LS clock generator - Digital)	-0.30	1.60	
	VDD_PLLM2 (1.1V Master - HS clock generator - Digital)	-0.30	1.60	
	VDD_PLLD (1.8V DMD clock generator - Analog)	-0.30	2.50	
	VDD_PLLM1 (1.8V Master - LS clock generator - Analog)	-0.30	2.50	
	VDD_PLLM2 (1.8V Master - HS clock generator - Analog)	-0.30	2.50	
	VDD_PLLS (1.1V Video 2X - Analog)	-0.50	1.40	
V_I Input Voltage(3)	USB	-1.0	5.25	V
	OSC	-0.3	V_{DD33} + 0.3	
	3.3 LVTTL	-0.3	3.6	
	3.3 I2C	-0.5	3.8	
V_O Output Voltage	USB	-1.0	5.25	V
	OSC	-0.3	2.2	
	3.3 LVTTL	-0.3	3.6	
	3.3 I2C	-0.5	3.8	
ENVIRONMENTAL				
T_J Operating Junction temperature		0	111	°C
T_{stg} Storage temperature range		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GROUND.
(3) Applies to external input and bidirectional buffers.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	± 2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	+500/-300	
	Machine Model (MM)	+200/-200	

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		I/O (1)	MIN	NOM	MAX	UNIT
ELECTRICAL						
VDD33	3.3V Supply voltage, I/O		3.135	3.3	3.465	V
VDD18	1.8V Supply voltage, LVDS & DRAM		1.71	1.8	1.89	V
VDD11	1.1V Supply voltage, Core logic		1.045	1.1	1.155	V
VDD_PLLD	1.8V Supply voltage, PLL Analog		1.71	1.8	1.89	V
VDD_PLLM1	1.8V Supply voltage, PLL Analog		1.71	1.8	1.89	V
VDD_PLLM2	1.8V Supply voltage, PLL Analog		1.71	1.8	1.89	V
VDD_PLLS	1.8V Supply voltage, PLL Analog		1.050	1.10	1.150	V
VDD_PLLD	1.8V Supply voltage, PLL Analog		1.045	1.1	1.155	V
VDD_PLLM1	1.8V Supply voltage, PLL Analog		1.045	1.1	1.155	V
VDD_PLLM2	1.8V Supply voltage, PLL Analog		1.045	1.1	1.155	V
V_I	Input Voltage	USB (9)	0		VDD33	V
		OSC (10)	0		VDD33	
		3.3 V LVTTL (1,2,3,4)	0		VDD33	
		3.3 V I^2C (8)	0		VDD33	
v_o	Output Voltage	USB (8)	0		VDD33	V
		3.3 V LVTTL (1,2,3,4)	0		VDD33	
		3.3 V I^2C (8)	0		VDD33	
		1.8 V LVDS (7)	0		VDD33	
T_A	Operating ambient temperature range	See (2)(3)	0		55	°C
T_C	Operating top center case temperature	See (3)(4)	0		109.16	°C
T_J	Operating junction temperature		0		111	°C

(1) The number inside each parenthesis for the I/O refers to the type defined in the I/O type subscript definition section.
(2) Assumes minimum 1 m/s airflow along with the JEDEC thermal resistance and associated conditions listed at www.ti.com/packaging. Thus this is an approximate value that varies with environment and PCB design.
(3) Maximum thermal values assume max power of 4.6 watts.
(4) Assume Psi_{JT} equals 0.4 C/W.

6.4 Thermal Information

THERMAL METRIC (1)		DLPC4422 ZPC (BGA) 516 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	14.4	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	4.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics Application Report*, SPRA953.
(2) In still air.

6.5 Electrical Characteristics(1)

over recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	USB (9)		2.0			V
		OSC (10)		2.0			
		3.3-V LVTTL (1,2,3,4)		2.0			
		3.3-V I^2C (8)		2.4		VDD33+0.5	
V_{IL}	Low-level input voltage	USB (9)				0.8	V
		OSC (10)				0.8	
		3.3-V LVTTL (1,2,3,4)				0.8	
		3.3-V I^2C (8)		-0.5		1.0	
V_{DIS}	Differential Input Voltage	USB(9)		200			mV
V_{ICM}	Differential Cross Point Voltage	USB(9)		0.8		2.5	V
V_{HYS}	Hysteresis (V_{T+}-V_{T-})	USB(9)		200			mV
		3.3-V LVTTL (1,2,3,4)			400		
		3.3-V I^2C (8)		300	550	600	
V_{OH}	High-level output voltage	USB (9)		2.8			V
		1.8-V LVDS (7)		1.520			
		3.3-V LVTTL (1,2,3)	I_{OH} = Max Rated	2.7			
V_{OL}	Low-level output voltage	USB (9)		0.0		0.3	V
		1.8-V LVDS (7)				0.880	
		3.3-V LVTTL (1,2,3)	I_{OL} = Max Rated			0.4	
		3.3-V I^2C (8)	I_{OL} = 3 mA sink			0.4	
V_{OD}	Output Differential Voltage	1.8-V LVDS (7)		0.065		0.440	V
I_{IH}	High-level input current	USB(9)				200	µA
		OSC (10)		-10.0		10	
		3.3-V LVTTL (1-4) without Internal Pull Down	V_{IH} = VDD33	-10.0		10	
		3.3-V LVTTL (1-4) with Internal Pull Down	V_{IH} = VDD33	10.0		200.0	
		3.3-V I^2C (8)	V_{IH} = VDD33			10.0	
I_{IL}	Low-level input current	USB(9)		-10.0		10.0	µA
		OSC (10)		-10.0		10.0	
		3.3-V LVTTL (1-4) without Internal Pull Down	V_{OH} = VDD33	-10.0		10.0	
		3.3-V LVTTL (1-4) with Internal Pull Down	V_{OH} = VDD33	-10.0		-200	
		3.3-V I^2C (8)	V_{OH} = VDD33			-10.0	
I_{OH}	High-level output current	USB(9)				-19.1	mA
		1.8-V LVDS (7) (V_{OD} = 300mV)	VO = 1.4 V	6.5			
		3.3-V LVTTL (1)	VO = 2.4 V	-4.0			
		3.3-V LVTTL (2)	VO = 2.4 V	-8.0			
		3.3-V LVTTL (3)	VO = 2.4 V	-12.0			

(1) The number inside each parenthesis or the I/O refers to the type defined in Table 1.

Electrical Characteristics(1) (continued)

over recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OL}	Low-level output current	USB(9)		19.1			mA
		1.8-V LVDS (7) (V_{OD} = 300mV)	VO = 1.0 V	6.5			
		3.3-V LVTTL (1)	VO = 0.4 V	4.0			
		3.3-V LVTTL (2)	VO = 0.4 V	8.0			
		3.3-V LVTTL (3)	VO = 0.4 V	12.0			
		3.3-V I^2C (8)		3.0			
I_{OZ}	High-Impedance leakage current	USB (9)		-10			pF
		LVDS (7)		-10			
		3.3-V LVTTL (1,2,3)		-10			
		3.3-V I^2C (8)		-10			
C_I	Input capacitance	USB (9)		11.84		17.07	pF
		3.3-V LVTTL (1)		3.75		5.52	
		3.3-V LVTTL (2)		3.75		5.52	
		3.3-V LVTTL (4)		3.75		5.52	
		3.3-V I^2C (8)		5.26		6.54	
I_{CC11}	Supply voltage, 1.1-V core power		Normal Mode			1474	mA
I_{CC18}	Supply voltage, 1.8-V power (LVDS I/O & Internal DRAM)		Normal Mode			1005	mA
I_{CC33}	Supply voltage, 3.3-V I/O power		Normal Mode			33	mA
I_{CC11_PLLD}	Supply voltage, DMD PLL Digital Power (1.1 V)		Normal Mode		4.4	6.2	mA
I_{CC11_PLLM1}	Supply voltage, Master-LS Clock Generator PLL Digital power (1.1 V)		Normal Mode		4.4	6.2	mA
I_{CC11_PLLM2}	Supply voltage, Master-HS Clock Generator PLL Digital power (1.1 V)		Normal Mode		4.4	6.2	mA
I_{CC18_PLLD}	Supply voltage, DMD PLL Analog Power (1.8 V)		Normal Mode		8.0	10.2	mA
I_{CC18_PLLM1}	Supply voltage, Master-LS Clock Generator PLL Analog power (1.8 V)		Normal Mode		8.0	10.2	mA
I_{CC18_PLLM2}	Supply voltage, Master-HS Clock Generator PLL Analog power (1.8 V)		Normal Mode		8.0	10.2	mA
I_{CC11_PLLS}	Supply voltage, Video-2X PLL Analog Power (1.1 V)		Normal Mode			2.9	mA
	Total Power		Normal Mode			3.73	W
I_{CC11}	Supply voltage, 1.1-V core power		Low Power Mode			21	mA
I_{CC18}	Supply voltage, 1.8-V power (LVDS I/O & Internal DRAM)		Low Power Mode			0	mA
I_{CC33}	Supply voltage, 3.3-V I/O power		Low Power Mode			18	mA
I_{CC11_PLLD}	Supply voltage, DMD PLL Digital Power (1.1 V)		Low Power Mode			2.03	mA
I_{CC11_PLLM1}	Supply voltage, Master-LS Clock Generator PLL Digital power (1.1 V)		Low Power Mode			2.03	mA
I_{CC11_PLLM2}	Supply voltage, Master-HS Clock Generator PLL Digital power (1.1 V)		Low Power Mode			2.03	mA
I_{CC18_PLLD}	Supply voltage, DMD PLL Analog Power (1.8 V)		Low Power Mode			5.42	mA
I_{CC18_PLLM1}	Supply voltage, Master-LS Clock Generator PLL Analog power (1.8 V)		Low Power Mode			5.42	mA
I_{CC18_PLLM2}	Supply voltage, Master-HS Clock Generator PLL Analog power (1.8 V)		Low Power Mode			5.42	mA
I_{CC11_PLLS}	Supply voltage, Video-2X PLL Analog Power (1.1 V)		Low Power Mode			.03	mA
	Total Power		Low Power Mode			106	mW

6.6 System Oscillators Timing Requirements

over operating free-air temperature range(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
SYSTEM OSCILLATORS					
f_{clock}	Clock frequency, MOSC(1)		19.998	20.002	MHz
t_c	Cycle time, MOSC(1)		49.995	50.005	MHz
$t_{w(H)}$	Pulse duration(2), MOSC, high	50% to 50% reference points (signal)	20		ns
$t_{w(L)}$	Pulse duration(2), MOSC, low	50% to 50% reference points (signal)	20		ns
t_t	Transition time(2), MOSC, tt = tf /tr	20% to 80% reference points (signal)		12	ns
t_{jp}	Period Jitter(2), MOSC (This is the deviation in period from the ideal period due solely to high frequency jitter).			18	ps

(1) The frequency range for MOSC is 20 MHz with +/-100 PPM accuracy (This shall include impact to accuracy due to aging, temperature and trim sensitivity). The MOSC input can not support spread spectrum clock spreading.
(2) Applies only when driven via an external digital oscillator.

6.7 Test and Reset Timing Requirements

			MIN	MAX	UNIT
$t_{W1(L)}$	Pulse duration, inactive low, PWRGOOD	50% to 50% reference points (signal)	4.0		µs
$t_{W1(L)}$	Pulse duration, inactive low, PWRGOOD	50% to 50% reference points (signal)		1000(1)	ms
t_{t1}	Transition time, PWRGOOD, $t_{t1}= t_f/t_r$	20% to 80% reference points (signal)		625	µs
$t_{W2(L)}$	Pulse duration, inactive low, POSENSE	50% to 50% reference points (signal)	500		µs
$t_{W2(L)}$	Pulse duration, inactive low, POSENSE	50% to 50% reference points (signal)		1000(1)	ms
t_{t2}	Transition time, POSENSE, $t_{t1}= t_f/t_r$	20% to 80% reference points (signal)		25(2)	µs
t_{PH}	Power Hold time, POSENSE remains active after PWRGOOD is de-asserted	20% to 80% reference points (signal)	500		µs
t_{EW}	Early Warning time, PWRGOOD goes inactive low prior to any power supply voltage going below its specification		500		µs
$t_{W1(L)}+t_{W2(L)}$	The sum of PWRGOOD and POSENSE inactive time			1050(1)	ms

(1) With 1.8 V power applied. If the 1.8 V power is disabled by the controller command (For example – if system is placed in Low Power mode where the controller disables 1.8 V power), these signals can be placed and remain in their inactive state indefinitely.
(2) As long as noise on this signal is below the hysteresis threshold.

6.8 JTAG Interface: I/O Boundary Scan Application Timing Requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency, TCK			10	MHZ
t_C	Cycle time, TCK		100		ns
$t_{W(H)}$	Pulse duration, high	50% to 50% reference points (signal)	40		ns
$t_{W(L)}$	Pulse duration, low	50% to 50% reference points (signal)	40		ns
t_t	Transition time, $t_t = t_f/t_r$	20% to 80% reference points (signal)		5	ns
t_{SU}	Setup time, TDI valid before TCK↑		8		ns
t_h	Hold time, TDI valid after TCK↑		2		ns
t_{SU}	Setup time, TMS1 valid before TCK↑		8		ns
t_h	Hold time, TMS1 valid before TCK↑		2		ns

6.9 Port 1 Input Pixel Timing Requirements

		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, P_CLK1, P_CLK2, P_CLK3 (30-bit bus)		12	175	MHz
f_{clock}	Clock frequency, P_CLK1, P_CLK2, P_CLK3 (60-bit bus)		12	160	MHz
t_C	Cycle Time, P_CLK1, P_CLK2, P_CLK3		5.714	83.33	ns
$t_{W(H)}$	Pulse Duration, high	50% to 50% reference points (signal)	2.3		ns
$t_{W(L)}$	Pulse Duration, low	50% to 50% reference points (signal)	2.3		ns
t_{jp}	Clock period jitter, P_CLK1, P_CLK2, P_CLK3	Max f_{clock}		See (1)	ps
t_t	Transition time, $t_t=t_f/t_r$, P_CLK1, P_CLK2, P_CLK3	20% to 80% reference points (signal)	0.6	2.0	ns
t_t	Transition time, $t_t=t_f/t_r$, P1_A(9-0), P1_B(9-0), P1_C(9-0), P1_HSYNC, P1_VSYNC, P1_DATAEN	20% to 80% reference points (signal)	0.6	3.0	ns
t_t	Transition time, $t_t=t_f/t_r$, ALF_HSYNC, ALF_VSYNC, ALF_CSYNC (2)	20% to 80% reference points (signal)	0.6	3.0	ns
SETUP AND HOLD TIMES					
t_{su}	Setup time, P1_A(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_h	Hold time, P1_A(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_{su}	Setup time, P1_B(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_h	Hold time, P1_B(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_{su}	Setup time, P1_C(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_h	Hold time, P1_C(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_{su}	Setup time, P1_VSYNC, valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_h	Hold time, P1_VSYNC valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_{su}	Setup time, P1_HSYNC, valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_h	Hold time, P1_HSYNC valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_{su}	Setup time, P2_A(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns

(1) For frequencies (fclock) less than 175 MHZ, use following formula to obtain the jitter: Max Clock Jitter = +/- [$(1/f_{clock})$ – 5414 ps]
(2) ALF_CSYNC, ALF_VSYNC and ALF_HSYNC are Asynchronous signals.

Port 1 Input Pixel Timing Requirements (continued)

		TEST CONDITIONS	MIN	MAX	UNIT
t_h	Hold time, P2_A(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_{su}	Setup time, P2_B(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_h	Hold time, P2_B(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_{su}	Setup time, P2_C(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_h	Hold time, P2_C(9-0), valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_{su}	Setup time, P2_VSYNC, valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_h	Hold time, P2_VSYNC valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_{su}	Setup time, P2_HSYNC, valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_h	Hold time, P2_HSYNC valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_{su}	Setup time, P_DATAEN1, valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_h	Hold time, P_DATAEN1 valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_{su}	Setup time, P_DATAEN2, valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
t_h	Hold time, P_DATAEN2 valid before P_CLK1↑↓, P_CLK2↑↓, or P_CLK3↑↓		0.8		ns
$t_{w(A)}$	VSYNC Active Pulse Width		1		Video Line
$t_{w(A)}$	HSYNC Active Pulse Width		16		Pixel Clocks

6.10 Port 3 Input Pixel Interface (via GPIO) Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock Frequency, P3_CLK		27	54	MHz
t_c	Cycle time, P3_CLK		18.5	37.1	ns
$t_{W(H)}$	Pulse Duration, high	50% to 50% reference points (signal)	7.4		ns
$t_{W(L)}$	Pulse Duration, low	50% to 50% reference points (signal)	7.4		ns
t_{jp}	Clock period jitter, P3_CLK	Max f_{clock}	See (1)	See (1)	ps
t_t	Transition time, $t_t = t_f/t_r$, P3_CLK	20% to 80% reference points (signal)	1.0	5.0	ns
t_t	Transition time, $t_t = t_f/t_r$, P3_DATA(9-0)	20% to 80% reference points (signal)	1.0	5.0	ns
t_{su}	Setup time, P3_DATA(9-0) valid before P3_CLK↑↓		2.0		ns
t_h	Hold time, P3_DATA(9-0) valid after P3_CLK↑↓		2.0		ns

(1) For frequencies less than 54 MHZ, use following formula to obtain the jitter: Jitter = [(1/F) – 5414 ps].

6.11 DMD LVDS Interface Timing Requirements

		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock}	Clock frequency, DCK_A	N/A	DCK_A	100	400	MHz
t_C	Cycle time, DCK_A (1)	N/A	DCK_A	2475.3		ps
$t_{W(H)}$	Pulse duration, high	N/A	DCK_A	1093		ps
$t_{W(L)}$	Pulse duration, low	N/A	DCK_A	1093		ps
t_t	Transition time, $t_t = t_f/t_r$	N/A	DCK_A	100	400	ps
t_{osu}	Output Setup time at max clock rate (2)	DCK_A↑↓	SCA, DDA(15:0)	438		ps
t_{oh}	Output hold time at max clock rate (2)	DCK_A↑↓	SCA, DDA(15:0)	438		ps
f_{clock}	Clock frequency, DCK_B	N/A	DCK_B	100	400	MHz
t_C	Cycle time, DCK_B (1)	N/A	DCK_B	2475.3		ps
$t_{W(H)}$	Pulse duration, high	N/A	DCK_B	1093		ps
$t_{W(L)}$	Pulse duration, low	N/A	DCK_B	1093		ps
t_t	Transition time, $t_t = t_f/t_r$	N/A	DCK_B	100	400	ps
t_{osu}	Output Setup time at max clock rate (2)	DCK_B↑↓	SCA, DDB(15:0)	438		ps
t_{oh}	Output hold time at max clock rate (2)	DCK_B↑↓	SCA, DDB(15:0)	438		ps
t_{sk}	Output Skew, Channel A to Channel B	DCK_A↑	DCK_B↑		250	ps

(1) The minimum cycle time (t_c) for DCK_A and DCL_B includes 1.0% spread spectrum modulation. User must verify that DMD can support this rate.
(2) Output Setup & Hold times for DMD clock frequencies below the maximum can be calculated as follows: t_{osu}(fclock) = t_{osu}(fmax) + 250000*(1/fclock – 1/400) & t_{oh}(fclock) = t_{oh}(fmax) + 250000*(1/fclock – 1/400) where fclock is in MHz.

6.12 Synchronous Serial Port (SSP) Interface Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
SSP MASTER					
t_{su}	Setup time, SSPx_DI valid before SSPx_CLK		15		ns
t_{su}	Setup time, SSPx_DI valid before SSPx_CLK		15		ns
t_h	Hold time, SSPx_DI valid after SSPx_CLK		0		ns
t_h	Hold time, SSPx_DI valid after SSPx_CLK		0		ns
t_t	Transition time, SSPx_DI, $t_t = t_f/t_r$	20% to 80% reference points (signal)		1.5	ns
SSP SLAVE					
t_{su}	Setup time, SSPx_DI valid before SSPx_CLK		12		ns
t_{su}	Setup time, SSPx_DI valid before SSPx_CLK		12		ns
t_h	Hold time, SSPx_DI valid after SSPx_CLK		12		ns
t_h	Hold time, SSPx_DI valid after SSPx_CLK		12		ns
t_t	Transition time, SSPx_DI, $t_t = t_f/t_r$	20% to 80% reference points (signal)		1.5	ns

6.13 Programmable Output Clocks Switching Characteristics

over operating free air temperature range, C_L(min timing) = 5 pF, C_L(max timing) = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock}	Clock frequency, OCLKA (1)		OCLKA	0.787	50	MHz
t_C	Cycle Time, OCLKA		OCLKA	20	1270.6	ns
$t_{W(H)}$	Pulse Duration, high (2)	50% to 50% reference points (signal)	OCLKA	(t_C/2_-2)		ns
$t_{W(L)}$	Pulse Duration, low (2)	50% to 50% reference points (signal)	OCLKA	(t_C/2_-2)		ns
	Jitter		OCLKA		350	ps
f_{clock}	Clock frequency, OCLKB (1)		OCLKB	0.787	50	MHz
t_C	Cycle Time, OCLKB		OCLKB	20	1270.6	ns
$t_{W(H)}$	Pulse Duration, high (2)	50% to 50% reference points (signal)	OCLKB	(t_C/2_-2)		ns
$t_{W(L)}$	Pulse Duration, low (2)	50% to 50% reference points (signal)	OCLKB	(t_C/2_-2)		ns
	Jitter		OCLKB		350	ps
f_{clock}	Clock frequency, OCLKC (1)		OCLKC	0.787	50	MHz
t_C	Cycle Time, OCLKC (2)		OCLKC	20	1270.6	ns
$t_{W(H)}$	Pulse Duration, high	50% to 50% reference points (signal)	OCLKC	(t_C/2_-2)		ns
$t_{W(L)}$	Pulse Duration, low (2)	50% to 50% reference points (signal)	OCLKC	(t_C/2_-2)		ns
	Jitter		OCLKC		350	ps

(1) The frequency of OCLKA thru OCLKC is programmable.
(2) The Duty Cycle of OCLKA thru OCLKC will be within +/- 2 ns of 50%.

6.14 Synchronous Serial Port Interface (SSP) Switching Characteristics

over operating free-air temperature range, C_L(min timing) = 5 pF, C_L(max timing) = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock}	Clock Frequency, SSPx_CLK		N/A	SSPx_CLK	73	25000	kHz
t_c	Cycle time, SSPx_CLK		N/A	SSPx_CLK	0.040	13.6	µs
$t_{W(H)}$	Pulse Duration, high	50% to 50% reference points (signal)	N/A	SSPx_CLK	40%		
$t_{W(L)}$	Pulse Duration, low	50% to 50% reference points (signal)	N/A	SSPx_CLK	40%		
SSP Master (1)							
t_{pd}	Output Propagation, Clock to Q, SSPx_DO (2)		SSPx_CLK↓	SSPx_DO	-5	5	ns
t_{pd}	Output Propagation, Clock to Q, SSPx_DO (2)		SSPx_CLK↑	SSPx_DO	-5	5	ns
SSP Slave (1)							
t_{pd}	Output Propagation, Clock to Q, SSPx_DO (2)		SSPx_CLK↓	SSPx_DO	0	34	ns
t_{pd}	Output Propagation, Clock to Q, SSPx_DO (2)		SSPx_CLK↑	SSPx_DO	0	34	ns

(1) The SSP can be used as an SSP Master, or as an SSP Slave. When used as a Master, the SSP can be configured to sample DI with the same internal clock edge used to transmit the next DO. This essentially provides a full cycle rather than a half cycle timing path, allowing operation at higher SPI clock frequencies.
(2) The SSP can be configured into four different operational modes/configurations.

Table 2. SSP Clock Operational Modes

SPI Clocking Mode	SPI Clock Polarity (CPOL)	SPI Clock Phase (CPHA)
0	0	0
1	0	1
2	1	0
3	1	1

6.15 JTAG Interface: I/O Boundary Scan Application Switching Characteristics

over operating free-air temperature range, C_L(min timing) = 5 pF, C_L(max timing) = 85 pF (unless otherwise noted)

PARAMETER		FROM INPUT	TO OUTPUT	MIN	MAX	UNIT
t_{pd}	Output Propagation, Clock to Q	TCK↓	TDO1	3	12	ns

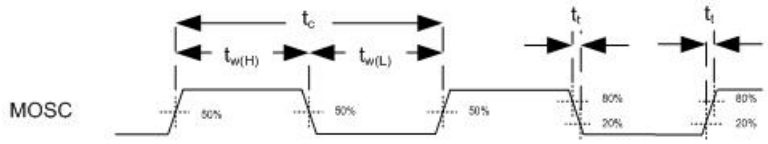


Figure 1. System Oscillators

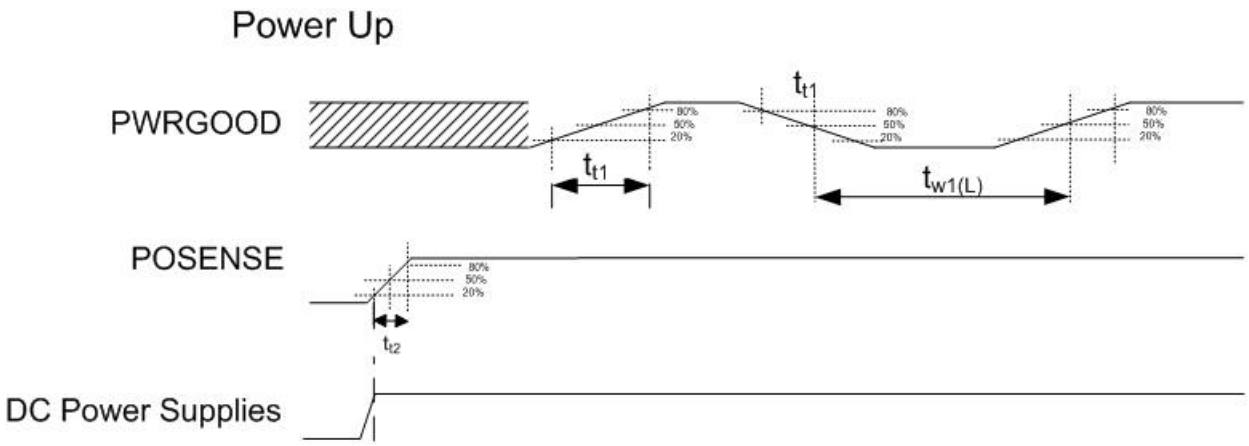


Figure 2. Power Up

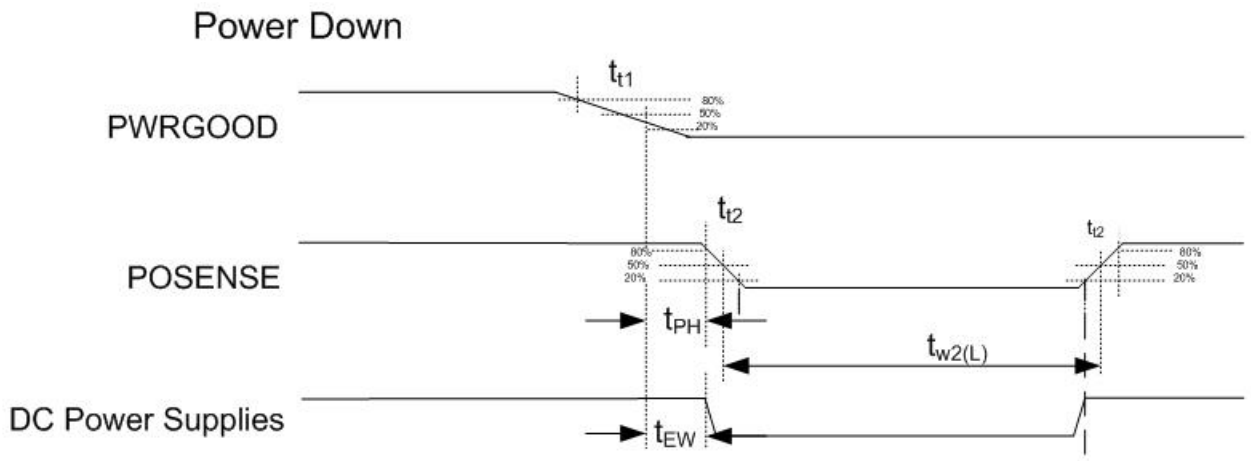


Figure 3. Power Down

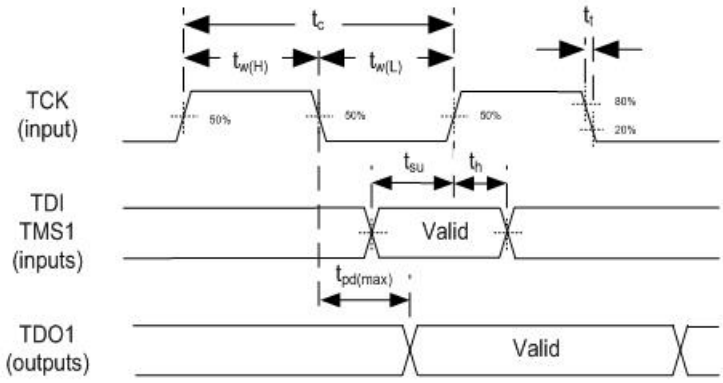


Figure 4. I/O Boundary Scan

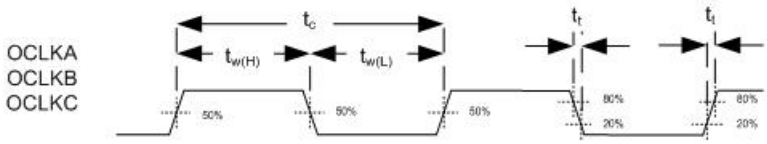


Figure 5. Programmable Output Clocks

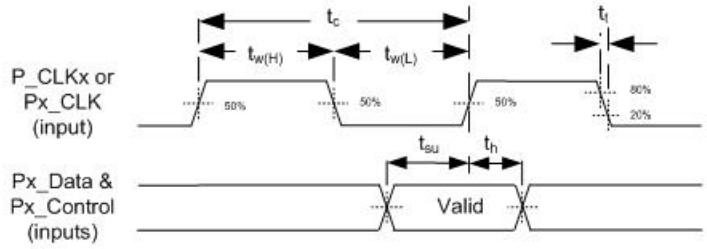


Figure 6. Port1, Port2, and Port3 Input Interface

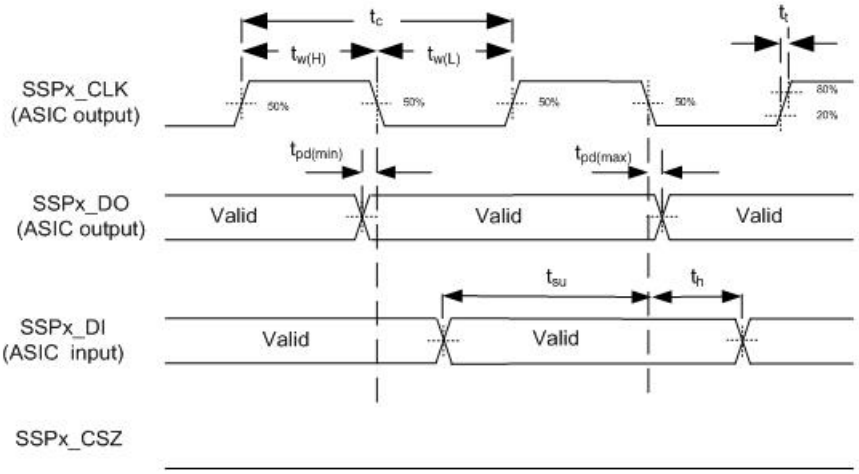


Figure 7. Synchronous Serial Port Interface - Master

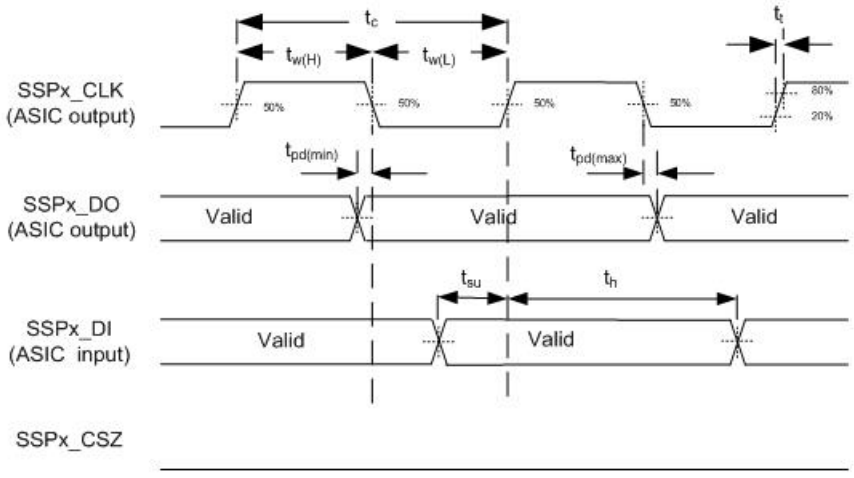


Figure 8. Synchronous Serial Port Interface - Slave

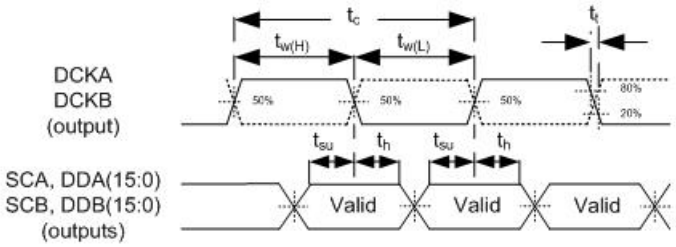


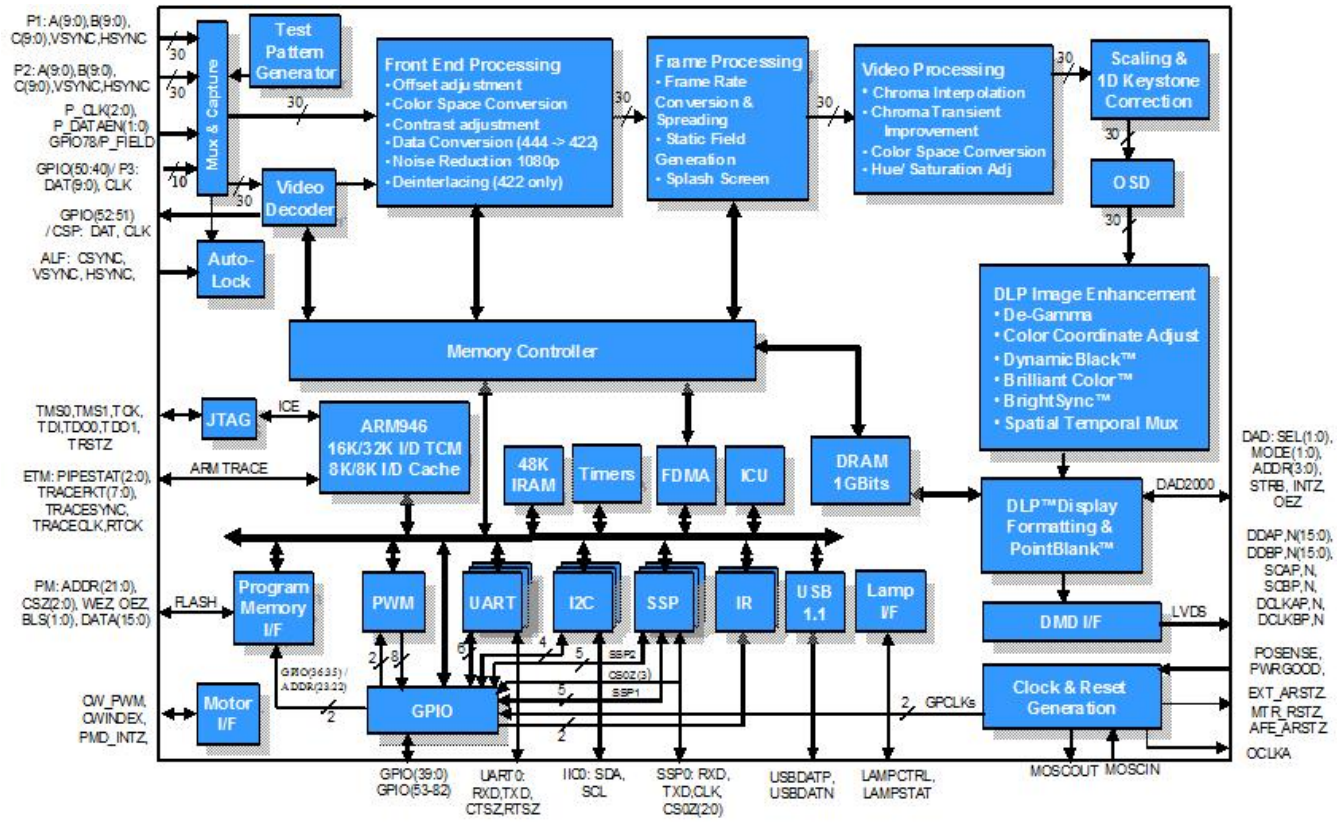
Figure 9. DMD LVDS Interface

7 Detailed Description

7.1 Overview

As with prior DLP® electronics solutions, image data is 100% digital from the DLPC4422 input port to the image projected on to the display screen. The image stays in digital form and is never converted into an analog signal. The DLPC4422 processes the digital input image and converts the data into bit-plane format as needed by the DMD. The DLPC4422 display controller is optimized for high-resolution and high-brightness display applications. Applications include 4K UHD display applications, smart lighting, digital signage, and Laser TV.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 System Reset Operation

7.3.1.1 Power-up Reset Operation

Immediately following a power-up event, DLPC4422 hardware automatically brings up the Master PLL and places the ASIC in normal power mode. It then follows the standard system reset procedure (see *System Reset Operation*).

7.3.1.2 System Reset Operation

Immediately following any type of system reset (Power-up reset, PWRGOOD reset, watchdog timer timeout, lamp-strike reset, etc), the DLPC4422 device shall automatically return to NORMAL power mode and return to the following state:

- All GPIO will tri-state.
- The Master PLL will remain active (it is reset only after a power-up reset sequence) and most of the derived clocks are active. However, only those resets associated with the ARM9 processor and its peripherals will be released (The ARM9 is responsible for releasing all other resets).

Feature Description (continued)

- ARM9 associated clocks default to their full clock rates. (Boot-up is a full speed)
- All front end clocks derived are disabled.
- The PLL feeding the LVDS DMD I/F (PLLD) defaults to its power-down mode and all derived clocks are inactive with corresponding resets asserted (The ARM9 is responsible for enabling these clocks and releasing associated resets).
- LVDS I/O defaults to its power-down mode with outputs tri-stated.
- All resets output by the DLPC4422 device remain asserted until released by the ARM9. (after boot-up)
- The ARM9 processor boots-up from external flash.

When the ARM9 boots-up, the ARM9 API:

- Configures the programmable DDR Clock Generator (DCG) clock rates (i.e. the DMD LVDS I/F rate)
- Enables the DCG PLL (PLLD) while holding divider logic in reset
- When the DCG PLL locks, ARM9 software sets DMD clock rates
- API software then releases DCG divider logic resets, which in turn, enable all derived DCG clocks
- Release external resets

Application software then typically waits for a wake-up command (through the soft power switch on the projector) from the end user. When the projector is requested to wake-up, the software places the ASIC back in normal mode, re-initialize clocks, and resets as required.

7.3.2 Spread Spectrum Clock Generator Support

The DLPC4422 controller supports limited, internally-controlled, spread spectrum clock spreading on the DMD interface. The purpose of this is to frequency spread all signals on this high-speed, external interface to reduce EMI emissions. Clock spreading is limited to triangular waveforms. The DLPC4422 controller provides modulation options of 0%, +/-0.5% and +/-1.0% (center-spread modulation).

7.3.3 GPIO Interface

The DLPC4422 controller provides 83 software-programmable, general-purpose I/O pins. Each GPIO pin is individually configurable as either input or output. In addition, each GPIO output can be either configured as push-pull or open-drain. Some GPIO have one or more alternate-use modes, which are also software configurable. The reset default for all GPIO is as an input signal. However, any alternate function connected to these GPIO pins, with the exception of general purpose clocks and PWM generation, will be reset. When configured as open-drain, the outputs must be externally pulled-up (to the 3.3V supply). External pull-up or pull-down resistors may be required to ensure stable operation before software is able to configure these ports.

7.3.4 Source Input Blanking

Vertical and horizontal blanking requirements for both input ports are defined as follows (See *Video Timing Parameter Definitions*).

- Minimum port 1 and port 2 vertical blanking
  - Vertical back porch: 370 µs
  - Vertical front porch: 1 line
  - Total vertical blanking: 370 µs + 2 lines
- Minimum port 3 vertical blanking
  - Vertical back porch: 370 µs
  - Vertical front porch: 0 lines
  - Total vertical blanking: 370 µs+ 2 lines
- Minimum port1, port 2, and port 3 horizontal blanking
  - Horizontal back porch (HBP): 10 pixels
  - Horizontal front porch (HFP): 0 pixels
  - Total horizontal blanking (THB): 80 pixels

Feature Description (continued)

7.3.5 Video Graphics Processing Delay

The DLPC4422 controller introduces a variable number of field/ frame delays dependent on the source type and selected processing steps performed on the source. For optimum audio/ video synchronization this delay must be matched in the audio path. The following tables define various video delay scenarios to aid in audio matching.

Frame and Fields in table refer to source frames and fields.

- For 2-D sources, “N” is defined to be the ratio of the primary channel source frame rate (or field rate for interlaced video) to the display frame/ field rate.
- For 3-D sources, “M” is defined to be the ratio of the primary channel source frame rate (or field rate for interlaced video) required to obtain both the left and right image, to the display frame/field rate (The rate at which each eye is displayed).

Table 3. Primary Channel/Video-Graphics Processing Delay

Source	3D Video Decoder	De-Interlacing	Frame Rate Conversion	FRC Type	Formatter Buffer	Total Delay
50 to 60 Hz Interlaced SDTV Video	Disabled	Disabled	2 Fields	Sync (1:4)	M Fields	2 + M Fields
60Hz Progressive Video	Disabled	Disabled	2 Frames	Sync (1:4)	M Frames	2 + M Frames
120Hz Progressive Video	Disabled	Disabled	2 Frames	Sync (1:2)	M Frames	2 + M Frames
24Hz 1080p	Disabled	Disabled	1 Frame	Sync (1:6)	M Frames	1 + M Frames
50 to 60 Hz (720p, 1080p)	Disabled	Disabled	1 Frame	Sync (1:2)	M Frames	1 + M Frames
50 to 60 Hz 1080p	Disabled	Disabled	1 Frame	Sync (1:2)	M Frames	1 + M Frames
60Hz Interlaced Graphics (VGA-WUXGA)	Disabled	Disabled	1 Field	Sync (1:4)	M Frames	1 + M Frames
60 Hz Graphics	Disabled	Disabled	1 Frame	Sync (1:4)	M Frames	1 + M Frames
120 Hz Graphics	Disabled	Disabled	1 Frame	Sync (1:2)	M Fields	1 + M Fields
50 to 60 Hz Interlaced	Disabled	Disabled	1 Field	Sync(1:2)	M Fields	1 + M Fields
50 to 60 Hz Progressive	Disabled	Disabled	1 Frame	Sync(1:2)	M Frames	1 + M Frames

7.3.6 Program Memory Flash/SRAM Interface

The DLPC4422 controller provides three external program memory chip selects:

- PM_CSZ_0 – available for optional SRAM or flash device (≤ 128 Mb)
- PM_CSZ_1 – dedicated CS for boot flash device (ie. Standard NOR-type flash, ≤ 128 Mb)
- PM_CSZ_2 – available for optional SRAM or flash device (≤ 128 Mb)

Flash and SRAM access timing is software programmable up to 31 wait states. Wait state resolution is 6.7 ns in normal mode and 53.33 ns in low power modes. Wait state program values for typical flash access times are shown in the Table 4.

Table 4. Wait State Program Values for Typical Flash Access Times

	Normal Mode (1)	Low Power Mode (1)
Formula to Calculate the Required Wait State Value	= Roundup (Device_Access_Time / 6.7 ns)	= Roundup (Device_Access_Time / 53.33 ns)
Max Supported Device Access Time	207 ns	1660 ns

(1) Assumes a maximum single direction trace length of 75 mm.

Note that when another device such as an SRAM or additional flash is used in conjunction with the boot flash, care must be taken to keep stub length short and located as close as possible to the flash end of the route.

The DLPC4422 controller provides enough Program Memory Address pins to support a flash or SRAM device up to 128 Mb. For systems not requiring this capacity, up to two address pins can be used as GPIO instead. Specifically, the two most significant address bits (i.e. PM_ADDR_22 and PM_ADDR_21) are shared on pins GPIO_36 and GPIO_35 respectively. Like other GPIO pins, these pins float in a high-impedance input state following reset; therefore, if these GPIO pins are to be reconfigured as Program Memory Address pins, they require board-level pull-down resistors to prevent any flash address bits from floating until software is able to reconfigure the pins from GPIO to Program Memory Address. Also note that until software reconfigures the pins from GPIO to Program Memory Address, upper portions of flash memory are not accessible.

Table 5 shows typical GPIO_35 and GPIO36 pin configuration for various flash sizes.

Table 5. Typical GPIO_35 and GPIO_36 Pin Configurations for Various Flash Sizes

FLASH SIZE	GPIO_36 Pin Configuration	GPIO_35 Pin Configuration
32 Mb or less	GPIO_36	GPIO_35
64 Mb	GPIO_36	PM_ADDR_21 (1)
128 Mb	PM_ADDR_22 (1)	PM_ADDR_21 (1)

(1) Board-level pulldown resistor required.

7.3.7 Calibration and Debug Support

The DLPC4422 controller contains a test point output port, TSTPT_(7:0), which provides selected system calibration support as well as ASIC debug support. These test points are inputs while reset is applied and switch to outputs when reset is released. The state of these signals is sampled upon the release of system reset and the captured value configures the test mode until the next time reset is applied. Each test point includes an internal pull-down resistor and thus external pull-ups are used to modify the default test configuration. The default configuration (x00) corresponds to the TSTPT_(7:0) outputs being driven low for reduce switching activity during normal operation. For maximum flexibility, an option to jumper to an external pull-up is recommended for TSTPT_(3:0). Note that adding pull-up to TSTPT_(7:4) may have adverse affects for normal operation and are not recommended. Note that these external pull-ups are only sampled upon a zero to one transition on POSENSE and thus changing their configuration after reset has been released will not have any effect until the next time reset is asserted and released. Table 6 defines the test mode selection for 3 of the 16 programmable scenarios defined by TSTPT_(3:0):

Table 6. Test Mode Selection

	No Switching Activity	System Calibration	ARM Debug Signal Set
TSTPT(3:0) Capture Value	**x0**	**x8**	**x1**
TSTPT(0)	0	Vertical Sync	ARM9_Debug (0)
TSTPT(1)	0	Delayed CW Index	ARM9_Debug (1)
TSTPT(2)	0	Sequence Index	ARM9_Debug (2)
TSTPT(3)	0	CW Spoke Test Pt	ARM9_Debug (3)
TSTPT(4)	0	CW Revolution Test Pt	ARM9_Debug (4)
TSTPT(5)	0	Reset Seq. Aux Bit 0	ARM9_Debug (5)
TSTPT(6)	0	Reset Seq. Aux Bit 1	ARM9_Debug (6)
TSTPT(7)	0	Reset Seq. Aux Bit 2	ARM9_Debug (7)

7.3.8 Board Level Test Support

The in-circuit tri-state enable signal (ICTSEN) is a board level test control signal. By driving ICTSEN to a logic high state, all ASIC outputs (except TDO1 and TDO2) will be tri-stated.

The DLPC4422 controller also provides JTAG boundary scan support on all I/O except non-digital I/O and a few special signals. Table 7 defines these exceptions.

Table 7. DLPC4422 -Signals Not Covered by JTAG

Signal Name	PKG Ball
HW_TEST_EN	M25
MOSC	M26
MOSCN	N26
USB_DAT_N	C5
USB_DAT_P	D6
TCK	N24
TDI	N25
TRSTZ	M23
TDO1	N23
TDO2	N22
TMS1	P25
TMS2	P26

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLPC4422 display controller is part of the DLP660TE chipset. The controller integrates all system image processing and control and DMD data formatting onto a single integrated circuit (IC). It will support LED, Lamp, or Hybrid illumination systems, and it also includes multiple image processing algorithms such as DynamicBlack™ or BrilliantColor™. Applications of interest include 4K UHD display applications, Laser TV, digital signage and projection mapping.

8.2 Typical Application

The DLPC4422 controller is ideal for applications requiring high brightness and high resolution displays. When two DLPC4422 display controllers are combined with the DLP660TE DMD, an FPGA, a power management and motor driver device (DLPA100), and other electrical, optical and mechanical components the chipset enables bright, affordable, full 4K UHD display solutions. A typical 4K UHD system application using the DLPC4422 controller and DLP660TE DMD is shown in Figure 10.

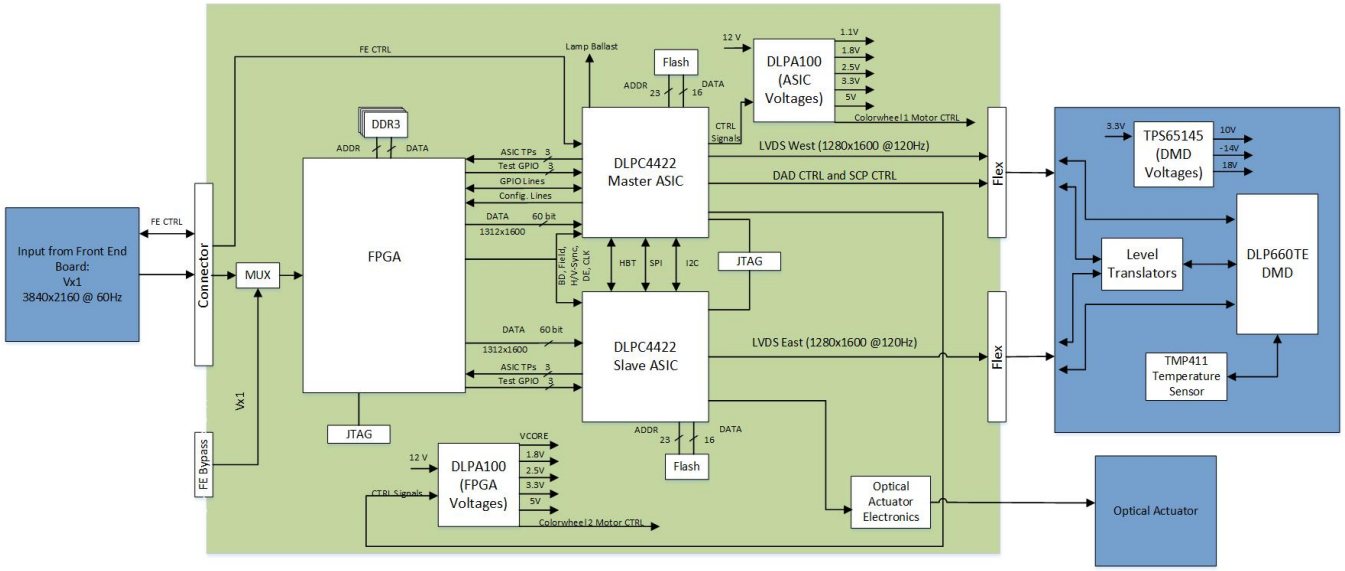


Figure 10. Typical 4K UHD Display Application

8.2.1 Design Requirements

The display controller is the digital interface between the DMD and the rest of the system. The display controller takes digital input from front end digital receivers and drives the DMD over a high speed interface. The display controller also generates the necessary signals (data, protocols, timings) required to display images on the DMD. Some systems require a dual controller to format the incoming data before sending it to the DMD. Reliable operation of the DMD is only insured when the DMD and the controller are used together in a system. In addition to the DLP devices in the chipset, other devices may be needed. Typically a Flash part is needed to store the software and firmware.

Typical Application (continued)

8.2.1.1 Recommended MOSC Crystal Oscillator Configuration

Table 8. Crystal Port Characteristics

PARAMETER	NOMINAL	UNIT
MOSC TO GROUND Capacitance	1.5	pF
MOSCZ TO GROUND Capacitance	1.5	pF

Table 9. Recommended Crystal Configuration

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (1st Harmonic)	
Crystal nominal frequency	20	MHz
Crystal frequency temperature stability	+/- 30	PPM
Overall crystal frequency tolerance (including accuracy, stability, aging, and trim sensitivity)	+/- 100	PPM
Crystal Equivalent Series Resistor (ESR)	50 max	Ω
Crystal load	20	pF
Crystal shunt load	7 max	pF
RS drive resistor (nominal)	100	Ω
RFB feedback resistor (nominal)	1	MΩ
CL1 external crystal load capacitor (MOSC)	See (1)	pF
CL2 external crystal load capacitor (MOSCN)	See (1)	pF
PCB layout	TI recommends a ground isolation ring around the crystal.	

(1) Typical drive level with the XSA020000FK1H-OCX Crystal (ESRmax = 40 Ω) = 50 μW.

C_L = Crystal load capacitance (Farads)
$C_{L1} = 2 * (C_L – C_{Stray\text{-}MOSC})$
$C_{L2} = 2 * (C_L – C_{Stray\text{-}MOSCN})$
$C_{Stray\text{-}MOSC}$ = Sum of Package & PCB capacitance at the crystal pin associated with ASIC signal MOSC.
$C_{Stray\text{-}MOSCN}$ = Sum of Package & PCB capacitance at the crystal pin associated with ASIC signal MOSCN.

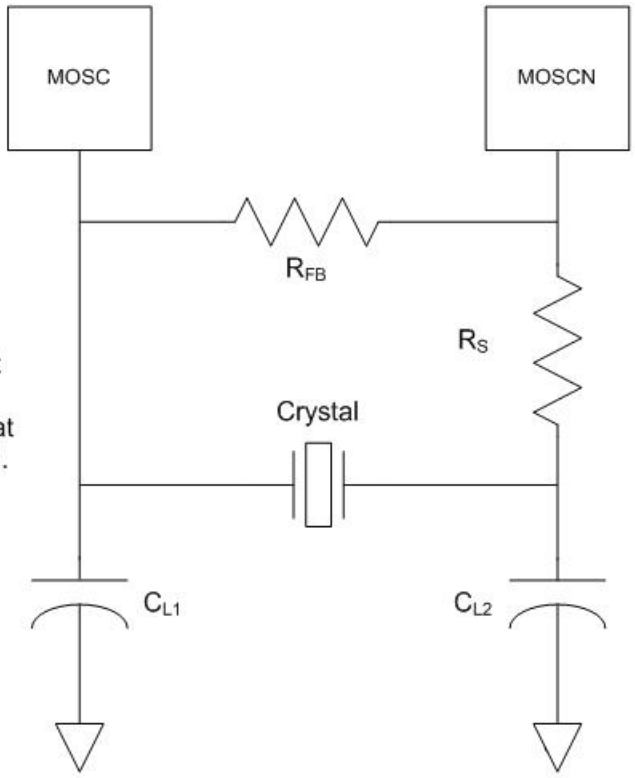


Figure 11. Recommended Crystal Oscillator Configuration

It is assumed that the external crystal oscillator will stabilize within 50 ms after stable power is applied.

8.2.2 Detailed Design Procedure

For connecting the DLPC4422 controller and the DLP660TE DMD together, see the reference design schematic. Layout guidelines should be followed to achieve a reliable projector. To complete the DLP system, an optical module or light engine is required that contains the DLP660TE DMD, associated illumination sources, optical elements, and necessary mechanical components.

9 Power Supply Recommendations

9.1 System Power Regulations

TI strongly recommends that the VDD18_PLLD, VDD18_PLLM1, and VDD18_PLLM2 power feeding internal PLLs be derived from an isolated linear regulator in order to minimize the AC Noise component. It is acceptable for VDD11_PLLD, VDD11_PLLM1, VDD11_PLLM2, and VDD11_PLLS to be derived from the same regulator as the core VDD11, but they should be filtered.

9.2 System Power-Up Sequence

Although the DLPC4422 controller requires an array of power supply voltages (1.1 V, 1.8 V, 3.3 V), there are no restrictions regarding the relative order of power supply sequencing. This is true for both power-up and power-down scenarios. Similarly, there is no minimum time between powering-up or powering-down the different supplies feeding the DLPC4422 controller. However, note that it is not uncommon for there to be power sequencing requirements for the devices that share the supplies with the DLPC4422 controller.

- 1.1-V core power should be applied whenever any I/O power is applied. This ensures the state of the associated I/O that are powered are controlled to a known state. Thus, TI recommends apply core power first. Other supplies should be applied only after the 1.1-Vcore has ramped up.
- All DLPC4422 device power should be applied before POSENSE is asserted to ensure proper power-up initialization is performed.

It is assumed that all DLPC4422 device power-up sequencing is handled by external hardware. It is also assumed that an external power monitor will hold the DLPC4422 device in system reset during power-up (i.e. POSENSE = 0). During this time all DLPC4422 device I/O will be tri-stated. The master PLL (PLLM1) is released from reset upon the low to high transition of POSENSE but the DLPC4422 device keeps the rest of the device in reset for an additional 60 ms to allow the PLL to lock and stabilize its outputs. After this 60 ms delay the ARM-9 related internal resets will be de-asserted causing the microprocessor to begin its boot-up routine.

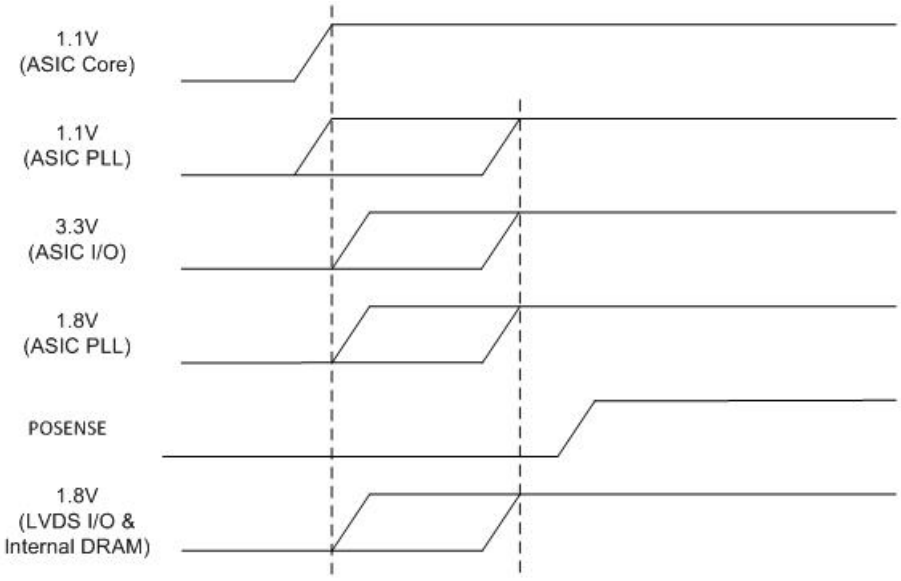


Figure 12. System Power-Up Sequence

9.3 Power-On Sense (POSENSE) Support

It is difficult to set up a power monitor to trip exactly on the DLPC4422 device minimum supply voltage spec. Thus for practical reasons, TI recommends that the external power monitor generating POSENSE target its threshold to 90% of the minimum supply voltage specs and ensure that POSENSE remain low a sufficient amount of time for all supply voltages to reach minimum device requirements and stabilize. Note that the trip voltage for detecting the loss of power, as well as the reaction time to respond to a low voltage condition is not critical for POSENSE as PWRGOOD is used for this purpose. As such, PWRGOOD has critical requirements in these areas.

9.4 System Environment and Defaults

9.4.1 DLPC4422 System Power-Up and Reset Default Conditions

Following system power-up, the DLPC4422 device performs a power-up initialization routine that defaults the device to it's normal power mode, in which ARM9-related clocks are enabled at their full rate and associated resets are released. Most other clocks default to disabled state with associated resets asserted until released by the processor. In addition, the default for system power gating enables all power. These same defaults are also applied as part of all system reset events (Watch Dog timer timeout, Lamp Strike reset, etc) that occur without removing or cycling power, with the possible exception of power for the LVDS I/O and internal DRAM. For an extended reset condition, the OEM is expected to place the ASIC in Low Power mode prior to reset, in which case the 1.8-V power for the LVDS I/O and internal DRAM will be disabled. When this reset is release, the 1.8-V power won't be enabled until the ARM9 has been initialized and is executing it's system initialization routines.

Following power-up or system reset initialization, the ARM9 boots from an external flash memory after which it enables the 1.8-V power (from the DLPA100), enables the rest of the ASIC clocks, and initializes the internal DRAM. Once system initialization is complete the Application software determines if and when to enter low power mode.

9.4.2 1.1-V System Power

The DLPC4422 device can support a low cost power delivery system with a single 1.1-V power source derived from a switching regulator. To enable this approach, appropriate filtering must be provided for the 1.1-V power pins of the PLLs.

9.4.3 1.8-V System Power

TI recommends that the DLPC4422 device power delivery system provide two independent 1.8-V power sources. One of the 1.8 V power sources should be used to supply 1.8-V power to the DLPC4422 device LVDS I/O and internal DRAM. Power for these functions should always be fed from a common source which is recommended to be linear regulator. The second 1.8-V power source should be used (along with appropriate filtering as discussed in the PCB layout guidelines for internal ASIC PLL power section of this document) to supply all of the DLPC4422 device internal PLLs. In order to keep this power as clean as possible, TI highly recommends a dedicated linear regulator for the 1.8-V power to the PLLs.

9.4.4 3.3-V System Power

The DLPC4422 device can support a low cost power delivery system with a single 3.3-V power sources derived from a switching regulator. This 3.3-V power will supply all LVTTL I/O and the Crystal Oscillator cell. 3.3-V power should remain active in all power modes for which 1.1-V core power is applied.

9.4.5 Power Good (PWRGOOD) Support

The PWRGOOD signal is defined as an early warning signal that alerts the DLPC4422 device a specified amount of time before the DC supply voltages drop below specifications. This allows the DLPC4422 device to park the DMD and to place the system into reset, ensuring the integrity of future operation. For practical reasons, TI recommends that the monitor sensing PWRGOOD be on the input side of supply regulators.

9.4.6 5V Tolerant Support

With the exception of USB_DAT, the DLPC4422 device does not support any other 5V tolerant I/O. However, note that source signals ALF_HSYNC, ALF_VSYNC & I2C typically have 5V requirements and special measures must be taken to support them. TI recommends the use of a 5V to 3.3V level shifter.

10 Layout

10.1 Layout Guidelines

TI recommends 2-ounce copper planes in the PCB design to achieve needed thermal connectivity.

10.1.1 PCB Layout Guidelines for Internal ASIC Power

TI recommends the following guidelines to achieve desired ASIC performance relative to internal PLLs:

- The DLPC4422 device contains four PLLs (PLLM1, PLLM2, PLLD & PLLS), each of which have a dedicated 1.1-V digital supply, and three (PLLM1, PLLM2 & PLLD) which have a dedicated 1.8-V analog supply. It is important to have filtering on the supply pins that covers a broad frequency range. Each 1.1-V PLL supply pin should have individual high frequency filtering in the form of a ferrite bead and a 0.1 µF ceramic capacitor. These components should be located very close to the individual PLL supply balls. The impedance of the ferrite bead should be much greater than that of the capacitor at frequencies above 10 MHz. The 1.1-V to the PLL supply pins should also have low frequency filtering in the form of an RC filter. This filter can be common to all the PLLs. The voltage drop across the resistor is limited by the 1.1-V regulator tolerance and the DLPC4422 device voltage tolerance. A resistance of 0.36 Ω and a 100 µF ceramic are recommended.
- The analog 1.8-V PLL power pins should have a similar filter topology as the 1.1 V. In addition, TI recommends that the 1.8-V be generated with a dedicated linear regulator.
- When designing the overall supply filter network, care must be taken to ensure no resonance occurs. Particular care must be taken around the 1- to 2-MHz band, as this coincides with the PLL natural loop frequency.

Layout Guidelines (continued)

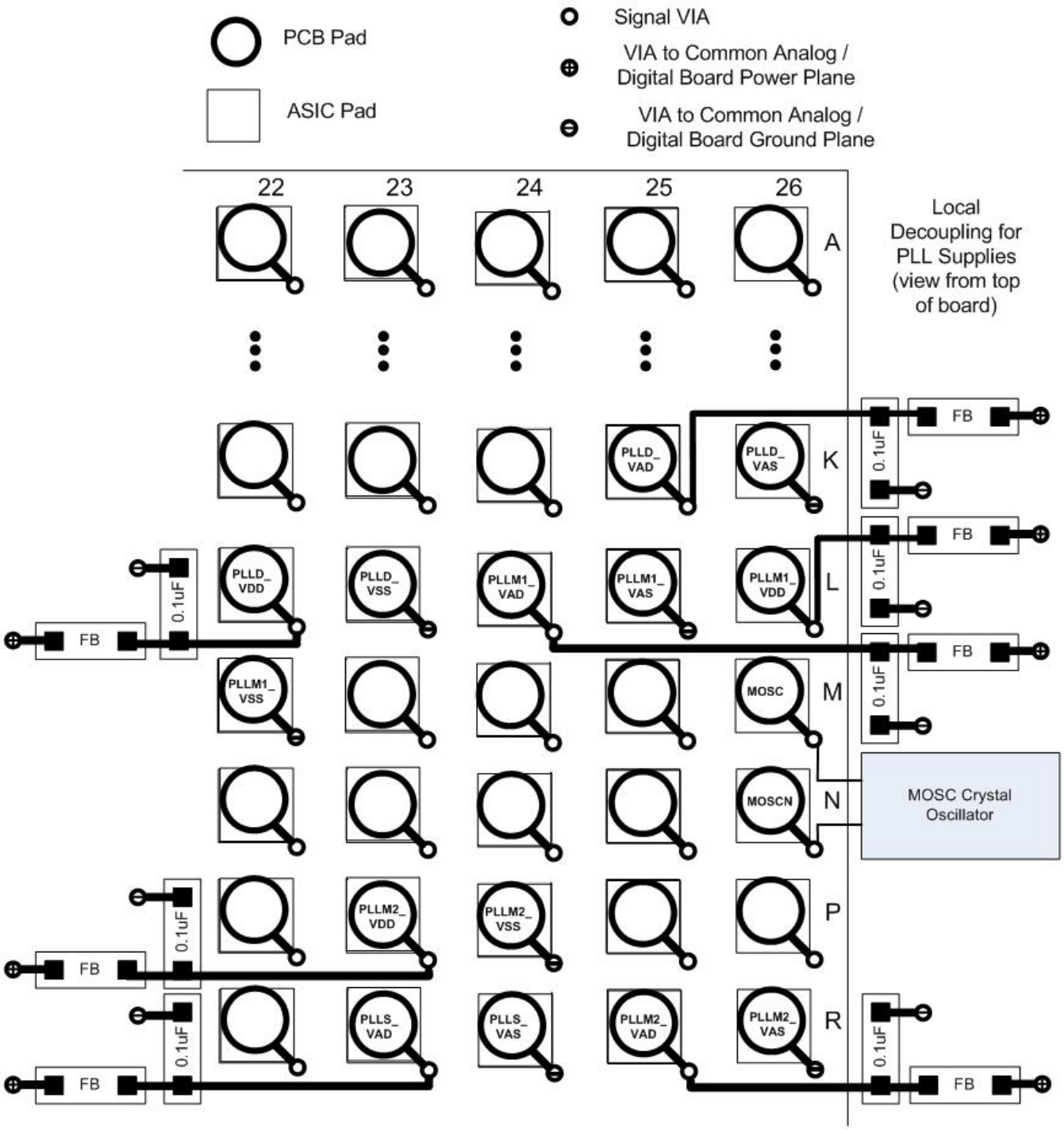


Figure 13. PLL Filter Layout

Layout Guidelines (continued)

High frequency decoupling is required for both 1.1-V and 1.8-V PLL supplies and should be provided as close as possible to each of the PLL supply package pins. TI recommends placing decoupling capacitors under the package on the opposite side of the board. Use high quality, low-ESR, monolithic, surface mount capacitors. Typically 0.1µF for each PLL supply should be sufficient. The length of a connecting trace increases the parasitic inductance of the mounting and thus, where possible, there should be no trace, allowing the via to butt up against the land itself. Additionally, the connecting trace should be made as wide as possible. Further improvement can be made by placing vias to the side of the capacitor lands or doubling the number of vias.

The location of bulk decoupling depends on the system design.

10.1.2 PCB Layout Guidelines for Auto-Lock Performance

One of the most important factors in getting good performance from Auto-Lock is to design the PCB with the highest quality signal integrity possible. TI recommends the following:

- Place the ADC chip as close to the VESA/Video connectors as possible.
- Avoid crosstalk to the analog signals by keeping them away from digital signals
- Do not place the digital ground or power planes under the analog area between the VESA connector to the ADC chip.
- Avoid crosstalk onto the RGB analog signals, by separating them from the VESA Hsync and Vsync signals.
- Analog power should not be shared with the digital power directly.
- Try to keep the trace lengths of the RGB as equal as possible.
- Use good quality (1%) termination resistors for the RGB inputs to the ADC
- If the green channel must be connected to more than the ADC green input and ADC sync-on-green input, provide a good quality high impendence buffer to avoid adding noise to the green channel.

10.1.3 DMD Interface Considerations

High speed interface waveform quality and timing on the DLPC4422 device (i.e. the LVDS DMD Interface) is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus ensuring positive timing margin requires attention to many factors.

As an example, DMD Interface system timing margin can be calculated as follows:

- Setup Margin = (DLPC4422 output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation)
- Hold-time Margin = (DLPC4422 output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

Where *PCB SI degradation* is signal integrity degradation due to PCB effects, which include simultaneously switching output (SSO) noise, cross-talk and inter-symbol interference (ISI) noise. The DLPC4422 device I/O timing parameters as well as DMD I/O timing parameters can be easily found in their corresponding datasheets. Similarly, *PCB routing mismatch* can be budgeted and met through controlled PCB routing. However, PCB SI degradation is not so straight forward.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided as a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations may also work, but should be confirmed with PCB signal integrity analysis or lab measurements

PDB Design:

● Configuration	Asymmetric Dual Stripline
● Etch Thickness	1.0 oz copper (1.2 mil)
● Flex Etch Thickness	0.5 oz copper (0.6 mil)
● Single Ended Signal Impedance	50 ohms (+/- 10%)
● Differential Signal Impedance	100 ohms differential (+/- 10%)

Layout Guidelines (continued)

PCB Stackup:

- Reference plane 1 is assumed to be a ground plane for proper return path
- Reference plane 2 is assumed to be the I/O power plane or ground
- Dielectric FR4, (Er): 4.2 (nominal)
- Signal trace distance to reference plane 1 (H1) 5.0 mil (nominal)
- Signal trace distance to reference plane 2 (H2) 34.2 mil (nominal)

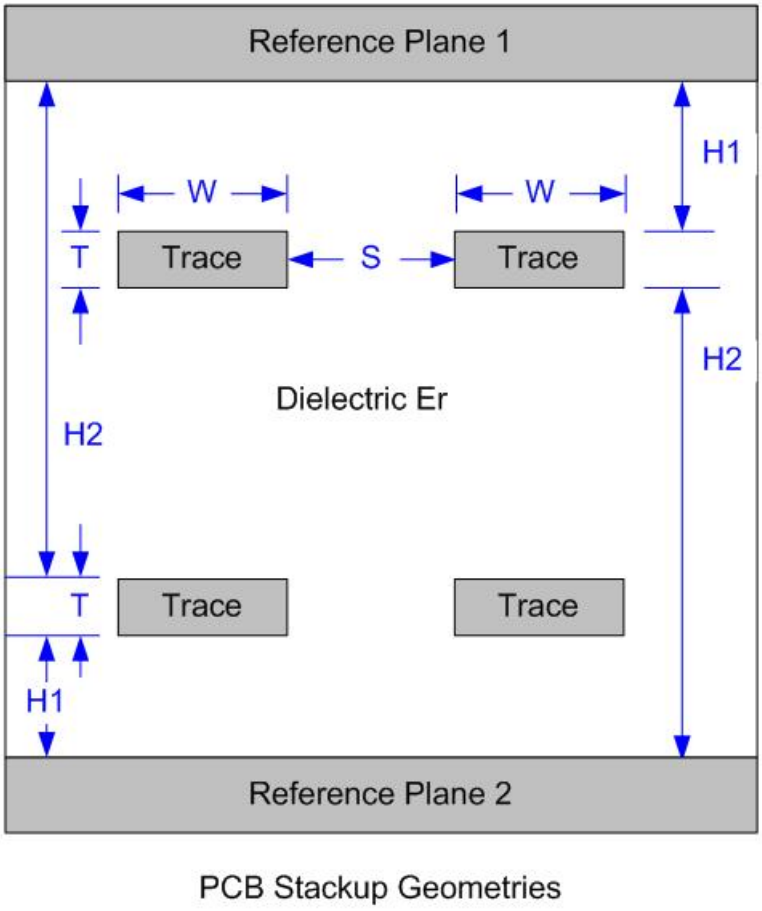


Figure 14. PCB Stackup Geometries

Layout Guidelines (continued)

Table 10. General PCB Routing (Applies to All Corresponding PCB Signals)

PARAMETER	APPLICATION	SINGLE-ENDED SIGNAL	DIFFERENTIAL PAIRS	UNIT
Line width (W)(1)	Escape Routing in Ball Field	4 (0.1)	4 (0.1)	mil (mm)
	PCB Etch Data or Control	7 (0.18)	4.25 (0.11)	mil (mm)
	PCB Etch Clocks	7 (0.18)	4.25 (0.11)	mil (mm)
Minimum Line spacing to other signals (S)	Escape Routing in Ball Field	4 (0.1)	4 (0.1)	mil (mm)
	PCB Etch Data or Control	10 (0.25)	20 (0.51)	mil (mm)
	PCB Etch Clocks	20 (0.51)	20 (0.51)	mil (mm)

(1) Line width is expected to be adjusted to achieve impedance requirements

Table 11. DMD I/F, PCB Interconnect Length Matching Requirements(1)(2)

SIGNAL GROUP LENGTH MATCHING				
I/F	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD (LVDS)	SCA_P,SCA_N, DDA_P(15:0), DDA_N(15:0)	DCKA_P, DCKA_N	+/-150 (+/-3.81)	mil (mm)
DMD (LVDS)	SCB_P,SCB_N, DDB_P(15:0), DDB_N(15:0)	DCKB_P, DCKB_N	+/-150 (+/-3.81)	mil (mm)

(1) These values apply to the PCB routing only. They do not include any internal package routing mismatch associated with the DLPC4422 controller or the DMD. Additional margin can be attained if internal DLPC4422 package skew is taken into account.
(2) To minimize EMI radiation, serpentine routes added to facilitate matching should be implemented on signal layers only, and between reference planes.

Number of layer changes:

- Single ended signals: Minimize
- Differential signals: Individual differential pairs can be routed on different layers but the signals of a given pair should not change layers.

Termination requirements:

- DMD Interface - None, the DMD receiver is differentially terminated to 100 ohm internally

  Connector (DMD-LVDS I/F bus only) - High Speed Connectors that meet the following requirements should be used:

  - Differential Crosstalk <5 %
  - Differential Impedance 75-125 ohms

Routing requirements for right angle connectors:

When using right angle connectors, P-N pairs should be routed in same row to minimize delay mismatch. When using right angle connectors, propagation delay difference for each row should be accounted for on associated PCB etch lengths.

10.1.4 Layout Example

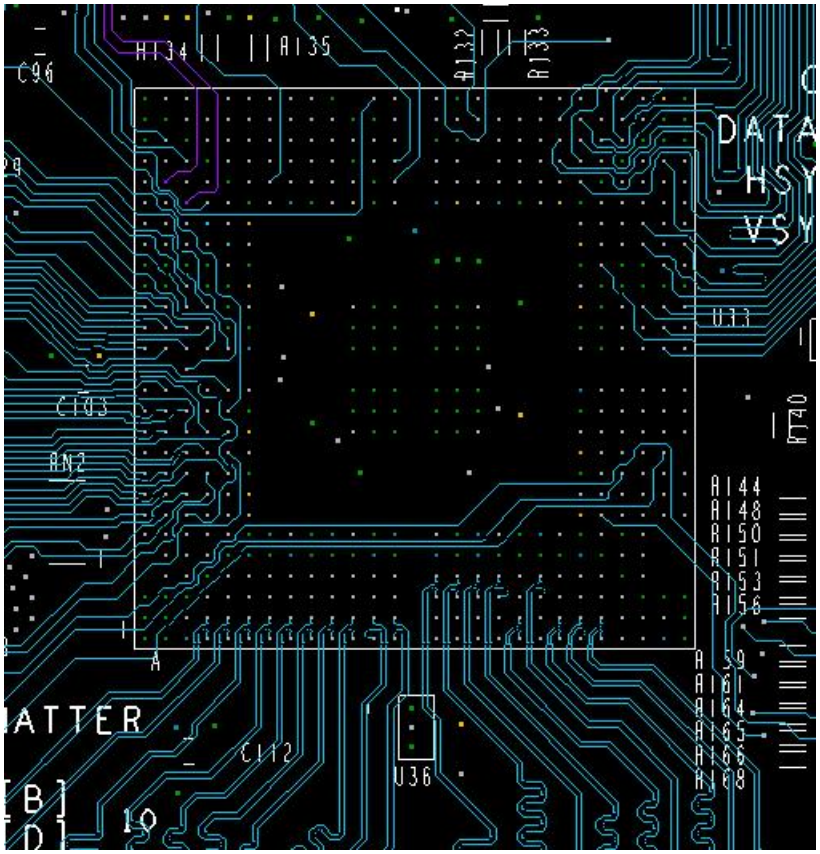


Figure 15. Layer 3

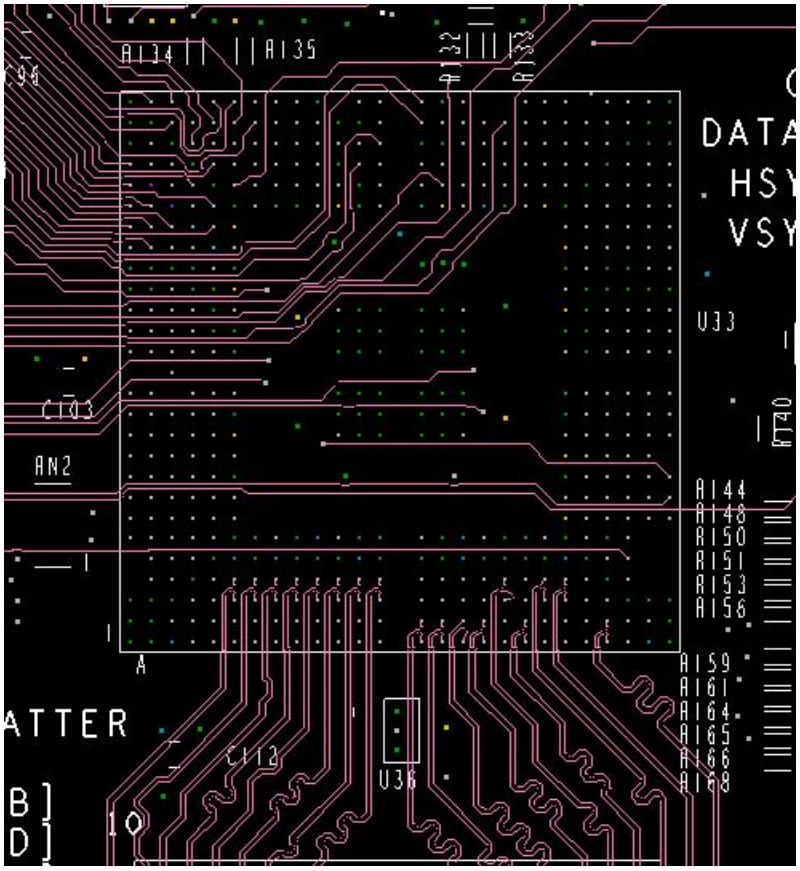


Figure 16. Layer 4

10.1.5 Thermal Considerations

The underlying thermal limitation for the DLPC4422 device is that the maximum operating junction temperature (T_J) not be exceeded (this is defined *Recommended Operating Conditions*). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC4422 device and power dissipation of surrounding components. The DLPC4422 package is designed primarily to extract heat through the power and ground planes of the PCB, thus copper content and airflow over the PCB are important factors.

The recommended maximum operating ambient temperature (T_A) is provided primarily as a design target and is based on maximum DLPC4422 power dissipation and $R_{\theta JA}$ at 1 m/s of forced airflow, where $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC4422 PCB, and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance. However, after the PCB is designed and the product is built, TI highly recommends that thermal performance be measured and validated.

To do this, the top center case temperature should be measured under the worse case product scenario (max power dissipation, max voltage, max ambient temp) and validated not to exceed the maximum recommended case temperature (T_C). This specification is based on the measured φ_{JT} for the DLPC4422 package and provides a relatively accurate correlation to junction temperature. Note that care must be taken when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approx 40 gauge) thermocouple. The bead and the thermocouple wire should contact the top of the package and be covered with a minimal amount of thermally conductive epoxy. The wires should be routed closely along the package and the board surface to avoid cooling the bead through the wires.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Video Timing Parameter Definitions

- **Active Lines Per Frame (ALPF)** - Defines the number of lines in a Frame containing displayable data: ALPF is a subset of the TLPF.
- **Active Pixels Per Line (APPL)** - Defines the number of pixel clocks in a line containing displayable data: APPL is a subset of the TPPL
- **Horizontal Back Porch Blanking (HBP)** - Number of blank pixel clocks after Horizontal Sync but before the first active pixel. Note: HBP times are reference to the leading (active) edge of the respective sync signal
- **Horizontal Front Porch Blanking (HFP)** – Number of blank pixel clocks after the last active pixel but before Horizontal Sync.
- Horizontal Sync (HS) – Timing reference point that defines the start of each horizontal interval (line). The absolute reference point is defined by the “active” edge of the HS signal. The “active” edge (either rising or falling edge as defined by the source) is the reference from which all Horizontal Blanking parameters are measured.
- **Total Lines Per Frame (TLPF)** - Defines the Vertical Period (or Frame Time) in lines: TLPF = Total number of lines per frame (active and inactive).
- **Total Pixel Per Line (TPPL)** - Defines the Horizontal Line Period in pixel clocks: TPPL = Total number of pixel clocks per line (active and inactive).
- **Vertical Back Porch Blanking (VBP)** - Number of blank lines after Vertical Sync but before the first active line.
- **Vertical Front Porch Blanking (VFP)** - Number of blank lines after the last active line but before Vertical Sync.
- **Vertical Sync (VS)** – Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the “active” edge of the VS signal. The “active” edge (either rising or falling edge as defined by the source) is the reference from which all Vertical Blanking parameters are measured.

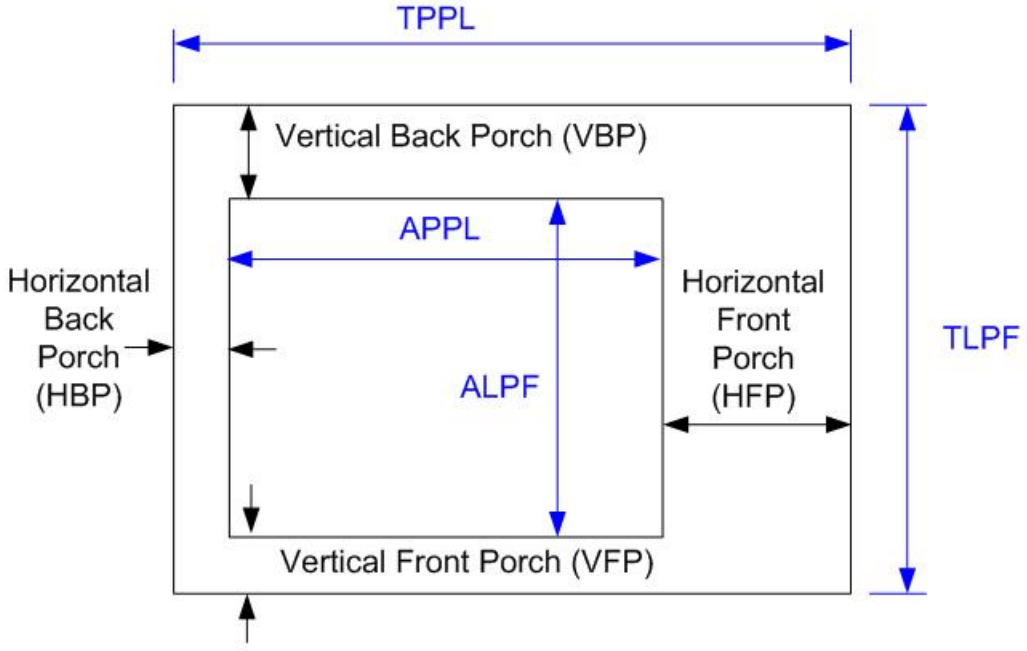


Figure 17. Timing Parameter Diagram

11.1.2 Device Nomenclature

Table 12. Part Number Description

TI PART NUMBER	DESCRIPTION
DLPC4422	DLPC4422 Digital Controller

11.1.3 Device Markings

11.1.3.1 Device Marking

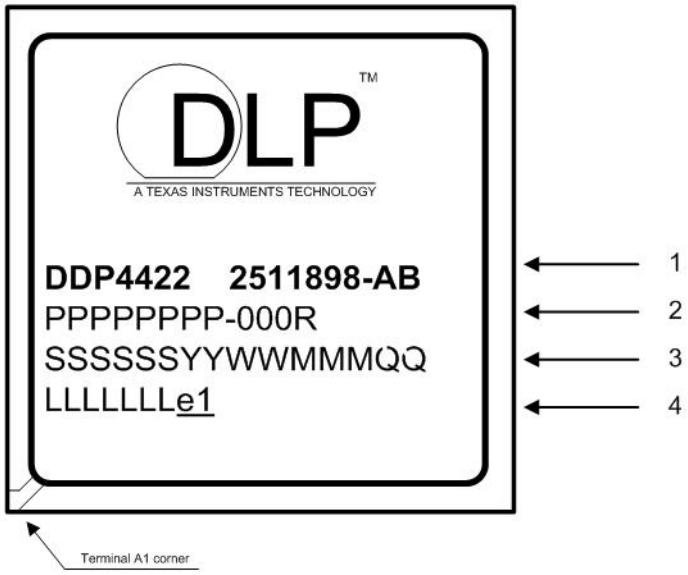


Figure 18. DLPC4422 Device Markings

Marking Definitions:

Line1: DLP Device Name followed by TI Part Number

Line2: Foundry part number

Line3:

- SSSSSSYYWWMMM-QQ Package Assembly information
- SSSSSS: Manufacturing Country
- YYWW: Date Code (YY =Year :: WW = Week)
- MMM: Manufacturing Site (HAL = Taiwan, HBL = Japan)
- QQ: Qualification level

Line4:

- LLLLLLL: Manufacturing Lot code
- e1: lead-free solder balls consisting of SnAgCu

11.2 Documentation Support

11.2.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLPC4422:

- DLP660TE DMD Data Sheet
- DLPA100 Power Management and Motor Driver Data Sheet

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
DLP is a registered trademark of Texas Instruments.
ARM946 is a trademark of ARM.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC4422AZPC	PREVIEW	BGA	ZPC	516	1	TBD	Call TI	Call TI	0 to 55		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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