Application Report
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AN-1729 DP83640 IEEE 1588 PTP Synchronized Clock Output

ABSTRACT

The DP83640 provides a highly precise, low-jitter clock output that is frequency-aligned to the master IEEE 1588 clock and can be phase-aligned as well. Empirical testing shows very low jitter (less than 1 ns peak-to-peak and standard deviation when using the FCO source) and precise phase alignment. While test results show that the FCO has superior long term jitter performance, using the PGM as a clock source has the advantage of allowing multimode (10 MB or 100 MB) linked operation.

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1 Introduction

Many industrial, test and measurement, and telecommunications applications require highly accurate and precise clock signals in order to synchronize control signals, capture data, and so forth. The IEEE 1588 Precision Time Protocol (PTP) used in standard Ethernet provides a method for propagating a master clock time to many nodes in a system. Current implementations rely purely on software or on a mix of software and FPGA or ASIC hardware. While nodes based on these implementations may be able to generate a clock output signal based on the master clock time, the precision of such a signal may not be sufficient for systems requiring extremely low clock jitter. In addition, there may be stringent requirements for clock phase alignment across the system. The DP83640 precision PHYTER™ provides solutions to both of these issues.

This document is applicable to the following product: DP83640.

2 Background

The DP83640 includes a highly configurable clock output signal that is syntonized to its internal IEEE 1588 clock. Note that syntonization implies equal frequency but not necessarily equal phase. The nominal frequency of this clock is an integer division of 250 MHz, (250 MHz/N, where N is an integer from 2 to 255). Therefore, the possible nominal frequencies are discrete values between 980.4 kHz and 125 MHz.

The DP83640 uses software assisted rate correction to eliminate the frequency offset between the local and master reference clocks. The final output frequency incorporates the same rate correction parameter (ppm offset) as the internal IEEE 1588 clock time. Since the rate correction is in units of subnanoseconds (one subnanosecond = 2^{-32} nanoseconds), the clock output frequency can be finely tuned (to the order of 1 part per billion).

In addition to fixed values, the rate correction can be programmed to operate at one value for a short time duration of up to 1/2 second (a “temporary rate”). After the temporary rate duration expires, the rate correction returns to the fixed rate correction value. By correcting additional frequency offset over a short time interval, the clock output signal will not exhibit discrete jumps in frequency or phase.

The DP83640 also offers a method for aligning the phase of the clock output signal with that of the master clock. Unlike the trigger outputs of the device, which are generated with a discrete resolution of 8 ns, the clock output is generated from a highly tunable analog source, either a frequency-controlled oscillator (FCO) or phase generation module (PGM). The clock output is enabled at power-up by default, running at 25 MHz; however, the 1588 logic, including the 1588 clock, must be initialized prior to operation. Therefore, the initial phase relationship between the clock output and the 1588 master clock is not known. However, clever use of the DP83640 features allows alignment of the clock output phase to the phase of the 1588 clock.

There are advantages to both sources of the 1588 clock output. The FCO offers better jitter performance but has a smaller correction range and some usage restrictions in order to preserve the clock phase on a link loss event. The PGM does not have these restrictions and has a larger correction range, but its long term jitter performance is not as good as that of the FCO.

3 Theory

3.1 Rate Correction

The IEEE 1588 clock output rate correction function utilizes the same logic as that of the internal 1588 clock. The DP83640 includes a 26-bit rate correction parameter in units of subnanoseconds per reference clock cycle. Under software control, the rate correction is positive when the local reference clock runs more slowly than the master clock and negative when the local reference clock runs faster than the master clock. With a rate correction granularity of one subnanosecond per 8 nanosecond clock cycle, the clock output is tunable with an increment of 2^{-32} subnanoseconds/8 nanoseconds = 0.029 parts per billion (ppb).

The PTP rate is controlled using the PTP Rate Control Registers (PTP_RATEH and PTP_RATEL) and PTP Temporary Rate Duration Control Registers (PTP_TRDH and PTP_TRDL).

A fixed rate correction may be programmed as follows:

1. Write the rate direction (0x8000 for higher, 0x0000 for lower) and the upper 10 bits of the value to the PTP_RATEH register.

2. Write the lower 16 bits of the value to the PTP_RATEL register. The rate takes effect upon writing PTP_RATEL.

Example: Set fixed rate correction to -100 ppm relative to the master.

1. Since the nominal reference clock period is 8 ns, 100 ppm is 0.0008 ns. This is 0.0008 * 2^{32} subnanoseconds, which equals approximately 3435974 subnanoseconds (0x346DC6).
2. Write 0x8034 to PTP_RATEH.
3. Write 0x6DC6 to PTP_RATEL.

A temporary rate correction is programmed in a manner similar to that of the fixed rate correction, except that bit 14 (0x4000) of PTP_RATEH must also be set. Since the temporary rate takes effect upon writing the PTP_RATEL register, the PTP temporary rate Duration registers must be programmed before setting the temporary rate. The rate correction value switches back to the fixed rate value after the temporary rate duration expires. The temporary rate duration is configured as follows:

1. The temporary rate duration is a 26-bit number in units of clock cycles. At the default 8 ns reference clock period, the maximum duration is about 537 ms.
2. Write the upper 10 bits of the temporary rate duration to PTP_TRDH.
3. Write the lower 16 bits of the temporary rate duration to PTP_TRDL. The temporary rate duration setting takes effect upon writing this register, and remains constant until modified via register write. Often there will not be a need to change the temporary rate duration.

Example: Set a temporary rate correction of +3 ns over 10 ms:

1. For a temporary rate duration of 1 ms at the default reference clock period, you need 10 ms / 8 ns = 1250000 clock cycles (0x1312D0). For +3 ns of correction over 1250000 clock cycles, you need 3 ns / 1250000 = 0.0000024 ns = 10308 subnanoseconds/clock cycle (0x2844).
2. Write 0x0013 to PTP_TRDH
3. Write 0x12D0 to PTP_TRDL
4. Write 0xC000 to PTP_RATEH
5. Write 0x2844 to PTP_RATEL

3.1.1 Maximum Rate Correction

While large rate corrections (greater than 100 ppm) are typically not required, the choice of the source for the 1588 clock output determines the maximum available rate correction. The maximum effective rate correction when using the FCO is 0x1555555, which translates to ± 651 ppm. The maximum effective rate correction when using the PGM is 0x3FFFFFF, which translates to ± 1953 ppm.

3.2 Phase Alignment

Aligning the phase of the clock output requires the following steps:

1. Ensure the clock output pin is enabled.
2. Prior to enabling the PTP synchronization protocol, enable the clock output and the PTP clock.
3. Enable an event monitor for a single event to catch the rising edge of the clock output pin.
4. Determine clock output offset from aligned expected time: clock output period – (event timestamp mod clock output period).
5. Do a step adjustment to align the clock output.
6. During synchronization, all step adjustments should be in units of the clock output period.

Example: Phase alignment of a 10 MHz clock output:

1. Ensure the clock output pin is enabled. This can be done by strapping the GPIO1 pin high prior to power-up, or by clearing the CLK_OUT_DISABLE bit (bit 2) in the PHYCR2 register (register 0x1C).
2. Enable the clock output at 10 MHz: write 0x8019 to the PTP_COC register. Note that 0x19 is 25 decimal, to divide the 250 MHz clock by 25. Enable the PTP clock: write 0x0004 to the PTP_CTL register.
3. Take 100 samples of the CLK_OUT phase error.

- Enable the Event monitor and get the event timestamp:
  - Write 0x1C0F to the PTP_EVNT register.
  - Write 0x5C0F to the PTP_EVNT register. The first write sets up a single event capture for CLK_OUT/GPIO12 with Event 7 (though any event may be used). The second write does the same plus it enables the capture.
  - Read the PTP_ESTS register for bit 0 set. If not, wait and repeat this step.
  - Once bit 0 of PTP_ESTS has been set, determine the event timestamp length (1-4 16-bit words) by adding 1 to bits 7:6 of the PTP_ESTS value.
  - Ensure the Event number is 7, (the PTP_ESTS value bits 4:2 equal 7).
  - Ensure the event was a rising edge. This is indicated by the value of PTP_ESTS bit 5 equaling 1.
  - Read the PTP_EDATA register. The event timestamp is returned as follows:
    - Event nanoseconds bits 15:0
    - Event nanoseconds bits 29:16
    - Event seconds bits 15:0
    - Event seconds bits 31:16
  - Subtract (3 times the reference clock period + 11) from the timestamp; with the typical 8 ns reference clock period, this value is 35 ns. This corrects for the pin input delay and edge detection.
- Calculate the phase error as (100 – (event timestamp mod 100)). If the result is equal to the clock period (100 ns in this case), the phase error is 0. If the phase error is within 10 ns of the clock period (91 – 99 ns in this case), set a flag “HighValue”. This is equivalent to a negative phase error of between -9 and -1 ns.

4. Average the phase error. If there are small positive and negative phase error samples, HighValue is set and a phase error sample is less than 10 ns, the clock period must be added to the sample in order for it to be averaged correctly:
   - If (HighValue & error[sample]<10) error[sample] += clkout_period
5. If the average phase error is greater than the clock period, subtract the clock period to get the final average phase error.
6. Calculate the correction value, which is the average phase error plus twice the reference clock period:
   - Correction = 2 * ref_period + avg_phase_error
7. Do a step adjustment to the 1588 clock time:
   - Write the correction value to PTP_TDR.
   - Write PTP_STEP_CLK (0x8) to PTP_CTL.

3.2.1 Maintaining Phase Alignment Through Loss of Link

When using the FCO for generating the CLK_OUT signal, a loss of link may cause the CLK_OUT signal to stop for a short period of time, resulting in a loss of phase alignment. The DP83640 offers three options for retaining the alignment of CLK_OUT with the 1588 clock time and triggers upon loss of link.

- Link is established using autonegotiation on a network known to be 100Mb/s. In this case, write 0x803F twice to register 0x1E. This allows the CLK_OUT phase alignment to be preserved following a loss of link. In addition, the DP83640 can be strapped to advertise 100Mb/s only by either pulling the LED_SPEED pin low with a 2.2kOhm resistor, or by writing 0x0181 to the Auto-Negotiation Advertisement Register (ANAR) - register 0x04. Do not advertise 100Mb/s only if the link speed may need to be 10Mb/s.
- The network speed is 10Mb/s or cannot be guaranteed to be 100Mb/s, and the application can tolerate the somewhat higher jitter from the PGM source to CLK_OUT. Set bit 14 (PTP_CLKOUT_SEL) in the PTP Clock Output Control Register (PTP_COC), register 0x14.

- Low jitter on CLK_OUT is a requirement and option 1 cannot be used. Force the PHY into a known 100Mb/s or 10Mb/s mode if the network configuration will tolerate it. In the BMCR register (register 0x00), clear bit 12 to disable autonegotiation. Set bit 13 for 100Mb/s and set bit 8 for full duplex.

4 Jitter Test Results

4.1 Test Setup

A series of tests were performed to measure the jitter on the clock output with the devices synchronized to a master using version 1 of the IEEE 1588 PTP, with a synchronization interval of one second and temporary rate duration of 10 milliseconds.

A Tektronix TDS784C oscilloscope was used to measure the histogram of the jitter on the signal (10 MHz) at a single cycle (100 ns) and at a 10 µs delay.

With the probe connected to the clock output signal of the device, the internal histogram function of the Tektronix TDS784C was used to capture the rising edge of the clock signal at the specified delay time. For each test condition, approximately 1000 data points were captured, and the peak-to-peak and standard deviation of the histogram were recorded.

4.2 Test Conditions

Table 1 summarizes the conditions for the jitter test setup.

Table 1. Test Conditions for Jitter Test

Operating Voltage	3.3 V
Temperature	25 °C
Reference Frequency Source	On-board 25 MHz crystal
Clock Output Frequency	10 MHz
IEEE 1588 PTP Synchronization Interval	1 s
Temporary Rate Duration	10 ms

4.3 Test Results

Table 2 shows the jitter measurements for the FCO and PGM sources.

Table 2. Jitter Results

Source	Cycle-to-Cycle		10 µs Delay	
	Peak to Peak (ps)	Standard Deviation (ps)	Peak to Peak (ps)	Standard Deviation (ps)
FCO	320	53.1	340	58.5
PGM	340	53.2	1160	267.5

From this data, it is evident that while short-term (cycle-to-cycle) jitter is comparable between the FCO and PGM sources, the long-term jitter is worse when using the PGM.

Figure 1, Figure 2, Figure 3, and Figure 4, represent typical histogram plots of the clock output signal when the DP83640 is synchronized to the Master.

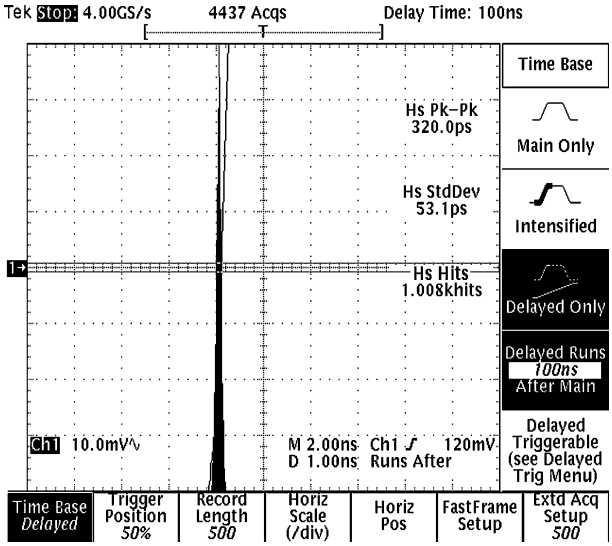

Figure 1. Cycle-to-Cycle Jitter Histogram With FCO Source

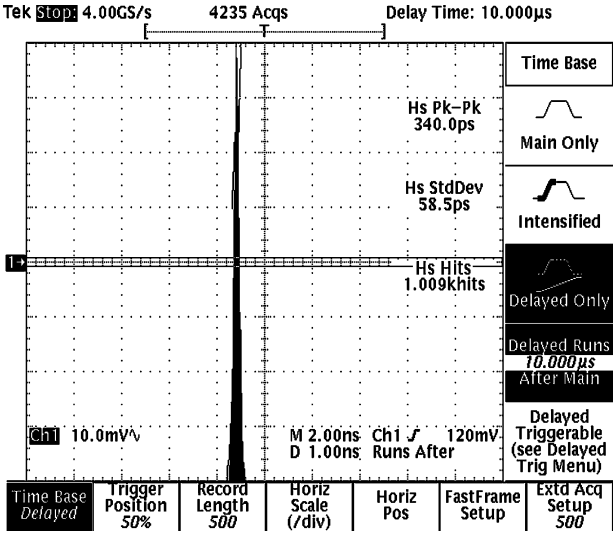

Figure 2. 10 µs Delay Jitter Histogram With FCO Source

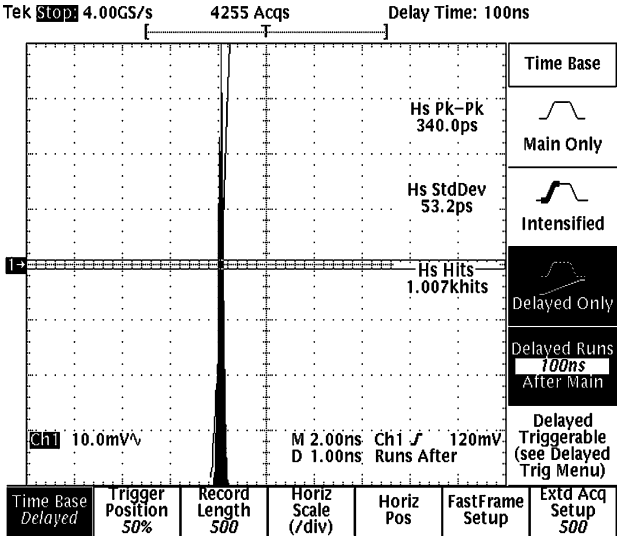

Figure 3. Cycle-to-Cycle Jitter Histogram With PGM Source

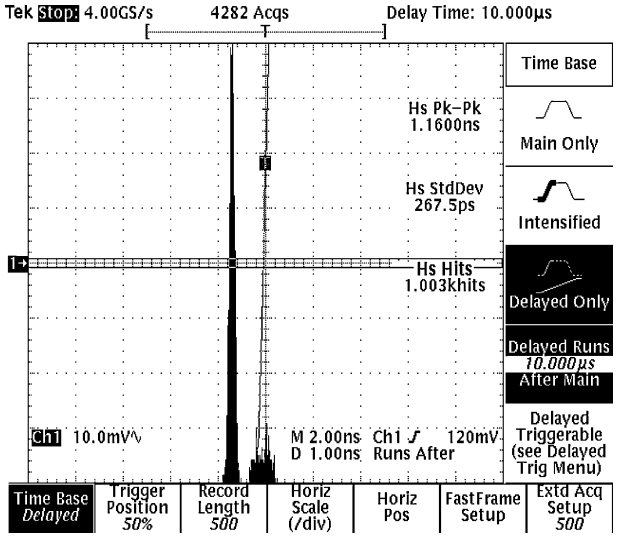

Figure 4. 10 µs Delay Jitter Histogram With PGM Source

5 Clock Phase Error Test Results

5.1 Test Setup

The synchronization error to the master is measured by determining the delay from the master clock output pin to the slave clock output pin. The devices were connected directly using a 1 m CAT5 cable. IEEE 1588 v1 was used with a 1 second sync period, 100 ms temporary rate duration, timestamp insertion enabled, and one-step operation enabled.

5.2 Test Conditions

Table 3 summarizes the conditions for the clock phase error test setup.

Table 3. Test Conditions For Phase Error Test

Operating Voltage	3.3 V
Temperature	25 °C
Reference Frequency Source	On-board 25 MHz crystal
Clock Output Frequency	10 MHz
IEEE 1588 PTP Synchronization Interval	1 s
Temporary Rate Duration	100 ms

5.3 OSCILLOSCOPE SETUP

The configuration of the Tektronix TDS784C oscilloscope is given in Table 4.

Table 4. Oscilloscope Setup For Phase Error Test

Horizontal Scale	25 ns/div
Vertical Scale (CH1)	1 V/div
Vertical Scale (CH2)	500 mV/div
Trigger Level	1.58 V
Trigger Mode	Rising Edge
Sweep	Main

5.4 TEST RESULTS

Table 5 shows the resulting mean and standard deviation for the clock phase error test using each of the clock sources.

Table 5. Clock Phase Error

Source	Cycle-to-Cycle	
	Mean (ns)	Standard Deviation (ns)
FCO	4.647	5.905
PGM	5.134	6.381

The results indicate that the clock phase error does not depend on the selection of the FCO versus the PGM.

Figure 5 and Figure 6 represent typical histogram plots of the clock output phase error when the DP83640 is synchronized to the Master.

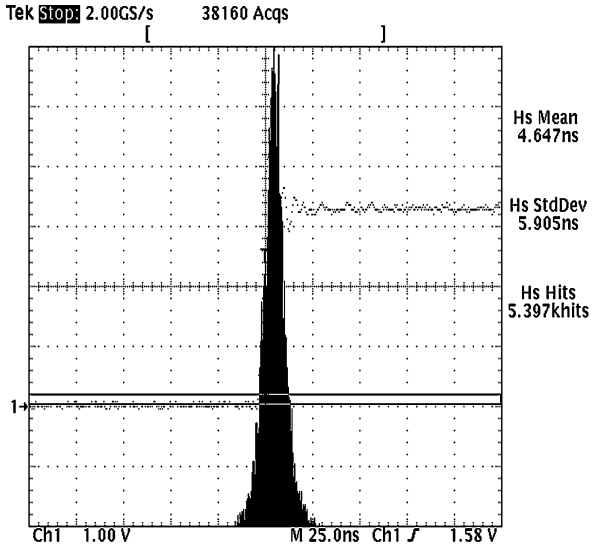

Figure 5. Clock Output Phase Error With FCO Source

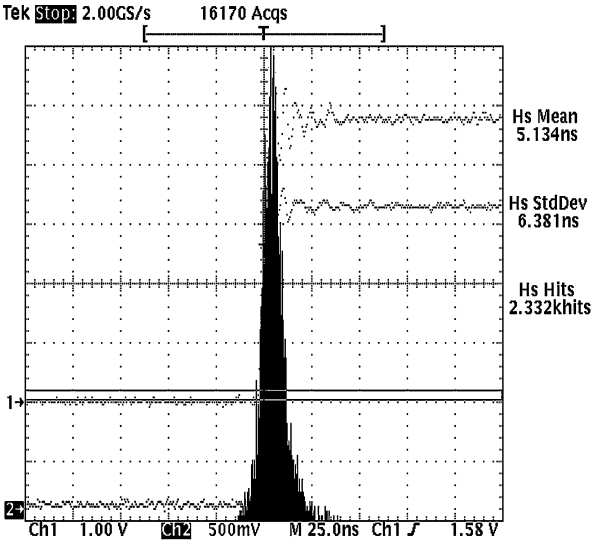

Figure 6. Clock Output Phase Error With PGM Source

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