Application Report
SNLA266–January 2016

DP83822 IEEE 802.3u Compliance and Debug

Yue Cai, Ross Pimentel

ABSTRACT

The DP83822 was designed to meet the needs of rugged and high performance applications while still maintaining strict adherence to the IEEE 802.3u standard. This application note will discuss how to configure the DP83822 for various Ethernet compliance tests, identify common system level mistakes and present solutions to those mistakes to ensure compliance.

Contents

List of Figures

List of Tables

1 Introduction

The DP83822 10/100 Mbps Industrial Ethernet PHY is IEEE 802.3u compliant to:

- 100BASE-TX
- 100BASE-FX
- 10BASE-Te

This application note will only discuss 100BASE-TX and 10BASE-Te compliance. For additional support, visit our Texas Instruments E2E Community at www.e2e.ti.com.

Table 1. Terminology

ACRONYM	DEFINITION
DUT	Device Under Test
LP	Link Partner
PHY	Physical Layer Transceiver
SMI	Serial Management Interface
IPG	Inter-Packet Gap
FLP	Fast Link Pulse
NLP	Normal Link Pulse
TX	Transmit – Digital Pins
RX	Receive – Digital Pins
TD	Transmit – Analog Pins
RD	Receive – Analog Pins
AVD	Analog Supply
CT	Magnetic Center Tap
VDDIO	Digital Supply
BIST	Built-In Self-Test
TPM	Twisted Pair Model
AOI	Active Output Interface
AFE	Analog Front-End

2 Standards and System Requirements

2.1 Standards

The following standards serve as references for the tests described in this document.

- IEEE802.3-2005 Sub Clause 14.3.1
- IEEE802.3-2005 Sub Clause 25.4
- ANSI X3.263-1995

2.2 Test Equipment Suppliers

The following test equipment suppliers are known to offer IEEE 802.3 compliance test equipment.

- Tektronix
- Spirent
- Agilent (Keysight)

2.3 Test Equipment Requirements

For this application note, the following hardware and software was used.

- Oscilloscope and Physical Layer Compliance Software (Tektronix TDSET3)
- Differential Probe
- Ethernet Compliance Test Fixture
- TI USB-2-MDIO tool With PC (Not Required For All Tests)
- MSP430 LaunchPad MSP-EXP430F5529LP
- USB Cable
- DC Power Supply

3 Ethernet Physical Layer Compliance Testing

3.1 Standard Test Setup and Procedures

For Ethernet physical layer compliance testing, the PHY is managed through SMI to enable various test modes. Test results are determined and recorded by the oscilloscope's Ethernet compliance software (for example, Tektronix's TDSET3).

Variation between Ethernet physical layer compliance tests is primarily the test mode of the PHY (configured by setting the internal PHY registers via SMI) and the connection on the test fixture.

1. Connect 5-V DC supply to the EVM through the micro-USB connector. For other power supply options, see the *DP83822 EVM User's Guide* (SNLU179).
2. Connect the EVM to the test fixture according to setup outlined in the test fixture/software manual (see Figure 1). Identify if a link partner and/or packet generator is needed for the test, and connect accordingly.
3. Set the thermal stream or oven to desired temperature (if applicable).
4. Configure the PHY's registers for the specific test. The SMI can be managed using TI's USB-2-MDIO tool through a MSP430 Launchpad (see Appendix D). Register configurations are outlined in Appendix A. All test mode configuration scripts can be copied and used directly with the USB-2-MDIO tool.
5. Start and configure the oscilloscope's Ethernet testing software (see software user's manual).
6. Run the test and store the results (using the Ethernet compliance testing software).
7. Determine if the test has passed or failed according to IEEE standards.
8. Change test parameters or test channel and repeat.

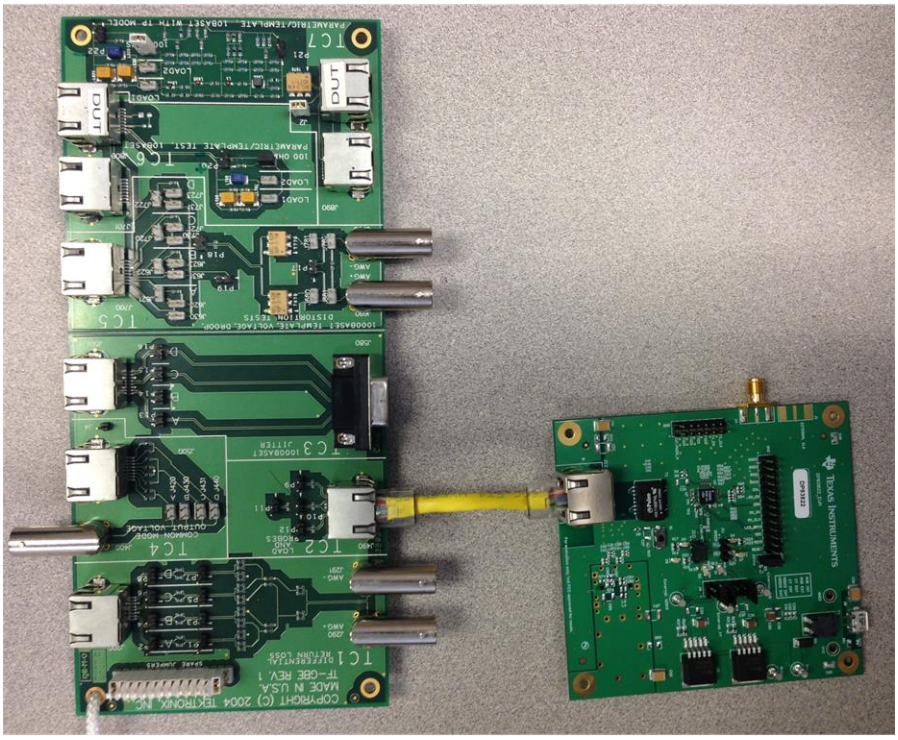

Figure 1. DP83822 EVM Connected to a Testing Fixture

3.2 10BASE-Te Compliance Testing

Refer to Appendix A for 10BASE-Te test mode scripts. Sample test waveforms are included in Appendix C.

3.2.1 Link Pulse

Purpose: To ensure that the link pulse waveform is within the specified bounds.

Pass Condition: The link pulse must fit into the IEEE-defined template.

Specific Test Setup: Verify the test fixture connections. Set registers according to 10BASE-Te Link Pulse in Appendix A.

3.2.2 TP_IDL

Purpose: To ensure that the transmitter functions properly after transitioning to an idle state.

Pass Condition: The transmitter TP_IDL pulse must fit within the template for Load 1, 2, and 3 with and without the TPM.

Specific Test Setup: Verify the test fixture connections. Configure the PHY to be in analog loopback mode by setting registers according to 10BASE-Te Standard in Appendix A.

3.2.3 MAU, Internal

Purpose: To ensure that the transmitter output equalization is within the specified bounds.

Pass Condition: The transmitter waveform should fit within the IEEE-defined template for all data sequences when terminated with a 100-Ω resistor.

Specific Test Setup: Verify the test fixture. Configure the PHY to be in analog loopback mode by setting registers according to 10BASE-Te Standard in Appendix A.

3.2.4 Jitter With TPM

Purpose: Purpose: To ensure that the jitter is within the specified bounds.

Pass Condition: The transmitter output jitter should be less than ±5.5 ns.

Note: Failure with TPM does not necessarily mean noncompliance.

Specific Test Setup: Verify the test fixture connections. Configure the PHY to be in analog loopback mode by setting registers according to 10BASE-Te Standard in Appendix A.

3.2.5 Jitter Without TPM

Purpose: To ensure that the jitter is within the specified bounds.

Pass Condition: The transmitter output jitter should be less than ±8.0 ns.

Specific Test Setup: Verify the test fixture. Configure the PHY to be in analog loopback mode by setting registers according to 10BASE-Te Standard in Appendix A.

3.2.6 Differential Voltage

Purpose: To ensure that the differential voltage is within the specified bounds.

Pass Condition: The peak differential voltage should be between 1.54-V and 1.96-V when terminated with 100-Ω resistor.

Specific Test Setup: Verify the test fixture. Configure the PHY to be in analog loopback mode by setting registers according to 10BASE-Te Standard in Appendix A.

3.2.7 Harmonic Content

Purpose: To ensure the harmonic content of the PHY is within the specified bounds.

Pass Condition: The Data Out circuit must drive all ones. All subsequent harmonics must be 27-dB below the fundamental.

Specific Test Setup: Verify the test fixture. Configure the PHY to be in analog loopback mode by setting registers according to 10BASE-Te Standard in Appendix A.

3.2.8 Common-Mode Voltage

Purpose: To ensure the common-mode voltage is within the specified bounds.

Pass Condition: The magnitude of the common-mode voltage should be less than 50-mV peak.

Specific Test Setup: Verify the test fixture connections. Configure the PHY to be in analog loopback mode by setting registers according to 10BASE-Te Standard in Appendix A.

3.2.9 Return Loss

Purpose: To ensure that the return loss is above the specified attenuation.

Pass Condition: The reflection of any incident signal to the PHY must be attenuated: ≥ 15 dB over the frequency range of 5 MHz to 10 MHz

Specific Test Setup: Two waveform inputs may be necessary depending on testing setup. Verify the test fixture connections. Configure the PHY to be in analog loopback mode by setting registers according to 10BASE-Te Standard in Appendix A.

3.2.10 Common-Mode Rejection

Purpose: Verify that the PHY's common-mode rejection ratio is within the specified bounds.

Pass Condition: See IEEE 802.3 14.3.1.2.6

Specific Test Setup: Refer to the high voltage injection testing procedures (not included in this app note). Set registers according to 10BASE-Te Standard in Appendix A.

3.3 100BASE-TX Compliance Testing

Refer to Appendix A for 100BASE-TX register writes. The following tests are done with forced MDI using the PHY Control Register (PHYCR, address 0x0019). For MDIX operation set bits [15:14] = 0b01. Sample test waveforms are included in Appendix C.

3.3.1 Template (Active Output Interface)

Purpose: To ensure that the output fits the transmit template.

Pass Condition: MLT-3 eye fits into the specified ANSI AOI template.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to 100BASE-TX Standard in Appendix A.

3.3.2 Differential Output Voltage

Purpose: To ensure the differential output voltage is within the specified bounds.

Pass Condition: The differential output voltage should be within a positive +950-mV to +1050-mV and negative –950-mV to –1050-mV.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to 100BASE-TX Standard in Appendix A.

3.3.3 Signal Amplitude Symmetry

Purpose: To ensure the Signal Amplitude Symmetry is within the specified bounds.

Pass Condition: The ratio of the positive peak to negative peak amplitudes should be within 2% or $0.98 \leq |+VOUT| / |-VOUT| \leq 1.02$

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to 100BASE-TX Standard in Appendix A.

3.3.4 Rise and Fall Time

Purpose: To ensure that the device rise and fall time are within the specified bounds.

Pass Condition: The rise and fall time (between 10% and 90% voltage levels for both positive and negative) should be between 3 ns and 5 ns. The maximum and minimum rise and fall times should be within 0.5 ns.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to 100BASE-TX Standard in Appendix A.

3.3.5 Rise and Fall Time Symmetry

Purpose: To ensure that the device rise and fall time symmetry are within the specified bounds.

Pass Condition: Rise and fall time symmetry should be less than 500 ps.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to 100BASE-TX Standard in Appendix A.

3.3.6 Waveform Overshoot

Purpose: To ensure that the waveform overshoot is below the specified bound.

Pass Condition: The overshoot (both positive and negative maximum voltage level on transition) should not exceed 5% over the steady-state voltage level (VOUT).

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to 100BASE-TX Standard in Appendix A.

3.3.7 Jitter

Purpose: To ensure that the transmit output jitter is within the specified bounds.

Pass Condition: The transmit output jitter should be less than 1.4 ns.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to 100BASE-TX Standard in Appendix A.

3.3.8 Duty Cycle Distortion

Purpose: To ensure that the duty cycle distortion is below the specified bound.

Pass Condition: The duty cycle distortion (defined as above and below 50% of Vout) should not exceed ±0.25 ns.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to 100BASE-TX Standard in Appendix A.

3.3.9 Return Loss

Purpose: To ensure that the return loss is above the specified attenuation.

Pass Condition: The reflection of any incident signal to the PHY must be attenuated:

- ≥16 dB over the frequency range of 2 MHz to 30 MHz
- ≥10 – 20log 10 (f /30) dB over the frequency range 30 MHz to 60 MHz (f in MHz)
- ≥10 dB over the frequency range 60 MHz to 80 MHz

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to 100BASE-TX Standard in Appendix A.

Note: A spectrum analyzer may be needed depending on Ethernet Compliance Software.

3.3.10 Common-Mode Rejection

Purpose: Verify that the PHY's common-mode rejection ratio is within the specified bounds.

Pass Condition: See ANSI X3-263-1995 9.2.3

Specific Test Setup: Refer to the high voltage injection testing procedures (not included in this app note). Verify the correct test fixture connections. Configure PHY to 100BASE-TX Standard in Appendix A.

4 Debug Test Methods

The DP83822 includes various debug tools within the device to identify issues with the connected system or improper implementation of the device itself. The following subsections are ordered in the way that debug should proceed if operation is not as expected.

4.1 Common System Issues

This list serves as a common check to ensure that the DP83822 is properly implemented.

- Are the AVD, CT, and VDDIO supply rails at expected levels?
- Is the Magnetic CT tied to AVD?
- Is RBIAS resistor 4.87 KΩ?
- Is the reference clock at the correct frequency?
- Does the MDIO have a 2.2-KΩ pullup resistor?
- Do the LED_0 and LED_1 pins have parallel pullup or pulldown resistors to the LED and current-limiting resistor?
- Are the RESET_N and INT/PWDN_N not pulled to a low state?
- Are the bootstraps latching to the expected state?
  - Read Strap Latch-in Register #1 (SOR1, address 0x0467)
  - Read Strap Latch-in Register #2 (SOR2, address 0x0468)
- Register settings are correctly executed?

4.2 Loopback Modes

There are six internal loopback paths within the DP83822. Each loopback serves a unique purpose in the debug process and system verification. The subsections below detail the most common loopback modes used and possible case scenarios for why they might be implemented.

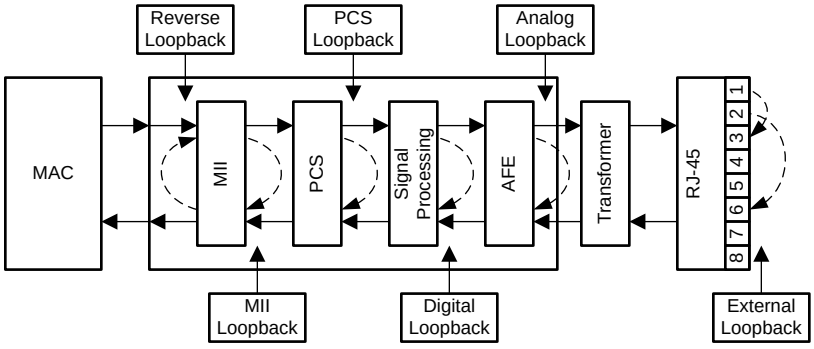

Figure 2. Loopback Test Modes

4.2.1 MII Loopback

MII Loopback is the shallowest loopback within the DP83822. Data presented on the TX pins is internally routed back to the RX pins. This loopback mode is enabled by setting bit[14] in the Basic Mode Control Register (BMCR, address 0x0000).

Purpose: MII Loopback is typically used to identify issues along the digital transmit and receive paths. This shallow loopback can isolate and help identify issues with routing errors, cut traces and unconnected pins.

Register Setting: Refer to MII Loopback 100BASE-TX or 10BASE-Te script in Appendix B.

4.2.2 Analog Loopback

Analog Loopback is the deepest forward loopback within the DP83822. Data received on the TX pins from a connected MAC is passed through the entire transmit block. The data is then outputted on the TD pins by the AFE. An internal path within the DP83822 routes the TD data to the AFE receiver, where the data is then passed through the entire receive block and presented on the RX pins to the connected MAC. This loopback mode is enabled by setting bit[3] in the BIST Control Register (BISCR, address 0x0016).

Note: This mode requires 100-Ω termination as shown in Figure 3. This mode also requires the PHY to be operating in either forced 100BASE-TX or 10BASE-Te mode.

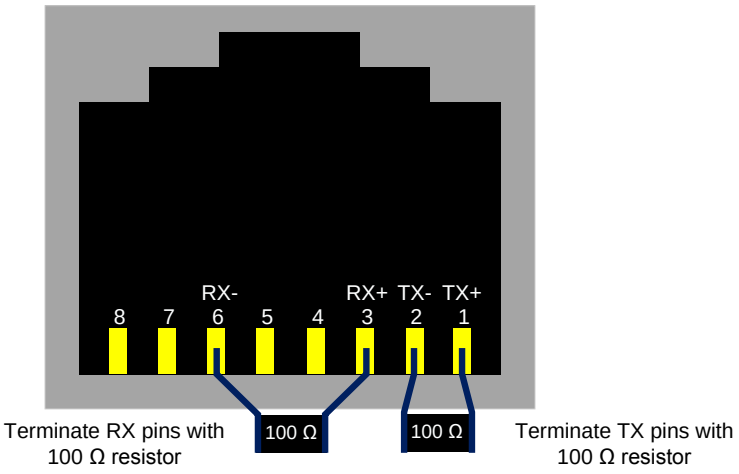

Figure 3. Analog Loopback Terminations

Purpose: Analog loopback is typically used to identify issues with improper MDI termination and reference clock violations. This loopback is often used when performing IEEE 802.3 compliance tests.

Register Setting: Refer to Analog Loopback 100BASE-TX or 10BASE-Te script in Appendix B.

4.2.3 External Loopback

External loopback is not a loopback within the DP83822; however, it is included in this discussion because it is a useful tool in the debug process. Data received on the TX pins from a connected MAC is passed through the entire transmit block. The data is then outputted on the TD pins by the AFE. Transmit data pins are directly wired back to the receive data pins using a loopback cable. The data is received by the DP83822 and is then passed through the entire receive block and presented on the RX pins to the connected MAC.

Note: External loopback requires the use of a loopback cable as shown in Figure 4.

Figure 4. Loopback Cable

Purpose: External loopback is used to check the entire system, including external passive components (that is, termination resistors, magnetics and connectors).

Register Setting: No register configuration is necessary for external loopback.

4.3 Built-In Self-Test

The DP83822 has an internal BIST that allows for on-board testing without the need for a connected MAC. BIST can be used for customized testing and debugging scenarios. The DP83822 BIST is controlled using the BIST Control Register (BISCR, address 0x0016), BIST Control and Status Register #1 (BICSR1, address 0x001B) and the BIST Control and Status Register #2 (BICSR2, address 0x001C).

BIST packet length (address 0x001C) and IPG (address 0x001B) can be controlled in the DP83822 allowing for customizable test scenarios. Bits[7:0] in BICSR1(address 0x001B) defines the IPG in bytes. Bits[10:0] in BICSR2(address 0x001C) defines the packet length in bytes.

Standard Setup for BIST:

1. Connect 5-V DC supply to the EVM through the micro-USB connector. For other external power supply options see the *DP83822 EVM User's Guide* (SNLU179).
2. Configure the PHY for the specific loopback test by setting the corresponding SMI registers as outlined in Appendix B.
3. Perform the test by writing the SMI registers as outlined in Appendix B. Read the BIST Control Register (BISCR, address 0x0016) for PRBS status, and BIST Control and Status Register #1 (BICSR1, address 0x001B) for BIST error count. Note that to read BIST error count, bit[15] in BICSR1(address 0x001B) must be set to 1. This will lock the current value of the BIST errors for reading. Note that setting bit[15] also clears the BIST Error Counter.

4.4 Cable Diagnostics

The DP83822 offers Time Domain Reflectometry (TDR) . TDR can be used to determine opens, shorts, cable impedance mismatch, cable length, and other discontinuities along the cable.

IEEE802.3u Compliance Testing Scripts for the DP83822

A.1 100BASE-TX Standard Test Script

```
begin
001F 8000        //software reset (clears register)
0000 2100        //programs DUT to 100BASE-TX mode
0019 0021        //programs DUT to Forced MDI mode, set to 4021 for MDIX mode
001F 4000        //digital reset (doesn't clear register)
end
```

A.2 10BASE-Te Link Pulse Test Script

```
begin
001F 8000        //software reset (clears register)
0000 0100        //programs DUT to 10BASE-Te mode
0019 0021        //programs DUT to Forced MDI mode, set to 4021 for MDIX mode
001F 4000        //digital reset (doesn't clear register)
end
```

A.3 10BASE-Te Standard Test Script

```
begin
001F 8000        //software reset (clears register)
0000 0100        //programs DUT to 10BASE-Te mode
0019 0021        //programs DUT to Forced MDI mode, set to 4021 for MDIX mode
0016 7108        //programs DUT to generate data and enables analog loopback mode
001F 4000        //digital reset (doesn't clear register)
end
```

Loopback and BIST Mode Scripts for the DP83822

B.1 MII Loopback 100BASE-TX Script

```
begin
001F 8000          //software reset (clears register)
0000 6100          //programs DUT to 100BASE-TX mode and enables MII Loopback
001F 4000          //digital reset (doesn't clear register)
end
```

B.2 MII Loopback 10BASE-Te Script

```
begin
001F 8000          //software reset (clears register)
0000 4100          //programs DUT to 10BASE-Te mode and enables MII Loopback
001F 4000          //digital reset (doesn't clear register)
end
```

B.3 Analog Loopback 100BASE-TX Script

```
begin
001F 8000          //software reset (clears register)
0000 2100          //programs DUT to 100BASE-TX mode
0019 0021          //programs DUT to Forced MDI mode, set to 4021 for MDIX mode
0016 0108          //enables analog loopback mode
001F 4000          //digital reset (doesn't clear register)
end
```

B.4 Analog Loopback 10BASE-Te Script

```
begin
001F 8000          //software reset (clears register)
0000 0100          //programs DUT to 10BASE-Te mode
0019 0021          //programs DUT to Forced MDI mode , set to 4021 for MDIX mode
0016 0108          //enables analog loopback mode
001F 4000          //digital reset (doesn't clear register)
end
```

B.5 Reverse Loopback 100BASE-TX Script

```
begin
001F 8000        //software reset (clears register)
0000 2100        //programs DUT to 100BASE-TX mode
0016 0110        //enables reverse loopback mode
001F 4000        //digital reset (doesn't clear register)
end
```

B.6 Reverse Loopback 10BASE-Te Script

```
begin
001F 8000        //software reset (clears register)
0000 0100        //programs DUT to 10BASE-Te mode
0016 0110        //enables reverse loopback mode
001F 4000        //digital reset (doesn't clear register)
end
```

B.7 BIST 100BASE-TX Script

```
begin
001F 8000        //software reset (clears register)
0000 2100        //programs DUT to 100BASE-TX mode
001B 007D        //bits[7:0] determine IPG, default 0x7D is equal to 125 bytes
001C 05EE        //bits[10:0] determine packet length, default 0x05EE is equal to 1518 bytes
0016 7100        //enable continuous error check BIST mode
001F 4000        //digital reset (doesn't clear register)
end
```

B.8 BIST 100BASE-TX with Analog Loopback Script

```
begin
001F 8000        //software reset (clears register)
0000 2100        //programs DUT to 100BASE-TX mode
0019 0021        //programs DUT to Forced MDI mode
001B 007D        //bits[7:0] determine IPG, default 0x7D is equal to 125 bytes
001C 05EE        //bits[10:0] determine packet length, default 0x05EE is equal to 1518 bytes
0016 7108        //enable continuous error check BIST mode with analog loopback mode
001F 4000        //digital reset (doesn't clear register)
end
```

B.9 BIST Status and Error Count Script

```
begin
0016          //reads address 0x0016, bits[11:9] show packet generator and checker status
001B 807D     //writes bit[15] to ‘1’, sets bits[7:0] for 125 byte IPG.
001B          //reads address 0x001B, bits[15:8] show BIST Error Count
end
```

PHY Test Mode Waveforms

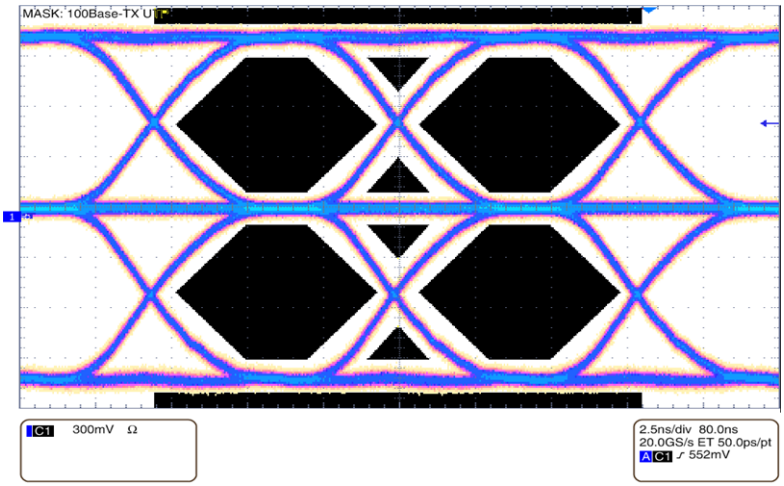

Figure 5. 100BASE-TX Template

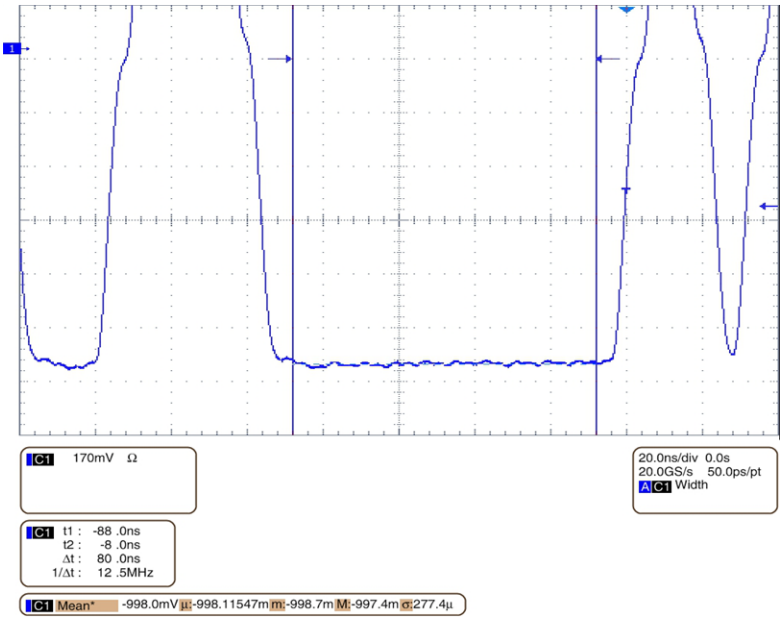

Figure 6. 100BASE-TX Differential Output Voltage (Negative)

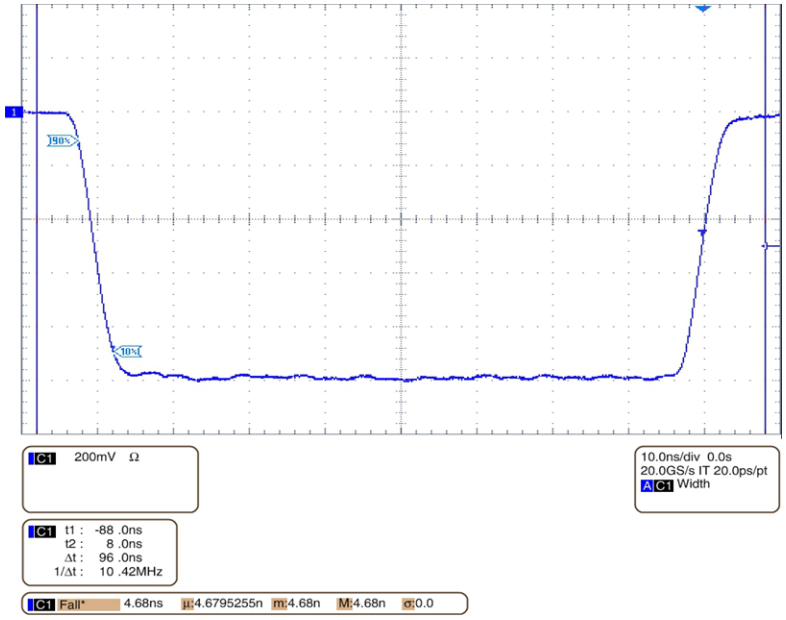

Figure 7. 100BASE-TX Fall Time

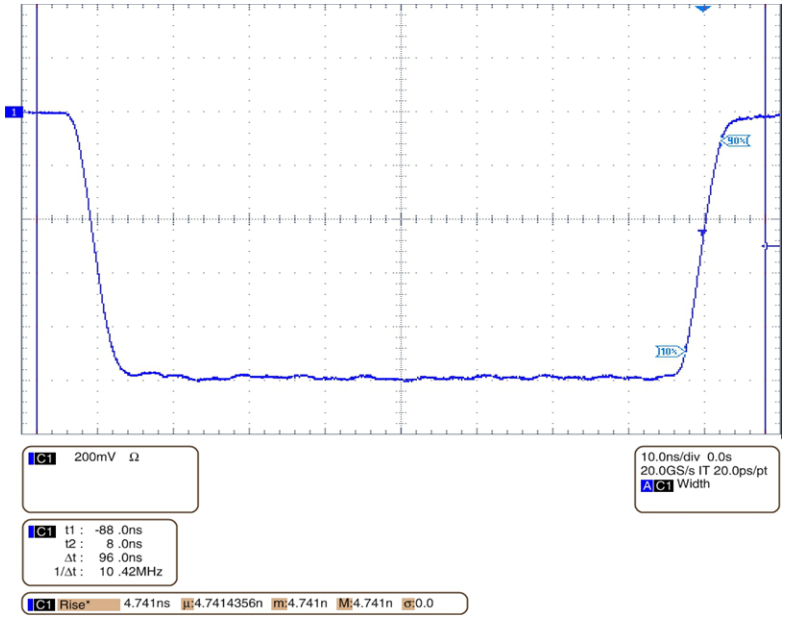

Figure 8. 100BASE-TX Rise Time

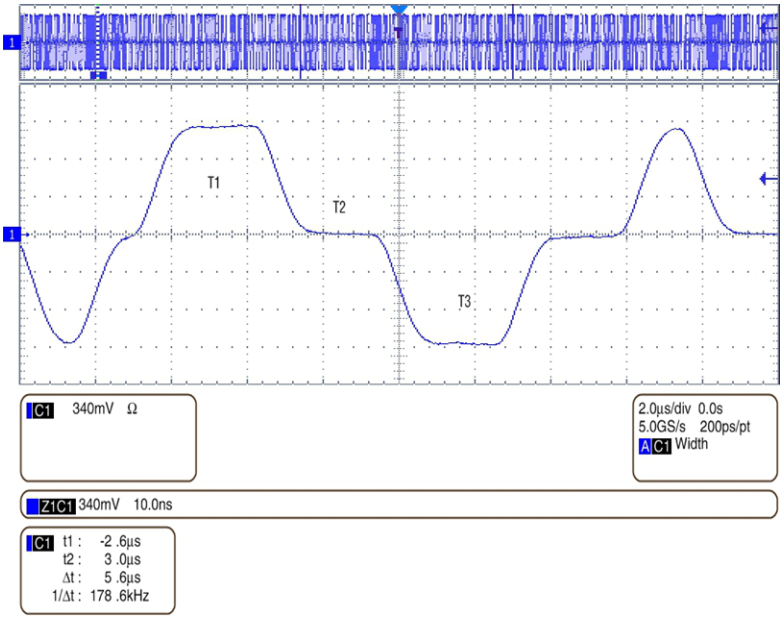

Figure 9. 100BASE-TX Duty Cycle Distortion

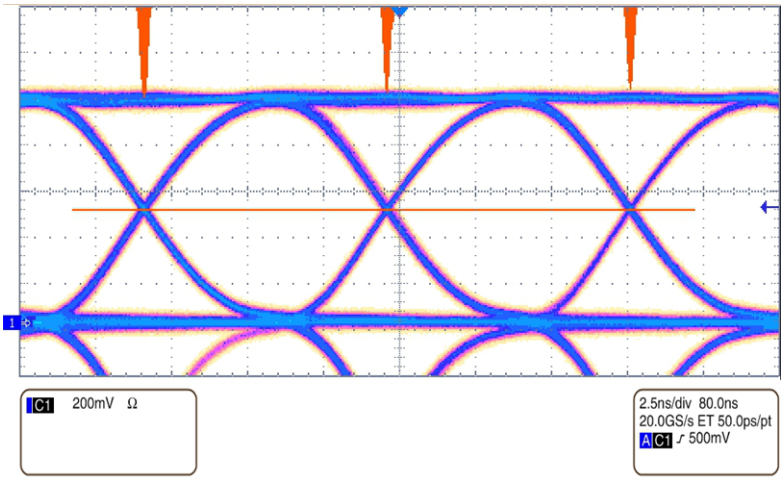

Figure 10. 100BASE-TX Jitter

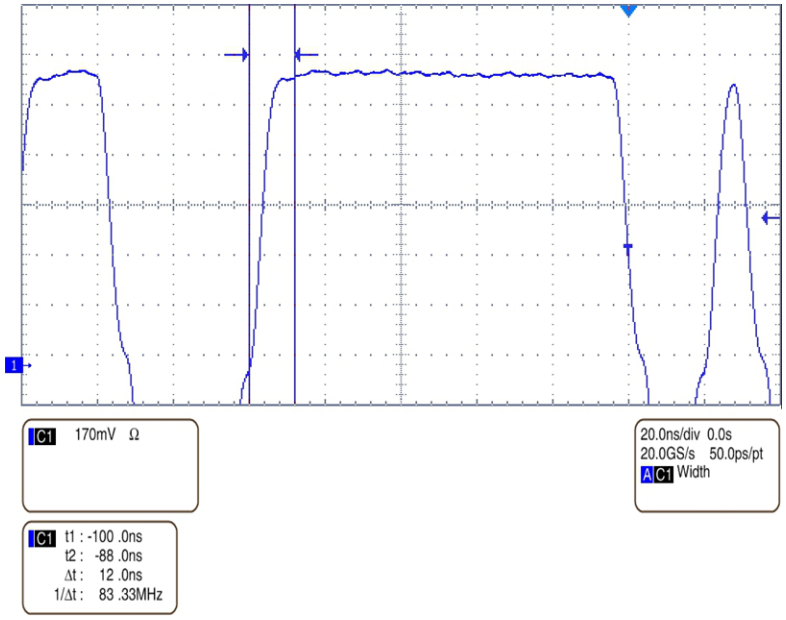

Figure 11. 100BASE-TX Waveform Overshoot

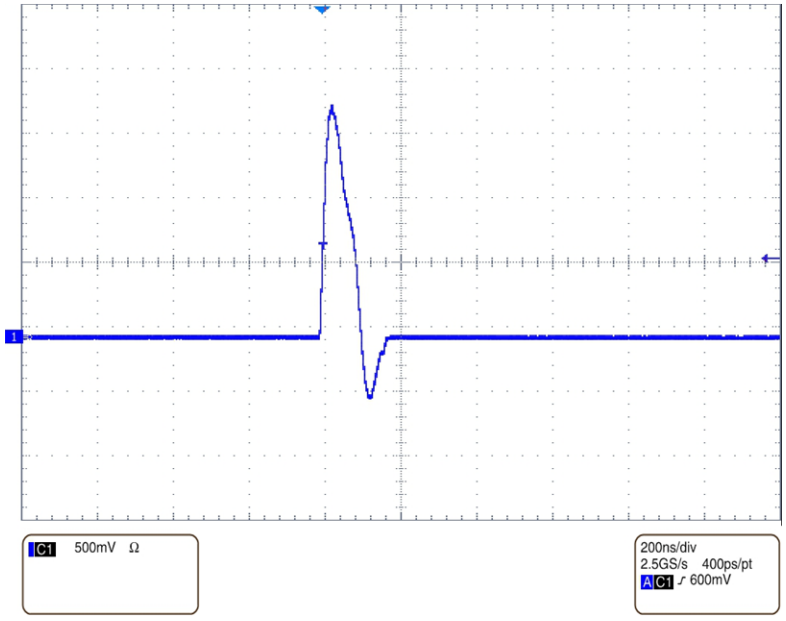

Figure 12. 10BASE-Te Link Pulse

TI's USB-2-MDIO Tool

The SMI can be managed using TI's USB-2-MDIO tool via a MSP430 Launchpad (either MSP430G2 or MSP430F5).

Setup for SMI access with TI's USB-2-MDIO Tool:

1. Download and follow the setup instructions for TI's USB-2-MDIO Tool (see the *USB-2-MDIO User's Guide* (SNLU197)). Verify that the MSP430 LaunchPad drivers are installed.
2. Connect Host PC to DP83822 EVM via MSP430 Launchpad. Connect a USB cable to the LaunchPad, and then break out MDIO, MDC, and GND. When using the MSP430G2, pin 1.5 connects to MDIO pin on the DP83822 EVM and pin 1.4 connects to MDC pin on the DP83822 EVM. When using the MSP430F5, pin 4.1 connects to MDIO pin on the DP83822 EVM and pin 4.2 connects to MDC pin on the DP83822 EVM. A common ground needs to be connected between the DP83822 EVM and MSP430.

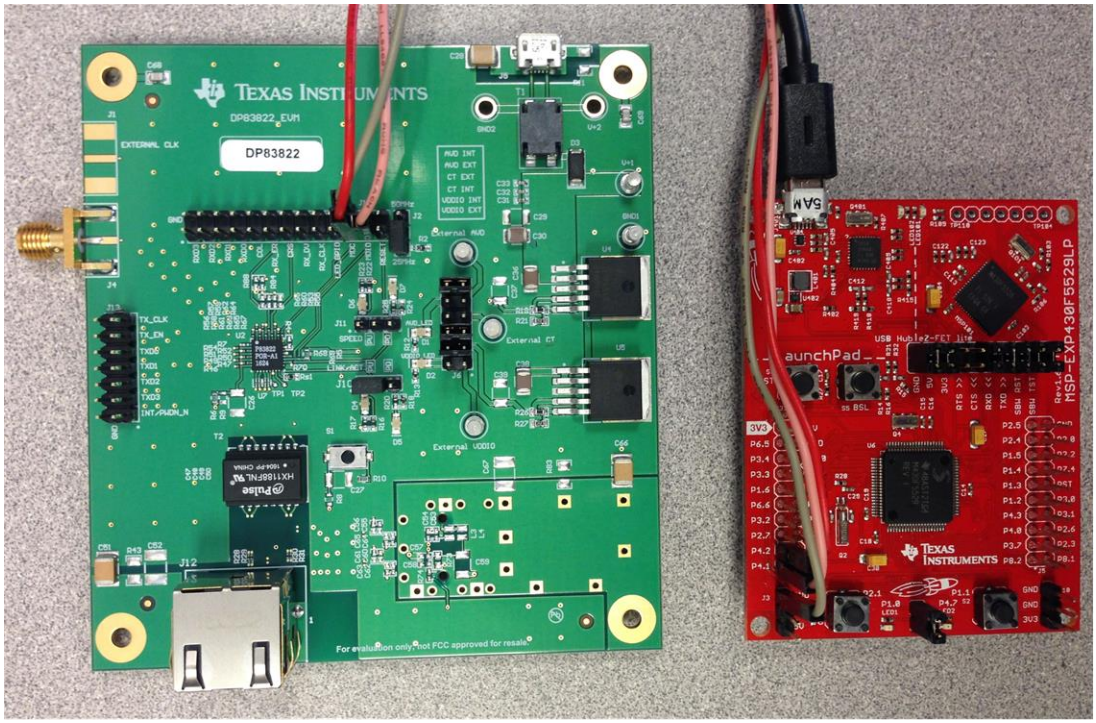

Figure 13. DP83822 EVM Connected to a MSP430F5

3. Start the USB-2-MDIO Tool, select the correct PHYID and com port (PHY must be powered). Open the port and write and/or read desired registers. Scripts can be run by navigating to the *File* tab located on the top left corner of the tool. For additional information regarding scripting and saving, refer to the *USB-2-MDIO User's Guide* (SNLU197).

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265