Application Report
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DP83822 Jitter Analysis

Aniruddha Khadye

ABSTRACT

This application note explores how clock jitter affects performance of DP83822 10/100 Industrial Ethernet PHY. The methods in this document describe how to set up a jitter measurement test bench and determine acceptable levels of clock jitter for proper operation and compliance.

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1 Introduction

The timing variations in signal edges from their ideal values is called Jitter. With the increase in data rates, jitter has become important factor in system design. A clock with high jitter can cause performance degradation in Ethernet subsystem such as compliance failures, high Bit Error Rate etc. Clock jitter can be caused due to factors such as thermal noise, power supply variations, loading conditions, device nosie and interference coupled from other circuit on the subsystem. Jitter can be measured and expressed in multiple ways. Important types of jitter are as follows;

- Period Jitter
- Cycle to Cycle Jitter
- Long Term Jitter
- Time Interval Jitter
- Phase Noise

For the purpose of this app note we will be focusing on Phase Noise.

2 Phase Noise

Phase Noise is a method of describing jitter in the frequency domain. Phase noise can be described as a set of noise values at different frequency offsets or as a continuos noise plot over a range of frequencies. When a continuos noise plot is used phase noise is expressed in seconds.

An ideal clock has all the energy located at the carrier frequency. In real-life scenario, energy is leaked out over a range of frequencies on both sides of the carrier frequencies. For expressing Phase Noise it is necessary to define a start and stop frequency offset with respect to the carrier frequency. These frequency offsets are application dependent.

For the scope of this application note, phase noise will be expressed as the integrated noise from 100Hz to 20MHz offset from center frequency of 25MHz. For measuring jitter tolerance of the PHY it is required to inject controlled jitter in the reference clock and observe the effect on PHY Performance. The performance metrics for the PHY will be the 100Base-TX Transmit jitter and an optional measurement of Bit Error Rate.

Figure 1 shows the Jitter measurement setup.

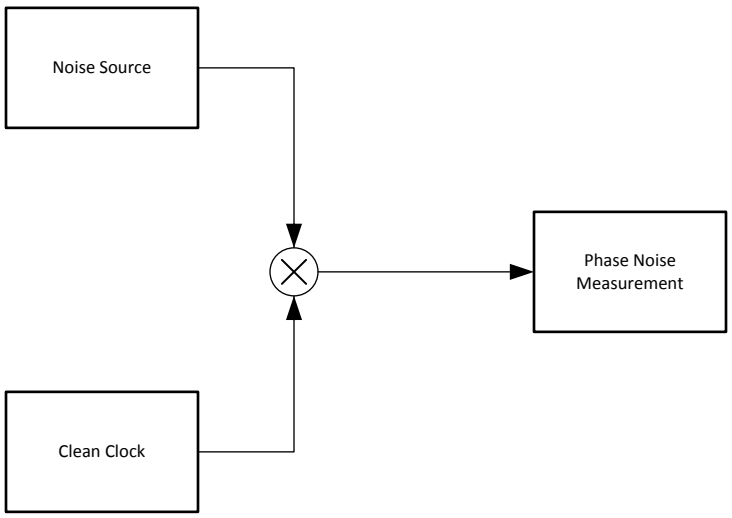


Figure 1. Clock Jitter Measurement Setup

A clean clock is modulated with controlled amount of noise. The output is connected to a signal analyzer in Phase Noise measurement mode. The noise source can be any signal generator which can generate random noise signal. Test setup for this application note used R & S SMB100A as the clock source, Agilent 33250A as the noise source and Agilent E5052A as the phase noise measurement device. The output of 33250A is connected to SMB100A and modulation of clean clock with noise occurs within the SMB100A.

The phase noise plots of reference clock with and without jitter are shown in Figure 2 and Figure 3.

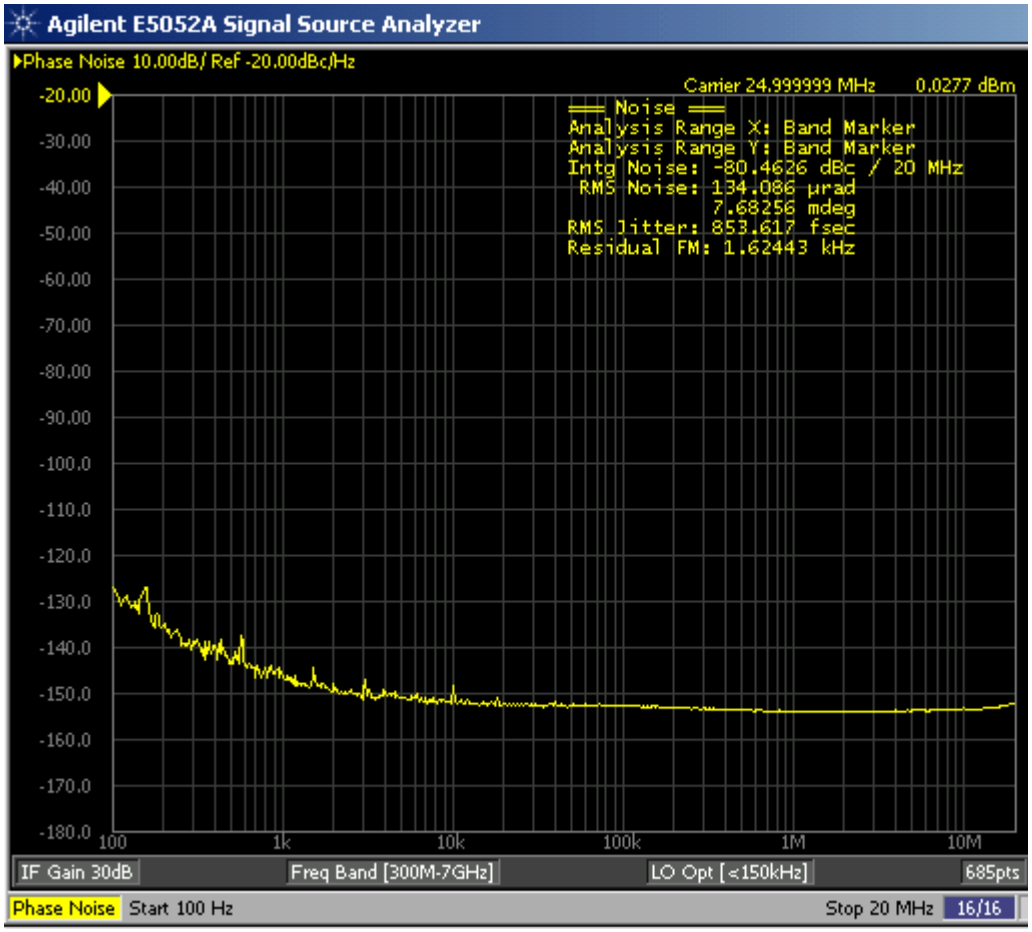


Figure 2. Phase Noise of Reference Clock without Jitter

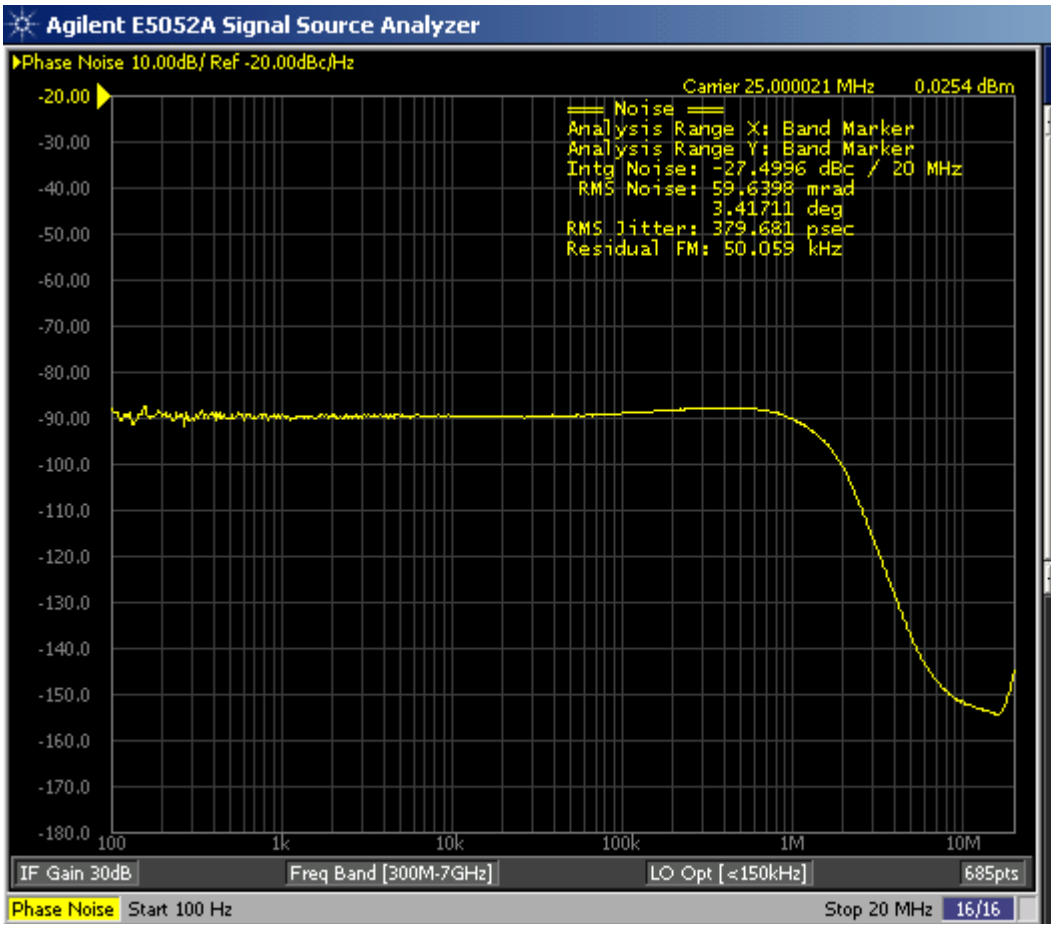


Figure 3. Phase Noise of Reference Clock with Jitter

3 DP83822 Jitter Tolerance

For demonstrating DP83822 jitter tolerance, a DP83822 EVM is used as Equipment Under Test (EUT). The EUT is configured to accept external reference clock (25MHz). For observing performance difference, 100Base-TX Transmit Jitter is measured at output of EUT using the Ethernet Compliance Software on TEK DPO 70804C oscilloscope and TEK P6330 Differential Probe. Bit Error Rate measurements are also conducted using SmartBits 200 chassis with SX-7405 card (Network Traffic Generator). Figure 4 shows the block diagram for Jitter Tolerance measurement.

Please note that these measurements are conducted at room temperature in lab setting on limited samples.

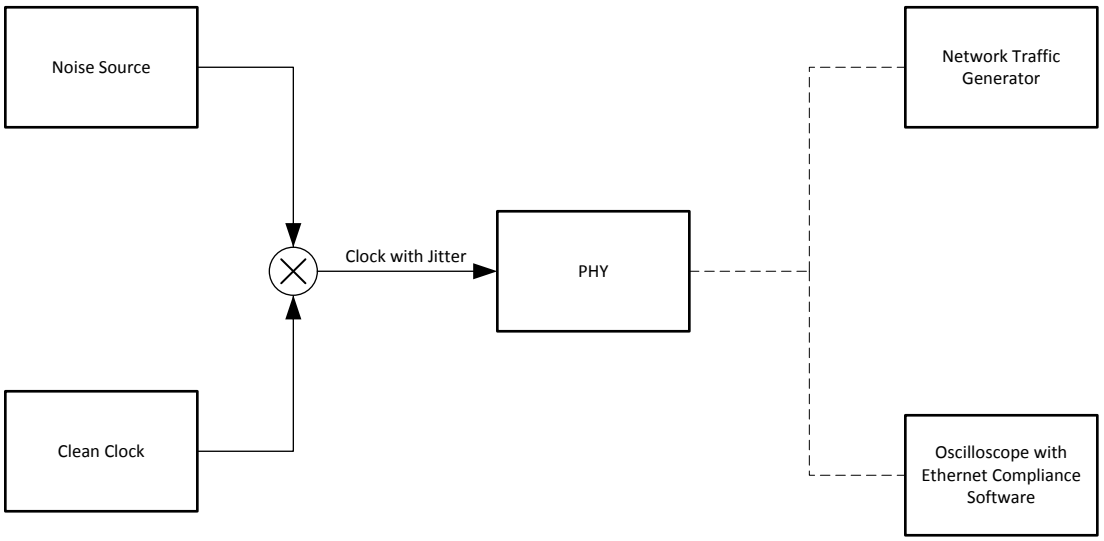


Figure 4. Jitter Tolerance Test Bench

3.1 100Base-TX Transmit Jitter

The DP83822 is configured for generating scrambled idles and the transmit jitter is measured on the compliance software. The aim is to check at what jitter level the DP83822 fails IEEE compliance test. The procedure is explained below.

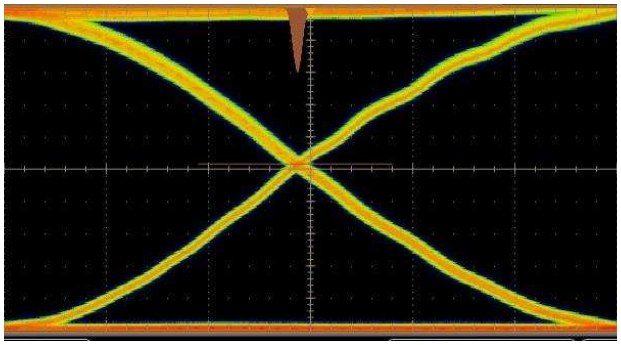
Equipment List

- Agilent 33250A
- R & S AMB100A
- Tek DPO 70804C with Tek P6330 differential probe
- Agilent E5052A
- Ethernet Compliance software
- Ethernet Compliance Test Fixture TF-GBE
- Co-ax cables

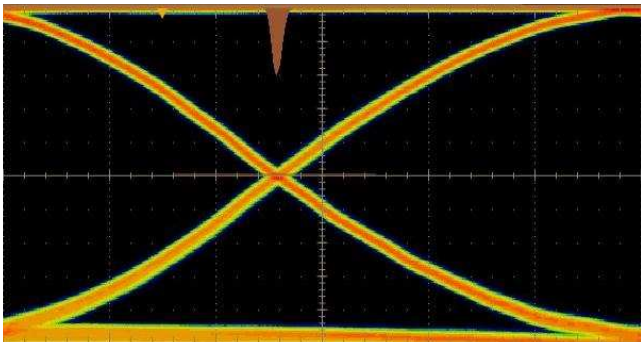
Procedure

- Turn off modulation to get jitter free reference clock.
- Configure DP83822 for scrambled idles.
  - Write 0x2100 to Register 0x00. This forces 100M operation.
  - Write 0x0021 to Register 0x19. This force MDI mode.
- Use TC2 section of the Ethernet Compliance Test Fixture to probe Channel A of EUT using the differential probe.
- Follow the test guide for running Transmit Jitter Measurement. This test should be a pass since there is no jitter on the clock
- Turn modulation on and repeat the measurement. Increase the amplitude of noise wave untill Transmit jitter test results in failure.
- Disconnect the Clock from the EUT and connect it to Agilent E5052A via DC Block. Record the RMS Jitter with Averaging turned on.

Figure 5 and Figure 6 show the difference in output transmit jitter with and without clock jitter.

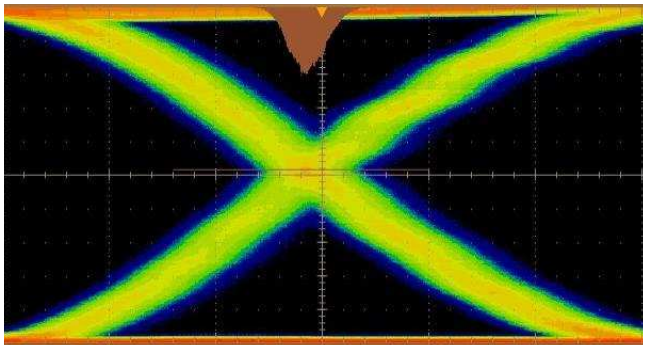


Transmit Jitter (+ve)

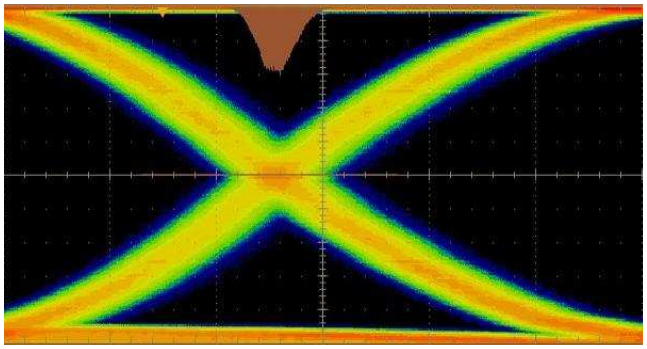


Transmit Jitter (-ve)

Figure 5. 100Base-TX Transmit Jitter with Clean Clock



Transmit Jitter (+ve)



Transmit Jitter (-ve)

Figure 6. 100Base-TX Transmit Jitter with Bad Clock

The DP83822 can tolerate approximately 375ps of RMS jitter on the clock. The RMS jitter was measured from 100Hz offset to 20MHz offset from the center frequency.

3.2 Bit Error Rate

This test is optional. A network traffic generator is used for transmitting packets to the DP83822. The DP83822 is configured in reverse loopback. The network traffic generator receives the packet and checks for transmit errors. The input clock jitter for EUT is increased untill Packet errors are observed at the network traffic generator. For this experiment, SMB200 chassis with SX-7405 card is used as the traffic generator. SMB200 has its own SmartWindows software for configuring and controlling the cards.

Equipment List

- Agilent 33250A
- R & S AMB100A
- Tek DPO 70804C with Tek P6330 differential probe
- Agilent E5052A
- SMB200 Chassis with SX-7405 10/100 card
- Windows XP computer with SmartWindows Software
- Co-ax cables

Procedure

- Power on SMB200 and EUT. Configure EUT for reverse loopback by writing 0x0110 in register 0x16.
- Connect SX-7405 card with EUT using a Cat5 cable.
- Configure SX-7405 to transmit ethernet packets. The packets should be 1518bytes and channel utilization should be 100%.
- Slowly increase Noise Amplitude on Agilent 33250A till errors are observed on received ethernet packets.
- Connect the clock to the Phase Noise measurement setup as shown in Figure 1 and measure RMS jitter with Averaging turned on.

DP83822 can tolerate approximately 445ps of input clock jitter.

4 Conclusion

This app note explains the effect of reference clock jitter on the performance of DP83822 and the procedure to test the jitter performance. Jitter tolerance numbers are provided at the end of each test. These numbers are derived from limited sample set of DP83822 devices tested in lab setting.

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