Application Note

How and Why to Use the DP83826E for EtherCAT® Applications

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ABSTRACT

This document describes how to connect an Ethernet PHY onto an EtherCAT® ESC.

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Trademarks

1 Introduction

When starting an EtherCAT® design, first review the *Section I – Technology EtherCAT® Protocol, Physical Layer, EtherCAT® Processing Unit, FMMU, SyncManager, SII EEPROM, Distributed Clocks Data Sheet*. This document describes how to connect an Ethernet PHY onto an EtherCAT® ESC. This document describes the needed interfaces between the ESC and the Ethernet PHYs, those interfaces are the PHY Management (PHY MI) and EtherCAT Interface and are illustrated in Figure 1 from the previously referenced data sheet. In chapter 4 (Physical Layer Common Features) and chapter 5 (Ethernet Physical Layer) The interface between the ESC and the PHY is described. Some key points to investigate here include:

- ESC in reset state has to leave the PHY disabled (No link connection until active ESC)
- MII interface has special use the pins TX_CLK,COL,CRS,TX_ER; for details, see table 14 (Special/Unused MII Interface signals).
  - EtherCAT® has a special setup to determine Link Detection in several steps; see section 5.6
- LINK_MII signal, this is typically an LED output signal which indicate a 100 Mbit/s Full Duplex link
- Enhanced link detection which is ensuring that the link signal is checked every approximately 10 µs; see section 5.6.2 for details

Another part to look into is the document EtherCAT PHY specification. This is found in the *Application Note – PHY Selection Guide* on the EtherCAT® home page. In this document the specifications and the

recommendations of Ethernet PHY performance is documented the following lists and are a copy paste of that document version 2.6 (2017-10-04).

This document compares the EtherCAT® specification and recommendations in respect to the new TI PHY the DP83826. The first bullet is the EtherCAT® PHY specification requirement and the second bullet is the DP83826 compliance to the requirement.

2 EtherCAT® Specification Requirements

- The PHYs have to comply with IEEE 802.3 100BaseTX or 100BaseFX.
  - The DP83826 is a IEEE 802.3 compliant 100BASE-TX Ethernet PHY, see section 9.1 in the data sheet
- The PHYs have to support 100 Mbit/s Full Duplex links.
  - DP83826 supports full duplex operation for both 10Mbit/s and 100Mbit/s, see section 9.5.1, register BMSR(address 0x1)
- The PHYs have to provide an MII (or RMII/RGMII1) interface.
  - The DP83826 provides a MII and RMII interface connection, see section 9.1 in the data sheet)
  - Notice that the typical latency of the RMII interface (in general) is higher than the EtherCAT® specified latency requirement.
- The PHYs have to use auto-negotiation in 100BaseTX mode.
  - Has an Auto-negotiation feature which can be enabled or disabled with the strap option, see section 9.3.1 in the data sheet
- The PHYs have to support the MII management interface.
  - Supports the serial management interface up to a maximum clock rate of 24 MHz (MII management interface). This is in section 9.3.9 in the data sheet.
- The PHYs have to support MDI/MDI-X auto-crossover in 100BaseTX mode.
  - Supports MDI/MDI-X auto-crossover reception, see section 9.3.2 in the data sheet
- PHY link loss reaction time (link loss to link signal/LED output change) has to be faster than 15 µs to enable redundancy operation.
  - Fast link-Drop functionality called FLD which shortens the observation window to 10 µs before enabling the link loss indication, see section 8.6 “Fast Link Pulse Timing” and 9.3.14.2 in the data sheet.
- The PHYs must not modify the preamble length.
  - The DP83826 does not modify the preamble length.
- The PHYs must not use IEEE802.3az Energy Efficient Ethernet.
  - The DP83826 supports the IEEE802.3az standard, this feature is disabled by default
- The PHYs must offer the RX_ER signal (MII/RMII) or RX_ER as part of the RX_CTL signal (RGMII).
  - The DP83826 supports MII/RMII with standard interface including the RX_ER signal
- The PHYs have to provide a signal indicating a 100 Mbit/s (Full Duplex) link, typically a configurable LED output. The signal polarity is active low or configurable for some ESCs.
  - Four programmable LED outputs which can each show 100 Mbit/s (Full Duplex) link. See section 9.5.1, register BMSR (address MLEDCR (0x25), LEDCFG (0x460).
- The PHY addresses should be equivalent to the logical port number (0–3). Some ESCs also support a fixed offset (for example, offset 16, PHY addresses are logical port number plus 16: 16-19), an arbitrary offset, or even individually configurable PHY addresses. If none of these possibilities can be used, the PHY address should be configured to logical port number plus 1 (1–4), although some features (for example, Enhanced Link Detection) cannot be used in this case, because apart from the optional configurable PHY address offset, the PHY addresses are hard-coded inside the ESCs.
  - The Serial Management interface has 8 PHY addresses which can be set using strap resistors, see section 9.3.9 and 9.4.1 in the data sheet.
- PHY configuration must not rely on configuration via the MII management interface, that is, required features have to be enabled after power-on, for example, by default or by strapping options. PHY startup should not rely on MII management interaction, that is MDC clocking, since many ESCs do not communicate with the PHY via management interface unless the EtherCAT® master requests this (only the EtherCAT® IP Core with MI Link detection and configuration will communicate without master interaction).
  - Bootstrap configuration setting up the PHY in a specific mode which allow EtherCAT® communication a short list of the important boostrap pins are seen in Table 2-1. F or more details, see section 9.4.1.2 in the data sheet.

Table 2-1. Strap Function Pin per DP83826 Data Sheet

Function	Pin Name (Number)	Pullup or Pulldown
Auto-Neg /Force Mode	LED0 (30)	Pullup to Enable
PHY address	RX_D3 (13), RX_D2 (14), RX_D1 (15)	Default 0001

- All PHYs connected to one ESC and the ESC itself must share the same clock source, so a TX FIFO can be omitted. This can be achieved by sourcing the PHYs from an ESC clock output or by sourcing the PHYs and the ESC from the same quartz oscillator. The ESC10/20 uses TX_CLK as a clock source, both PHYs have to share the same quartz oscillator.
  - This can be resolved using an external clock source for the DP83826 specification for this clock source is described in section 8.6, *25MHz Input Clock Tolerance*.
  - The DP83826 PHY has a clock out option which can be used to clock the second PHY
- The phase offset between TX_CLK and the clock input of the PHYs is compensated inside the ESC, either manually by configuration or automatically. The clock period cannot change between the devices since the PHYs and the ESC have to share the same clock source.
  - This requirement is PHY independent and is a requirement for the MAC interface
- Manual TX Shift compensation: ET1100, ET1200, and IP Core provide a TX Shift configuration option (configurable TX_EN/TXD signal delay by 0/10/20/30 ns) which is used for all MII ports. Thus, all PHYs connected to one ESC must have the same fixed phase relation between TX_CLK and the clock input of the PHY, with a tolerance of ±5 ns. The phase relation has to be the same each time the PHYs are powered on, or establish a link. As the ESC10/20 use TX_CLK as device clock source, configuration is not necessary, but the requirements for manual TX Shift compensation have to be fulfilled anyway.
  - This tolerance is ±2 ns on the DP83826 and is described in section 8.6 “Latency Timing”.
- Automatic TX Shift compensation: The IP Core supports automatic TX Shift compensation individually for each port. With automatic TX Shift compensation, the PHYs are not required to have the same fixed phase relation each time they are powered on, or establish a link.
  - This requirement is PHY independent and is a requirement for the MAC interface.

Recommendations to Ethernet PHYs used for EtherCAT®:

- Receive and transmit delays should be deterministic, and as low as possible.
  - This latency of the RX and TX signals based on the MII interface is is ±2 ns on the DP83826 and is described in section 8.6 “Latency Timing”.
- Maximum cable length should be ≥ 120 m to maintain a safety margin if the standard maximum cable length of 100 m is used.
  - The DP83826 has been tested up to 150 m, see section 1 in the data sheet.
- ESD tolerance should be as high as possible (4 kV, or better)
  - The DP83826 has been tested out with external protection to withstand ESD Ratings based on the ESD (HBM) for MDI pins ±5 kV and all pins except MDI ±2 kV and ESD (CDM) ±0.7 kV, see section 8.2 ESD Ratings.
  - With external protection IEC 61000-4-2 ESD: ±8 kV contact, ±15 kV air and for IEC 61000-4-4 EFT: ±4 kV @ 5 kHz and 100 kHz using the EVM (DP83826EVM). See section 1 in the data sheet.
- Baseline wander should be compensated (the PHYs should cope with the ANSI X3.263 DDJ test pattern for baseline wander measurements at maximum cable length)
  - Testing has been performed on this parameter and the DP83826 shows excellent performance compensating the baseline wander.
  - It is recommended that the register 0xB has bit 0 set to 0, otherwise the Baseline wander test will fail because the phy drops the link due to the Energy detection is seeing this test pattern as a link drop.
- The PHYs should detect link loss within the link loss reaction time of 15 µs also if only one of the RX+ and RX- lines gets disconnected.
  - Fast link-Drop functionality called FLD which shortens the observation window to 10 µs before enabling the link loss indication, see section 8.6 “Fast Link Pulse Timing” and 9.3.14.2 in the data sheet.
- The PHYs should maintain the link state regardless of the received symbols, as long as the symbols are valid.
  - Fast Link-Drop function FLD, see *Fast link-Drop functionality*.

- Ethernet PHYs for 100BaseFX should implement Far-End-Fault (FEF) completely (generation and detection).
  - This is only needed for the Fiber connections, DP83826 is a 100baseTX
- MDC should not incorporate pullup, pulldown resistors, as this signal is used as a configuration input signal by some ESCs.
  - MDC having internal pulldown resistor (10 kΩ), this has to be taken into account when defining pullup, see section “8.5 Electrical Characteristics” and “7 Pin Configuration and Functions (BASIC Mode”.
- Restriction of Auto-negotiation advertisement to 100 Mbit/s / Full Duplex is desirable (configured by hardware strapping options).
  - Advertisement can be set by strap configuration, see section 9.4.1 in the data sheet.
- Power consumption should be as low as possible.
  - Worst-case power consumption for MII interfaced 100Base TX is a total of 67 mA at 3.3-V Vdda and Vddio, see section 8.5 “Power consumption (Active mode worst case, …..”
- I/O voltage: 3.3 V should be supported for current ASIC and FPGA ESCs, an additional 2.5 V, 1.8 V I/O support is recommended for recent FPGA ESCs.
  - The DP83826 supports 3.3 V and 1.8 V I/O voltage, see section 9.1 in the data sheet.
- Single power supply according to I/O voltage.
  - Support single power supply at 3.3 V, see section 9.1 in the data sheet.
- The PHY should use a 25-MHz clock source (quartz oscillator or ESC output).
  - The DP83826 supports Crystal and oscillator inputs, for details see section 10.2.2.1 “Clock Requirements”
- Industrial temperature range should be supported.
  - The DP83826 supports an industrial temperature range of –40 to 105°C, see section 8.3 in the data sheet

3 Different Methods of Setting up the PHY

To setup the PHY in the correct mode for it to work in the EtherCAT® environment there are some settings which either have to be setup using the Serial Management Interface or using the strap configuration. This setup is like programming the PHY to be setup in a specific mode. The next two sections describe how to setup the PHY.

3.1 Using Serial Management Interface to Setup DP83826 PHY

For this design, the serial management interface was used to program the PHY.

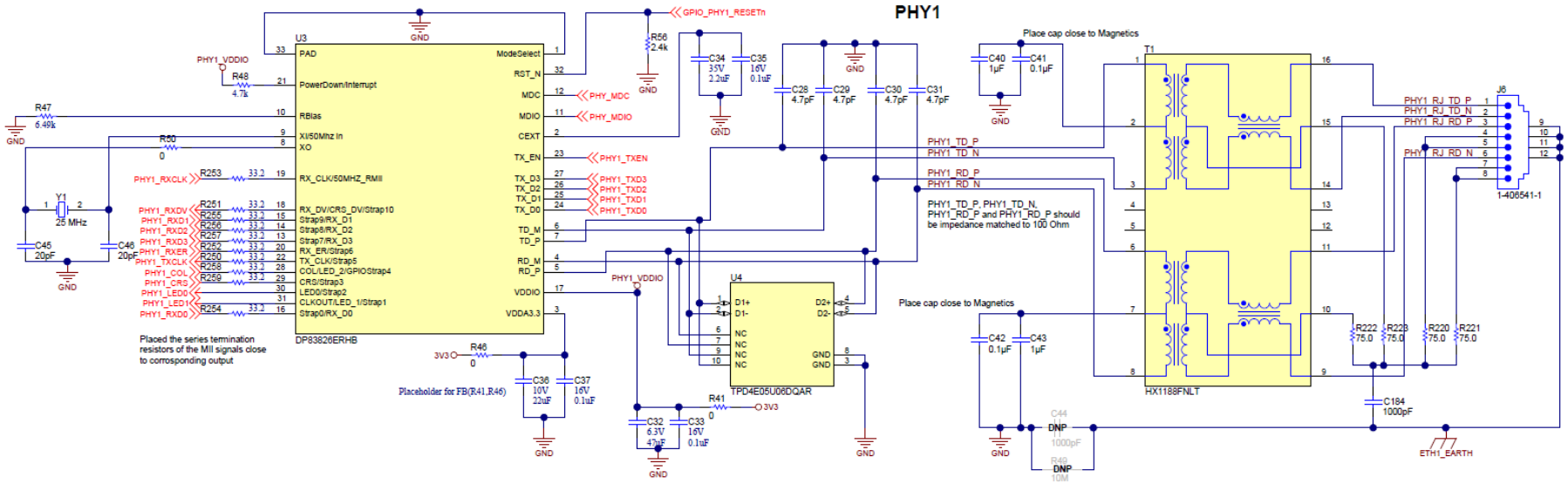

Figure 3-1. PHY1 With SMI Address 0x01

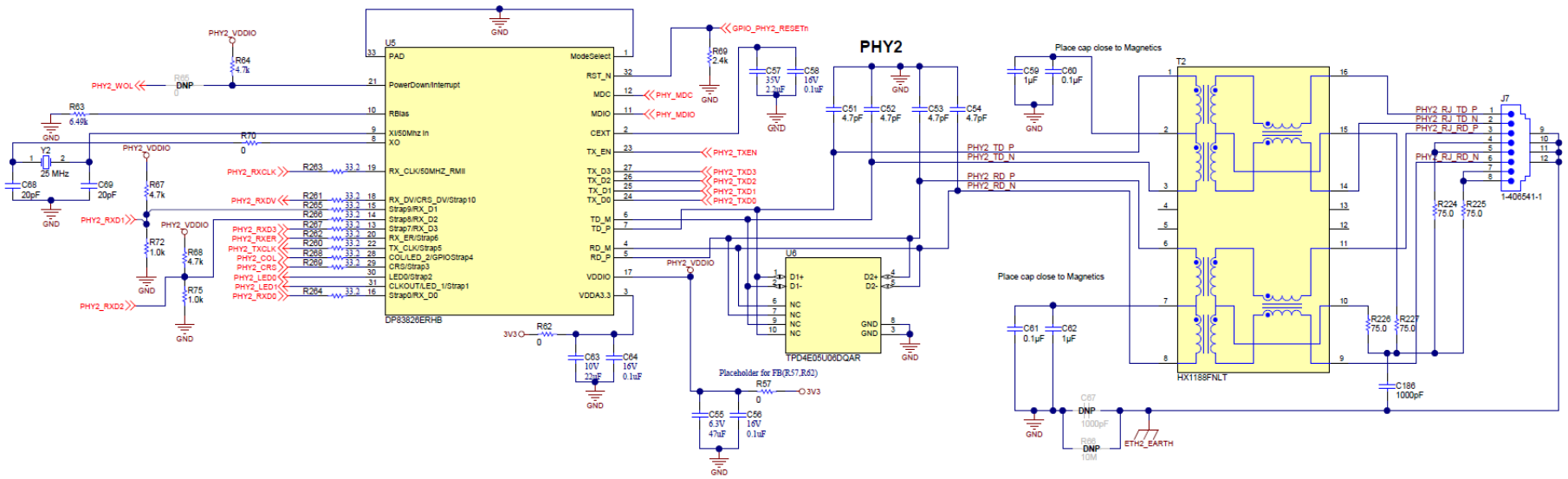

Figure 3-2. PHY1 With SMI Address 0x07

Updated bullet baseline wander test in recommendations to Ethernet PHY's section

Strap resistors soldered: R67 and R68 which changes the address to 0x7 and Auto-negotiate is disabled to ensure no communication before the EtherCAT® stack has been properly initialized.

DP83826 register setup

When setting up the DP83826 PHY to work for EtherCAT® the following register is written as follows.

LED configuration

```
LED 0
Write to PHY register 0x19 value 0x8020 (Auto-MDIX enable and enable LED0 config)
Write to PHY register 0x18 value 0x0080 (Active High polarity)
LED 1
Write to PHY register 0x460 value 0x0005 (100Mbit speed)
Write to PHY register 0x469 value 0x0004 (Active High polarity)
Write to PHY register 0x304 value 0x0008 (Set pin 31 function to LED1)
Auto negotiate enable configuration
Write to PHY register 0x04 value 0x01E1 (Advertise which modes PHY support)
Write to PHY register 0x09 value 0x0020 (Enable Robust Auto MDIX)
Write to PHY register 0x00 value 0x3300 (Enable Auto negotiate and restart process)
Odd-nibble Detection Disable Configuration
Write to PHY register 0x0A value 0x0001 (Disable Odd-nibble detection)
Fast Link-Drop Enable
Write to PHY register 0x0B value 0x0008 (Enable FLD with correct FLD features RX Error count)
```

With the previous write functions, the following register settings can now be read out of both PHYs.

Table 3-1. DP83826 Register Dump in Working EtherCAT® Configuration

MDIO PHY Address 0x01	MDIO PHY Address 0x07
DP83826 register dump[addr:data]	DP83826 register dump[addr:data]
Register 0x0000 : 0x3100	Register 0x0000 : 0x3100
Register 0x0000 : 0x3100	Register 0x0000 : 0x3100
Register 0x0001 : 0x786d	Register 0x0001 : 0x7849
Register 0x0001 : 0x786d	Register 0x0001 : 0x7849
Register 0x0002 : 0x2000	Register 0x0002 : 0x2000
Register 0x0002 : 0x2000	Register 0x0002 : 0x2000
Register 0x0003 : 0xa110	Register 0x0003 : 0xa110
Register 0x0003 : 0xa110	Register 0x0003 : 0xa110
Register 0x0004 : 0x01e1	Register 0x0004 : 0x01e1
Register 0x0004 : 0x01e1	Register 0x0004 : 0x01e1
Register 0x0005 : 0xcde1	Register 0x0005 : 0x0000
Register 0x0005 : 0xcde1	Register 0x0005 : 0x0000
Register 0x0006 : 0x000f	Register 0x0006 : 0x0004
Register 0x0006 : 0x000d	Register 0x0006 : 0x0004
Register 0x0007 : 0x2001	Register 0x0007 : 0x2001
Register 0x0007 : 0x2001	Register 0x0007 : 0x2001
Register 0x0008 : 0x0000	Register 0x0008 : 0x0000
Register 0x0008 : 0x0000	Register 0x0008 : 0x0000
Register 0x0009 : 0x0024	Register 0x0009 : 0x0024
Register 0x0009 : 0x0024	Register 0x0009 : 0x0024
Register 0x000a : 0x0100	Register 0x000a : 0x0100
Register 0x000a : 0x0100	Register 0x000a : 0x0100
Register 0x000b : 0x0000	Register 0x000b : 0x0000
Register 0x000b : 0x0000	Register 0x000b : 0x0000
Register 0x000c : 0x0000	Register 0x000c : 0x0000
Register 0x000c : 0x0000	Register 0x000c : 0x0000

Table 3-1. DP83826 Register Dump in Working EtherCAT® Configuration (continued)

MDIO PHY Address 0x01	MDIO PHY Address 0x07
Register 0x000d : 0x401f	Register 0x000d : 0x401f
Register 0x000d : 0x401f	Register 0x000d : 0x401f
Register 0x000e : 0x0008	Register 0x000e : 0x0008
Register 0x000e : 0x0008	Register 0x000e : 0x0008
Register 0x000f : 0x0000	Register 0x000f : 0x0000
Register 0x000f : 0x0000	Register 0x000f : 0x0000
Extended registers	Extended registers
Extended register 0x0010 : 0x4215	Extended register 0x0010 : 0x0002
Extended register 0x0010 : 0x4615	Extended register 0x0010 : 0x0002
Extended register 0x0011 : 0x010b	Extended register 0x0011 : 0x010b
Extended register 0x0011 : 0x010b	Extended register 0x0011 : 0x010b
Extended register 0x0012 : 0x6400	Extended register 0x0012 : 0x0000
Extended register 0x0012 : 0x0000	Extended register 0x0012 : 0x0000
Extended register 0x0013 : 0x2800	Extended register 0x0013 : 0x0800
Extended register 0x0013 : 0x0000	Extended register 0x0013 : 0x0000
Extended register 0x0014 : 0x0000	Extended register 0x0014 : 0x0000
Extended register 0x0014 : 0x0000	Extended register 0x0014 : 0x0000
Extended register 0x0015 : 0x0000	Extended register 0x0015 : 0x0000
Extended register 0x0015 : 0x0000	Extended register 0x0015 : 0x0000
Extended register 0x0016 : 0x0100	Extended register 0x0016 : 0x0100
Extended register 0x0016 : 0x0100	Extended register 0x0016 : 0x0100
Extended register 0x0017 : 0x0049	Extended register 0x0017 : 0x0041
Extended register 0x0017 : 0x0049	Extended register 0x0017 : 0x0041
Extended register 0x0018 : 0x0480	Extended register 0x0018 : 0x0480
Extended register 0x0018 : 0x0480	Extended register 0x0018 : 0x0480
Extended register 0x0019 : 0x8c21	Extended register 0x0019 : 0x8027
Extended register 0x0019 : 0x8c21	Extended register 0x0019 : 0x8027
Extended register 0x001a : 0x0000	Extended register 0x001a : 0x0000
Extended register 0x001a : 0x0000	Extended register 0x001a : 0x0000
Extended register 0x001b : 0x007d	Extended register 0x001b : 0x007d
Extended register 0x001b : 0x007d	Extended register 0x001b : 0x007d
Extended register 0x001c : 0x05ee	Extended register 0x001c : 0x05ee
Extended register 0x001c : 0x05ee	Extended register 0x001c : 0x05ee
Extended register 0x001d : 0x0000	Extended register 0x001d : 0x0000
Extended register 0x001d : 0x0000	Extended register 0x001d : 0x0000
Extended register 0x001e : 0x0102	Extended register 0x001e : 0x0102
Extended register 0x001e : 0x0102	Extended register 0x001e : 0x0102
Extended register 0x001f : 0x0000	Extended register 0x001f : 0x0000
Extended register 0x001f : 0x0000	Extended register 0x001f : 0x0000
Register dump mode completed.	Register dump mode completed.
Extended register [addr:data] 0x0025:0x0041	Extended register [addr:data] 0x0025:0x0041
Extended register [addr:data] 0x0304:0x0008	Extended register [addr:data] 0x0304:0x0008
Extended register [addr:data] 0x0460:0x0005	Extended register [addr:data] 0x0460:0x0005
Extended register [addr:data] 0x0469:0x0004	Extended register [addr:data] 0x0469:0x0004

3.2 Using Strap Configuration to Set Up DP83826 PHY for EtherCAT® Configuration

The section describing *hardware bootstrap configuration* in the *DP83826 Deterministic, Low-Latency, Low-Power, 10/100 Mbps, Industrial Ethernet PHY* data sheet describes how the device can be configured without using the Serial Management Interface (SMI). This section of the data sheet presents two configuration options: *ENHANCED* mode and *BASIC* mode.

When setting up the PHY to work in an EtherCAT® system, it is important that the PHY has an LED which is set up to show 100 Mbit full duplex and the signal polarity is active low or configurable for some ESCs.

If SMI is not used to program the PHY, the DP83826 must be set up in hardware to support *ENHANCED* function to enable EtherCAT functionality.

To define the LED polarity, the following circuit can be used to make either high or low polarity configuration. The PHY has an internal circuit which measures the polarity that is needed and automatically configures this depending on the input signal. Figure 3-3 shows this internal circuit.

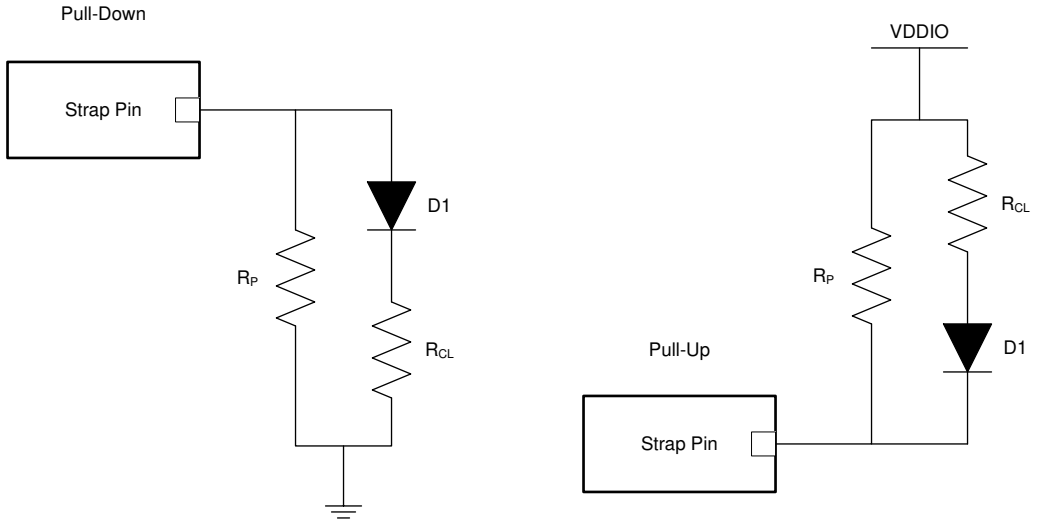

Figure 3-3. Example Strap Connections

In some cases, pending the strap settings this automatic LED feature has been disabled, see the *hardware bootstrap configuration* section of the data sheet for more details.

When setting up the DP83826 device to work in an EtherCAT system without SMI, use the configuration presented in Table 3-2.

Table 3-2. DP83826 Strap Pin Configuration for EtherCAT®

Strap Number | Pin	Enhanced Function	Default	Strap Setting
Strap 0 | pin 16	Auto negotiation disable. Force mode 100 M enabled	0 (Enable)	0(Enable)
Strap 1 | pin 31	Odd Nibble Detection disabled	1 (enable)	0 (Disable) If Strap7 = 1, only RX_Error and Signal Energy detect will be enabled for FLD.
Strap 2 | pin 30	PHY_ADD0	0 (pull down)	Define address with pull up
Strap 3 | pin 29	PHY_ADD1	0 (pull down)	Define address with pull up
Strap 4 | pin 28	PHY_ADD2	0 (pull down)	Define address with pull up
Strap 5 | pin 22	RMII mode	0 (master mode)	0 (master mode) Not needed due to MII mode chosen
Strap 6 | pin 20	Function on Pin 31	0 (CLKOUT 25 MHz)	1 (LED1)

Table 3-2. DP83826 Strap Pin Configuration for EtherCAT® (continued)

Strap Number | Pin	Enhanced Function	Default	Strap Setting
Strap 7 | pin 13	Fast link-drop enable All available mechanisms will be enabled except MLT3_Error.	0 (disable)	1 (Enable) If Strap1 = 0, only RX_Error and Signal Energy detect will be enabled for FLD.
Strap 8 | pin 14	MII MAC mode ALT. Function: When Strap1 =0 AND Strap7 =1, Signal Energy Detect enabled	0 (MII mode)	1 (Signal Energy Detect disabled)
Strap 9 | pin 15	Auto MDIX	0 (enable)	0(enable)
Strap 10 | pin 18	Applicable only when auto-MDIX is disabled Enhanced function	0 (MDIX)	0 (MDIX) Not needed due to auto MDIX enabled
Pin 1		1 (Pull up)	NC(Enhanced mode Enable)

The information in this table shows that fast link down must be enabled in a special way. Only enable Fast link Down using RX Error Count as a detection feature.

4 References

1. Texas Instruments, *DP83826 Low-Power 10/100 Ethernet PHY Data Sheet*
2. Texas Instruments, *KSZ8081 to DP83826E System Rollover Application Report*
3. Beckhoff, *Application Note – PHY Selection Guide*
4. Beckhoff, *Section I – Technology EtherCAT® Protocol, Physical Layer, EtherCAT® Processing Unit, FMMU, SyncManager, SII EEPROM, Distributed Clocks Data Sheet*

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2021) to Revision B (March 2022) **Page**

- Added Section 3.2 based on new data.....9

Changes from Revision * (June 2020) to Revision A (March 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 1
- Globally changed instances of legacy terminology where EtherCAT is mentioned.....1
- Updated bullet baseline wander test in recommendations to Ethernet PHYs section.....7

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