Application Report
SNLA093A–December 2006–Revised April 2013

AN-1565 LXT972M to DP83848C/I/YB PHYTER® System Rollover Document

ABSTRACT

This application report provides information about the process to upgrade an existing 10/100 Mb/s Ethernet design, using Intel's LXT972M Ethernet Physical Layer (PHY) product, our new DP83848C/I/YB PHYTER product.

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1 Purpose

This following points are to be considered when upgrading to the new National Semiconductor DP83848C/I/YB PHYTER product. Both LXT972M and DP83848C/I/YB feature the following:

- Support 10/100 MII interface
- Operation over the commercial temperature range, DP83848I also supports Industrial and DP83848YB supports extended temperature ranges
- Compliant with IEEE 802.3 specification

While both products have many similarities, DP83848C/I/YB offers several features that simplify end user setup to ensure a better user experience. This document compares differences including feature set, pin functions, package and pinout, and possible register operation differences between LXT972M and DP83848C/I/YB. The impact to a design is dependant on features used and their implementation.

2 Required Changes

This section documents the hardware changes required to transition to DP83848C/I/YB. The required changes for proper operation include package, pinout, bias and termination connections.

2.1 Package

LXT972M is only available in the 48 pin LQFP. DP83848C/I/YB is available in a 48 pin LQFP package. The differences in package between DP83848C/I/YB and LXT972M are shown in Table 1. For more information on the DP83848 LQFP package please visit

http://www.national.com/packaging/folders/vbh48a.html.

Table 1. Packaging Differences

	DP83848C/I/YB	LXT972M
Package	48-LQFP	48-LQFP
Footprint	7x7mm	7x7mm
Package Drawing	VBH48A	

2.2 Pinout

Both the LXT972M and the DP83848C/I/YB have 48 pins. Please see Section 5 for the pin mapping between LXT972M and DP83848C/I/YB, as well as pins not applicable in the DP83848C/I/YB.

2.3 PCB Modification

This section describes the LXT972M circuit modifications required to use the DP83848C/I/YB in a similar design.

2.3.1 PFBOUT

Parallel capacitors (10uF Tantalum capacitor and 0.1uF) should be placed close to pin 23 (PFBOUT, the output of the regulator) in DP83848C/I/YB. In DP83848C/I/YB, Pin 18 (PFBIN1) and 37 (PFBIN2) should be externally connected to pin 23 as shown in Figure 1. A small 0.1uF capacitor should be placed close to pin 18 and pin 37. LXT972M does not require a similar connection.

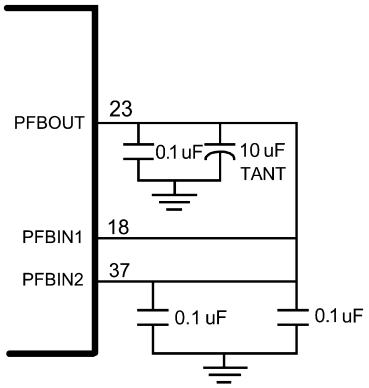

Figure 1. Special Connection in DP83848C/I/YB

2.3.2 Bias Resistor

Internal circuitry biasing between the devices is accomplished in a similar manner. The only difference is the value of the bias resistor and the bias connection pin number.

DP83848C/I/YB used 4.87k Ohm on pin 24

LXT972M uses 22.1k Ohm on pin 17 or 1H

Table 2. Bias Resistor Values

	DP83848C/I/YB	LXT972M
Bias Resistor Value	4.87K Ohm	22.1K Ohm
Bias Pin	24	12

2.3.3 Termination and PMD Biasing

DP83848C/I/YB requires a pair of 49.9 Ohm resistors, biased to VDD of the device. This matching of the termination resistors and common biasing between the receiver and transmitter of the DP83848C/I/YB allows the addition of the Auto-MDIX feature to the device. LXT972M has the 100 Ohm termination integrated in the device. Hence, the receive pair is biased to VDD and does not require external resistors. LXT972M supports Auto-MDIX only through board design.

Table 3. Termination and Biasing Differences

	DP83848C/I/YB	LXT972M
TX Termination	49.9 Ohms	50 Ohms
TX Bias	3.3V	AC to GND
RX Termination	49.9 Ohms	none
RX Bias	3.3V	3.3V

Refer to Figure 2 and Figure 3 for a graphic explanation of this.

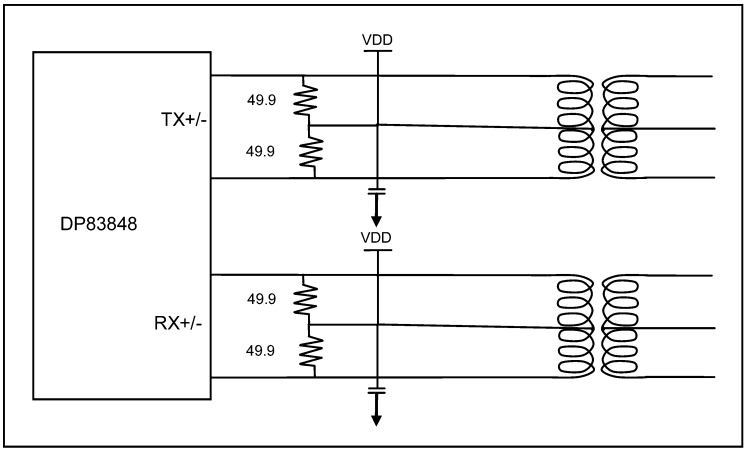

Figure 2. DP83848C/I/YB PMD Connections (Termination)

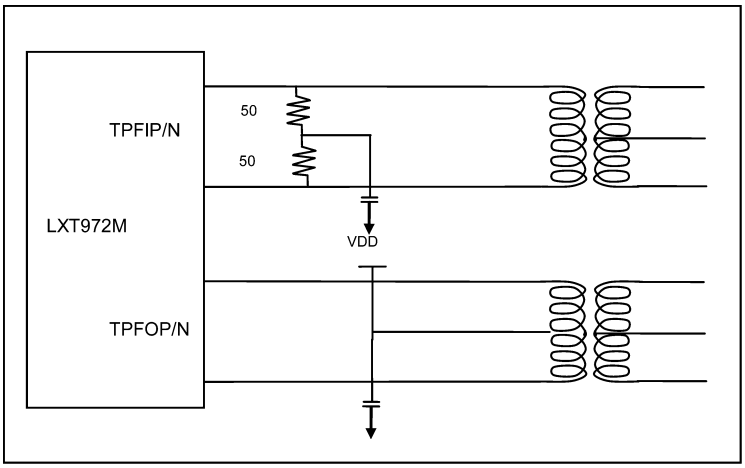

Figure 3. LXT972M PMD Connections (Termination)

3 Potential Changes

The following section describes the specific changes that may need to be changed in converting to a DP83848C/I/YB based design.

3.1 MII Interface

The MII interface is used to connect the PHY to the MAC in 10/100 Mb/s systems. For a 5V MII application, it is recommended to use 33 Ohm series resistor between the MAC and DP83848C/I/YB. The MII interface is a nibble-wide interface consisting of transmit data, receive data and control signals.

The transmit interface is comprised of the following signals:

- Transmit data bus, TXD[0:3] (pins 3,4,5 and 6 in DP83848C/I/YB)
- Transmit enable signal, TX_EN (pin 2 in DP83848C/I/YB)
- Transmit clock, TX_CLK (pin 1 in DP83848C/I/YB) which runs at 2.5MHz in 10 Mb/s mode and 25MHz in 100 Mb/s mode

The receive interface is comprised of the following signals:

- Receive data bus, RXD[0:3] (pin 43,44,45 and 46 in DP83848C/I/YB)
- Receive error signal, RX_ER (pin 41 in DP83848C/I/YB)

- Receive data valid, RX_DV (pin 39 in DP83848C/I/YB)
- Receive clock, RX_CLK (pin 38 in DP83848C/I/YB) for synchronous data transfer which runs at 2.5MHz in 10 Mb/s mode and 25MHz in 100 Mb/s mode

Refer to Section 5 for an LXT972M to DP83848C/I/YB pin mapping.

3.2 PHY Address

In a given system, multiple PHYs may be controlled by a single MII management interface. In order to support this, each PHY must have a unique address. DP83848C/I/YB facilitates this with PHY address strap options.

In DP83848C/I/YB, RXD0:3 and COL are also used at power-up or reset time to set the PHY address. Pin COL has a weak internal pull-up and RXD0:3 have weak internal pull-downs in DP83848C/I/YB. Hence, the default setting for PHY address in DP83848C/I/YB is 01h. To change the PHY address, from the default, add external 2.2K Ohm pull-ups or pull-downs to the appropriate pin(s). LXT971 uses discrete ADDR [0:4] pins to set the device address. However, LXT972M has ADDR[0:1] pins to set the device address. Hence, the device is limited to 4 addresses (00h, 01h, 1Ch, and 1Dh) in the LXT972M.

3.3 Physical Layer ID Register

The PHYsical Layer ID (PHYID) register allows system software to determine applicability of device specific software based on the vendor model number. The vendor model number is represented by bits 9 to 4 in PHYIDR2. The vendor model number in DP83848C/I/YB is 001001b. In LXT972M, the vendor model number is 001110b.

Table 4. Register Change for Vendor Model Number

Register Address	Register Name	Register Description	Device	
Hex			DP83848 C/I/YB	LXT972M
03h	PHYIDR2	PHY ID 2	5C90h	78EXh

3.4 Auto-Negotiation and LED Pins

DP83848C/I/YB has 3 multifunction pins to configure the Auto-Negotiation capabilities. At power-up or reset time they strap the media mode and during normal operation they provide status LED indications. Pin 26 has multiple LED functions, Activity or Collision status, as well as enabling Auto-Negotiation. Pin 28 indicates link status and controls the advertised or forced mode (AN0) of DP83848C/I/YB. Pin 27 indicates speed status and controls the advertised and forced mode (AN1) of DP83848C/I/YB. DP83848C/I/YB does not have separate LED pins to indicate transmit and receive activity status.

In LXT972M, LED/CFG1 pin enables Auto-Negotiation when set. The functions of AN0 and AN1 pins are performed by the LED/CFG2 and LED/CFG3 pins. Each LED can display one of the following status based on the programming of bits 4 to 12 in the LEDCR (014h) register – Speed, Transmit, Receive, Collision, Link, Duplex, Link and Receive status combined, Link and Activity status combined, Duplex and Collision status combined.

Table 5. DP83848C/I/YB Pins for Auto-Negotiation and LED

DP83848C/I/YB Pin Number	Auto-Negotiation Function	LED Function
26	Auto-Negotiation enable	Activity and collision status
27	Controls the advertised and forced mode (AN1)	Speed status
28	Controls the advertised and forced mode (AN0)	Link status

Table 6. DP83848C/I/YB Auto-Negotiation Modes

AN_EN	AN0	AN1	Forced Mode
0	0	0	10 Base-T, Half-Duplex
0	0	1	10 Base-T, Full-Duplex

Table 6. DP83848C/I/YB Auto-Negotiation Modes (continued)

AN_EN	AN0	AN1	Forced Mode
0	1	0	100 Base-TX, Half-Duplex
0	1	1	100 Base-TX, Full-Duplex
AN_EN	**AN0**	**AN1**	**Advertised mode**
1	0	0	10 Base-T, Half/Full-Duplex
1	0	1	100 Base-TX, Half/Full-Duplex
1	1	0	10 Base-T, Half-Duplex
			100 Base-TX, Half-Duplex
1	1	1	10 Base-T, Half/Full-Duplex
			100 Base-TX, Half/Full-Duplex

Table 7. DP83848C/I/YB Auto-Negotiation Modes

LED/CFG1	LED/CFG2	LED/CFG3	Forced Mode
0	0	0	10 Base-T, Half-Duplex
0	0	1	10 Base-T, Full-Duplex
0	1	0	100 Base-TX, Half-Duplex
0	1	1	100 Base-TX, Full-Duplex
LED/CFG1	**LED/CFG2**	**LED/CFG3**	**Advertised Mode**
1	0	0	100 Base-TX, Half-Duplex
1	0	1	100 Base-TX, Full-Duplex
1	1	0	10 Base-T, Half-Duplex
			100 Base-TX, Half-Duplex
1	1	1	10 Base-T, Half/Full-Duplex
			100 Base-TX, Half/Full-Duplex

4 Informational Changes

This section describes new features offered in the DP83848C/I/YB and the changes required to implement them. These features may or may not be offered in LXT972M device.

Table 8. LXT972M Auto-Negotiation Modes

	DP83848C/I/YB	LXT972M
System_Interfaces		
RMII	Yes	No
SNI	Yes	No
JTAG	Available in DP83848I and DP83848YB	Yes
Auto-MDIX	Yes	No
Energy Detect	Yes	No
LED Outputs	3	3
CLK-to-MAC Output	Yes	No
Power Down/Interrupt	Yes	No
Temperature Range		
0_to_70°C	Yes	Yes
-40_to_85°C	Available in DP83848I	No
-40_to_125°C	Available in DP83848YB	No
Power Consumption		
Active Power (Typ)	264mW	300mW

4.1 RMII Interface

The RMII interface (see Figure 4) can be used to connect the MAC to the PHY, in 10/100 Mb/s systems, using a reduced number of pins. By utilizing this feature, significant PCB space savings can be realized within the system, especially a design with a large number of physical layer devices.

DP83848C/I/YB uses an external 50 MHz clock (X1) as reference for both transmit and receive in the RMII mode. The 50 MHz is provided by an external oscillator. To enable RMII mode, RX_DV should be pulled high using a 2.2k Ohm resistor.

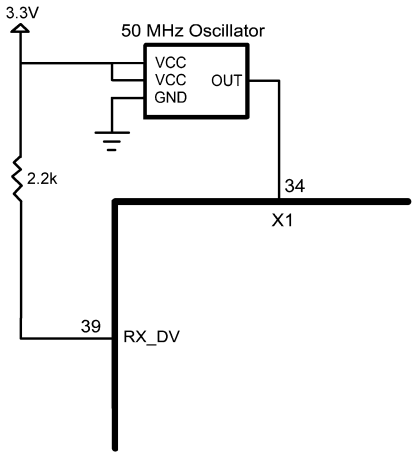

Figure 4. RMII Selection on DP83848C/I/YB

4.2 SNI Mode

DP83848C/I/YB incorporates a 10 Mb/s Serial Network Interface (SNI) which allows a simple data interface for 10 Mb/s only system. While there is no defined standard for this interface, the interface is based on the earlier National Semiconductor's 10 Mb/s physical layer devices. The following pins are used in SNI mode:

- TX_CLK
- TX_EN
- TXD_0
- RX_CLK
- RXD_0
- CRS
- COL

4.3 Auto_MDIX Setting

Auto-MDIX (see Figure 5) removes cabling complications and simplifies end customer applications by allowing either a straight or a cross-over cable to be used without changing the system configuration. Auto-MDIX is enabled by default in the DP83848C/I/YB. To disable Auto-MDIX, pin 41 (RX_ER) should be pulled to ground using a 2.2 K Ohm resistor. When enabled, this function utilizes Auto-Negotiation to determine the proper configuration for transmission and reception of data and subsequently selects the appropriate MDI pair for MDI/MDIX operation.

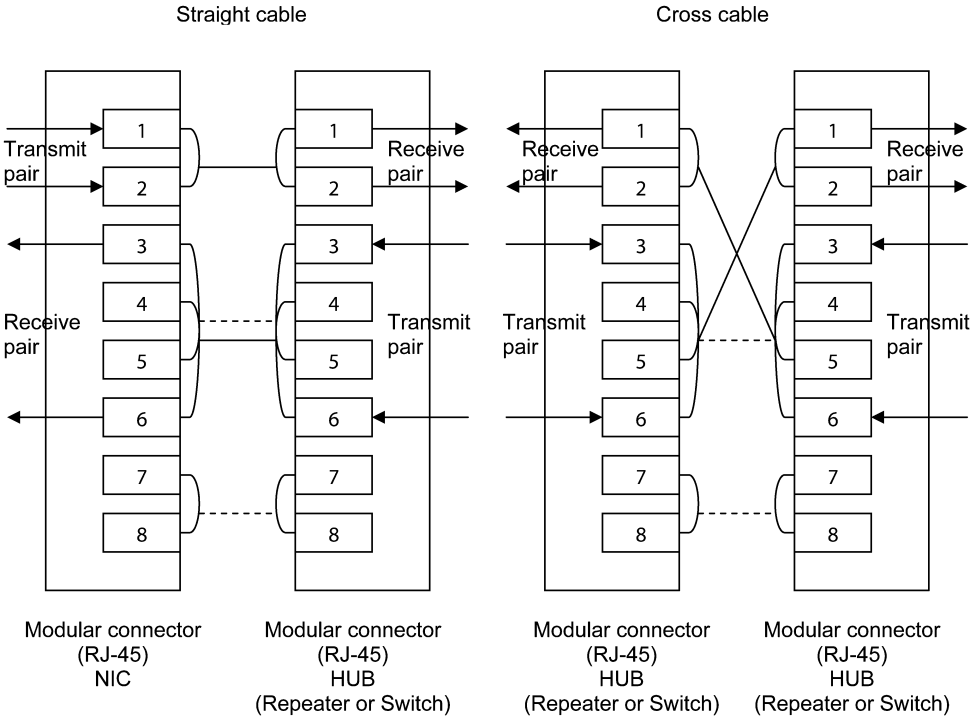

Figure 5. Auto-MDIX Operation

4.4 Energy Detect

Energy Detect facilitates flexible and automatic power management based on detection of a signal on the cable. This enables an application to use an absolute minimum amount of power over time. Energy Detect functionality is controlled via the Energy Detect Control Register (EDCR), address 1Dh. When Energy detect is enabled and there is no activity on the cable, DP83848C/I/YB will remain in a low power mode while monitoring the receive pair in the transmission line. Activity on the line will cause the DP83848C/I/YB to return to the normal power mode.

4.5 CLK_to_MAC Output

DP83848C/I/YB offers a clock output that may be routed directly to the MAC and act as the MAC reference clock, eliminating the need, and hence space and cost, of an additional MAC clock source. In MII mode, the clock output is 25 MHz and in RMII mode, it is 50 MHz clock.

4.6 Power Down / Interrupt

DP83848C/I/YB offers a separate, multifunction pin to allow the system to power down the device, or to indicate an interrupt. In Power_Down mode, the PWR_DOWN/INT pin (pin 7) may be asserted low to put the device in a power down state. In Interrupt mode, this pin is an open drain output and will be asserted low when an interrupt condition occurs, based on various criteria defined by the MISR and MICR registers. It is recommended to use an external pull-up resistor for proper operation of this function.

5 Appendix A

Table 9. DP83848C/I/YB & LXT972M Pin Map

DP83848C/I/YB Signal Name	DP83848C/I/YB Pin #	LXT972M Pin #	Description
MII Interface Pins			
MDC	31	32	MGMT DATA CLOCK
MDIO	30	31	MGMT DATA I/O
RXD0:3/PHYAD1:4	43,44,45,46	36,35,34,33	MII RX DATA
RX_CLK	38	40	MII RX CLOCK
RX_ER/MDIX_EN	41	41	MII RX ERROR
RX_DV/MII_MODE	39	37	MII RX DATA VALID
TXD0:3	3,4,5,6	44,45,46,47	MII TX DATA
TX_CLK	1	42	MII TX CLOCK
TX_EN	2	43	MII TX ENABLE
TX_ER	n/a	n/a	MII TX ERROR
COL/PHYAD0	42	48	MII COL DETECT
CRS/LED_CFG	40	1	MII CARRIER SENSE
PMD Interface Pins			
RD-/+	13,14	14,15	RX DATA
TD-/+	16,17	17,18	TX DATA
Clock Interface Pins			
X1	34	2	XTAL/OSC INPUT
X2	33	3	XTAL OUTPUT
LED Interface Pins			
LED_ACT/COL/AN_EN	26	26,27,28	COL LED STATUS
LED_ACT/COL/AN_EN	26	26,27,28	DUPLEX LED STATUS
LED_LINK/AN_0	28	26,27,28	LINK LED STATUS
LED_SPEED/AN_1	27	26,27,28	SPEED LED STATUS
LED_ACT/COL/AN_EN	26	26,27,28	ACT LED STATUS
LED_RX/PHYAD4	n/a	26,27,28	RX ACTIVITY LED
LED_TX/PHYAD3	n/a	26,27,28	TX ACTIVITY LED
JTAG Interface Pins			
TCK (1)	8	22	TEST CLOCK
TDO (1)	9	20	TEST DATA OUTPUT
TMS (1)	10	21	TEST MODE SELECT
TRST (1)	11	23	TEST RESET
TDI (1)	12	19	TEST DATA INPUT
Reset Function Pin			
RESET_N	29	4	RESET
Strap Pins			
PHYAD0:4	42,43,44,45,46	10,11	PHY ADDRESS
MDIX_EN/RX_ER	41	n/a	AUTO MDIX ENABLE
MII_MODE/RX_DV	39	n/a	MII MODE SELECT
SNI_MODE/TXD3	6	n/a	MII MODE SELECT
LED_CFG/CRS	40	26,27,28	LED CONFIGURATION
PAUSE_EN/RX_ER	n/a	n/a	PAUSE ENABLE
Bias Function Pins			
RBIAS	24	12	BIAS RES CONNECTION
Test Mode Pins			

(1) n/a for DP83848C.

Table 9. DP83848C/I/YB & LXT972M Pin Map (continued)

DP83848C/I/YB Signal Name	DP83848C/I/YB Pin #	LXT972M Pin #	Description
AN_0/LED_LINK	28	26	TEST MODE SELECT
AN_1/LED_SPEED	27	27	TEST MODE SELECT
AN_EN/LED_ACT/COL	26	28	TEST MODE SELECT
Special Function Pins			
25MHz_OUT	25	n/a	25 MHz CLOCK OUTPUT
PWR_DOWN/INT	7	n/a	POWER DOWN/INT
PFBIN1:2	18,37	n/a	POWER FEEDBACK IN
PFBOUT	23	n/a	POWER FEEDBACK OUT
Supply Pins			
VDD	22,32,48	6,16,29,39	3.3V
GND	15,19,35,36,47	5,9,13,24,25,30	GROUND
Reserved Pins			
RESERVED	8,9,10,11,12,20	7,8,37,38	RES

6 Appendix B

This section covers differences between the registers in DP83848C/I/YB and LXT972M applicable to software configuration of these devices.

Register Differences

IEEE specified registers of National Semiconductor Physical Layer devices comply with the respective IEEE standards. Only vendor specific registers have functions that may vary from device to device. If no vendor specific registers are modified for operation in the system application, the devices will have similar operation. In designs that modify any of these optional registers, the system may use the PHY_ID register, offset 03h, to detect which device is being used and make the appropriate changes to device registers. Specific functions of these vendor defined registers, may be available in another register or possibly in a different bit within the same register location.

Table 10. Register Bit Definitions

Reg Addr	Reg Name	Register Description	Device	
Hex			**DP83848C/I/YB**	**LXT972M**
00h	BMCR	Basic Mode Control	Bit 6 Res	Bit 6 Speed Selection
01h	BMSR	Basic Mode Status	Bits 10:8 Res	Bit 10 100Base-T2 Full Dup
				Bit 9 100Base-T2 Half Dup
				Bit 8 Extended Status
02h	PHYIDR1	PHY ID 1	2000h	0013h
03h	PHYIDR2	PHY ID 2	5C90h	78EXh
05h	ANLPAR	Auto-Neg Link Partner Ability	Bit 13 Message page	Bit 13 RF
			Bit 12 Acknowledge	Bit 12 Reserved
			Bit 11 Toggle	Bit 11 Asymmetric Pause
			Bit 10:0 NP transmission code	Bit 10 Pause
				Bit 9 100Base-T4
				Bit 8 100Base-TX Full Dup
				Bit 7 100Base-TX
				Bit 6 10 Base-T Full Dup
				Bit 5 10Base-T
				Bit 4:0 Selector field
06h	ANER	Auto-Neg Expansion	Bit 5 Res	Bit 5 Base Page

Table 10. Register Bit Definitions (continued)

Reg Addr	Reg Name	Register Description	Device	
Hex			DP83848C/I/YB	LXT972M
08h	ANLPNPR	Auto-Neg Link Partner Next Page Receive	Res	See LXT972M datasheet
10h : 1D		Function differs	(See datasheet)	(See datasheet)

For additional information on these devices, please refer to the applicable datasheet(s).

DP83848C PHYTER Commercial Temperature Single Port 10/100 Mb/s Ethernet Physical (SNOSAT2)

DP83848I PHYTER Industrial Temperature Single Port 10/100 Mb/s Ethernet Physical (SNLS207)

DP83848YB Extreme Temp Single Port 10/100 Mb/s Ethernet Phy Layer Transceiver (SNLS208)

LXT972M App Note 1565 LXT972M to DP83848C/I/YB PHYTER Sys Rollovr Doc (SNLA093)

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