Application Report
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How to Configure DP83867 SFDs

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ABSTRACT

The DP83867 can detect a Start of Frame Delimiter (SFD) for transmit and receive packets and output a pulse via a GPIO that can be used to assess the latency of the link between the DP83867 and a timestamp capable partner. For real-time systems and systems implementing the IEEE 1588 Precision Time Protocol (PTP) to timestamp packets for synchronizing devices across the network, the SFD output provides a more stable, repeatable timestamp reference when compared to measurements made at the xGMII interface. This application note provides a brief introduction to Start of Frame Delimiters as they relate to Ethernet packets and describes the necessary configuration required to implement SFDs in an Ethernet system.

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1 Synchronization in an Ethernet Application

Synchronization of devices in an Ethernet network is important for real-time systems and systems that implement the IEEE 1588 Precision Time Protocol. A common element in these systems is that packets are timestamped and these timestamps are then used to synchronize the time across the network. Sharing the time throughout the system and synchronizing the devices on the network to a common time is protocol dependent and is typically handled in the upper layers above the Ethernet Physical Layer device (commonly referred to as a PHY).

Packets can be timestamped in either hardware or in software depending on the accuracy required for the application. Every component that handles the packets can increase the error of the timestamp by adding non-deterministic latency.

Timestamping in the Ethernet MAC is a straightforward implementation, but is subject to multiple sources of variation. Timestamping within the Ethernet PHY provides better accuracy, but is a more complex implementation. Generating an SFD pulse prior to the MAC interface and timestamping the pulse offers good accuracy with moderate complexity.

2 Latency in an Ethernet PHY

For an Ethernet PHY, latency is the time required for a packet to traverse the PHY from the MAC interface to the media dependent interface (most often an Ethernet cable) or from the media dependent interface to the MAC interface. Latency through the PHY is an important aspect of the end to end latency of the system and is therefore a key attribute related to synchronization.

Latency is an important characteristic of real-time systems. Long latencies and variation in the latency can affect system performance.

Consider a system implemented in a ring topology. Each node in the ring might consist of two Ethernet PHYs. A packet will enter the node through one PHY and exit through the other PHY. The latency through each PHY will determine the amount of time required for a packet to traverse the full ring. A PHY with lower latency will allow a packet to traverse the ring more quickly or will support more nodes in the ring.

In addition to low latency, the repeatability of the latency is important. Variation in the latency from one packet to another packet will reduce the precision of the system. Start of Frame Detection within the PHY is one way to address this variation.

3 Start of Frame Detection

To understand the detection of the Start of Frame Delimiter in an Ethernet PHY, it is helpful to have a basic knowledge of the structure of an Ethernet frame.

An IEEE 802.3 Ethernet frame begins with a MAC destination address, a MAC source address, and a type/length field, followed by data. The Ethernet frame is preceded by preamble and a Start of Frame Delimiter (SFD). In hexadecimal format, preamble consists of octets of 0x55. The SFD consists of an octet of 0x5D. The SFD is commonly used as an identifier for the start of the packet and is therefore commonly used for timestamping the packet.

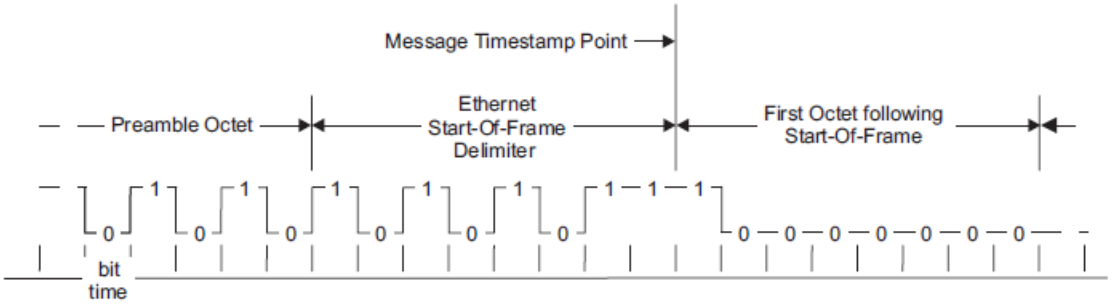

Figure 1. Ethernet SFD Timestamp Point

4 Start of Frame Detection in the DP83867

The DP83867 can be configured to output transmit and receive SFDs on a GPIO via MDIO register access.

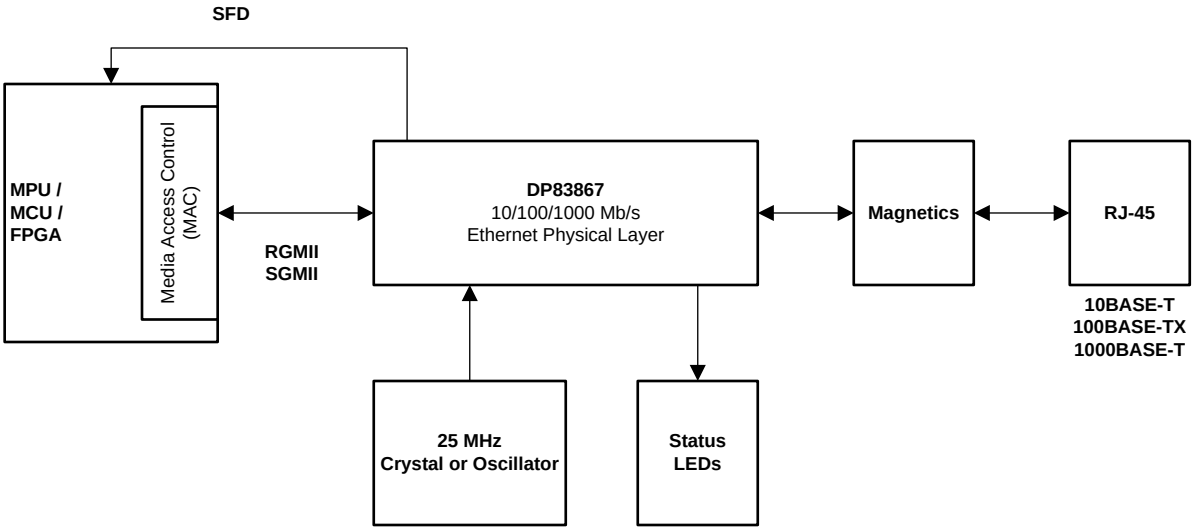

Figure 2. DP83867 SFD Connection Diagram

Configuration of SFDs requires four steps:

1. Enable enhanced receive features. Set bit 7 of the RXFCFG register, (Address 0x0134), to 0x1. This is the ENHANCED_MAC_SUPPORT register bit.
2. Select the desired output pins for the 1588 SFDs using the GPIO Mux Control Registers:
   - For DP83867IRPAP: GPIO_MUX_CTRL1 (Address 0x0171) and GPIO_MUX_CTRL2 (address 0x0172)
   - For DP83867CSRGZ, DP83867ISRGZ, DP83867ERGZ: GPIO_MUX_CTRL (Address 0x0172)
3. Set the internal SFD configuration. Write 0xDF22 to register 0x00E9.
4. Apply a software restart to refresh the registers.

Note that application of a hardware or software reset will cause the registers to lose their configuration.

Below is a step by step example for configuring a transmit SFD and a receive SFD:

1. Enable enhanced receive features by writing 0x1080 to register 0x0134.
2. Configure the device to output the SFDs by writing 0x0120 to register 0x0172.
   - For the DP83867IRPAP, this will configure the transmit SFD on the CRS pin and the receive SFD on the COL pin.
   - For the DP83867CSRGZ, DP83867ISRGZ, DP83867ERGZ, this will configure the transmit SFD on the GPIO_1 pin and the receive SFD on the GPIO_0 pin.
3. Set the internal SFD configuration by writing 0xDF22 to register 0x00E9.
4. Apply a software restart by writing 0x4000 to register 0x001F.

When configured, the SFD will assert on the GPIO pin when the Start of Frame Delimiter is identified in the packet. The SFD will remain asserted until the end of the packet.

5 Comparison of SFD versus MAC Interface Signal

Since the MAC and PHY may have independent clock sources, a clock domain crossing may occur at the MAC interface. Synchronization of signals across this clock domain crossing is one source of variability in the timestamp and highlights one of the benefits of timestamping the SFD via a PHY output. The diagram below shows a comparison of the RGMII RX_CTRL signal and the RX SFD for the DP83867.

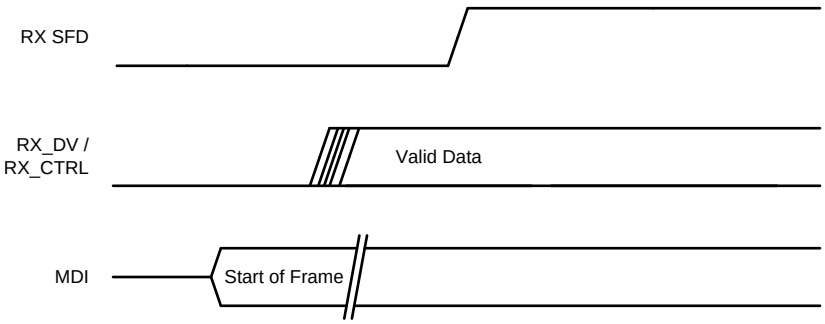

Figure 3. Comparison of RX_CTRL vs. RX SFD

The variation in the rising edge of the RX_CTRL signal would result in changes in the timestamp. By contrast, the repeatable rising edge of the RX SFD would provide a more stable, repeatable timestamp point.

Note that this variation can exist in both the transmit and the receive direction. A similar improvement in repeatability can also be made with the TX SFD in the transmit direction.

6 SFD Measurement Results

The end to end latency of a link can be measured by the delay from the transmit SFD on one device to the receive SFD of a second device. For real-time systems and systems implementing the IEEE 1588 Precision Time Protocol, this measurement could be made by comparing the timestamps of the two SFDs.

Start of Frame was measured using the configuration previously described in Section 4. The test setup consisted of two DP83867 boards connected via a 1m cable. Transmit data was provided to the Device under Test (DUT). Data received by the link partner was looped back to the link partner transmit pins via a wiring harness. In this way, all four SFDs could be measured relative to one another.

In the test setup, the end to end latencies were measured using an oscilloscope. The latency measurements were calculated as:

- DUT TX SFD to Partner RX SFD (shown as C1->C4 in the oscilloscope shots below)
- Partner TX SFD to DUT RX SFD (shown as C3->C2 in the oscilloscope shots below)

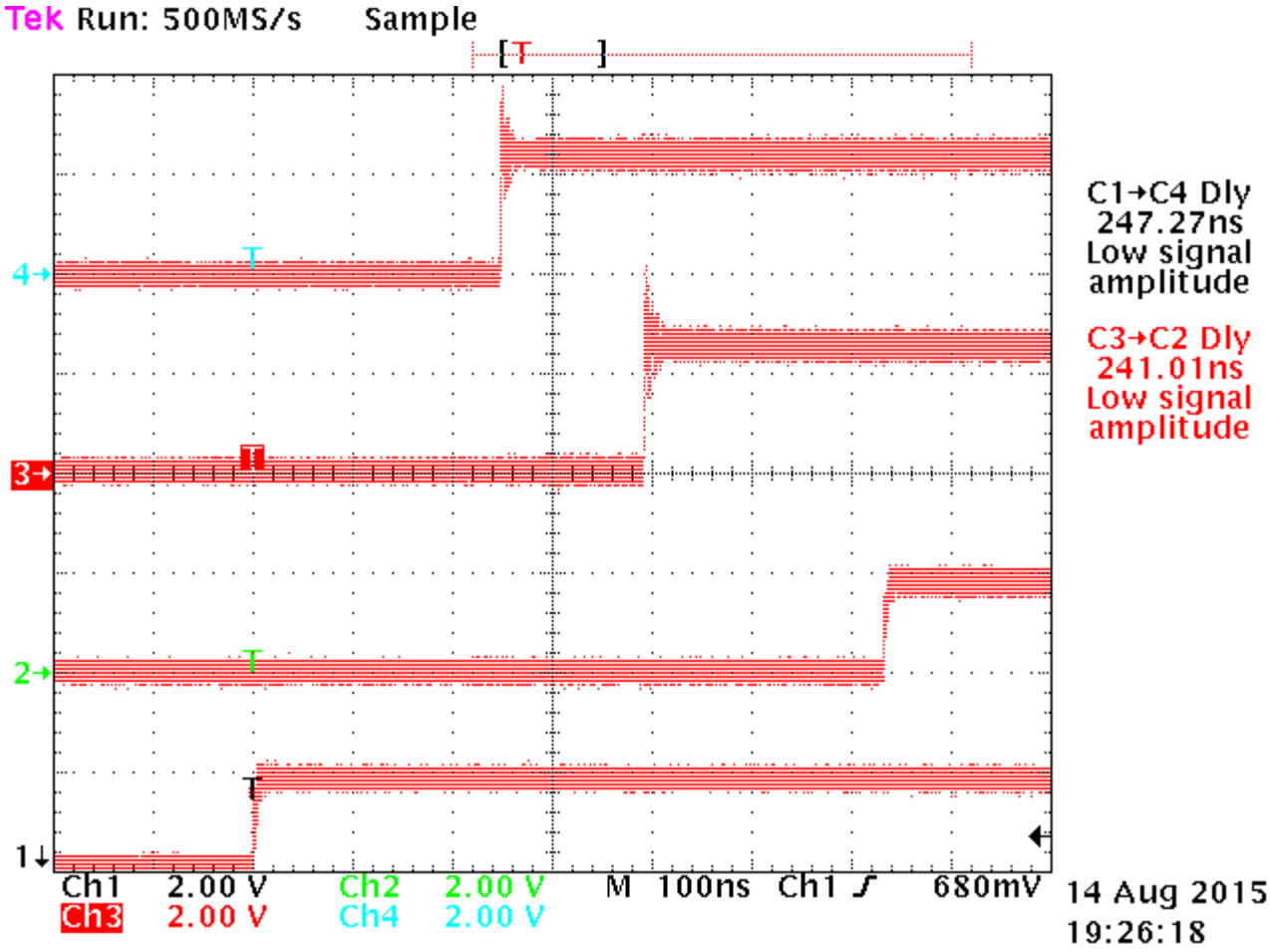

Figure 4. Start of Frame Measurement

Ch1: DUT TX SFD
Ch2: DUT RX SFD
Ch3: Partner TX SFD
Ch4: Partner RX SFD

Data taken for 100 consecutive links with oscilloscope configured for infinite persistence. Variation in the repeatability of the SFDs would be indicated by multiple edges on the rising edges of the SFD pulses. Note that there is no variation for the SFDs see Figure 4.

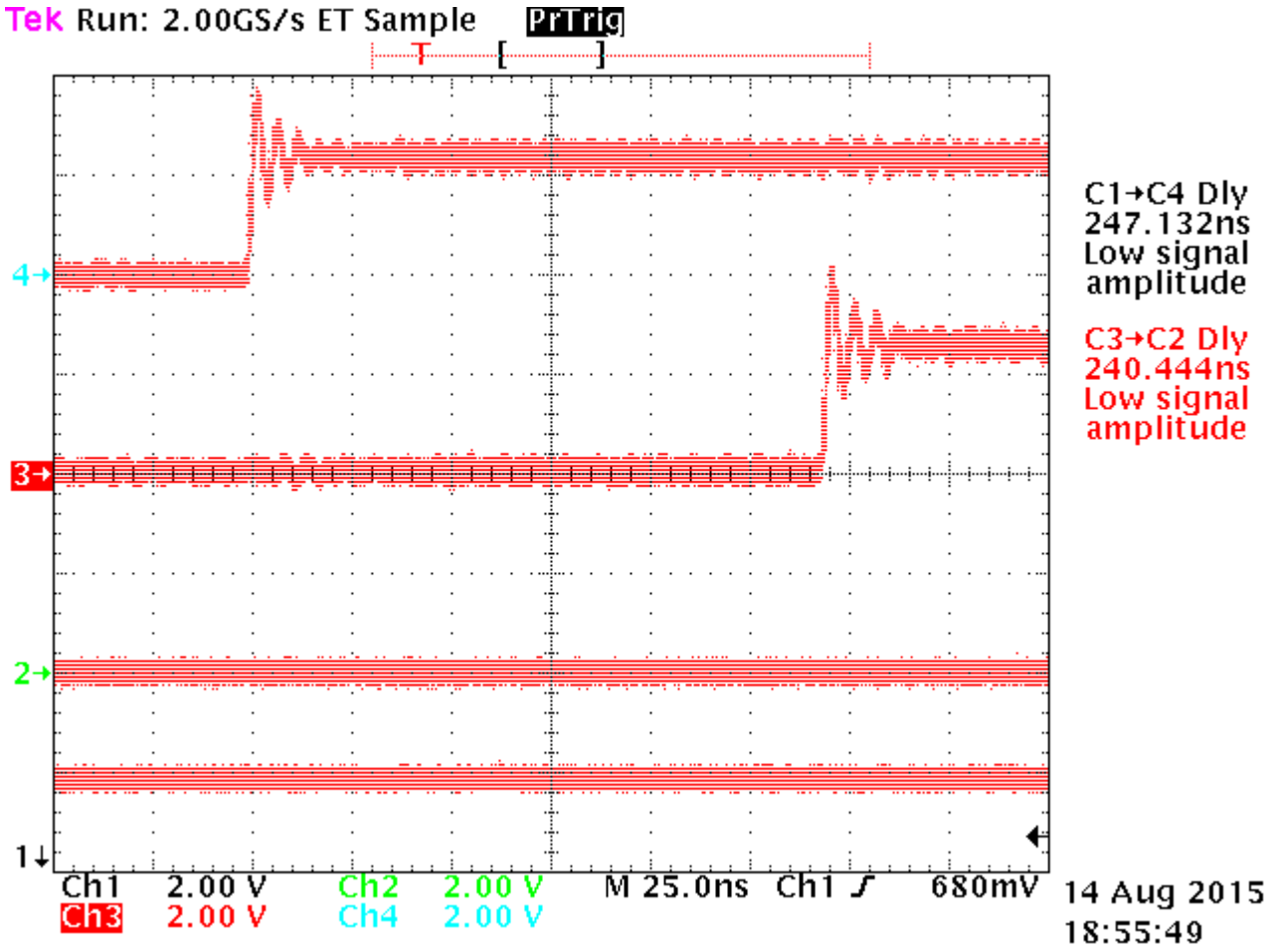

Figure 5. Start of Frame Measurement (Zoom)

The transmit and receive SFDs for the link partner are shown at higher oscilloscope resolution to confirm that there is no variation see Figure 5.

7 Conclusions

This application note provides details on how to configure the DP83867 to generate pulses upon transmission and reception of Start of Frame Delimiters (SFDs). These SFDs provide a reliable and repeatable indication of the start of the Ethernet packet and can be used for timestamping at the system level.

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