

DP83867 Troubleshooting Guide

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ABSTRACT

A 10/100/1000 Ethernet Physical Layer device has multiple connections and many possible configuration options. While the DP83867 is designed with a priority on ease of use, there are many factors to consider during initial board bring up. This application note provides guidance on the key criteria to verify in order to expedite initial validation of DP83867 applications.

The goal of this application note is to describe a flow to identify the most likely source of problems during board bring up. For a quick start guide, please see the Troubleshooting Checklist in [Section 3](#) at the end of this application note.

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1 DP83867 Application Overview

The DP83867 is a robust, low power, fully featured Physical Layer transceiver with integrated PMD sublayers to support the 10BASE-Te, 100BASE-TX, and 1000BASE-T Ethernet protocols.

Figure 1 is a high-level system block diagram of a typical DP83867 application.

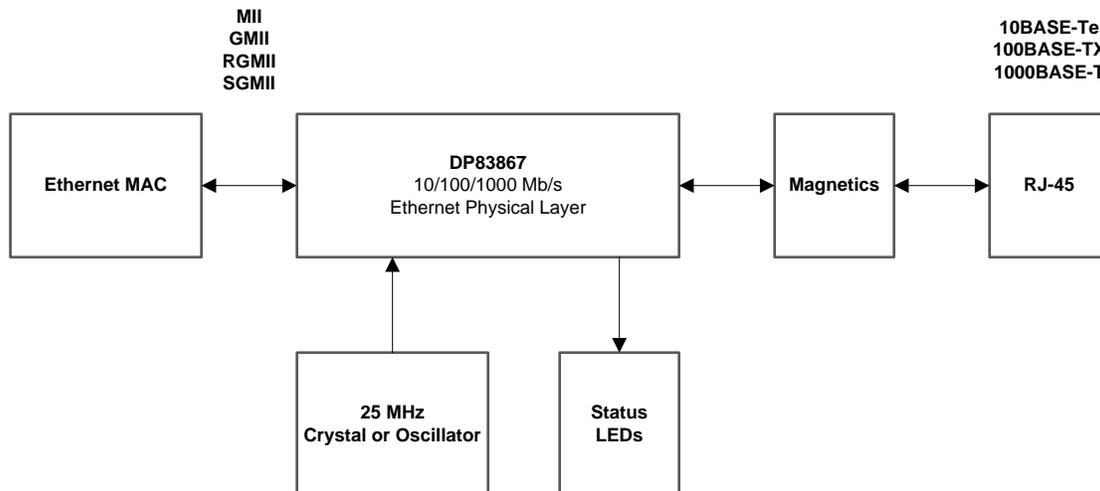


Figure 1. DP83867 Block Diagram

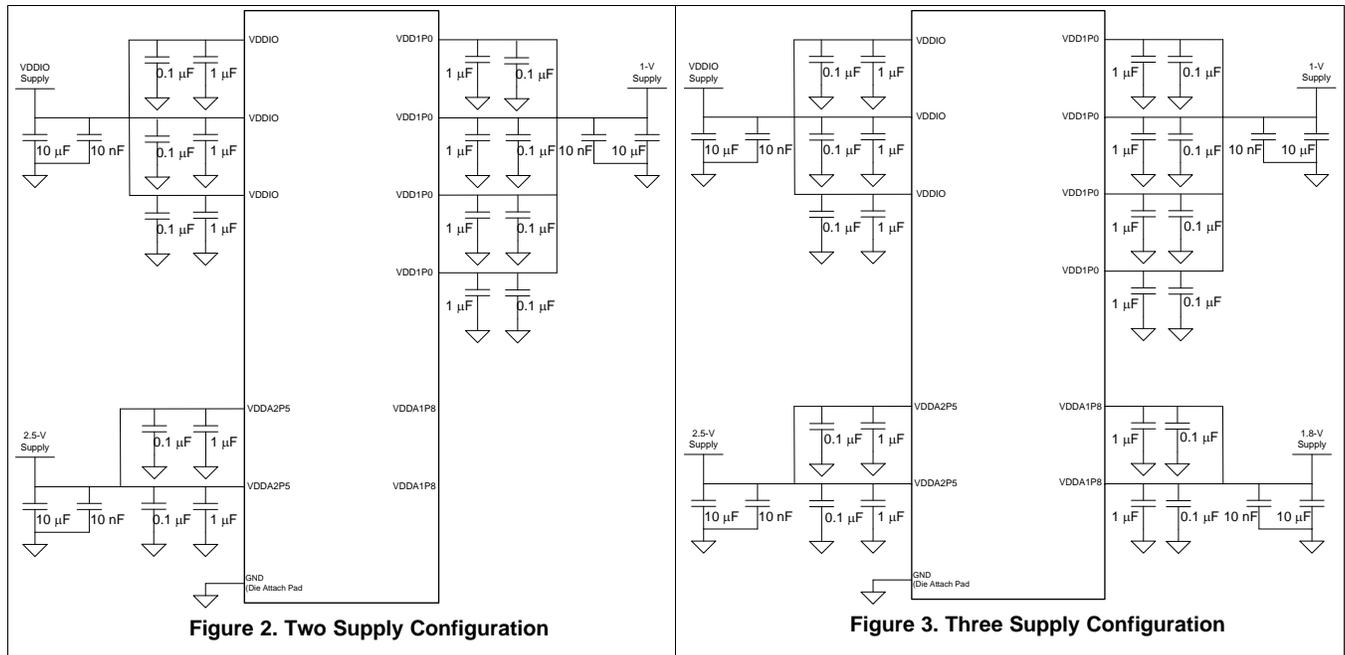
The DP83867 will connect to an Ethernet MAC and to a media. The connection to the media is via a transformer and a connector.

2 Troubleshooting the Application

The following sections approach the debug from a high level, attempting to start with application characteristics that have a broad impact and then zeroing in on more focused aspects of the design.

2.1 Power Supplies

The power supplies are the first key item to check. Power up the device and perform DC measurement of the supplies as close to the pin as possible. Confirm that each measurement is within the limits defined in the *Recommended Operating Conditions* section of the datasheet.



The DP83867 supports two configurations for power supplies as shown in [Figure 2](#) and [Figure 3](#) above. It can operate with as few as two supplies. When operating in the three supply configuration, the VDDA1P8 supply must be stable within 25ms of the VDDA2P5 supply ramping up. There is no sequencing requirement for other supplies when operating in three supply mode. When powering down the DP83867, the VDDA1P8 supply should be brought down before the VDDA2P5 supply. Power up the board and verify the sequence of these supplies with an oscilloscope.

2.2 RBIAS Voltage and Resistance

The RBIAS resistor is used to develop the internal bias currents and voltages in the PHY. It is specified for 1% tolerance so that the PHY can meet the tightest IEEE 802.3 specifications.

Measure the DC value of the voltage across the RBIAS resistor and confirm that the voltage is 1 V.

Power down the board and verify that the RBIAS resistor value is 11 kΩ ±1%.

2.3 Line Driver

The transmit circuitry that connects to the Media Dependent Interface is commonly referred to as the line driver. The connections and components associated with the line driver depend on the line driver architecture. The DP83867 implements a voltage mode line driver. Therefore, the required connections are very straightforward.

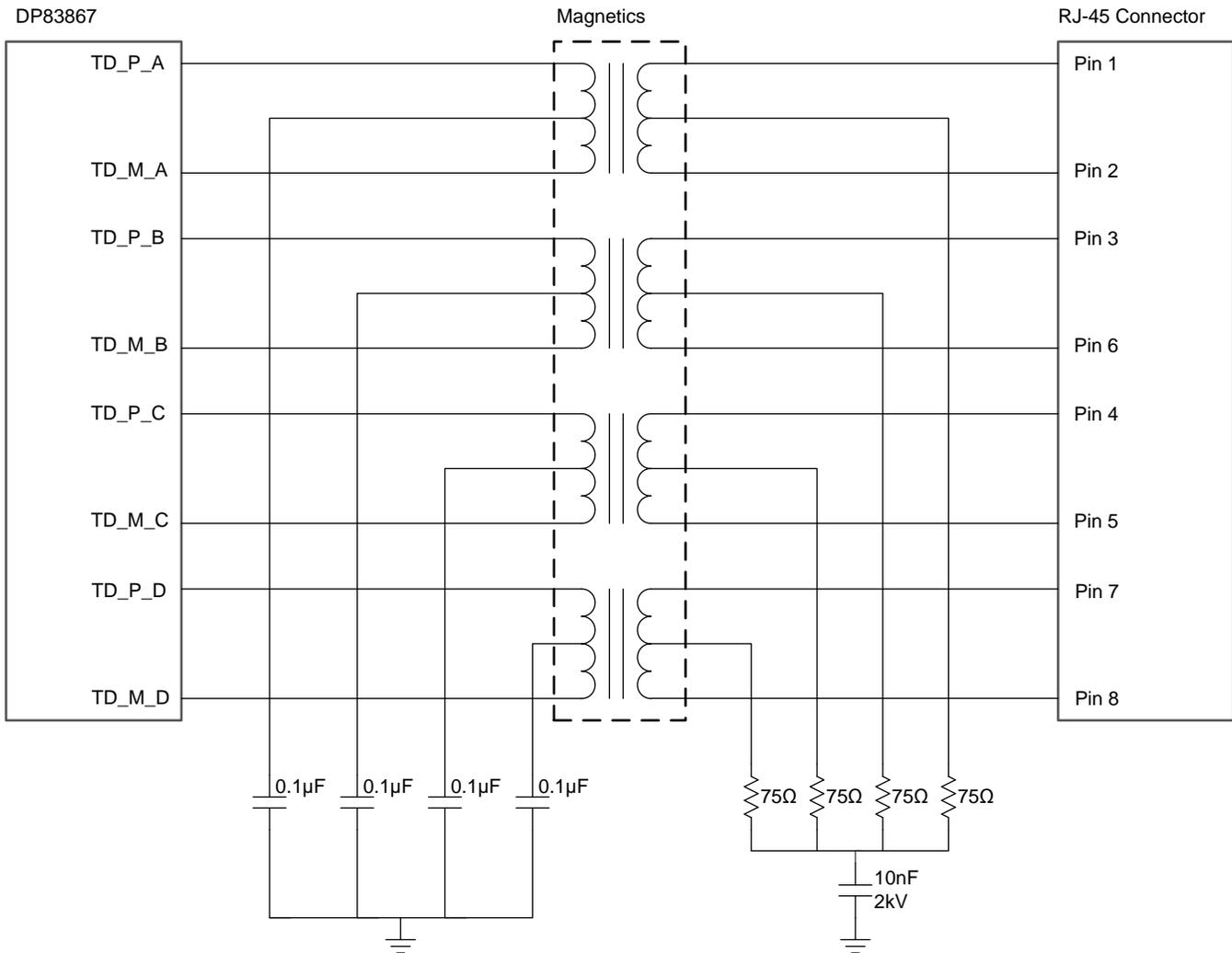


Figure 4. DP83867 MDI Connections

Each center tap of the magnetics should be independently de-coupled to ground via a 0.1µF capacitor. Connecting the magnetics center taps to a supply voltage is not necessary. Due to the voltage mode driver architecture, no current is drawn from the magnetics by the PHY.

No external termination resistors are necessary. Terminations are integrated into the DP83867.

2.4 Verify Key Signals

Power up the board and verify the following key signals.

2.4.1 Probe the RESET_N Signal

The reset input is active low. It is important to confirm that the controller is not driving the RESET_N signal low. Otherwise, the device will be held in reset and will not respond.

2.4.2 Probe the XI Clock

Verify the frequency and signal integrity. For link integrity the clock must be 25 MHz \pm 50 ppm.

If using a crystal as the clock source, probe the CLK_OUT signal. Probing the crystal can change the capacitive loading and therefore change the operational frequency. The default signal on CLK_OUT is a buffered version of the XI reference and will provide a representative measurement.

2.4.3 Probe the Strap Pins During Initialization

In some cases, other devices on the board (for example, the MAC) will pull or drive these pins unexpectedly. Confirm that these signals are in the range of the target voltages described in the datasheet. Measurements can be made during power up and after power up when the RESET_N signal is asserted.

For further confirmation, the strap values can be read from the registers. The values are available in register 0x006E (STRAP_STS1) and register 0x006F (STRAP_STS2).

2.4.4 Probe the Serial Management Interface Signals (MDC, MDIO)

MDIO should pull up to the I/O supply when undriven. Probe MDIO to confirm the default voltage.

Attempt to read the registers. Verify the MDIO data sequence with the datasheet to make sure the MDIO read access timing is correct

2.5 Probe the MDI Signals

In the default configuration, Auto-negotiation and Auto-MDIX will be enabled. A link pulse should be visible on the channel A and channel B transmit and receive differential pairs (TD_P_A, TD_M_A, TD_P_B, TD_M_B).

A short Ethernet cable with 100 Ohm terminations can be used for measuring the MDI signals. A terminated cable is shown in Figure 5. A connection diagram for making measurements with the terminated cable is shown in Figure 6.

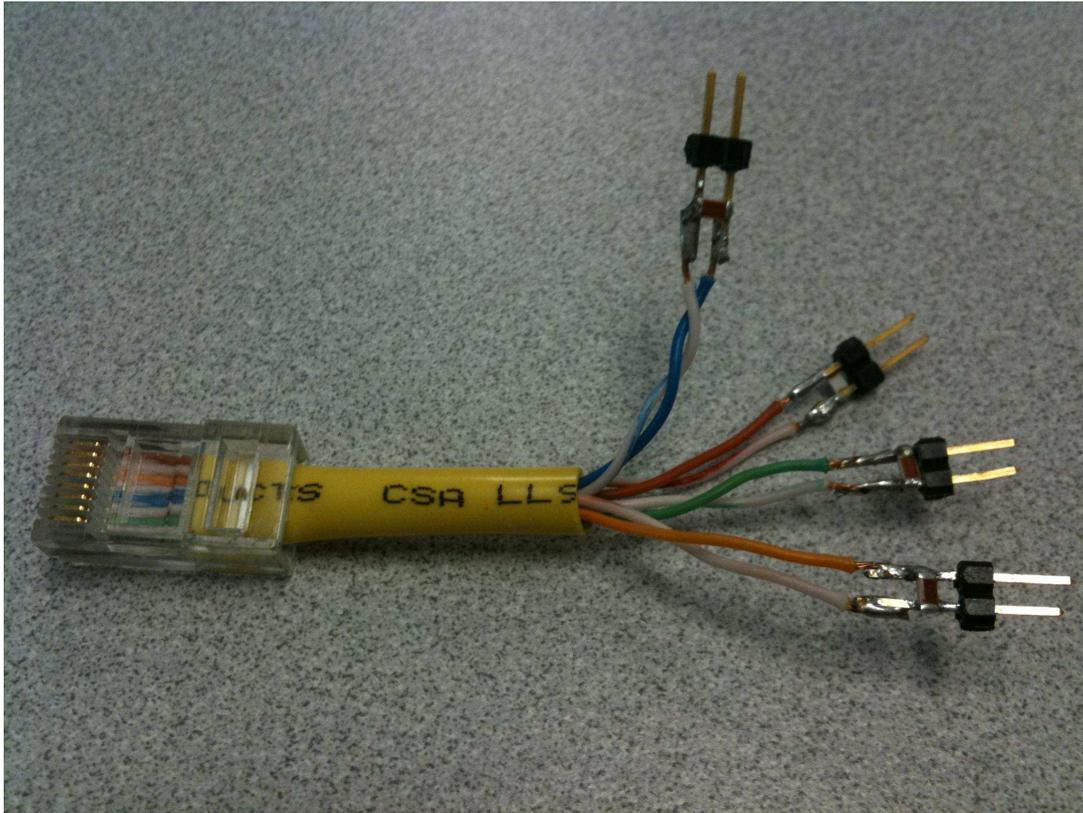


Figure 5. 100 Ohm Terminated Cable for MDI Signal Measurement

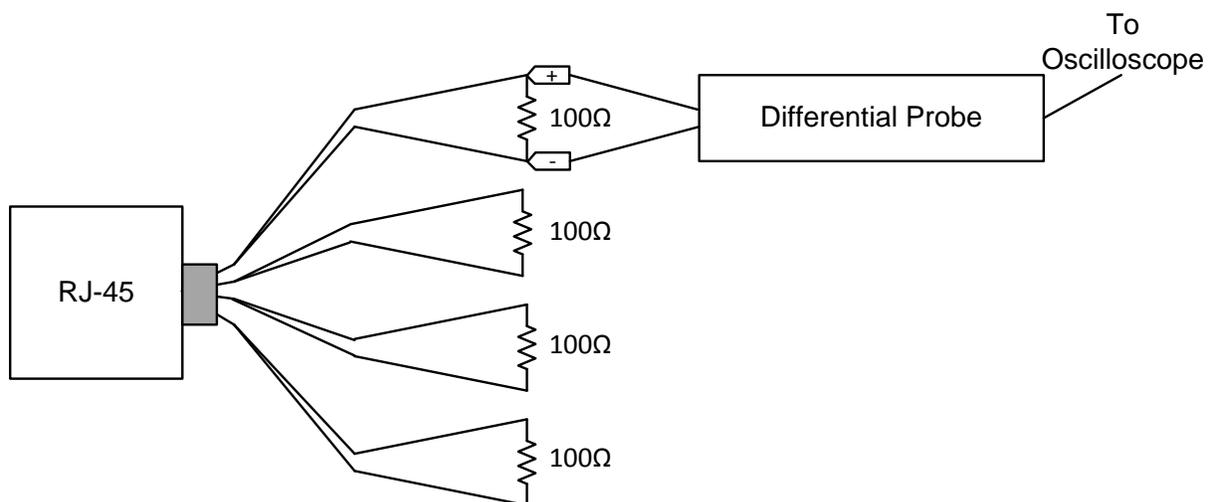


Figure 6. Connection Diagram for 100M Terminated Cable

Auto-Negotiation link pulses are nominally 100ns wide. Pulses are spaced by 62µs or 125µs and are transmitted in bursts. The bursts are nominally 2ms in duration and occur every 16ms. An example link pulse is shown below in [Figure 7](#)

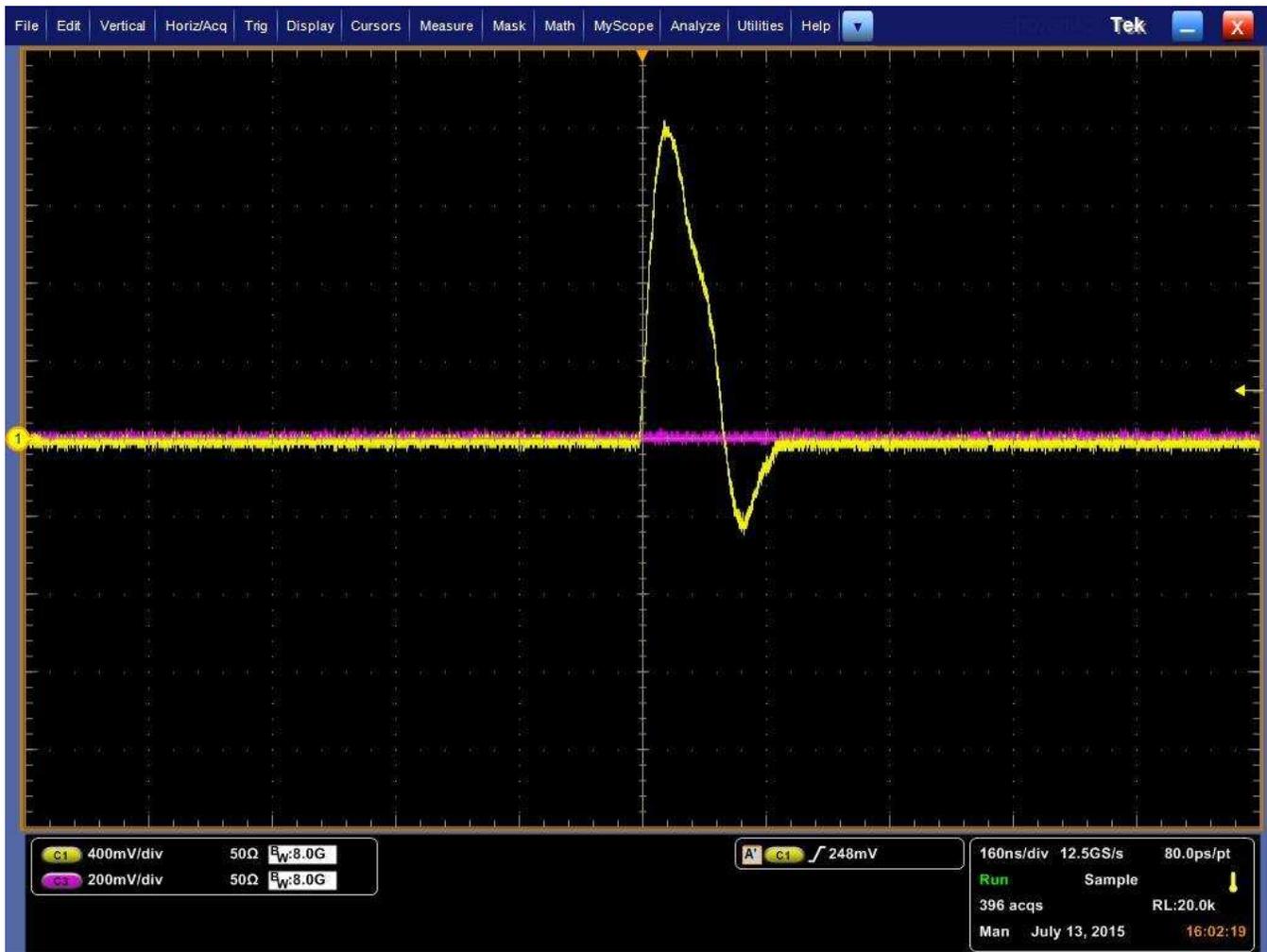


Figure 7. DP83867 Link Pulse

2.6 Read the Registers

Read the registers and verify the default values shown in the datasheet. Note that the initial values of some registers can vary based on strap options.

Some key configuration and status registers are:

- Basic Mode Control Register (BMCR), Address 0x0000
- Basic Mode Status Register (BMSR), Address 0x0001
- Auto-Negotiation Advertisement Register (ANAR), Address 0x0004
- Auto-Negotiation Link Partner Ability Register (ANLPAR), Address 0x0005
- Status Register 1 (STS1) Address 0x000A
- PHY Control Register (PHYCR), Address 0x0010
- PHY Status Register (PHYSTS), Address 0x0011

2.6.1 DP83867 Register Access

If register access is not readily available in the application, USB-2-MDIO GUI is available from TI and can be used with an MSP430 Launchpad, purchasable through the TI eStore (<https://store.ti.com/>). The GUI supports reading and writing registers as well as running script files. It can be used with the DP83867 and the other devices in TI's Ethernet portfolio. The USB-2-MDIO User's Guide and GUI are available for download at: <http://www.ti.com/tool/usb-2-mdio>



Figure 8. USB-2-MDIO GUI

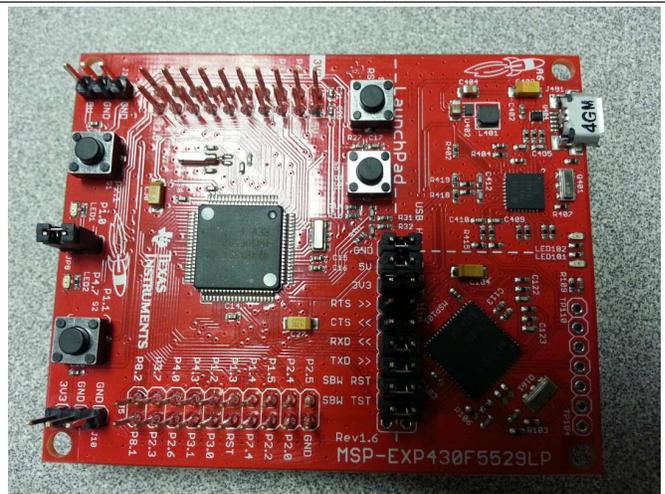


Figure 9. MSP430 LaunchPad

Below is an example script that can also be found in the USB-2-MDIO GUI in the Help menu:

```
// This is how you make a comment. All scripts must start with 'begin'
begin

// To read a register, all you need to do is put down the 4 digit
// HEX value of the registers (from 0000 to FFFF)
// Example to read registers 0001, 000A, and 0017
0001
000A
0017

// To write a register, all you need to do is put down the 4 digit
// HEX value of the register (from 0000 to FFFF) followed by the
// HEX you desire to configure the register to (from 0000 to FFFF)
// Example to write 2100 to register 0000 and
// Example to write 0110 to register 0016
0000 2100
0016 0110

// You must end the script by adding 'end' once you are finished
end
```

The Serial Management Interface defined by IEEE 802.3 is a single master bus. The MDC clock is generated by the bus master, typically an Ethernet MAC. To use the USB-2-MDIO GUI, connections must be made directly between the MSP430 Launchpad and the DP83867 MDIO and MDC pins.

2.7 Built-in Self Test

The device incorporates an internal PRBS Built-in Self Test (BIST) circuit to accommodate in-circuit testing or diagnostics. The BIST circuit can be used to test the integrity of the transmit and receive data paths. BIST can be performed using both internal loopback (digital or analog) or external loopback using a cable fixture. The BIST simulates pseudo-random data transfer scenarios in the format of real packets and Inter-Packet Gap (IPG) on the lines. The BIST allows full control of the packet lengths and of the IPG.

BIST functionality is configured using BISCRA register (0x0016h), Status is reflected in the BICSR1 register (0x0071), the BICSR2 register (0x0072), and the STS2 register (0x0017h).

2.8 Loopback Modes

There are several options for Loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the digital and analog data paths. Generally, the DP83867 may be configured to one of the Near-end loopback modes or to the Far-end (reverse) loopback. MII Loopback is configured using the BMCR (register address 0x0000). All other loopback modes are enabled using the BISCRA (register address 0x0016). Except where otherwise noted, loopback modes are supported for all speeds (10/100/1000) and all MAC interfaces.

2.8.1 Near-End Loopback Example

To verify the MAC interface, configure a Near-end loopback mode and transmit packets from the MAC. The transmit data received from the MAC will be looped back inside the PHY and returned to the MAC via the receive data signals.

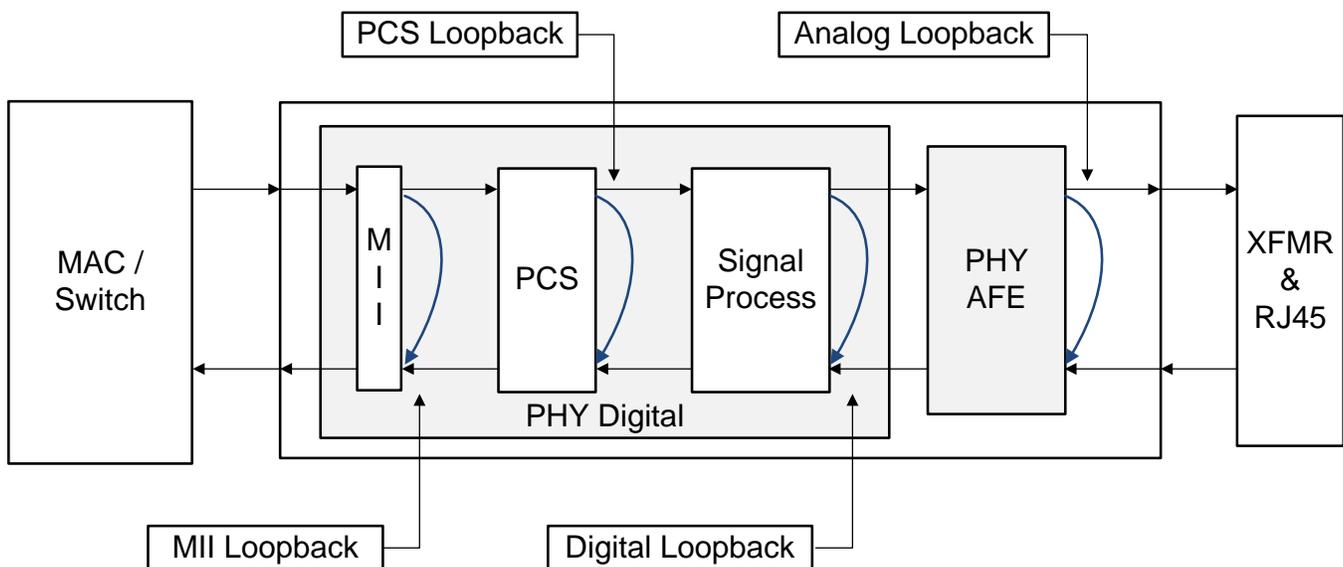


Figure 10. Block Diagram, Near-End Loopback Mode

Digital loopback is available for all operational speeds (10/100/1000). To enable Digital loopback for 1000BASE-T operation in RGMII mode, use the following sequence of register writes:

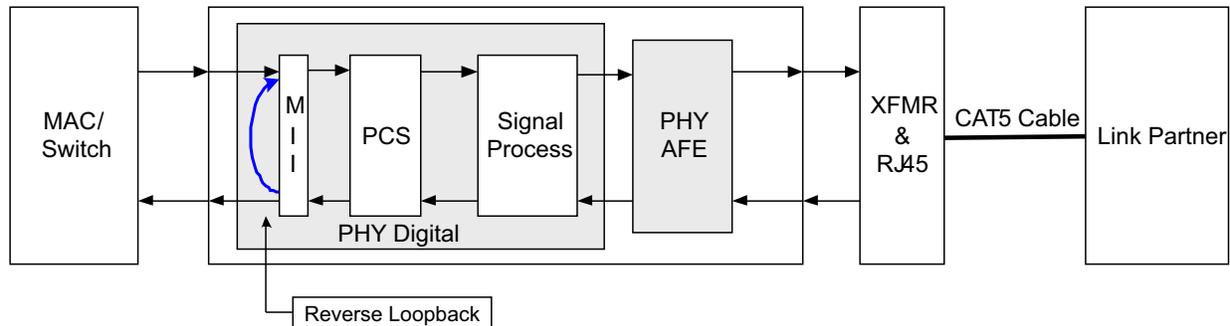
1. Write register 0x001F to 0x8000 to apply a software reset.
2. Write register 0x0000 to 0x0140 to force 1000BASE-T operation.
3. Write register 0x0032 to 0x00D3 to enable RGMII.
4. Write register 0x0016 to 0x0004 to enable digital loopback.
5. Write register 0x001F to 0x4000 to apply a software restart.

Once loopback is configured, packets can be transmitted from the MAC to verify the MAC interface.

For additional information on the RGMII timing, please refer to the application note *RGMII Interface Timing Budgets* ([SNLA243](#)).

2.8.2 Far-End Loopback Example

To verify the MDI interface, configure reverse loopback and transmit packets from a link partner. The packets received by the PHY will be looped back inside the PHY and transmitted back to the link partner via the cable.



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Figure 11. Block Diagram, Far-End Loopback Mode

Reverse loopback is available for all operational speeds (10/100/1000). Prior to configuring reverse loopback, establish a link with a link partner via good quality cabling. To enable reverse loopback, use the following sequence of register writes:

1. Write register 0x0016 to 0x0020 to enable reverse loopback.
2. Write register 0x001F to 0x4000 to apply a software restart.

Once loopback is configured, packets can be transmitted from the link partner to verify the PHY MDI interface.

2.9 Establish an MDI Link

Link with a known good partner using a known good Ethernet cabling. After establishing a valid link, confirm the key status register values. Visually verify that the link LED is lit.

There are several possible sources of link problems:

1. Link partner transmit problem
2. Cable length and quality
3. Clock quality of the 25MHz reference clock
4. MDI signal quality

IEEE compliance measurements can be made to verify the signaling. For details on these measurements, please refer to the application note *DP83867 Ethernet Compliance Testing* ([SNLA239](#)).

2.10 Establish an SGMII Link

The Serial Gigabit Media Independent Interface (SGMII) offers a high speed, low pin count connection between the MAC and the PHY. SGMII uses LVDS differential signaling and includes Auto-Negotiation capability to establish connection between the MAC and the PHY. Since this is a high speed analog connection, there are additional considerations for using this interface.

Below are several guidelines for successful communication via SGMII:

- The DP83867 includes internal SGMII terminations. No external terminations are required.
- All SGMII connections should be AC coupled via an 0.1- μ F capacitor.
- Traces should be routed with 100- Ω differential impedance.
- Skew matching within a pair should be less than 5 pS, which correlates to 30mil for standard FR4.
- When operating in 6-wire mode, the RX pair must match the Clock pair to within 5 pS, which correlates to 30mil for standard FR4.
- When operating in SGMII mode, dummy straps may be necessary to provide a balanced load for the SGMII differential pairs. Therefore, for SGMII applications with straps configured for RX_D0 and/or RX_D2, matching terminations must be used for RX_D1 and/or RX_D3. For more details, see the PHY Address Configuration section of the data sheet.
- When establishing an SGMII connection between the MAC and the PHY, both the MAC and the PHY should have a common configuration. SGMII Auto-Negotiation is the preferred mechanism for establishing communication. If Auto-Negotiation is not used, both the MAC and the PHY must be forced to the same speed and duplex configuration.
- Unstable MDI link can result in unstable SGMII connection. If the PHY cannot maintain a link, it can cause the SGMII Auto-Negotiation to loop. The unstable MDI link must be resolved in order to resolve the SGMII Auto-Negotiation loop.
- When SGMII Auto-Negotiation has completed successfully, communication between the MAC and the PHY can be verified using Near-End Loopback. Digital Loopback is recommended for SGMII testing.

3 Troubleshooting Checklist

1. Verify power supply connections, voltages, and I/O VDD selection.
2. Confirm the bandgap reference voltage (1 V) and bandgap resistor value (11 k Ω).
3. Check out the reset signal active level and inactive level.
4. Make sure reference clock has the correct frequency and amplitude.
5. Check the straps during initialization.
6. Debug the MDIO management interface. Check the pull up resistor on MDIO and the timing.
7. Is the analog functional? Verify the auto-negotiation link pulse.
8. Check out the registers. Key configuration and status registers are 0x00, 0x01, 0x04, 0x05, 0x0A, 0x10 and 0x11.
9. Use the BIST module to verify the transmit and receive functions.
10. Use loopback modes to check the MAC interface data integrity.
11. Try to link with a known good link partner.
12. Enable IEEE compliance test modes to check output signaling.

4 Conclusion

This application note provides a suggested flow for evaluating a new application and confirming the expected functionality. The step-by-step recommendations will help ease board bring up and initial evaluation of DP83867 designs.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2015) to A Revision	Page
• Added reference to troubleshooting checklist to support quick start.	1
• Deleted <i>most often</i> from text on connection via transformer in Section 1	2
• Changed phrasing of descriptions for two and three supply configurations in Section 2.1	3
• Changed description of three supply power sequencing in Section 2.1	3
• Changed order of RBIAS measurements in Section 2.2	3
• Changed line driver connections to show decoupling caps and Bob Smith terminations in Section 2.3	4
• Added pin numbers to RJ-45 connector in MDI connection diagram in Section 2.3	4
• Added note on de-coupling of magnetics center taps in Section 2.3	4
• Added recommendation to confirm strap values in strap status registers in Section 2.4.3	5
• Added cable connection diagram for termination cable in Section 2.5	6
• Added Auto-Negotiation status registers to list of key configuration and status registers in Section 2.6	7
• Added section on register access.	8
• Changed images for USB-2-MDIO GUI and MSP430 LaunchPad in Section 2.6.1	8
• Changed format of USB-2-MDIO link in Section 2.6.1	8
• Added example script for USB-2-MDIO in Section 2.6.1	8
• Added image for near-end loopback in Section 2.8.1	9
• Changed format of link for RGMII timing budgets in Section 2.8.1	9
• Added image for far-end loopback in Section 2.8.2	10
• Changed format of link for Ethernet compliance testing application note in Section 2.9	11
• Added section on establishing an SGMII link in Section 2.9	11

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