Application Report

DP83TG720: Configuring for Open Alliance Specification Compliance

ABSTRACT

OA TC12 mandates different tests for 1000BT1 PHY. This document describes the procedure to put DP83TG720R/S in the required test mode to carry out different TC12 tests.

The software and hardware configuration used during DP83TG720's TC12 testing can be found in this document. This configuration has been tested across different OA compliance houses: UNH, FTZ, and C&S and should be treated as a minimum requirement. Further improvement based on customer's system use-case is possible with additional hardware and software configuration.

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Trademarks

1 Introduction

The DP83TG720 was evaluated in accordance with the following OPEN Alliance (OA) specifications:

- OPEN Alliance 1000BASE-T1 EMC Test Specification for Transceivers - Version 2.1, by FTZ Zwickau
- OPEN Alliance 1000BASE-T1 Interoperability Test Suite, by C&S Group, GmbH
- OPEN Alliance 1000BASE-T1 test specifications for PMA (v. 1.0)/ IEEE Clause 97 1000BASE-T1 PMA by the University of New Hampshire (UNH) Inter-Operability Lab

This application note provides the details of unique hardware and software configuration used for all of the above tests.

Document also provides the required procedure details for these tests and this should assist customers implementing corresponding ECU level tests.

2 Hardware Configuration

2.1 Schematic

Schematics and right components for MDI, reference clock, and power network are very critical for the performance of 1000BT1 PHY. This section captures the recommended schematics and component values used during OA TC12 testing.

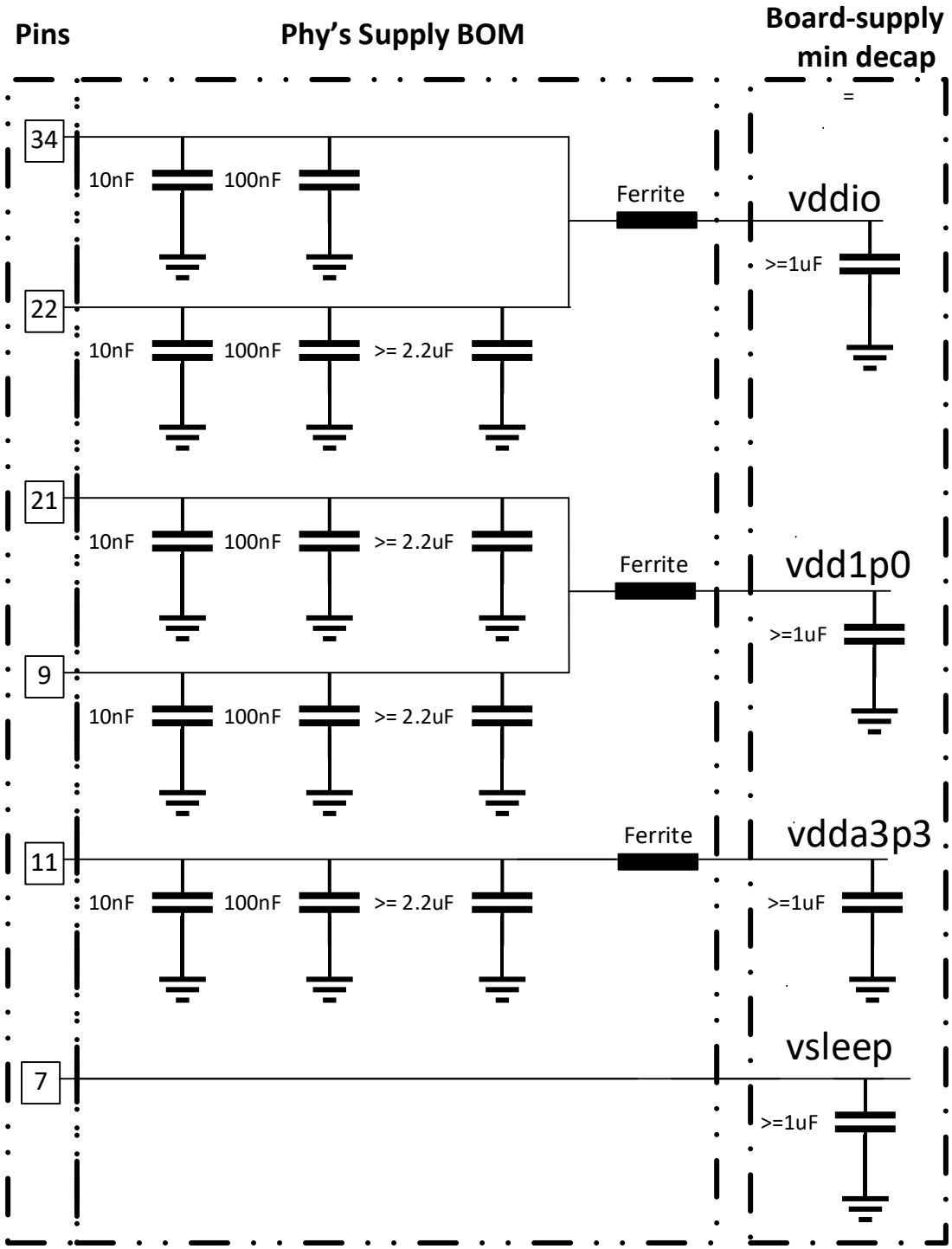

Figure 2-1. Power Supply Network: For applications with sleep mode requirement

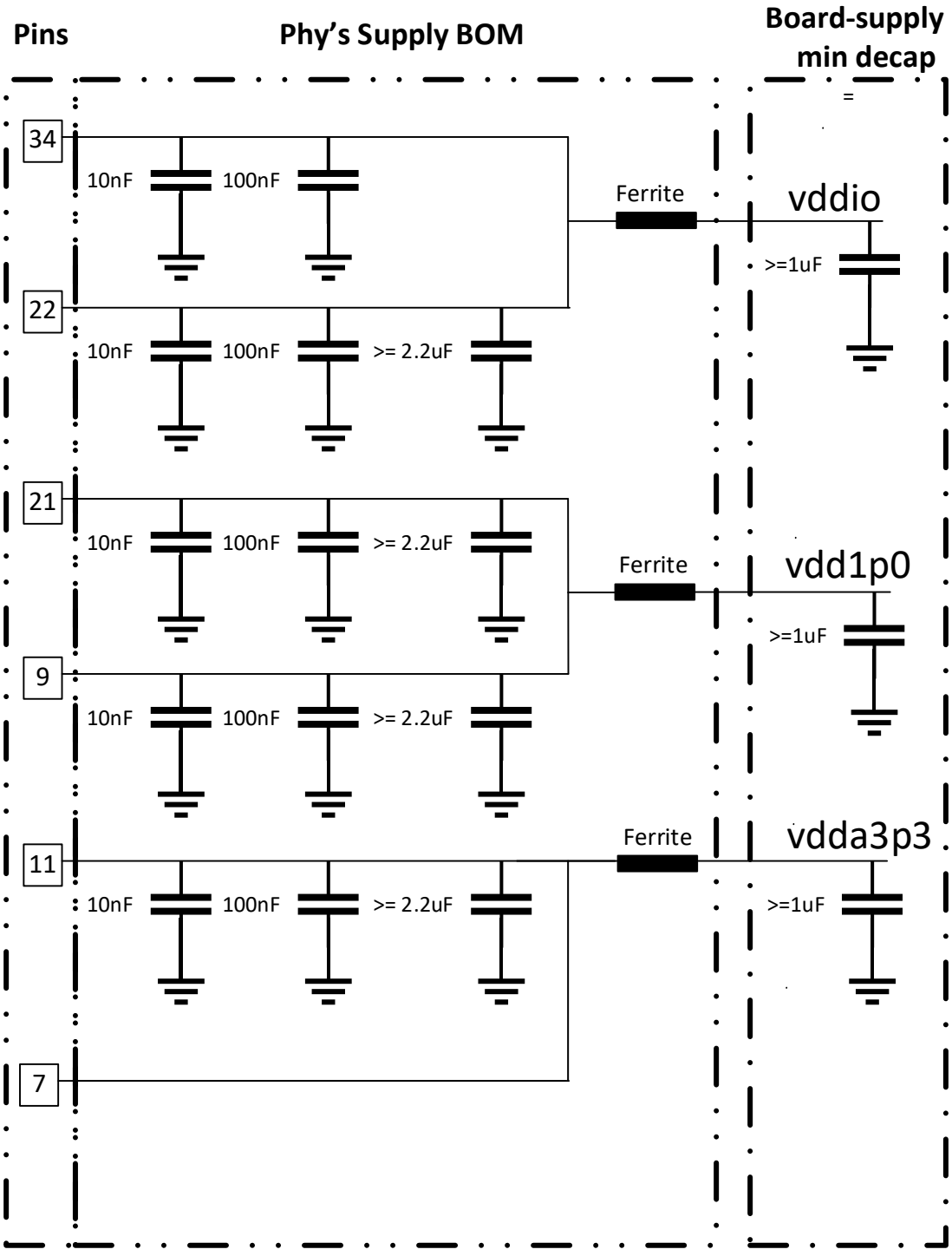

Figure 2-2. Power Supply Network: For applications without sleep mode requirement

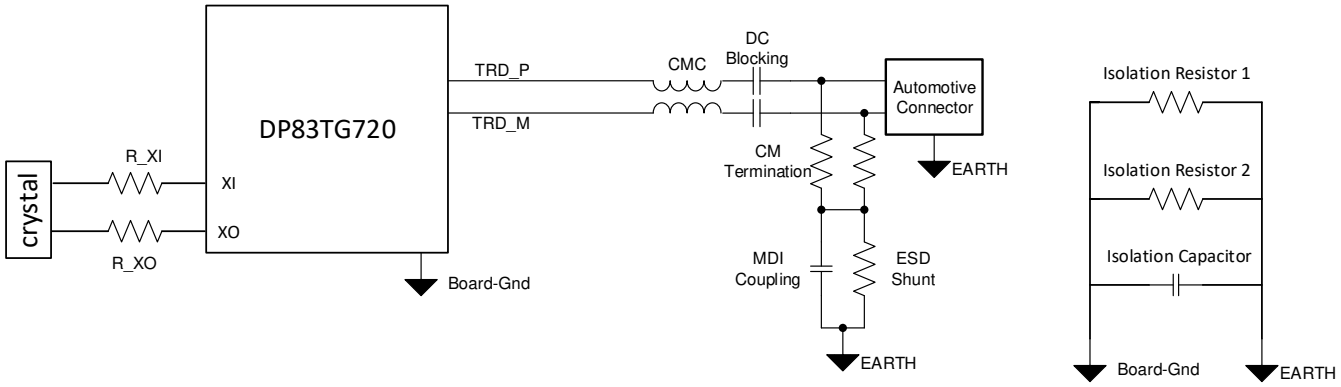

Figure 2-3. MDI and Crystal Schematic

Table 2-1. Parameters, Components, and Values

Parameter/Component	Value
V_{DDIO}	1.8 V, 2.5 V, or 3.3 V
De-Coupling Capacitors V_{DDIO} (pin 34)	10 nF, 100 nF
De-Coupling Capacitors V_{DDIO} (pin 22)	10 nF, 100 nF, 2.2uF
Combined Ferrite Bead for VDDIO	BLM18HE102SN1
V_{DDA}	3.3 V
De-Coupling Capacitors V_{DDA} (pin 11)	10 nF, 100 nF, 2.2uF
Ferrite Bead for V_{DDA}	BLM18KG601SH1
V_{DD1p0}	1 V or 1.05 V (to take care of IR drop)
De-Coupling Capacitors V_{DD1P0} (pin 9)	10 nF, 100 nF, 2.2uF
De-Coupling Capacitors V_{DDA} (pin 21)	10 nF, 100 nF, 2.2uF
Combined Ferrite Bead for V_{DD1P0}	BLM18KG601SH1
V_{sleep}	3.3 V
DC Blocking Capacitors (1% accurate, 100V)	0.1 µF
Common-Mode Choke	Murata: DLW32MH101XT2
Common Mode Termination Resistors (1% accurate,0.75 W, Size: 2010)	1 kΩ
MDI Coupling Capacitor	4.7 nF
ESD Shunt (5% accurate, 0.125 W, Size: 0805	100 kΩ
Isolation Resistor 1 (0.25 W, Size: 1206)	0 Ω
Isolation Resistor 2 (0.25 W, Size: 1206)	0 Ω
Isolation Capacitor	Not populated
R_XI	100 Ω
R_XO	Minimum required for crystal wattage spec

3 Software Configuration

This section contains the register settings of DP83TG720 used during tests in different OA compliance test houses. Most of these register settings are to take care of the margins during EMC/EMI testing. We recommend these settings as the minimum requirement. Further parameters are available to be programmed if required by system or board level constraints.

Table 3-1. Master Mode Configuration

MMD	Register	Default	Optimized	Description
1f	x001f	x0000	x8000	hard reset
1f	x0573	x0000	x0101	to not let the phy start the link-up procedure (till full configuration is written)
01	x0834	xC001	xC001	to configure phy in master mode (if not done through straps already)
1f	x0405	x6400	x5800	DSP settings for margins during OA EMC MDI emission test
1f	x08AD	x3051	x3C51	DSP settings for margins during OA EMC level-4 immunity test
1f	x0894	x5FF7	x5DF7	DSP settings for margins during OA EMC level-4 immunity test
1f	x08A0	x09F7	x09E7	DSP settings for margins during OA EMC level-4 immunity test
1f	x08C0	x1500	x4000	DSP settings for margins during OA EMC level-4 immunity test
1f	x0814	x1027	x4800	DSP settings for margins during OA EMC level-4 immunity test
1f	x080D	x2ABF	x2EBF	DSP settings for margins during OA EMC level-4 immunity test
1f	x08C1	x0800	x0B00	DSP settings for margins during OA EMC level-4 immunity test
1f	x087D	x0000	x0001	DSP settings for margins during OA EMC level-4 immunity test
1f	x082E	x0000	x0000	DSP settings for margins during OA EMC level-4 immunity test
1f	x0837	x0000	x00F4	DSP settings for margins during OA EMC level-4 immunity test
1f	x08BE	x0000	x0200	DSP settings for margins during OA EMC level-4 immunity test
1f	x08C5	x0000	x4000	DSP settings for margins during OA EMC level-4 immunity test
1f	x08C7	x0000	x2000	DSP settings for margins during OA EMC level-4 immunity test
1f	x08B3	x0000	x005A	DSP settings for margins during OA EMC level-4 immunity test
1f	x08B4	x0000	x005A	DSP settings for margins during OA EMC level-4 immunity test
1f	x08B0	x0203	x0202	DSP settings for margins during OA EMC level-4 immunity test
1f	x08B5	x0000	x00EA	DSP settings for margins during OA EMC level-4 immunity test
1f	x08BA	x0000	x2828	DSP settings for margins during OA EMC level-4 immunity test
1f	x08BB	x0000	x6828	DSP settings for margins during OA EMC level-4 immunity test
1f	x08BC	x0000	x0028	DSP settings for margins during OA EMC level-4 immunity test

Table 3-1. Master Mode Configuration (continued)

MMD	Register	Default	Optimized	Description
1f	x08BF	x0000	x0000	DSP settings for margins during OA EMC level-4 immunity test
1f	x08B1	x0014	x0014	DSP settings for margins during OA EMC level-4 immunity test
1f	x08B2	x0008	x0008	DSP settings for margins during OA EMC level-4 immunity test
1f	x08EC	x0006	x0000	DSP settings for margins during OA EMC level-4 immunity test
1f	x08C8	x0000	x0003	DSP settings for margins during OA EMC level-4 immunity test
1f	x08BE	x0000	x0201	DSP settings for margins during OA EMC level-4 immunity test
1f	x018C	0x0000	x0001	to bring phy out of non-autonomous mode (only if phy is strapped in non-auto mode)
1f	x001f	x0000	x4000	soft reset
1f	x0573	0x0000	x0001	to let phy start the link-up procedure (after above configuration is done).
1f	x056A	x1F49	x5F41	to start the send-s detection during link-up sequence

Table 3-2. Slave Mode Configuration

MMD	Register	Default	Optimized	Description
1f	x001f	x0000	x8000	hard reset
1f	x0573	x0000	x0101	to not let the phy start the link-up procedure (till full configuration is written)
01	x0834	x8001	x8001	to configure phy in slave mode (if not done through straps already)
1f	x0894	x5FF7	x5DF7	DSP settings for margins during OA EMC MDI emission test
1f	x056A	x1F49	x5F40	DSP settings for margins during OA EMC level-4 immunity test
1f	x0405	x6400	x5800	DSP settings for margins during OA EMC level-4 immunity test
1f	x08AD	x3051	x3C51	DSP settings for margins during OA EMC level-4 immunity test
1f	x0894	x5FF7	x5DF7	DSP settings for margins during OA EMC level-4 immunity test
1f	x08A0	x09F7	x09E7	DSP settings for margins during OA EMC level-4 immunity test
1f	x08C0	x1500	x4000	DSP settings for margins during OA EMC level-4 immunity test
1f	x0814	x1027	x4800	DSP settings for margins during OA EMC level-4 immunity test
1f	x080D	x2ABF	x2EBF	DSP settings for margins during OA EMC level-4 immunity test
1f	x08C1	x0800	x0B00	DSP settings for margins during OA EMC level-4 immunity test
1f	x087D	x0000	x0001	DSP settings for margins during OA EMC level-4 immunity test
1f	x082E	x0000	x0000	DSP settings for margins during OA EMC level-4 immunity test
1f	x0837	x0000	x00F4	DSP settings for margins during OA EMC level-4 immunity test
1f	x08BE	x0000	x0200	DSP settings for margins during OA EMC level-4 immunity test
1f	x08C5	x0000	x4000	DSP settings for margins during OA EMC level-4 immunity test
1f	x08C7	x0000	x2000	DSP settings for margins during OA EMC level-4 immunity test
1f	x08B3	x0000	x005A	DSP settings for margins during OA EMC level-4 immunity test
1f	x08B4	x0000	x005A	DSP settings for margins during OA EMC level-4 immunity test
1f	x08B0	x0203	x0202	DSP settings for margins during OA EMC level-4 immunity test
1f	x08B5	x0000	x00EA	DSP settings for margins during OA EMC level-4 immunity test
1f	x08BA	x0000	x2828	DSP settings for margins during OA EMC level-4 immunity test
1f	x08BB	x0000	x6828	DSP settings for margins during OA EMC level-4 immunity test
1f	x08BC	x0000	x0028	DSP settings for margins during OA EMC level-4 immunity test
1f	x08BF	x0000	x0000	DSP settings for margins during OA EMC level-4 immunity test
1f	x08B1	x0014	x0014	DSP settings for margins during OA EMC level-4 immunity test

Table 3-2. Slave Mode Configuration (continued)

MMD	Register	Default	Optimized	Description
1f	x08B2	x0008	x0008	DSP settings for margins during OA EMC level-4 immunity test
1f	x08EC	x0006	x0000	DSP settings for margins during OA EMC level-4 immunity test
1f	x08C8	x0000	x0003	DSP settings for margins during OA EMC level-4 immunity test
1f	x08BE	x0000	x0201	DSP settings for margins during OA EMC level-4 immunity test
1f	x056A	x1F49	x5F40	to avoid send-s detection till the configuration is done
1f	x018C	x0000	x0001	to bring phy out of non-autonomous mode (only if phy is strapped in non-auto mode)
1f	x001f	x0000	x4000	soft reset
1f	x0573	x0000	x0001	to let phy start the link-up procedure (after above configuration is done).
1f	x056A	x1F49	x5F41	to start the send-s detection during link-up sequence

Note

Sequence of above register writes is important. For both master and slave configuration all the DSP settings are in-between the writes to register 0x0573 and 0x056A. This is to make sure that the link-up sequence does not start before the full configuration is written.

4 Testing PMA

OA TC12 specifies different electrical tests for 1000BT1 PHY's front end. Different test modes have been specified in the standard document. In each test mode, PHY is supposed to generate patterns on MDI lines or expose internal clock signal on a pin for measurement of different electrical parameters.

DP83TG720 supports all these test modes. This section gives details of the required configuration to enter into each test modes.

Detailed PMA test report from UNH (OA compliance test house) with OA/IEEE compliant results is available on request.

4.1 PMA Testing Procedure

Note

- Before programming any of the test modes, DP83TG720 should be loaded with the respective initialization register configuration (master or slave) as described in earlier section.
- Test mode 1 requires link to be established between DUT and link-partner, hence register [0x0001] should read as 0x0145 before running the test.

Table 4-1. Programming PMA Test Modes

Test Mode	MMD	Register	Value
Test Mode 1: Tx_Tclk 125MHz on CLKOUT pin.	x01	0x0904	0x2000
Test Mode 2	x01	0x0904	0x4000
Test Mode 4: Tx_Tclk 125MHz on CLKOUT pin.	x01	0x0904	0x8000
	x1F	0x0453	0x0019
Test Mode 5	x01	0x0904	0xA000
Test Mode 6	x01	0x0904	0xC000
Test Mode 7	x01	0x0904	0xE000

5 Testing IOP: Link-up and Link-down

OA TC12 specifies different PHY level tests to test link-up time, link-down time and link stability. Similar ECU level tests have been highlighted in OA TC8. This section highlights the test sequence used for these IOP tests for PHY level testing and the same can be ported for ECU level tests.

TC12-interoperability tests are carried out by OA compliance test house C&S. To test interoperability of DP83TG720 , C&S tests each of these parameters with DP83TG720 and other 1000BT1 certified PHYs as its link-partners. Each of these parameters are tested for large number of iterations over different temperatures and cable lengths.

Detailed IOP test report from C&S with OA compliant results is available on request.

5.1 IOP Testing Procedure

Start of measurement:

For the IOP tests measuring link-up time either after power-up or after hardware reset, it is important to start the measurement of link-up time after the initialization configuration is loaded back into DP83TG720. As the configuration is loaded into the PHY by a controller, we recommend the controller to give an indication (a software bit or an IO state) after the last configuration register is written. This indicator going high is the start of measurement of link-up time.

Status to be poled:

Link-status is indicated by bit 15 of register 0x0180: 1 = link-up; 0 = link-down. This should be poled to indicate the event of link-up or link-down during these tests.

Note

If system desires no automatic link-up after power-up (link to only happen after writing the initialization script), managed mode of DP83TG720 should be used by using strap on pin LED_1.

6 Testing SQI

SQI gives the indication of signal quality on the copper cable.

OA TC-12 indicates that SQI values should decrease monotonically with increase in noise levels. We recommend to add extra hysteresis. Procedure for adding extra hysteresis is covered in this section.

Detailed SQI test report from C&S with OA compliant results is available on request.

6.1 SQI Testing Procedure

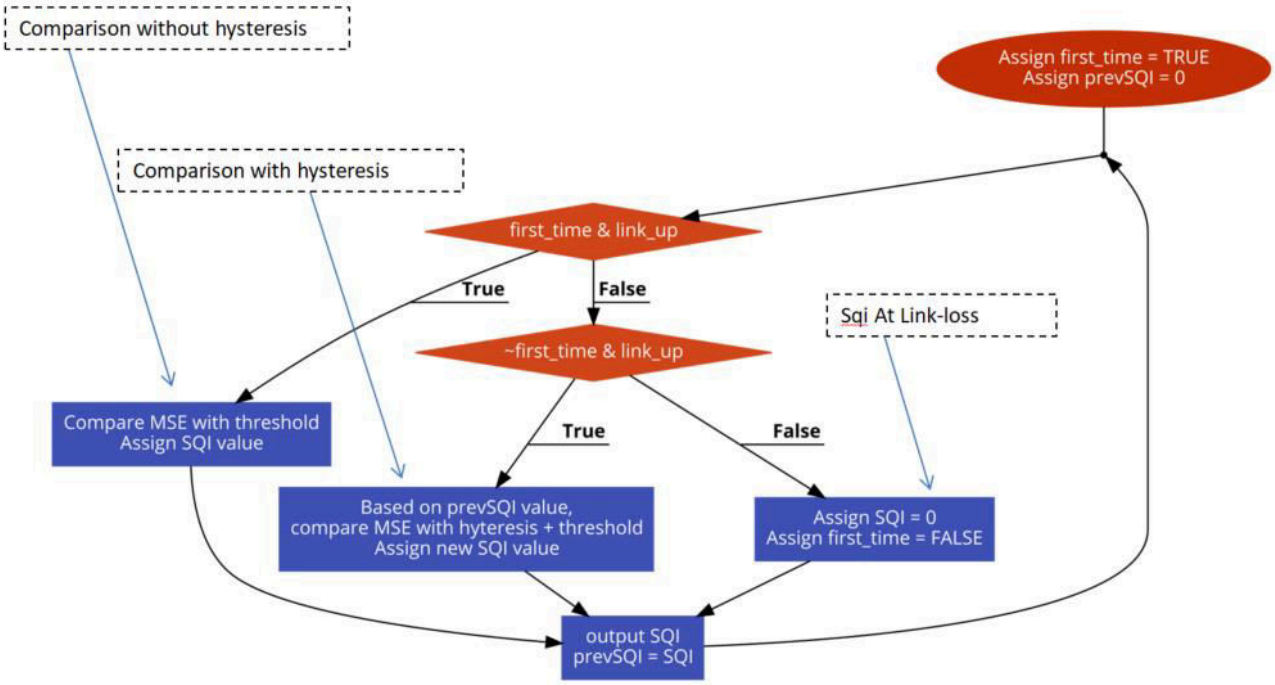

Figure 6-1. SQI Procedure For Extra Hysteresis

Sample Code for Extra Hysteresis :

```
cyg_uint8 TI_DP83TG720::GetSQI() {
    static cyg_uint16 first_time = 1;
    static cyg_uint16 prevSQI = 0;
    cyg_uint16 regValue;
    cyg_uint16 reg_link;
    cyg_uint16 mse_lock;
    cyg_uint16 result;

    reg_link = ReadRegister(0x1F, 0x0180);
    regValue = ReadRegister(0x1F, 0x875);
    mse_lock = (regValue & 0x3FF);

//comparison without hysterisis

    if ((first_time == 1) && ((reg_link & 0x3007) == 0x3007)){
        if (mse_lock >= 0x65)             //threshold1_down
            result = 0x1;
        else if (mse_lock >= 0x50)          //threshold2_down
            result = 0x2;
        else if (mse_lock >= 0x33)        //threshold3_down
            result = 0x3;
        else
            result = 0x4;
        first_time = 0;
    }

//comparison with hysterisis

    else if ((first_time == 0) && ((reg_link & 0x3007) == 0x3007)){
        if (prevSQI == 0x1)
            if (mse_lock < 0x65)        //threshold1_down
                result = 0x2;
            else
                result = 0x1;
        else if (prevSQI == 0x2)
            if (mse_lock < 0x50)        //threshold2_down
                result = 0x3;
            else if (mse_lock > 0x72)    //threshold2_up
                result = 0x1;
            else
                result = 0x2;
        else if (prevSQI == 0x3)
            if (mse_lock < 0x33)        //threshold3_down
                result = 0x4;
            else if (mse_lock > 0x5E)    //threshold3_up
                result = 0x2;
            else
                result = 0x3;
        else if (prevSQI == 0x4)
            if (mse_lock > 0x42)        //threshold4_up
                result = 0x3;
            else
                result = 0x4;
    }

//sqi at link-loss

    else {
        first_time = 1;
        result = 0x0;
    }

    prevSQI = result;

    return static_cast<cyg_uint8>(result);
}
```

7 Testing TDR

This section describes the procedure to test cable faults: open/short.

Detailed TDR test report from C&S with OA compliant results is available on request.

Note

OA TC-12 tests done at C&S tests are for open and short cable fault test cases. Also TDR is usually run to find root-cause when there is no link. Test procedure described in next section has an extra step over compliance test procedure: to force link-down condition when possible (use if required).

7.1 TDR Testing Procedure

Table 7-1. TDR Run Procedure

Sequence	Description	Register Read/Write
Step 1: For DP83TG720 as master	Force the link-down by writing register and enable link-partner to go silent. Wait for ~1s after register write. In case of valid open and short cable faults, TDR will still work fine without step 1. For good cable case, TDR register 0x001E may show *Fail* on bypassing this step.	Write register[0x0576] = 0x0400
Step 1: For DP83TG720 as slave	Link-partner should be made silent. In case of valid open and short cable faults, TDR will still work fine without step 1. For good cable case, TDR register 0x001E may show *Fail* on bypassing this step.	
Step 2	TDR configuration: Pre-run	reg[0x0301] = 0xA008, reg[0x0303] = 0x0928, reg[0x0304] = 0x0004, reg[0x0405] = 0x6400
Step 3	Start TDR	0x001E[15] = 1
Step 4	Wait for 100ms (should be sufficient for TDR to converge for maximum cable length)	
Step 5	Read 0x001E[1:0] = [TDR done : TDR fail]. Value should be [1,0]. Fault type/locations are valid only if this correct value is read. Value other than [1,0] will mean that there is some noise/ signal on the line which is causing TDR to fail.	
Step 6	Fault type and location is read.	Read register 0x030F for fault status and fault type. If a valid fault is detected : register 0x030F[7:4] = 0011 or 0110, then fault distance is decimal(register[0x030F][7:4]) meters.

8 Testing EMC/EMI

OA TC-12 specifies conducted EMC/EMI tests. For DP83TG720, these tests were carried out in OA compliance test house FTZ and testing of emissions on MDI, emissions on each supply pin, immunity to RF signals are part of the test suite. The board was designed in accordance with OA specifications by FTZ.

Hardware and software configurations highlighted in the document were used for these conducted EMC/EMI tests. Configurations are available if further enhancement over TC-12 specs are required for an application.

Detailed test report from FTZ with procedures and OA compliant results is available on request.

Other than conducted emission tests (for OA TC-12 compliance), DP83TG720 (with mentioned hardware and software configuration) has been tested against different radiated emission and radiated immunity requirements of different OEMs. Details of radiated emission and immunity test results are available on request. Configurations are available if further enhancement of margins is required for an application.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2020) to Revision A (March 2021)	Page
• SQI test procedure sample driver code is updated	12
• For TC12's SQI test, number of SQI steps, thresholds and corresponding sample code updated	12
• TDR configuration : Pre-run updated	14

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