Application Report
SPRAC62B–December 2016–Revised November 2017

Optimizing DRA7xx and TDA2xx Processors for Use With Video Display SerDes

ABSTRACT

The purpose of this application report is to provide guidance on configuring DRA7xx and TDA2xx processors to meet video Serializer/Deserializer (SerDes) jitter requirements.

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1 Introduction

Video display SerDes, such as the Texas Instruments FPD-Link SerDes, can be used to translate the parallel video output interfaces and high-definition multimedia interface (HDMI) interfaces of DRA7xx and TDA2xx Processors into high-speed serialized interfaces. To ensure proper operation of these high-speed serial interfaces, jitter on the clock input to the serializer should be controlled to meet the jitter requirements of the SerDes components. The FPD-Link SerDes jitter requirements can be found in the FPD-Link jitter measurement document.

This application report addresses the following products:

- DS90UB921,DS90UH921, DS90UB925, DS90UH925 parallel video FPD-Link serializers
- DS90UB926, DS90UH926, DS90UB928, DS90UH928, DS90UB924 parallel video FPD-Link deserializers
- DS90UB949, DS90UH949 HDMI FPD-Link serializers
- DS90UB948, DS90UH948 OpenLDI FPD-Link deserializers
- DRA77x, DRA76x, DRA75x, DRA74x, DRA72x infotainment application processors
- TDA2Px and TDA2x ADAS Applications Processors

2 Recommended Configurations

2.1 DRA75x/74x/72x and TDA2x Recommended Configurations in FPD-Link Applications

For video frequencies >85 MHz, the processor's HDMI interface should be used in conjunction with an HDMI serializer/deserializer solution such as the Texas Instruments DS90UB/H949 / DS90UB/H948 SerDes.

For video frequencies <=85 MHz, the processor's HDMI interface and parallel video output interface can be used in conjunction with a FPD-Link SerDes solution. When using the parallel video output interfaces in FPD-Link SerDes applications, the recommended processor configuration is dependent on the number of parallel-to-serial interfaces needed in the system.

If a single parallel-to-serial interface is needed, the following processor configuration is recommended:

- Use DPLL_HDMI to source the video port pixel clock
- Use any valid VOUT1/2/3 IOSET

If a second parallel-to-serial interface is needed, the following additional configuration is recommended:

- Use DPLL_VIDEOx (x=1,2) to source the video port pixel clock
- Use the VOUT1 IOSET configuration
- If running the video port pixel clock at frequencies > approximately 70 MHz, it is recommended to add a clock cleaner on the serializer clock input to reduce jitter.

The following sections cover the details on the above recommended configurations.

2.2 DRA77x/76x and TDA2Px Recommended Configurations in FPD-Link Applications

DRA77x/76x and TDA2Px support the following additional video port pixel clock sources that are not available in DRA75x/74x/72x and TDA2x devices:

- DPLL_PCIE_REF
- DPLL_SATA
- wakeup0 pin
- wakeup1 pin
- vin1a_clk pin
- vin1b_clk pin

In addition to the available DPLL_HDMI and DPLL_VIDEOx clock sources (described in the previous section), these new clock sources can be selected for any VOUT interface via the DSS_PLL_CONTROL register in the Control Module. These new clock sources are recommended for use instead of DPLL_VIDEOx in systems that require more than one parallel-to-serial interface.

If either the PCIe or SATA interface is unused in the system, DPLL_PCIE_REF or DPLL_SATA can be configured to source one or more of the video port pixel clocks. Similar to DPLL_HDMI, a clock cleaner is not required on the Serializer clock input, and any valid VOUT IOSET is recommended.

The four pins listed above can also be used as external clock inputs to source the video port pixel clocks. The reference clock provided on these pins must be compliant to the FPD-Link SERDES jitter requirements. If a compliant clock source is provided, then a clock cleaner on the Serializer clock input is not required, and any valid VOUT IOSET is recommended.

2.3 Recommended Configurations in Non-FPD-Link SerDes Applications

The recommended DRA7xx and TDA2xx configurations for non-FPD-Link applications are generally the same as those described above for FPD-Link applications. However, the interface timing requirements and input clock jitter requirements can vary between SerDes solutions. These items must be analyzed by the customer to assure robust system-level timing and jitter performance.

3 DRA7xx and TDA2xx PLL Configurations

The DRA7xx and TDA2xx processors contain integrated PLLs that play a large roll in controlling the jitter on the video output port pixel clocks that are used to drive the serializer clock input. These PLLs come in two types:

- DPLL_VIDEOx
- DPLL_HDMI (plus DPLL_PCIE_REF and DPLL_SATA on DRA77x/76x and TDA2Px devices)

The following sections describe how to configure each PLL type for minimal jitter in a Video SERDES application.

3.1 PLL Configurations in FPD-Link Applications

3.1.1 DPLL_HDMI Overview

Figure 1 shows a block diagram of the video output pixel clock when sourced by DPLL_HDMI. The system oscillator clock xi_oscx (x=0, 1) is used by DPLL_HDMI to generate the DPLL_HDMI_CLK1 output based on the programmed N/M/M2 pre-divider/multiplier/post-divider settings. The DPLL_HDMI_CLK1 output then passes through LCD and PCD dividers in the DISPC module before appearing on the voutx_clk (x=1,2,3) output.

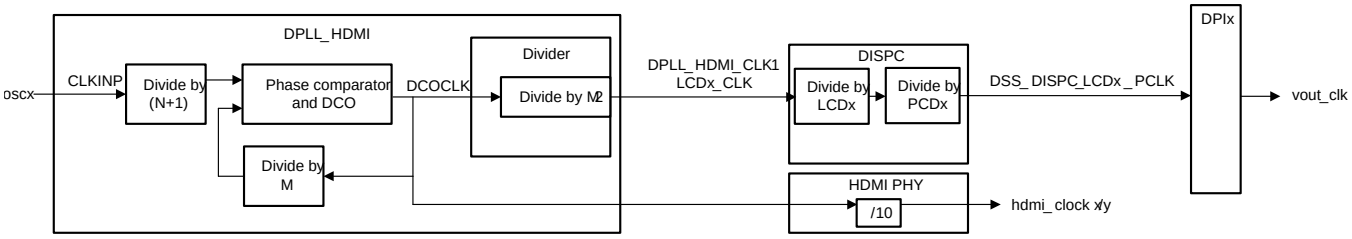

Figure 1. Block Diagram of DPLL_HDMI Clock Path

Equation 1 shows the calculation of the voutx_clk frequency based on the xi_oscx frequency and the DPLL_HDMI-based multiplier and dividers described above.

$$voutx\_clk = xi\_oscx * \frac{M}{(N+1)} * \frac{1}{(M2)} * \frac{1}{(LCD)} * \frac{1}{(PCD)} \quad (1)$$

The following restrictions also apply when configuring the multiplier and divider settings for DPLL_HDMI:

- 625 KHz < xi_oscx / (N + 1) < 2.5 MHz
- 750 MHz < xi_oscx / (N + 1) * M < 2.5 GHz
- SELFREQDCO set as follows:
  - SELFREQDCO = 2, when xi_oscx / (N + 1) * M < 1250 MHz
  - SELFREQDCO = 4, when xi_oscx / (N + 1) * M >= 1250 MHz
- PLL_SD Sigma Delta divider set as follows:
  - PLL_SD = ceiling (M / (N+1) * xi_oscx / 250)
- LCDx_CLK <= 165 MHz
- M2, LCD, and PCD should be even or 1, or followed by a divider that is even, to produce a 50% functional duty cycle.

3.1.1.1 DPLL_HDMI Recommended Configurations

DPLL_HDMI has a different architecture than DPLL_VIDEOx that does not produce significant sideband spectral content under any configurations. Therefore, any valid DPLL_HDMI configuration is generally suitable for FPD-Link applications.

Based on TI EVM characterization, a sample list of recommended DPLL_HDMI configurations, based on a 20 MHz CLKINP for common voutx_clk frequencies, is provided in Table 1. However, voutx_clk jitter is dependent on many system-level details and varies from system-to-system. Therefore, it is recommended that these and other configurations be measured directly on the customer system to validate compliance with the FPD-Link PCLK input requirements.

Table 1. Recommended DPLL_HDMI Configurations for Parallel Video Applications

voutx_clk	N	M	M2	SELFREQDCO	PLL_SD	PCD	LCD
74 MHz	23	2590	28	4	9	1	1
80 MHz	23	1920	20	4	7	1	1
82.4 MHz	24	1030	10	2	4	1	1

Table 2 contains a sample recommended DPLL_HDMI configuration for HDMI applications, based on TI EVM characterization. It is recommended that this and other configurations be measured directly on the customer system to validate compliance with the FPD-Link input requirements.

Table 2. Recommended DPLL_HDMI Configuration for HDMI Applications

hdmi1_clockx/y	N	M	SELFREQDCO	PLL_SD
148.5 MHz	23	1782	4	6

3.1.2 DPLL_PCIE_REF and DPLL_SATA Overview (DRA77x/76x and TDA2Px only)

The primary function of DPLL_PCIE_REF and DPLL_SATA is to provide the reference clocks to the PCIe and SATA modules within the device. However, if the PCIe or SATA interface is unused, DRA77x/76x and TDA2Px devices allow these PLLs to be used to source the video port pixel clock for any VOUT interface.

The functional description and recommended configurations for these PLLs, when used to source the video port pixel clock, is the same as described above for Parallel Video Applications in the DPLL_HDMI section.

3.1.3 DPLL_VIDEOx Overview

Figure 2 shows a block diagram of the video output pixel clock when sourced by DPLL_VIDEOx. The system oscillator clock xi_oscx (x=0, 1) is used by DPLL_VIDEOx to generate a high-frequency DCOCLK output based on the programmed N/M pre-divider/multiplier settings. The DCOCLK then passes through an HSDIVIDER module that divides the clock based on the programmed Mx (x=4,6,7) value. The HSDIVIDER clkoutx (x=1/3/4) output then passes through LCD and PCD dividers in the DISPC module before appearing on the voutx_clk (x=1,2,3) output.

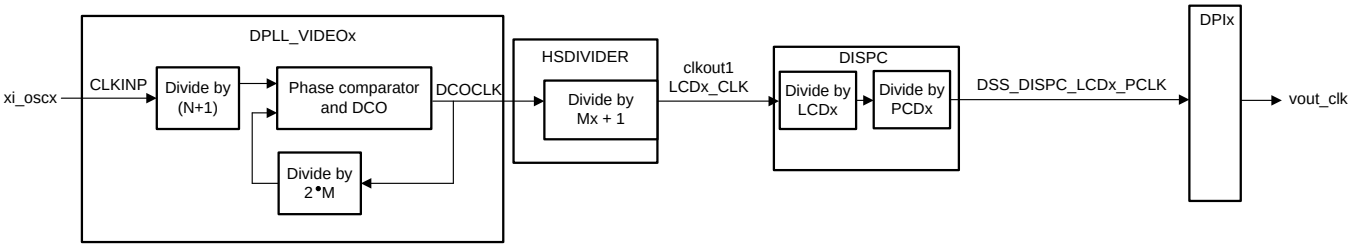

Figure 2. Block Diagram of DPLL_VIDEOx Clock Path

Equation 2 shows the calculation of the voutx_clk frequency based on the xi_oscx frequency and the DPLL_VIDEOx-based multiplier and dividers described above.

$$voutx\_clk = xi\_oscx * \frac{2M}{(N+1)} * \frac{1}{(M4\ +\ 1)} * \frac{1}{(LCD)} * \frac{1}{(PCD)} \quad (2)$$

The following restrictions also apply when configuring the multiplier and divider settings for DPLL_VIDEOx:

- 150 KHz < xi_oscx / (N + 1)
- 40 MHz < xi_oscx / (N + 1) * 2M < 2.8 GHz
- LCDx_CLK < = 165 MHz
- LCD and PCD should be even or 1, or followed by a divider that is even, to produce a 50% functional duty cycle.

3.1.3.1 DPLL_VIDEOx Recommended Configurations

DPLL_VIDEOx must be configured to use both large N (pre-divider, first priority) and large M (multiplier, second prioirty) values to achieve the lowest voutx_clk jitter as measured by the procedure described in the FPD-Link jitter measurement document (Tj at BER). Note that other forms of jitter (for example, cycle-to-cycle jitter) may increase when optimizing for Tj at BER. Therefore, only Tj at BER as described in the FPD-Link jitter measurement document should be optimized when determining the best PLL setting.

Based on TI EVM characterization, a sample list of recommended DPLL_VIDEOx configurations, based on a 20 MHz CLKINP for common voutx_clk frequencies, is provided in Table 3. Other configurations are possible and should target similar N and M values to those in the table. However, voutx_clk jitter is dependent on many system-level details and varies from system-to-system. Therefore it is recommended that these and other configurations be measured directly on the customer system to validate compliance with the FPD-Link PCLK input requirements.

Table 3. Recommended DPLL_VIDEOx Configurations

voutx_clk	N	M	M4	PCD	LCD
64.25 MHz	111	1799	9	1	1
74.12 MHz	117	1968	8	1	1
74.27 MHz	122	1827	7	1	1
80 MHz	122	1968	3	2	1
82.4 MHz	124	1545	5	1	1

When using DPLL_VIDEOx to source the video output pixel clock in an FPD-Link application, it is also required to insert a clock cleaner on the DS90Ux92x PCLK input to meet the jitter requirements. For more details on using a clock cleaner in a FPD-Link application, see Section 6.

3.2 PLL Configurations in non-FPD-Link Applications

The recommended DRA7xx and TDA2xx PLL configurations for non-FPD-Link applications are generally the same as those described above for FPD-Link applications. However, the input clock jitter requirements can vary between SerDes solutions and must be analyzed by the customer to assure robust jitter performance.

4 DRA776/76x and TDA2Px External Input Clocks

DRA77x/76x and TDA2Px support external clock reference inputs on the following pins to source the video port pixel clocks:

- wakeup0 pin
- wakeup1 pin
- vin1a_clk pin
- vin1b_clk pin

The reference clock provided on these pins must be compliant to the FPD-Link SERDES jitter requirements. In addition, it is recommended that the VOUT clock output be measured directly on the customer system to validate compliance with the FPD-Link PCLK input requirements.

5 FPD-Link Deserializer Equalizer Reset Requirements

FPD-Link Deserializers contain an Equalizer that automatically adapts to the channel. The adaptation works by cycling through pre-defined Equalizer settings each time the Deserializer loses lock on the input signal. To ensure that the most optimal Equalizer setting is chosen, it is required to reset the Equalizer when any changes are made to the Serializer output after the Deserializer has been enabled. Examples of run-time changes that would require an Equalizer reset include:

- Changing the Serializer PCLK input frequency
- Enabling the Serializer output after the Deserializer is enabled

Failing to reset the Equalizer in these situations can result in non-optimal settings that can cause Display artifacts such as flicker.

To reset the Equalizer in a DS90Ux92x FPD-Link Deserializer, the following register programming is required:

- Register Name: Reset → Register Address: 0x01 → Register Bit: 1 → Function: Digital RESET0 → Set Value: 1:Reset

6 Clock Cleaner Usage

6.1 When to Use a Clock Cleaner

Systems using DPLL_VIDEOx in parallel-video output applications to source PCLK at frequencies > approximately 70 MHz are recommended to add a clock cleaner component on the DS90Ux92x PCLK input to minimize jitter.

In general, adding a clock cleaner is not necessary when sourcing PCLK from DPLL_HDMI.

Adding a clock cleaner is also not necessary when using the processor's HDMI interface.

6.2 Clock Cleaner Block Diagram

Figure 3 shows a block diagram illustrating how to include a clock cleaner in a FPD-Link system.

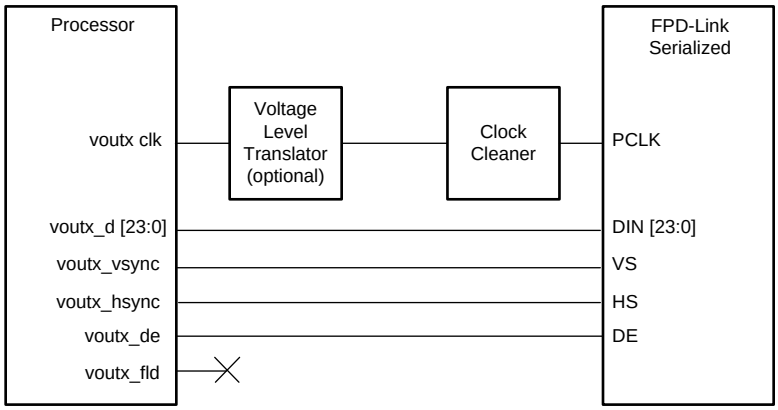

Figure 3. Clock Cleaner Block Diagram

6.3 Clock Cleaner Implementation

This section presents a recommended clock cleaner along with the associated implementation details.

6.3.1 CDCE813

The recommended clock cleaner is the Texas Instruments CDCE813. It is designed to supports clock frequencies > 70 MHz. Table 4 shows the recommended CDCE813 connections.

Table 4. CDCE813 Recommended Connections

CDCE813 Pin	Recommended Connection
Xin/CLK	Processor (voutx_clk) or voltage translator (output)
S0	Open
VDD	1.8 V
Vctrl	Open
GND	GND
VDDOUT	3.3 V
Xout	Open
S1/SDA	Processor (SDA)
S2/SCL	Processor (SCL)
Y1	Serializer (PCLK) (1)
GND	GND
Y2	Open
Y3	Open

(1) 50 Ω termination to GND at the Serializer (PCLK) input is required if the Serializer interface is operating at 1.8 V.

The CDCE813 input voltage level (controlled by VDD) is 1.8 V. Therefore, a voltage level shifter is required if the processor video port interface is operating at 3.3 V.

The CDCE813 output voltage level (controlled by VDDOUT) is 3.3 V. 50 Ω termination to GND at the Serializer (PCLK) input is required if the Serializer interface is operating at 1.8 V.

For more details on I/O translation, see Section 6.4.

The CDCE813 contains an on-chip EEPROM that is programmed with the following key settings for compatibility with a FPD-Link system:

- Generic Configuration Register → Register field “M1” → Clock source selection for output Y1: → Setting “1 - PLL1 clock”
- Generic Configuration Register → Register fields “Y1_ST1” and “Y1_ST2” → Y1-State0/1 → Setting “10 – Y1 disabled to low”

The CDCE813 has a non-zero input-to-output delay that must be factored into the timing analysis and closure for the processor/FPD-Link interface. For details, see Section 6.6.

6.4 Clock Cleaner IO Voltage Translation

IO voltage compatibility must be addressed when including a clock cleaner in a SerDes application. In a typical system, there are four groups of transmitter-receiver pairs to evaluate for IO voltage compatibility. Transmitter-receiver pairs in the same group must always operate at the same IO voltage. Table 5 lists the four transmitter-receiver pair groups and their associated voltage control.

Table 5. IO Voltage Compatibility Chart

	Transmitter		Receiver	
	Pin	**Voltage Control**	**Pin**	**Voltage Control**
Group 1	Processor voutx_clk output	Processor vddshvx Dual Voltage Power Supply	Clock Cleaner Input	Clock Cleaner Input Supply
Group 2	Processor voutx_d[23:0], voutx_vsync, voutx_hsync, voutx_de outputs	Processor vddshvx Dual Voltage Power Supply	Serializer DIN[23:0], VS, HS, DE inputs	Serializer VDDIO Supply
Group 3	Other Processor pins in the same Power Group as the voutx_* pins	Processor vddshvx Dual Voltage Power Supply	Other system IC inputs	Power Supplies for other ICs
Group 4	Clock Cleaner Output	Clock Cleaner Output Supply	Serializer PCLK Input	Serializer VDDIO Supply

If all transmitters and receivers run at the same voltage (1.8 V or 3.3 V), then no voltage translation is required.

If all transmitters and receivers run at 3.3 V, with the exception that the clock cleaner input runs at 1.8 V, then 3.3 V → 1.8 V voltage translation is required between voutx_clk and the clock cleaner input. An example of this configuration is processor and FPD-Link interfaces operating at 3.3 V with CDCE813 operating at 1.8 V input and 3.3 V output.

Other combinations of transmitter/receiver IO voltages are not covered in this document, but special care should be taken to ensure IO voltage compatibility for those configurations.

6.4.1 Special Considerations When Using a Voltage Level Translator

Voltage level translators affect both the signal shape and delay of the signal they are translating. Additional work is required to ensure that these affects do not degrade the performance of the video interface.

Since voltage level translators can affect the signal shape, special care should be taken when including them in a system. Signal integrity simulations and measurements are recommended to ensure that clean clock edges and voltage thresholds are maintained.

Voltage level translators also add input-to-output delay to the signal they are translating. For details on accounting for this delay in a timing analysis, see Section 6.6.

6.4.2 Voltage Level Translator Options

6.4.2.1 NXP 74CBTLVD3245

The NXP 74CBTLVD3245 is a level-shifting bus switch that can be used to translate a signal from 3.3 V to 1.8 V. For details on using the 74CBTLVD3245 to translate from 3.3 V to 1.8 V, see Table 6.

Table 6. 74CBTLVD3245 Recommended Connections for 3.3 V to 1.8 V Translation

74CBTLVD3245 Pin	Recommended Connection
Ax	50Ω pull-up to 1.8 V and clock cleaner clock input
Bx	Processor (voutx_clk)
OEn	GND
VCC	3.3 V (plus decoupling)

6.4.2.2 Texas Instruments LSF0102

The Texas Instruments LSF0102 is a level translator that can be used to translate a signal from 3.3 V to 1.8 V. For details on using the LSF0102 to translate from 3.3 V to 1.8 V, see Table 7.

Table 7. LSF0102 Recommended Connections for 3.3 V to 1.8 V Translation

74CBTLVD3245 Pin	Recommended Connection
Ax	1kΩ pull-up to 1.8 V and clock cleaner clock input
Bx	Processor (voutx_clk)
Vref_A	1.8 V
Vref_B	200 kΩ pull-up to 3.3 V and decoupling and short to EN
EN	Short to Vref_B

6.4.2.3 Texas Instruments CDCE813 With 50 Ω Termination on Y1 Output

The Texas Instruments CDCE813 output interface operates at 3.3 V. Instead of using an active level translator on the output, 50 Ω termination to GND at the Serializer (PCLK) input can be used to level shift down to 1.8 V. This technique will not affect signal integrity or input-to-output delay in any significant way.

6.5 Clock Cleaner Output Enable Considerations

Some clock cleaners, such as the CDCE813, can automatically generate an output clock even before an input clock is present. When the input clock is then applied to the clock cleaner, the output of the clock cleaner changes to match the input clock frequency. When this occurs, the FPD-Link Deserializer Equalizer should be reset as described in Section 5.

6.6 Clock Cleaner IO Timing Impacts

The setup time and hold time requirements of the FPD-Link serializer must be met to ensure proper data transmission. When clock cleaners and voltage level translators are added into a system, it changes the propagation delay of the clock signal relative to the control and data signals.

Changes to the clock-to-data and control delay time have the potential to cause setup and hold time violations at the FPD-Link inputs. These violations can manifest themselves as unwanted visual artifacts such as dots, lines, color shifts, and out-of-place pixels. To avoid these issues, an interface timing analysis should be performed that includes the delay effects of the clock cleaners and voltage level translators.

To perform the interface timing analysis, timing specifications for each component of the interface should be extracted from the device-specific data sheets.

6.6.1 Processor Timing Specifications

The timing specifications for the processor video output port can be found in the following two data sheet tables:

- DPI Video Output i (i = 1..3) Default Switching Characteristics
- DPI Video Output i (i = 1..3) Alternate Switching Characteristics

You can select between the above two sets of Switching Characteristics by programming the desired virtual or manual IO mode listed in the Modes Summary table in the device-specific data sheet. The recommended Switching Characteristics to use depends on whether a clock cleaner is used in the system. Default Switching Characteristics should be used if there is no clock cleaner in the system. Alternate Switching Characteristics should be used if the CDCE813 clock cleaner is in the system.

The key timing specifications from these tables are:

- Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid (MIN and MAX)
- Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid (MIN and MAX)
- Pulse duration, output pixel clock vouti_clk low/high (MIN)

CAUTION

The IOSETs defined in section “Display Subsystem – Video Output Ports” of the device-specific data sheet must be followed to ensure the timings specified in the Switching Characteristics tables. Non-standard combinations of clock/data/control pins are not supported and can result in setup/hold time violations.

6.6.2 FPD-Link Serializer Timing Specifications

The timing specifications for the FPD-Link serializer LVCMOS input port can be found in the following data sheet table:

- Switching Characteristics

The key timing specifications from this table are:

- Data Input Setup to PCLK
- Data Input Hold from PCLK

6.6.3 Clock Cleaner and Voltage Level Translator Timing Specifications

The key timing specification for clock cleaners and voltage level translators is:

- Input-to-output delay time (MIN and MAX)

Clock cleaners such as the CDCE813 can introduce several ns of input-to-output delay and input-to-output delay variation. If the clock cleaner’s nominal input-to-output delay is ~3 ns, as is the case with the CDCE813, it is recommended to use the processor “Alternate Timings” IO Mode that conforms to the timings specified in the “DPI Video Output i (i = 1..3) Alternate Switching Characteristics” table.

CAUTION

The input-to-output delay time specification in a given clock cleaner data sheet may not include the delay impacts of jitter removal. If not included, it is recommended to add margin to the input-to-output delay time specification to account for worst case jitter removal.

6.7 PCB Propagation Delays

The processor pixel clock and data/control signals should be skew matched to ± 10 pS, especially when including a clock cleaner. Achieving ± 5 pS matching can provide addition timing margin.

6.8 Example Interface Timing Analysis

This section provides example timing analysis formulas that can be used to check interface timing closure when using a clock cleaner and voltage level translator in a SerDes application.

The following formulas can be used to confirm timing closure when using a CDCE813 clock cleaner, voltage level translator, and processor alternate timings IO mode:

- ProcessorDelayMin > SerializerHoldMin – ProcessorPulseWidthMin + ClockCleanerDelayMax + LevelShifterDelayMax + SkewMatching
- ProcessorDelayMax < ProcessorPulseWidthMin - SerializerSetupMin + ClockCleanerDelayMin + LevelShifterDelayMin – SkewMatching

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (June 2017) to B Revision	Page
• Updates were made in Section 3.1.3.1.	6
• New Section 5 was added.	6
• Updates were made in Section 6.5.	10

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