*User's Guide*

# *Powering DRA821 with TPS6594-Q1 and LP8764-Q1*


**ABSTRACT**

This user's guide can be used as a guide for integrating the TPS6594-Q1 and LP8764-Q1 power management integrated circuits (PMICs) into a system powering the DRA821 processor.


## Table of Contents



## Trademarks

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# 1 Introduction

This user's guide defines the power distribution network (PDN) between the TPS6594-Q1 and LP8764-Q1 devices and the DRA821 processor. It describes the platform power resource connections, digital control connections, and PMIC sequencing settings to support the different processor state transitions. The PMIC default non-volatile memory (NVM) settings, internal state transitions, and power sequences are also defined in this document. This user's guide does not provide information about the electrical characteristics, external components, package, or the functionality of the PMICs or processor. For such information and the full register maps, refer to the datasheet for each device. In the event of any inconsistency between the official specification and any user's guide, application report, or other referenced material, the data sheet specification will be the definitive source.

# 2 Device Versions

There are different versions of the TPS6594-Q1 and LP8764-Q1 devices available with unique NVM settings to support different processor solutions. The unique NVM settings for each PMIC device are optimized per PDN design to support different processors, processing loads, SDRAM types, system functional safety levels, and end product features - such as low power modes, processor interface levels, SD Card, and so forth. The NVM settings can be distinguished using the TI_NVM_ID register. In this user guide, each PMIC device is distinguished by the TI orderable part number, TI_NVM_ID, and TI_NVM_REV values listed in Table 2-1.

**Table 2-1. TPS6594-Q1 and LP8764-Q1 NVM Settings and Orderable Part Numbers**

| PDN USE CASE | Orderable Part Number | Device Mode | TI_NVM_ID(1) | TI_NVM_REV |
|---|---|---|---|---|
| • Up to 4.25 A(2) on the CORE rail<br>• Up to 4.25 A(2) on the CPU rails<br>• Up to 3.4 A(2) on the SDRAM, with support for LPDDR4<br>• Supports Functional Safety up to ASIL-D level<br>• Supports low power modes, including MCU-only, GPIO Retention, and DDR Retention states<br>• Supports I/O level of 3.3 V or 1.8 V<br>• Supports use of SD card | PTPS659414F4RWERQ1 | Master | 0xF4 | 0x3 |
| | P876441A1RQKRQ1 | Slave | 0xA1 | 0x3 |

(1) TPS6594-Q1 is currently on early silicon version 1.0. On this version of silicon, the NVM registers are identified as NVM_ID and NVM_REV.
(2) TI recommends having 15% margin between the maximum expected load current and the maximum current allowed per each PMIC output rail.

## 3 Processor Connections

This section details how the TPS6594-Q1 and LP8764-Q1 power resources and GPIO signals are connected to the processor and other peripheral components to support the PDN use case.

Figure 3-1 shows the detailed power mapping between the processor and the TPS6594-Q1 and LP8764-Q1 PMICs. In this configuration, both PMICs use a 3.3 V input voltage. For Functional Safety applications, there is a protection FET before VCCA that connects to the OVPGDRV pin of the master PMIC, allowing voltage monitoring of the input supply to the PMICs.

The VCCA voltage must be the first voltage applied to the PMIC devices. VIO_IN of the PMICs must be supplied after VCCA. In this configuration, VIO_IN is supplied by the load switch that also supplies the VDDSHVx_MCU voltage domain of the processor to allow the digital components of the PMIC devices (such as GPIOs) to remain supplied in MCU-only mode. Additionally, by controlling VIO_IN of both PMICs through this load switch, the system can also reduce power consumption in GPIO Retention or DDR Retention modes, since the load switch is disabled.

This PDN supports the use of either a single dual load switch (TPS22966-Q1) with an AEC-100 Grade 2 (-40 to +105°C) temperature rating or two single load switches (TPS22965-Q1) with an AEC-100 Grade 1 (-40 to +125°C) rating if a higher ambient temperature range is desired. It also includes a few optional discrete power components to support additional system functions that may be needed. The TLV70033-Q1 LDO is used to support compliant USB data eye performance by supplying a low noise 3.3 V for USB 2.0 interface integration. The TLV70018-Q1 LDO is available to support on-board EFUSE programming on high security SoC PNs. Alternative LDOs can be chosen for SD card dual-voltage I/O support (3.3 V and 1.8 V), TLV7103318-Q1 dual-voltage LDO can be used to enable compliant, dual voltage, high-speed SD card operations. If these system functions are not required, the power connection can be removed and the processor voltage domains will need to be grouped into alternative power rails.

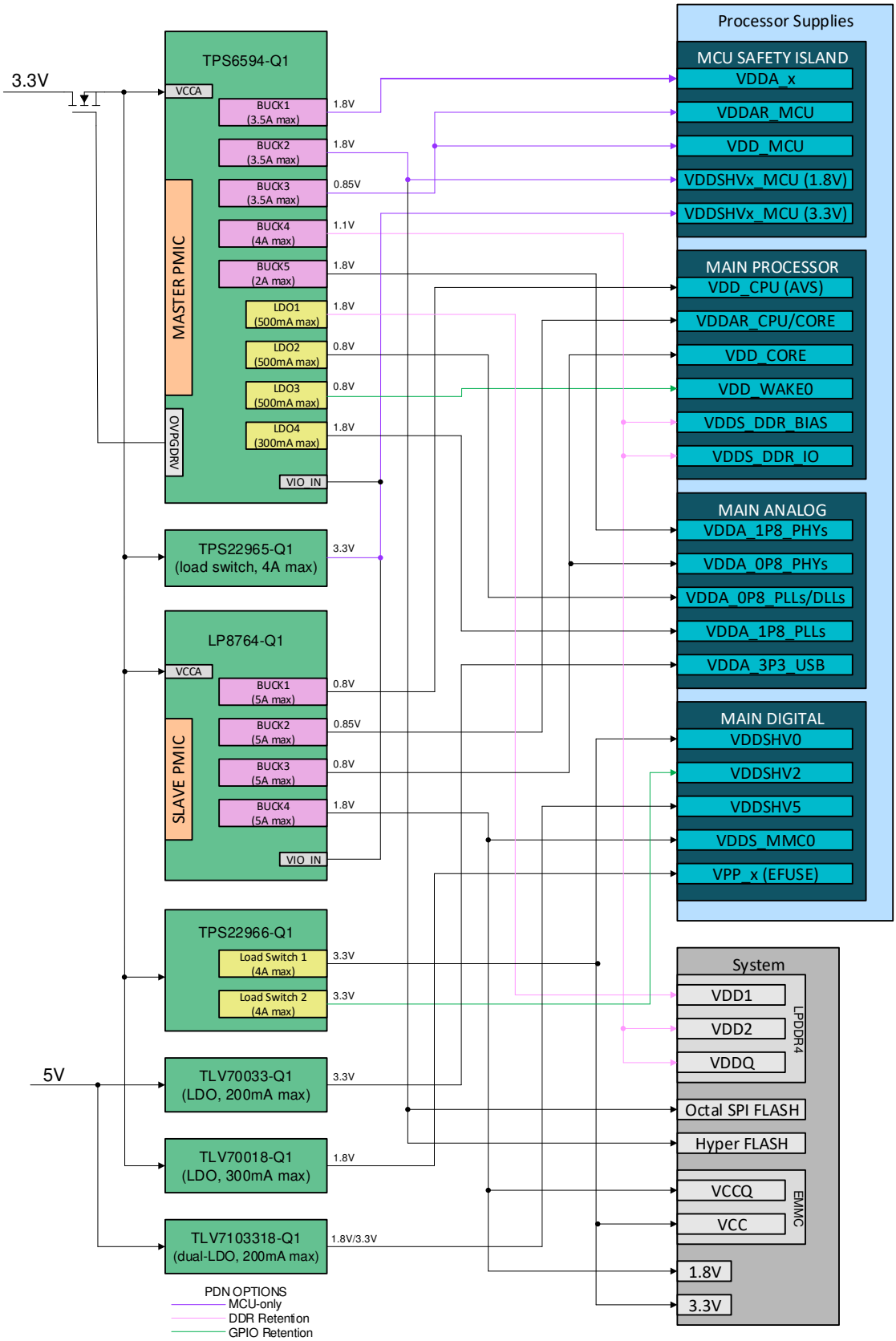


**Figure 3-1. TPS6594-Q1 and LP8764-Q1 Power Connections**

The power resource assignments shown in Figure 3-1 enable the support for different processor low-power modes, including MCU-only mode, GPIO Retention, and DDR Retention. Please use Table 3-1 as a guide to

understand which power resources are required to support different system features. If the system feature listed is not required, the power resource connection can be removed and the processor voltage domains will need to be grouped into alternative power rails.

**Table 3-1. Power Resources by System Power States**

| Device | PMIC Resource | Processor Domains | Power States | | | |
|---|---|---|---|---|---|---|
| | | | Active SoC | MCU - only | GPIO Retention | DDR Retention |
| TPS6594-Q1 | BUCK1 | VDDA_x | Required | Required | | |
| | BUCK2 | VDDSHVx_MCU (1.8V) | Required | Required | | |
| | BUCK3 | VDD_MCU, VDDAR_MCU | Required | Required | | |
| | BUCK4 | VDDS_DDR_BIAS, VDDS_DDR_IO | Required | | | Required |
| | BUCK5 | VDDA_1P8_PHYs | Required | | | |
| | LDO1 | N/A | Required | | | Required |
| | LDO2 | VDDA_0P8_PLLs/DLLs | Required | | | |
| | LDO3 | VDD_WAKE0 | Required | | Required | |
| | LDO4 | VDDA_1P8_PLLs | Required | | | |
| LP8764-Q1 | BUCK1 | VDD_CPU | Required | | | |
| | BUCK2 | VDDAR_CPU/CORE | Required | | | |
| | BUCK3 | VDD_CORE, VDDA_0P8_PHYs | Required | | | |
| | BUCK4 | VDDS_MMC0 | Required | | | |
| TPS22965-Q1 | Load Switch | VDDSHVx_MCU (3.3 V) | Required | Required | | |
| TPS22966-Q1 | Load Switch 1 | VDDSHV0(1) | Required | | | |
| | Load Switch 2 | VDDSHV2 | | | Required | |

(1) VDDSHV5 can also be powered by this rail if an SD card is not required in the system.

Figure 3-2 shows the digital control signal mapping between the processor and the PMIC devices. For the two PMIC devices to work together, the master PMIC and slave PMIC must establish an SPMI communication channel. This allows the TPS6594-Q1 and LP8764-Q1 to synchronize their internal Pre-Configurable State Machines (PFSM) so that they operate as one PFSM across all power and digital resources. The GPIO_5 and GPIO_6 pins on the TPS6594-Q1 and GPIO_8 and GPIO_9 pins on LP8764-Q1 are assigned for this functionality. In addition, the master PMIC's LDOVINT pin must be connected to the slave PMIC's ENABLE input (GPIO_4 of LP8764-Q1) to correctly initiate the PFSM.

Other digital connections from the TPS6594-Q1 devices to the processor allow support for error monitoring, processor reset, processor wake up, and system low-power modes. Specific GPIO pins have been assigned to key signals in order to ensure proper operation during low power modes when only a few GPIO pins will remain operational.

To support DDR retention low power mode, the following PMIC GPIO functions are required:

1. GPIO_2 and GPIO_3 of LP8764-Q1 connected to an external, low voltage latch to create a sustained control signal to DDR_RET of the processor. This is needed since the PMIC VIO_IN power rail supplying GPIO_2 and 3 will be disabled during DDR Retention state.
2. Sustained GPIO_3 of TPS6594-Q1 connected to in-line load switch's enable input to control MCU's 3.3 V domain.
3. Sustained GPIO_4 of TPS6594-Q1 with NVM default function set as LP_WKUP1 and mask bit set high to avoid false triggering until CAN wakeup signal is armed. SW must properly arm CAN PHY so that wakeup signal is set low and unmask GPIO_4 before entering DDR Retention state.

Both GPIO_3 and GPIO_4 of TPS6594-Q1 are powered by the VINT internal voltage domain of the PMIC. VINT remains powered in low power modes to keep these GPIOs sustained.

To support GPIO retention low power mode, the following PMIC GPIO functions are required:

1. Sustained GPIO_7 of LP8764-Q1 connected to in-line load switch's enable input to control processor's 3.3 V GPIO retention domain.

Additional digital options also include GPIO_10 of TPS6594-Q1, which can be configured by software as a 32 kHz clock output for the processor's oscillator input (LFOSC ). There is also the option to disable the watchdog timer using hardware, by pulling GPIO_8 of TPS6594-Q1 high. Lastly, the LP8764-Q1's GPIO_1 is included in the power up sequence to enable external regulators, for options such as DDR I/O.

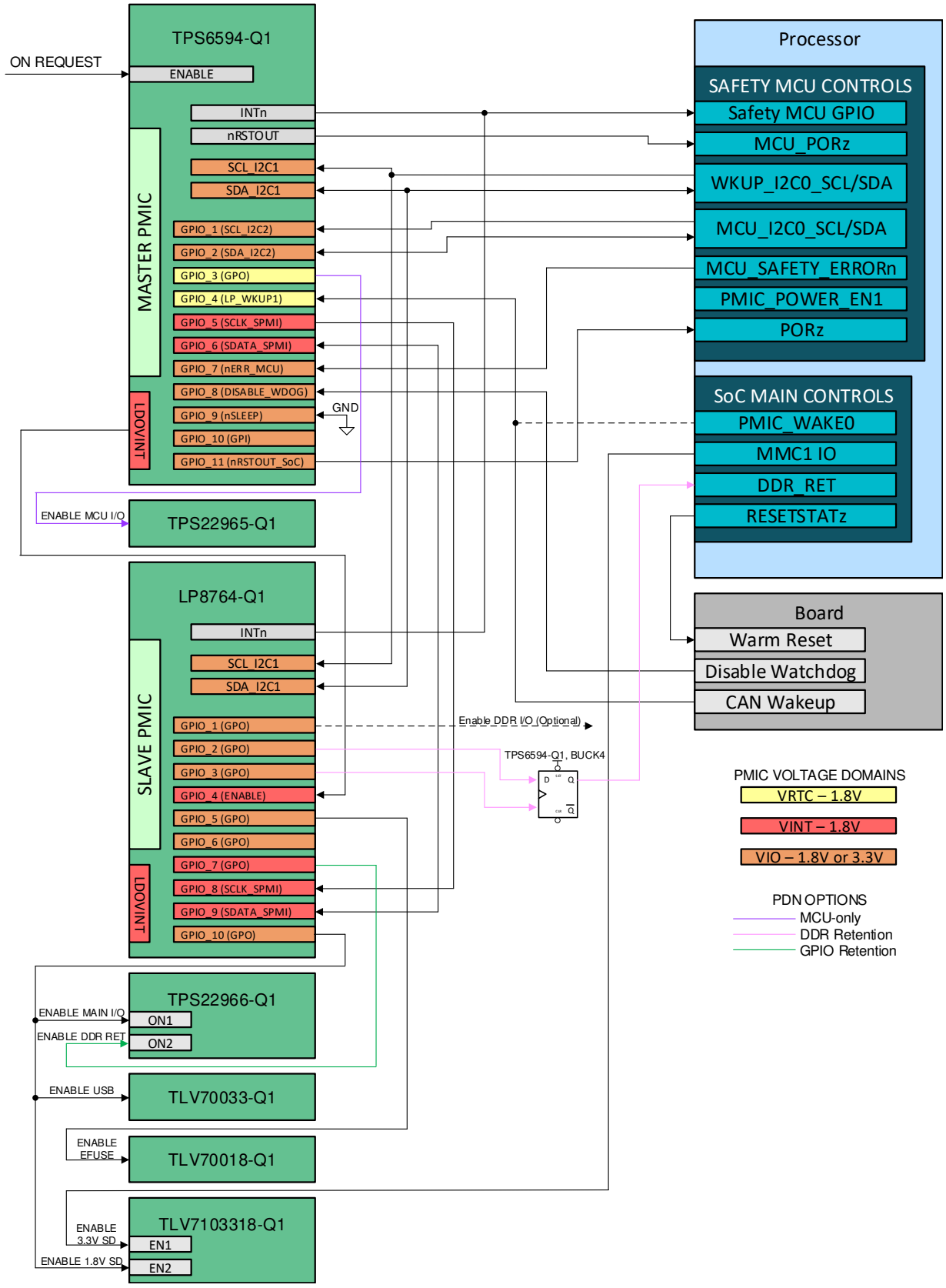


**Figure 3-2. TPS6594-Q1 and LP8764-Q1 Digital Connections**

The digital connections shown in Figure 3-2 allow system features including MCU-only mode, GPIO retention mode, DDR retention mode, and functional safety systems capable of supporting up to ASIL-D. Please use Table

3-2 as a guide to understand GPIO assignments required for these features. If the feature listed is not required, the digital connection can be removed. For details on how functional safety related connections help achieve functional safety system-level goals, see Section 4.

**Table 3-2. Digital Connections by System Feature**

| Device | PMIC Digital Signal | System Digital Signal | System Features | | | | |
|---|---|---|---|---|---|---|---|
| | | | Active SoC | Funtional Safety | MCU - only | GPIO Retention | DDR Retention |
| TPS6594-Q1 | nPWRON/ ENABLE | System ON Request | Required | | | | |
| | INT(1) | Safety MCU GPIO | | Required | | | |
| | nRSTOUT(1) | MCU_PORz | Required | | Required | | |
| | SCL_I2C1 | WKUP_I2C0_SCL | Required | | | | |
| | SDA_I2C1 | WKUP_I2C0_SDA | Required | | | | |
| | GPIO_1 | MCU_I2C0_SCL | | Required | | | |
| | GPIO_2 | MCU_I2C0_SCL | | Required | | | |
| | GPIO_3 | Enable MCU I/O | Required | | | | |
| | GPIO_4(2) | CAN Wakeup | | | | Required | Required |
| | GPIO_5 | PMIC SPMI CLK | Required | | | | |
| | GPIO_6 | PMIC SPMI DATA | Required | | | | |
| | GPIO_7 | MCU_SAFETY_ERRORn | | Required | | | |
| | GPIO_8(6) | Disable Watchdog | (3) | (3) | | | |
| | GPIO_9 | Ground(4) | Required | | | | |
| | GPIO_10(5) | WKUP_LFOSC0 | Required | | | | |
| | GPIO_11(1) | PORz | | Required | Required | | |
| LP8764-Q1 | INT(1) | Safety MCU GPIO | | Required | | | |
| | SCL_I2C1 | WKUP_I2C0_SCL | Required | | | | |
| | SDA_I2C1 | WKUP_I2C0_SDA | Required | | | | |
| | GPIO_1 | Enable DDR I/O (Optional) | | | | | |
| | GPIO_2(6) | External Latch Data Input | | | | | Required |
| | GPIO_3(6) | External Latch Clock Input | | | | | Required |
| | GPIO_4 | TPS6594-Q1 LDOVINT | Required | | | | |
| | GPIO_5(6) | Enable EFUSE | | | | | |
| | GPIO_6(6) | N/A | | | | | |
| | GPIO_7 | Enable DDR Retention | | | | Required | |
| | GPIO_8 | PMIC SPMI CLK | Required | | | | |
| | GPIO_9 | PMIC SPMI DATA | Required | | | | |
| | GPIO_10 | Enable Main I/O | | | Required | Required | Required |

(1) This pin is open-drain to enable voltage translation to correct voltage level for processor interface.
(2) Software must unmask GPIO_4 before the system expects to trigger a wakeup on this pin.
(3) If it is desired to disable the watchdog through hardware, GPIO_8 is required and must be set high by the time nRSTOUT goes high. After nRSTOUT is high, the watchdog state is latched and the pin can be configured for other functions through software.
(4) The GPIO_9 must be grounded when using 1.0 silicon of TPS6594-Q1.
(5) GPIO_10 is set as a general purpose input (GPI) by default to allow processor to boot up before sourcing the 32 kHz to the processor, since both bootmode and low frequency clock inputs to the processor utilize the same pin.
(6) This GPIO is not required for power sequencing or PMIC functionality and can be configured by software for a different purpose if desired.

# 4 Supporting Functional Safety Systems

By using the TPS6594-Q1 and LP8764-Q1 solution to power the DRA821 processor, the system can leverage the following PMIC functional safety features:

- Independent Power Control of MCU and Main Rails
- Independent Monitoring and Reset for MCU and Main Rails
- Input Supply Monitoring
- Output Voltage and Current Monitoring
- Question & Answer Watchdog
- Fault Reporting Interrupts
- Enable Drive Pin that provides an independent path to disable system actuators
- Error Pin Monitoring
- Internal Diagnostics including voltage monitoring, temperature monitoring, and Built-In Self-Test

Refer to the Safety Manuals of the TPS6594-Q1 and LP8764-Q1 devices for full descriptions and analysis of the PMIC functional safety features. These functional safety features can assist in achieving up to ASIL-D rating for a system. Additionally, these features help in achieving the functional safety assumptions utilized by the processor to achieve up to ASIL-D rating. See the DRA821 Safety Manual for Jacinto™ 7 Processors for a complete list of functional safety system assumptions.

## 4.1 Achieving ASIL-B System Requirements

To achieve a system functional safety level of ASIL-B, the following PDN features are available:

- PMIC over voltage and under voltage monitoring on the output power rails
- PMIC over-voltage monitoring and protection on the input to the PMIC (VCCA)
- Watchdog monitoring of safety processor
- MCU error monitoring
- MCU reset
- I2C communication
- Error indicator for driving external circuitry (optional)

The PDN has an in-line, external power FET between the input supply and PMICs. This FET can quickly isolate the PMICs when an over-voltage event greater than 6 V is detected on the input supply to protect the system from being damaged, as shown in Figure 3-1. Note that any power rail connected after the FET can be protected from an over voltage event. Any power connected upstream from the FET is not protected from over voltage events. In Figure 3-1 the load switches that supply power to the MCU and Main I/O domains and the discrete buck supplying the DDR are all connected after the FET to extend the over voltage protection to these processor domains and discrete power resoures.

The PMIC internal over voltage and under voltage monitoring and their respective monitoring threshold levels can be enabled through I2C after startup. To monitor the load switch voltage that supplies the MCU I/O of the processor, it is recommended to use the processor's POK monitor built into the VDDSHV0_MCU voltage domain.

The PMIC's Internal Q&A Watchdog is enabled by default on the TPS6594-Q1 device. Once the device is in ACTIVE state, the trigger or Q&A watchdog settings can be configured through the secondary I2C in the device. The steps for configuring the watchdog settings can be found in the TPS6594-Q1 datasheet. Setting the DISABLE_WDOG signal high on TPS6594-Q1 GPIO_8 will disable the watchdog timer if this feature needs to be suspended or is not required in the system.

GPIO_7 of the TPS6594-Q1 PMIC is configured as the MCU error signal monitoring, but will need to be enabled though the ESM_MCU_EN register bit. MCU reset is supported through the connection between the master PMIC nRSTOUT pin and the MCU_PORz of the processor. Lastly, there are 2 I2C ports between the TPS6594-Q1 and the processor which allows the watchdog monitoring to be on an independent communication channel.

There is an option to use the TPS6594-Q1 PMIC's EN_DRV to indicate an error has been detected and the system is entering SAFE state. This signal can be utilized if the system has some additional external circuitry that needs to be driven by an error event. In this PDN, the EN_DRV is not utilized, but available if needed.

### 4.2 Achieving up to ASIL-D System Requirements

For ASIL-C or ASIL-D systems, there are additional features to the ones described in Section 4.1 that can be utilized. These features include:

- PMIC current monitoring on all output power rails
- Isolation of the MCU and Main power domains of the processor
- SoC reset

The current monitoring is enabled by default for all BUCKs and LDOs for the TPS6594-Q1 and LP8764-Q1 devices. Additionally, Figure 3-1 shows that the MCU domain of the processor is powered by different power resources of the PMICs than the main power domain of the processor. SoC reset functionality is supported through the connection of GPIO_11 on TPS6594-Q1, configured as nRSTOUT_SoC, to the PORz pin of the processor.

**Note**

Residual voltage checking is available on the PMICs to prevent startup when output rails are not discharged below 100 mV as may happen under a fault condition. However, this feature is not enabled in the NVM settings of this PDN to support repetitive power cycling during system software development.

## 5 Static NVM Settings

The TPS6594-Q1 and LP8764-Q1 devices consist of fixed registers and configurable registers that are loaded from the NVM. For all NVM registers, the initial NVM settings that load into the registers are provided in this section. Note that these initial NVM settings can be changed during state transitions, such as moving from STANDBY to ACTIVE mode. The full register map, including default values of fixed registers, is located in the corresponding PMIC datasheet. Empty values indicate that the device does not have the register included. For example, LP8764-Q1 does not have BUCK5 registers at all and therefore the values for it are empty.

### 5.1 Application-Based Configuration Settings

In the LP8764-Q1 and TPS6594-Q1 datasheet, there are multiple application-based configurations for each BUCK to operate within. Table 5-1 includes the different configurations available:

**Table 5-1. LP8764-Q1 and TPS6594-Q1 Use Cases**

| TPS6594-Q1 | LP8764-Q1 |
|---|---|
| 2.2 MHz Single Phase for DDR Termination | 2.2 MHz Single Phase for DDR Termination |
| 4.4 MHz Multiphase Configuration | 4.4 MHz Multiphase Configuration |
| 4.4 MHz Single Phase Low Output Voltage | 4.4 MHz Single Phase Low Current |
| 4.4 MHz Single Phase High Output Voltage | 4.4 MHz Single Phase High Voltage |
| 2.2 MHz Multiphase with Full Range VIN | 2.2 MHz Multiphase with Full Range VIN |
| 2.2 MHz Single Phase with 5.0 V VIN | 2.2 MHz Single Phase with 5.0 V VIN |
| 2.2 MHz Single Phase with Full Range VIN | 2.2 MHz Single Phase with Full Range VIN |
| | 8.8 MHz Single Phase |

The seven configurations also have optimal output inductance values that optimize the performance of each buck under these various conditions. Table 5-2 shows the default configurations for the BUCKs. These settings cannot be changed after device startup.

**Table 5-2. Application Use Case Settings**

| Device | BUCK Rail | Default Application Use Case | Recommended Inductor Value |
|---|---|---|---|
| TPS6594-Q1 | BUCK1 | 4.4 MHz Multi-phase with Full Range VIN | 220 nH |
| | BUCK2 | 4.4 MHz Multi-phase with Full Range VIN | 220 nH |
| | BUCK3 | 4.4 MHz Multi-phase with Full Range VIN | 220 nH |
| | BUCK4 | 4.4 MHz Multi-phase with Full Range VIN | 220 nH |
| | BUCK5 | 4.4 MHz Multi-phase with Full Range VIN | 220 nH |
| LP8764-Q1 | BUCK1 | 4.4 MHz Multi-phase with Full Range VIN | 220 nH |
| | BUCK2 | 4.4 MHz Multi-phase with Full Range VIN | 220 nH |
| | BUCK3 | 4.4 MHz Multi-phase with Full Range VIN | 220 nH |
| | BUCK4 | 4.4 MHz Multi-phase with Full Range VIN | 220 nH |

## 5.2 Device Identification Settings

These settings are used to distinguish which device is detected in a system. These settings cannot be changed after device startup.

**Table 5-3. Device Identification NVM Settings**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| DEV_REV | SILICON_VERSION / SILICON_REV | | | | |
| | DEVICE_ID | 0x0 | 0x0 | 0x7 | 0x7 |
| NVM_CODE_1 | TI_NVM_ID | 0xf4 | 0xf4 | 0xa1 | 0xa1 |
| NVM_CODE_2 | TI_NVM_REV | 0x4 | 0x4 | 0x4 | 0x4 |
| PHASE_CONFIG | MP_CONFIG | 0x1 | 1+1+1+1+1 | 0x1 | 1+1+1+1 |

## 5.3 BUCK Settings

These settings detail the default voltages, configurations, and monitoring of the BUCK rails. All these settings can be changed though $I^2C$ after startup.

**Table 5-4. BUCK NVM Settings**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| BUCK1_CTRL | BUCK1_EN(1) | 0x0 | BUCK regulator is disabled | 0x0 | BUCK regulator is disabled. |
| | BUCK1_FPWM | 0x1 | Forced to PWM operation. | 0x1 | Forced to PWM operation. |
| | BUCK1_FPWM_MP | 0x0 | Automatic phase adding and shedding. | 0x0 | Automatic phase adding and shedding. |
| | BUCK1_VMON_EN | 0x0 | OV and UV comparators are disabled | 0x0 | OV, UV, SC and ILIM comparators are disabled. |
| | BUCK1_VSEL | 0x0 | BUCK1_VOUT_1 | 0x0 | BUCK1_VOUT_1 |
| | BUCK1_PLDN | 0x1 | Pull-down resistor enabled | 0x1 | Pull-down resistor is enabled. |
| | BUCK1_RV_SEL | 0x0 | Disabled | 0x0 | Disabled |
| BUCK1_CONF | BUCK1_SLEW_RATE | 0x3 | 5.0 mV/µs | 0x3 | 5.0 mV/µs |
| | BUCK1_ILIM | 0x5 | 5.5 A | 0x5 | 5.5 A |
| BUCK2_CTRL | BUCK2_EN(1) | 0x0 | BUCK regulator is disabled | 0x0 | BUCK regulator is disabled. |
| | BUCK2_FPWM | 0x1 | Forced to PWM operation. | 0x1 | Forced to PWM operation. |
| | BUCK2_VMON_EN | 0x0 | OV and UV comparators are disabled | 0x0 | OV, UV, SC, and ILIM comparators are disabled. |
| | BUCK2_VSEL | 0x0 | BUCK2_VOUT_1 | 0x0 | BUCK2_VOUT_1 |
| | BUCK2_PLDN | 0x1 | Pull-down resistor enabled | 0x1 | Pull-down resistor is enabled. |
| | BUCK2_RV_SEL | 0x0 | Disabled | 0x0 | Disabled |
| BUCK2_CONF | BUCK2_SLEW_RATE | 0x3 | 5.0 mV/µs | 0x3 | 5.0 mV/µs |
| | BUCK2_ILIM | 0x5 | 5.5 A | 0x5 | 5.5 A |
| BUCK3_CTRL | BUCK3_EN(1) | 0x0 | BUCK regulator is disabled | 0x0 | BUCK regulator is disabled. |
| | BUCK3_FPWM | 0x1 | Forced to PWM operation. | 0x1 | Forced to PWM operation. |
| | BUCK3_FPWM_MP | 0x0 | Automatic phase adding and shedding. | 0x0 | Automatic phase adding and shedding. |
| | BUCK3_VMON_EN | 0x0 | OV and UV comparators are disabled | 0x0 | OV, UV, SC, and ILIM comparators are disabled. |
| | BUCK3_VSEL | 0x0 | BUCK3_VOUT_1 | 0x0 | BUCK3_VOUT_1 |
| | BUCK3_PLDN | 0x1 | Pull-down resistor enabled | 0x1 | Pull-down resistor is enabled. |
| | BUCK3_RV_SEL | 0x0 | Disabled | 0x0 | Disabled |
| BUCK3_CONF | BUCK3_SLEW_RATE | 0x3 | 5.0 mV/µs | 0x3 | 5.0 mV/µs |
| | BUCK3_ILIM | 0x5 | 5.5 A | 0x5 | 5.5 A |
| BUCK4_CTRL | BUCK4_EN(1) | 0x0 | BUCK regulator is disabled | 0x0 | BUCK regulator is disabled. |
| | BUCK4_FPWM | 0x1 | Forced to PWM operation. | 0x1 | Forced to PWM operation. |
| | BUCK4_VMON_EN | 0x0 | OV and UV comparators are disabled | 0x0 | OV, UV, SC, and ILIM comparators are disabled. |
| | BUCK4_VSEL | 0x0 | BUCK4_VOUT_1 | 0x0 | BUCK4_VOUT_1 |
| | BUCK4_PLDN | 0x1 | Pull-down resistor enabled | 0x1 | Pull-down resistor is enabled. |
| | BUCK4_RV_SEL | 0x0 | Disabled | 0x0 | Disabled |
| BUCK4_CONF | BUCK4_SLEW_RATE | 0x3 | 5.0 mV/µs | 0x3 | 5.0 mV/µs |
| | BUCK4_ILIM | 0x5 | 5.5 A | 0x5 | 5.5 A |
| BUCK5_CTRL | BUCK5_EN(1) | 0x0 | BUCK regulator is disabled. | | |
| | BUCK5_FPWM | 0x1 | Forced to PWM operation. | | |
| | BUCK5_VMON_EN | 0x0 | OV and UV comparators are disabled. | | |
| | BUCK5_VSEL | 0x0 | BUCK5_VOUT_1 | | |
| | BUCK5_PLDN | 0x1 | Pull-down resistor enabled. | | |
| | BUCK5_RV_SEL | 0x0 | Disabled | | |

**Table 5-4. BUCK NVM Settings (continued)**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| BUCK5_CONF | BUCK5_SLEW_RATE | 0x3 | 5.0 mV/µs | | |
| | BUCK5_ILIM | 0x3 | 3.5 A | | |
| BUCK1_VOUT_1 | BUCK1_VSET1 | 0xb2 | 1.80 V | 0x37 | 0.800 V |
| BUCK1_VOUT_2 | BUCK1_VSET2 | 0x0 | 0.3 V | 0x0 | 0.3 V |
| BUCK2_VOUT_1 | BUCK2_VSET1 | 0xb2 | 1.80 V | 0x41 | 0.850 V |
| BUCK2_VOUT_2 | BUCK2_VSET2 | 0x0 | 0.3 V | 0x0 | 0.3 V |
| BUCK3_VOUT_1 | BUCK3_VSET1 | 0x41 | 0.850 V | 0x37 | 0.800 V |
| BUCK3_VOUT_2 | BUCK3_VSET2 | 0x0 | 0.3 V | 0x0 | 0.3 V |
| BUCK4_VOUT_1 | BUCK4_VSET1 | 0x73 | 1.10 V | 0xb2 | 1.80 V |
| BUCK4_VOUT_2 | BUCK4_VSET2 | 0x0 | 0.3 V | 0x0 | 0.3 V |
| BUCK5_VOUT_1 | BUCK5_VSET1 | 0xb2 | 1.80 V | | |
| BUCK5_VOUT_2 | BUCK5_VSET2 | 0x0 | 0.3 V | | |
| BUCK1_PG_WINDOW | BUCK1_OV_THR | 0x2 | +4% / +40 mV | 0x2 | +4% / +40 mV |
| | BUCK1_UV_THR | 0x2 | -4% / -40 mV | 0x2 | -4% / -40 mV |
| BUCK2_PG_WINDOW | BUCK2_OV_THR | 0x2 | +4% / +40 mV | 0x2 | +4% / +40 mV |
| | BUCK2_UV_THR | 0x2 | -4% / -40 mV | 0x2 | -4% / -40 mV |
| BUCK3_PG_WINDOW | BUCK3_OV_THR | 0x2 | +4% / +40 mV | 0x2 | +4% / +40 mV |
| | BUCK3_UV_THR | 0x2 | -4% / -40 mV | 0x2 | -4% / -40 mV |
| BUCK4_PG_WINDOW | BUCK4_OV_THR | 0x2 | +4% / +40 mV | 0x2 | +4% / +40 mV |
| | BUCK4_UV_THR | 0x2 | -4% / -40 mV | 0x2 | -4% / -40 mV |
| BUCK5_PG_WINDOW | BUCK5_OV_THR | 0x2 | +4% / +40 mV | | |
| | BUCK5_UV_THR | 0x2 | -4% / -40 mV | | |
| VMON1_PG_WINDOW | VMON1_RANGE | | | 0x0 | 0.3 - 3.34 V |
| | VMON1_UV_THR | | | 0x0 | -3% / -30 mV / (-150 mV) |
| | VMON1_OV_THR | | | 0x0 | +3% / +30 mV / (+150 mV) |
| VMON1_PG_LEVEL | VMON1_PG_SET | | | 0x0 | 0x0 |
| VMON2_PG_WINDOW | VMON2_RANGE | | | 0x0 | 0.3 - 3.34 V |
| | VMON2_UV_THR | | | 0x0 | -3% / -30 mV / (-150 mV) |
| | VMON2_OV_THR | | | 0x0 | +3% / +30mV / (+150 mV) |

(1) Note that this NVM default value can change when the device transitions to ACTIVE mode.

## 5.4 LDO Settings

These settings detail the default voltages, configurations, and monitoring of the LDO rails. All these settings can be changed though $I^2C$ after startup. Note that only TPS6594-Q1 device contains LDO outputs.

**Table 5-5. LDO NVM Settings**

| Register Name | Field Name | TPS6594-Q1 | |
|---|---|---|---|
| | | Value | Description |
| LDO1_CTRL | LDO1_EN(1) | 0x0 | LDO1 regulator is disabled. |
| | LDO1_PLDN | 0x2 | 250 Ω |
| | LDO1_VMON_EN | 0x0 | OV and UV comparators are disabled. |
| | LDO1_RV_SEL | 0x0 | Disabled |
| LDO2_CTRL | LDO2_EN(1) | 0x0 | LDO2 regulator is disabled. |
| | LDO2_PLDN | 0x1 | 125 Ω |
| | LDO2_VMON_EN | 0x0 | OV and UV comparators are disabled. |
| | LDO2_RV_SEL | 0x0 | Disabled |

**Table 5-5. LDO NVM Settings (continued)**

| Register Name | Field Name | TPS6594-Q1 | |
|---|---|---|---|
| | | Value | Description |
| LDO3_CTRL | LDO3_EN(1) | 0x0 | LDO3 regulator is disabled. |
| | LDO3_PLDN | 0x1 | 125 Ω |
| | LDO3_VMON_EN | 0x0 | OV and UV comparators are disabled. |
| | LDO3_RV_SEL | 0x0 | Disabled |
| LDO4_CTRL | LDO4_EN(1) | 0x0 | LDO4 regulator is disabled. |
| | LDO4_PLDN | 0x1 | 125 Ω |
| | LDO4_VMON_EN | 0x0 | OV and UV comparators are disabled. |
| | LDO4_RV_SEL | 0x0 | Disabled |
| LDOINT_CTRL | LDOINT_VMON_EN | 0x1 | OV and UV comparators are enabled. |
| LDORTC_CTRL | LDORTC_VMON_EN | 0x1 | OV and UV comparators are enabled. |
| LDO1_VOUT | LDO1_VSET | 0x1c | 1.80 V |
| | LDO1_BYPASS | 0x0 | LDO is set to linear regulator mode. |
| LDO2_VOUT | LDO2_VSET | 0x8 | 0.80 V |
| | LDO2_BYPASS | 0x0 | LDO is set to linear regulator mode. |
| LDO3_VOUT | LDO3_VSET | 0x8 | 0.80 V |
| | LDO3_BYPASS | 0x0 | LDO is set to linear regulator mode. |
| LDO4_VOUT | LDO4_VSET | 0x38 | 1.800 V |
| LDO1_PG_WINDOW | LDO1_OV_THR | 0x2 | +4% / +40 mV |
| | LDO1_UV_THR | 0x2 | -4% / -40 mV |
| LDO2_PG_WINDOW | LDO2_OV_THR | 0x2 | +4% / +40 mV |
| | LDO2_UV_THR | 0x2 | -4% / -40 mV |
| LDO3_PG_WINDOW | LDO3_OV_THR | 0x2 | +4% / +40 mV |
| | LDO3_UV_THR | 0x2 | -4% / -40 mV |
| LDO4_PG_WINDOW | LDO4_OV_THR | 0x2 | +4% / +40 mV |
| | LDO4_UV_THR | 0x2 | -4% / -40 mV |

(1) Note that this NVM default value can change when the device transitions to ACTIVE mode.

## 5.5 VCCA Settings

These settings detail the default monitoring enabled on VCCA. All these settings can be changed though $I^2C$ after startup.

**Table 5-6. VCCA NVM Settings**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| VCCA_VMON_CTRL | VMON_DEGLITCH_SEL | | | 0x0 | 4 µs |
| | VMON2_RV_SEL | | | 0x0 | Disabled |
| | VMON2_EN | | | 0x0 | OV and UV comparators are disabled. |
| | VMON1_RV_SEL | | | 0x0 | Disabled |
| | VMON1_EN | | | 0x0 | OV and UV comparators are disabled. |
| | VCCA_VMON_EN | 0x1 | OV and UV comparators are enabled. | 0x1 | OV and UV comparators are enabled. |
| VCCA_PG_WINDOW | VCCA_OV_THR | 0x7 | +10% | 0x7 | +10% |
| | VCCA_UV_THR | 0x7 | -10% | 0x7 | -10% |
| | VCCA_PG_SET | 0x0 | 3.3 V | 0x0 | 3.3 V |

## 5.6 GPIO Settings

These settings detail the default configurations of the GPIO rails. All these settings can be changed though $I^2C$ after startup. Note that the contents of the GPIOx_SEL field determine which other fields in the GPIOx_CONF and GPIO_OUT_x registers are applicable. To understand which NVM fields apply to each GPIOx_SEL option, see the *Digital Signal Descriptions* section in TPS6594-Q1 and LP8764-Q1 data sheets.

**Table 5-7. GPIO NVM Settings**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| GPIO1_CONF | GPIO1_OD | 0x0 | Push-pull output | 0x0 | Push-pull output |
| | GPIO1_DIR | 0x0 | Input | 0x1 | Output |
| | GPIO1_SEL | 0x1 | SCL_I2C2/CS_SPI | 0x0 | GPIO1 |
| | GPIO1_PU_SEL | 0x0 | Pull-down resistor is selected. | 0x0 | Pull-down resistor is selected. |
| | GPIO1_PU_PD_EN | 0x0 | Pull-up or pull-down resistor is disabled. | 0x0 | Pull-up or pull-down resistor is disabled. |
| | GPIO1_DEGLITCH_EN | 0x0 | No deglitch, only synchronization. | 0x0 | No deglitch, only synchronization. |
| GPIO2_CONF | GPIO2_OD | 0x0 | Push-pull output | 0x0 | Push-pull output |
| | GPIO2_DIR | 0x0 | Input | 0x1 | Output |
| | GPIO2_SEL | 0x2 | SDA_I2C2/SDO_SPI | 0x0 | GPIO2 |
| | GPIO2_PU_SEL | 0x0 | Pull-down resistor is selected. | 0x0 | Pull-down resistor is selected. |
| | GPIO2_PU_PD_EN | 0x0 | Pull-up or pull-down resistor is disabled. | 0x0 | Pull-up or pull-down resistor is disabled. |
| | GPIO2_DEGLITCH_EN | 0x0 | No deglitch, only synchronization. | 0x0 | No deglitch, only synchronization. |
| GPIO3_CONF | GPIO3_OD | 0x0 | Push-pull output | 0x0 | Push-pull output |
| | GPIO3_DIR | 0x1 | Output | 0x1 | Output |
| | GPIO3_SEL | 0x0 | GPIO3 | 0x0 | GPIO3 |
| | GPIO3_PU_SEL | 0x0 | Pull-down resistor is selected. | 0x0 | Pull-down resistor is selected. |
| | GPIO3_PU_PD_EN | 0x0 | Pull-up or pull-down resistor is disabled. | 0x0 | Pull-up or pull-down resistor is disabled. |
| | GPIO3_DEGLITCH_EN | 0x0 | No deglitch, only synchronization. | 0x0 | No deglitch, only synchronization. |
| GPIO4_CONF | GPIO4_OD | 0x0 | Push-pull output | 0x0 | Push-pull output |
| | GPIO4_DIR | 0x0 | Input | 0x0 | Input |
| | GPIO4_SEL | 0x6 | LP_WKUP1 | 0x1 | ENABLE |
| | GPIO4_PU_SEL | 0x0 | Pull-down resistor is selected. | 0x0 | Pull-down resistor is selected. |
| | GPIO4_PU_PD_EN | 0x1 | Pull-up/pull-down resistor enabled | 0x1 | Pull-up or pull-down resistor is enabled. |
| | GPIO4_DEGLITCH_EN | 0x1 | 10 µs deglitch time. | 0x1 | 8 µs deglitch time. |
| GPIO5_CONF | GPIO5_OD | 0x0 | Push-pull output | 0x0 | Push-pull output |
| | GPIO5_DIR | 0x0 | Input | 0x1 | Output |
| | GPIO5_SEL | 0x1 | SCLK_SPMI | 0x0 | GPIO5 |
| | GPIO5_PU_SEL | 0x0 | Pull-down resistor is selected. | 0x0 | Pull-down resistor is selected. |
| | GPIO5_PU_PD_EN | 0x0 | Pull-up or pull-down resistor is disabled. | 0x0 | Pull-up or pull-down resistor is disabled. |
| | GPIO5_DEGLITCH_EN | 0x0 | No deglitch, only synchronization. | 0x0 | No deglitch, only synchronization. |

**Table 5-7. GPIO NVM Settings (continued)**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| GPIO6_CONF | GPIO6_OD | 0x0 | Push-pull output | 0x0 | Push-pull output |
| | GPIO6_DIR | 0x0 | Input | 0x0 | Input |
| | GPIO6_SEL | 0x1 | SDATA_SPMI | 0x0 | GPIO6 |
| | GPIO6_PU_SEL | 0x0 | Pull-down resistor is selected. | 0x0 | Pull-down resistor is selected |
| | GPIO6_PU_PD_EN | 0x0 | Pull-up or pull-down resistor is disabled. | 0x1 | Pull-up or pull-down resistor is enabled. |
| | GPIO6_DEGLITCH_EN | 0x0 | No deglitch, only synchronization. | 0x1 | 8 µs deglitch time. |
| GPIO7_CONF | GPIO7_OD | 0x0 | Push-pull output | 0x0 | Push-pull output |
| | GPIO7_DIR | 0x0 | Input | 0x1 | Output |
| | GPIO7_SEL | 0x1 | NERR_MCU | 0x0 | GPIO7 |
| | GPIO7_PU_SEL | 0x0 | Pull-down resistor is selected. | 0x0 | Pull-down resistor is selected. |
| | GPIO7_PU_PD_EN | 0x1 | Pull-up or pull-down resistor is enabled. | 0x0 | Pull-up or pull-down resistor is disabled |
| | GPIO7_DEGLITCH_EN | 0x1 | 10 µs deglitch time. | 0x0 | No deglitch, only synchronization. |
| GPIO8_CONF | GPIO8_OD | 0x0 | Push-pull output | 0x0 | Push-pull output |
| | GPIO8_DIR | 0x0 | Input | 0x0 | Input |
| | GPIO8_SEL | 0x3 | DISABLE_WDOG | 0x1 | SCLK_SPMI |
| | GPIO8_PU_SEL | 0x0 | Pull-down resistor is selected. | 0x0 | Pull-down resistor is selected. |
| | GPIO8_PU_PD_EN | 0x1 | Pull-up or pull-down resistor is enabled. | 0x1 | Pull-up or pull-down resistor is enabled. |
| | GPIO8_DEGLITCH_EN | 0x1 | 10 µs deglitch time. | 0x0 | No deglitch, only synchronization. |
| GPIO9_CONF | GPIO9_OD | 0x0 | Push-pull output | 0x0 | Push-pull output |
| | GPIO9_DIR | 0x0 | Input | 0x0 | Input |
| | GPIO9_SEL | 0x4 | NSLEEP1 | 0x1 | SDATA_SPMI |
| | GPIO9_PU_SEL | 0x0 | Pull-down resistor is selected. | 0x0 | Pull-down resistor is selected. |
| | GPIO9_PU_PD_EN | 0x1 | Pull-up or pull-down resistor is enabled. | 0x1 | Pull-up or pull-down resistor is enabled. |
| | GPIO9_DEGLITCH_EN | 0x0 | No deglitch, only synchronization. | 0x0 | No deglitch, only synchronization. |
| GPIO10_CONF | GPIO10_OD | 0x0 | Push-pull output | 0x0 | Push-pull output |
| | GPIO10_DIR | 0x0 | Input | 0x1 | Output |
| | GPIO10_SEL | 0x0 | GPIO10 | 0x0 | GPIO10 |
| | GPIO10_PU_SEL | 0x0 | Pull-down resistor is selected. | 0x0 | Pull-down resistor is selected. |
| | GPIO10_PU_PD_EN | 0x1 | Pull-up or pull-down resistor is enabled. | 0x0 | Pull-up or pull-down resistor is disabled. |
| | GPIO10_DEGLITCH_EN | 0x0 | No deglitch, only synchronization. | 0x0 | No deglitch, only synchronization. |
| GPIO11_CONF | GPIO11_OD | 0x1 | Open-drain output | | |
| | GPIO11_DIR | 0x1 | Output | | |
| | GPIO11_SEL | 0x2 | NRSTOUT_SOC | | |
| | GPIO11_PU_SEL | 0x0 | Pull-down resistor is selected. | | |
| | GPIO11_PU_PD_EN | 0x0 | Pull-up or pull-down resistor is disabled. | | |
| | GPIO11_DEGLITCH_EN | 0x0 | No deglitch, only synchronization. | | |

**Table 5-7. GPIO NVM Settings (continued)**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| NPWRON_CONF | NPWRON_SEL | 0x0 | ENABLE | | |
| | ENABLE_PU_SEL | 0x0 | Pull-down resistor is selected. | | |
| | ENABLE_PU_PD_EN | 0x1 | Pull-up ir pull-down resistor is enabled. | | |
| | ENABLE_DEGLITCH_EN | 0x1 | 10 µs deglitch time when ENABLE, 50 ms deglitch time when NPWRON. | | |
| | ENABLE_POL | 0x0 | Active high | 0x0 | Active high |
| | NRSTOUT_OD | 0x1 | Open-drain output | | |
| GPIO_OUT_1 | GPIO1_OUT(1) | 0x0 | Low | 0x0 | Low |
| | GPIO2_OUT(1) | 0x0 | Low | 0x0 | Low |
| | GPIO3_OUT(1) | 0x0 | Low | 0x0 | Low |
| | GPIO4_OUT(1) | 0x0 | Low | 0x0 | Low |
| | GPIO5_OUT(1) | 0x0 | Low | 0x0 | Low |
| | GPIO6_OUT(1) | 0x0 | Low | 0x0 | Low |
| | GPIO7_OUT(1) | 0x0 | Low | 0x0 | Low |
| | GPIO8_OUT(1) | 0x0 | Low | 0x0 | Low |
| GPIO_OUT_2 | GPIO9_OUT(1) | 0x0 | Low | 0x0 | Low |
| | GPIO10_OUT(1) | 0x0 | Low | 0x0 | Low |
| | GPIO11_OUT(1) | 0x0 | Low | | |

(1) Note that this NVM default value can change when the device transitions to ACTIVE mode.

## 5.7 Finite State Machine (FSM) Settings

These settings describe how the PMIC output rails are assigned to various system-level states. Also, the default trigger for each system-level state is described. All these settings can be changed though $I^2C$ after startup.

**Table 5-8. FSM NVM Settings**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| RAIL_SEL_1 | BUCK1_GRP_SEL | 0x1 | MCU rail group | 0x2 | SOC rail group |
| | BUCK2_GRP_SEL | 0x1 | MCU rail group | 0x2 | SOC rail group |
| | BUCK3_GRP_SEL | 0x1 | MCU rail group | 0x2 | SOC rail group |
| | BUCK4_GRP_SEL | 0x1 | MCU rail group | 0x2 | SOC rail group |
| RAIL_SEL_2 | BUCK5_GRP_SEL | 0x2 | SOC rail group | | |
| | LDO1_GRP_SEL | 0x1 | MCU rail group | | |
| | LDO2_GRP_SEL | 0x2 | SOC rail group | | |
| | LDO3_GRP_SEL | 0x1 | MCU rail group | | |
| RAIL_SEL_3 | VMON2_GRP_SEL | | | 0x0 | No group assigned |
| | VMON1_GRP_SEL | | | 0x0 | No group assigned |
| | LDO4_GRP_SEL | 0x2 | SOC rail group | | |
| | VCCA_GRP_SEL | 0x1 | MCU rail group | 0x1 | MCU rail group |
| FSM_TRIG_SEL_1 | MCU_RAIL_TRIG | 0x2 | MCU power error | 0x2 | MCU power error |
| | SOC_RAIL_TRIG | 0x3 | SOC power error | 0x3 | SOC power error |
| | OTHER_RAIL_TRIG | 0x3 | SOC power error | 0x3 | SOC power error |
| | SEVERE_ERR_TRIG | 0x0 | Immediate shutdown | 0x0 | Immediate shutdown |
| FSM_TRIG_SEL_2 | MODERATE_ERR_TRIG | 0x1 | Orderly shutdown | 0x1 | Orderly shutdown |

## 5.8 Interrupt Settings

These settings detail the default configurations for what is monitored by nINT pin. All these settings can be changed though $I^2C$ after startup.

**Table 5-9. Interrupt NVM Settings**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| FSM_TRIG_MASK_1 | GPIO1_FSM_MASK | 0x1 | Masked | 0x1 | Masked |
| | GPIO1_FSM_MASK_POL | 0x0 | Masking sets the signal value to '0'. | 0x0 | Masking sets the signal value to '0'. |
| | GPIO2_FSM_MASK | 0x1 | Masked | 0x1 | Masked |
| | GPIO2_FSM_MASK_POL | 0x0 | Masking sets the signal value to '0'. | 0x0 | Masking sets the signal value to '0'. |
| | GPIO3_FSM_MASK | 0x1 | Masked | 0x1 | Masked |
| | GPIO3_FSM_MASK_POL | 0x0 | Masking sets the signal value to '0'. | 0x0 | Masking sets the signal value to '0'. |
| | GPIO4_FSM_MASK | 0x1 | Masked | 0x1 | Masked |
| | GPIO4_FSM_MASK_POL | 0x0 | Masking sets the signal value to '0'. | 0x0 | Masking sets the signal value to '0'. |
| FSM_TRIG_MASK_2 | GPIO5_FSM_MASK | 0x1 | Masked | 0x1 | Masked |
| | GPIO5_FSM_MASK_POL | 0x0 | Masking sets the signal value to '0'. | 0x0 | Masking sets the signal value to '0'. |
| | GPIO6_FSM_MASK | 0x1 | Masked | 0x1 | Masked |
| | GPIO6_FSM_MASK_POL | 0x0 | Masking sets the signal value to '0'. | 0x0 | Masking sets the signal value to '0'. |
| | GPIO7_FSM_MASK | 0x1 | Masked | 0x1 | Masked |
| | GPIO7_FSM_MASK_POL | 0x0 | Masking sets the signal value to '0'. | 0x0 | Masking sets the signal value to '0'. |
| | GPIO8_FSM_MASK | 0x1 | Masked | 0x1 | Masked |
| | GPIO8_FSM_MASK_POL | 0x0 | Masking sets the signal value to '0'. | 0x0 | Masking sets the signal value to '0'. |
| FSM_TRIG_MASK_3 | GPIO9_FSM_MASK | 0x1 | Masked | 0x1 | Masked |
| | GPIO9_FSM_MASK_POL | 0x0 | Masking sets the signal value to '0'. | 0x0 | Masking sets the signal value to '0'. |
| | GPIO10_FSM_MASK | 0x1 | Masked | 0x1 | Masked |
| | GPIO10_FSM_MASK_POL | 0x0 | Masking sets the signal value to '0'. | 0x0 | Masking sets the signal value to '0'. |
| | GPIO11_FSM_MASK | 0x1 | Masked | | |
| | GPIO11_FSM_MASK_POL | 0x0 | Masking sets the signal value to '0'. | | |
| MASK_BUCK1_2 | BUCK1_ILIM_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | BUCK1_OV_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | BUCK1_UV_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | BUCK2_ILIM_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | BUCK2_OV_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | BUCK2_UV_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| MASK_BUCK3_4 | BUCK3_ILIM_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | BUCK3_OV_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | BUCK3_UV_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | BUCK4_OV_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | BUCK4_UV_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | BUCK4_ILIM_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |

**Table 5-9. Interrupt NVM Settings (continued)**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| MASK_BUCK5 | BUCK5_ILIM_MASK | 0x1 | Interrupt is not generated. | | |
| | BUCK5_OV_MASK | 0x1 | Interrupt is not generated. | | |
| | BUCK5_UV_MASK | 0x1 | Interrupt is not generated. | | |
| MASK_LDO1_2 | LDO1_OV_MASK | 0x1 | Interrupt is not generated. | | |
| | LDO1_UV_MASK | 0x1 | Interrupt is not generated. | | |
| | LDO2_OV_MASK | 0x1 | Interrupt is not generated. | | |
| | LDO2_UV_MASK | 0x1 | Interrupt is not generated. | | |
| | LDO1_ILIM_MASK | 0x1 | Interrupt is not generated. | | |
| | LDO2_ILIM_MASK | 0x1 | Interrupt is not generated. | | |
| MASK_LDO3_4 | LDO3_OV_MASK | 0x1 | Interrupt is not generated. | | |
| | LDO3_UV_MASK | 0x1 | Interrupt is not generated. | | |
| | LDO4_OV_MASK | 0x1 | Interrupt is not generated. | | |
| | LDO4_UV_MASK | 0x1 | Interrupt is not generated. | | |
| | LDO3_ILIM_MASK | 0x1 | Interrupt is not generated. | | |
| | LDO4_ILIM_MASK | 0x1 | Interrupt is not generated. | | |
| MASK_VMON | VMON2_UV_MASK | | | 0x1 | Interrupt is not generated. |
| | VMON2_OV_MASK | | | 0x1 | Interrupt is not generated. |
| | VMON1_UV_MASK | | | 0x1 | Interrupt is not generated. |
| | VMON1_OV_MASK | | | 0x1 | Interrupt is not generated. |
| | VCCA_OV_MASK | 0x0 | Interrupt is generated. | 0x0 | Interrupt is generated. |
| | VCCA_UV_MASK | 0x0 | Interrupt is generated. | 0x0 | Interrupt is generated. |
| MASK_GPIO1_8_FALL | GPIO1_FALL_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO2_FALL_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO3_FALL_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO4_FALL_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO5_FALL_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO6_FALL_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO7_FALL_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO8_FALL_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| MASK_GPIO1_8_RISE | GPIO1_RISE_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO2_RISE_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO3_RISE_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO4_RISE_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO5_RISE_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO6_RISE_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO7_RISE_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO8_RISE_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| MASK_GPIO9_11 / MASK_GPIO9_10 | GPIO9_FALL_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO9_RISE_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO10_FALL_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO11_FALL_MASK | 0x1 | Interrupt is not generated. | | |
| | GPIO10_RISE_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | GPIO11_RISE_MASK | 0x1 | Interrupt is not generated. | | |

**Table 5-9. Interrupt NVM Settings (continued)**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| MASK_STARTUP | NPWRON_START_MASK | 0x1 | Interrupt is not generated. | | |
| | ENABLE_MASK | 0x0 | Interrupt is generated. | 0x0 | Interrupt is generated. |
| | FSD_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| MASK_MISC | TWARN_MASK | 0x0 | Interrupt is generated. | 0x0 | Interrupt is generated. |
| | BIST_PASS_MASK | 0x0 | Interrupt is generated. | 0x0 | Interrupt is generated. |
| | EXT_CLK_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| MASK_MODERATE_ERR | BIST_FAIL_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | REG_CRC_ERR_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | SPMI_ERR_MASK | 0x0 | Interrupt is generated. | 0x0 | Interrupt is generated. |
| | NPWRON_LONG_MASK | 0x1 | Interrupt is not generated. | | |
| | PFSM_ERR_MASK | 0x0 | Interrupt is generated. | 0x0 | Interrupt is generated |
| MASK_FSM_ERR | WD_MASK | | | 0x1 | Interrupt is not generated. |
| | IMM_SHUTDOWN_MASK | 0x0 | Interrupt is generated. | 0x0 | Interrupt is generated. |
| | MCU_PWR_ERR_MASK | 0x0 | Interrupt is generated. | 0x1 | Interrupt is not generated. |
| | SOC_PWR_ERR_MASK | 0x0 | Interrupt is generated. | 0x0 | Interrupt is generated. |
| | ORD_SHUTDOWN_MASK | 0x0 | Interrupt is generated. | 0x0 | Interrupt is generated. |
| MASK_COMM_ERR | COMM_FRM_ERR_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | COMM_CRC_ERR_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | COMM_ADR_ERR_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | I2C2_CRC_ERR_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | I2C2_ADR_ERR_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| MASK_READBACK_ERR | EN_DRV_READBACK_MASK | 0x0 | Interrupt is generated. | 0x1 | Interrupt is not generated. |
| | NINT_READBACK_MASK | 0x0 | Interrupt is generated. | 0x0 | Interrupt is generated. |
| | NRSTOUT_READBACK_ MASK | 0x0 | Interrupt is generated. | 0x1 | Interrupt is not generated. |
| | NRSTOUT_SOC_ READBACK_MASK | 0x0 | Interrupt is generated. | 0x1 | Interrupt is not generated. |
| MASK_ESM | ESM_SOC_PIN_MASK | 0x1 | Interrupt is not generated. | | |
| | ESM_SOC_RST_MASK | 0x1 | Interrupt is not generated. | | |
| | ESM_SOC_FAIL_MASK | 0x1 | Interrupt is not generated. | | |
| | ESM_MCU_PIN_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | ESM_MCU_RST_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |
| | ESM_MCU_FAIL_MASK | 0x1 | Interrupt is not generated. | 0x1 | Interrupt is not generated. |

## 5.9 POWERGOOD Settings

These settings detail the default configurations for what is monitored by PGOOD pin. All these settings can be changed though $I^2C$ after startup.

**Table 5-10. POWERGOOD NVM Settings**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| PGOOD_SEL_1 | PGOOD_SEL_BUCK1 | 0x0 | Masked | 0x0 | Masked |
| | PGOOD_SEL_BUCK2 | 0x0 | Masked | 0x0 | Masked |
| | PGOOD_SEL_BUCK3 | 0x0 | Masked | 0x0 | Masked |
| | PGOOD_SEL_BUCK4 | 0x0 | Masked | 0x0 | Masked |
| PGOOD_SEL_2 | PGOOD_SEL_BUCK5 | 0x0 | Masked | | |
| PGOOD_SEL_3 | PGOOD_SEL_LDO1 | 0x0 | Masked | | |
| | PGOOD_SEL_LDO2 | 0x0 | Masked | | |
| | PGOOD_SEL_LDO3 | 0x0 | Masked | | |
| | PGOOD_SEL_LDO4 | 0x0 | Masked | | |
| PGOOD_SEL_4 | PGOOD_SEL_VCCA | 0x0 | Masked | 0x0 | Masked |
| | PGOOD_SEL_VMON1 | | | 0x0 | Masked |
| | PGOOD_SEL_VMON2 | | | 0x0 | Masked |
| | PGOOD_SEL_TDIE_WARN | 0x0 | Masked | 0x0 | Masked |
| | PGOOD_SEL_NRSTOUT | 0x0 | Masked | 0x0 | Masked |
| | PGOOD_SEL_NRSTOUT_ SOC | 0x0 | Masked | 0x0 | Masked |
| | PGOOD_POL | 0x0 | PGOOD signal is high when monitored inputs are valid | 0x0 | PGOOD signal is high when monitored inputs are valid |
| | PGOOD_WINDOW | 0x1 | Both undervoltage and overvoltage are monitored | 0x0 | Only undervoltage is monitored |

## 5.10 Miscellaneous Settings

These settings detail the default configurations of additional settings, such as spread spectrum, BUCK frequency, and LDO timeout. All these settings can be changed though $I^2C$ after startup.

**Table 5-11. Miscellaneous NVM Settings**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| PLL_CTRL | EXT_CLK_FREQ | 0x1 | 2.2 MHz | 0x0 | 1.1 MHz |
| CONFIG_1 | TWARN_LEVEL | 0x0 | 120°C | 0x0 | 130°C |
| | I2C1_HS | 0x0 | Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode master code. | 0x0 | Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode master code. |
| | I2C2_HS | 0x0 | Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode master code. | 0x0 | Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode master code. |
| | EN_ILIM_FSM_CTRL | 0x0 | Buck/LDO regulators ILIM interrupts do not affect FSM triggers. | 0x0 | Buck regulators ILIM interrupts do not affect FSM triggers. |
| | NSLEEP1_MASK | 0x0 | NSLEEP1(B) affects FSM state transitions. | 0x1 | NSLEEP1(B) does not affect FSM state transitions. |
| | NSLEEP2_MASK | 0x0 | NSLEEP2(B) affects FSM state transitions. | 0x1 | NSLEEP2(B) does not affect FSM state transitions. |

**Table 5-11. Miscellaneous NVM Settings (continued)**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| CONFIG_2 | BB_CHARGER_EN | 0x0 | Disabled | | |
| | BB_VEOC | 0x0 | 2.5 V | | |
| | BB_ICHR | 0x0 | 100 µA | | |
| RECOV_CNT_REG_2 | RECOV_CNT_THR | 0xf | 0xf | 0xf | 0xf |
| BUCK_RESET_REG | BUCK1_RESET | 0x0 | 0x0 | 0x0 | 0x0 |
| | BUCK2_RESET | 0x0 | 0x0 | 0x0 | 0x0 |
| | BUCK3_RESET | 0x0 | 0x0 | 0x0 | 0x0 |
| | BUCK4_RESET | 0x0 | 0x0 | 0x0 | 0x0 |
| | BUCK5_RESET | 0x0 | 0x0 | | |
| SPREAD_SPECTRUM_1 | SS_EN | 0x0 | Spread spectrum disabled | 0x0 | Spread spectrum disabled |
| | SS_MODE | 0x1 | Mixed dwell | 0x1 | Mixed dwell |
| | SS_DEPTH | 0x0 | No modulation | 0x0 | No modulation |
| SPREAD_SPECTRUM_2 | SS_PARAM1 | 0x7 | 0x7 | 0x7 | 0x7 |
| | SS_PARAM2 | 0xc | 0xc | 0xc | 0xc |
| FREQ_SEL | BUCK1_FREQ_SEL | 0x1 | 4.4 MHz | 0x1 | 4.4 MHz |
| | BUCK2_FREQ_SEL | 0x1 | 4.4 MHz | 0x1 | 4.4 MHz |
| | BUCK3_FREQ_SEL | 0x1 | 4.4 MHz | 0x1 | 4.4 MHz |
| | BUCK4_FREQ_SEL | 0x1 | 4.4 MHz | 0x1 | 4.4 MHz |
| | BUCK5_FREQ_SEL | 0x1 | 4.4 MHz | | |
| FSM_STEP_SIZE | PFSM_DELAY_STEP | 0xb | 0xb | 0xb | 0xb |
| LDO_RV_TIMEOUT_REG_1 | LDO1_RV_TIMEOUT | 0xf | 16 ms | | |
| | LDO2_RV_TIMEOUT | 0xf | 16 ms | | |
| LDO_RV_TIMEOUT_REG_2 | LDO3_RV_TIMEOUT | 0xf | 16 ms | | |
| | LDO4_RV_TIMEOUT | 0xf | 16 ms | | |
| USER_SPARE_REGS | USER_SPARE_1 | 0x0 | 0x0 | 0x0 | 0x0 |
| | USER_SPARE_2 | 0x0 | 0x0 | 0x0 | 0x0 |
| | USER_SPARE_3 | 0x0 | 0x0 | 0x0 | 0x0 |
| | USER_SPARE_4 | 0x0 | 0x0 | 0x0 | 0x0 |
| ESM_MCU_MODE_CFG | ESM_MCU_EN | 0x0 | ESM_MCU disabled. MCU can set ENABLE_DRV bit to 1 if all other interrupt bits are cleared. | 0x0 | ESM_MCU disabled. MCU can set ENABLE_DRV bit to 1 if all other interrupt bits are cleared. |
| ESM_SOC_MODE_CFG | ESM_SOC_EN | 0x0 | ESM_SoC disabled. MCU can set ENABLE_DRV bit to 1 if all other interrupt bits are cleared. | | |
| RTC_CTRL_2 | XTAL_EN | 0x1 | Crystal oscillator is enabled | | |
| | LP_STANDBY_SEL | 0x1 | Low power standby state is used as standby state (LDOINT is disabled). | 0x0 | Normal standby state is used. |
| | FAST_BIST | 0x1 | Only analog BIST is run when transitioning from LP_STANDBY to ACTIVE state. | 0x1 | Only analog BIST is run at BOOT BIST. |
| | STARTUP_DEST | 0x3 | ACTIVE | 0x3 | ACTIVE |
| | XTAL_SEL | 0x1 | 9 pF | | |
| PFSM_DELAY_REG_1 | PFSM_DELAY1 | 0x54 | 0x54 | 0x0 | 0x0 |
| PFSM_DELAY_REG_2 | PFSM_DELAY2 | 0x0 | 0x0 | 0x0 | 0x0 |
| PFSM_DELAY_REG_3 | PFSM_DELAY3 | 0x0 | 0x0 | 0x0 | 0x0 |

**Table 5-11. Miscellaneous NVM Settings (continued)**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| PFSM_DELAY_REG_4 | PFSM_DELAY4 | 0x0 | 0x0 | 0x0 | 0x0 |

## 5.11 Interface Settings

These settings detail the default interface, interface configurations, and device addresses. These settings cannot be changed after device startup.

**Table 5-12. Interface NVM Settings**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| SERIAL_IF_CONFIG | I2C_SPI_SEL | 0x0 | I2C | 0x0 | I2C |
| | I2C1_SPI_CRC_EN | 0x0 | CRC disabled | 0x0 | CRC disabled |
| | I2C2_CRC_EN | 0x0 | CRC disabled | 0x0 | CRC disabled |
| I2C1_ID_REG | I2C1_ID | 0x48 | 0x48 | 0x4c | 0x4c |
| I2C2_ID_REG | I2C2_ID | 0x12 | 0x12 | 0x13 | 0x13 |

## 5.12 Multi-Device Settings

These settings detail whether the device is a operating as a master or slave in the system. These settings cannot be changed after device startup.

**Table 5-13. Multi-Device NVM Settings**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| SPMI_CONFIG_1 | SPMI_CRC_EN | 0x1 | SPMI CRC check is enabled. | 0x1 | SPMI CRC check is enabled. |
| | SPMI_MASTER_SEL | 0x1 | Master mode | 0x0 | Slave mode |
| | SPMI_CLK_SEL | 0x2 | 5 MHz | 0x2 | 5 MHz |
| SPMI_CONFIG_2 | SPMI_IF_SEL | 0x0 | Debugs feature and uses master logic to implement the logical slave. | 0x0 | Debug feature and uses master logic to implement logical slave. |
| | SPMI_RETRY_LIMIT | 0x3 | Three retries in case an error is detected. | 0x3 | Three retries in case of error detected. |
| | SPMI_SLAVE_ASR_HOLD | 0x0 | TBD | 0x0 | TBD |
| | SPMI_WD_AUTO_BOOT | 0x1 | SPMI auto boot is enabled. | 0x1 | SPMI auto boot is enabled. |
| | SPMI_EN | 0x1 | SPMI is enabled. | 0x1 | SPMI is enabled. |
| | SPMI_WD_EN | 0x1 | SPMI WD is enabled. | 0x1 | SPMI WD is enabled. |
| SPMI_CONFIG_3 | SPMI_WD_BOOT_INTERVAL | 0x8 | 0x8 | 0x8 | 0x8 |
| | SPMI_WD_RUNTIME_INTERVAL | 0x8 | 0x8 | 0x8 | 0x8 |
| SPMI_CONFIG_4 | SPMI_WD_RESPONSE_TIMEOUT | 0x8 | 0x8 | 0x8 | 0x8 |
| | SPMI_PFSM_RESPONSE_TIMEOUT | 0x8 | 0x8 | 0x8 | 0x8 |
| SPMI_CONFIG_5 | SPMI_WD_AUTO_BOOT_TIMEOUT | 0x8 | 0x8 | | |
| SPMI_CONFIG_6 | SPMI_BOOT_DELAY | 0x0 | 0x0 | | |
| SPMI_ID | SPMI_SID | 0x5 | 0x5 | 0x3 | 0x3 |
| | SPMI_MID | 0x0 | 0x0 | 0x0 | 0x0 |
| SLAVE_NVM_ID_1 | SLAVE1_NVM_ID | 0x5 | 0x5 | | |

**Table 5-13. Multi-Device NVM Settings (continued)**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| SLAVE_NVM_ID_2 | SLAVE2_NVM_ID | 0x33 | 0x33 | | |
| SLAVE_NVM_ID_3 | SLAVE3_NVM_ID | 0x0 | 0x0 | | |
| SLAVE_NVM_ID_4 | SLAVE4_NVM_ID | 0x0 | 0x0 | | |
| SLAVE_NVM_ID_5 | SLAVE5_NVM_ID | 0x0 | 0x0 | | |
| SLAVE_NVM_ID_6 | SLAVE6_NVM_ID | 0x0 | 0x0 | | |

## 5.13 Watchdog Settings

These settings detail the default watchdog addresses. These settings can be changed though $I^2C$ after startup.

**Table 5-14. Watchdog NVM Settings**

| Register Name | Field Name | TPS6594-Q1 | | LP8764-Q1 | |
|---|---|---|---|---|---|
| | | Value | Description | Value | Description |
| WD_THR_CFG | WD_EN | 0x1 | Watchdog enabled. MCU can set the ENABLE_DRV bit to 1 if: - watchdog is out of the Long Window - WD_FAIL_CNT[3:0] =< WD_FAIL_TH[2:0] - WD_FIRST_OK=1 - all other interrupt status bits are cleared. | 0x0 | Watchdog disabled. MCU can set the ENABLE_DRV bit to 1 if all other interrupt status bits are cleared. |

# 6 Pre-Configurable Finite State Machine (PFSM) Settings

This section describes the default PFSM settings of the TPS6594-Q1 and LP8764-Q1 devices. These settings cannot be changed after device startup.

## 6.1 Configured States

In this PDN, the following four power states are configured into the PMIC devices:

- Standby
- Active
- MCU Only
- Retention (both DDR and GPIO retention modes)

In Figure 6-1, the configured power states are described, along with the transition conditions required to move between configured states. Additionally, the transitions to hardware states, such as SAFE RECOVERY are described.

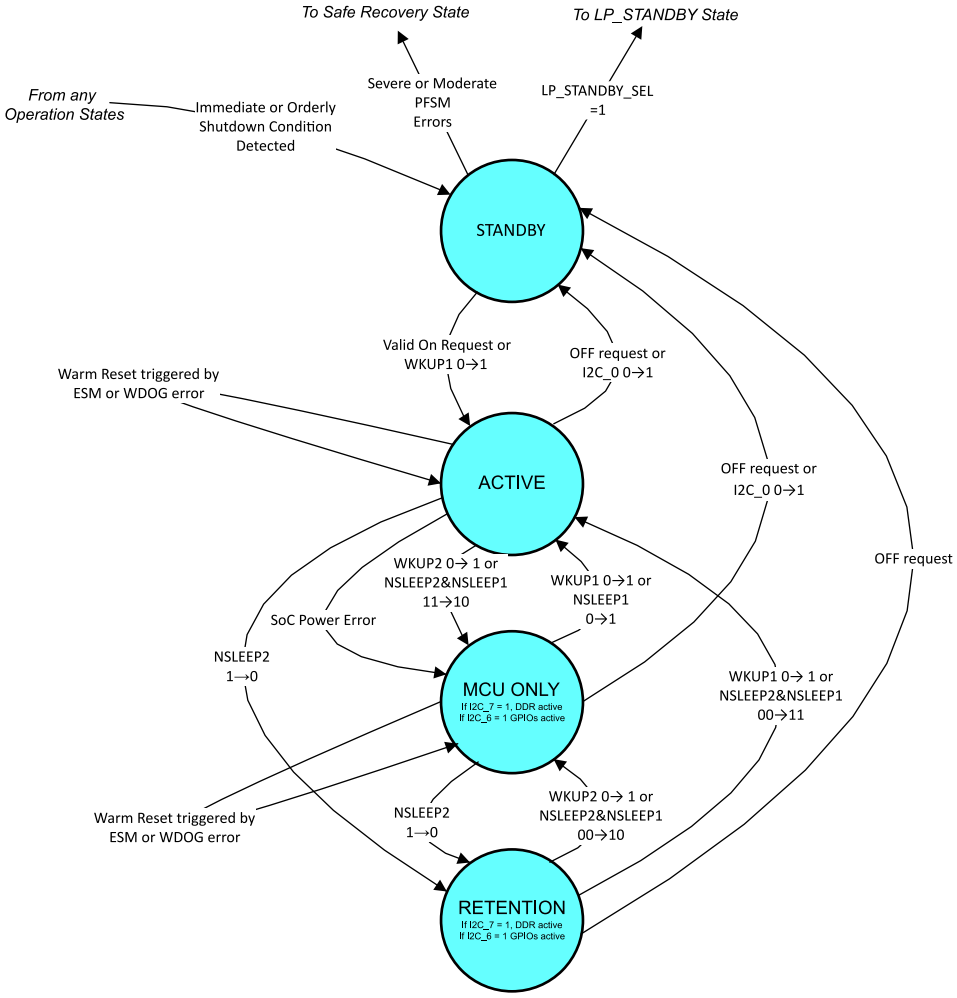


**Figure 6-1. Pre-Configurable State Machine (PFSM) States and Transitions**

The definition for each power state is described below:

**STANDBY** The PMICs are powered by a valid supply on the system power rail (VCCA > VCCA_UV) and waiting for a start-up event or condition. All device resources are powered down in the STANDBY state. EN_DRV is forced low in this state. The processor is in the Off State, no voltage domains are energized.

**ACTIVE** The PMICs are powered by a valid supply and have received a start-up event. The PMICs have full capacity to supply the processor and other platform modules. The processor has completed a recommended power up sequence with all voltage domains energized in both MCU & Main processor sections. MCU can now set the ENABLE_DRV bit high.

**MCU ONLY** The PMICs are powered by a valid supply. Only the power resources assigned to the processor's MCU rails are on or in a low power mode (LPM) depending on the specific resource setting. If a given resource is maintained active, then all linked subsystems are automatically maintained active. ENABLE_DRV bit can be set high by the MCU, or remains unchanged in this state.

**RETENTION (DDR or GPIO)** The PMICs are powered by a valid supply. Only the power resources assigned to the processor’s retention rails are on or in LPM depending on the specific resource setting. If a given resource is maintained active, then all linked subsystems are automatically maintained active. ENABLE_DRV bit is cleared by the device in this state. If the I2C_6 bit is set high in both PMICs, they will enter GPIO retention state. If the I2C_7 bit is set high in both PMICs, they will enter DDR retention state. These bits need to be set by I2C before a trigger for the retention state occurs.

## 6.2 State Transitions

As shown in Figure 6-1, there are various triggers that can enable a state transition between configured states and hardware states. Table 6-1 describes each trigger and its associated state transition from highest priority to lowest priority.

**Table 6-1. State Transition Triggers**

| Trigger | PFSM Current State | PFSM Destination State | Power Sequence Executed |
|---|---|---|---|
| Immediate Shutdown | STANDBY, ACTIVE, MCU ONLY, RETENTION | SAFE | TO_SAFE_SEVERE |
| MCU Power Error | STANDBY, ACTIVE, MCU ONLY, RETENTION | SAFE | TO_SAFE |
| Orderly Shutdown | STANDBY, ACTIVE, MCU ONLY, RETENTION | SAFE | TO_SAFE_ORDERLY |
| OFF Request | STANDBY, ACTIVE, MCU ONLY, RETENTION | STANDBY | TO_STANDBY |
| WDOG Error | ACTIVE | ACTIVE | WDOG_ERROR_ACTIVE |
| ESM MCU Error | ACTIVE | ACTIVE | ESM_ERROR |
| ESM SOC Error | ACTIVE | ACTIVE | |
| WDOG Error | MCU ONLY | MCU ONLY | WDOG_ERROR_MCU |
| ESM MCU Error | MCU ONLY | MCU ONLY | ESM_ERROR |
| SOC Power Error | ACTIVE | MCU ONLY | TO_MCU |
| I2C1 bit goes high | ACTIVE, MCU ONLY | No State Change | No Sequence, RUNTIME BIST executes |
| ON Request | STANDBY, ACTIVE, MCU ONLY, RETENTION | ACTIVE | TO_ACTIVE |
| WKUP1 goes high | STANDBY, ACTIVE, MCU ONLY, RETENTION | ACTIVE | |
| NSLEEP1 and NSLEEP2 are high(1) | STANDBY, ACTIVE, MCU ONLY, RETENTION | ACTIVE | |
| MCU ON Request | STANDBY, ACTIVE, MCU ONLY, RETENTION | MCU ONLY | TO_MCU |
| WKUP2 goes high | STANDBY, ACTIVE, MCU ONLY, RETENTION | MCU ONLY | |
| NSLEEP1 goes low and NSLEEP2 goes high(1) | ACTIVE, MCU ONLY, RETENTION | MCU ONLY | |
| NSLEEP1 goes low and NSLEEP2 goes low(1) | ACTIVE, MCU ONLY | RETENTION | TO_RETENTION |
| NSLEEP1 goes high and NSLEEP2 goes low(1) | ACTIVE, MCU ONLY | RETENTION | |
| I2C_0 bit goes high | STANDBY, ACTIVE, MCU ONLY | STANDBY | TO_STANDBY |

(1) NSLEEP1 and NSLEEP2 of the master PMIC can be accessed through GPIO pin or through a register bit. If either the register bit or the GPIO pin is pulled high, the NSLEEPx value will read as a *high* logic level.

## 6.3 Power Sequences

### 6.3.1 TO_SAFE_SEVERE and TO_SAFE

The immediate shutdown and MCU error events both cause the PMICs to shut down all rails without delay. However, the immediate shutdown (TO_SAFE_SEVERE) will disable the clocks and switching of the BUCKs first and rely on the pulldown resistors of the BUCKs and LDOs to discharge the rails. This is to prevent any damage of the PMICs in case of over voltage on VCCA or thermal shutdown. The MCU error (TO_SAFE) will keep the BUCKs switching until they are disabled. The sequence for these triggers is shown in Figure 6-2.

| Sequence Name | Device | Delay Diagram | Total Delay | Rail Name |
|---|---|---|---|---|
| nRSTOUT_SOC | TPS6594-Q1 | | 0 us | SOC_PORz_1V8 |
| nRSTOUT | TPS6594-Q1 | | 0 us | MCU_PORz_1V8 |
| GPIO1 | LP8764-Q1 | | 0 us | EXT_VDDR_IO |
| BUCK4 | TPS6594-Q1 | | 0 us | VDD_DDR_1V1 |
| BUCK2 | LP8764-Q1 | | 0 us | VDD_RAM_0V85 |
| LDO3 | TPS6594-Q1 | | 0 us | VDD_WK_0V8 |
| LDO2 | TPS6594-Q1 | | 0 us | VDA_DLL_0V8 |
| BUCK3 | LP8764-Q1 | | 0 us | VDD_CORE_0V8 |
| BUCK1 | LP8764-Q1 | | 0 us | VDD_CPU_AVS |
| BUCK3 | TPS6594-Q1 | | 0 us | VDD_MCU_0V85 |
| LDO4 | TPS6594-Q1 | | 0 us | VDA_PLL_1V8 |
| BUCK5 | TPS6594-Q1 | | 0 us | VDA_PHY_1V8 |
| BUCK4 | LP8764-Q1 | | 0 us | VDD_IO_1V8 |
| LDO1 | TPS6594-Q1 | | 0 us | VDD1_LPDDR4_1V8 |
| BUCK1 | TPS6594-Q1 | | 0 us | VDA_MCU_1V8 |
| BUCK2 | TPS6594-Q1 | | 0 us | VDD_MCUIO_1V8 |
| GPIO7 | LP8764-Q1 | | 0 us | GPIORET_LDSW |
| GPIO10 | LP8764-Q1 | | 0 us | 3V3IO_LDSW |
| GPIO3 | TPS6594-Q1 | | 0 us | MCUIO3V3_LDSW |

**Figure 6-2. TO_SAFE_SEVERE and TO_SAFE Sequence**

### 6.3.2 TO_SAFE_ORDERLY and TO_STANDBY

If a moderate error occurs, an orderly shutdown trigger will be generated. This will shutdown the PMICs using the processor's recommended power down sequence and then transition to SAFE state to allow the devices to restart and check if the error is still present.

If an OFF request occurs, such as the ENABLE pin of the TPS6594-Q1 device being pulled low, the same power down sequence will occur, except that the PMICs will remain in STANDBY state at the end, rather than going into SAFE state. The power sequence for both of these events is shown in Figure 6-3.

| Sequence Name | Device | Delay Diagram | Total Delay | Rail Name |
|---|---|---|---|---|
| nRSTOUT_SOC | TPS6594-Q1 | | 0 us | SOC_PORz_1V8 |
| nRSTOUT | TPS6594-Q1 | | 0 us | MCU_PORz_1V8 |
| GPIO1 | LP8764-Q1 | | 200 us | EXT_VDDR_IO |
| BUCK4 | TPS6594-Q1 | | 500 us | VDD_DDR_1V1 |
| BUCK2 | LP8764-Q1 | | 500 us | VDD_RAM_0V85 |
| LDO3 | TPS6594-Q1 | | 1000 us | VDD_WK_0V8 |
| LDO2 | TPS6594-Q1 | | 1000 us | VDA_DLL_0V8 |
| BUCK3 | LP8764-Q1 | | 1000 us | VDD_CORE_0V8 |
| BUCK1 | LP8764-Q1 | | 1000 us | VDD_CPU_AVS |
| BUCK3 | TPS6594-Q1 | | 1000 us | VDD_MCU_0V85 |
| LDO4 | TPS6594-Q1 | | 1500 us | VDA_PLL_1V8 |
| BUCK5 | TPS6594-Q1 | | 1500 us | VDA_PHY_1V8 |
| BUCK4 | LP8764-Q1 | | 1500 us | VDD_IO_1V8 |
| LDO1 | TPS6594-Q1 | | 1500 us | VDD1_LPDDR4_1V8 |
| BUCK1 | TPS6594-Q1 | | 1500 us | VDA_MCU_1V8 |
| BUCK2 | TPS6594-Q1 | | 1500 us | VDD_MCUIO_1V8 |
| GPIO7 | LP8764-Q1 | | 2000 us | GPIORET_LDSW |
| GPIO10 | LP8764-Q1 | | 2000 us | 3V3IO_LDSW |
| GPIO3 | TPS6594-Q1 | | 2000 us | MCUIO3V3_LDSW |

**Figure 6-3. TO_SAFE_ORDERLY and TO_STANDBY Sequence**

### 6.3.3 WDOG_ERROR_ACTIVE

In the event of a watchdog error, the nRSTOUT and nRSTOUT_SOC signals will be driven low and the recovery count will increment. Then, all BUCKs and LDOs will be reset to their default voltages. If no errors are present, the nRSTOUT and nRSTOUT_SOC signals will return to a high value and the PMICs will remain in ACTIVE state. Note that the GPIOs do not reset during the warm reset event. The sequence is shown in Figure 6-4.

| Sequence Name | Device | Delay Diagram | Total Delay | Rail Name |
|---|---|---|---|---|
| nRSTOUT_SOC | TPS6594-Q1 | | 0 us | SOC_PORz_1V8 |
| nRSTOUT | TPS6594-Q1 | | 0 us | MCU_PORz_1V8 |
| BUCK2 | TPS6594-Q1 | | 0 us | VDD_MCUIO_1V8 |
| BUCK1 | TPS6594-Q1 | | 0 us | VDA_MCU_1V8 |
| LDO1 | TPS6594-Q1 | | 0 us | VDD1_LPDDR4_1V8 |
| BUCK4 | LP8764-Q1 | | 0 us | VDD_IO_1V8 |
| BUCK5 | TPS6594-Q1 | | 0 us | VDA_PHY_1V8 |
| LDO4 | TPS6594-Q1 | | 0 us | VDA_PLL_1V8 |
| BUCK3 | TPS6594-Q1 | | 0 us | VDD_MCU_0V85 |
| BUCK1 | LP8764-Q1 | | 0 us | VDD_CPU_AVS |
| BUCK3 | LP8764-Q1 | | 0 us | VDD_CORE_0V8 |
| LDO2 | TPS6594-Q1 | | 0 us | VDA_DLL_0V8 |
| LDO3 | TPS6594-Q1 | | 0 us | VDD_WK_0V8 |
| BUCK2 | LP8764-Q1 | | 0 us | VDD_RAM_0V85 |
| BUCK4 | TPS6594-Q1 | | 0 us | VDD_DDR_1V1 |
| nRSTOUT | TPS6594-Q1 | | 1000 us | MCU_PORz_1V8 |
| nRSTOUT_SOC | TPS6594-Q1 | | 1000 us | SOC_PORz_1V8 |

**Figure 6-4. WDOG_ERROR_ACTIVE Sequence**

### 6.3.4 ESM_ERROR

In the event of an ESM error, the nRSTOUT signal will be driven low and then driven high again after 200 µs. There is no change to the power rails. The sequence is shown in Figure 6-5.

| Sequence Name | Device | Delay Diagram | Total Delay | Rail Name |
|---|---|---|---|---|
| nRSTOUT_SOC | TPS6594-Q1 | | 0 us | SOC_PORz_1V8 |
| nRSTOUT_SOC | TPS6594-Q1 | | 200 us | SOC_PORz_1V8 |

**Figure 6-5. ESM_ERROR Sequence**

### 6.3.5 WDOG_ERROR_MCU

In the event of an watchdog error while in MCU-only mode, the nRSTOUT signal will be driven low and the recovery count will increment. Then, all the BUCKs and LDOs that are active in MCU state will be reset to their default voltages. If no errors are present, then the nRSTOUT signal will return to a high logic value and the PMICs will remain in MCU state. Note that the GPIOs do not reset during the MCU warm reset event. The sequence is shown in Figure 6-6.

| Sequence Name | Device | Delay Diagram | Total Delay | Rail Name |
|---|---|---|---|---|
| nRSTOUT | TPS6594-Q1 | | 0 us | MCU_PORz_1V8 |
| BUCK2 | TPS6594-Q1 | | 0 us | VDD_MCUIO_1V8 |
| BUCK1 | TPS6594-Q1 | | 0 us | VDA_MCU_1V8 |
| LDO1 | TPS6594-Q1 | | 0 us | VDD1_LPDDR4_1V8 |
| BUCK3 | TPS6594-Q1 | | 0 us | VDD_MCU_0V85 |
| LDO3 | TPS6594-Q1 | | 0 us | VDD_WK_0V8 |
| BUCK4 | TPS6594-Q1 | | 0 us | VDD_DDR_1V1 |
| nRSTOUT | TPS6594-Q1 | | 1000 us | MCU_PORz_1V8 |

**Figure 6-6. WDOG_ERROR_MCU Sequence**

### 6.3.6 TO_MCU

Any event that triggers this sequence will allow all rails not powering the MCU domain of the processor to shutdown. It will then enable the MCU rails, in the event that they are not already active (such as the STANDBY to MCU case). If the I2C_6 bit is set high in both PMICs, they will retain the processor GPIOs while keeping the MCU active as shown in Figure 6-7. If the I2C_7 bit is set high in both PMICs, they will retain the SRAM while keeping the MCU active as shown in Figure 6-8. If both bits are set high in both devices, both GPIO and DDR rail will be retained while the MCU is active, as shown in Figure 6-9. Lastly, if both I2C6 and I2C7 are set low in both devices, only the MCU will remain active in this state as shown in Figure 6-10. These bits need to be set by I2C in both PMICs before a trigger for the retention state occurs.

| Sequence Name | Device | Delay Diagram | Total Delay | Rail Name |
|---|---|---|---|---|
| nRSTOUT_SOC | TPS6594-Q1 | | 0 us | SOC_PORz_1V8 |
| GPIO1 | LP8764-Q1 | | 200 us | EXT_VDDR_IO |
| BUCK4 | TPS6594-Q1 | | 500 us | VDD_DDR_1V1 |
| BUCK2 | LP8764-Q1 | | 500 us | VDD_RAM_0V85 |
| LDO2 | TPS6594-Q1 | | 1000 us | VDA_DLL_0V8 |
| BUCK3 | LP8764-Q1 | | 1000 us | VDD_CORE_0V8 |
| BUCK1 | LP8764-Q1 | | 1000 us | VDD_CPU_AVS |
| LDO4 | TPS6594-Q1 | | 1500 us | VDA_PLL_1V8 |
| BUCK5 | TPS6594-Q1 | | 1500 us | VDA_PHY_1V8 |
| BUCK4 | LP8764-Q1 | | 1500 us | VDD_IO_1V8 |
| LDO1 | TPS6594-Q1 | | 1500 us | VDD1_LPDDR4_1V8 |
| GPIO10 | LP8764-Q1 | | 2000 us | 3V3IO_LDSW |
| GPIO3 | TPS6594-Q1 | | 2000 us | MCU3V3IO_LDSW |
| GPIO7 | LP8764-Q1 | | 2000 us | GPIORET_LDSW |
| BUCK2 | TPS6594-Q1 | | 4000 us | VDD_MCUIO_1V8 |
| BUCK1 | TPS6594-Q1 | | 4000 us | VDA_MCU_1V8 |
| BUCK3 | TPS6594-Q1 | | 4500 us | VDD_MCU_0V85 |
| LDO3 | TPS6594-Q1 | | 4500 us | VDD_WK_0V8 |
| nRSTOUT | TPS6594-Q1 | | 14000 us | MCU_PORz |

**Figure 6-7. TO_MCU Sequence with I2C_6 = 1**

| Sequence Name | Device | Delay Diagram | Total Delay | Rail Name |
|---|---|---|---|---|
| nRSTOUT_SOC | TPS6594-Q1 | | 0 us | SOC_PORz_1V8 |
| BUCK2 | LP8764-Q1 | | 500 us | VDD_RAM_0V85 |
| LDO3 | TPS6594-Q1 | | 1000 us | VDD_WK_0V8 |
| LDO2 | TPS6594-Q1 | | 1000 us | VDA_DLL_0V8 |
| BUCK3 | LP8764-Q1 | | 1000 us | VDD_CORE_0V8 |
| BUCK1 | LP8764-Q1 | | 1000 us | VDD_CPU_AVS |
| LDO4 | TPS6594-Q1 | | 1500 us | VDA_PLL_1V8 |
| BUCK5 | TPS6594-Q1 | | 1500 us | VDA_PHY_1V8 |
| BUCK4 | LP8764-Q1 | | 1500 us | VDD_IO_1V8 |
| GPIO7 | LP8764-Q1 | | 2000 us | GPIORET_LDSW |
| GPIO10 | LP8764-Q1 | | 2000 us | 3V3IO_LDSW |
| GPIO3 | TPS6594-Q1 | | 2000 us | MCU3V3IO_LDSW |
| BUCK2 | TPS6594-Q1 | | 4000 us | VDD_MCUIO_1V8 |
| BUCK1 | TPS6594-Q1 | | 4000 us | VDA_MCU_1V8 |
| LDO1 | TPS6594-Q1 | | 4000 us | VDD1_LPDDR4_1V8 |
| BUCK3 | TPS6594-Q1 | | 4500 us | VDD_MCU_0V85 |
| BUCK4 | TPS6594-Q1 | | 5000 us | VDD_DDR_1V1 |
| GPIO1 | LP8764-Q1 | | 5500 us | EXT_VDDR_IO |
| nRSTOUT | TPS6594-Q1 | | 14000 us | MCU_PORz |

**Figure 6-8. TO_MCU Sequence with I2C_7 = 1**

| Sequence Name | Device | Delay Diagram | Total Delay | Rail Name |
|---|---|---|---|---|
| nRSTOUT_SOC | TPS6594-Q1 | | 0 us | SOC_PORz_1V8 |
| BUCK2 | LP8764-Q1 | | 500 us | VDD_RAM_0V85 |
| LDO2 | TPS6594-Q1 | | 1000 us | VDA_DLL_0V8 |
| BUCK3 | LP8764-Q1 | | 1000 us | VDD_CORE_0V8 |
| BUCK1 | LP8764-Q1 | | 1000 us | VDD_CPU_AVS |
| LDO4 | TPS6594-Q1 | | 1500 us | VDA_PLL_1V8 |
| BUCK5 | TPS6594-Q1 | | 1500 us | VDA_PHY_1V8 |
| BUCK4 | LP8764-Q1 | | 1500 us | VDD_IO_1V8 |
| GPIO10 | LP8764-Q1 | | 2000 us | 3V3IO_LDSW |
| GPIO3 | TPS6594-Q1 | | 2000 us | MCU3V3IO_LDSW |
| GPIO7 | LP8764-Q1 | | 2000 us | GPIORET_LDSW |
| BUCK2 | TPS6594-Q1 | | 4000 us | VDD_MCUIO_1V8 |
| BUCK1 | TPS6594-Q1 | | 4000 us | VDA_MCU_1V8 |
| LDO1 | TPS6594-Q1 | | 4000 us | VDD1_LPDDR4_1V8 |
| BUCK3 | TPS6594-Q1 | | 4500 us | VDD_MCU_0V85 |
| LDO3 | TPS6594-Q1 | | 4500 us | VDD_WK_0V8 |
| BUCK4 | TPS6594-Q1 | | 5000 us | VDD_DDR_1V1 |
| GPIO1 | LP8764-Q1 | | 5500 us | EXT_VDDR_IO |
| nRSTOUT | TPS6594-Q1 | | 14000 us | MCU_PORz |

**Figure 6-9. TO_MCU Sequence with I2C6 = 1 and I2C_7 = 1**

| Sequence Name | Device | Delay Diagram | Total Delay | Rail Name |
|---|---|---|---|---|
| nRSTOUT_SOC | TPS6594-Q1 | | 0 us | SOC_PORz_1V8 |
| GPIO1 | LP8764-Q1 | | 200 us | EXT_VDDR_IO |
| BUCK4 | TPS6594-Q1 | | 500 us | VDD_DDR_1V1 |
| BUCK2 | LP8764-Q1 | | 500 us | VDD_RAM_0V85 |
| LDO3 | TPS6594-Q1 | | 1000 us | VDD_WK_0V8 |
| LDO2 | TPS6594-Q1 | | 1000 us | VDA_DLL_0V8 |
| BUCK3 | LP8764-Q1 | | 1000 us | VDD_CORE_0V8 |
| BUCK1 | LP8764-Q1 | | 1000 us | VDD_CPU_AVS |
| LDO4 | TPS6594-Q1 | | 1500 us | VDA_PLL_1V8 |
| BUCK5 | TPS6594-Q1 | | 1500 us | VDA_PHY_1V8 |
| BUCK4 | LP8764-Q1 | | 1500 us | VDD_IO_1V8 |
| LDO1 | TPS6594-Q1 | | 1500 us | VDD1_LPDDR4_1V8 |
| GPIO7 | LP8764-Q1 | | 2000 us | GPIORET_LDSW |
| GPIO10 | LP8764-Q1 | | 2000 us | 3V3IO_LDSW |
| GPIO3 | TPS6594-Q1 | | 2000 us | MCU3V3IO_LDSW |
| BUCK2 | TPS6594-Q1 | | 4000 us | VDD_MCUIO_1V8 |
| BUCK1 | TPS6594-Q1 | | 4000 us | VDA_MCU_1V8 |
| BUCK3 | TPS6594-Q1 | | 4500 us | VDD_MCU_0V85 |
| nRSTOUT | TPS6594-Q1 | | 14000 us | MCU_PORz |

**Figure 6-10. TO_MCU Sequence with I2C6 = 0 and I2C_7 = 0**

### 6.3.7 TO_ACTIVE

When a trigger causes the TO_ACTIVE sequence to execute, all rails of the PMICs will power up in the processor's recommended power up sequence as shown in Figure 6-11.

| Sequence Name | Device | Delay Diagram | Total Delay | Rail Name |
|---|---|---|---|---|
| GPIO3 | TPS6594-Q1 | | 0 us | MCUIO3V3_LDSW |
| GPIO10 | LP8764-Q1 | | 0 us | 3V3IO_LDSW |
| GPIO7 | LP8764-Q1 | | 0 us | GPIORET_LDSW |
| BUCK2 | TPS6594-Q1 | | 2000 us | VDD_MCUIO_1V8 |
| BUCK1 | TPS6594-Q1 | | 2000 us | VDA_MCU_1V8 |
| LDO1 | TPS6594-Q1 | | 2000 us | VDD1_LPDDR4_1V8 |
| BUCK4 | LP8764-Q1 | | 2000 us | VDD_IO_1V8 |
| BUCK5 | TPS6594-Q1 | | 2000 us | VDA_PHY_1V8 |
| LDO4 | TPS6594-Q1 | | 2000 us | VDA_PLL_1V8 |
| BUCK3 | TPS6594-Q1 | | 2500 us | VDD_MCU_0V85 |
| BUCK1 | LP8764-Q1 | | 2500 us | VDD_CPU_AVS |
| BUCK3 | LP8764-Q1 | | 2500 us | VDD_CORE_0V8 |
| LDO2 | TPS6594-Q1 | | 2500 us | VDA_DLL_0V8 |
| LDO3 | TPS6594-Q1 | | 2500 us | VDD_WK_0V8 |
| BUCK2 | LP8764-Q1 | | 3000 us | VDD_RAM_0V85 |
| BUCK4 | TPS6594-Q1 | | 3000 us | VDD_DDR_1V1 |
| GPIO1 | LP8764-Q1 | | 3500 us | EXT_VDDR_IO |
| nRSTOUT | TPS6594-Q1 | | 12000 us | MCU_PORz_1V8 |
| nRSTOUT_SOC | TPS6594-Q1 | | 12000 us | SOC_PORz_1V8 |

**Figure 6-11. TO_ACTIVE Sequence**

### 6.3.8 TO_RETENTION

Any event that triggers this sequence will disable all power rails and GPIOs that are not supplying the retention rails. If the I2C_6 bit is set high in both PMICs, they will enter GPIO retention state as shown in Figure 6-12. If the I2C_7 bit is set high in both PMICs, they will enter DDR retention state as shown in Figure 6-13. If both bits are set, both GPIO and DDR rail will be retained, as shown in Figure 6-14. These bits need to be set by I2C in both PMICs before a trigger for the retention state occurs. If neither I2C6 or I2C7 are set high, the GPIOs and DDR will not remain active, as shown in Figure 6-15.

| Sequence Name | Device | Delay Diagram | Total Delay | Rail Name |
|---|---|---|---|---|
| nRSTOUT_SOC | TPS6594-Q1 | | 0 us | SOC_PORz_1V8 |
| nRSTOUT | TPS6594-Q1 | | 0 us | MCU_PORz |
| GPIO1 | LP8764-Q1 | | 200 us | EXT_VDDR_IO |
| BUCK4 | TPS6594-Q1 | | 500 us | VDD_DDR_1V1 |
| BUCK2 | LP8764-Q1 | | 500 us | VDD_RAM_0V85 |
| LDO2 | TPS6594-Q1 | | 1000 us | VDA_DLL_0V8 |
| BUCK3 | LP8764-Q1 | | 1000 us | VDD_CORE_0V8 |
| BUCK1 | LP8764-Q1 | | 1000 us | VDD_CPU_AVS |
| BUCK3 | TPS6594-Q1 | | 1000 us | VDD_MCU_0V85 |
| LDO4 | TPS6594-Q1 | | 1500 us | VDA_PLL_1V8 |
| BUCK5 | TPS6594-Q1 | | 1500 us | VDA_PHY_1V8 |
| BUCK4 | LP8764-Q1 | | 1500 us | VDD_IO_1V8 |
| LDO1 | TPS6594-Q1 | | 1500 us | VDD1_LPDDR4_1V8 |
| BUCK1 | TPS6594-Q1 | | 1500 us | VDA_MCU_1V8 |
| BUCK2 | TPS6594-Q1 | | 1500 us | VDD_MCUIO_1V8 |
| GPIO10 | LP8764-Q1 | | 2000 us | 3V3IO_LDSW |
| GPIO3 | TPS6594-Q1 | | 2000 us | MCU3V3IO_LDSW |

**Figure 6-12. TO_RETENTION Sequence, I2C6 = 1**

| Sequence Name | Device | Delay Diagram | Total Delay | Rail Name |
|---|---|---|---|---|
| nRSTOUT_SOC | TPS6594-Q1 | | 0 us | SOC_PORz_1V8 |
| nRSTOUT | TPS6594-Q1 | | 0 us | MCU_PORz |
| BUCK2 | LP8764-Q1 | | 500 us | VDD_RAM_0V85 |
| LDO3 | TPS6594-Q1 | | 1000 us | VDD_WK_0V8 |
| LDO2 | TPS6594-Q1 | | 1000 us | VDA_DLL_0V8 |
| BUCK3 | LP8764-Q1 | | 1000 us | VDD_CORE_0V8 |
| BUCK1 | LP8764-Q1 | | 1000 us | VDD_CPU_AVS |
| BUCK3 | TPS6594-Q1 | | 1000 us | VDD_MCU_0V85 |
| LDO4 | TPS6594-Q1 | | 1500 us | VDA_PLL_1V8 |
| BUCK5 | TPS6594-Q1 | | 1500 us | VDA_PHY_1V8 |
| BUCK4 | LP8764-Q1 | | 1500 us | VDD_IO_1V8 |
| BUCK1 | TPS6594-Q1 | | 1500 us | VDA_MCU_1V8 |
| BUCK2 | TPS6594-Q1 | | 1500 us | VDD_MCUIO_1V8 |
| GPIO7 | LP8764-Q1 | | 2000 us | GPIORET_LDSW |
| GPIO10 | LP8764-Q1 | | 2000 us | 3V3IO_LDSW |
| GPIO3 | TPS6594-Q1 | | 2000 us | MCU3V3IO_LDSW |

**Figure 6-13. TO_RETENTION Sequence, I2C7 = 1**

| Sequence Name | Device | Delay Diagram | Total Delay | Rail Name |
|---|---|---|---|---|
| nRSTOUT_SOC | TPS6594-Q1 | | 0 us | SOC_PORz_1V8 |
| nRSTOUT | TPS6594-Q1 | | 0 us | MCU_PORz |
| BUCK2 | LP8764-Q1 | | 500 us | VDD_RAM_0V85 |
| LDO2 | TPS6594-Q1 | | 1000 us | VDA_DLL_0V8 |
| BUCK3 | LP8764-Q1 | | 1000 us | VDD_CORE_0V8 |
| BUCK1 | LP8764-Q1 | | 1000 us | VDD_CPU_AVS |
| BUCK3 | TPS6594-Q1 | | 1000 us | VDD_MCU_0V85 |
| LDO4 | TPS6594-Q1 | | 1500 us | VDA_PLL_1V8 |
| BUCK5 | TPS6594-Q1 | | 1500 us | VDA_PHY_1V8 |
| BUCK4 | LP8764-Q1 | | 1500 us | VDD_IO_1V8 |
| BUCK1 | TPS6594-Q1 | | 1500 us | VDA_MCU_1V8 |
| BUCK2 | TPS6594-Q1 | | 1500 us | VDD_MCUIO_1V8 |
| GPIO10 | LP8764-Q1 | | 2000 us | 3V3IO_LDSW |
| GPIO3 | TPS6594-Q1 | | 2000 us | MCU3V3IO_LDSW |

**Figure 6-14. TO_RETENTION Sequence, I2C6 = 1 and I2C7 = 1**

| Sequence Name | Device | Delay Diagram | Total Delay | Rail Name |
|---|---|---|---|---|
| nRSTOUT_SOC | TPS6594-Q1 | | 0 us | SOC_PORz_1V8 |
| nRSTOUT | TPS6594-Q1 | | 0 us | MCU_PORz |
| GPIO1 | LP8764-Q1 | | 200 us | EXT_VDDR_IO |
| BUCK4 | TPS6594-Q1 | | 500 us | VDD_DDR_1V1 |
| BUCK2 | LP8764-Q1 | | 500 us | VDD_RAM_0V85 |
| LDO3 | TPS6594-Q1 | | 1000 us | VDD_WK_0V8 |
| LDO2 | TPS6594-Q1 | | 1000 us | VDA_DLL_0V8 |
| BUCK3 | LP8764-Q1 | | 1000 us | VDD_CORE_0V8 |
| BUCK1 | LP8764-Q1 | | 1000 us | VDD_CPU_AVS |
| BUCK3 | TPS6594-Q1 | | 1000 us | VDD_MCU_0V85 |
| LDO4 | TPS6594-Q1 | | 1500 us | VDA_PLL_1V8 |
| BUCK5 | TPS6594-Q1 | | 1500 us | VDA_PHY_1V8 |
| BUCK4 | LP8764-Q1 | | 1500 us | VDD_IO_1V8 |
| LDO1 | TPS6594-Q1 | | 1500 us | VDD1_LPDDR4_1V8 |
| BUCK1 | TPS6594-Q1 | | 1500 us | VDA_MCU_1V8 |
| BUCK2 | TPS6594-Q1 | | 1500 us | VDD_MCUIO_1V8 |
| GPIO7 | LP8764-Q1 | | 2000 us | GPIORET_LDSW |
| GPIO10 | LP8764-Q1 | | 2000 us | 3V3IO_LDSW |
| GPIO3 | TPS6594-Q1 | | 2000 us | MCU3V3IO_LDSW |

**Figure 6-15. TO_RETENTION Sequence, I2C6 = 0 and I2C7 = 0**

# 7 Additional Resources

For additional information regarding the PMIC or processor devices, use Table 7-1 for helpful resources:

**Table 7-1. Additional Documents**

| Title | Document Type | Devices | Link |
|---|---|---|---|
| TPS6594-Q1 Power Management IC (PMIC) for Processors with 5 Bucks and 4 LDOs | Datasheet | TPS6594-Q1 | Link |
| LP8764-Q1 Four Phase, 20-A Buck Converter with Integrated Switches | Datasheet | LP8764-Q1 | Request through mySecure |
| Jacinto™ DRA821 Automotive Processors Silicon Revision 1.0 | Datasheet | DRA821 | Request through mySecure |
| TPS6594-Q1 Safety Manual | Safety Manual | TPS6594-Q1 | Request through mySecure |
| LP8764-Q1 Safety Manual | Safety Manual | LP8764-Q1 | Request through mySecure |
| DRA821 Safety Manual Jacinto™ 7 Processors | Safety Manual | DRA821 | Request through mySecure |
| TPS6594-Q1 Schematic PCB Checklist | Application Note | TPS6594-Q1 | Link |

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**CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

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*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

**FCC Interference Statement for Class B EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

**Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

**Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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東京都新宿区西新宿 6 丁目 2 4 番 1 号
西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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