

DRV3201 Current Sense Amplifier

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ABSTRACT

This application report describes the DRV3201 Current Sense Amp.

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1 Current Sense Amp

The two channel current measurement is done by measuring the voltage drop across two external shunt resistors. It contains one shift buffer, two 1st and two 2nd stages.

2 Shift Buffer

The DRV3201 offers a unity gain amplifier that supports a shift voltage with lower output impedance. This allows each current sense path to handle negative common-mode voltages across the external shunt resistor. The shift-voltage is applied externally on the RI pin, with the actual shift-voltage being buffered on the RO pin. The RI input pin is a high-impedant input to a MOS gate with internal ESD protection to ground. There is no reverse pull-up path present to any supply (fail-safe ESD structure).

3 Two 1st Stage Amplifiers

A 1st stage operational amplifier is operating with an external resistor network for higher flexibility to adjust the current measurement to the application requirements.

In a recommended application, add a shift voltage to move the transfer curve. This shift voltage can be based on an external reference, for example, an external voltage regulator. Each channel of the first amplifier has its own output going, for example, to the input of the MCU ADC.

The input of the 1st stage is high-voltage compatible, use the device to measure the voltage drop across the LS MOSFET for low requirement applications. The maximum output voltage of the O1 and O2 pins is clamped to the ADREF voltage.

The input pins INx and IPx pin are high-impedance inputs to a MOS gate with internal ESD protection to ground. There is no reverse pull-up path present to any supply (fail-safe ESD structure).

4 Two 2nd Stage Amplifiers

The 2nd stage amplifiers with separately-programmable gain via SPI enable higher resolution measurement at low current. They directly connect to inputs of the MCU ADC.

The gain of the 2nd stage amplifiers is programmable in steps 2, 4, 6, and 8 by SPI using the CFG2 register. The maximum output voltage of the O3 and O4 pins clamps to the ADREF voltage.

5 ADREF Voltage Clamp

The maximum output voltage of pins O1...O4 is clamped to the voltage applied to ADREF by an active clamp. The ADREF voltage is the reference supply voltage for the ADC in the MCU. In this way, the outputs O1...O4 have maximum signal range related to the input range of the ADC in the MCU.

6 Application Circuit for Current Sense Amp

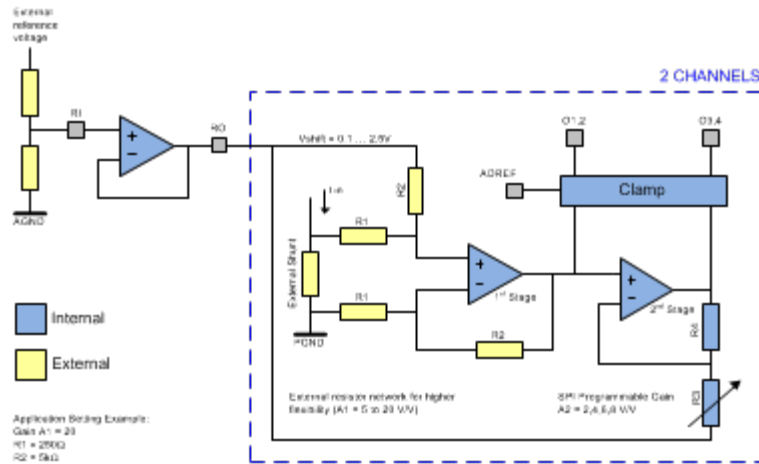


Figure 1. Application Circuit for Current Sense

$$V_{O1} = V_{RO} \left(\frac{R_1}{R_1 + R_2} \right) \left(1 + \frac{R_1}{R_2} \right) + (V_+) \left(\frac{R_2}{R_1 + R_2} \right) \left(1 + \frac{R_2}{R_1} \right) \left(1 + \frac{R_2}{R_1} \right) \quad (1)$$

$$\rightarrow A_1 = \left(\frac{R_2}{R_1 + R_2} \right) \left(1 + \frac{R_2}{R_1} \right) = 10 \text{ V/V} \quad (2)$$

$$V_{O3} = V_{O1} \left(1 + \frac{R'_2}{R'_1} \right) - \frac{R'_2}{R'_1} (V_{RO}) \quad (3)$$

$$\rightarrow A_2 = \left(1 + \frac{R'_2}{R'_1} \right) = 2 \text{ V/V} \quad (4)$$

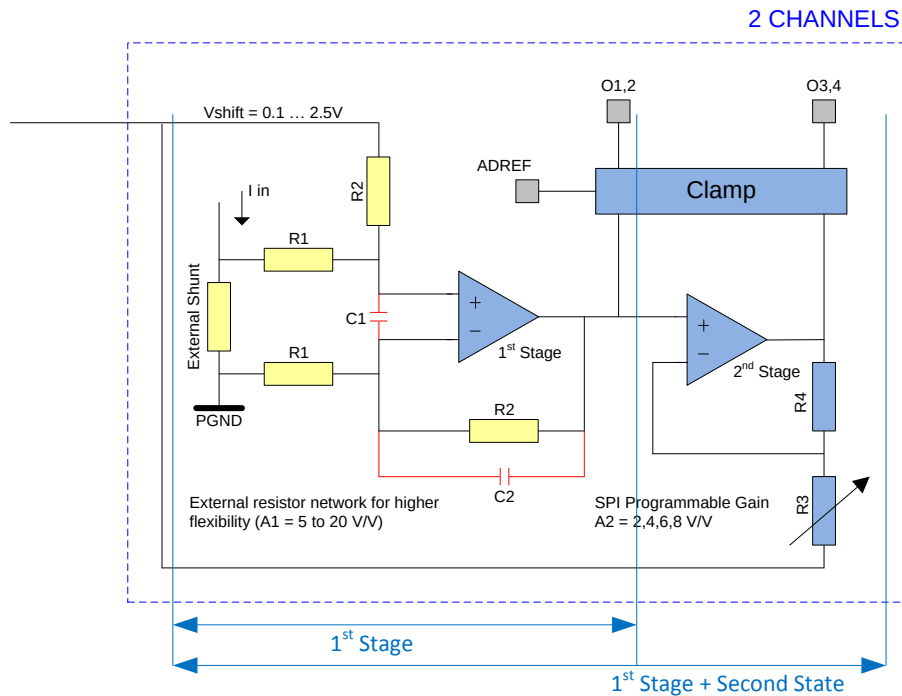


Figure 2. Characteristics with C1 and C2

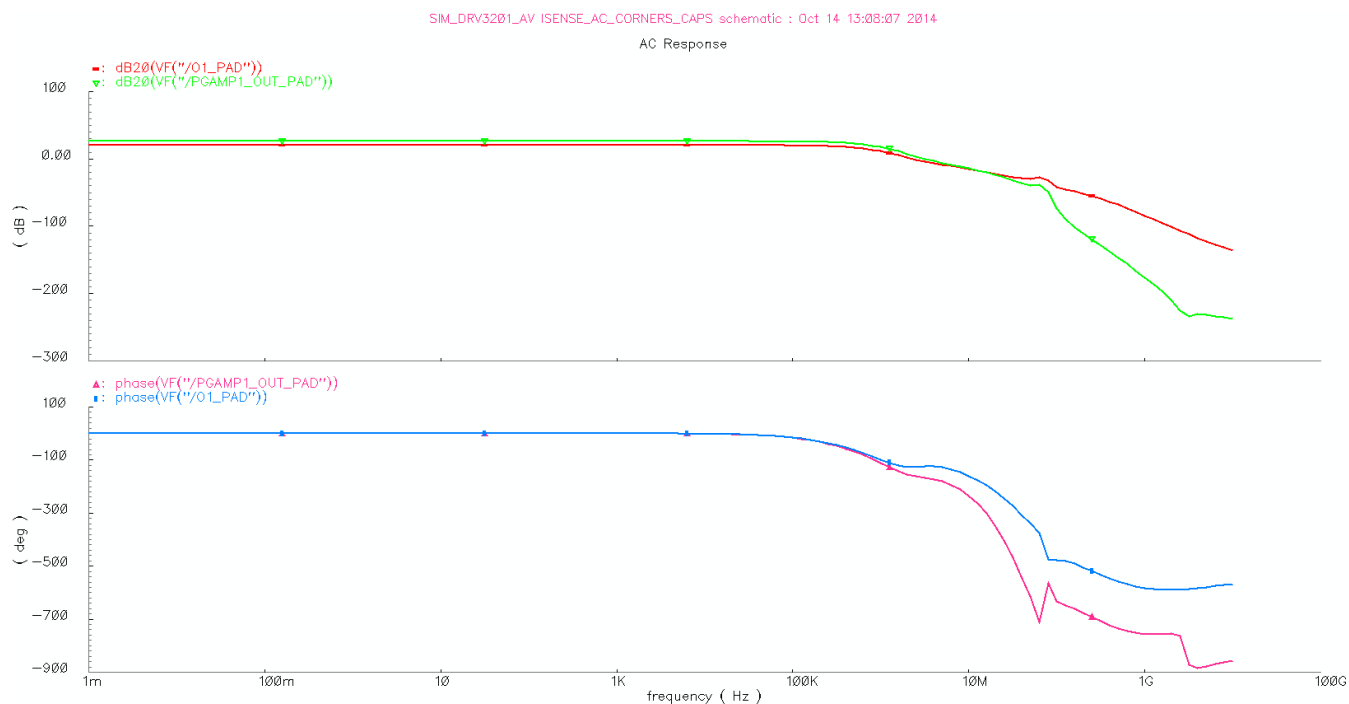


Figure 3. AC Simulation, C1 = 22 pF / C2 = 10 pF

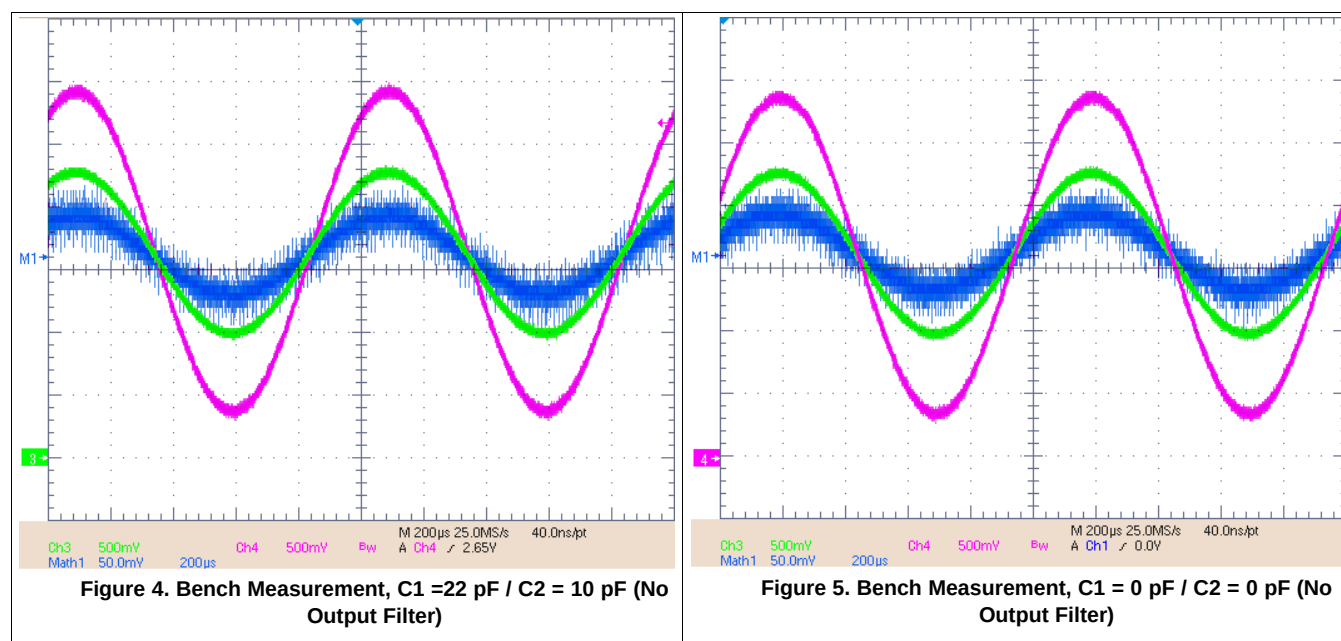


Figure 4. Bench Measurement, C1 = 22 pF / C2 = 10 pF (No Output Filter)

Figure 5. Bench Measurement, C1 = 0 pF / C2 = 0 pF (No Output Filter)

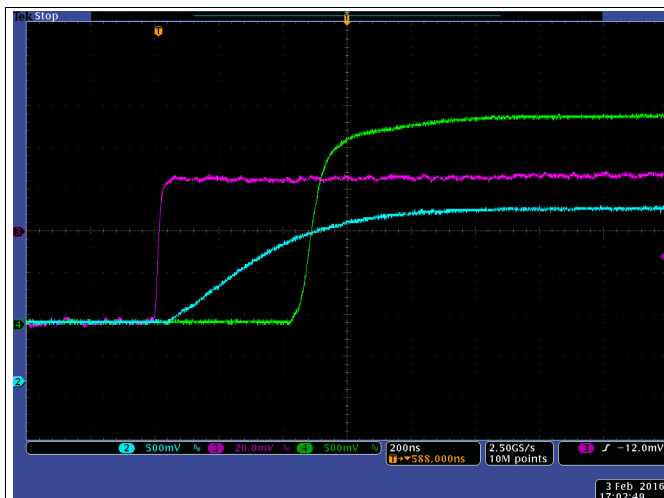


Figure 6. Settling Time Rising Edge, C1 = 0 pF / C2 = 0 pF

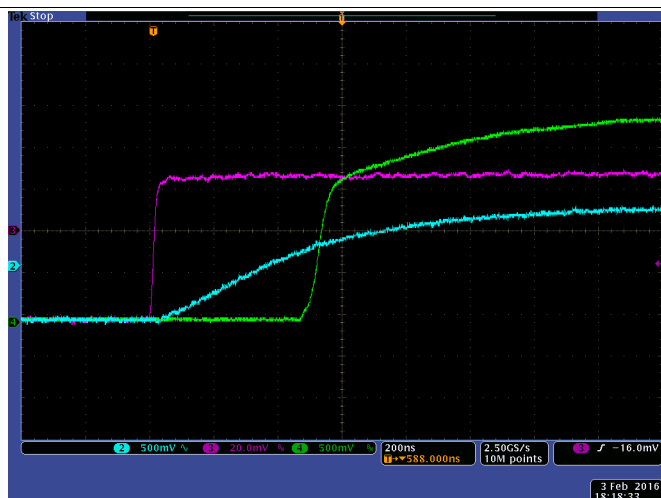


Figure 7. Settling Time Rising Edge, C1 = 22 pF / C2 = 10 pF

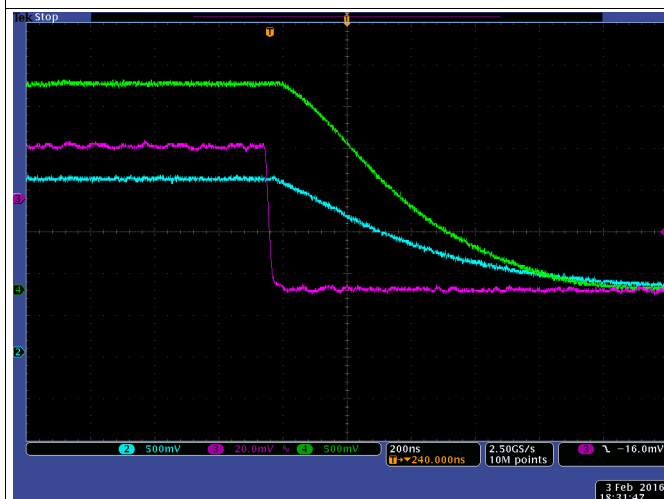


Figure 8. Settling Time Falling Edge, C1 = 0 pF / C2 = 0 pF

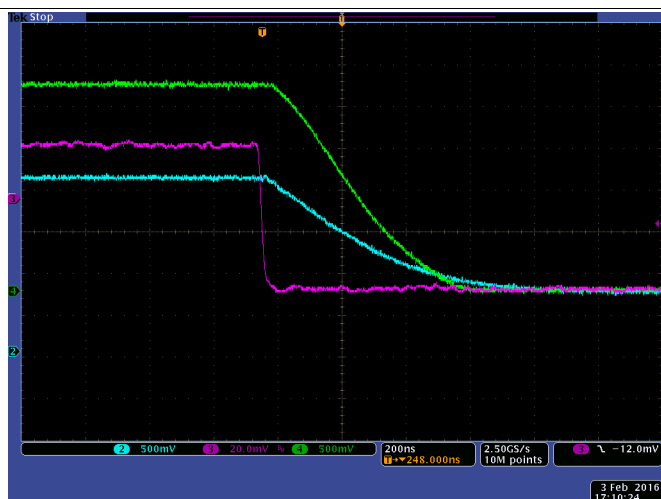


Figure 9. Settling Time Falling Edge, C1 = 22 pF / C2 = 10 pF

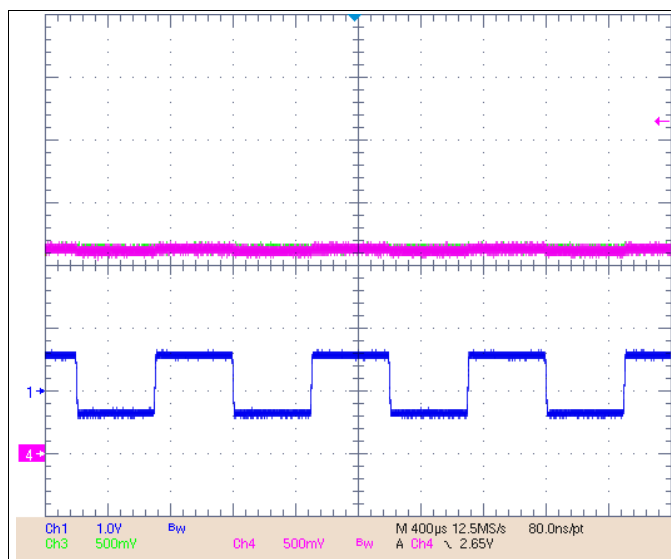


Figure 10. Common Mode Voltage, C1 = 22 pf / C2 = 10 pf
(No Output Filter)

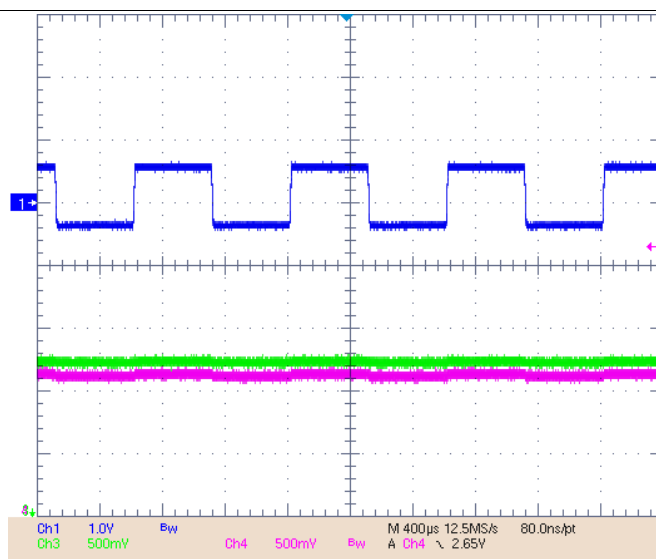


Figure 11. Common Mode Voltage, C1 = 0 pf / C2 = 0 pf
(No Output Filter)

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