Application Report
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DRV3205-Q1 Negative Voltage Stress on Source Pins

Motor Drive Business Unit - Advanced Protection Motor Drivers

ABSTRACT

A common problem in motor drive systems when switching an inductive load are negative voltage spikes on the source nodes of the power stage. These spikes can be large in magnitude, which can cause damage to connected IC devices.

This application report will look at the result of a bench test which stresses the DRV3205-Q1 with negative voltage transients on each of the gate and source pins.

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1 DRV3205-Q1 Specification

The DRV3205-Q1 device specifies a minimum and maximum for all of the gate and source pins—GHSx, SHSx, GLSx, and SLSx—of the device, as well as the current-sense pins—IPx and INx. Stresses beyond those listed under the *Absolute Maximum Ratings* in the data sheet may cause permanent damage to the device. These values are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under the *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Refer to the *Absolute Maximum Ratings* section of the DRV3205-Q1 datasheet for details on the ratings of these pins.

2 Bench Stress Experiment

To run this experiment, several DRV3205-Q1 devices were characterized across all tested parameters and the results data logged. The data log was used as a base line dataset to compare the performance of each unit before and after the test, and included a control device.

To adequately generate the voltage on each of the source pins, all connections between the device and the sense resistor and external FETs were disconnected, and the source pins connected directly to the spike source. Figure 1 shows the high-level test set up used for this test.

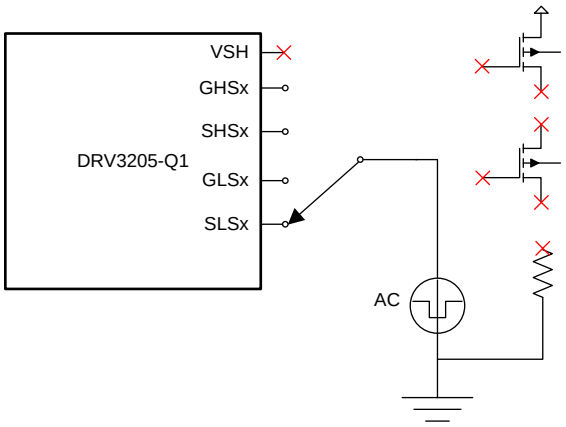

Figure 1. Stress Test Block Diagram

The experiment was run using a high power-pulse generator, hooked up directly to the source and gate pins on the DRV3205-Q1 device. Each device was stressed with 20-kHz pulses to each source and gate pin at a specific voltage below the absolute minimum rating for the pin. After the first set of pulses, the devices were again characterized using the same program, and all parameters compared to the pretest data logs to look for any parametric shifts. The experiment was run once more on the same pins, and the results compared to the original logs for the final results.

Figure 2 shows a scope capture of the pulse probed at the DRV3205-Q1 pin for the –12-V condition.

Figure 2. Conditions at DRV3205-Q1 Pin for –12-V Pulse Train

3 Results

Table 1 lists the results of the stress for each device. A grade of *pass* was given if each device in the group showed no damage and had no shifts in the parameters after comparing the pre-test data logs to the post-test data logs.

Table 1. Experiment Results

Voltage	Frequency	Duration	Test Result
0 V (Control)	N/A	N/A	Pass
–9 V	20 kHz	1 Hr/Pin	Pass
–12 V	20 kHz	1 Hr/Pin	Pass
–15 V	20 kHz	1 Hr/Pin	Pass

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