TEXAS INSTRUMENTS
DRV8462
SLOSE79 – AUGUST 2022

DRV8462 Stepper Motor Driver with Auto-torque, Silent Step Decay Mode and Automatic Microstepping

ADVANCE INFORMATION

1 Features

- Stepper motor driver
  - SPI or H/W interface with STEP/DIR pins
  - Up to 1/256 microstepping indexer
- **4.5 V to 65 V** operating supply voltage range
- Low $R_{DS(ON)}$: **100 mΩ** HS + LS at 24 V, 25°C
- High current capacity per bridge:
  - DDW Package: **5A** full-scale, 3.5A RMS
  - DDV Package: **10A** full-scale, 7A RMS
- DDW package **pin-to-pin compatible** with -
  - DRV8452DDWR: 48 V, 5A full-scale
- Integrated current sensing and regulation
  - 5% full-scale current accuracy
- Smart tune and mixed decay regulation options
- **Silent step** decay mode for silent operation at standstill and low speed
- **Automatic Microstepping** mode for step frequency interpolation
- **Customizable microstepping** indexer table
- **Auto-torque** for load dependent current control
- **Standstill Power Saving** mode
- Supports 1.8-V, 3.3-V, 5.0-V logic inputs
- Low-current sleep mode (3 µA)
- Separate logic supply voltage (**VCC**)
- Protection and diagnostic features
  - Sensorless **Stall Detection**
  - VM undervoltage lockout (UVLO)
  - Open-load detection (OL)
  - Overcurrent protection (OCP)
  - Thermal shutdown (OTSD)
  - Fault condition output (nFAULT)
  - Indexer zero position output (**nHOME**)

2 Applications

- Textile Machines
- Factory Automation, Stepper Drives and Robotics
- Medical Imaging, Diagnostics and Equipment
- Stage Lighting
- ATMs and Currency Counters
- PLC
- Printers
- 3D Printer
- Outdoor IP Camera

3 Description

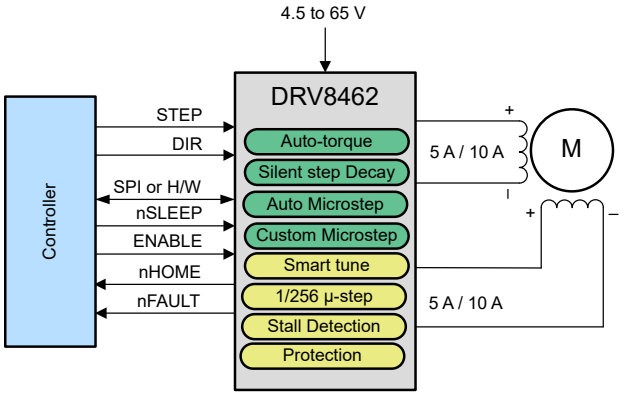
The DRV8462 is a wide-voltage, high-power, high-performance stepper motor driver. The device supports up to 65-V supply voltage, and integrated MOSFETs with 100 mΩ HS + LS on-resistance allow up to 5-A current with the DDW package; and up to 10-A current with the DDV package.

The auto-torque feature boosts system efficiency by adjusting the coil current according to load torque. The standstill power saving mode reduces power loss during motor holding condition. The silent step decay mode guarantees noiseless operation. The internal current sense architecture eliminates the need for external sense resistors, therefore saving PCB area and system cost. The built-in indexer of the DRV8462 supports up to 1/256 microstepping, and the automatic microstepping mode interpolates the input STEP signal to reduce overhead on the controller MCU. Sensorless stall detection eliminates end stops from the system. The device supports other protection and diagnostic features for robust and reliable operation.

The DRV8462 requires only minimal tuning to configure the advanced features. High energy efficiency coupled with precise, noiseless operation makes the DRV8462 an ideal choice for high-performance stepper motor systems.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
DRV8462DDWR	HTSSOP (44), bottom exposed pad	14 mm x 6.1 mm
DRV8462DDVR	HTSSOP (44), top exposed pad	14 mm x 6.1 mm



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2022	*	Initial Release

5 Pin Configuration and Functions

The DRV8462 is available in thermally-enhanced, 44-Pin HTSSOP packages.

- The DDW package contains a PowerPAD™ on the bottom side of the device.
- The DDV package contains a PowerPAD™ on the top side of the device for thermal coupling to a heatsink.

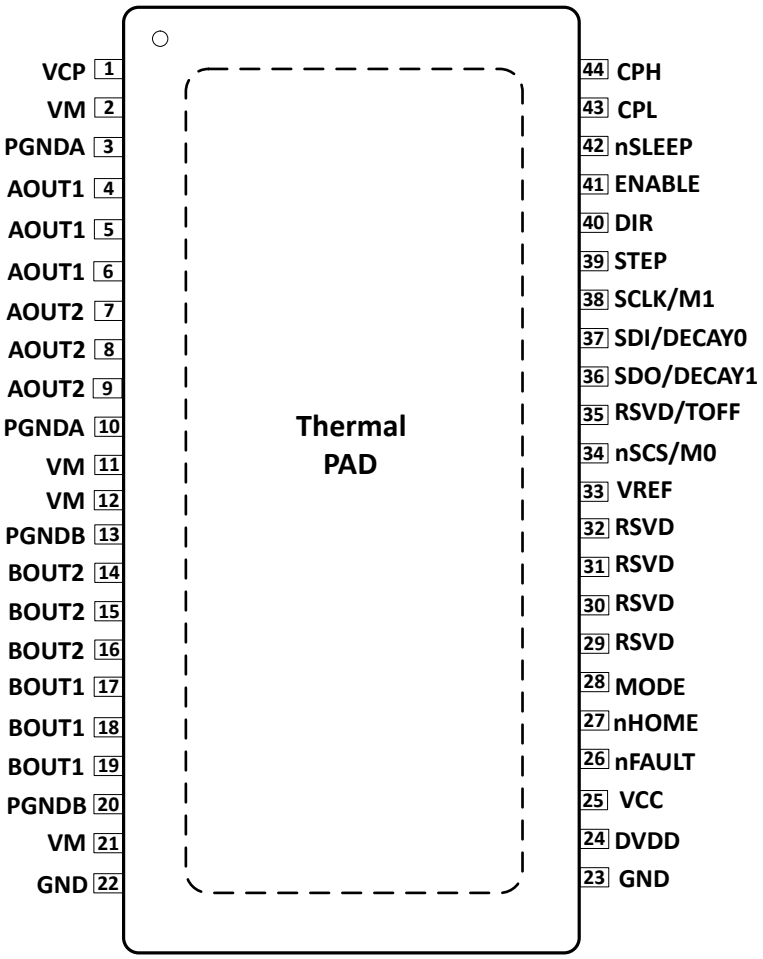

Figure 5-1. DDW Package (44-Pin HTSSOP), Top View

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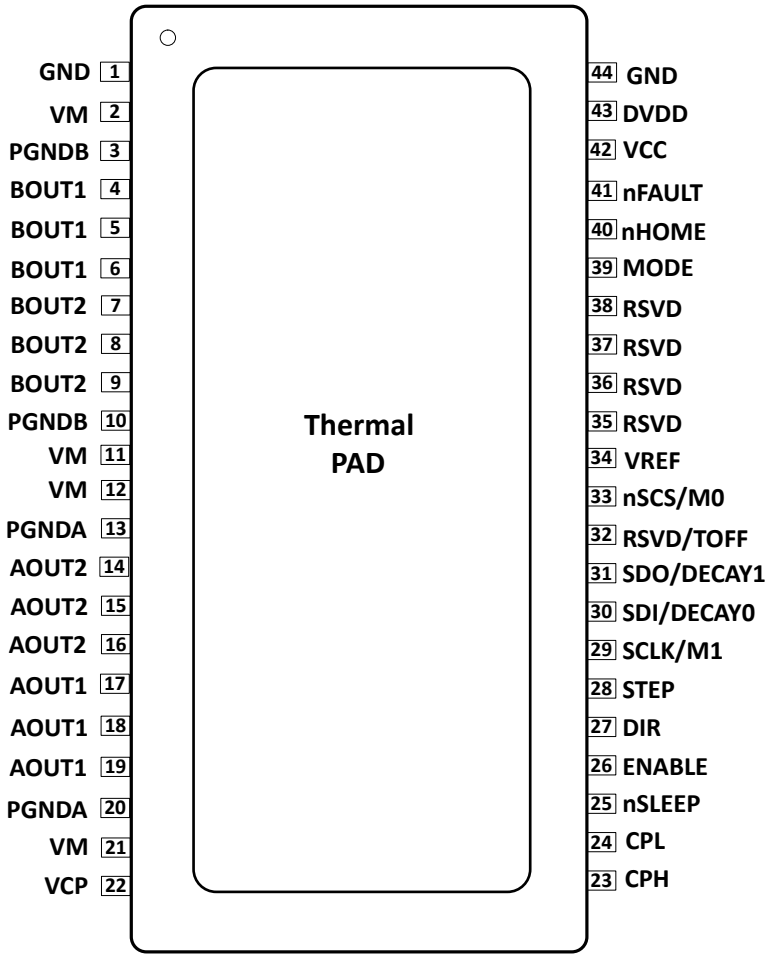

Figure 5-2. DDV Package (44-Pin HTSSOP), Top View

PIN			TYPE	DESCRIPTION
NAME	DDW	DDV		
VCP	1	22	Power	Charge pump output. Connect a X7R, 1-µF, 16-V ceramic capacitor from VCP to VM.
VM	2, 11, 12, 21	2, 11, 12, 21	Power	Power supply. Connect to motor supply voltage and bypass to PGNDA and PGNDB with two 0.01-µF ceramic capacitors (one for each pair of pins) plus a bulk capacitor rated for VM.
PGNDA	3, 10	13, 20	Power	Power ground. Connect to system ground.
PGNDB	13, 20	3, 10	Power	Power ground. Connect to system ground.
AOUT1	4, 5, 6	17, 18, 19	Output	Winding A output. Connect to motor winding.
AOUT2	7, 8, 9	14, 15, 16	Output	Winding A output. Connect to motor winding.
BOUT2	14, 15, 16	7, 8, 9	Output	Winding B output. Connect to motor winding.
BOUT1	17, 18, 19	4, 5, 6	Output	Winding B output. Connect to motor winding.
GND	22, 23	1, 44	Power	Device ground. Connect to system ground.
DVDD	24	43	Power	Internal LDO output. Connect a X7R, 1-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
VCC	25	42	Power	Supply voltage for internal logic blocks. When separate logic supply voltage is not available, tie the VCC pin to the DVDD pin. When configured with SPI interface, the VCC pin also acts as the supply pin for SDO output.

PIN			TYPE	DESCRIPTION
NAME	DDW	DDV		
nFAULT	26	41	Open Drain	Fault indication output. Pulled logic low with fault condition. Open-drain nFAULT requires an external pullup resistor.
nHOME	27	40	Open Drain	Pulled logic low when the internal indexer is at home position (45°) of step table. The nHOME pin outputs one low pulse per 360º electrical rotation (four fullsteps).
MODE	28	39	Input	MODE pin programs the device to operate with either SPI or hardware (H/W) pin interface.
RSVD	29	38	-	Reserved. Leave unconnected.
RSVD	30	37	-	Reserved. Leave unconnected.
RSVD	31	36	-	Reserved. Leave unconnected.
RSVD	32	35	-	Reserved. Leave unconnected.
VREF	33	34	Input	Voltage reference input for setting full-scale current. DVDD can be used to generate VREF through a resistor divider. When configured with SPI interface, the VREF pin can be left unconnected if VREF_INT_EN = 1b.
nSCS/M0	34	33	Input	With SPI interface, this pin acts as serial chip select. An active low on this pin enables the serial interface communications. With H/W interface, this pin programs the microstepping mode.
RSVD/TOFF	35	32	Input	This pin is not used with SPI interface. With H/W interface, this pin programs the OFF time for PWM current regulation.
SDO/ DECAY1	36	31	Push-Pull/Input	With SPI interface, this pin acts as serial data output. Data is shifted out on the rising edge of the SCLK pin. With H/W interface, this pin programs the decay-mode.
SDI/DECAY0	37	30	Input	With SPI interface, this pin acts as serial data input. Data is captured on the falling edge of the SCLK pin. With H/W interface, this pin programs the decay-mode.
SCLK/M1	38	29	Input	With SPI interface, this pin acts as serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. With H/W interface, this pin programs the microstepping mode.
STEP	39	28	Input	Step input. An active edge causes the indexer to advance one step. With SPI interface, STEP active edge can be either rising edge or both rising and falling edge. With H/W interface, STEP active edge is always the rising edge.
DIR	40	27	Input	Direction input. Logic level sets the direction of stepping.
ENABLE	41	26	Input	Logic low to disable device outputs; logic high to enable. When the device operates with H/W interface, the ENABLE pin also determines the OCP, OL and OTSD fault recovery methods.
nSLEEP	42	25	Input	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode. A narrow nSLEEP reset pulse clears latched faults.
CPL	43	24	Power	Charge pump switching node. Connect a X7R, 0.1-µF, VM-rated ceramic capacitor from CPH to CPL.
CPH	44	23	Power	
PAD	-	-	-	Thermal pad. Connect to system ground.

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6 Specifications

6.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	70	V
Charge pump voltage (VCP, CPH)	-0.3	V_{VM} + 5.75	V
Charge pump negative switching pin (CPL)	-0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
External logic supply (VCC)	-0.3	5.75	V
Control pin voltage	–0.3	5.75	V
Reference input pin voltage (VREF)	–0.3	5.75	V
PGNDx to GND voltage	-0.5	0.5	V
PGNDx to GND voltage, < 1 µs	-2.5	2.5	V
Open drain output current (nFAULT, nHOME)	0	10	mA
Continuous Output pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–1	V_{VM} + 1	V
Transient 100 ns Output pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–3	V_{VM} + 3	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

over operating free-air temperature range (unless otherwise noted)(1)(2)

1. *Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*
2. *All voltage values are with respect to network ground terminal GND.*

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	Corner Pins	±750	
			Other Pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Over operating free-air temperature range (unless otherwise noted).

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	65	V
V_I	Logic level input voltage	0	5.5	V
V_{VCC}	VCC pin voltage	3.05	5.5	V
V_{REF}	Reference voltage (VREF)	0.05	3.3	V
f_{STEP}	Applied STEP signal (STEP)	0	100 (1)	kHz
I_{FS}	Motor full-scale current with DDW package (xOUTx)	0	5 (2)	A

6.3 Recommended Operating Conditions (continued)

		MIN	MAX	UNIT
I_{FS}	Motor full-scale current with DDV package (xOUTx)	0	10 (2)	A
I_{RMS}	Motor RMS current with DDW package (xOUTx)	0	3.5 (2)	A
I_{RMS}	Motor RMS current with DDW package (xOUTx)	0	7 (2)	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

1. STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load.
2. Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC		DDW	DDV	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.6	41.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.8	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.0	14.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.9	14.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	N/A	°C/W

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6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	ENABLE = 1, nSLEEP = 1, No motor load, VCC = External 5V		5	8	mA
		ENABLE = 1, nSLEEP = 1, No motor load, VCC = DVDD		7	12	
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		3	8	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	H/W interface, nSLEEP = 1 to output transition		0.8	1.2	ms
		SPI interface, nSLEEP = 1 to SPI ready		0.15	0.25	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.8	1.3	ms
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 65 V	4.75	5	5.25	V
		No external load, V_{VM} = 4.5 V	4.2	4.35		V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	6 V < V_{VM} < 65 V		V_{VM} + 5		V
f_{VCP}	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		357		kHz
f_{CLK}	Internal digital clock frequency	V_{VM} > UVLO; nSLEEP = 1		10		MHz
LOGIC-LEVEL INPUTS (STEP, DIR, MODE, nSCS, SCLK, SDI, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis (all pins except nSLEEP)			150		mV
V_{HYS_SLEEP}	nSLEEP logic hysteresis			250		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
$I_{IL(nSCS)}$	nSCS logic-low current	nSCS = 0V	8		12	µA
I_{IH}	Input logic-high current	V_{IN} = DVDD			50	µA
$I_{IH(nSCS)}$	nSCS logic-high current	nSCS = DVDD			0.1	µA
TRI-LEVEL INPUTS (M0, DECAY0, DECAY1, ENABLE)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I3}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10		µA
QUAD-LEVEL INPUTS (M1, TOFF)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}		330kΩ ± 5% to GND	1	1.25	1.4	V
V_{I3}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I4}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10		µA

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Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PUSH-PULL OUTPUT (SDO)						
$R_{PD,SDO}$	Internal pull-down resistance	5mA load, with respect to GND		30	60	Ω
$R_{PU,SDO}$	Internal pull-up resistance	5mA load, with respect to VCC		60	110	Ω
I_{SDO}	SDO Leakage Current	V_{VM} > 6 V, SDO = VCC and 0V	-1		1	µA
CONTROL OUTPUTS (nFAULT, nHOME)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic-high leakage		-1		1	µA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ONH)}$	High-side FET on resistance	T_J = 25 °C, I_O = -5 A		50	60	mΩ
		T_J = 125 °C, I_O = -5 A		75	90	mΩ
		T_J = 150 °C, I_O = -5 A		85	105	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance	T_J = 25 °C, I_O = 5 A		50	60	mΩ
		T_J = 125 °C, I_O = 5 A		75	90	mΩ
		T_J = 150 °C, I_O = 5 A		85	105	mΩ
t_{RF}	Output rise/fall time	H/W interface, I_O = 5 A, between 10% and 90%		140		ns
		SPI interface, SR = 0b, I_O = 5 A, between 10% and 90%		140		
		SPI interface, SR = 1b, I_O = 5 A, between 10% and 90%		70		
t_D	Output dead time	VM = 24V, I_O = 5 A		300		ns
PWM CURRENT CONTROL (VREF)						
K_V	Transimpedance gain	VREF = 3.3 V, DDW Package	0.625	0.66	0.695	V/A
		VREF = 3.3 V, DDV Package	0.313	0.33	0.347	
I_{VREF}	VREF Pin Leakage Current	VREF = 3.3 V			100	nA
t_{OFF}	PWM off-time	TOFF = 0 or TOFF = 00b		7		µs
		TOFF = 1 or TOFF = 01b		16		
		TOFF = Hi-Z or TOFF = 10b		24		
		TOFF = 330kΩ to GND or TOFF = 11b		32		
ΔI_{TRIP_EXT}	Current trip accuracy, external VREF input	10% to 20% full-scale current	-12		12	%
		20% to 40% full-scale current	-8		5	
		40% to 100% full-scale current	-5		4	
ΔI_{TRIP_INT}	Current trip accuracy, internal VREF	10% to 20% full-scale current	-12		12	%
		20% to 40% full-scale current	-9		6	
		40% to 100% full-scale current	-6		5	
$I_{O,CH}$	AOUT and BOUT current matching	100% full-scale current	-2.5		2.5	%

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Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{BLK}	Current regulation blanking time	SPI interface, TBLANK_TIME = 00b		1		µs
		H/W interface or SPI interface, TBLANK_TIME = 01b		1.5		
		SPI interface, TBLANK_TIME = 10b		2		
		SPI interface, TBLANK_TIME = 11b		2.5		
t_{DEG}	Current regulation deglitch time			0.5		µs
PROTECTION CIRCUITS						
VM_{UVLO}	VM UVLO lockout	VM falling	4.1	4.25	4.35	V
		VM rising	4.2	4.35	4.45	
VCC_{UVLO}	VCC UVLO lockout	VCC connected to external voltage, VCC falling	2.7	2.8	2.9	V
		VCC connected to external voltage, VCC rising	2.8	2.9	3.05	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{RST}	VM UVLO reset	VCC = DVDD, SPI interface, VM falling, device reset, no SPI communications			3.9	V
V_{CPUV}	Charge pump undervoltage	VCP falling		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET, DDW Package	8			A
		Current through any FET, DDV Package	16			A
t_{OCP}	Overcurrent detection delay	H/W Interface		2		µs
		SPI Interface, TOCP = 0b		1		
		SPI Interface, TOCP = 1b		2		
t_{RETRY}	Overcurrent retry time			4		ms
t_{OL}	Open load detection time	H/W Interface			60	ms
		SPI Interface, OL_T = 00b			30	
		SPI Interface, OL_T = 01b			60	
		SPI Interface, OL_T = 10b			120	
I_{OL}	Open load current threshold			150		mA
T_{OTW}	Overtemperature warning	SPI Interface, Die temperature T_J	135	150	165	°C
T_{HYS_OTW}	Overtemperature warning hysteresis	SPI Interface, Die temperature T_J		20		°C
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

6.5.1 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
t_{READY}	SPI ready, VM > V_{RST}		1		ms
t_{SCLK}	SCLK minimum period	100			ns
t_{SCLKH}	SCLK minimum high time	50			ns
t_{SCLKL}	SCLK minimum low time	50			ns

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		MIN	NOM	MAX	UNIT
t_{SU_SDI}	SDI input setup time	20			ns
t_{H_SDI}	SDI input hold time	30			ns
t_{D_SDO}	SDO output delay time, SCLK high to SDO valid, C_L = 20 pF			30	ns
t_{SU_nSCS}	nSCS input setup time	50			ns
t_{H_nSCS}	nSCS input hold time	50			ns
t_{HI_nSCS}	nSCS minimum high time before active low			2	µs
t_{DIS_nSCS}	nSCS disable time, nSCS high to SDO high impedance		10		ns

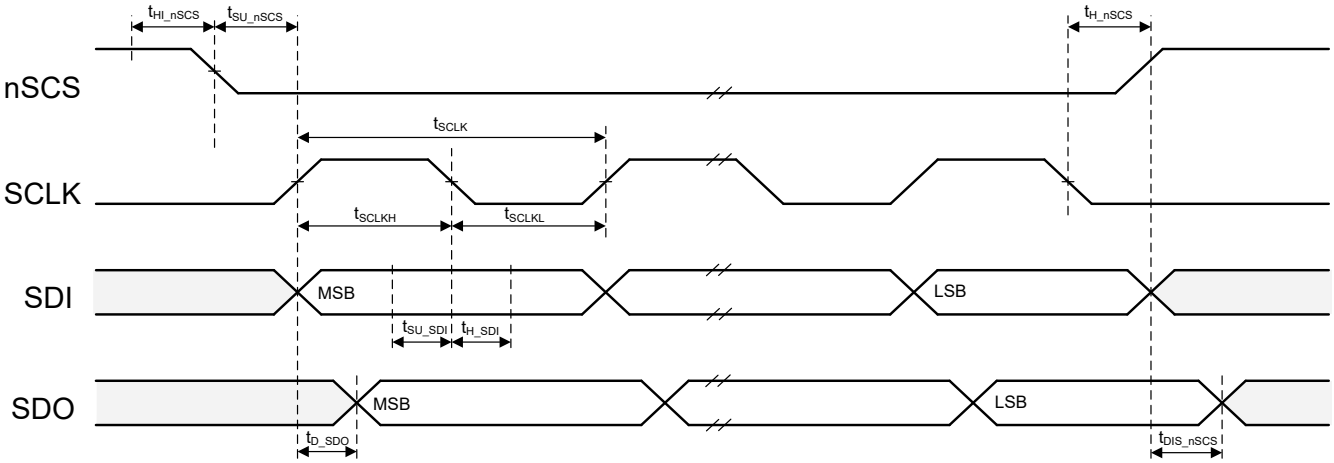

Figure 6-1. SPI Timing Diagram

6.5.2 STEP and DIR Timing Requirements

Typical limits are at T_J = 25°C and V_{VM} = 24 V. Over recommended operating conditions unless otherwise noted.

NO.			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		500(1)	kHz
2	t_{WH_STEP}	Pulse duration, STEP high	970		ns
3	t_{WL_STEP}	Pulse duration, STEP low	970		ns
4	$t_{SU\_DIR,\ Mx}$	Setup time, DIR or Mx to STEP rising	200		ns
5	$t_{H\_DIR,\ Mx}$	Hold time, DIR or Mx to STEP rising	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load.

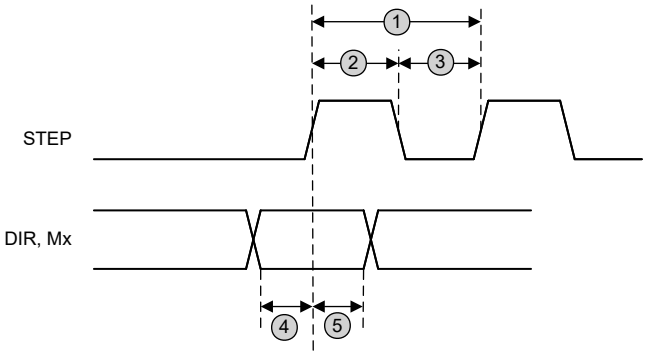

Figure 6-2. STEP and DIR Timing Diagram

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7 Detailed Description

7.1 Overview

The DRV8462 is an integrated motor-driver solution for bipolar stepper motors. The device integrates two N-channel power MOSFET H-bridges, current sense resistors, current regulation circuitry, and a microstepping indexer. The DRV8462 is capable of supporting wide supply voltage of 4.5 V to 65 V. The device is available in two packages - a 44-pin HTSSOP (DDW) package with exposed pad at the bottom of the package; and another 44-pin HTSSOP (DDV) package with exposed pad on the top of the package. The DDW package provides an output current up to 8-A peak, 5-A full-scale, or 3.5-A root mean square (rms). When used with a low thermal resistance heat sink installed on the top of the DDV package, the DRV8462 can deliver an output current up to 16-A peak, 10-A full-scale, or 7-A root mean square (rms). The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal design. The DRV8462 DDW package is pin-to-pin compatible with the DRV8452, which is rated for 48 V maximum operating voltage and 5 A full-scale current.

The DRV8462 integrates the auto-torque feature to reduce power loss and improve system efficiency by adjusting output current according to the load torque. The SPI interface provides various options to optimize the performance of the auto-torque algorithm for specific motor and system use case. The stall detection feature detects and reports a stall condition to the controller when the motor is obstructed or has reached an end-of-travel stop. Additionally, the standstill power saving mode reduces power loss when the motor is at holding position.

The DRV8462 uses an integrated current-sense architecture which eliminates the need for two external power sense resistors, hence saving significant board space, BOM cost, design efforts and reduces significant power consumption. This architecture eliminates the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. Optional external power sense resistors can also be connected between the PGND pins and board ground to monitor motor health and for implementing closed-loop algorithms such as Field Oriented Control. The current regulation set point is adjusted by the voltage at the VREF pin. For the SPI interface, an 8-bit register allows the controller to scale the output current without needing to scale the VREF voltage reference; and another 8-bit register allows configuration of the holding current level for the purpose of reducing power loss at motor standstill.

A STEP/DIR pin interface allows an external controller to manage the direction and step rate of the stepper motor. The internal microstepping indexer can execute high-accuracy micro-stepping without requiring the external controller to manage the winding current level. The indexer is capable of full step, half step, and 1/4,1/8, 1/16, 1/32, 1/64, 1/128, and 1/256 microstepping. High microstepping contributes to significant audible noise reduction and smooth motion. The automatic microstepping mode interpolates the input step frequency to high resolution, thereby improving current regulation and reducing audible noise while running with a low frequency step input from the controller. The custom microstepping table allows adjusting the current waveform to the needs of a particular motor.

Stepper motor drivers need to re-circulate the winding current by implementing several types of decay modes, such as slow decay, mixed decay and fast decay. The DRV8462 supports smart tune decay modes. The smart tune is an innovative decay mechanism that automatically adjusts for optimal current regulation performance agnostic of supply voltage and motor speed variations and aging effects. Smart tune Ripple Control uses a variable off-time ripple current control scheme to minimize distortion of the motor winding current. Smart tune Dynamic Decay uses a fixed off-time dynamic fast decay percentage scheme. Along with the smart tune decay modes, the DRV8462 also features a silent step decay mode for noiseless operation at standstill and low speeds of rotation.

The device integrates a spread spectrum clocking feature for both the internal digital oscillator and internal charge pump. This feature minimizes the electromagnetic emissions from the device. A low-power sleep mode is included which allows the system to save power when not actively driving the motor.

7.2 Functional Block Diagram

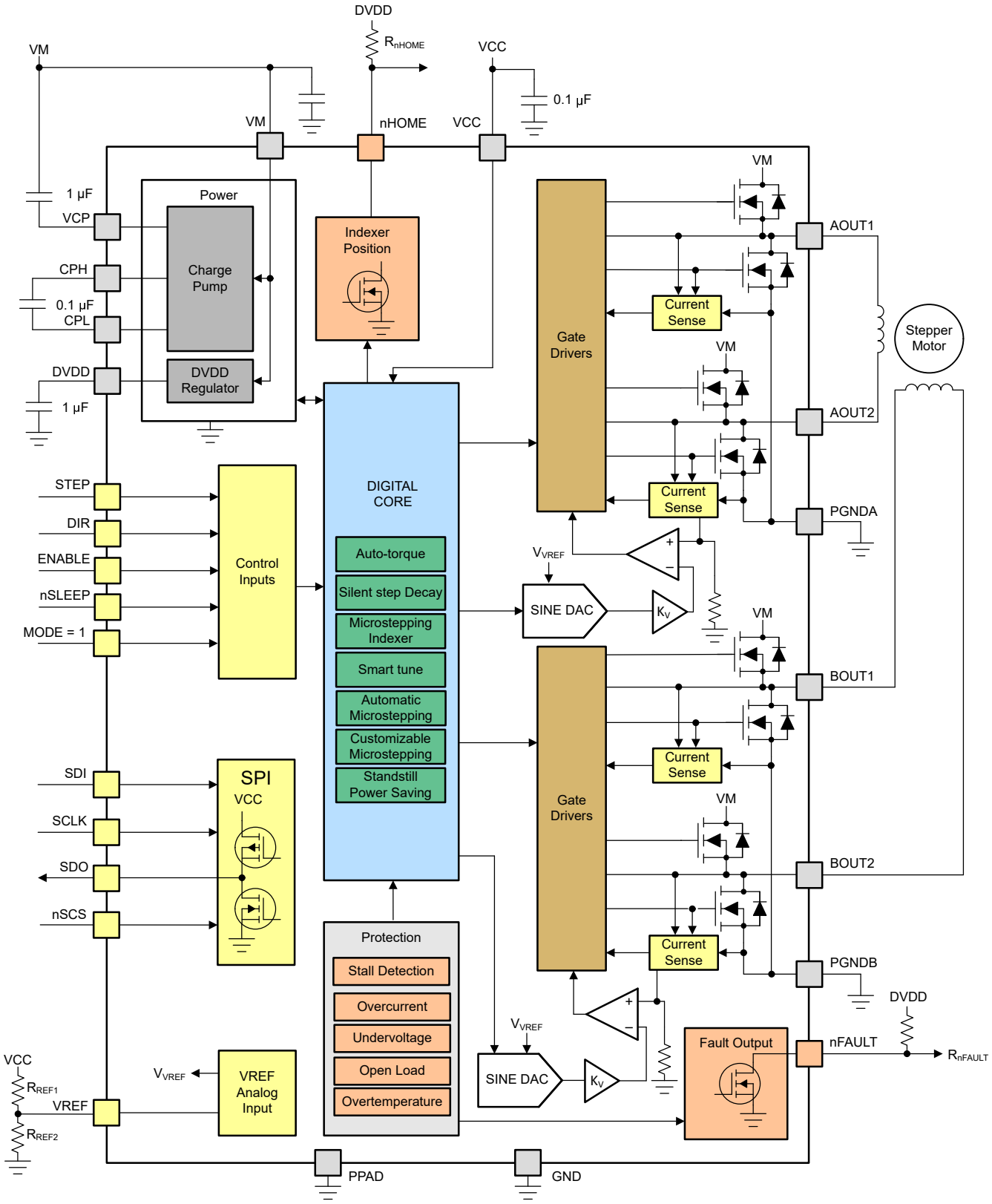

Figure 7-1. DRV8462 Block Diagram with SPI Interface (MODE = 1)

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7.3 Functional Block Diagram

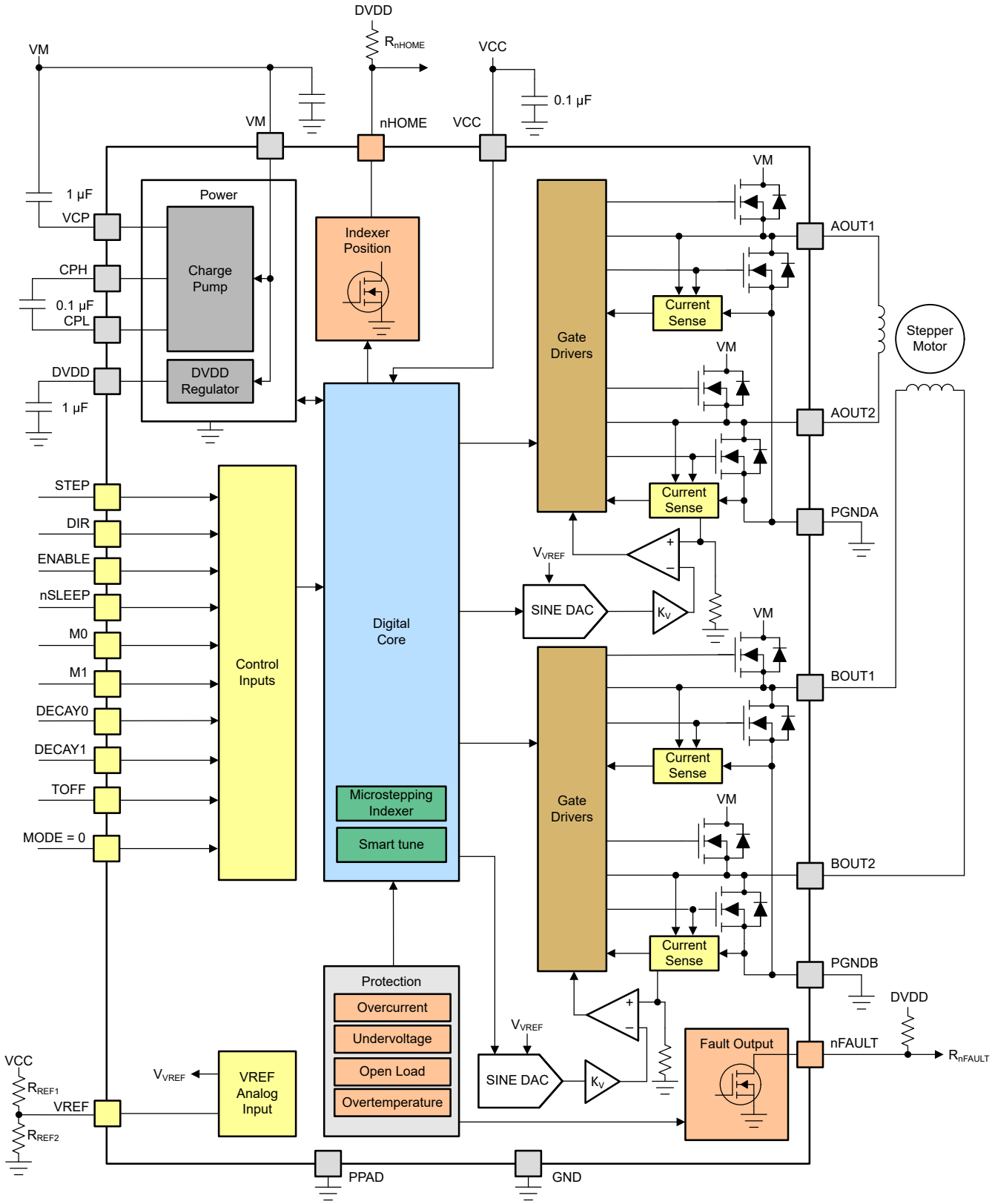

Figure 7-2. DRV8462 Block Diagram with Hardware Interface (MODE = 0)

7.4 Feature Description

Table 7-1 lists the recommended external components for the DRV8462.

Table 7-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGNDA	X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM2}	VM	PGNDB	X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM3}	VM	PGNDA	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 1-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.1-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 1-µF, 6.3-V ceramic capacitor
C_{VCC}	VCC	GND	X7R, 0.1-µF, 6.3-V ceramic capacitor
R_{nFAULT}	DVDD or VCC	nFAULT	10-kΩ resistor
R_{nHOME}	DVDD or VCC	nHOME	10-kΩ resistor
R_{REF1}	VREF	DVDD or VCC	Resistor to set chopping current.
R_{REF2}	VREF	GND	

7.4.1 Operation Interface

The DRV8462 can operate with hardware (H/W) pin interface or SPI interface. When operating with SPI interface, the device supports additional features and detailed diagnostics, as shown in Table 7-4.

The logic-level MODE pin latches the operating interface information at power up or after nSLEEP cycling -

- If the MODE pin is grounded at this time, the device operates with H/W pin interface.
- If the MODE pin is logic high at this time, the device operates with SPI interface.
- Do not change MODE pin logic level on the fly after power up or after nSLEEP cycling.

The functionality of five pins depend on the interface of operation, as shown in Table 7-2 and Table 7-3 -

Table 7-2. Pin function, DDW package

Pin Number	MODE = 0, H/W interface	MODE = 1, SPI interface
34	M0	nSCS
35	TOFF	Reserved
36	DECAY1	SDO
37	DECAY0	SDI
38	M1	SCLK

Table 7-3. Pin function, DDV package

Pin Number	MODE = 0, H/W interface	MODE = 1, SPI interface
29	M1	SCLK
30	DECAY0	SDI
31	DECAY1	SDO
32	TOFF	Reserved
33	M0	nSCS

Table 7-4 compares the feature set and diagnostic features for the two operating interfaces -

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Table 7-4. Feature Set Difference

Feature	MODE = 0, H/W interface	MODE = 1, SPI interface
Smart tune	Yes	Yes
Up to 1/256 microstepping	Yes	Yes
Separate logic supply (VCC)	Yes	Yes
nHOME output	Yes	Yes
nFAULT output	Yes	Yes
Automatic microstepping	No	Yes
Customizable microstepping	No	Yes
Indexer output	No	Yes
Internal 3.3V reference voltage	No	Yes
Dual STEP active edge	No	Yes
Silent step decay	No	Yes
Auto-torque	No	Yes
Standstill power saving	No	Yes
Spread spectrum	No	Yes
Protection features		
VM and VCP UVLO	Yes	Yes
VCC Power on Reset	Yes	Yes
Overcurrent Protection	Yes	Yes
Open-load detection	Yes	Yes
Thermal shutdown	Yes	Yes
Stall detection	No	Yes
Overtemperature warning	No	Yes

Note

For pre-production samples, if the device is configured to operate with H/W interface, and the M0 pin is Hi-z at power-up, then the nFAULT pin will stay low even if there are no faults. To release the nFAULT, the user has to apply an nSLEEP reset pulse.

This behavior will not be present in the production samples - nFAULT will be pulled-high after power-up if there are no faults.

7.4.2 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, RMS, and full-scale.

7.4.2.1 Peak Current Rating

The peak current in a stepper driver is limited by the overcurrent protection trip threshold I_{OCP}. In general the minimum value of I_{OCP} specifies the peak current rating of the stepper motor driver. For the DRV8462 in DDW package, the peak current rating is 8 A per bridge. For the DDV package, the peak current rating is 16 A per bridge.

7.4.2.2 RMS Current Rating

The RMS current is determined by the thermal considerations of the IC. The RMS current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The actual operating RMS current may be higher or lower depending on heatsinking and ambient temperature. For the DRV8462 in DDW package, the RMS current rating is 3.5 A per bridge. For the DDV package, the RMS current rating is 7 A per bridge.

7.4.2.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Because the sinusoid amplitude is related to the RMS current, the full-scale current is also determined by the thermal considerations of the device. The full-scale current rating is approximately $\sqrt{2} \times I_{RMS}$ for a sinusoidal current waveform, and I_{RMS} for a square wave current waveform (full step).

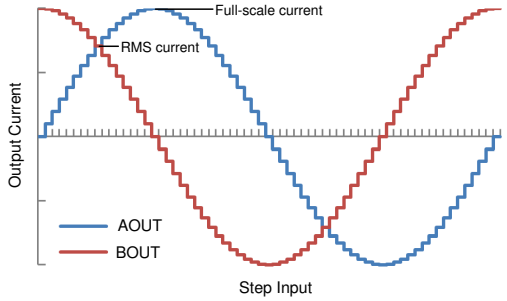

Figure 7-3. Full-Scale and RMS Current

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7.4.3 PWM Motor Drivers

The DRV8462 has drivers for two full H-bridges to drive the two windings of a bipolar stepper motor. Figure 7-4 shows the block diagram of the circuitry.

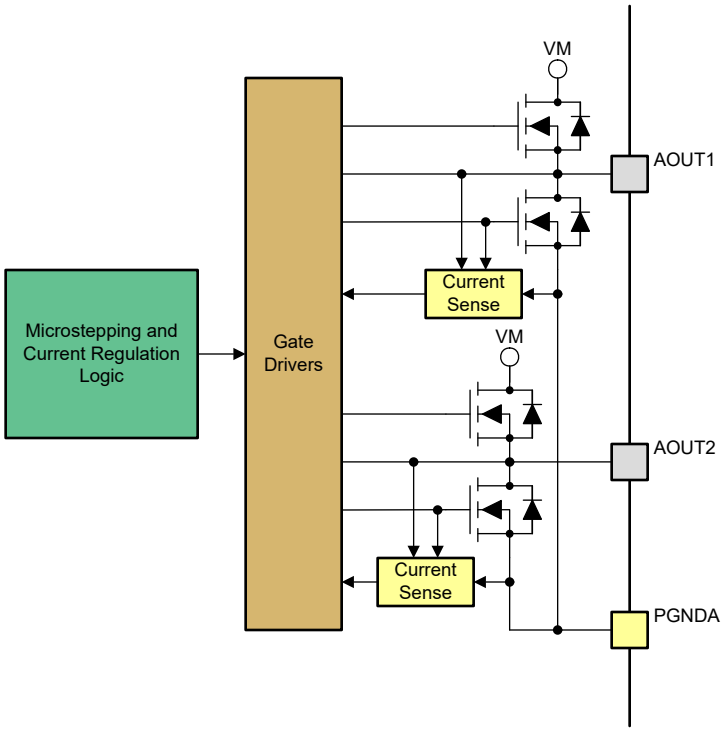

Figure 7-4. PWM Motor Driver Block Diagram

7.4.4 Microstepping Indexer

Built-in indexer logic in the device allows a number of different microstep modes. The MICROSTEP_MODE bits in the SPI register or the M0 and M1 pins are used to configure the step mode as shown in Table 7-5.

Table 7-5. Microstepping Indexer Settings

MODE = 1	MODE = 0		
MICROSTEP_MODE	M0	M1	STEP MODE
0000b	0	0	Full step (2-phase excitation) with 100% current
0001b	0	330 kΩ to GND	Full step (2-phase excitation) with 71% current
0010b	1	0	Non-circular 1/2 step
0011b	Hi-Z	0	1/2 step
0100b	0	1	1/4 step
0101b	1	1	1/8 step
0110b (default)	Hi-Z	1	1/16 step
0111b	0	Hi-Z	1/32 step
1000b	Hi-Z	330kΩ to GND	1/64 step
1001b	Hi-Z	Hi-Z	1/128 step

Table 7-5. Microstepping Indexer Settings (continued)

MODE = 1	MODE = 0		
MICROSTEP_MODE	M0	M1	STEP MODE
1010b	1	Hi-Z	1/256 step

Table 7-6 shows the relative current and step directions for full-step (71% current), 1/2 step, 1/4 step and 1/8 step operations. Higher microstepping resolutions follow the same pattern. The AOUT current is the sine of the electrical angle and the BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from the xOUT1 pin to the xOUT2 pin while driving.

Table 7-6. Relative Current and Step Directions

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	1	1		0%	100%	0.00
2				20%	98%	11.25
3	2			38%	92%	22.50
4				56%	83%	33.75
5	3	2	1	71%	71%	45.00
6				83%	56%	56.25
7	4			92%	38%	67.50
8				98%	20%	78.75
9	5	3		100%	0%	90.00
10				98%	-20%	101.25
11	6			92%	-38%	112.50
12				83%	-56%	123.75
13	7	4	2	71%	-71%	135.00
14				56%	-83%	146.25
15	8			38%	-92%	157.50
16				20%	-98%	168.75
17	9	5		0%	-100%	180.00
18				-20%	-98%	191.25
19	10			-38%	-92%	202.50
20				-56%	-83%	213.75
21	11	6	3	-71%	-71%	225.00
22				-83%	-56%	236.25
23	12			-92%	-38%	247.50
24				-98%	-20%	258.75
25	13	7		-100%	0%	270.00
26				-98%	20%	281.25
27	14			-92%	38%	292.50
28				-83%	56%	303.75
29	15	8	4	-71%	71%	315.00
30				-56%	83%	326.25
31	16			-38%	92%	337.50
32				-20%	98%	348.75

Table 7-7 shows the full step operation with 100% full-scale current. This stepping mode consumes more power than full-step mode with 71% current, but provides a higher torque at high motor RPM.

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Table 7-7. Full Step with 100% Current

FULL STEP 100%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	100	100	45
2	100	-100	135
3	-100	-100	225
4	-100	100	315

Table 7-8 shows the noncircular 1/2–step operation. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor RPM.

Table 7-8. Non-Circular 1/2-Stepping Current

NON-CIRCULAR 1/2-STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	–100	135
5	0	–100	180
6	–100	–100	225
7	–100	0	270
8	–100	100	315

When operating with SPI interface, the device allows stepping and direction change over SPI. Four bits are dedicated for this purpose -

- **SPI_DIR**:
  - When this bit is '0', the driver changes direction based on DIR pin inputs.
  - If this bit is '1', the direction changes depend on the DIR bit.
- **SPI_STEP**:
  - When this bit is '0', the stepping depends on the STEP pin inputs.
  - If this bit is '1', the step changes depend on the STEP bit.
- **DIR**: When SPI_DIR = '1' -
  - If DIR = '1', motor moves in the forward direction
  - If DIR = '0', motor moves in the reverse direction.
- **STEP**: When SPI_STEP = '1' -
  - If STEP = '1', the indexer advances by one step.
  - STEP bit is self-clearing, it becomes '0' after writing '1' to it.

When operating with the SPI interface, depending on the STEP_EDGE bit, STEP active edge can be either rising edge or both rising and falling edge, as shown in Table 7-9. When configured with H/W interface, the STEP active edge is only the rising edge. For applications that need to run at high input STEP rate, configuring both edges as active edge reduces controller overhead by half, because the input STEP rate is effectively doubled.

Table 7-9. STEP Active Edge

MODE	STEP_EDGE	STEP Active Edge
1	0b (default)	Rising edge
1	1b	Rising edge and falling edge
0	X	Rising edge

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At each active edge of the STEP input the indexer advances to the next state in the table. The direction shown is with the DIR pin logic high. If the DIR pin is logic low, the sequence table is reversed.

After power-up, after exiting logic undervoltage lockout, or after exiting sleep mode, the indexer moves to an initial excitation state (home position) of 45° electrical angle, corresponding to 71% of full-scale current in both coils. All the registers are restored to their deafult values in such scenario.

Note

- The production samples will feature an INDEX_RESET bit located in CTRL1 register bit 5. This bit will reset the indexer to 45° electrical angle, but the contents of the registers will not change. In pre-production samples, this bit will be reserved.
- If the step mode is changed dynamically while stepping, the indexer advances to the next valid state for the new step mode setting at the active edge of STEP.

If the STEP input frequency is jittery, the device filters the signal for the purpose of stall detection. The FRQ_CHG and STEP_FRQ_TOL bits program the filter setting, as shown in Table 7-10. 2% filtering means up to 2% jitter around the center frequency will be filtered out to generate a clean STEP signal for internal circuits to detect motor stall.

Table 7-10. STEP frequency filtering

FRQ_CHG	STEP_FRQ_TOL	Filtering
0 (default)	00	1%
	01 (default)	2%
	10	4%
	11	6%
1	Don't care	No filtering

7.4.5 Indexer Output

- A 10-bit INDEX_POS register indicates actual position in the microstep table for coil A current.
- 8 bit CUR_A register and CUR_A_SIGN bit indicate the microstep current for motor coil A for the position indicated by the INDEX_POS bits.
- 8 bit CUR_B register and CUR_B_SIGN bit indicate the microstep current for motor coil B.
- When the microstep indexer advances within the table through each possible value of the INDEX_POS bits, the actual current values in the motor coils can be calculated by -
  - Coil A current = I_{FS} x sin (90° x CUR_A / 255)
  - Coil B current = I_{FS} x sin (90° x CUR_B / 255)
  - Current will be positive if the corresponding sign bit is '1' and negative if the sign bit is '0'
- CUR_A and CUR_B become initialized to 0 and 255 respectively whenever INDEX_POS passes zero.

The following table shows the outputs of the indexer registers for a current waveform corresponding to 1/256 microstepping.

Table 7-11. Indexer Output Table

Current Quadrant	INDEX_POS	CUR_A	CUR_A_SIGN	CUR_B	CUR_B_SIGN
First (0° -> 90°)	0 -> 255	0 -> 255	1	255 -> 0	1
Second (90° -> 180°)	256 -> 511	255 -> 0	1	0 -> 255	0
Third (180° -> 270°)	512 -> 767	0 -> 255	0	255 -> 0	0
Fourth (270° -> 360°)	768 -> 1023	255 -> 0	0	0 -> 255	1

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The Indexer outputs together with the nHOME signal allow determination of the motor position within the electrical wave. They can be compared with an encoder output to detect discrepancies in the movement of the motor - such as detecting step loss.

Note

In production samples, the INDEX_POS bits will output the actual coil A current -> sin (90° x CUR_A / 255).

7.4.5.1 nHOME Output

When the microstepping indexer reaches the home position (electrical angle of 45°), corresponding to 71% of full-scale current in both coils, the open-drain nHOME output is pulled low. At all other times, the nHOME output will be pulled high. When the device operates with SPI interface, additionally the NHOME bit in SPI register goes low when the indexer reaches home position.

Therefore, the nHOME output gives one low pulse per electrical rotation, i.e. one pulse per each four fullsteps, as shown in Figure 7-5. The nHOME low pulse thus corresponds to a defined position of the motor for every four fullsteps. A more precise homing of the motor can be achieved by combining nHOME with a mechanical home switch.

Pull up the nHOME to a 5-V, 3.3-V or 1.8-V supply using a pull-up resistor. For a 5-V pullup, the nHOME pin can be tied to the DVDD pin with a resistor. For a 3.3-V or 1.8-V pullup, an external supply must be used.

Traces from top to bottom: BOUT2, BOUT1, coil B current, coil A current, nHOME

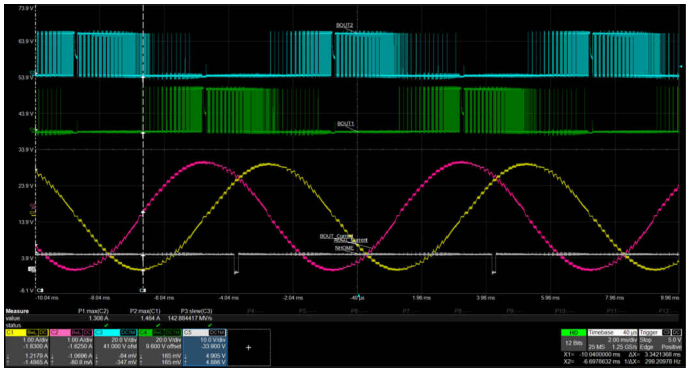

Figure 7-5. nHOME Pin Waveform

7.4.6 Automatic Microstepping Mode

When the DRV8462 is operating with SPI interface, automatic microstepping mode interpolates the input step pulses to generate a current waveform corresponding to higher resolution microstep. This results in smooth sinusoidal current and noiseless operation at any step frequency.

The EN_AUTO bit should be '1' to enable the automatic microstepping mode.

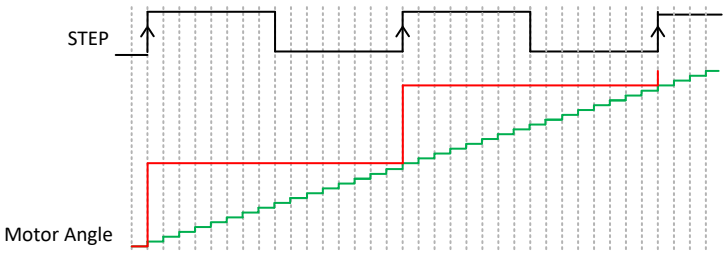

Figure 7-6. Automatic Microstepping Interpolation

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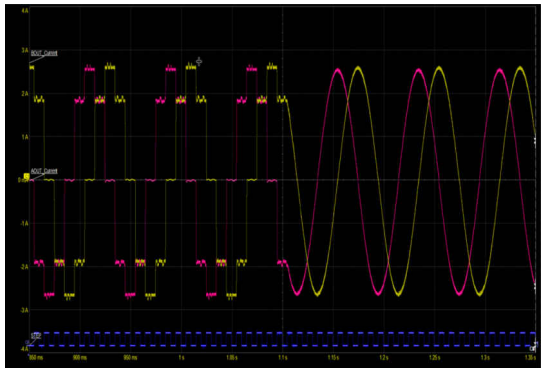
Figure 7-6 shows increment in motor angle with and without automatic microstepping. Without automatic microstepping (red plot), the motor angle increments by a large amount on every step input active edge. Automatic microstepping (green plot) results in a much smoother change in motor angle.

The DRV8462 supports interpolation to 1/32, 1/64, 1/128 or 1/256 microstepping levels, configured by the RES_AUTO bits as shown in Table 7-12. The interpolation setting can be changed on the fly.

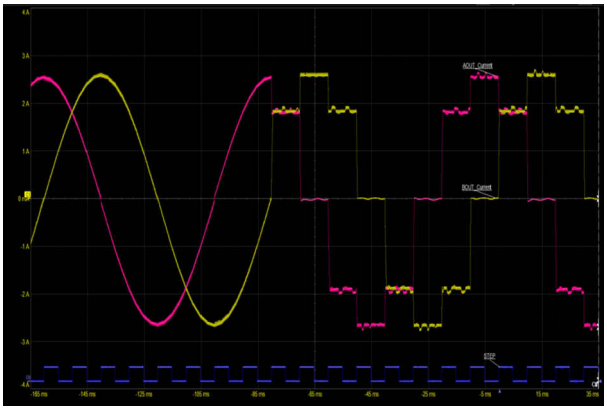
Table 7-12. Automatic Microstepping Interpolation Level

RES_AUTO	Interpolation
00 (default)	1/256
01	1/128
10	1/64
11	1/32

The following scopeshots show both coil currents and the smooth transition between half-step mode and automatic microstepping mode by writing '1' and '0' respectively to the EN_AUTO bit. Notice that the step frequency is same in both half-step and 1/256 automatic microstepping modes.



Transition from half-step mode to 1/256 automatic microstepping



Transition from 1/256 automatic microstepping to half-step mode

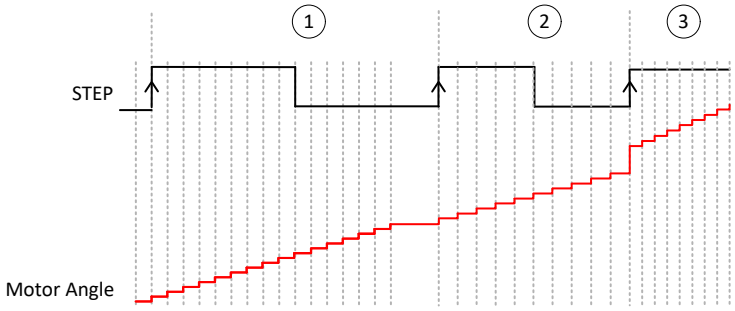


Figure 7-7. Automatic Microstepping with Changing STEP Frequency

As shown in Figure 7-7, the interpolation is done based on the time between the two previous step pulses. The previous interval time is interpolated to equal divisions, depending on the RES_AUTO bit setting.

When input step frequency reduces from previous interval (shown in segment '1'), the motor holds its position till the next STEP active edge occurs. Device will go to standstill power saving mode if the EN_STSL bit is '1', and the next active edge does not come before t_{STSL_DLY} expires. Standstill power saving mode is exited on the next STEP active edge.

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When step frequency increases from previous interval (shown in segment '2'), the motor angle auto-corrects when the next STEP active edge comes, because the indexer moves to a position corresponding to the STEP input. In segment '3', the motor angle is incremented at a faster rate, corresponding to the step frequency of segment '2'.

If automatic microstepping is disabled, the system controller will be forced to output high frequency STEP signals to generate current waveforms corresponding to 1/256 microstep. When automatic microstepping is enabled, smooth current waveform can be generated by low frequency STEP signals. This drastically reduces controller overhead and is beneficial for applications such as 3D printer, factory automation and medical. It should be ensured that the interpolated frequency does not fall in the resonant frequency band of the stepper motor. The frequency of the STEP input in automatic microstepping mode should not exceed 300 kHz.

7.4.7 Custom Microstepping Table

The performance and audible noise of any stepper motor system depends on the torque ripple generated by both the motor and the load. The torque ripple is defined by the variation in torque at each microstep. For most stepper motors, the standard sinusoidal microstep indexer is sufficient to achieve acceptable torque ripple and a good performance.

However, for some motor and load torque combinations, altering the current profile can reduce torque ripple, resulting in lower vibration and audible noise. When properly programmed, the customized current waveform ensures equally distanced microstep positions with constant torque and therefore also the best positional accuracy.

For example, in case of permanent magnet motors, variations in torque are more prominent due to larger step angle (3.6° to 18°) than that of hybrid motors (0.9° or 1.8°). Due to fewer number of stator teeths, less amount of flux interacts between the stator teeth and the rotor when the rotor is in between two stator teeths. If the current level is increased at these intermediate positions, the torque ripple will be lower compared to the default sinusoidal indexer.

The DRV8462 features a lookup table for tailoring the microstepping current profile to suit the requirements of a specific motor. The modified current profile is used in place of the default sinusoidal profile by writing '1' to the EN_CUSTOM bit. The frequency of the STEP input in custom microstepping mode should not exceed 300 kHz. The details of the interpolation process is described below -

- The user should program the current (% of TRQ_DAC) corresponding to the first quadrant of coil A current in a 1/8 microstepping setting.
- These current values are stored in CUSTOM_CURRENT1 to CUSTOM_CURRENT8 registers.
- The position for these current values correspond to 11.25°, 22.5°, 33.75°, 45°, 56.25°, 67.5°, 78.75° and 90° electrical angles.
- The current value for 0° position is assumed to be zero.
- The nine current values (including 0% full-scale current) are interpolated to a total of 256 points using a piecewise-linear approach to build the complete current waveform. The interpolated waveform always corresponds to 1/256 microstep, irrespective of the programmed microstepping mode.
- The values for the first quadrant are then mirrored and repeated for the other three quadrants of coil A and again for the four quadrants of coil B current to construct the complete current waveform.

Table 7-13 shows an example of the user inputs.

Table 7-13. Custom Microstepping Table Values

Position (degrees)	Sine Indexer Value	Modified Value (CUSTOM_CURRENTx)
0	0	0
11.25	49.7	24
22.5	97.6	56
33.75	141.7	96
45	180.3	152
56.25	212	192

Table 7-13. Custom Microstepping Table Values (continued)

67.5	235.6	224
78.75	250.1	240
90	255	255

Figure 7-8 shows the corresponding modified current waveform (red plot) of coil A for one full electrical angle, compared to waveform generated by sine indexer (blue plot).

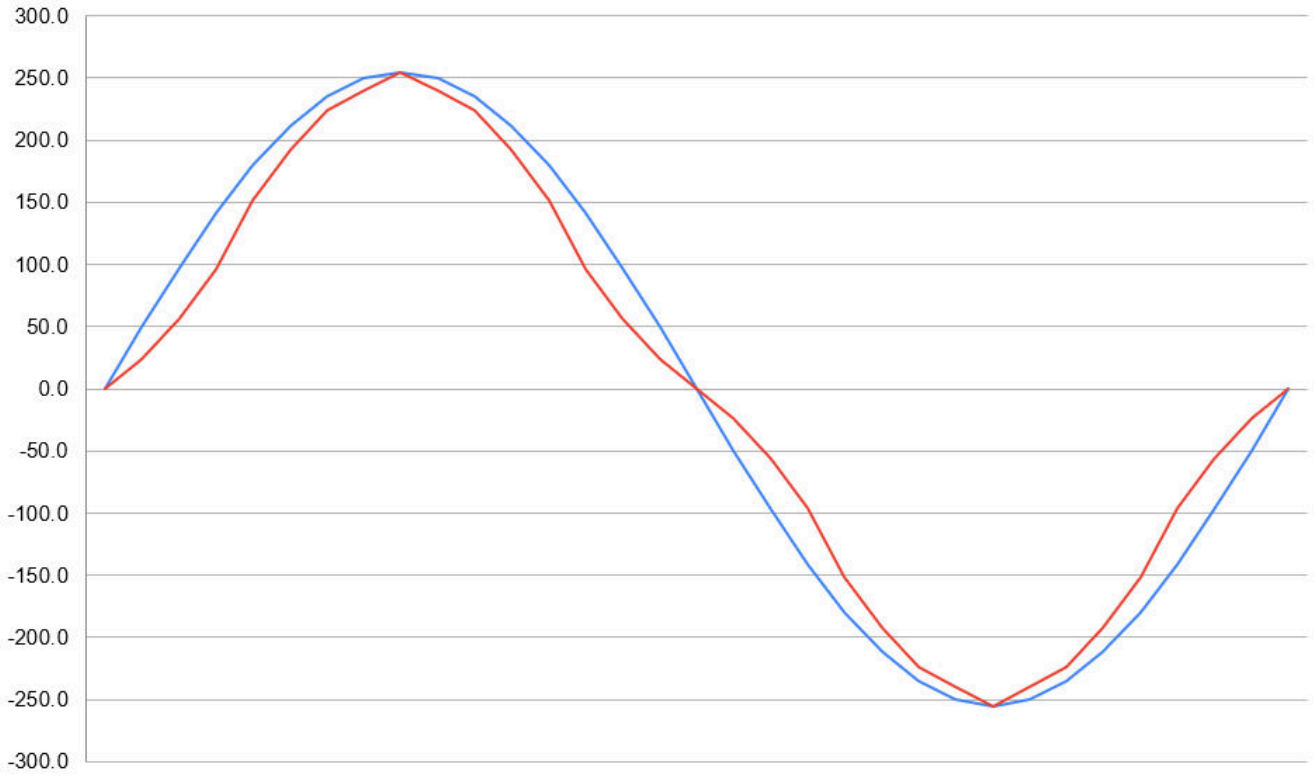

Figure 7-8. Customizable Microstepping

7.4.8 Current Regulation

The current through the motor windings is regulated by a PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for the OFF time to decrease the current. After the off-time expires, the bridge is re-enabled, starting another PWM cycle.

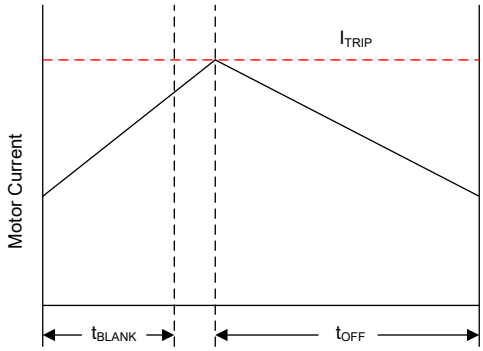

Figure 7-9. Current Chopping Waveform

The PWM regulation current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. When the device is configured with H/W interface, the current sense MOSFETs are biased with a reference current that is the output of a current-mode sine-weighted DAC whose full-scale reference current is set by the voltage at the VREF pin. When operating with SPI interface, two registers (TRQ_DAC and ISTSL) can further scale the reference current.

Use Equation 1 to calculate the full-scale regulation current for H/W interface.

$$I_{FS}\ (A) = VREF\ (V) / K_V\ (V/A) \quad (1)$$

For the SPI interface, the 8-bit TRQ_DAC register further scales the full-scale current as follows -

$$I_{FS}\ (A) = VREF\ (V) \times TRQ\_DAC / K_V\ (V/A) \quad (2)$$

Table 7-14. TRQ_DAC Settings

TRQ_DAC	CURRENT SCALAR
11111111b	100%
11111110b	99.61%
11111101b	99.22%
11111100b	98.83%
.....	.....
00000000b	0.39%

Another 8-bit register ISTSL programs the holding current (I_{HOLD}) when STEP pulses are not applied and the motor is being held at same position. Transitioning to a lower value of holding current reduces motor and driver power loss. See Standstill Power Saving Mode for details.

$$I_{HOLD}\ (A) = VREF\ (V) \times ISTSL / K_V\ (V/A) \quad (3)$$

Table 7-15. ISTSL Settings

ISTSL	Holding Current Value
11111111b	100%
11111110b	99.61%
11111101b	99.22%
11111110b	98.83%
.....	.....
00000000b	0.39%

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Note

Always set ISTSL to a value lower than the TRQ_DAC value.

7.4.9 Internal Reference Voltage

When operating with the SPI interface, the DRV8462 features an internal 3.3V reference voltage by writing '1' to the VREF_INT_EN bit. The voltage on the VREF pin will be ignored in this case, and the VREF pin can be left open or connected to ground.

The full-scale current and the holding current will be calculated as -

$$I_{FS}\ (A) = 3.3\ V \times TRQ\_DAC / K_V\ (V/A) \quad (4)$$

$$I_{HOLD}\ (A) = 3.3\ V \times ISTSL / K_V\ (V/A) \quad (5)$$

Using the internal 3.3V as reference for setting full-scale current and holding current will save BOM cost by eliminating the two resistors connected to the VREF pin.

Note

The VREF_INT_EN bit is located in ATQ_CTRL18 register bit 5 in pre-production samples. For production samples, the VREF_INT_EN bit will be located in CTRL13 register bit 1.

7.4.10 Current Regulation Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7-10, Item 1.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, as soon as the PWM chopping current level is reached, the H-bridge reverses state by switching on the opposite arm MOSFETs to allow the winding current to flow in the opposite direction. As the winding current approaches zero, the H-bridge is disabled to prevent further reverse current flow. Fast decay mode is shown in Figure 7-10, item 2. In slow decay mode, the winding current is re-circulated by enabling both low-side MOSFETs in the H-bridge. This is shown in Figure 7-10, Item 3.

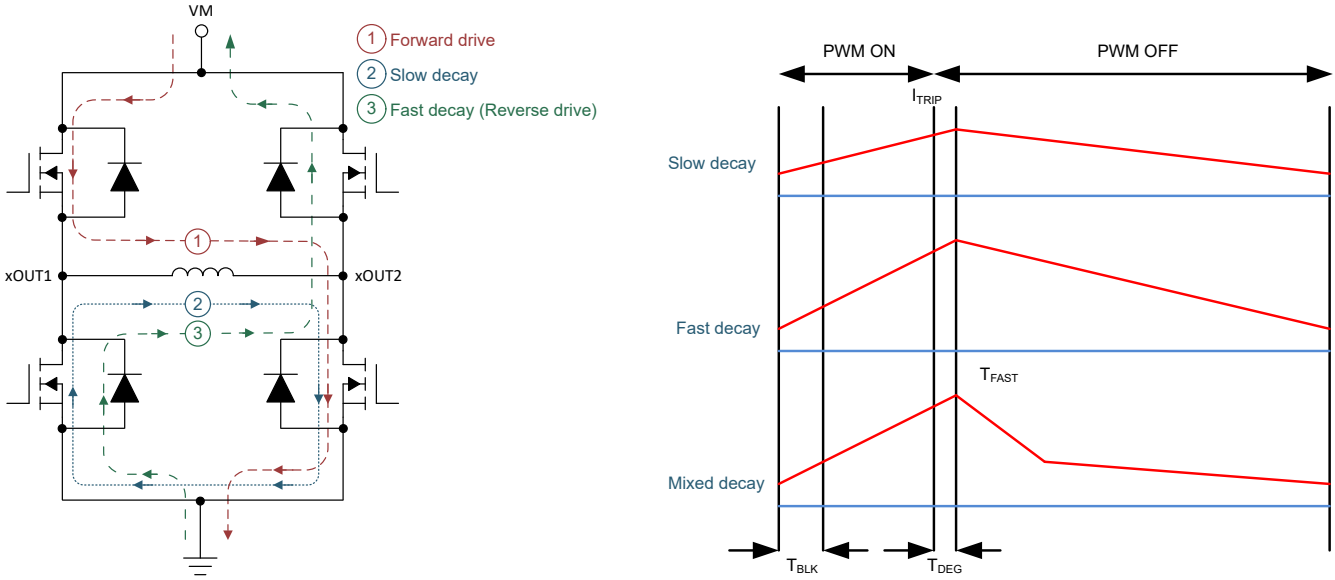

Figure 7-10. Decay Modes

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The decay mode is selected by the DECAY register or the DECAY0 and DECAY1 pins, as shown in Table 7-16. The decay modes can be changed on the fly. In full step and noncircular 1/2-step, the decay mode corresponding to decreasing steps is always used.

Table 7-16. Decay Mode Settings

SPI Interface	H/W Interface		INCREASING STEPS	DECREASING STEPS
DECAY	DECAY0	DECAY1		
000b	Hi-Z	1	Reserved	
001b	1	1	Slow decay	Mixed decay: 30% fast
010b	0	Hi-Z	Slow decay	Mixed decay: 60% fast
011b	1	Hi-Z	Slow decay	Fast decay
100b	1	0	Mixed decay: 30% fast	Mixed decay: 30% fast
101b	Hi-Z	0	Mixed decay: 60% fast	Mixed decay: 60% fast
110b	0	0	Smart tune Dynamic Decay	Smart tune Dynamic Decay
111b (default)	0	1	Smart tune Ripple Control	Smart tune Ripple Control

Figure 7-11 defines increasing and decreasing current.

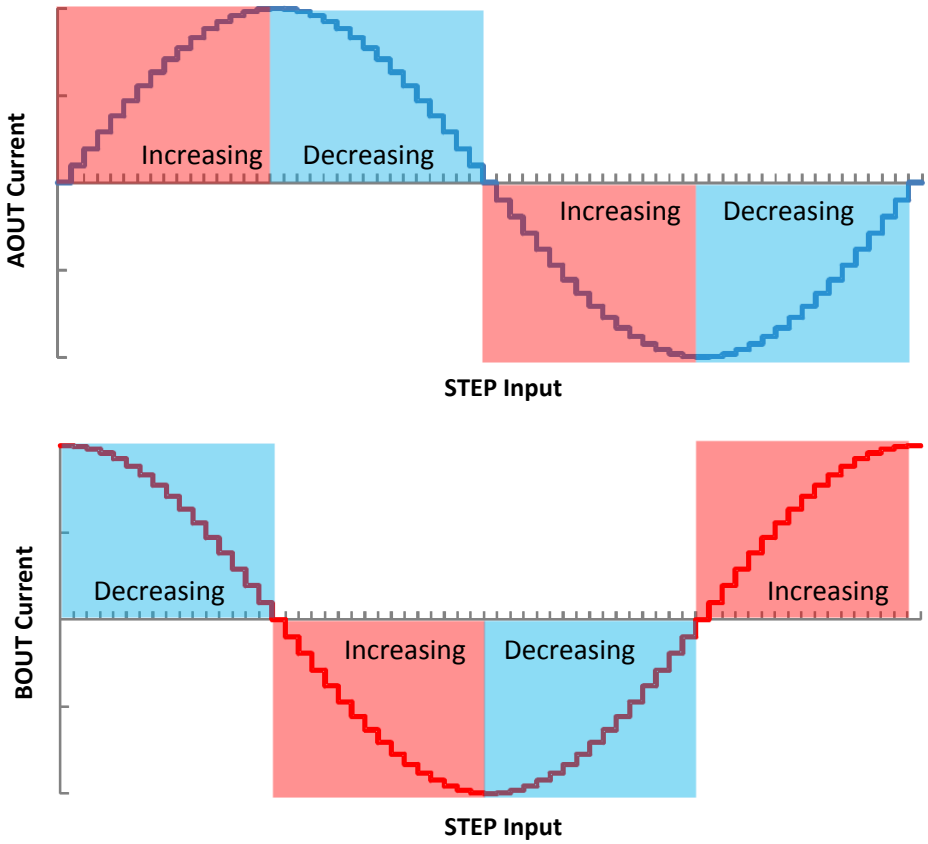

Figure 7-11. Definition of Increasing and Decreasing Steps

Note

For the pre-production samples, the DECAY = '000' or DECAY0 = Hi-Z, DECAY1 = 1 condition is reserved. In production samples, this option will enable slow decay for both increasing and decreasing steps.

The DRV8462 also features the silent step decay mode for ultra-silent operation at low speed and standstill. See Silent step decay mode for details.

7.4.10.1 Slow Decay for Increasing Current, Fast Decay for Decreasing Current

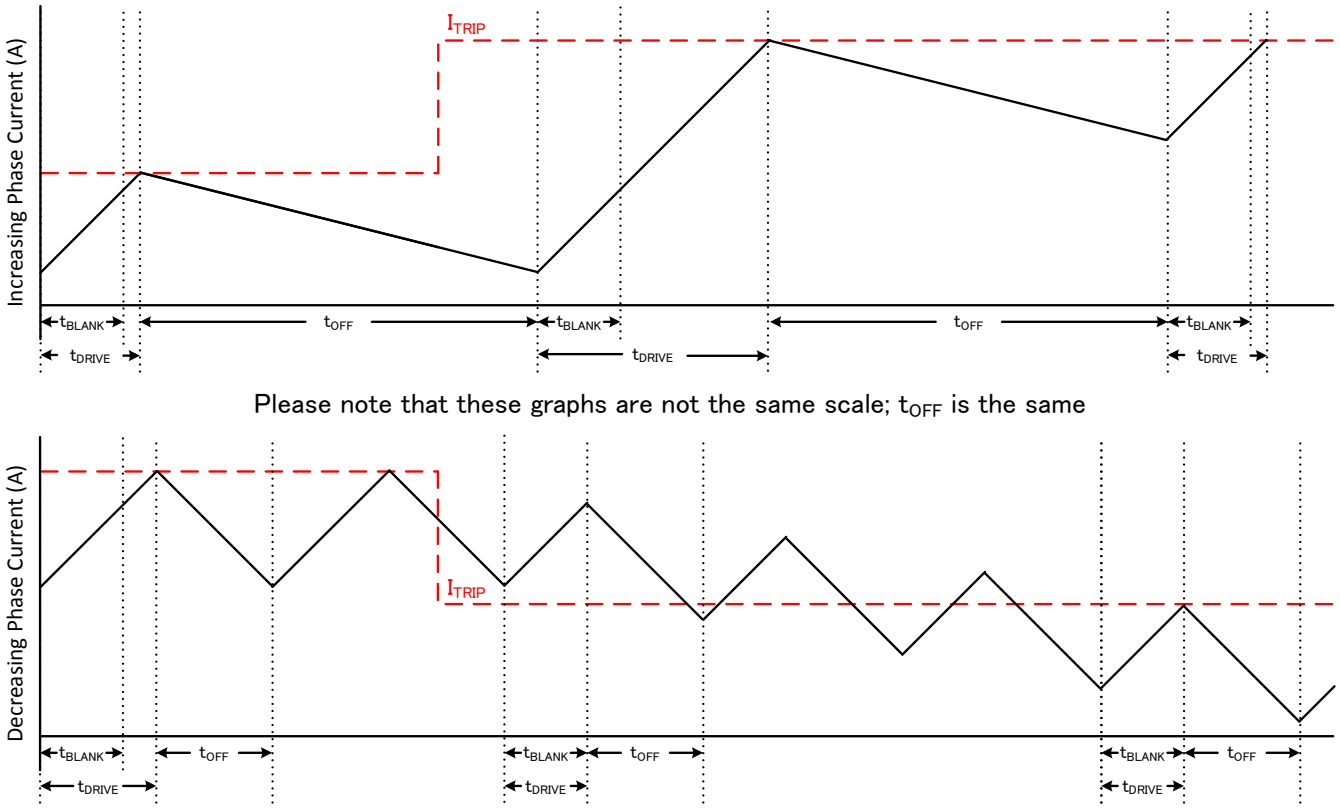

Figure 7-12. Slow/Fast Decay Mode

During fast decay, the polarity of the H-bridge is reversed. The H-bridge will be turned off as current approaches zero in order to prevent current flow in the reverse direction. In this mode, fast decay only occurs during decreasing current. Slow decay is used for increasing current.

Fast decay exhibits the highest current ripple of the decay modes for a given t_{OFF}. Transition time on decreasing current steps is much faster than slow decay since the current is allowed to decrease much faster.

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7.4.10.2 Slow Decay for Increasing Current, Mixed Decay for Decreasing Current

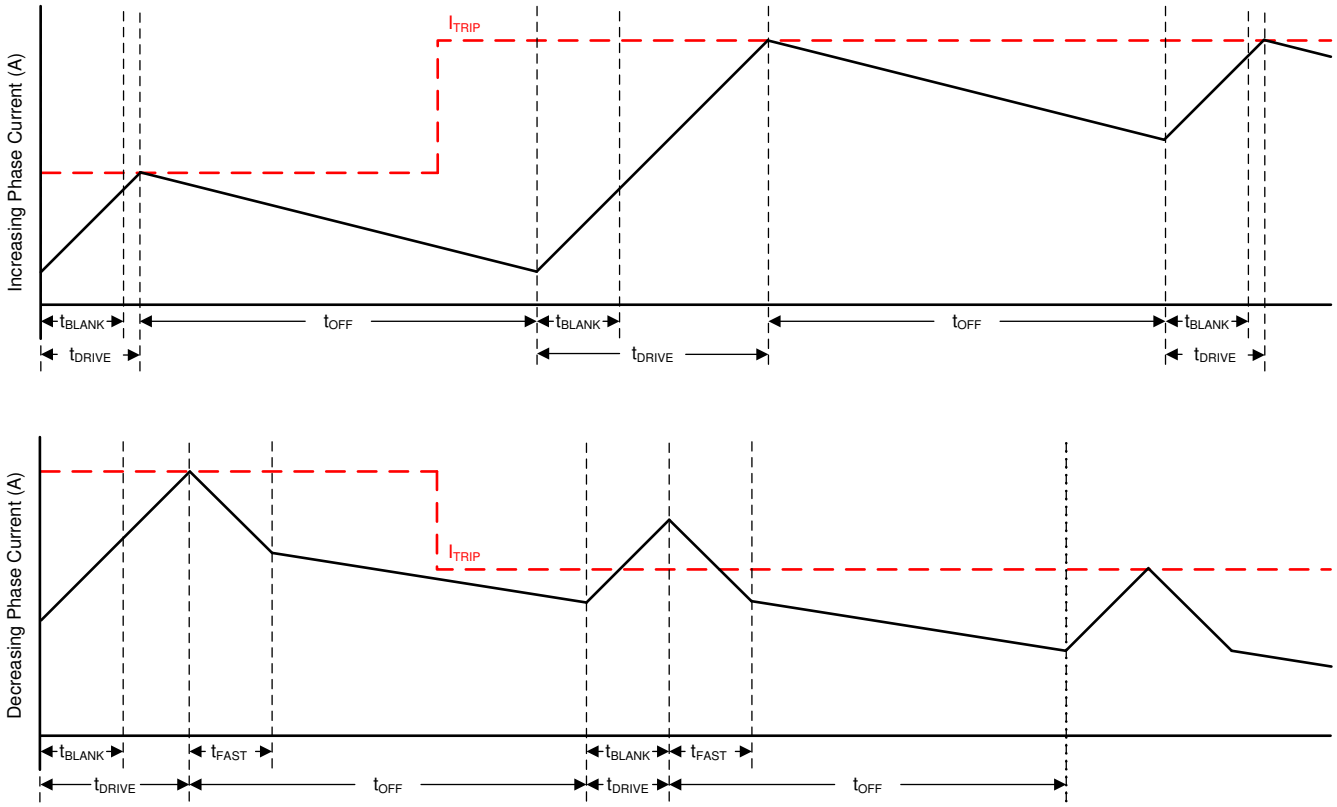

Figure 7-13. Slow-Mixed Decay Mode

Mixed decay begins as fast decay for an initial duration of the t_{OFF}, followed by slow decay for the remainder of the t_{OFF} time. Mixed decay only occurs during decreasing current. Slow decay is used for increasing current.

This decay mode exhibits the same current ripple as slow decay mode does for increasing current, because for increasing current, only slow decay is used in this mode. For decreasing current, the ripple is larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

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7.4.10.3 Mixed Decay for Increasing and Decreasing Current

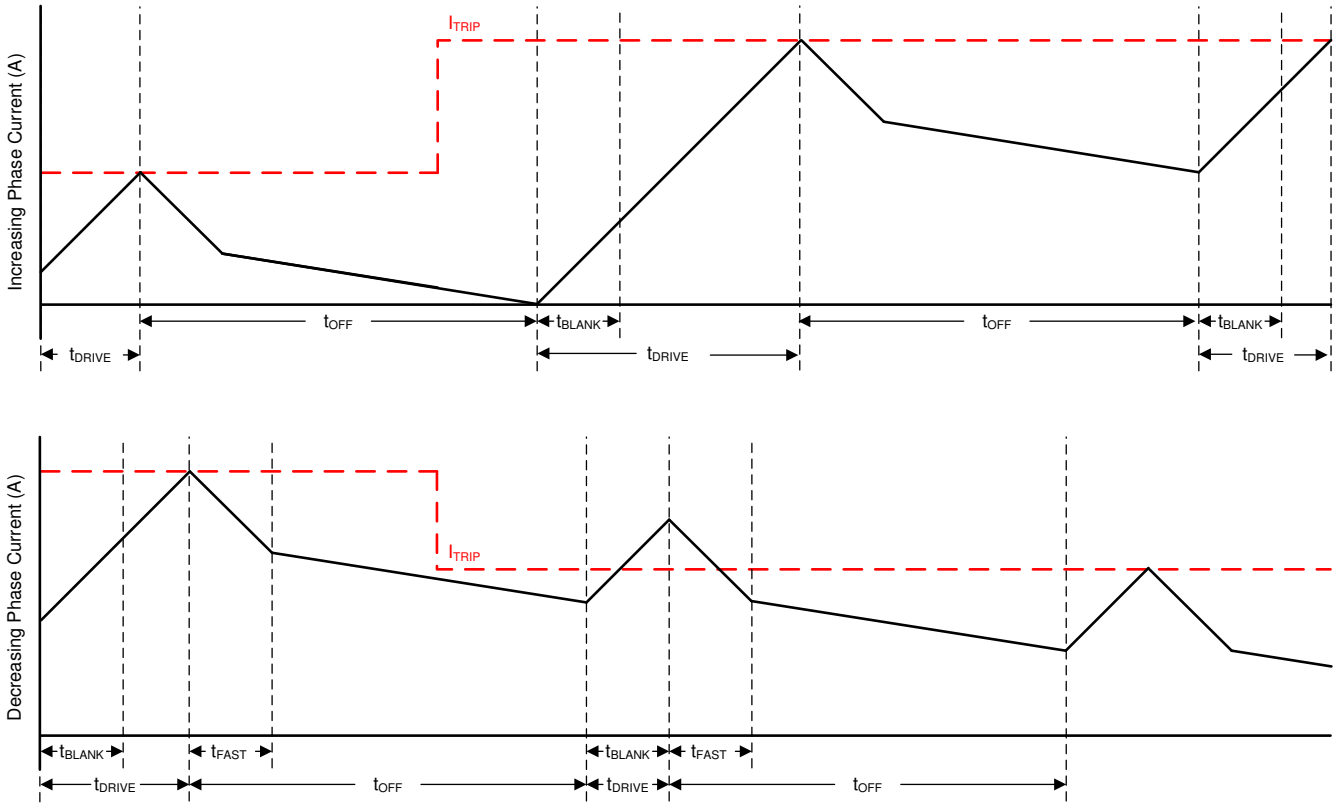

Figure 7-14. Mixed-Mixed Decay Mode

Mixed decay begins as fast decay for an initial duration of the t_{OFF} time, followed by slow decay for the remainder of t_{OFF} time. In this mode, mixed decay occurs for both increasing and decreasing current steps.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

When the winding current is held static for a long time (for example while no STEP input is present) or at very low step rates, slow decay may not properly regulate the current because back-EMF will be small or absent across the motor windings. In this case the motor current can rise rapidly and require an extremely long off-time to regulate the current. Increasing and decreasing current mixed decay mode allows the current to stay in regulation when no back-EMF is present across the motor windings.

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7.4.10.4 Smart tune Dynamic Decay

The smart tune current regulation schemes are advanced current-regulation control methods compared to traditional fixed off-time current regulation schemes. Smart tune current regulation schemes help the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Motor back-EMF difference on rising and falling steps
- Step transitions
- Low-current versus high-current dI/dt

The device provides two different smart tune current regulation modes, named smart tune Dynamic Decay and smart tune Ripple Control.

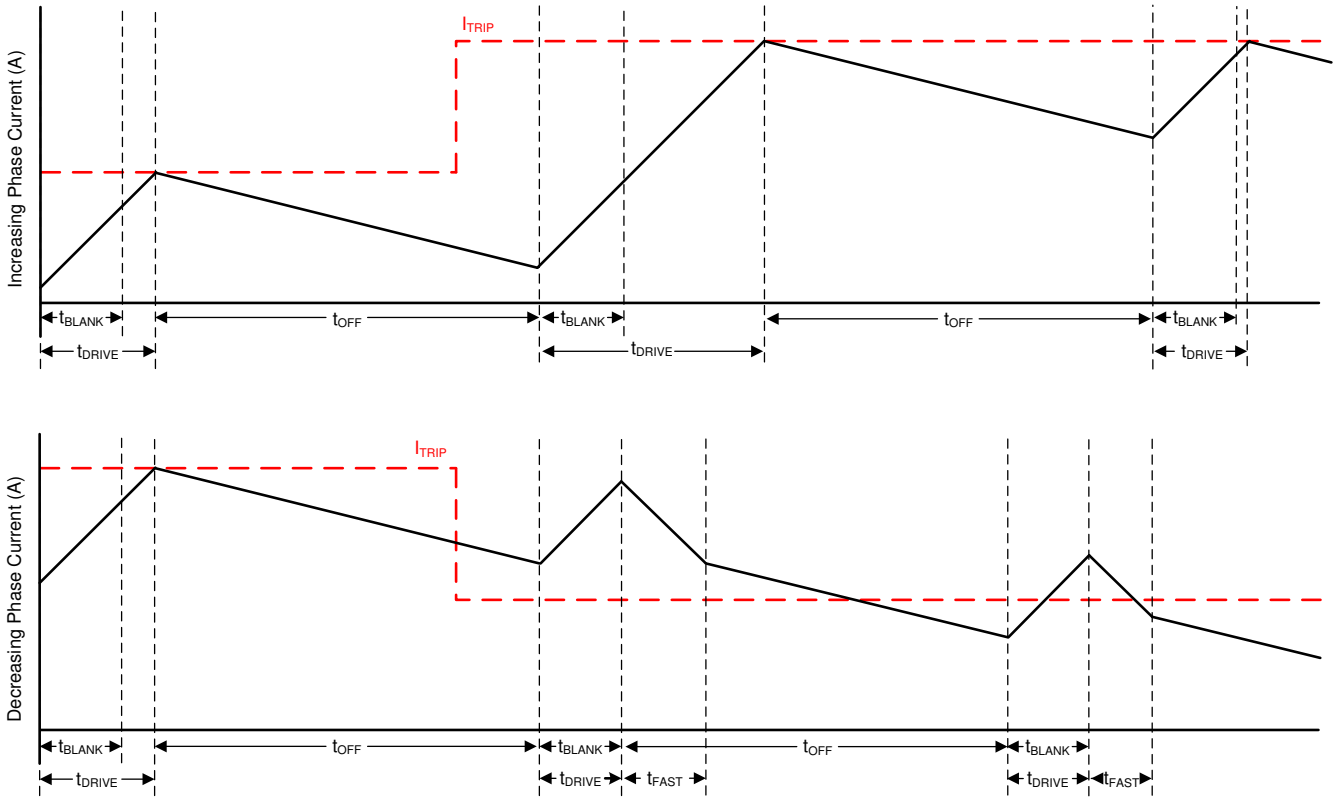

Figure 7-15. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

7.4.10.5 Smart tune Ripple Control

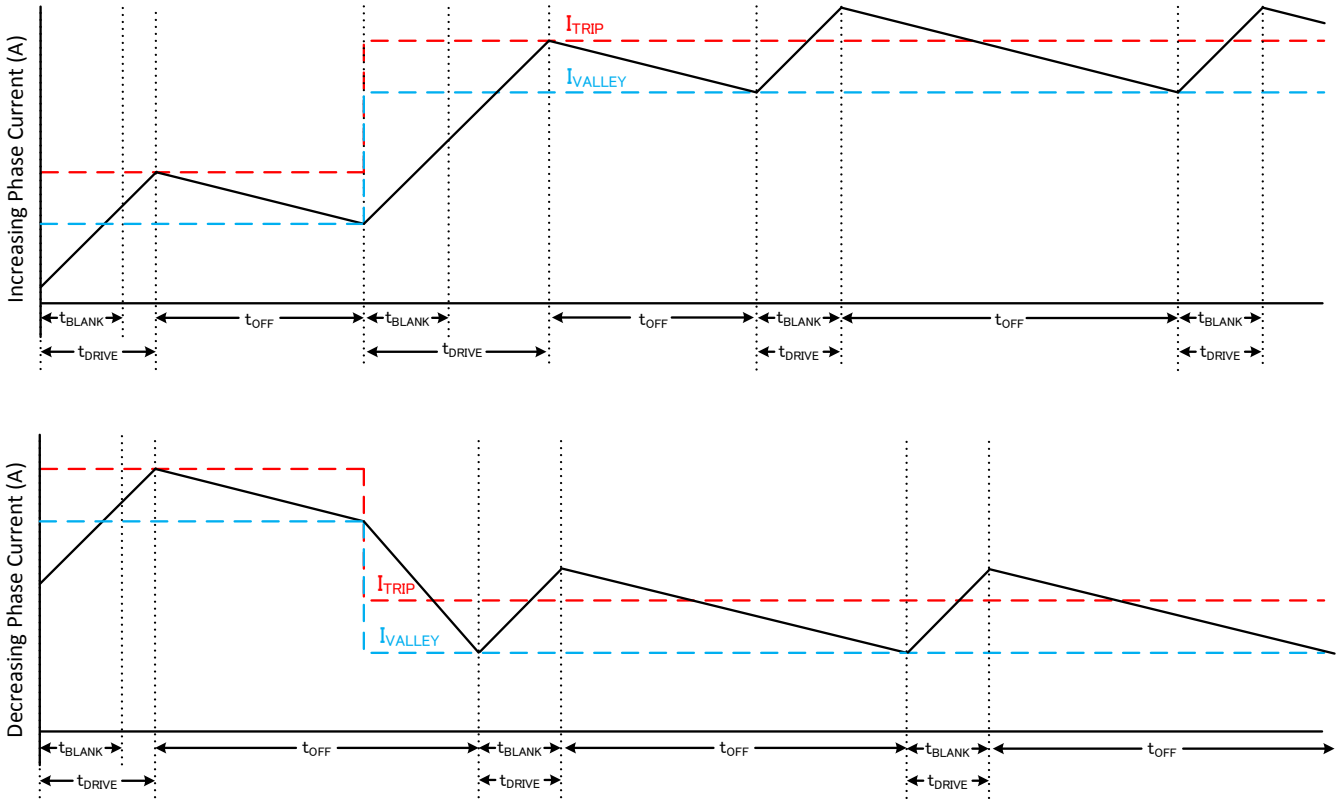

Figure 7-16. Smart tune Ripple Control Decay Mode

Smart tune Ripple Control operates by setting an I_{VALLEY} level along with the I_{TRIP} level. When the current level reaches I_{TRIP}, instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached. Slow decay operates similar to slow/slow decay where both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, t_{OFF} is variable depending on the current level and operating parameters.

The ripple current in smart tune ripple control mode is programmed by the RC_RIPPLE[1:0] bits or the TOFF pin, as shown below.

Table 7-17. Current Ripple Settings

MODE = 0, H/W Interface	MODE = 1, SPI Interface	Current Ripple at a specific microstep level
TOFF	RC_RIPPLE	
0	00b	25 mA + 1% of I_{TRIP}
1	01b	25 mA + 2% of I_{TRIP}
Hi-Z	10b	25 mA + 4% of I_{TRIP}
330kΩ to GND	11b	25 mA + 6% of I_{TRIP}

The ripple control method allows much tighter regulation of the current level, thereby increasing motor efficiency and system performance. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve low current ripple with current regulation. Select a lowest possible ripple current setting that ensures the PWM frequency does not fall in the audible range (< 20 kHz).

7.4.10.6 PWM OFF Time

The TOFF bits or the TOFF pin configure the PWM OFF time for all decay modes except smart tune ripple control and silent step decay modes, as shown in Table 7-18. The OFF time settings can be changed on-the-fly.

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Table 7-18. OFF Time Settings

MODE = 1, SPI Interface	MODE = 0, H/W Interface	OFF Time
TOFF	TOFF	
00b	0	7 µs
01b	1	16 µs
10b	Hi-Z	24 µs
11b	330kΩ to GND	32 µs

7.4.10.7 Current Regulation Blanking Time and Deglitch Time

After the current is enabled (start of drive phase) in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM.

- When the device operates with hardware interface, the blanking time is fixed at 1.5 µs.
- When the device is operating with SPI interface, the blanking time can be programmed by the TBLANK_TIME bits, with a default value of 1.5 µs.

Table 7-19. TBLANK_TIME Settings

TBLANK_TIME	Blanking Time
00	1 µs
01	1.5 µs
10	2 µs
11	2.5 µs

When the current is close to the I_{TRIP} level, a 0.5 µs deglitch time ensures proper current regulation.

7.4.11 Current Sensing with External Resistor

PWM current regulation is based on the voltage sensed across the internal sense resistor of the DRV8462. Optional external resistors can be placed between the PGND pins and system ground (or in series with the VM pins) to sense the coil current, as shown in Figure 7-17. The DRV8462 has two PGNDA pins and two PGNDB pins - one pair for each H-bridge. So, the current of each stepper motor coil can be sensed separately by placing sense resistors between PGND pins and system ground. All the four VM pins are shorted internally - so if a sense resistor is placed in the VM path, it will sense the combined current of both the H-bridges.

The voltage drop across the external sense resistor should not exceed 300 mV. The sensed coil current can be processed to monitor motor health, or used to generate necessary signals in a field-oriented-control loop to improve overall system efficiency.

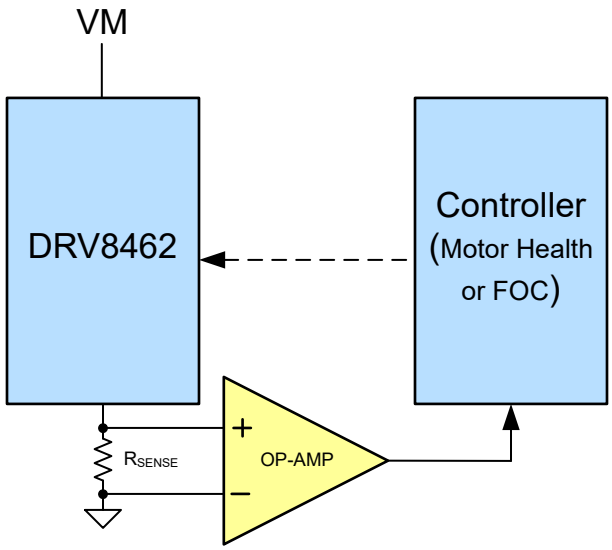

Figure 7-17. Current Sensing with External Resistor

No current flows through the sense resistor during the slow decay, so the sense resistor conducts less than the coil RMS current. Place the sense resistors as close as possible to the corresponding IC pins. Use a symmetrical sense resistor layout to ensure good matching. Low-inductance sense resistors should be used to prevent voltage spikes and ringing. For optimal performance, the sense resistor should be a surface-mount resistor rated for high enough power.

7.4.12 Silent step decay mode

Conventional peak current mode control looks at instantaneous current in the sensing MOSFETs to determine drive and decay durations. As a result, the motor driver reacts to instantaneous inaccuracies in the system. These sudden changes in current cause audible noise from the motor.

To ensure noiseless stepper motor operation, the DRV8462 features the silent step decay mode. The silent step is a voltage mode PWM regulation scheme to remove noise due to PWM switching at standstill and low speeds. Thus, silent step operated stepper motor applications are highly suitable for applications such as 3D printer, medical equipment and factory automation.

Note

When the device is operating in silent step decay mode, open-load fault detection and stall detection are not supported, and spread spectrum feature is disabled.

The silent step loop is designed with low bandwidth, therefore at moderate to high motor speeds, the decay mode can be switched back to one of the conventional current-mode decay schemes programmed by the DECAY bits. Transition from silent step to another decay mode is immediate, whereas the transition from other decay modes to silent step happens at the boundary of electrical half-cycles.

Figure 7-18 shows the block diagram of the silent step decay mode implementation -

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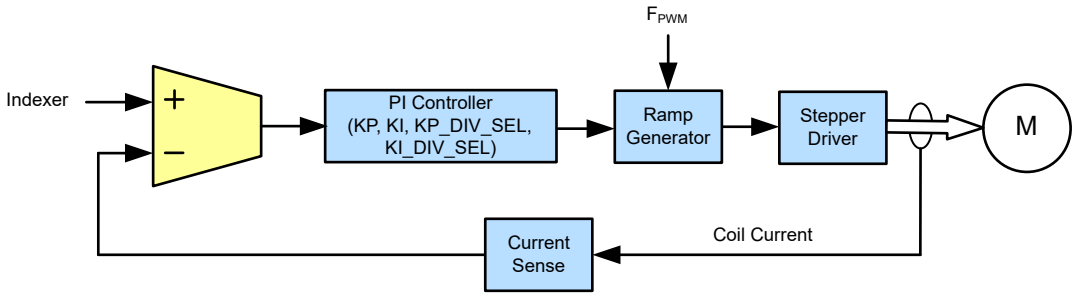

Figure 7-18. Silent step block diagram

Table 7-20 shows the SPI register parameters related to the silent step decay mode.

Table 7-20. Silent step Parameter Table

Parameter	Description
EN_SS	When EN_SS bit is '1', silent step decay mode is enabled. Device starts operating with silent step after one zero cross each for currents in coil A and coil B.
SS_PWM_FREQ	Represents the PWM frequency (F_{PWM}) in silent step decay mode. '00' = 25 kHz '01' = 33 kHz '10' = 42 kHz '11' = 50 kHz Default value of F_{PWM} is 25 kHz. Higher PWM frequency results in higher switching loss.
SS_KP	Represents the proportional gain of the silent step PI controller. Has a range of 0 to 127.
SS_KI	Represents the integral gain of the silent step PI controller. Has a range of 0 to 127.
SS_KP_DIV_SEL	Divider factor for KP. Actual KP = SS_KP / SS_KP_DIV_SEL. **000b - SS_KP/32** 001b - SS_KP/64 010b - SS_KP/128 011b - SS_KP/256 100b - SS_KP/512 101b - SS_KP/16 110b - SS_KP
SS_KI_DIV_SEL	Divider factor for KI. Actual KI = SS_KI / SS_KI_DIV_SEL. **000b - SS_KI/32** 001b - SS_KI/64 010b - SS_KI/128 011b - SS_KI/256 100b - SS_KI/512 101b - SS_KI/16 110b - SS_KI
SS_THR	Programs the frequency at which the device transitions from silent step decay mode to another decay mode programmed by the DECAY bits. This frequency corresponds to the frequency of the sinusoidal current waveform. 00000001b = 2 Hz 00000010b = 4 Hz . . **11111111b = 510 Hz**

To convert the SS_THR threshold to STEP frequency (f_{STEP}) for a specified microstepping setting, the following formula should be used -

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$$f_{STEP} = (SS\_THR * 1000 * usm) / 256 \quad (6)$$

Where usm corresponds to the number of microsteps (4, 16, 256 etc.). When the device is operating with custom microstepping mode, use usm = 256 in Equation 6 when calculating the STEP frequency.

The gain vs frequency plot of the silent step loop is shown in Figure 7-18 -

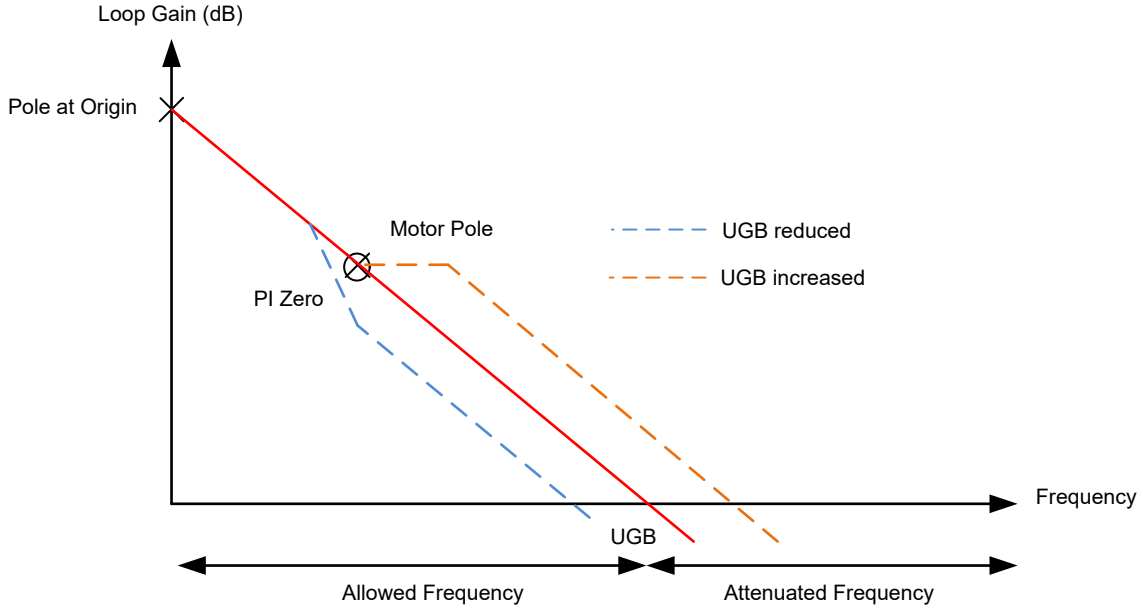

Figure 7-19. Silent step Gain vs. Frequency

The loop transfer function has two poles and one zero -

- One pole at origin
- One pole (f_P) due to the motor coil resistance and inductance -

$$f_P = R_{MOTOR} / (2 * \pi * L_{MOTOR}) \quad (7)$$

- One zero (f_Z) created by the PI loop

$$f_Z = (KI * F_{PWM}) / (2 * \pi * KP) \quad (8)$$

The proportional gain KP should be chosen to achieve the desired loop gain. Use the following equation to calculate the KP -

$$\mathbf{KP = 20 * \pi * UGB * L_{MOTOR} / VM} \text{ - for DDV package} \quad (9)$$

$$\mathbf{KP = 10 * \pi * UGB * L_{MOTOR} / VM} \text{ - for DDW package} \quad (10)$$

Where UGB is the unity-gain bandwidth of the loop, R_{MOTOR} is the motor coil resistance, L_{MOTOR} is the motor coil inductance, I_{FS} is the full-scale current and VM is the supply voltage.

- If any frequency is less than UGB, it is allowed to propagate.
- Frequencies higher than UGB, such as PWM frequency or STEP frequency are attenuate and do not contribute to motor noise.
- 200 Hz is a reasonable choice for UGB to attenuate most frequencies in the audible range.
- In the event of supply voltage change, UGB can be changed by modifying the value of KP. This way similar audio noise suppression can be achieved across a wide range of operating conditions.
- If the zero is chosen to be at a lower frequency than the motor pole, UGB will increase, as shown in Figure 7-18.

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The zero should be placed to cancel the motor pole. By equating f_P and f_Z for a discretized implementation, the following equation can be used to calculate KI.

$$KI = KP * R_{MOTOR} / (F_{PWM} * L_{MOTOR}) \quad (11)$$

As an example, consider the following use case -

- VM = 24 V
- I_{FS} = 5 A
- R_{MOTOR} = 0.3 Ω
- L_{MOTOR} = 0.7 mH
- UGB = 200 Hz
- F_{PWM} = 25 kHz
- Above 50 RPM, the decay mode should change from silent step to smart tune ripple control.

Using the previous equations, KP = 0.18326 and KI = 0.00314. The following register values can be set -

- SS_KP = 0101111b = 47
- SS_KI = 0000001b = 1
- SS_KP_DIV_SEL = 011b = 1/256
- SS_KI_DIV_SEL = 011b = 1/256
- 50 RPM corresponds to roughly 42.6 kpps at 1/256 microstepping, so SS_THR = 00010101b = 21

Figure 7-20 shows the smooth sinusoidal coil current waveforms when the motor operates in silent step decay mode.

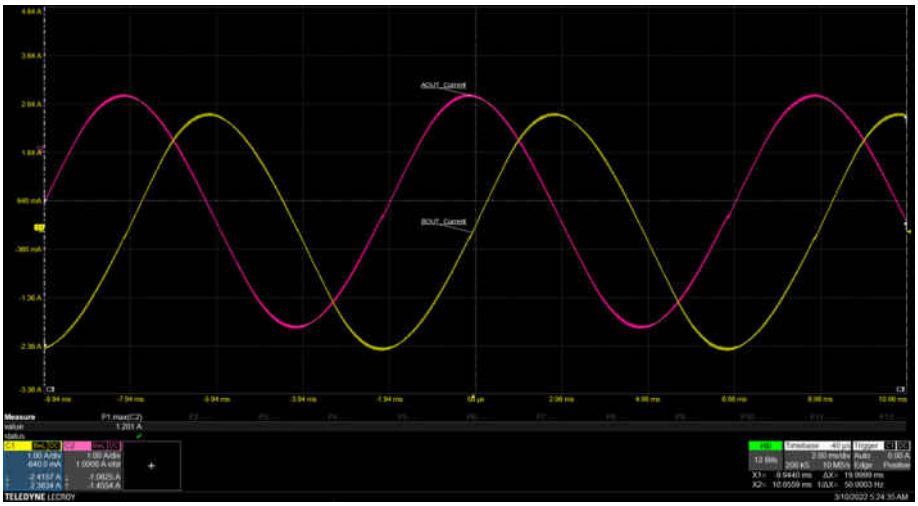

Figure 7-20. Coil Current Waveform with Silent Step Decay

Note

For pre-production samples, writing 1b to EN_SS latches the part to operate with silent step decay mode, and transition between silent step and other decay modes happen when motor speed exceeds or drops below the SS_THR threshold. If EN_SS bit is toggled, a nSLEEP cycling is required.

For production samples, EN_SS can be toggled to enable or disable silent step decay mode.

7.4.13 Auto-torque Dynamic Current Adjustment

For a typical stepper motor driver, the full-scale current is designed based on the peak load torque demand and ensures that the motor does not lose steps any time peak load is demanded. The current therefore is always constant irrespective of the load torque. As a result, when the load torque is lower than peak load, the driver and the motor dissipate some of the input power as resistive power loss, as represented in Figure 7-21.

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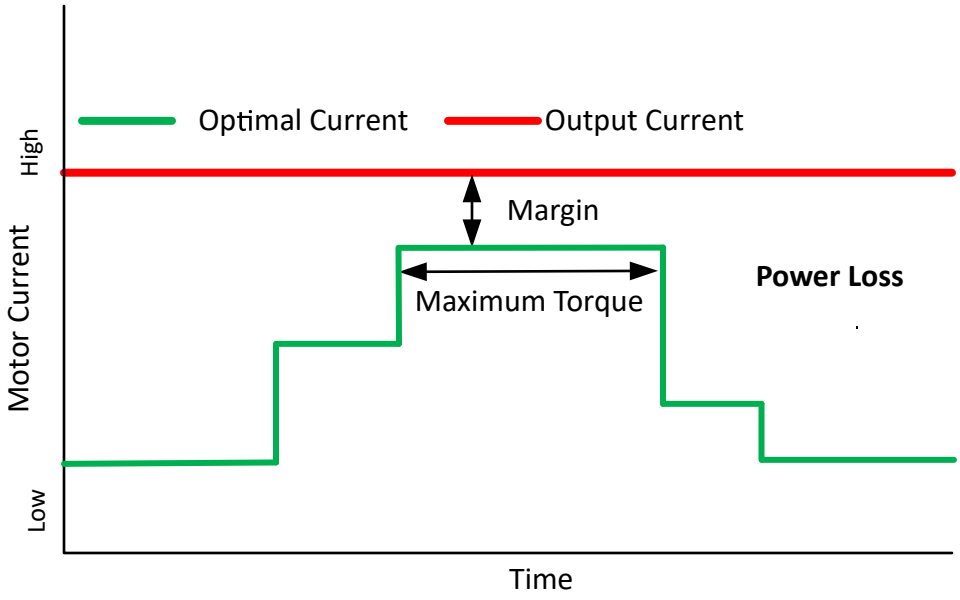

Figure 7-21. Power Loss with Conventional Stepper Driver

In most systems, the demand for peak load torque occurs only rarely. For example, in an ATM machine, the stepper motors might be needed to deliver peak load for less than 15% of their overall run time. A typical stepper driver though ends up delivering full-scale current to the motors all the time - leading to lower system efficiency due to the unwanted power loss, larger system size and shorter lifetime of components.

The auto-torque algorithm implemented in the DRV8462 improves system efficiency by dynamically changing the output current according to the load torque. Whenever the load torque is low, the output current is lower to reduce resistive losses; and when the load torque goes up, the output current increases immediately to prevent motor step loss. This concept is shown in Figure 7-22. As a result of improved efficiency due to auto-torque, the system runs at a lower temperature, which extends the lifetime of the components. Auto-torque can also enable the use of cheaper and smaller sized stepper motors.

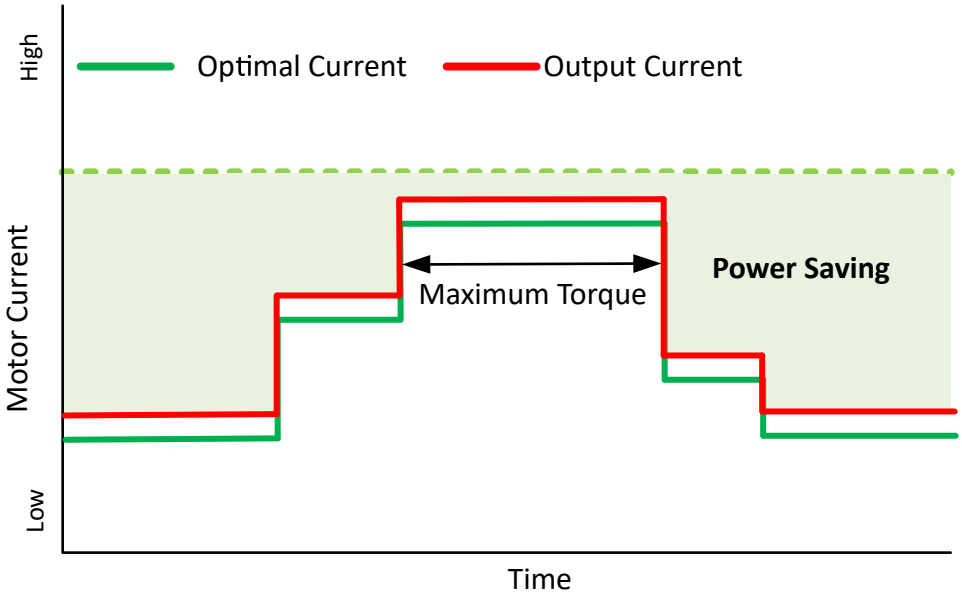

Figure 7-22. Power Saving with Auto-torque

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The auto-torque feature is enabled by writing '1' to the ATQ_EN bit. To dynamically adapt the full-scale current, the auto-torque algorithm generates the ATQ_CNT parameter, which varies linearly with load torque. Figure 7-23 shows the block diagram of the closed-loop auto-torque algorithm -

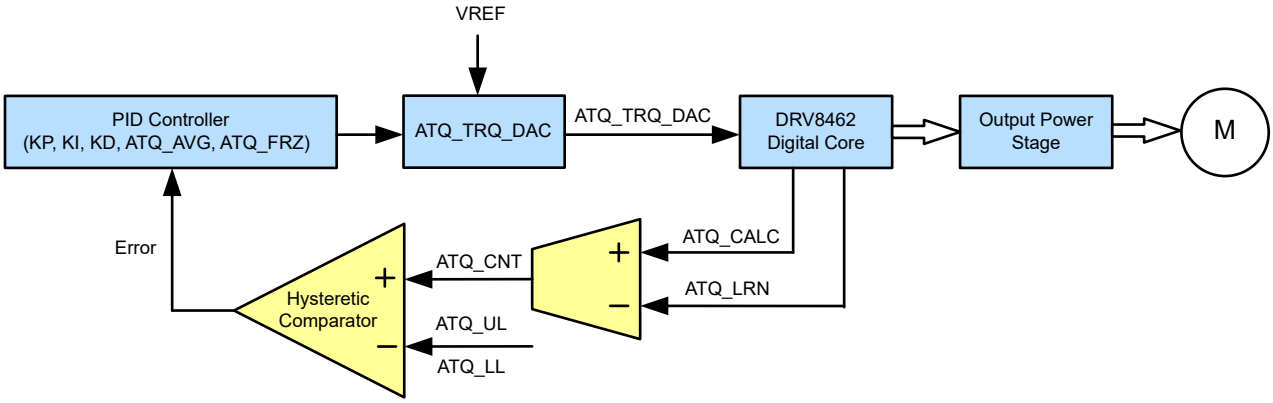

Figure 7-23. Auto-torque Block Diagram

Note

When auto-torque is enabled, program ISTSL between ATQ_TRQ_MAX and ATQ_TRQ_MIN.

7.4.13.1 Auto-torque Learning Routine

For auto-torque algorithm to work, it is mandatory to estimate the ATQ_LRN parameter using the auto-torque learning routine. The ATQ_LRN parameter depends on the operating conditions and motor parameters, therefore re-learning is required everytime motor is changed or operating conditions are significantly changed.

Table 7-21. Description of auto-torque learning parameters

Parameter	Description
ATQ_LRN	ATQ_LRN is the output of the auto-torque learning routine. It represents losses in the system at minimum load - such as I^2R losses in the motor and the driver and friction in the motor. ATQ_LRN is proportional to the full-scale current setting of the driver. ATQ_LRN is represented by two parameters - ATQ_LRN_CONST1 and ATQ_LRN_CONST2.
ATQ_LRN_MIN_CURRENT	Represents the initial current level for auto torque learning routine. Initial current level = ATQ_LRN_MIN_CURRENT * 8
ATQ_LRN_STEP	Represents the increase to initial current level for the learning routine. Final current level = ATQ_LRN_MIN_CURRENT + ATQ_LRN_STEP • 00b : ATQ_LRN_STEP = 128 • 01b : ATQ_LRN_STEP = 16 • 10b : ATQ_LRN_STEP = 32 • 11b : ATQ_LRN_STEP = 64 Example : If ATQ_LRN_STEP = 10b and ATQ_LRN_MIN_CURRENT = 11000b, then Initial learn current level = 24*8 = 192 Final learn current level = 192 + 32 = 224
ATQ_LRN_CYCLE_SELECT	Number of sine half cycles in one current level after which the learning routine lets the current jump to the next level. • 00b : 8 half-cycles • 01b : 16 half-cycles • 10b : 24 half-cycles • 11b : 32 half-cycles

Table 7-21. Description of auto-torque learning parameters (continued)

LRN_START	Writing '1' to this bit enables the auto torque learning process. After learning is completed, this bit automatically goes to '0'.
LRN_DONE	This bit becomes '1' after learning is complete.
ATQ_LRN_CONST1	Indicates the ATQ_LRN parameter at the initial learning current level.
ATQ_LRN_CONST2	Indicates the ATQ_LRN parameter at the final learning current level.

Note

ATQ_LRN_MIN_CURRENT and ATQ_LRN_STEP should be chosen such that the final current level does not exceed 255.

The ATQ_LRN parameter has a linear relation with full-scale current. So, the learning routine needs to run at two different currents to deduce the values of the necessary parameters, as is shown in Figure 7-24. Once learning is enabled, the algorithm changes ATQ_TRQ_DAC automatically for few electrical cycles to extract the learning parameters. The learning finishes in less than 100 ms.

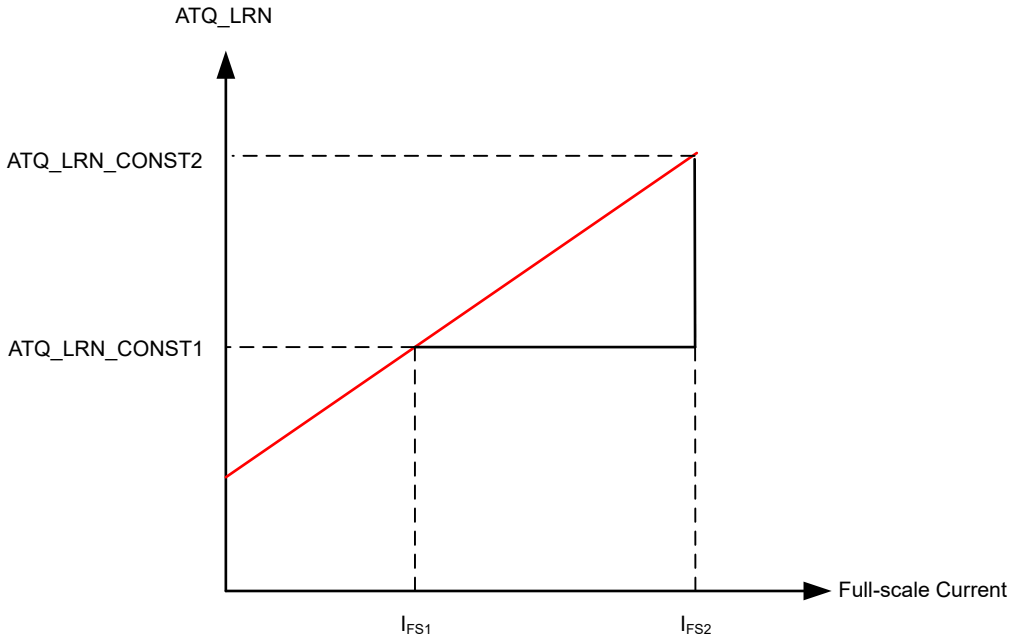

Figure 7-24. ATQ_LRN at two currents

To enable automatic learning, following sequence of commands should be applied:

- Write 1b to ATQ_EN
- Run the motor with minimum load
- Program ATQ_LRN_MIN_CURRENT.
- Program ATQ_LRN_STEP.
- Program ATQ_LRN_CYCLE_SELECT.
- Write 1b to ATQ_LRN_START
- The algorithm runs the motor with minimum current level for ATQ_LRN_CYCLE_SELECT number of half cycles
- Next, the algorithm runs the motor with final current level for ATQ_LRN_CYCLE_SELECT number of half cycles
- After learning is complete,
  - ATQ_LRN_START bit is auto cleared

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  - ATQ_LRN_DONE bit goes high
- ATQ_LRN_CONST1 and ATQ_LRN_CONST2 are populated in their respective registers

Once the ATQ_LRN_CONST1 and ATQ_LRN_CONST2 are known from the prototyping phase, they can be used in the mass production phase without invoking the learning routine. The following sequence of commands should be applied:

- Program ATQ_LRN_MIN_CURRENT
- Program ATQ_LRN_STEP
- Program ATQ_LRN_CONST1
- Program ATQ_LRN_CONST2
- Enable ATQ

Figure 7-25 shows the consolidated flowchart of the auto-torque laerning routine.

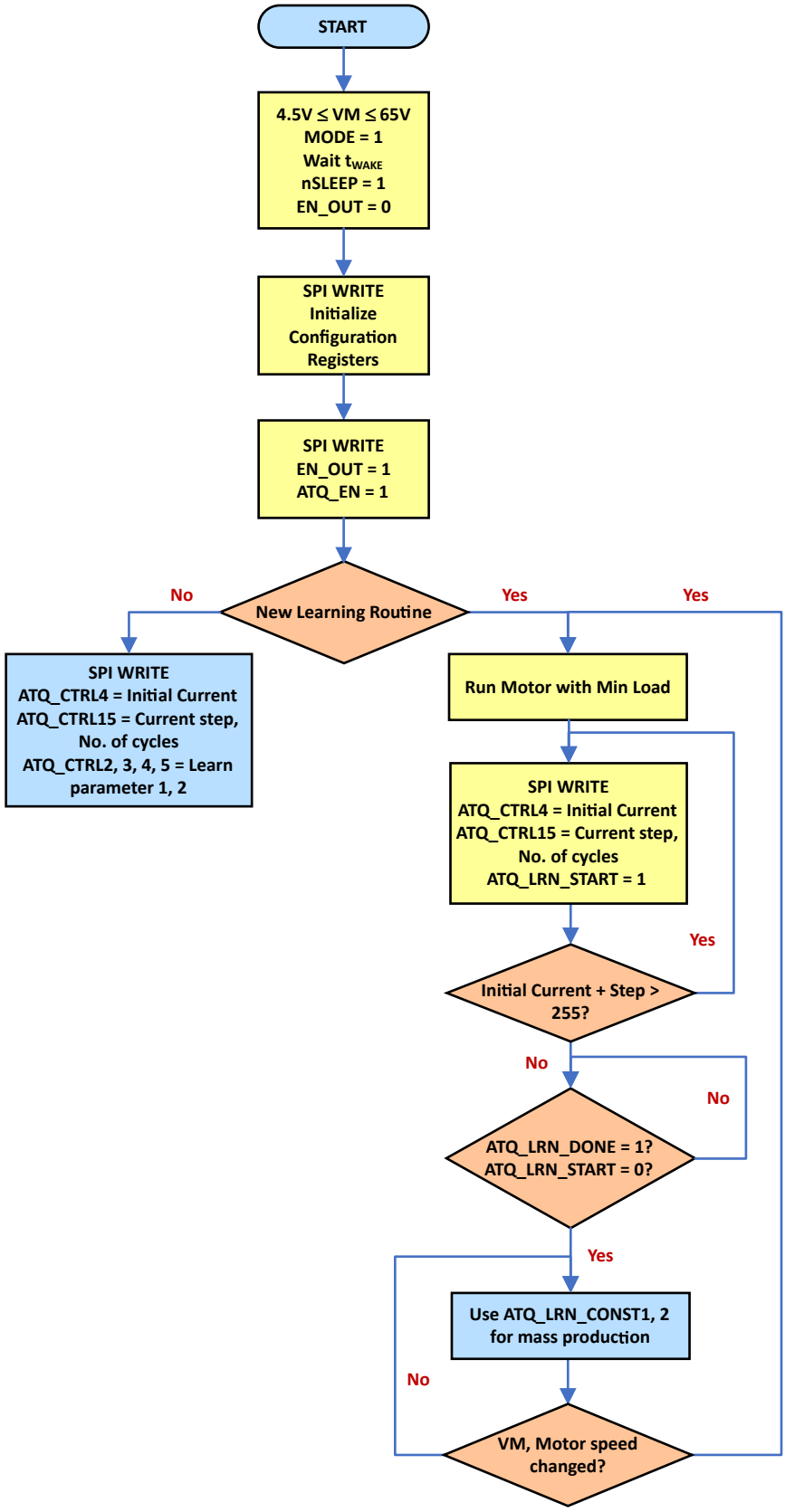

Figure 7-25. Auto-torque Learning Flowchart

The scopeshot below shows an automatic learning process with 740 mA initial current (I_{FS1}) and 2.2 A final current (I_{FS2}). The ATQ_LEARN_CYCLE_SELECT corresponds to 32 half-cycles.

Traces from top to bottom: Load torque, coil current, supply current, nSCS

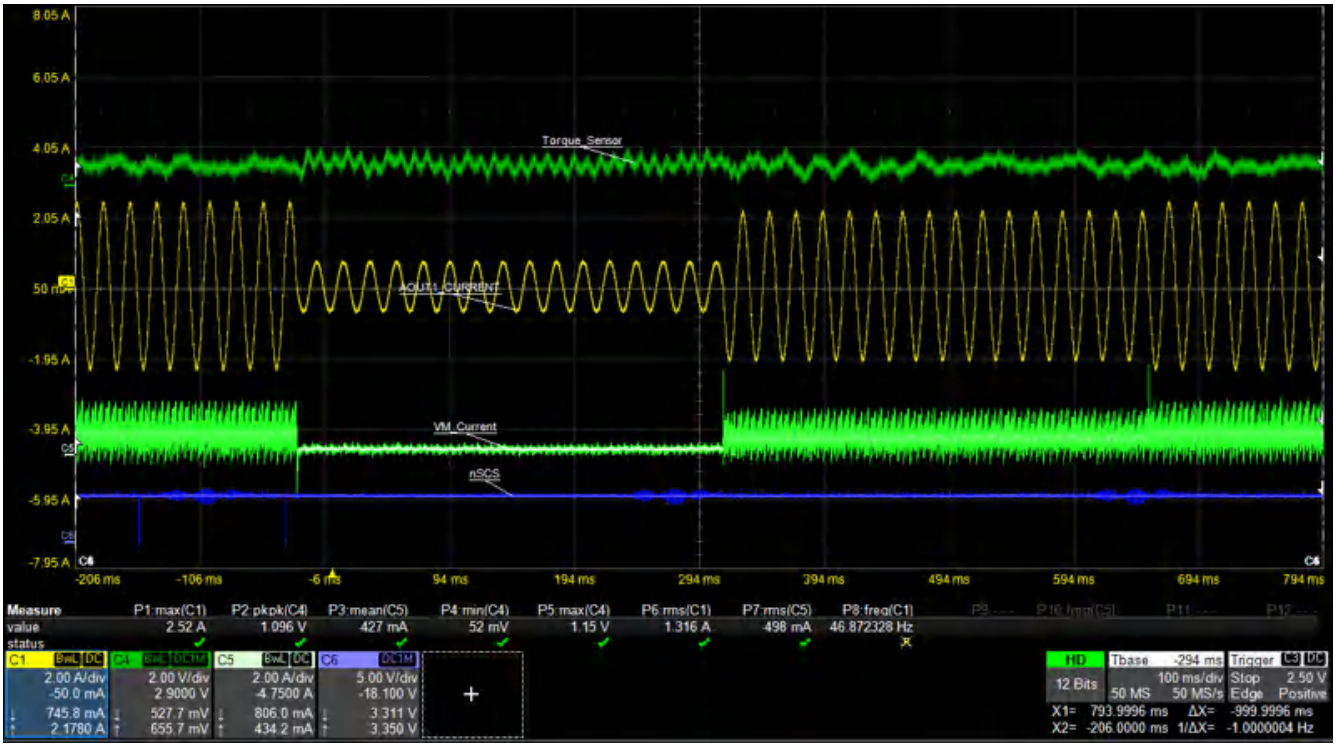

Figure 7-26. Automatic learning

Note

The production samples will feature a VM_SCALE bit located in ATQ_CTRL17 bit 6. When enabled, this bit will automatically modify the auto-torque learning routine parameters in the event of a supply voltage change. In pre-production samples, this bit will be reserved.

7.4.13.2 ATQ_CNT and PID Control Loop

Figure 7-27 shows the ATQ_CALC parameter shown in the auto-torque block diagram.

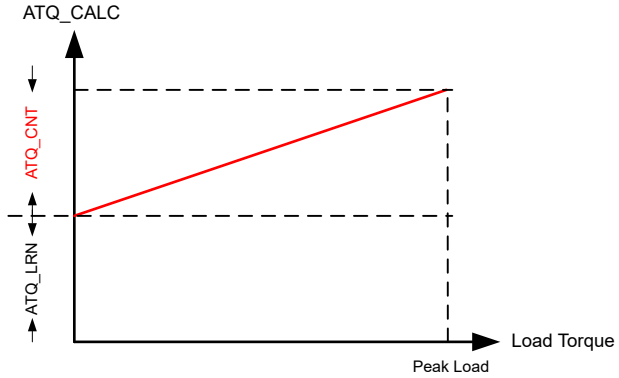

Figure 7-27. ATQ_CALC

Therefore, ATQ_CALC = ATQ_LRN + ATQ_CNT. As mentioned before, the ATQ_CNT parameter is proportional to load torque and inversely proportional to the full-scale current setting of the stepper driver. This relation is represented by Figure 7-28-

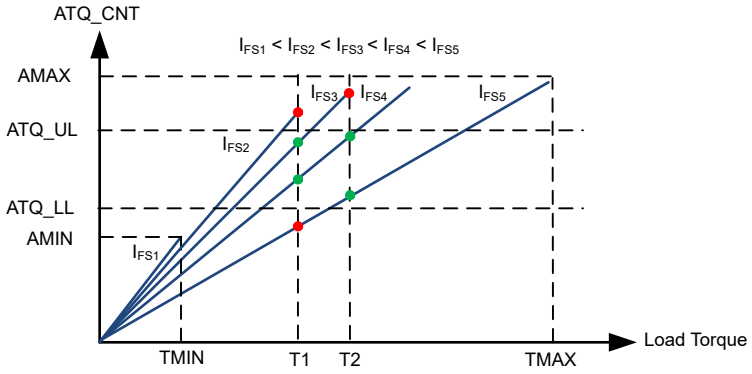

Figure 7-28. ATQ_CNT change with load torque and full-scale current

A high value of ATQ_CNT corresponding to a lower full-scale current is preferable, because that minimizes the unwanted resistive losses in the system and improves efficiency.

The PID controller smoothens the response to load transients while minimizing the error. The PID algorithm is expressed as -

$$u(t) = KP * e(t) + KI * \int e(t)dt + KD * de(t)/dt \quad (12)$$

where,

KP, KI and KD = PID loop constants

u(t) = output of controller

e(t) = error signal

- In general, increasing the KP will increase the speed of the control system response. However, if KP is too large, the current waveform will begin to oscillate. If KP is increased further, the oscillations will become larger and the system will become unstable and may even oscillate out of control.
- The KI term sums the error over time, so the effect is to drive the steady-state error to zero.
- Increasing the KD parameter will cause the control system to react more strongly to changes in the error term and will increase the speed of the overall control system response. Most practical control systems use very small KD, because the derivative response is highly sensitive to noise.

Table 7-22 describes the major parameters associated with the PID control loop -

Table 7-22. Parameters for auto-torque PID control loop

ATQ_CALC	ATQ_CALC is an output of the auto-torque algorithm. It has two components - a no-load loss component (ATQ_LRN) and another component (ATQ_CNT) proportional to load torque. ATQ_CALC = ATQ_LRN + ATQ_CNT A simplistic plot of the ATQ_CALC prameter is shown in Figure 7-27.
ATQ_CNT	The component of auto-torque algorithm output that changes proportional to load torque. The ATQ_CNT parameter is also inversely proportional to the full-scale current setting of the stepper driver. ATQ_CNT ∝ Load torque; and ATQ_CNT ∝ 1 / Full-scale Current ATQ_CNT has a length of 12 bits.
ATQ_UL	Upper and lower boundaries of the hysteretic loop within which ATQ_CNT is controlled by modifying the ATQ_TRQ_DAC parameter. The CNT_OFLW flag indicates ATQ_CNT is more than ATQ_UL, and the CNT_UFLW indicates ATQ_CNT is less than ATQ_LL.
ATQ_LL	
KP	Proportional, integral and differential gain parameters for the PID control loop. KP has a length of 8 bits. KI and KD each have a length of 4 bits.
KI	
KD	

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Table 7-22. Parameters for auto-torque PID control loop (continued)

ATQ_AVG	The ATQ_CNT parameter is a moving average of ATQ_AVG number of half-cycles. Therefore, a high value for ATQ_AVG slows down the loop response time to a sudden peak load demand, but ensures smooth jerk-free transition to higher torque output. A low value causes the loop to respond immediately to a sudden load demand. 2 - 2 cycle average 4 - 4 cycle average 7 - 8 cycle average Other values : no averaging
ATQ_FRZ	Delay in electrical half-cycles after which current is changed in response to the PID loop. A small value increases the current quickly to meet peak load demand. This parameter has a range of 1 to 7. 1 - Fastest response time, but the loop can become unstable 7 - Slowest response, but the loop will be stable
ATQ_TRQ_DAC	Read-only. Auto-torque current level readout. Represents the full-scale current setting of the stepper driver when auto-torque is enabled. ATQ_TRQ_DAC can vary between user programmable ATQ_TRQ_MIN (minimum regulation current) and ATQ_TRQ_MAX (maximum regulation current) levels.
ATQ_D_THR	If error change is less then ATQ_D_THR, then KD does not contribute to correction. KD contributes only when error change is greater than ATQ_D_THR. For example: if ATQ_D_THR = 10, • If error change is 9, u(t) = KP * *e(t)* + KI * ∫*e(t)dt* • If error change is 12, then u(t) = KP * *e(t)* + KI * ∫*e(t)dt* + KD * d*e(t)*/dt
ATQ_MAX_INTEGRAL	Indicates the saturation point of error integration. For example: if ATQ_MAX_INTEGRAL=10, error integration stops at 10 *u(t)* = KP * *e(t)* + KI * 10 + KD * d*e(t)*/dt
ATQ_ERROR_TRUNCATE	Number of LSB bits truncated from error before used in PID loop equations. This option helps removing noise in current.

The auto-torque algorithm maintains the ATQ_CNT value within the hysteretic band defined by ATQ_UL and ATQ_LL, by modulating the full-scale current.

- If load demand suddenly increases, the ATQ_CNT goes above the ATQ_UL threshold, and the algorithm brings the ATQ_CNT within the band by increasing the full-scale current.
- When load demand drops and ATQ_CNT goes below ATQ_LL, the algorithm reduces the full-scale current to bring the ATQ_CNT within the hysteretic band.
- If the hysteretic band between ATQ_UL and ATQ_LL is moved up, efficiency and thermal performance improves due to lower full-scale current. But in the event of a sudden peak load, it takes longer to increase the current to its maximum value, leading to chances of step loss.
- If the hysteretic band between ATQ_UL and ATQ_LL is moved down, efficiency improvement is only moderate due to the higher value of full-scale current, but step loss is no longer a concern.
- If the gap between ATQ_UL and ATQ_LL is increased, it improves the immunity of the loop against system noise.

Guidelines to tune the PID loop parameters are as follows -

- Observe the ATQ_CNT during no load and desired current level
- Write ATQ_UL and ATQ_LL such that ATQ_CNT is within those limits
- The ATQ_UL should be chosen depending on the max pull-out torque of the motor, with some safety margin accounted for
- Set KI and KD to zero first
- Program a minimum KP value
- Enable auto-torque and observe the current waveform at different loads
- Increase KP to obtain the desired response time to load transients
- Increase KI and ATQ_ERROR_TRUNCATE to stop any oscillation in the current waveform

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The flowchart for selecting ATQ_UL, ATQ_LL, ATQ_TRQ_MAX and ATQ_TRQ_MIN parameters is shown below.

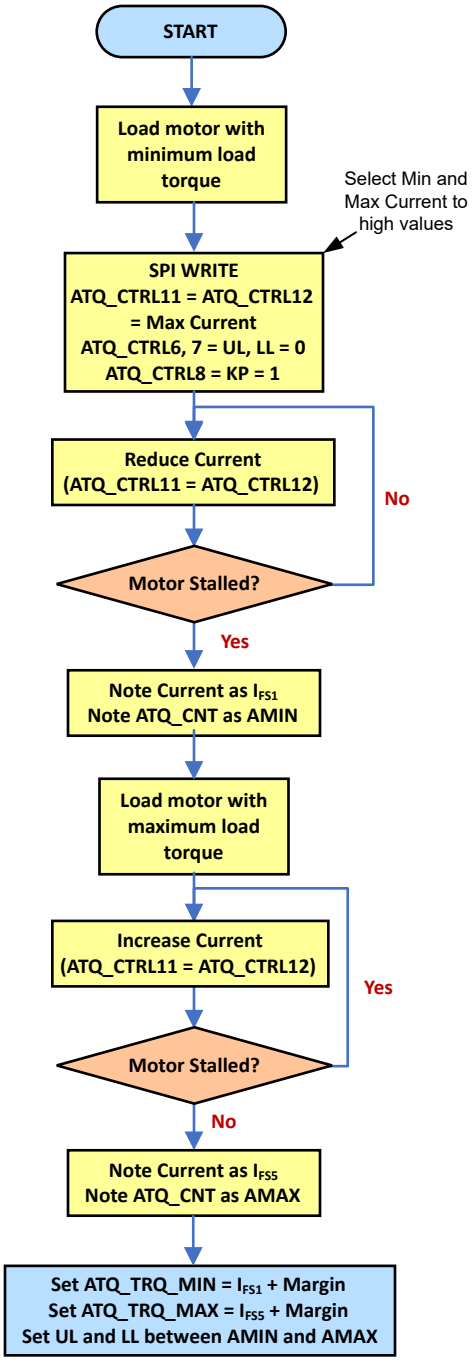

Figure 7-29. Selecting ATQ_UL, ATQ_LL, ATQ_TRQ_MIN, ATQ_TRQ_MAX

The following flowchart is for selecting KP, KI and KD parameters for tuning the auto-torque PID loop.

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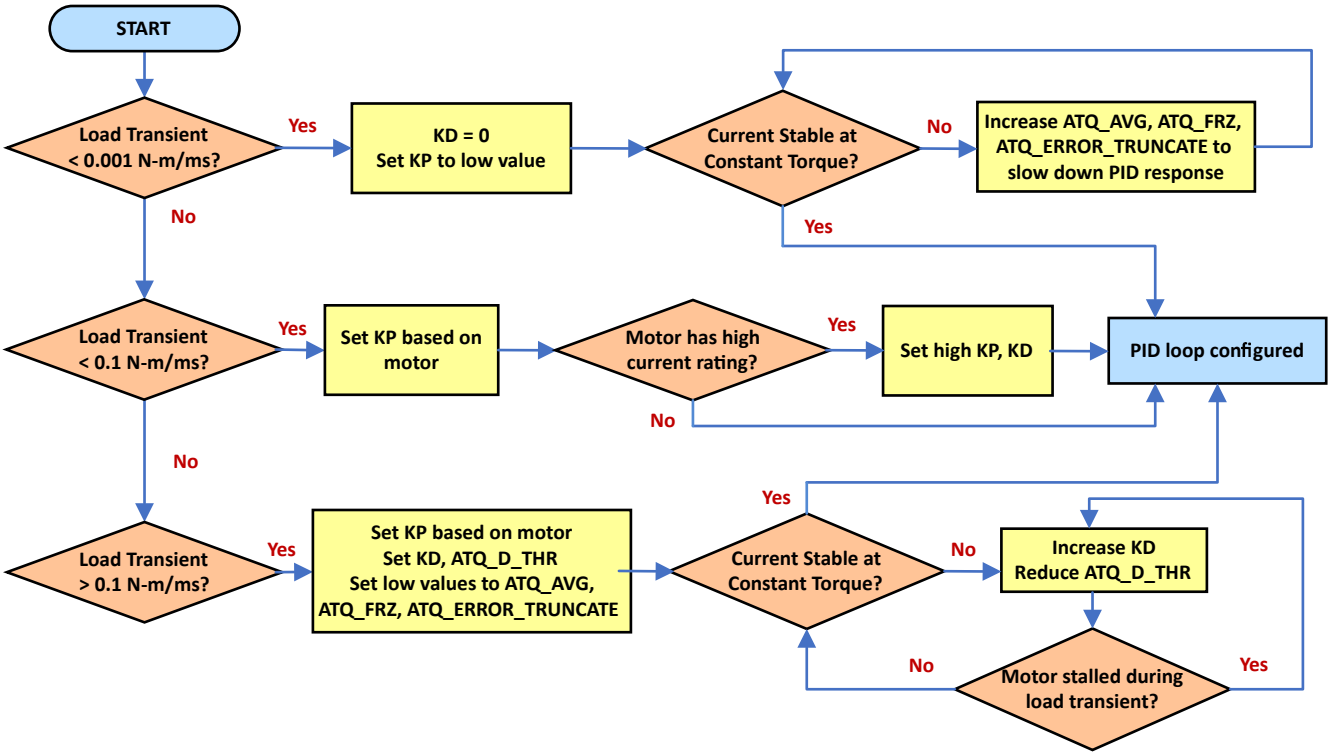


Figure 7-30. Selecting KP, KI, KD

The figure below shows the coil current waveform when load torque changes over 300 ms.

KP = 1, KD = 5, ATQ_D_THR = 20, ATQ_ERROR_TRUNCATE = 2, current waveform in yellow trace.

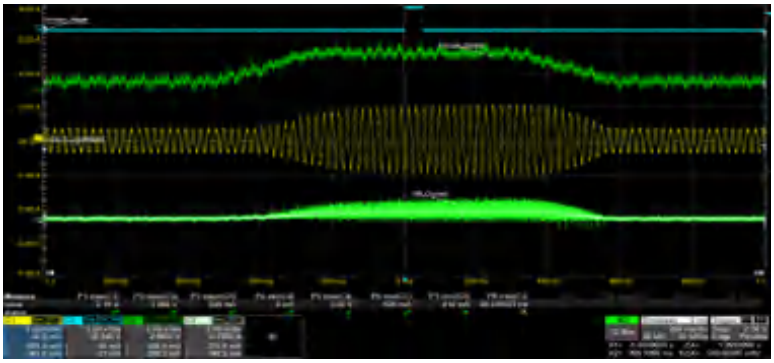


Figure 7-31. Current waveform with 300 ms Load Transient

The following figure shows the coil current waveform when load torque changes over 40 ms.

KP = 1, KD = 5, ATQ_D_THR = 20, ATQ_ERROR_TRUNCATE = 2, current waveform in yellow trace.

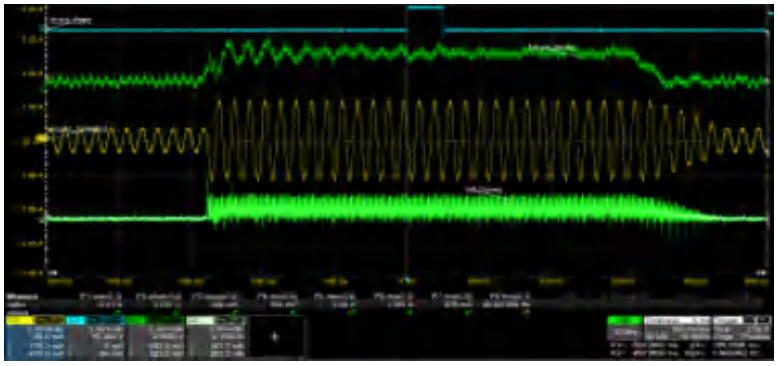


Figure 7-32. Current waveform with 40 ms Load Transient

7.4.13.3 Troubleshooting Tips

Observation : Current waveform is noisy

- Increase ATQ_ERROR_TRUNCATE
- Choose a wider band.i.e increase ATQ_UL,Reduce ATQ_LL
- Increase ATQ_FRZ (upto 7)
- Make ATQ_AVG = 4 or 8
- Reduce KP
- If KD is non-zero, use a higher ATQ_D_THR

Observation : Current response is slow

- Reduce ATQ_UL
- Increase KP
- Increase KD
- Reduce ATQ_D_THR
- Set ATQ_FRZ = 1
- Set ATQ_AVG = 0 (Averaging disabled)

Observation : Full-scale current in no load is relatively high

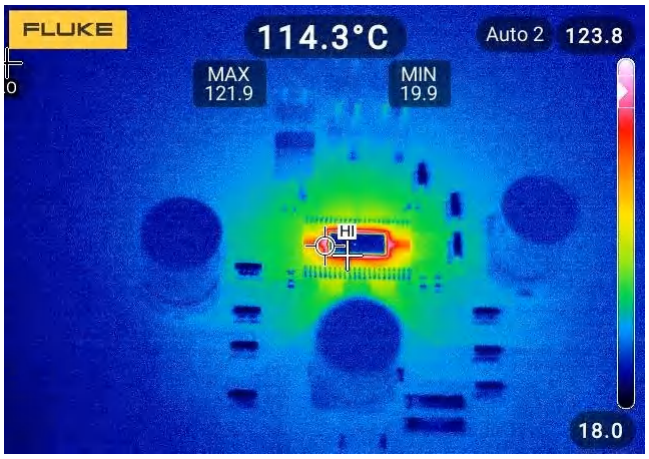
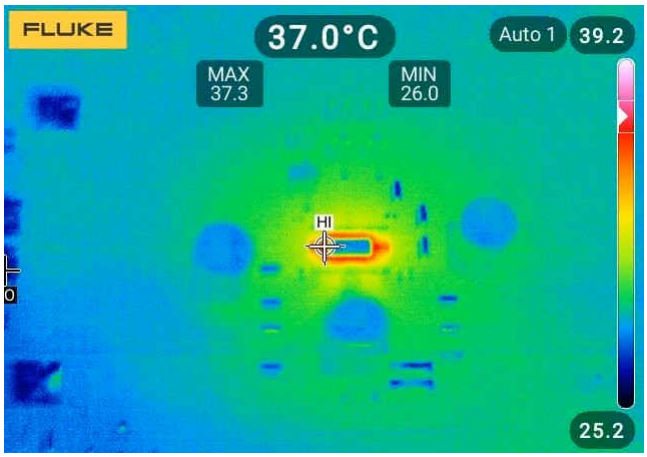
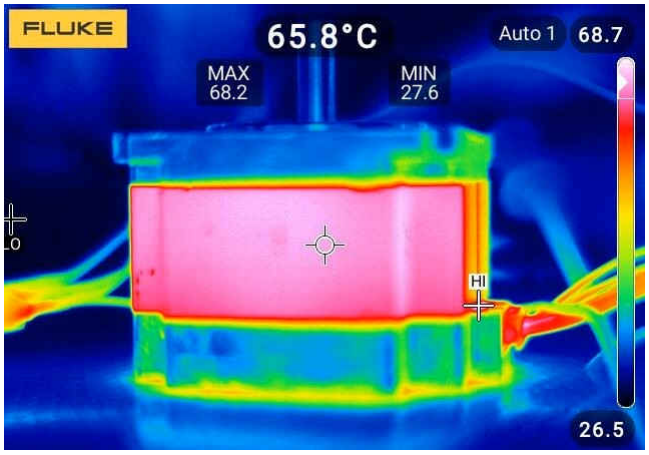
- Increase ATQ_LL
- Check CNT_UFLW status. If it is high and full-scale current in no load is still high, reduce ATQ_TRQ_MIN.

7.4.13.4 Efficiency Improvement with Auto-torque

The following images show the thermal performance improvements as a result of auto-torque. The thermal images are captured at the following condition:

VM = 24 V, 1/16 microstep, 4A full-scale current, 3000 pps speed, No load, Room temperature ambient, Power on time = 10 minutes

Table 7-23. Thermal performance improvement with Auto-torque

	
DRV8462 Thermal Image: Auto-torque disabled	DRV8462 Thermal Image: Auto-torque enabled
	
Motor Thermal Image: Auto-torque disabled	Motor Thermal Image: Auto-torque enabled

7.4.14 Standstill Power Saving Mode

When the controller is not sending any step pulses and the motor is holding the same position, the DRV8462 can be configured to operate in the standstill power saving mode. When this mode is enabled by writing '1' to the EN_STSL bit, the power dissipation of the system can be reduced by lowering the coil current from run current to holding current.

After the last STEP pulse, the device waits for an amount of time programmed by the TSTSL_DLY register, after which the coil currents are ramped down from run current to holding current over a time period programmed by the TSTSL_FALL register. The STSL flag goes up to indicate that the device is in standstill power saving mode. Once the next STEP pulse is detected, the coil current immediately ramps up to run current.

The run current is programmed by the TRQ_DAC register and the holding current is programmed by the ISTSL register, as shown in Section 7.4.8.

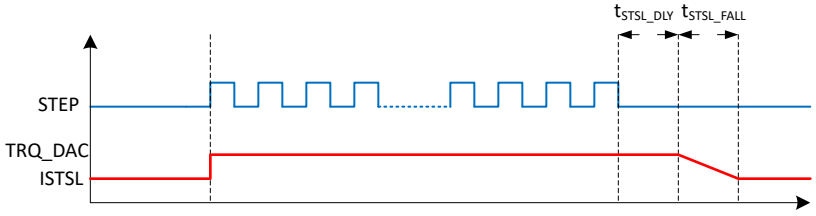


Figure 7-33. Standstill Power Saving Mode

Note

- TSTSL_FALL in production samples will be 1/16 th of their value in the pre-production samples. For example, TSTSL_FALL = 0001b will mean fall time for each current step will be 1 ms.
- If ISTSL has to be changed while the device is in standstill power saving mode, first cycle the EN_STSL bit from 1b to 0b and back to 1b.

7.4.15 Charge Pump

A charge pump is integrated to supply the high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

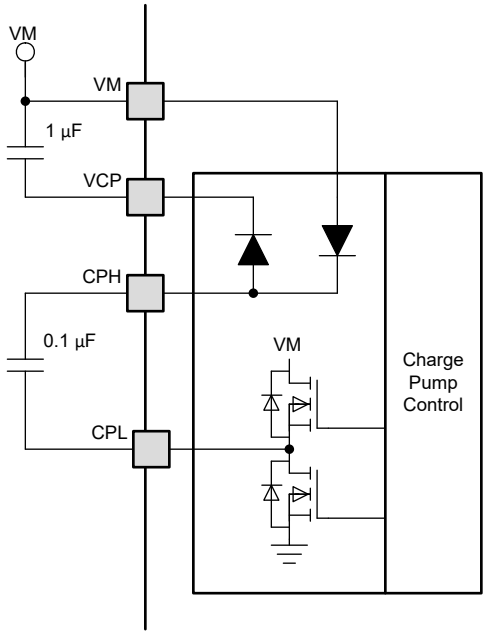


Figure 7-34. Charge Pump Block Diagram

7.4.16 Linear Voltage Regulator

A linear voltage regulator is integrated in the device. When the VCC pin is connected to DVDD, the DVDD regulator provides power to the low-side gate driver and all the internal circuits. For proper operation, bypass the DVDD pin to GND using a 1 µF ceramic capacitor. The DVDD output is nominally 5-V.

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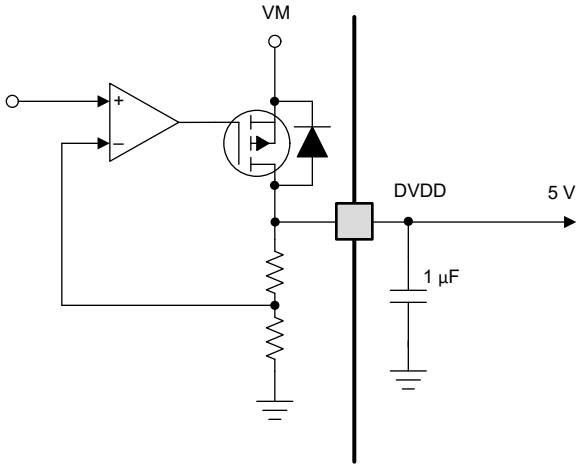

Figure 7-35. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high, tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

7.4.17 VCC Voltage Supply

An external voltage can be applied to the VCC pin to power the internal logic circuitry. The voltage on the VCC pin should be between 3.05V and 5.5V and should be well regulated. When an external supply is not available, VCC must be connected to the DVDD pin of the device.

When powered by the VCC, the internal logic blocks do not consume power from the VM supply rail - thereby reducing the power loss in the DRV8462. This is highly beneficial in high voltage applications, and when thermal conditions are critical. Bypass the VCC pin to ground using a 0.1 µF ceramic capacitor.

7.4.18 Logic Level, Tri-Level and Quad-Level Pin Diagrams

Figure 7-36 shows the input structure for M0, DECAY0, DECAY1 and ENABLE pins.

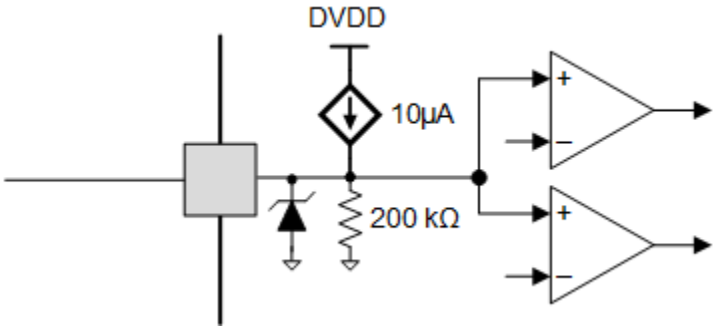

Figure 7-36. Tri-Level Input Pin Diagram

Figure 7-37 shows the input structure for M1 and TOFF pins.

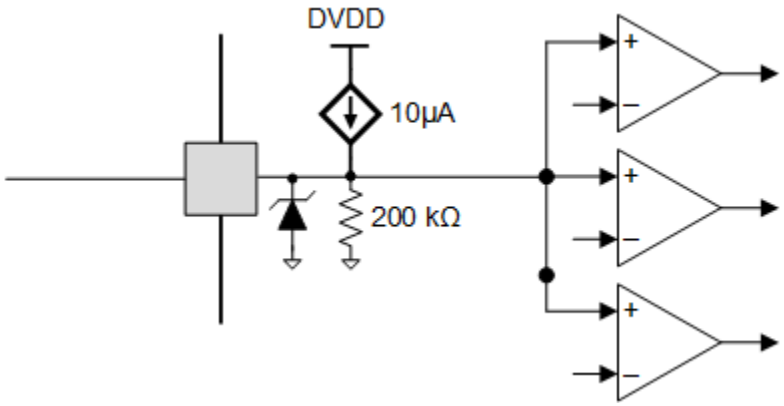

Figure 7-37. Quad-Level Input Pin Diagram

Figure 7-38 shows the input structure for STEP, DIR, MODE, SDI, SCLK and nSLEEP pins.

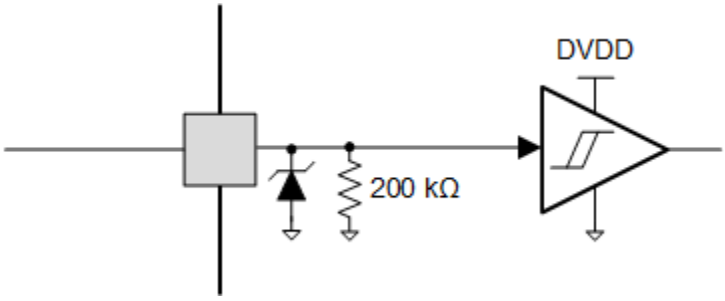

Figure 7-38. Logic-Level Input Pin Diagram

The diagram below shows the input structure for the logic-level pin nSCS.

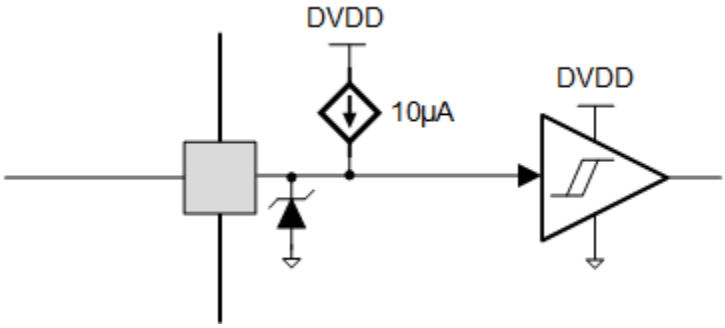

Figure 7-39. nSCS Input Pin Diagram

7.4.19 Spread spectrum

Spread spectrum or frequency dithering is used to reduce the effect of EMI by converting a narrowband signal into a wideband signal, which will spread the energy across multiple frequencies. Figure 7-40 illustrates how manipulating the clock frequency over time has the effect of spreading the energy.

In the context of the DRV8462, the frequencies of the internal clock for digital circuits (10 MHz typical) and the clock for charge pump (357 kHz typical) are manipulated to reduce the peak energy and is distributed to other frequencies and their harmonics. This feature combined with output slew rate control minimizes the radiated emissions from the device and helps pass strict EMI standards.

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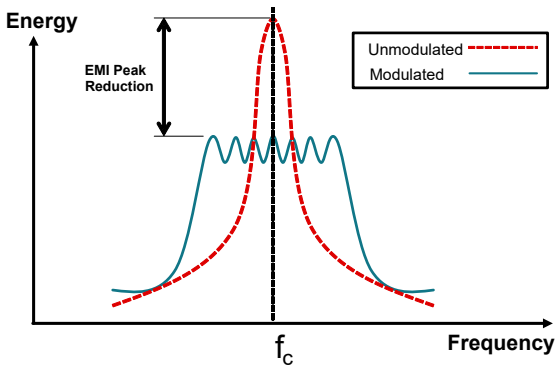

Figure 7-40. EMI Reduction by Spread Spectrum, Frequency Modulation

When the DRV8462 is configured with the SPI interface, spread spectrum can be enabled or disabled by the DIS_SSC bit. By default, spread spectrum is disabled after power-up. Writing '0' to the DIS_SSC bit enables spread spectrum. If the device is operating with silent step decay mode, spread spectrum is disabled. Additionally, when the DRV8462 is configured with the GPIO interface, spread spectrum is permanently disabled.

There are many ways to implement spread spectrum. The DRV8462 uses the triangular analog modulation profile. Figure 7-41 and Figure 7-42 show the spread spectrum profiles of the internal digital clock and the charge pump clock around their respective centre frequencies. The digital clock varies by equal amounts over 14 steps between 9 MHz and 11 MHz.

Note that the centre frequencies themselves will vary with process and temperature changes as shown in the electrical characteristics table, and the variations due to spread spectrum will be in addition to those.

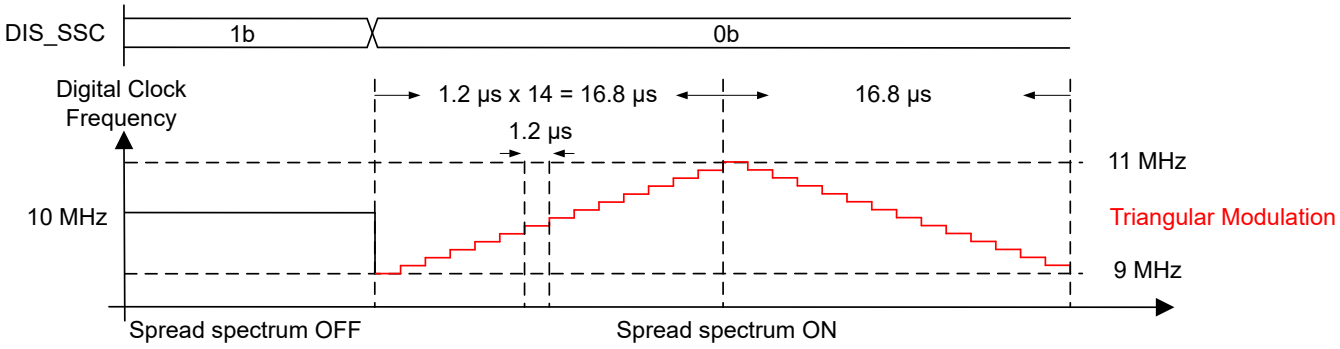

Figure 7-41. Triangular Spread Spectrum of Internal Digital Clock

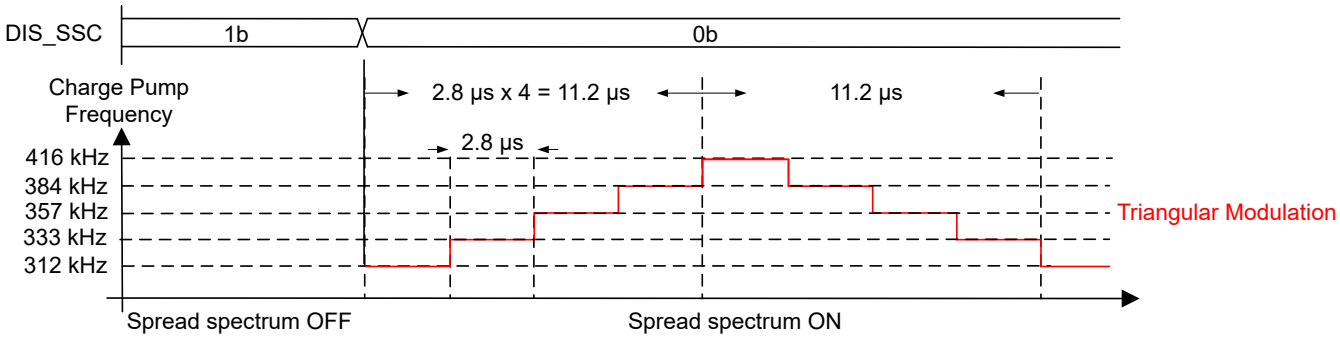

Figure 7-42. Triangular Spread Spectrum of Charge Pump Clock

7.4.20 Protection Circuits

The device is fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, open load, and device overtemperature events. In addition, when operating with SPI interface, the device is protected against stall detection in the event of overload or end-of-line movement.

7.4.20.1 VM Undervoltage Lockout

If at any time the voltage on the VM pin falls below the UVLO falling threshold voltage:

- All the outputs are disabled (High-Z)
- The charge pump is disabled
- nFAULT is driven low

Normal operation resumes (motor driver and charge pump) when the VM voltage recovers above the UVLO rising threshold voltage.

When operating with SPI interface, if the voltage on the VM pin falls below the UVLO falling threshold voltage, but is above the V_{RST} or VCC UVLO (shown in Figure 7-43) :

- SPI communication is available and the digital core of the device is active
- The FAULT and UVLO bits are made high
- The nFAULT pin is driven low

From this condition, if the VM voltage recovers above the UVLO rising threshold voltage:

- nFAULT pin is released (is pulled-up to the external voltage)
- The FAULT bit is reset
- The UVLO bit remains latched high until cleared through the CLR_FLT bit or an nSLEEP reset pulse.

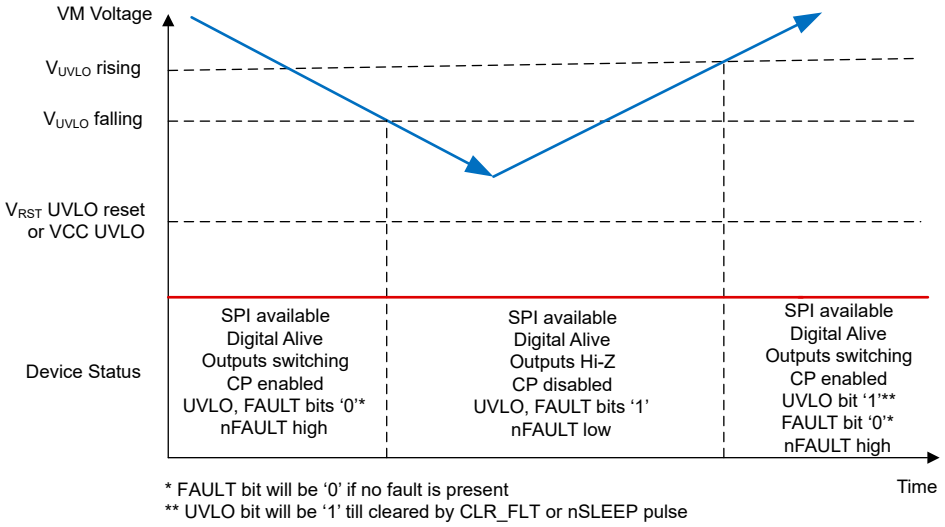

Figure 7-43. Supply Voltage Ramp Profile

When the voltage on the VM pin falls below the V_{RST} or VCC UVLO (shown in Figure 7-44) :

- SPI communication is unavailable and the digital core is shutdown
- The FAULT and UVLO bits are low
- The nFAULT pin is high

During a subsequent power-up, when the VM voltage exceeds the V_{RST} voltage:

- The digital core comes alive
- UVLO bit stays low
- The FAULT bit is made high
- The nFAULT pin is pulled low
- When the VM voltage exceeds the VM UVLO rising threshold

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– FAULT bit is reset
– UVLO bit stays low
– nFAULT pin is pulled high.

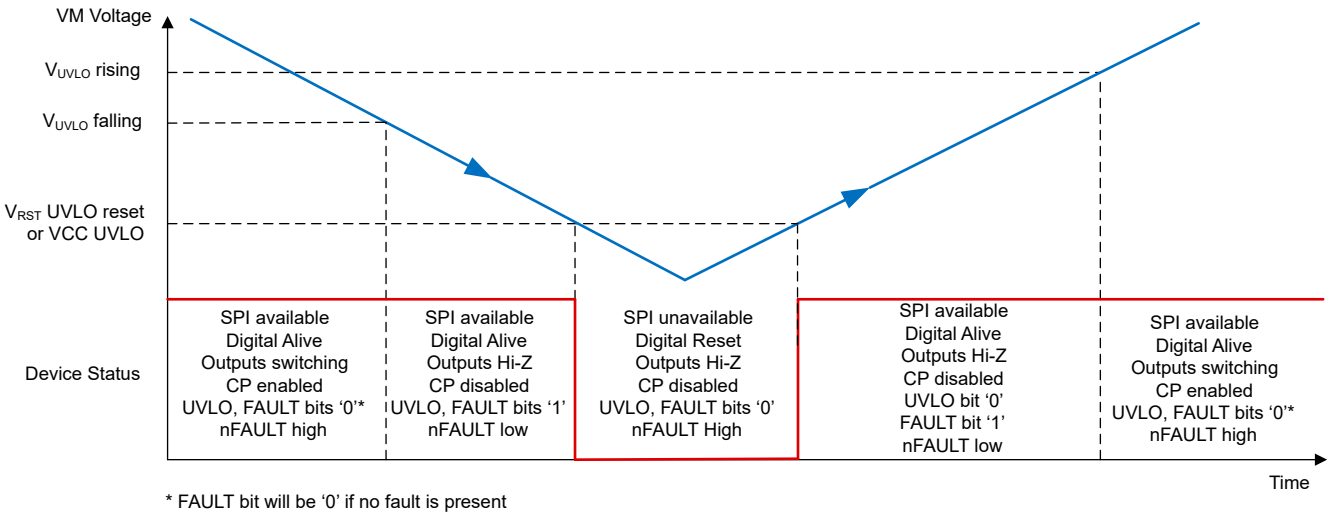

Figure 7-44. Supply Voltage Ramp Profile

7.4.20.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage:

- All the outputs are disabled (High-Z)
- nFAULT pin is driven low
- The charge pump remains active
- For the SPI version, the FAULT and CPUV bits are made high.

Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed. The CPUV bit remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse.

7.4.20.3 Logic Supply Power on Reset (POR)

If at any time the voltage on the VCC pin falls below the VCC_{UVLO} threshold:

- All the outputs are disabled (High-Z)
- Charge pump is disabled.

VCC UVLO is not reported on the nFAULT pin. Normal motor-driver operation resumes when the VCC undervoltage condition is removed.

When device operates with SPI interface:

- The NPOR bit is reset and latched low once VCC goes above the UVLO threshold.
- NPOR remains in reset condition until cleared through the CLR_FLT bit or nSLEEP reset pulse.
- After power up, NPOR is automatically latched high once the CLR_FLT command is issued.

The VCC UVLO scenario is shown in Figure 7-45.

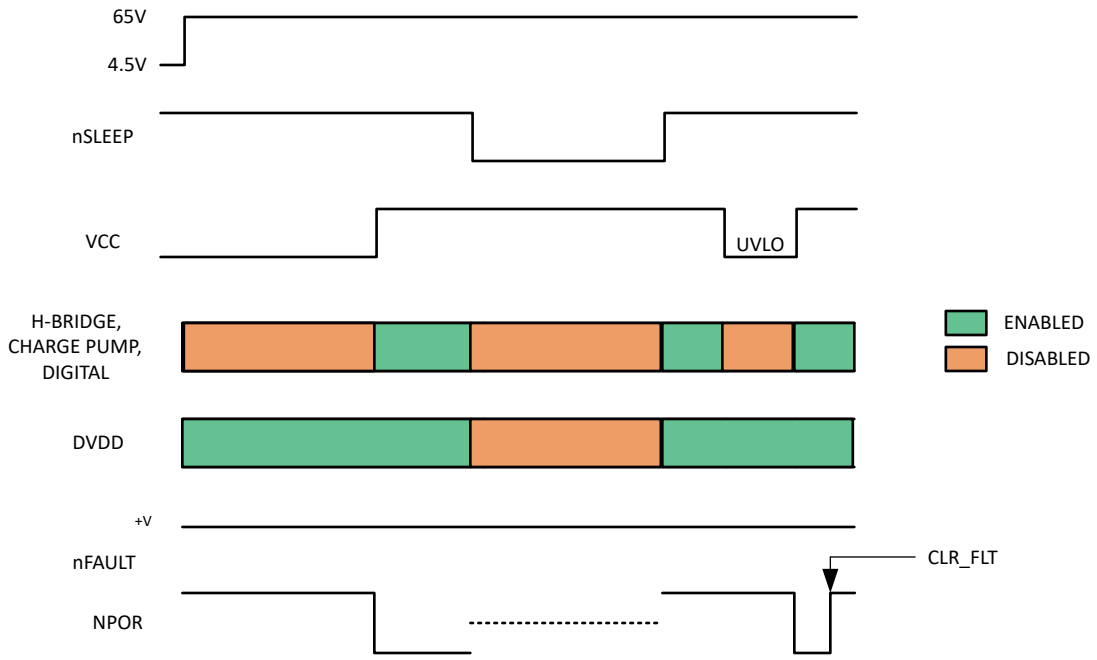

Figure 7-45. Logic Supply POR

7.4.20.4 Overcurrent Protection (OCP)

An analog current-limit circuit on any MOSFET limits the current through that MOSFET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, an overcurrent fault is detected.

- The MOSFETs in both H-bridges are disabled
- nFAULT is driven low
- Charge pump remains active.
- When operating with SPI interface -
  - FAULT and OCP bits are latched high
  - For xOUTy to VM short, corresponding OCP_LSy_x bit goes high.
  - For xOUTy to ground short, corresponding OCP_HSxy_x bit goes high.
  - The TOCP bit programs the overcurrent protection deglitch time.

The overcurrent protection can operate in two different modes: latched shutdown and automatic retry. The operating modes can be changed on the fly.

7.4.20.4.1 Latched Shutdown

To select latched shutdown mode:

- For H/W interface, the ENABLE pin has to be Hi-Z
- For SPI interface, the OCP_MODE bit should be '0'

In this mode, once the OCP condition is removed, normal operation resumes after applying a CLR_FLT command, an nSLEEP reset pulse or a power cycling.

7.4.20.4.2 Automatic Retry

To select automatic retry mode:

- For H/W interface, the ENABLE pin has to be HIGH (> 2.7 V)
- For SPI interface, the OCP_MODE bit should be '1'

In this mode, normal operation resumes automatically (motor-driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

7.4.20.5 Stall Detection

When operating with the SPI interface, the DRV8462 supports stall detection.

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Stepper motors have a distinct relation between the winding current, back-EMF, and mechanical torque load of the motor, as shown in Figure 7-46. For an unloaded motor, the back-EMF is 90° out-of-phase with the winding current. As motor load approaches the maximum torque capability of the motor for a given winding current, the back-EMF will move in phase with the winding current. By detecting back-EMF phase shift between rising and falling current quadrants of the motor current, the DRV8462 can detect a motor overload stall condition or an end-of-line travel.

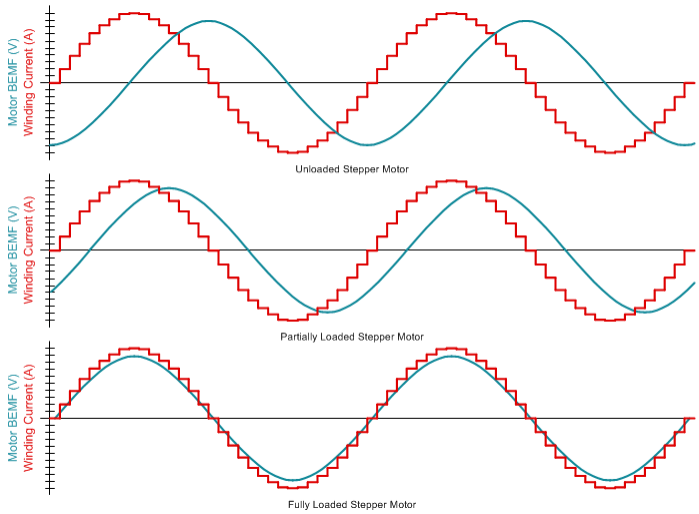

Figure 7-46. Stall Detection by Monitoring Motor Back-EMF

The Stall Detection algorithm is enabled when -

- The device is programmed to operate with the SPI interface (MODE = 1)
- The decay mode is programmed as smart tune Ripple Control (DECAY = '111')
- EN_STL is '1'
- No fault condition exists (UVLO, OCP, OL, OTSD etc.).

The algorithm compares the back-EMF between the rising and falling current quadrants by monitoring PWM off time and generates a parameter called torque count, represented by the 12-bit register TRQ_COUNT. The comparison is done in such a way that the TRQ_COUNT is largely independent of motor current, ambient temperature and supply voltage. Motor stall can be detected even if the driver is operating in full step mode.

TRQ_COUNT is calculated as a running average from the most recent four electrical half-cycles. TRQ_COUNT register is updated once every electrical half-cycle. The updated TRQ_COUNT is compared with the STALL_TH, and if a stall condition is detected, stall fault will be reported and latched at the electrical half-cycle current zero crossing.

For a lightly loaded motor, the TRQ_COUNT will be a non-zero value. As the motor approaches stall condition, TRQ_COUNT will approach zero and can be used to detect stall condition.

- If anytime TRQ_COUNT falls below the stall threshold (represented by the 12-bit STALL_TH register), the device will detect a stall.
- STALL, STL and FAULT bits are latched high in the SPI register.
- The STL_REP bit controls how stall is reported.
  - If STL_REP is '1', the nFAULT pin will be driven low when a stall is detected.
  - If STEL_REP is '0', the nFAULT pin will stay high even if stall is detected.

In the stalled condition, the motor shaft does not spin. The motor starts to spin again when the stall condition is removed and the motor ramps to its target speed. The nFAULT is released and the fault registers are cleared when a clear faults command is issued either via the CLR_FLT bit or an nSLEEP reset pulse.

High motor coil resistance can result in low TRQ_COUNT. The TRQ_SCALE bit allows scaling up low TRQ_COUNT values, for ease of further processing.

- If the initially calculated TRQ_COUNT value is less than 500 and the TRQ_SCALE bit is '1', then the TRQ_COUNT output in register is multiplied by a factor of 8.
- If the TRQ_SCALE bit is '0', TRQ_COUNT retains the value originally calculated by the algorithm.

Stall threshold can be set in two ways –

- The user can write the STALL_TH bits by observing the behavior of the TRQ_COUNT output at all operating conditions.
- The algorithm can learn the stall threshold using the automatic stall learning process, described below:
  - Before learning, ensure that the motor has reached its target speed. Do not learn stall threshold while the motor speed is ramping up or down.
  - Start learning by setting the STL_LRN bit to '1'.
  - Run motor with no load.
  - Wait for 32 electrical cycles for the driver to learn the steady-state count.
  - Stall the motor.
  - Wait for 16 electrical cycles for the driver to learn the stall count.
  - The STL_LRN_OK bit becomes '1' if learning is successful.
  - Stall threshold is calculated as the average of steady count and stall count and stored in the STALL_TH register.

The following flowchart shows the ways to set stall threshold.

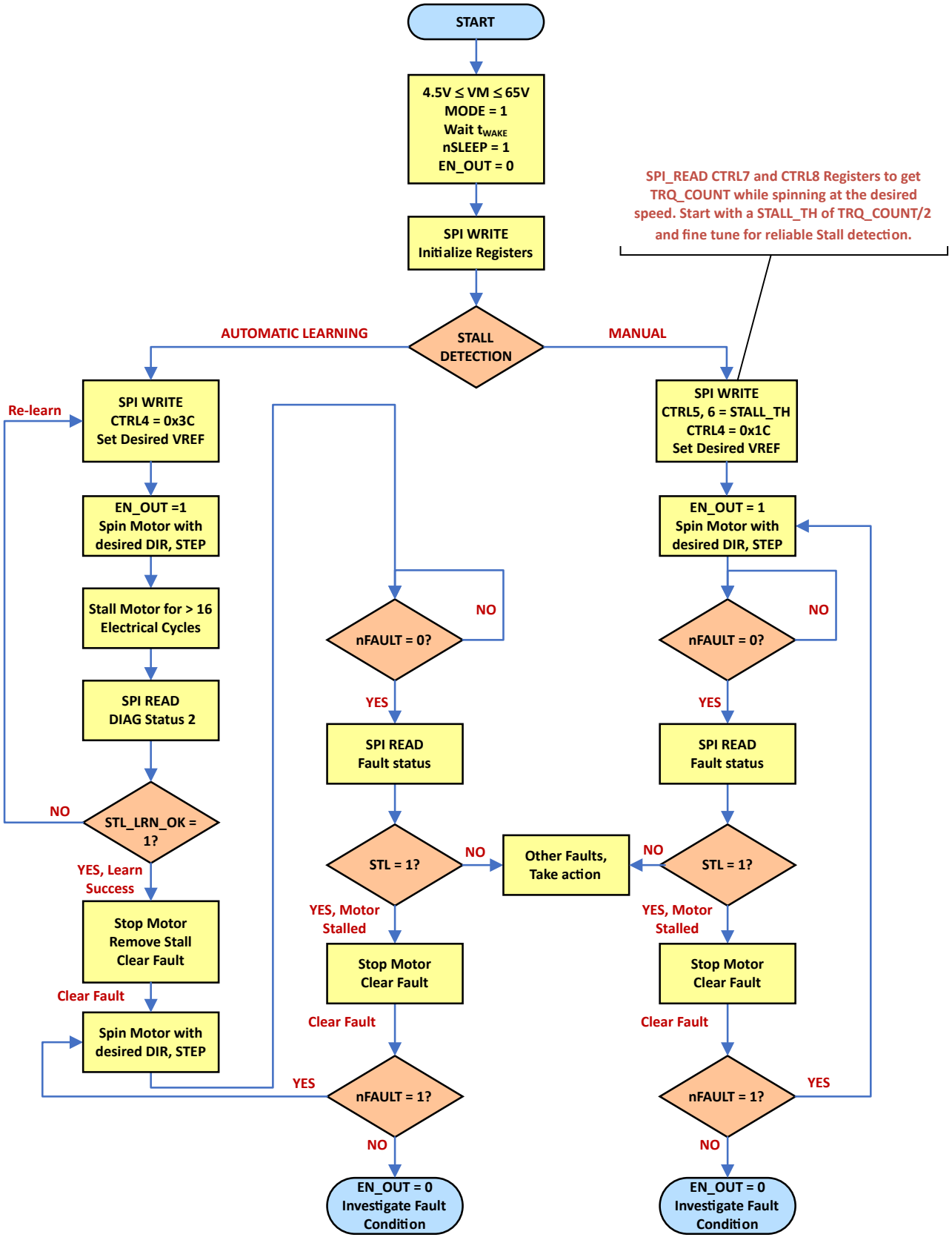

Figure 7-47. Stall learning flowchart

Sometimes the automatic stall learning process might not be successful due to an unstable torque count while the motor is running or stalled. For example, when the motor has high coil resistance or is running at very high or low speeds, the torque count might vary a lot over time and the difference between steady count and stall count might be small. In such cases, it is recommended not to use the automatic stall learning method. Instead, the user should carefully study the steady count and torque count across the range of operating conditions and set the threshold midway between the minimum steady count and the maximum stall count.

A stall threshold learnt at one speed may not work well for another speed. It is recommended to re-learn the stall threshold every time the motor speed is changed considerably.

Note

- The stall detection algorithm depends on back-EMF modifying the PWM off time. The back-EMF is directly proportional to the speed of the motor. In order for stall detection to work reliably, minimum motor speed is required for generating back-EMF with sufficient amplitude. Higher motor coil resistance would require higher minimum speed for reliable stall detection.
- If there is loss of current regulation due to low supply voltage, high coil resistance or high speed of the motor, stall detection may not work reliably, because the TRQ_COUNT can be erratic and may jump to a high value. This can be checked and confirmed by looking at the coil current waveform. If the coil current has a standard sinusoidal waveform, and the peak of the sinusoid reaches the desired full-scale current, then stall detection will work reliably. If the current waveform is triangular due to high speed or low supply voltage, stall detection algorithm might not work reliably.
- If EN_STL = '1' and auto-torque is also enabled, coil current goes to ATQ_TRQ_MAX when motor stall is detected
- If EN_STL = '0' and auto-torque is enabled, coil current goes to ATQ_TRQ_MIN when motor is stalled.

7.4.20.6 Open-Load Detection (OL)

Open-load fault is detected -

- When the motor is running, if the winding current in any coil drops below the open-load current threshold (I_{OL})
- When the motor is in a holding condition, if the winding current in any coil drops below the I_{TRIP} level set by the indexer.
- If this condition persists for more than the open-load detection time (t_{OL})
- The EN_OL bit is '1' if the device is operating with SPI interface.

The open-load detection time (t_{OL}) is set as follows -

Table 7-24. Open-load Detection Time

MODE	OL_T	Maximum t_{OL} (ms)
0 (H/W interface)	NA	60
1 (SPI interface)	00	30
	01 (default)	60
	10	120

Once the open-load fault is detected -

- nFAULT is pulled low.
- If the device is operating with SPI interface -
  - OL and FAULT bits are latched high
  - If the OL_A bit is high, it indicates an open load fault in winding A, between AOUT1 and AOUT2.
  - An open load fault between BOUT1 and BOUT2 causes the OL_B bit to go high.

When the open-load condition is removed, the behavior depends on whether the device is configured with H/W interface or SPI interface.

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When the device is configured with H/W interface and open-load condition is removed:

- If the ENABLE pin is logic HIGH, nFAULT is released immediately.
- If the ENABLE pin is Hi-Z, nFAULT is released after a nSLEEP reset pulse has been applied.

When the device is configured with SPI interface and open-load condition is removed:

- If the OL_MODE bit is '1', nFAULT is released immediately.
- If the OL_MODE bit is '0', nFAULT is released after a clear faults command is issued either via the CLR_FLT bit or an nSLEEP reset pulse.

The open-load fault also clears when the device is power cycled or comes out of sleep mode.

Note

- The open-load fault detection is not supported in the silent step decay mode. Write '0' to EN_OL if EN_SS is '1'.
- If ENABLE pin is changed from logic HIGH to Hi-Z on-the-fly, apply a nSLEEP reset pulse.
- If OL_MODE is changed from '1' to '0' or EN_OL is changed from '1' to '0', apply a clear faults command.
- When the device is operating with auto-torque enabled, if open-load fault is detected, the coil current goes to a value corresponding to TRQ_DAC.

7.4.20.7 Overtemperature Warning (OTW)

OTW is detected -

- If the device is operating with SPI interface (MODE = 1)
- If the die temperature exceeds the trip point of the overtemperature warning (T_{OTW})

When the OTW is detected -

- OTW and TF bits are set.
- The device performs no additional action and continues to function.
- The charge pump remains active.
- If the TW_REP bit is '1' -
  - nFAULT is pulled low in the event of OTW
  - FAULT bit is set

When the die temperature falls below the hysteresis point (T_{HYS_OTW}) of the overtemperature warning, the OTW and TF bits clear automatically.

7.4.20.8 Thermal Shutdown (OTSD)

Thermal shutdown is detected if the die temperature exceeds the thermal shutdown limit (T_{OTSD}). When thermal shutdown is detected -

- All MOSFETs in the H-bridges are disabled
- nFAULT is driven low
- Charge pump is disabled
- For operation with SPI interface
  - FAULT, TF and OTS bits are set high

The recovery from thermal shutdown protection can be in two different modes: latched shutdown and automatic retry. The recovery modes can be changed on the fly.

7.4.20.8.1 Latched Shutdown

To select latched shutdown mode,

- If device is operating with H/W interface, the ENABLE pin should be Hi-Z
- If device is operating with SPI interface, OTSD_MODE should be '0'

In this mode, after the junction temperature falls below the overtemperature threshold limit minus the hysteresis (T_{OTSD} – T_{HYS_OTSD}), normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

7.4.20.8.2 Automatic Retry

To select automatic retry mode,

- For H/W interface, the ENABLE pin has to be logic HIGH (>2.7V)
- For SPI interface, OTSD_MODE bit should be '1'

In this mode, normal operation resumes (motor-driver operation and the nFAULT line released) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis (T_{OTSD} – T_{HYS_OTSD}). When operating with SPI interface, the TF and OTS bits remain latched high indicating that a thermal event occurred until a clear faults command is issued either via the CLR_FLT bit or an nSLEEP reset pulse.

7.4.20.9 nFAULT Output

The nFAULT pin has an open-drain output and should be pulled up to a 5-V, 3.3-V or 1.8-V supply. nFAULT pin will be high after power-up. When a fault is detected, the nFAULT pin will be logic low. For a 5-V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V or 1.8-V pullup, an external supply must be used.

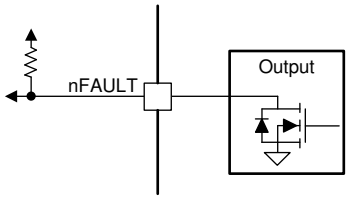

Figure 7-48. nFAULT Pin

7.4.20.10 Fault Condition Summary

Table 7-25. Fault Condition Summary

FAULT	CONDITION	CONFIGURATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	—	nFAULT / SPI	Disabled	Disabled	Disabled	Reset	VM > V_{UVLO}
VCP undervoltage (CPUV)	VCP < V_{CPUV}	—	nFAULT / SPI	Disabled	Operating	Operating	Operating	VCP > V_{CPUV}
Logic Supply POR	VCC < VCC_{UVLO}	—	SPI	Disabled	Disabled	Disbaled	Reset	VCC > VCC_{UVLO}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	OCP_MODE = 0b / ENABLE = Hi-Z	nFAULT / SPI	Disabled	Operating	Operating	Operating	Latched: CLR_FLT / nSLEEP
		OCP_MODE = 1b / ENABLE = 1	nFAULT / SPI	Disabled	Operating	Operating	Operating	Automatic retry: t_{RETRY}
Open Load (OL)	No load detected	Default (H/W) / EN_OL = 1b (SPI)	nFAULT / SPI	Operating	Operating	Operating	Operating	Report only
Stall Detection (STALL)	Stall / stuck motor	STL_REP = 0b	SPI	Operating	Operating	Operating	Operating	CLR_FLT / nSLEEP
		STL_REP = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	
Overtemperature Warning (OTW)	T_J > T_{OTW}	TW_REP = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	Automatic: T_J < T_{OTW} - T_{HYS_OTW}
		TW_REP = 0b	SPI	Operating	Operating	Operating	Operating	

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Table 7-25. Fault Condition Summary (continued)

FAULT	CONDITION	CONFIGURATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
Thermal Shutdown (OTSD)	$T_J > T_{OTSD}$	OTSD_MODE = 0b / ENABLE = Hi-Z	nFAULT / SPI	Disabled	Disabled	Operating	Operating	Latched: CLR_FLT / nSLEEP
		OTSD_MODE = 1b / ENABLE = 1	nFAULT/ SPI	Disabled	Disabled	Operating	Operating	Automatic: $T_J < T_{OTSD} - T_{HYS\_OTSD}$

Note

For pre-production samples, if the device is configured to operate with H/W interface, and the M0 pin is Hi-z at power-up, then the nFAULT pin will stay low even if there are no faults. To release the nFAULT, the user has to apply an nSLEEP reset pulse.

This behavior will not be present in the production samples - nFAULT will be pulled-high after power-up if there are no faults.

7.4.21 Device Functional Modes

7.4.21.1 Sleep Mode

When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs, the DVDD regulator, SPI and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.21.2 Disable Mode

The ENABLE pin is used to enable or disable the half bridges in the device. When the ENABLE pin is low, the output drivers are disabled (Hi-Z). For operation with SPI interface, the EN_OUT bit can also be used to disable the output drivers. When the EN_OUT bit is '0', the output drivers are disabled (Hi-Z).

Table 7-26. Conditions to Enable or Disable Output Drivers

nSLEEP	ENABLE	EN_OUT	H-BRIDGE
0	Don't Care	Don't Care	Disabled
1	0	0	Disabled
1	0	1	Disabled
1	1	0	Disabled
1	1	1	Enabled

7.4.21.3 Operating Mode

This mode is enabled when -

- nSLEEP is high
- ENABLE pin is Hi-Z or 1
- EN_OUT = '1' for SPI interface
- VM > UVLO

The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.21.4 nSLEEP Reset Pulse

A latched fault can be cleared by an nSLEEP reset pulse. This pulse width must be greater than 20 µs and smaller than 40 µs. If nSLEEP is low for longer than 40 µs, but less than 120 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram below. This reset pulse does not affect the status of the charge pump or other functional blocks.

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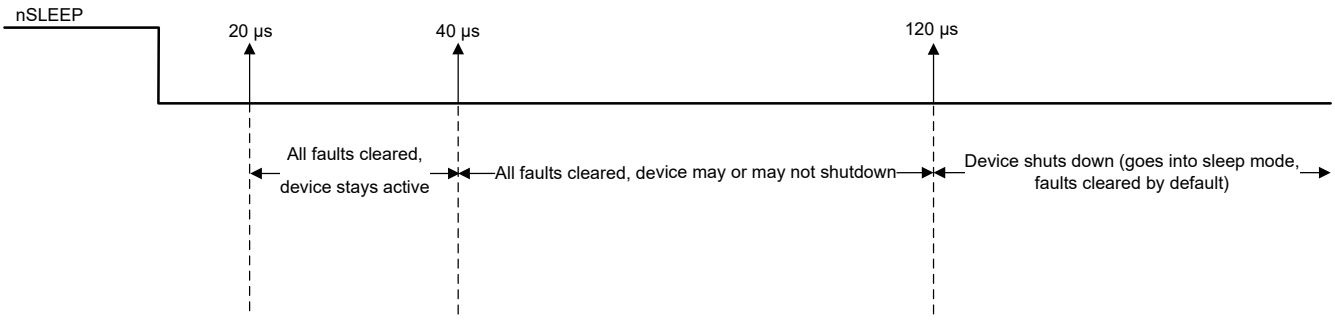

Figure 7-49. nSLEEP Reset Pulse

Note

For the pre-production samples, when the device is configured to operate with H/W interface, nFAULT will be pulled-low after device wakes up. An nSLEEP reset pulse has to be applied to release the nFAULT output.

This behavior will not be present in production samples.

7.4.21.5 Functional Modes Summary

Table 7-27. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	INDEXER	Logic
Sleep mode	4.5 V < VM < 65 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled	Disabled
Operating	4.5 V < VM < 65 V	nSLEEP pin = 1 ENABLE = 1 and EN_OUT = '1'	Operating	Operating	Operating	Operating	Operating
Disabled	4.5 V < VM < 65 V	nSLEEP pin = 1 ENABLE pin = 0 or EN_OUT = '0'	Disabled	Operating	Operating	Operating	Operating

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7.5 Programming

7.5.1 Serial Peripheral Interface (SPI) Communication

When configured to operate with SPI interface, the device has full duplex, 4-wire synchronous communication that is used to set device configurations, operating parameters, and read out diagnostic information from the device. This section describes the SPI protocol, the command structure, and the control and status registers. The SPI operates in target mode and can be connected with a controller in the following configurations:

- One target device
- Multiple target devices in parallel connection
- Multiple target devices in series (daisy chain) connection

7.5.1.1 SPI Format

The serial data input (SDI) word consists of a 16-bit word, with an 8 bit-command (A1), followed by 8-bit data (D1). The serial data output (SDO) word consists of 8 bits of status register with fault status indication (S1), followed by a report byte (R1). Figure 7-50 shows the data sequence between the controller and the SPI target driver.

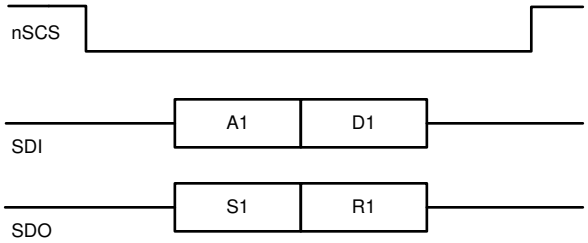

Figure 7-50. SPI Format - Standard "16-bit" Frame

A valid frame must meet the following conditions:

- The SCLK pin must be low when the nSCS pin goes low and when the nSCS pin goes high.
- The nSCS pin should be taken high for at least 500 ns between frames.
- When the nSCS pin is asserted high, any signals at the SCLK and SDI pins are ignored, and the SDO pin is in the high-impedance state (Hi-Z).
- A full 16 SCLK cycles must occur for a valid transaction for a standard frame, or alternately, for a daisy chain frame with "n" number of peripheral devices, 16 + (n x 16) SCLK cycles must occur for a valid transaction. Else, a frame error (SPI_ERROR) is reported and the data is ignored if it is a WRITE operation.
- Data on SDO from the device is propagated on the rising edge of SCLK, while data on SDI is captured by the device on the subsequent falling edge of SCLK.
- The most-significant bit (MSB) is shifted in and out first.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit command data.

The SDI input data word is 16 bits long and consists of the following format:

- Command byte (first 8 bits)
  - MSB bit indicates frame type (bit B15 = 0 for standard frame).
  - Next to MSB bit, W0, indicates read or write operation (bit B14, write = 0, read = 1)
  - W0 is followed by 6 address bits, A[5:0] (bits B13 through B8)
- Data byte (last 8 bits)
  - Last 8 bits indicate data, D[7:0] (bits B7 through B0). For a read operation, these bits are typically set to null values, while for a write operation, these bits have the data value for the addressed register.

Table 7-28. SDI - Standard Frame Format

	R/W	ADDRESS						DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

The SDO output data word is 16 bits long and consists of the following format:

- Status byte (first 8 bits)
  - 2 MSB bits are forced high (B15, B14 = 1).
  - Following 6 bits are from the FAULT register (bits B13 through B8)
- Report byte (last 8 bits)
  - The last 8 bits (B7:B0) are either the data currently in the register being read for a read operation (W0 =1), or, existing data in the register being written to for a write command (W0 = 0).

Table 7-29. SDO Output Data Word Format

STATUS								REPORT							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	UVLO	CPUV	OCP	STL	TF	OL	D7	D6	D5	D4	D3	D2	D1	D0

7.5.1.2 SPI for Multiple Target Devices in Daisy Chain Configuration

Multiple devices can be connected to the controller with and without the daisy chain. For connecting 'n' number of devices to a controller without using a daisy chain, 'n' number of GPIO resources from controller have to be utilized for nSCS pins. Whereas, if the daisy chain configuration is used, a single nSCS line can be used for connecting multiple devices.

Figure 7-51 shows the topology when three devices are connected in daisy chain. This configuration saves GPIO ports when multiple devices are communicating to the same controller.

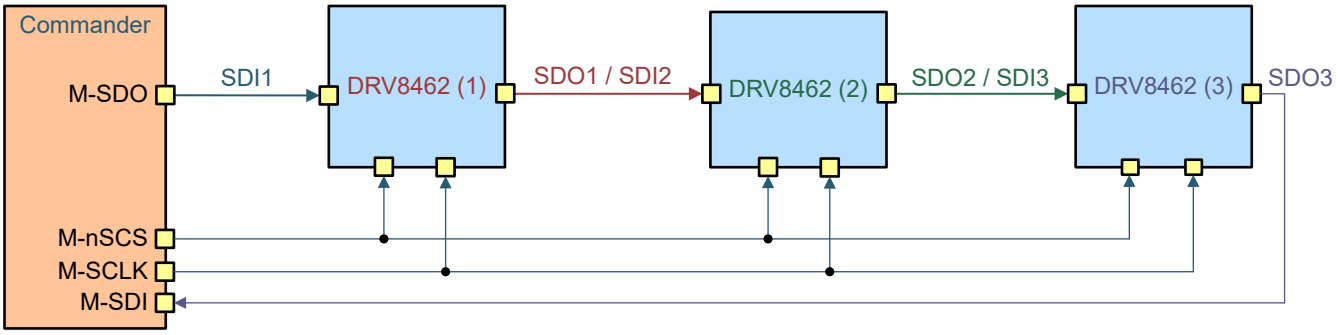

Figure 7-51. Three Devices Connected in Daisy Chain

The first device in the chain receives data from the MCU in the following format for 3-device configuration: 2 bytes of header (HDRx) followed by 3 bytes of address (Ax) followed by 3 bytes of data (Dx).

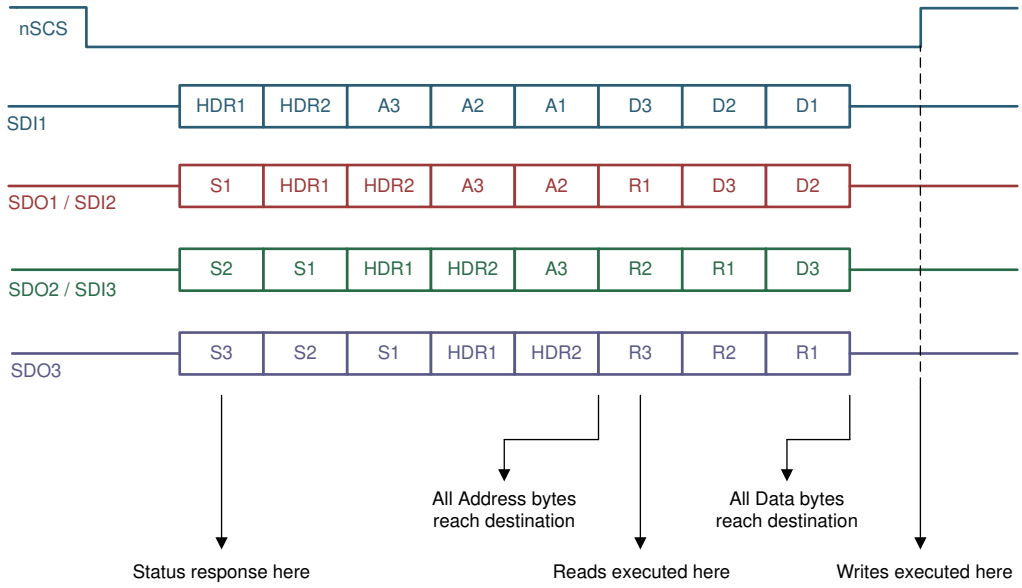

Figure 7-52. SPI Frame With Three Devices

After the data has been transmitted through the chain, the MCU receives the data string in the following format for 3-device configuration: 3 bytes of status (Sx) followed by 2 bytes of header followed by 3 bytes of report (Rx).

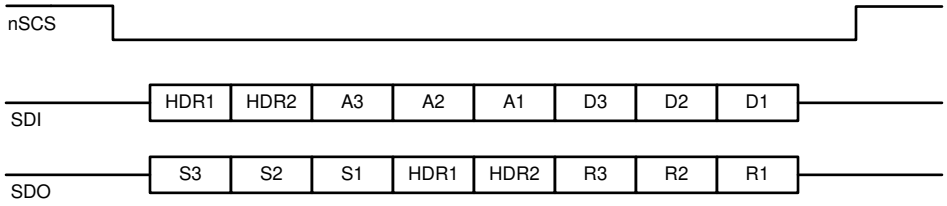

Figure 7-53. SPI Data Sequence for Three Devices

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The header bytes contain information of the number of devices connected in the chain, and a global clear fault command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. Header values N5 through N0 are 6 bits dedicated to show the number of devices in the chain. Up to 63 devices can be connected in series for each daisy chain connection.

The 5 LSBs of the HDR2 register are don't care bits that can be used by the MCU to determine integrity of the daisy chain connection. Header bytes must start with 1 and 0 for the two MSBs.

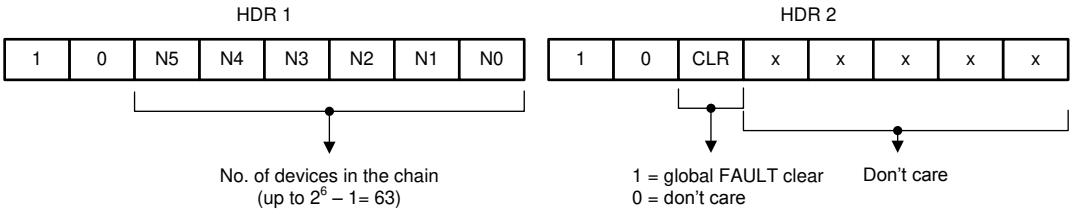

Figure 7-54. Header Bytes

The status byte provides information about the fault status register for each device in the daisy chain so that the MCU does not have to initiate a read command to read the fault status from any particular device. This keeps additional read commands for the MCU and makes the system more efficient to determine fault conditions flagged in a device. Status bytes must start with 1 and 1 for the two MSBs.

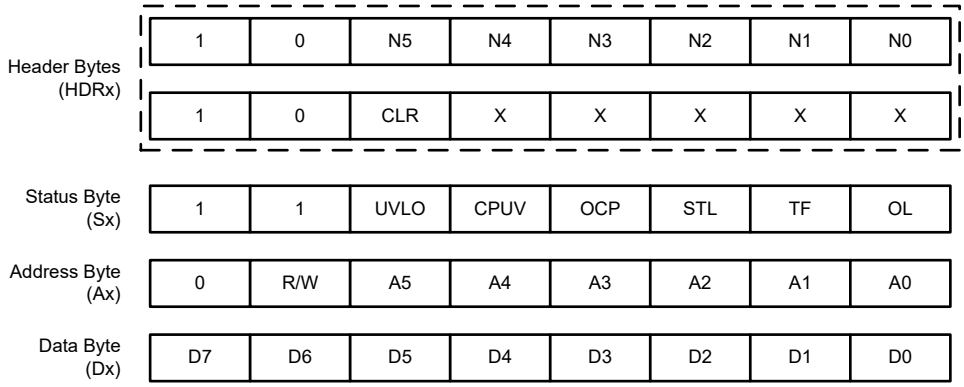

Figure 7-55. Contents of Header, Status, Address, and Data Bytes

When data passes through a device, it determines the position of itself in the chain by counting the number of status bytes it receives followed by the first header byte. For example, in this 3-device configuration, device 2 in the chain receives two status bytes before receiving the HDR1 byte which is then followed by the HDR2 byte.

From the two status bytes, the data can determine that its position is second in the chain. From the HDR2 byte, the data can determine how many devices are connected in the chain. In this way, the data only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The address and data bytes remain the same with respect to a 1-device connection. The report bytes (R1 through R3), as shown in Figure 7-53, are the content of the register being accessed.

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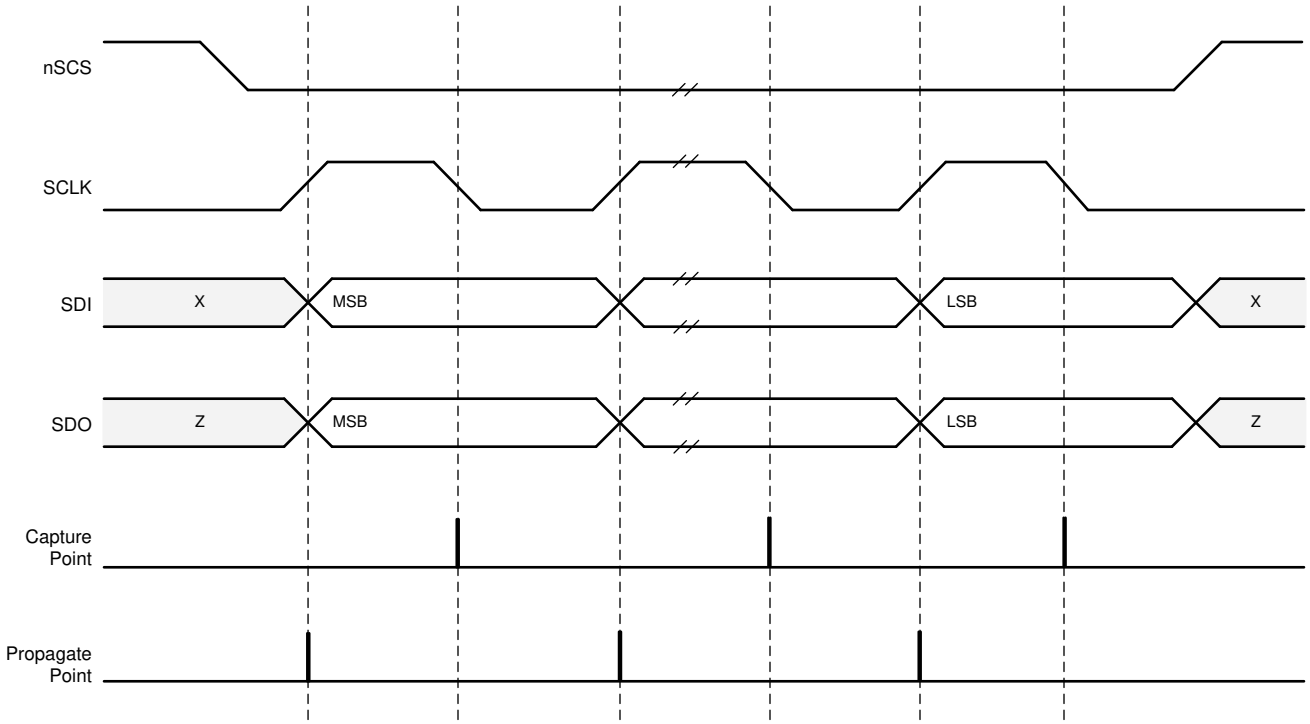

Figure 7-56. SPI Transaction

7.5.1.3 SPI for Multiple Target Devices in Parallel Configuration

Figure 7-57 shows three DRV8462 devices connected in parallel configuration.

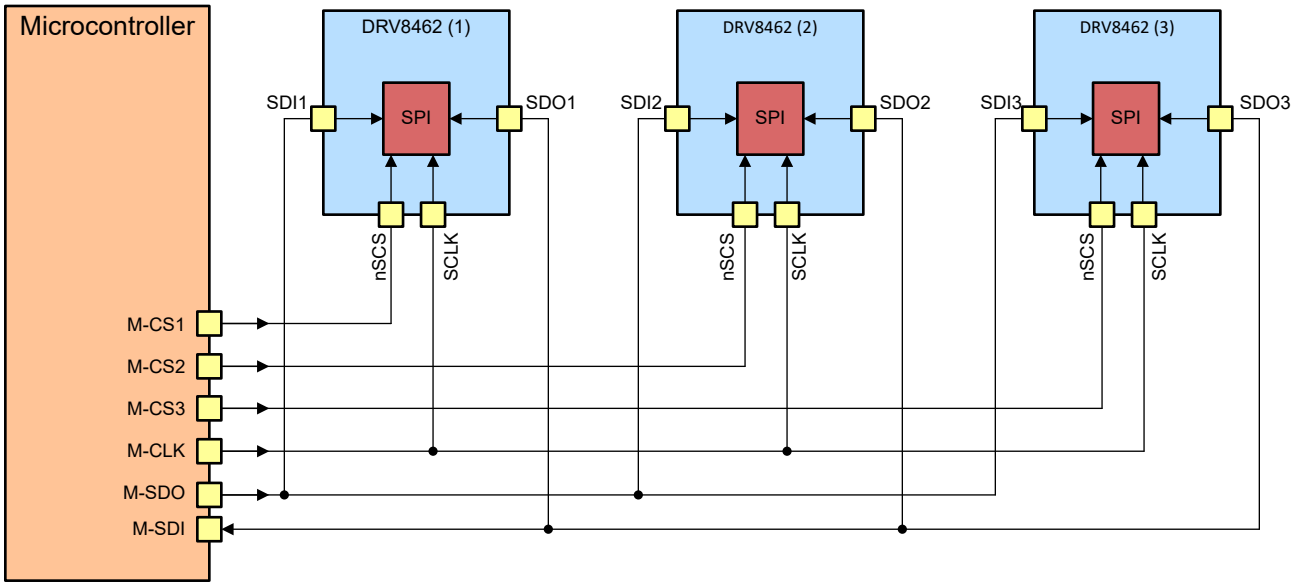

Figure 7-57. Three Devices Connected in Parallel Configuration

7.6 Register Maps

Table 7-30 lists the memory-mapped registers for the device. All register addresses not listed in Table 7-30 should be considered as reserved locations and the register contents must not be modified.

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Table 7-30. Memory Map

Register	7	6	5	4	3	2	1	0	Type	Address
FAULT	FAULT	SPI_ERROR	UVLO	CPUV	OCP	STL	TF	OL	R	0x00
DIAG1	OCP_LS2_B	OCP_HS2_B	OCP_LS1_B	OCP_HS1_B	OCP_LS2_A	OCP_HS2_A	OCP_LS1_A	OCP_HS1_A	R	0x01
DIAG2	STSL	OTW	OTS	STL_LRN_OK	STALL	LRN_DONE	OL_B	OL_A	R	0x02
DIAG3	RSVD	NHOME	CNT_OFLW	CNT_UFLW	RSVD	NPOR	RSVD		R	0x03
CTRL1	EN_OUT	SR	RSVD	TOFF [1:0]		DECAY [2:0]			RW	0x04
CTRL2	DIR	STEP	SPI_DIR	SPI_STEP	MICROSTEP_MODE [3:0]				RW	0x05
CTRL3	CLR_FLT	LOCK [2:0]			TOCP	OCP_MODE	OTSD_MODE	OTW_REP	RW	0x06
CTRL4	TBLANK_TIME[1:0]		STL_LRN	EN_STL	STL_REP	STL_FRQ	STEP_FRQ_TOL[1:0]		RW	0x07
CTRL5	STALL_TH [7:0]								RW	0x08
CTRL6	RC_RIPPLE[1:0]		DIS_SSC	TRQ_SCALE	STALL_TH[11:8]				RW	0x09
CTRL7	TRQ_COUNT [7:0]								R	0x0A
CTRL8	RSVD				TRQ_COUNT[11:8]				R	0x0B
CTRL9	EN_OL	OL_MODE	OL_T[1:0]		STEP_EDGE	RES_AUTO[1:0]		EN_AUTO	RW	0x0C
CTRL10	ISTSL[7:0]								RW	0x0D
CTRL11	TRQ_DAC[7:0]								RW	0x0E
CTRL12	EN_STSL	TSTSL_FALL[3:0]				RSVD			RW	0x0F
CTRL13	TSTSL_DLY[5:0]						RSVD		RW	0x10
INDEX1	CUR_A_POS[7:0]								R	0x11
INDEX2	CUR_A_SIGN	RSVD							R	0x12
INDEX3	CUR_B_POS[7:0]								R	0x13
INDEX4	CUR_B_SIGN	RSVD					INDEX_POS[9:8]		R	0x14
INDEX5	INDEX_POS[7:0]								R	0x15
CUSTOM_CTRL1	RSVD							EN_CUSTOM	RW	0x16
CUSTOM_CTRL2	CUSTOM_CURRENT1[7:0]								RW	0x17
CUSTOM_CTRL3	CUSTOM_CURRENT2[7:0]								RW	0x18
CUSTOM_CTRL4	CUSTOM_CURRENT3[7:0]								RW	0x19
CUSTOM_CTRL5	CUSTOM_CURRENT4[7:0]								RW	0x1A
CUSTOM_CTRL6	CUSTOM_CURRENT5[7:0]								RW	0x1B
CUSTOM_CTRL7	CUSTOM_CURRENT6[7:0]								RW	0x1C
CUSTOM_CTRL8	CUSTOM_CURRENT7[7:0]								RW	0x1D
CUSTOM_CTRL9	CUSTOM_CURRENT8[7:0]								RW	0x1E
ATQ_CTRL1	ATQ_CNT[7:0]								R	0x1F
ATQ_CTRL2	ATQ_CNT[10:8]			RSVD		ATQ_LRN_CONST1[10:8]			RW	0x20
ATQ_CTRL3	ATQ_LRN_CONST1[7:0]								RW	0x21
ATQ_CTRL4	ATQ_LRN_MIN_CURRENT[4:0]					ATQ_LRN_CONST2[10:8]			RW	0x22
ATQ_CTRL5	ATQ_LRN_CONST2[7:0]								RW	0x23
ATQ_CTRL6	ATQ_UL[7:0]								RW	0x24
ATQ_CTRL7	ATQ_LL[7:0]								RW	0x25
ATQ_CTRL8	KP[7:0]								RW	0x26
ATQ_CTRL9	KI[3:0]				KD[3:0]				RW	0x27
ATQ_CTRL10	ATQ_EN	LRN_START	ATQ_FRZ[2:0]			ATQ_AVG[2:0]			RW	0x28

Table 7-30. Memory Map (continued)

Register	7	6	5	4	3	2	1	0	Type	Address
ATQ_CTRL11	ATQ_TRQ_MIN[7:0]								RW	0x29
ATQ_CTRL12	ATQ_TRQ_MAX[7:0]								RW	0x2A
ATQ_CTRL13	ATQ_D_THR[7:0]								RW	0x2B
ATQ_CTRL14	ATQ_MAX_INTEGRAL[7:0]								RW	0x2C
ATQ_CTRL15	ATQ_ERROR_TRUNCATE[3:0]				ATQ_LRN_STEP[1:0]		ATQ_LRN_CYCLE_SELECT[1:0]		RW	0x2D
ATQ_CTRL16	ATQ_TRQ_DAC[7:0]								R	0x2E
ATQ_CTRL17	RSVD								RW	0x2F
ATQ_CTRL18	RSVD		VREF_INT_EN	RSVD					RW	0x30
SS_CTRL1	RSVD				SS_PWM_FREQ[1:0]		RSVD	EN_SS	RW	0x31
SS_CTRL2	RSVD	SS_KP[6:0]							RW	0x32
SS_CTRL3	RSVD	SS_KI[6:0]							RW	0x33
SS_CTRL4	RSVD	SS_KI_DIV_SEL[2:0]			RSVD	SS_KP_DIV_SEL[2:0]			RW	0x34
SS_CTRL5	SS_THR[7:0]								RW	0x35
CTRL14	RSVD								RW	0x3C

Complex bit access types are encoded to fit into small table cells. Table 7-31 shows the codes that are used for access types in this section.

Table 7-31. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

Note

- The VREF_INT_EN bit is located in ATQ_CTRL18 register bit 5 in pre-production samples. For production samples, the VREF_INT_EN bit will be located in CTRL13 register bit 1.
- The production samples will feature an INDEX_RESET bit located in CTRL1 register bit 5. This bit will reset the indexer to 45° electrical angle, but the contents of the registers will not change.
- The production samples will feature a VM_SCALE bit located in ATQ_CTRL17 bit 6. When enabled, this bit will modify the auto-torque learning routine parameters in the event of a supply voltage change. In pre-production samples, this bit will be reserved.
- The production samples will feature VM_ADC bits located in the CTRL14 register. These bits will output the value of the supply voltage. For the pre-production samples, the CTRL14 will be reserved.

7.6.1 Status Registers

The status registers are used to reporting warning and fault conditions. Status registers are read-only registers.

Table 7-32 lists the memory-mapped registers for the status registers. All register offset addresses not listed in Table 7-32 should be considered as reserved locations and the register contents should not be modified.

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Table 7-32. Status Registers Summary Table

Address	Register Name	Section
0x00	FAULT	Go
0x01	DIAG1	Go
0x02	DIAG2	Go
0x03	DIAG3	Go

7.6.1.1 FAULT (address = 0x00) [Default = 00h]

FAULT status is shown in Figure 7-58 and described in Table 7-33.

Read-only

Return to the Register Maps Table

Figure 7-58. FAULT Register

7	6	5	4	3	2	1	0
FAULT	SPI_ERROR	UVLO	CPUV	OCP	STL	TF	OL
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-33. FAULT Register Field Descriptions

Bit	Field	Type	Default	Description
7	FAULT	R	0b	FAULT bit is '1' when device has any fault condition. During normal operation, FAULT bit is '0'. nFAULT pin is pulled down when FAULT bit is '1'. nFAULT pin is released during normal operation.
6	SPI_ERROR	R	0b	Indicates SPI protocol errors, such as more SCLK pulses than are required or SCLK is absent even though nSCS is low. SPI_ERROR becomes '1' in fault and the nFAULT pin is driven low. Normal operation resumes when the protocol error is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse.
5	UVLO	R	0b	When this bit is '1', it indicates an supply undervoltage lockout fault condition.
4	CPUV	R	0b	When this bit is '1', it indicates charge pump undervoltage fault condition.
3	OCP	R	0b	When this bit is '1', it indicates overcurrent fault condition
2	STL	R	0b	When this bit is '1', it indicates motor stall condition.
1	TF	R	0b	Logic OR of the overtemperature warning (OTW) and overtemperature shutdown (OTSD). When this bit is '1', it indicates overtemperature fault.
0	OL	R	0b	When this bit is '1', it indicates open-load condition.

7.6.1.2 DIAG1 (address = 0x01) [Default = 00h]

DIAG1 is shown in Figure 7-59 and described in Table 7-34.

Read-only

Return to the Register Maps Table

Figure 7-59. DIAG1 Register

7	6	5	4	3	2	1	0
OCP_LS2_B	OCP_HS2_B	OCP_LS1_B	OCP_HS1_B	OCP_LS2_A	OCP_HS2_A	OCP_LS1_A	OCP_HS1_A
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-34. DIAG1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	OCP_LS2_B	R	0b	When this bit is '1', it indicates overcurrent fault on the low-side FET of half bridge connected to BOUT2
6	OCP_HS2_B	R	0b	When this bit is '1', it indicates overcurrent fault on the high-side FET of half bridge connected to BOUT2
5	OCP_LS1_B	R	0b	When this bit is '1', it indicates overcurrent fault on the low-side FET of half bridge connected to BOUT1
4	OCP_HS1_B	R	0b	When this bit is '1', it indicates overcurrent fault on the high-side FET of half bridge connected to BOUT1
3	OCP_LS2_A	R	0b	When this bit is '1', it indicates overcurrent fault on the low-side FET of half bridge connected to AOUT2
2	OCP_HS2_A	R	0b	When this bit is '1', it indicates overcurrent fault on the high-side FET of half bridge connected to AOUT2
1	OCP_LS1_A	R	0b	When this bit is '1', it indicates overcurrent fault on the low-side FET of half bridge connected to AOUT1
0	OCP_HS1_A	R	0b	When this bit is '1', it indicates overcurrent fault on the high-side FET of half bridge connected to AOUT1

7.6.1.3 DIAG2 (address = 0x02) [Default = 00h]

DIAG2 is shown in Figure 7-60 and described in Table 7-35.

Read-only

Return to the Register Maps Table

Figure 7-60. DIAG2 Register

7	6	5	4	3	2	1	0
STSL	OTW	OTS	STL_LRN_OK	STALL	LRN_DONE	OL_B	OL_A
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-35. DIAG2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	STSL	R	0b	When this bit is '1', it indicates that the device is operating with standstill power saving mode.
6	OTW	R	0b	When this bit is '1', it indicates overtemperature warning.
5	OTS	R	0b	When this bit is '1', it indicates overtemperature shutdown.
4	STL_LRN_OK	R	0b	When this bit is '1', it indicates stall detection learning is successful.
3	STALL	R	0b	When this bit is '1', it indicates motor stall condition.
2	LRN_DONE	R	0b	When this bit is '1', it indicates auto torque learning is successful.
1	OL_B	R	0b	When this bit is '1', it indicates open-load detection on BOUT coil.
0	OL_A	R	0b	When this bit is '1', it indicates open-load detection on AOUT coil.

7.6.1.4 DIAG3 (address = 0x03) [Default = 00h]

DIAG3 is shown in Figure 7-61 and described in Table 7-36.

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Read-only

Return to the Register Maps Table

Figure 7-61. DIAG3 Register

7	6	5	4	3	2	1	0
RSVD	NHOME	CNT_OFLW	CNT_UFLW	RSVD	NPOR	RSVD	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-00b	

Table 7-36. DIAG3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R	0b	Reserved
6	NHOME	R	0b	When this bit is '1', it indicates indexer is at a position other than home position.
5	CNT_OFLW	R	0b	When this bit is '1', it indicates ATQ_CNT is more than ATQ_UL
4	CNT_UFLW	R	0b	When this bit is '1', it indicates ATQ_CNT is less than ATQ_LL
3	RSVD	R	0b	Reserved
2	NPOR	R	0b	**0b = Indicates a prior VCC UVLO event** 1b = Indicates that the NPOR bit has been cleared by a CLR_FLT or nSLEEP reset pulse input after a VCC UVLO event
1-0	RSVD	R	00b	Reserved

7.6.2 Control Registers

The IC control registers are used to configure the device. Control registers are read and write capable.

Table 7-37 lists the memory-mapped registers for the control registers. All register offset addresses not listed in Table 7-37 should be considered as reserved locations and the register contents should not be modified.

Table 7-37. Control Registers Summary Table

Address	Register Name	Section
0x04	CTRL1	Go
0x05	CTRL2	Go
0x06	CTRL3	Go
0x07	CTRL4	Go
0x08	CTRL5	Go
0x09	CTRL6	Go
0x0A	CTRL7	Go
0x0B	CTRL8	Go
0x0C	CTRL9	Go
0x0D	CTRL10	Go
0x0E	CTRL11	Go
0x0F	CTRL12	Go
0x1A	CTRL13	Go
0x3C	CTRL14	Go

7.6.2.1 CTRL1 (address = 0x04) [Default = 0Fh]

CTRL1 is shown in Figure 7-62 and described in Table 7-38.

Read/Write

Return to the Register Maps Table

Figure 7-62. CTRL1 Control Register

7	6	5	4	3	2	1	0
EN_OUT	SR	RSVD	TOFF [1:0]		DECAY [2:0]		
R/W-0b	R/W-0b	R/W-0b	R/W-01b		R/W-111b		

Table 7-38. CTRL1 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	EN_OUT	R/W	0b	**0b = All outputs are disabled** 1b = All outputs are enabled
6	SR	R/W	0b	**0b = Output rise/fall time 100 ns** 1b = Output rise/fall time 50 ns
5	RSVD	R/W	0b	Reserved.
4-3	TOFF [1:0]	R/W	01b	00b = 7 µs **01b = 16 µs** 10b = 24 µs 11b = 32 µs
2-0	DECAY [2:0]	R/W	111b	000b = Reserved 001b = SLOW - MIXED 30% decay 010b = SLOW - MIXED 60% decay 011b = SLOW - FAST decay 100b = MIXED 30% - MIXED 30% decay 101b = Reserved 110b = Smart tune Dynamic Decay **111b = Smart tune Ripple Control**

Note

The production samples will feature an INDEX_RESET bit located in CTRL1 register bit 5. This bit will reset the indexer to 45° electrical angle, but the contents of the registers will not change. For pre-production samples, the CTRL1 bit 5 will be reserved.

7.6.2.2 CTRL2 (address = 0x05) [Default = 06h]

CTRL2 is shown in Figure 7-63 and described in Table 7-39.

Read/Write

Return to the Register Maps Table

Figure 7-63. CTRL2 Control Register

7	6	5	4	3	2	1	0
DIR	STEP	SPI_DIR	SPI_STEP	MICROSTEP_MODE [3:0]			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0110b			

Table 7-39. CTRL2 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	DIR	R/W	0b	Direction input. When SPI_DIR = 1, if DIR = 1, motor moves in the forward direction; and when DIR = 0, motor moves in the reverse direction.

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Table 7-39. CTRL2 Control Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6	STEP	R/W	0b	Step input. Logic '1' causes the indexer to advance one step, when SPI_STEP = 1. This bit is self-clearing, automatically becomes '0' after writing '1'.
5	SPI_DIR	R/W	0b	**0b = Outputs follow input DIR pin for direction of stepping** 1b = Outputs follow DIR bit in SPI register for direction of stepping
4	SPI_STEP	R/W	0b	**0b = Outputs follow input STEP pin for stepping** 1b = Outputs follow STEP bit in SPI register for stepping
3-0	MICROSTEP_MODE [3:0]	R/W	0110b	0000b = Full step (2-phase excitation) with 100% current 0001b = Full step (2-phase excitation) with 71% current 0010b = Non-circular 1/2 step 0011b = 1/2 step 0100b = 1/4 step 0101b = 1/8 step **0110b = 1/16 step** 0111b = 1/32 step 1000b = 1/64 step 1001b = 1/128 step 1010b = 1/256 step 1011b to 1111b = Reserved

7.6.2.3 CTRL3 (address = 0x06) [Default = 38h]

CTRL3 is shown in Figure 7-64 and described in Table 7-40.

Read/Write

Return to the Register Maps Table

Figure 7-64. CTRL3 Control Register

7	6	5	4	3	2	1	0
CLR_FLT	LOCK [2:0]			TOCP	OCP_MODE	OTSD_MODE	OTW_REP
R/W-0b	R/W-011b			R/W-1b	R/W-0b	R/W-0b	R/W-0b

Table 7-40. CTRL3 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	CLR_FLT	R/W	0b	Write '1' to this bit to clear all latched fault bits. This bit automatically resets to '0' after '1' is written.
6-4	LOCK [2:0]	R/W	011b	Write 110b to lock the settings by ignoring further register writes except to these bits and address 0x06h bit 7 (CLR_FLT). Writing any sequence other than 110b has no effect when unlocked. Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.
3	TOCP	R/W	1b	**1b = Overcurrent protection deglitch time is 2 µs** 0b = Overcurrent protection deglitch time is 1 µs
2	OCP_MODE	R/W	0b	**0b = Overcurrent condition causes a latched fault** 1b = Overcurrent condition fault recovery is auto-retry
1	OTSD_MODE	R/W	0b	**0b = Overtemperature condition causes a latched fault** 1b = Overtemperature condition fault recovery is auto-retry

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Table 7-40. CTRL3 Control Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
0	TW_REP	R/W	0b	**0b = Overtemperature or undertemperature warning is not reported on nFAULT** 1b = Overtemperature or undertemperature warning is reported on nFAULT

7.6.2.4 CTRL4 (address = 0x07) [Default = 49h]

CTRL4 control is shown in Figure 7-65 and described in Table 7-41.

Read/Write

Return to the Register Maps Table

Figure 7-65. CTRL4 Control Register

7	6	5	4	3	2	1	0
TBLANK_TIME[1:0]		STL_LRN	EN_STL	STL_REP	FRQ_CHG	STEP_FREQ_TOL[1:0]	
R/W-01b		R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-00b	

Table 7-41. CTRL4 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	TBLANK_TIME[1:0]	R/W	01b	Controls the current sense blanking time. 00b = 1.5 µs blanking time **01b = 2 µs blanking time** 10b = 2.5 µs blanking time 11b = 3 µs blanking time
5	STL_LRN	R/W	0b	Write '1' to enable automatic learning of stall detection threshold. This bit automatically returns to '0' when the stall learning process is complete.
4	EN_STL	R/W	0b	**0b = Stall detection is disabled** 1b = Stall detection is enabled
3	STL_REP	R/W	1b	0b = Stall detection is not reported on nFAULT **1b = Stall detection is reported on nFAULT**
2	FRQ_CHG	R/W	0b	**0b = STEP input is filtered as per the STEP_FRQ_TOL bits** 1b = STEP input is not filtered
1-0	STEP_FRQ_TOL[1:0]	R/W	01b	Programs the filter setting for the STEP input. 00b = 1% filtering **01b = 2% filtering** 10b = 4% filtering 11b = 6% filtering

7.6.2.5 CTRL5 (address = 0x08) [Default = 03h]

CTRL5 is shown in Figure 7-66 and described in Table 7-42.

Read/Write

Return to the Register Maps Table

Figure 7-66. CTRL5 Control Register

7	6	5	4	3	2	1	0
STALL_TH [7:0]							
R/W-00000011b							

Table 7-42. CTRL5 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	STALL_TH [7:0]	R/W	00000011b	Lower 8-bits of stall threshold. 000000000000b = 0 count **000000000011b = 3 counts** XXXXXXXXXXXXb = 1 to 4094 counts 111111111111b = 4095 counts

7.6.2.6 CTRL6 (address = 0x09) [Default = 20h]

CTRL6 is shown in Figure 7-67 and described in Table 7-43.

Read/Write

Return to the Register Maps Table

Figure 7-67. CTRL6 Control Register

7	6	5	4	3	2	1	0
RC_RIPPLE[1:0]		DIS_SSC	TRQ_SCALE	STALL_TH[11:8]			
R/W-00b		R/W-1b	R/W-0b	R/W-0000b			

Table 7-43. CTRL6 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RC_RIPPLE[1:0]	R/W	00b	Controls the current ripple in smart tune ripple control decay mode. **00b = 1% ripple** 01b = 2% ripple 10b = 4% ripple 11b = 6% ripple
5	DIS_SSC	R/W	1b	0b = spread-spectrum enabled **1b = spread-spectrum disabled**
4	TRQ_SCALE	R/W	0b	**0b = No torque count scaling is applied** 1b = Torque count is scaled up by a factor of 8
3-0	STALL_TH[11:8]	R/W	0000b	4 MSB bits of stall threshold.

7.6.2.7 CTRL7 (address = 0x0A) [Default = FFh]

CTRL7 is shown in Figure 7-68 and described in Table 7-44.

Read-only

Return to the Register Maps Table

Figure 7-68. CTRL7 Control Register

7	6	5	4	3	2	1	0
TRQ_COUNT[7:0]							
R-11111111b							

Table 7-44. CTRL7 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	TRQ_COUNT[7:0]	R	11111111b	8 LSB bits of TRQ_COUNT. 000000000000b = 0 count XXXXXXXXXXXXb = 1 to 4094 counts **111111111111b = 4095 counts**

7.6.2.8 CTRL8 (address = 0x0B) [Default = 0Fh]

CTRL8 is shown in Figure 7-69 and described in Table 7-45.

Read-only

Return to the Register Maps Table

Figure 7-69. CTRL8 Control Register

7	6	5	4	3	2	1	0
RSVD				TRQ_COUNT[11:8]			
R-0000b				R-1111b			

Table 7-45. CTRL8 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	RSVD	R	0000b	Reserved.
3-0	TRQ_COUNT[11:8]	R	1111b	4 MSB bits of TRQ_COUNT.

7.6.2.9 CTRL9 (address = 0x0C) [Default = 10h]

CTRL9 is shown in Figure 7-70 and described in Table 7-46.

Read/Write

Return to the Register Maps Table

Figure 7-70. CTRL9 Control Register

7	6	5	4	3	2	1	0
EN_OL	OL_MODE	OL_T[1:0]		STEP_EDGE	RES_AUTO[1:0]		EN_AUTO
R/W-0b	R/W-0b	R/W-01b		R/W-0b	R/W-00b		R/W-0b

Table 7-46. CTRL9 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	EN_OL	R/W	0b	Write '1' to enable open load detection. When this bit is '0', open load detection is disabled.
6	OL_MODE	R/W	0b	**0b = nFAULT is released after latched OL fault is cleared using CLR_FLT bit or nSLEEP reset pulse** 1b = nFAULT is released immediately after OL fault condition is removed
5-4	OL_T[1:0]	R/W	01b	Controls the open load fault detection time. 00b = 30 ms (max) **01b = 60 ms** (max) 10b = 120 ms (max) 11b = Reserved
3	STEP_EDGE	R/W	0b	**0b = Active edge for STEP input is only rising edge** 1b = Active edge for STEP input is both rising and falling edges
2-1	RES_AUTO[1:0]	R/W	00b	Controls the microstepping resolution in automatic microstepping mode. **00b = 1/256** 01b = 1/128 10b = 1/64 11b = 1/32
0	EN_AUTO	R/W	0b	**0b = Automatic microstepping disabled** 1b = Automatic microstepping enabled

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7.6.2.10 CTRL10 (address = 0x0D) [Default = 80h]

CTRL10 control is shown in Figure 7-71 and described in Table 7-47.

Read/Write

Return to the Register Maps Table

Figure 7-71. CTRL10 Control Register

7	6	5	4	3	2	1	0
ISTSL[7:0]							
R/W-10000000b							

Table 7-47. CTRL10 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ISTSL[7:0]	R/W	10000000b	Determines the holding current. 11111111b = 256/256 x 100% 11111110b = 255/256 x 100% 11111101b = 254/256 x 100% 11111100b = 253/256 x 100% ..... 00000000b = 1/256 x 100%

7.6.2.11 CTRL11 (address = 0x0E) [Default = FFh]

CTRL11 control is shown in Figure 7-72 and described in Table 7-48.

Read/Write

Return to the Register Maps Table

Figure 7-72. CTRL11 Control Register

7	6	5	4	3	2	1	0
TRQ_DAC[7:0]							
R/W-11111111b							

Table 7-48. CTRL11 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	TRQ_DAC[7:0]	R/W	11111111b	Determines the run current. **11111111b = 256/256 x 100%** 11111110b = 255/256 x 100% 11111101b = 254/256 x 100% 11111100b = 253/256 x 100% ..... 00000000b = 1/256 x 100%

7.6.2.12 CTRL12 (address = 0x0F) [Default = 20h]

CTRL12 is shown in Figure 7-73 and described in Table 7-49.

Read/Write

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Figure 7-73. CTRL12 Control Register

7	6	5	4	3	2	1	0
EN_STSL	TSTSL_FALL[3:0]				RSVD		

Figure 7-73. CTRL12 Control Register (continued)

R/W-0b	R/W-0100b	R/W-000b

Table 7-49. CTRL12 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	EN_STSL	R/W	0b	**0b = Standstill power saving mode disabled** 1b = Standstill power saving mode enabled
6-3	TSTSL_FALL[3:0]	R/W	0100b	Controls the time it takes the current to reduce from TRQ_DAC to ISTSL after TSTSL_DLY time has elapsed 0000b: fall time = 0 0001b: fall time for each current step = 16 ms ..... **0100b: fall time for each current step = 64 ms** ..... 1111b: fall time for each current step = 240 ms
2-0	RSVD	R/W	000b	Reserved

Note

TSTSL_FALL in production samples will be 1/16 th of their value in the pre-production samples. For example, TSTSL_FALL = 0001b will mean fall time for each current step will be 1 ms.

7.6.2.13 CTRL13 (address = 0x10) [Default = 10h]

CTRL13 is shown in Figure 7-74 and described in Table 7-50.

Read/Write

Return to the Register Maps Table

Figure 7-74. CTRL13 Control Register

7	6	5	4	3	2	1	0
TSTSL_DLY[5:0]						RSVD	
R/W-000100b						R/W-00b	

Table 7-50. CTRL13 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-2	TSTSL_DLY[5:0]	R/W	000100b	Controls the delay between last STEP pulse and activation of standstill power saving mode. 000000b: Reserved 000001b: Delay = 1 x 16 ms = 16 ms ..... **000100b: Delay = 4 x 16 ms = 64 ms** ..... 111111b: Delay = 63 x 16 ms = 1.008 s
1-0	RSVD	R/W	00b	Reserved

Note

- Do not set TSTSL_DLY to 000000b.
- The VREF_INT_EN bit is located in ATQ_CTRL18 register bit 5 in pre-production samples. For production samples, the VREF_INT_EN bit will be located in CTRL13 register bit 1.

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7.6.2.14 CTRL14 (address = 0x3C) [Default = 00h]

CTRL14 is shown in Figure 7-75 and described in Table 7-51.

Read/Write

Return to the Register Maps Table

Figure 7-75. CTRL14 Control Register

7	6	5	4	3	2	1	0
RSVD							
R/W-00000000b							

Table 7-51. CTRL14 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	RSVD	R/W	00000000b	Reserved

Note

The production samples will feature VM_ADC bits located in CTRL14 register. These bits will output the value of the supply voltage, monitored by an internal ADC.

For the pre-production samples, the CTRL14 will be reserved.

7.6.3 Indexer Registers

The indexer registers provide signed current values for coils A and B, and the position in the microstep table for the current in coil A. Indexer registers are read only.

Table 7-52 lists the memory-mapped registers for the indexer registers. All register offset addresses not listed in Table 7-52 should be considered as reserved locations and the register contents should not be modified.

Table 7-52. Indexer Registers Summary Table

Address	Register Name	Section
0x11	INDEX1	Go
0x12	INDEX2	Go
0x13	INDEX3	Go
0x14	INDEX4	Go
0x15	INDEX5	Go

7.6.3.1 INDEX1 (address = 0x11) [Default = 80h]

INDEX1 is shown in Figure 7-76 and described in Table 7-53.

Read only

Return to the Register Maps Table

Figure 7-76. INDEX1 Register

7	6	5	4	3	2	1	0
CUR_A[7:0]							
R-10000000b							

Table 7-53. INDEX1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUR_A[7:0]	R	10000000b	Indicates the current of motor coil A for the position indicated by the INDEX_POS bits.

7.6.3.2 INDEX2 (address = 0x12) [Default = 80h]

INDEX2 is shown in Figure 7-77 and described in Table 7-54.

Read only

Return to the Register Maps Table

Figure 7-77. INDEX2 Register

7	6	5	4	3	2	1	0
CUR_A_SIGN	RSVD						
R-1b	R-0000000b						

Table 7-54. INDEX2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	CUR_A_SIGN	R	1b	Outputs the sign of coil A current for the position indicated by the INDEX_POS bits. **1b = Coil A current is positive** 0b = Coil A current is negative
6-0	RSVD	R	0000000b	Reserved

7.6.3.3 INDEX3 (address = 0x13) [Default = 80h]

INDEX3 is shown in Figure 7-78 and described in Table 7-55.

Read only

Return to the Register Maps Table

Figure 7-78. INDEX3 Register

7	6	5	4	3	2	1	0
CUR_B[7:0]							
R-10000000b							

Table 7-55. INDEX3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUR_B[7:0]	R	10000000b	Indicates the current of motor coil B for the position indicated by the INDEX_POS bits.

7.6.3.4 INDEX4 (address = 0x14) [Default = 80h]

INDEX4 is shown in Figure 7-79 and described in Table 7-56.

Read only

Return to the Register Maps Table

Figure 7-79. INDEX4 Register

7	6	5	4	3	2	1	0
CUR_B_SIGN	RSVD					INDEX_POS[9:8]	
R-1b	R-00000b					R-00b	

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Table 7-56. INDEX4 Register Field Descriptions

Bit	Field	Type	Default	Description
7	CUR_B_SIGN	R	1b	Outputs the sign of coil B current for the position indicated by the INDEX_POS bits. **1b = Coil B current is positive** 0b = Coil B current is negative
6-2	RSVD	R	00000b	Reserved
1-0	INDEX_POS[9:8]	R	00b	Upper two MSBs of the indexer position

7.6.3.5 INDEX5 (address = 0x15) [Default = 80h]

INDEX5 is shown in Figure 7-80 and described in Table 7-57.

Read only

Return to the Register Maps Table

Figure 7-80. INDEX5 Register

7	6	5	4	3	2	1	0
INDEX_POS[7:0]							
R-10000000b							

Table 7-57. INDEX5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	INDEX_POS[7:0]	R	10000000b	Outputs the lower 8 bits of the indexer position

Note

In production samples, the INDEX_POS bits will output the actual coil A current -> sin (90° x CUR_A / 255).

7.6.4 Custom Microstepping Registers

The custom microstep registers store the current values corresponding to the first quadrant of coil A current. Custom microstep registers are read and write capable.

Table 7-58 lists the memory-mapped registers for the custom microstep registers. All register offset addresses not listed in Table 7-58 should be considered as reserved locations and the register contents should not be modified.

Table 7-58. Custom microstep Registers Summary Table

Address	Register Name	Section
0x16	CUSTOM_CTRL1	Go
0x17	CUSTOM_CTRL2	Go
0x18	CUSTOM_CTRL3	Go
0x19	CUSTOM_CTRL4	Go
0x1A	CUSTOM_CTRL5	Go
0x1B	CUSTOM_CTRL6	Go
0x1C	CUSTOM_CTRL7	Go
0x1D	CUSTOM_CTRL8	Go
0x1E	CUSTOM_CTRL9	Go

7.6.4.1 CUSTOM_CTRL1 (address = 0x16) [Default = 00h]

CUSTOM_CTRL1 is shown in Figure 7-81 and described in Table 7-59.

Read/Write

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Figure 7-81. CUSTOM_CTRL1 Register

7	6	5	4	3	2	1	0
RSVD							EN_CUSTOM
R/W-0000000b							R/W-0b

Table 7-59. CUSTOM_CTRL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-1	RSVD	R/W	0000000b	Reserved
0	EN_CUSTOM	R/W	0b	**0b = Custom microstepping table is disabled** 1b = Custom microstepping table is enabled

7.6.4.2 CUSTOM_CTRL2 (address = 0x17) [Default = 00h]

CUSTOM_CTRL2 is shown in Figure 7-82 and described in Table 7-60.

Read/Write

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Figure 7-82. CUSTOM_CTRL2 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT1[7:0]							
R/W-00000000b							

Table 7-60. CUSTOM_CTRL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT1[7:0]	R/W	00000000b	Current value for position 1 in first quadrant

7.6.4.3 CUSTOM_CTRL3 (address = 0x18) [Default = 00h]

CUSTOM_CTRL3 is shown in Figure 7-83 and described in Table 7-61.

Read/Write

Return to the Register Maps Table

Figure 7-83. CUSTOM_CTRL3 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT2[7:0]							
R/W-00000000b							

Table 7-61. CUSTOM_CTRL3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT2[7:0]	R/W	00000000b	Current value for position 2 in first quadrant

7.6.4.4 CUSTOM_CTRL4 (address = 0x19) [Default = 00h]

CUSTOM_CTRL4 is shown in Figure 7-84 and described in Table 7-62.

Read/Write

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Figure 7-84. CUSTOM_CTRL4 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT3[7:0]							
R/W-00000000b							

Table 7-62. CUSTOM_CTRL4 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT3[7:0]	R/W	00000000b	Current value for position 3 in first quadrant

7.6.4.5 CUSTOM_CTRL5 (address = 0x1A) [Default = 00h]

CUSTOM_CTRL5 is shown in Figure 7-85 and described in Table 7-63.

Read/Write

Return to the Register Maps Table

Figure 7-85. CUSTOM_CTRL5 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT4[7:0]							
R/W-00000000b							

Table 7-63. CUSTOM_CTRL5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT4[7:0]	R/W	00000000b	Current value for position 4 in first quadrant

7.6.4.6 CUSTOM_CTRL6 (address = 0x1B) [Default = 00h]

CUSTOM_CTRL6 is shown in Figure 7-86 and described in Table 7-64.

Read/Write

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Figure 7-86. CUSTOM_CTRL6 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT5[7:0]							
R/W-00000000b							

Table 7-64. CUSTOM_CTRL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT5[7:0]	R/W	00000000b	Current value for position 5 in first quadrant

7.6.4.7 CUSTOM_CTRL7 (address = 0x1C) [Default = 00h]

CUSTOM_CTRL7 is shown in Figure 7-87 and described in Table 7-65.

Read/Write

Return to the Register Maps Table

Figure 7-87. CUSTOM_CTRL7 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT6[7:0]							
R/W-00000000b							

Table 7-65. CUSTOM_CTRL7 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT6[7:0]	R/W	00000000b	Current value for position 6 in first quadrant

7.6.4.8 CUSTOM_CTRL8 (address = 0x1D) [Default = 00h]

CUSTOM_CTRL8 is shown in Figure 7-88 and described in Table 7-66.

Read/Write

Return to the Register Maps Table

Figure 7-88. CUSTOM_CTRL8 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT7[7:0]							
R/W-00000000b							

Table 7-66. CUSTOM_CTRL8 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT7[7:0]	R/W	00000000b	Current value for position 7 in first quadrant

7.6.4.9 CUSTOM_CTRL9 (address = 0x1E) [Default = 00h]

CUSTOM_CTRL9 is shown in Figure 7-89 and described in Table 7-67.

Read/Write

Return to the Register Maps Table

Figure 7-89. CUSTOM_CTRL9 Register

7	6	5	4	3	2	1	0
CUSTOM_CURRENT8[7:0]							
R/W-00000000b							

Table 7-67. CUSTOM_CTRL9 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	CUSTOM_CURRENT8[7:0]	R/W	00000000b	Current value for position 8 in first quadrant

7.6.5 Auto torque Registers

The auto torque registers control the auto torque feature. Auto torque registers are read and write capable.

Table 7-68 lists the memory-mapped registers for the auto torque registers. All register offset addresses not listed in Table 7-68 should be considered as reserved locations and the register contents should not be modified.

Table 7-68. Auto torque Registers Summary Table

Address	Register Name	Section
0x1F	ATQ_CTRL1	Go
0x20	ATQ_CTRL2	Go
0x21	ATQ_CTRL3	Go
0x22	ATQ_CTRL4	Go
0x23	ATQ_CTRL5	Go
0x24	ATQ_CTRL6	Go
0x25	ATQ_CTRL7	Go

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Table 7-68. Auto torque Registers Summary Table (continued)

Address	Register Name	Section
0x26	ATQ_CTRL8	Go
0x27	ATQ_CTRL9	Go
0x28	ATQ_CTRL10	Go
0x29	ATQ_CTRL11	Go
0x2A	ATQ_CTRL12	Go
0x2B	ATQ_CTRL13	Go
0x2C	ATQ_CTRL14	Go
0x2D	ATQ_CTRL15	Go
0x2E	ATQ_CTRL16	Go
0x2F	ATQ_CTRL17	Go
0x30	ATQ_CTRL18	Go

7.6.5.1 ATQ_CTRL1 (address = 0x1F) [Default = 00h]

ATQ_CTRL1 is shown in Figure 7-90 and described in Table 7-69.

Read ONLY

Return to the Register Maps Table

Figure 7-90. ATQ_CTRL1 Register

7	6	5	4	3	2	1	0
ATQ_CNT[7:0]							
R-00000000b							

Table 7-69. ATQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_CNT[7:0]	R	00000000b	Read-only. Indicates the 8 LSB bits of the ATQ_CNT output. ATQ_CNT is proportional to the mechanical load torque.

7.6.5.2 ATQ_CTRL2 (address = 0x20) [Default = 00h]

ATQ_CTRL2 is shown in Figure 7-91 and described in Table 7-70.

Read/Write

Return to the Register Maps Table

Figure 7-91. ATQ_CTRL2 Register

7	6	5	4	3	2	1	0
ATQ_CNT[10:8]			RSVD		ATQ_LRN_CONST1[10:8]		
R/W-000b			R/W-00b		R/W-000b		

Table 7-70. ATQ_CTRL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	ATQ_CNT[10:8]	R/W	000b	Indicates the 3 MSB bits of the ATQ_CNT output
4-3	RSVD	R/W	00b	Reserved
2-0	ATQ_LRN_CONST1[10:8]	R/W	000b	Indicates the 3 MSB bits of the ATQ_LRN parameter at the initial learning current level.

7.6.5.3 ATQ_CTRL3 (address = 0x21) [Default = 00h]

ATQ_CTRL3 is shown in Figure 7-92 and described in Table 7-71.

Read/Write

Return to the Register Maps Table

Figure 7-92. ATQ_CTRL3 Register

7	6	5	4	3	2	1	0
ATQ_LRN_CONST1[7:0]							
R/W-00000000b							

Table 7-71. ATQ_CTRL3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_LRN_CONST1[7:0]	R/W	00000000b	8 LSB bits of the ATQ_LRN parameter at the initial learning current level.

7.6.5.4 ATQ_CTRL4 (address = 0x22) [Default = 20h]

ATQ_CTRL4 is shown in Figure 7-93 and described in Table 7-72.

Read/Write

Return to the Register Maps Table

Figure 7-93. ATQ_CTRL4 Register

7	6	5	4	3	2	1	0
ATQ_LRN_MIN_CURRENT[4:0]					ATQ_LRN_CONST2[10:8]		
R/W-00100b					R/W-000b		

Table 7-72. ATQ_CTRL4 Register Field Descriptions

Bit	Field	Type	Default	Description
7-3	ATQ_LRN_MIN_CURRENT[4:0]	R/W	00100b	Represents the initial current level for auto torque learning. Initial learning current = ATQ_LRN_MIN_CURRENT * 8
2-0	ATQ_LRN_CONST2[10:8]	R/W	000b	3 MSB bits of the ATQ_LRN parameter at the final learning current level.

7.6.5.5 ATQ_CTRL5 (address = 0x23) [Default = 00h]

ATQ_CTRL5 is shown in Figure 7-94 and described in Table 7-73.

Read/Write

Return to the Register Maps Table

Figure 7-94. ATQ_CTRL5 Register

7	6	5	4	3	2	1	0
ATQ_LRN_CONST2[7:0]							
R/W-00000000b							

Table 7-73. ATQ_CTRL5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_LRN_CONST2[7:0]	R/W	00000000b	8 LSB bits of the ATQ_LRN parameter at the final learning current level.

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7.6.5.6 ATQ_CTRL6 (address = 0x24) [Default = 00h]

ATQ_CTRL6 is shown in Figure 7-95 and described in Table 7-74.

Read/Write

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Figure 7-95. ATQ_CTRL6 Register

7	6	5	4	3	2	1	0
ATQ_UL[7:0]							
R/W-00000000b							

Table 7-74. ATQ_CTRL6 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_UL[7:0]	R/W	00000000b	Programs the upper limit of the auto torque hysterestic band. Upper band of desired operating region of ATQ_CNT.

7.6.5.7 ATQ_CTRL7 (address = 0x25) [Default = 00h]

ATQ_CTRL7 is shown in Figure 7-96 and described in Table 7-75.

Read/Write

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Figure 7-96. ATQ_CTRL7 Register

7	6	5	4	3	2	1	0
ATQ_LL[7:0]							
R/W-00000000b							

Table 7-75. ATQ_CTRL7 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_LL[7:0]	R/W	00000000b	Programs the lower limit of the auto torque hysterestic band. Lower Band of desired operating region of ATQ_CNT.

7.6.5.8 ATQ_CTRL8 (address = 0x26) [Default = 00h]

ATQ_CTRL8 is shown in Figure 7-97 and described in Table 7-76.

Read/Write

Return to the Register Maps Table

Figure 7-97. ATQ_CTRL8 Register

7	6	5	4	3	2	1	0
KP[7:0]							
R/W-00000000b							

Table 7-76. ATQ_CTRL8 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	KP[7:0]	R/W	00000000b	Proportional constant for tuning the auto torque control loop.

7.6.5.9 ATQ_CTRL9 (address = 0x27) [Default = 00h]

ATQ_CTRL9 is shown in Figure 7-98 and described in Table 7-77.

Read/Write

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Figure 7-98. ATQ_CTRL9 Register

7	6	5	4	3	2	1	0
KI[3:0]				KD[3:0]			
R/W-0000b				R/W-0000b			

Table 7-77. ATQ_CTRL9 Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	KI[3:0]	R/W	0000b	Integral constant for tuning the auto torque control loop.
3-0	KD[3:0]	R/W	0000b	Differential constant for tuning the auto torque control loop.

7.6.5.10 ATQ_CTRL10 (address = 0x28) [Default = 08h]

ATQ_CTRL10 is shown in Figure 7-99 and described in Table 7-78.

Read/Write

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Figure 7-99. ATQ_CTRL10 Register

7	6	5	4	3	2	1	0
ATQ_EN	LRN_START	ATQ_FRZ[2:0]			ATQ_AVG[2:0]		
R/W-0b	R/W-0b	R/W-001b			R/W-000b		

Table 7-78. ATQ_CTRL10 Register Field Descriptions

Bit	Field	Type	Default	Description
7	ATQ_EN	R/W	0b	**0 = auto torque is disabled** 1 = auto torque is enabled
6	LRN_START	R/W	0b	Writing '1' to this bit enables the auto torque learning process. After learning is completed, the bit automatically goes to '0'.
5-3	ATQ_FRZ[2:0]	R/W	001b	After any output current update, delay in number of half cycles for which current update is frozen.
2-0	ATQ_AVG[2:0]	R/W	000b	Number of half cycles used for averaging in ATQ_COUNT calculation.

7.6.5.11 ATQ_CTRL11 (address = 0x29) [Default = 0Ah]

ATQ_CTRL11 is shown in Figure 7-100 and described in Table 7-79.

Read/Write

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Figure 7-100. ATQ_CTRL11 Register

7	6	5	4	3	2	1	0
ATQ_TRQ_MIN[7:0]							
R/W-00001010b							

Table 7-79. ATQ_CTRL11 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_TRQ_MIN[7:0]	R/W	00001010b	Auto torque minimum current limit.

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7.6.5.12 ATQ_CTRL12 (address = 0x2A) [Default = FFh]

ATQ_CTRL12 is shown in Figure 7-101 and described in Table 7-80.

Read/Write

Return to the Register Maps Table

Figure 7-101. ATQ_CTRL12 Register

7	6	5	4	3	2	1	0
ATQ_TRQ_MAX[7:0]							
R/W-11111111b							

Table 7-80. ATQ_CTRL12 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_TRQ_MAX[7:0]	R/W	11111111b	Auto torque maximum current limit.

7.6.5.13 ATQ_CTRL13 (address = 0x2B) [Default = 05h]

ATQ_CTRL13 is described below.

Read/Write

Return to the Register Maps Table

Figure 7-102. ATQ_CTRL13 Register

7	6	5	4	3	2	1	0
ATQ_D_THR[7:0]							
R/W-00000101b							

Table 7-81. ATQ_CTRL13 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_D_THR	R/W	00000101b	Error limit above which KD is used in PID equations.

7.6.5.14 ATQ_CTRL14 (address = 0x2C) [Default = 0Fh]

ATQ_CTRL14 is described below.

Read/Write

Return to the Register Maps Table

Figure 7-103. ATQ_CTRL14 Register

7	6	5	4	3	2	1	0
ATQ_MAX_INTEGRAL							
R/W-00001111b							

Table 7-82. ATQ_CTRL14 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_MAX_INTEGRAL	R/W	00001111b	Indicates the saturation point of error integration.

7.6.5.15 ATQ_CTRL15 (address = 0x2D) [Default = 00h]

ATQ_CTRL15 is described below.

Read/Write

Return to the Register Maps Table

Figure 7-104. ATQ_CTRL15 Register

7	6	5	4	3	2	1	0
ATQ_ERROR_TRUNCATE[3:0]				ATQ_LRN_STEP[1:0]		ATQ_LRN_CYCLE_SELECT[1:0]	
R/W-0000b				R/W-00b		R/W-00b	

Table 7-83. ATQ_CTRL15 Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	ATQ_ERROR_TRUNCATE[3:0]	R/W	0000b	Number of LSB bits truncated from error before used in PID loop equations.
3-2	ATQ_LRN_STEP[1:0]	R/W	00b	Step increment in ATQ learn current.
1-0	ATQ_LRN_CYCLE_SELECT[1:0]	R/W	00b	Number of sine half cycles in one current level before which the learning routine lets the current jump to the next level.

7.6.5.16 ATQ_CTRL16 (address = 0x2E) [Default = FFh]

ATQ_CTRL16 is described below.

Read only

Return to the Register Maps Table

Figure 7-105. ATQ_CTRL16 Register

7	6	5	4	3	2	1	0
ATQ_TRQ_DAC[7:0]							
R-11111111b							

Table 7-84. ATQ_CTRL16 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	ATQ_TRQ_DAC[7:0]	R	11111111b	Read-only. Auto torque current level readout.

Note

When auto-torque is disabled, ATQ_TRQ_DAC reads the value programmed to ATQ_TRQ_MAX.

7.6.5.17 ATQ_CTRL17 (address = 0x2F) [Default = 00h]

ATQ_CTRL17 is described below.

Read/Write

Return to the Register Maps Table

Figure 7-106. ATQ_CTRL17 Register

7	6	5	4	3	2	1	0
RSVD							
R/W-00000000b							

Table 7-85. ATQ_CTRL17 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	RSVD	R/W	00000000b	Reserved.

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Note

The production samples will feature a VM_SCALE bit located in ATQ_CTRL17 bit 6. When enabled, this bit will modify the auto-torque learning routine parameters in the event of a supply voltage change. In pre-production samples, this bit will be reserved.

7.6.5.18 ATQ_CTRL18 (address = 0x30) [Default = 00h]

ATQ_CTRL18 is described below.

Read/Write

Return to the Register Maps Table

Figure 7-107. ATQ_CTRL18 Register

7	6	5	4	3	2	1	0
RSVD		VREF_INT_EN	RSVD				
R/W-00b		R/W-0b	R/W-00000b				

Table 7-86. ATQ_CTRL18 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RSVD	R/W	00b	Reserved.
5	VREF_INT_EN	R/W	0b	1b = Enables internal 3.3V reference voltage **0b = Device works with external reference voltage (VREF pin)**
4	RSVD	R/W	00000b	Reserved.

Note

The VREF_INT_EN bit is located in ATQ_CTRL18 register bit 5 in pre-production samples. For production samples, the VREF_INT_EN bit will be located in CTRL13 register bit 1.

7.6.6 Silent Step Registers

The silent step registers control the silent step decay mode. Silent step registers are read and write capable.

Table 7-87 lists the memory-mapped registers for the silent step registers. All register offset addresses not listed in Table 7-87 should be considered as reserved locations and the register contents should not be modified.

Table 7-87. Silent step Registers Summary Table

Address	Register Name	Section
0x31	SS_CTRL1	Go
0x32	SS_CTRL2	Go
0x33	SS_CTRL3	Go
0x34	SS_CTRL4	Go
0x35	SS_CTRL5	Go

7.6.6.1 SS_CTRL1 (address = 0x31) [Default = 00h]

SS_CTRL1 is shown in Figure 7-108 and described in Table 7-88.

Read/Write

Return to the Register Maps Table

Figure 7-108. SS_CTRL1 Register

7	6	5	4	3	2	1	0
RSVD				SS_PWM_FREQ[1:0]		RSVD	EN_SS
R/W-0000b				R/W-00b		R/W-0b	R/W-0b

Table 7-88. SS_CTRL1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	RSVD	R/W	0000b	Reserved
3-2	SS_PWM_FREQ[1:0]	R/W	00b	Silent step decay PWM frequency configuration **00b - 25KHz** 01b - 33KHz 10b - 42KHz 11b - 50KHz
1	RSVD	R/W	0b	Reserved
0	EN_SS	R/W	0b	**0b = silentstep decay mode is disabled** 1b = silentstep decay mode is enabled

7.6.6.2 SS_CTRL2 (address = 0x32) [Default = 00h]

SS_CTRL2 is shown in Figure 7-109 and described in Table 7-89.

Read/Write

Return to the Register Maps Table

Figure 7-109. SS_CTRL2 Register

7	6	5	4	3	2	1	0
RSVD	SS_KP[6:0]						
R/W - 0b	R/W-0000000b						

Table 7-89. SS_CTRL2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R/W	0b	Reserved.
6-0	SS_KP[6:0]	R/W	0000000b	Silent step decay mode proportional constant of the compensation loop. Range from 0 to 127.

7.6.6.3 SS_CTRL3 (address = 0x33) [Default = 00h]

SS_CTRL3 is shown in Figure 7-110 and described in Table 7-90.

Read/Write

Return to the Register Maps Table

Figure 7-110. SS_CTRL3 Register

7	6	5	4	3	2	1	0
RSVD	SS_KI[6:0]						
R/W-0b	R/W-0000000b						

Table 7-90. SS_CTRL3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R/W	0b	Reserved.

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Table 7-90. SS_CTRL3 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
6-0	SS_KI[6:0]	R/W	0000000b	Silent step decay mode integral constant of the compensation loop. Range from 0 to 255.

7.6.6.4 SS_CTRL4 (address = 0x34) [Default = 00h]

SS_CTRL4 is shown in Figure 7-111 and described in Table 7-91.

Read/Write

Return to the Register Maps Table

Figure 7-111. SS_CTRL4 Register

7	6	5	4	3	2	1	0
RSVD	SS_KI_DIV_SEL[2:0]			RSVD	SS_KP_DIV_SEL[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 7-91. SS_CTRL4 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R/W	0b	Reserved
6-4	SS_KI_DIV_SEL[2:0]	R/W	000b	Silent step decay mode KI divider Actual KI = SS_KI/SS_KI_DIV_SEL **000b - SS_KI/32** 001b - SS_KI/64 010b - SS_KI/128 011b - SS_KI/256 100b - SS_KI/512 101b - SS_KI/16 110b - SS_KI
3-1	RSVD	R/W	0b	Reserved
0	SS_KP_DIV_SEL[2:0]	R/W	000b	Silent step decay mode KP divider Actual KP = SS_KP/SS_KP_DIV_SEL **000b - SS_KP/32** 001b - SS_KP/64 010b - SS_KP/128 011b - SS_KP/256 100b - SS_KP/512 101b - SS_KP/16 110b - SS_KP

7.6.6.5 SS_CTRL5 (address = 0x35) [Default = FFh]

SS_CTRL5 is shown in Figure 7-112 and described in Table 7-92.

Read/Write

Return to the Register Maps Table

Figure 7-112. SS_CTRL5 Register

7	6	5	4	3	2	1	0
SS_THR[7:0]							
R/W-11111111b							

Table 7-92. SS_CTRL5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	SS_THR[7:0]	R/W	11111111b	Programs the frequency at which the device transitions from silent step decay mode to another decay mode programmed by the DECAY bits. This frequency corresponds to the frequency of the sinusoidal current waveform. 00000001b = 2 Hz 00000010b = 4 Hz . . **11111111b = 510 Hz**

Note

Do not set SS_THR to 00000000b.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DRV8462 is used in bipolar stepper control.

8.2 Typical Application

The following design procedure can be used to configure the DRV8462.

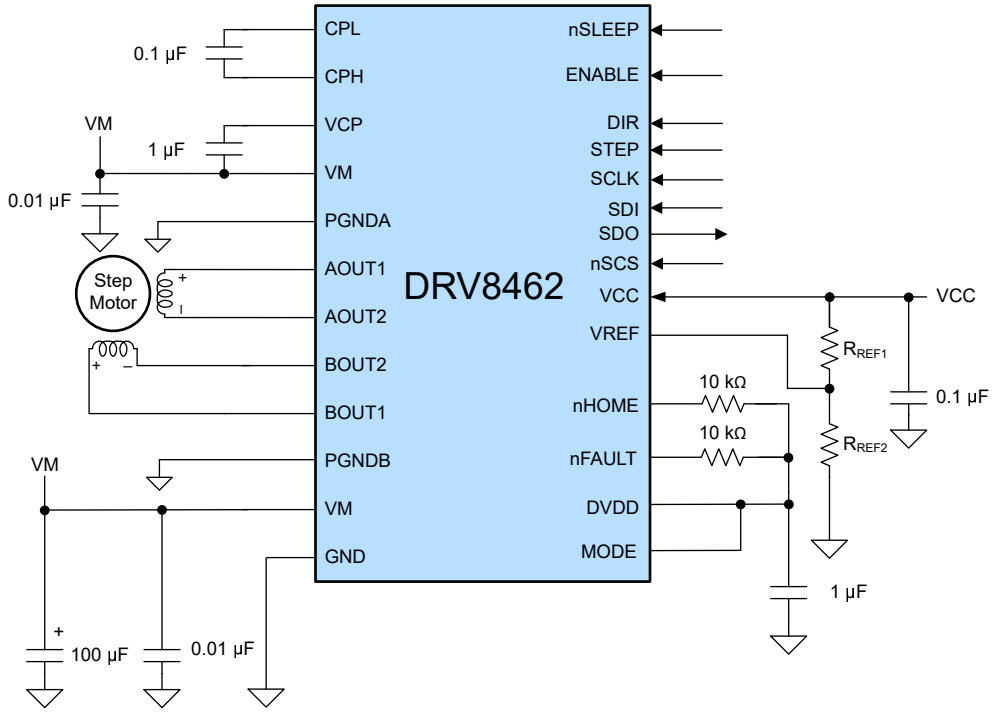

Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Table 8-1 lists the design input parameters for system design.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	0.5 Ω/phase
Motor winding inductance	L_L	0.4 mH/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	1/32 step
Target motor speed	v	50 rpm
Target full-scale current	I_{FS}	5 A

8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8462 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin. If the target motor speed is too high, the motor does not spin. Make sure that the motor can support the target speed. Use Equation 13 to calculate f_{step} for a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step})

$$f_{step}\ (\text{steps / s}) = \frac{\text{v (rpm)} \times 360\ (^\circ / \text{rot})}{\theta_{step}\ (^\circ / \text{step}) \times n_m\ (\text{steps / microstep}) \times 60\ (\text{s / min})} \tag{13}$$

The value of θ_{step} can be found in the stepper motor data sheet, or written on the motor. For example, the motor in this application is required to rotate at 1.8°/step for a target of 50 rpm at 1/32 microstep mode. Using Equation 13, f_{step} can be calculated as 5300 Hz.

The microstepping level is set by the M0 and M1 pins or the MICROSTEP_MODE bits and can be any of the settings listed in Table 7-5. Higher microstepping results in a smoother motor motion and less audible noise, but requires a higher f_{step} to achieve the same motor speed.

8.2.3 Thermal Application

This section presents the power dissipation calculation and junction temperature estimation of the device.

8.2.3.1 Power Dissipation

The total power dissipation constitutes of three main components - conduction loss (P_{COND}), switching loss (P_{SW}) and power loss due to quiescent current consumption (P_Q).

8.2.3.2 Conduction Loss

The current path for a motor connected in full-bridge is through the high-side FET of one half-bridge and low-side FET of the other half-bridge. The conduction loss (P_{COND}) depends on the motor rms current (I_{RMS}) and high-side ($R_{DS(ONH)}$) and low-side ($R_{DS(ONL)}$) on-state resistances as shown in Equation 14.

$$P_{COND} = 2 \text{ x } (I_{RMS})^2 \text{ x } (R_{DS(ONH)} + R_{DS(ONL)}) \tag{14}$$

The conduction loss for the typical application shown in Table 8-1 is calculated in Equation 15.

$$P_{COND} = 2 \text{ x } (I_{RMS})^2 \text{ x } (R_{DS(ONH)} + R_{DS(ONL)}) = 2 \text{ x } (5\text{-A} / \sqrt{2})^2 \text{ x } (0.1\text{-}\Omega) = 2.5\text{-W} \tag{15}$$

Note

This power calculation is highly dependent on the device temperature which significantly effects the high-side and low-side on-resistance of the FETs. For more accurate calculation, consider the dependency of on-resistance of FETs with device temperature.

8.2.3.3 Switching Loss

The power loss due to the PWM switching frequency depends on the output voltage rise/fall time (t_{RF}), supply voltage, motor RMS current and the PWM switching frequency. The switching losses in each H-bridge during rise-time and fall-time are calculated as shown in Equation 16 and Equation 17.

$$P_{SW\_RISE} = 0.5 \text{ x } V_{VM} \text{ x } I_{RMS} \text{ x } t_{RF} \text{ x } f_{PWM} \tag{16}$$

$$P_{SW\_FALL} = 0.5 \text{ x } V_{VM} \text{ x } I_{RMS} \text{ x } t_{RF} \text{ x } f_{PWM} \tag{17}$$

The DRV8462 features two values of output rise/fall time (t_{RF}) - 140 ns and 70 ns. The smaller rise/fall time obviously results in lesser switching loss. Assuming t_{RF} = 140 ns and 30-kHz PWM frequencyfor this exercise,

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and after substituting the values of various parameters, the switching losses in each H-bridge are calculated as shown below -

$$P_{SW\_RISE} = 0.5 \times 24\text{-V} \times (5\text{-A} / \sqrt{2}) \times (140\text{ ns}) \times 30\text{-kHz} = 0.178\text{-W} \quad (18)$$

$$P_{SW\_FALL} = 0.5 \times 24\text{-V} \times (5\text{-A} / \sqrt{2}) \times (100\text{ ns}) \times 30\text{-kHz} = 0.178\text{-W} \quad (19)$$

The total switching loss for the stepper motor driver (P_{SW}) is calculated as twice the sum of rise-time (P_{SW_RISE}) switching loss and fall-time (P_{SW_FALL}) switching loss as shown below -

$$P_{SW} = 2 \times (P_{SW\_RISE} + P_{SW\_FALL}) = 2 \times (0.178\text{-W} + 0.178\text{-W}) = 0.712\text{-W} \quad (20)$$

Note

The output rise/fall time (t_{RF}) is expected to change based on the supply-voltage, temperature and device to device variation.

The switching loss is directly proportional to the PWM switching frequency. The PWM frequency in an application depends on the supply voltage, inductance of the motor coil, back emf voltage and OFF time or the ripple current (for smart tune ripple control decay mode).

8.2.3.4 Power Dissipation Due to Quiescent Current

When the VCC pin is connected to an external voltage, the quiescent current is typically 5 mA. The power dissipation due to the quiescent current consumed by the power supply is calculated as shown below -

$$P_Q = V_{VM} \times I_{VM} \quad (21)$$

Substituting the values, quiescent power loss can be calculated as shown below -

$$P_Q = 24\text{-V} \times 5\text{-mA} = 0.12\text{-W} \quad (22)$$

Note

The quiescent power loss is calculated using the typical operating supply current (I_{VM}) which is dependent on supply-voltage, temperature and device to device variations.

8.2.3.5 Total Power Dissipation

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss as shown in Equation 23.

$$P_{TOT} = P_{COND} + P_{SW} + P_Q = 2.5\text{-W} + 0.712\text{-W} + 0.12\text{-W} = 3.332\text{-W} \quad (23)$$

8.2.3.6 Device Junction Temperature Estimation

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as -

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 21.6 °C/W for the DDW package.

Assuming 25°C ambient temperature, the junction temperature for the DDW package is calculated as shown below -

$$T_J = 25°C + (3.332\text{-W} \times 21.6\ °C/W) = 97\ °C \quad (24)$$

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As explained before, for more accurate calculation, consider the dependency of on-resistance of FETs with device junction temperature shown in the Typical Operating Characteristics section.

For example,

- At 97 °C junction temperature, the on-resistance will likely increase by a factor of 1.25 compared to the on-resistance at 25 °C.
- The initial estimate of conduction loss was 2.5 W.
- New estimate of conduction loss will therefore be 2.5 W x 1.25 = 3.125 W.
- New estimate of the total power loss will accordingly be 3.957 W.
- New estimate of junction temperature for the DDW package will be 110.5 °C.
- Further iterations are unlikely to increase the junction temperature estimate by significant amount.

When using the DDV package, if a heat sink with less than 4 °C/W thermal resistance is chosen, the junction to ambient thermal resistance can be lower than 5 °C/W. The initial estimate of the junction temperature with the DDV package in this application will therefore be -

$$T_J = 25°C + (3.332\text{-W} \times 5\ °C/W) = 41.7\ °C \quad (25)$$

As the DDV package results in low thermal resistance, it can deliver 10 A full-scale current.

9 Thermal Considerations

9.1 DDV Package

The DDV package is designed to interface directly to a heat sink using a thermal interface compound in between, (e.g., Ceramique from Arctic Silver, TIMTronics 413, etc.). The heat sink absorbs heat from the DRV8462 and transfers it to the air. With proper thermal management this process can reach equilibrium and heat can be continually transferred from the device. A concept digram of the heatsink on top of the DDV package is shown in Figure 9-1.

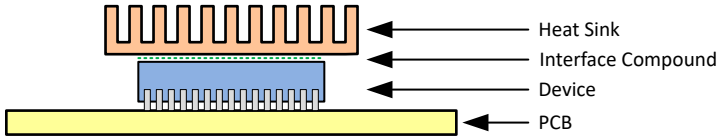

Figure 9-1. Heat sink on DDV Package

Care must be taken when mounting the heatsinks, ensuring good contact with thermal pads and not exceeding the mechanical stress capability of the parts to avoid breakage. The DDV package is capable of tolerating up to 90 Newton load. In production, it is recommended to apply less than 45 Newton load torque.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- $R_{\theta JC}$ of the DDV Package (thermal resistance from junction to exposed pad)
- Thermal resistance of the thermal interface material
- Thermal resistance of the heat sink

$R_{\theta JA} = R_{\theta JC}$ + thermal interface resistance + heat sink resistance

The thermal resistance of the thermal interface material can be determined from the area of the exposed metal package and manufacturer's value for the area thermal resistance (expressed in °Cmm^2/W). For example, a typical white thermal grease with a 0.0254 mm (0.001 inch) thick layer has 4.52 °Cmm^2/W thermal resistance. The DDV package has an exposed area of 28.7 mm^2. By dividing the area thermal resistance by the exposed metal area determines the thermal resistance for the interface material as 0.157°C/W.

Heat sink thermal resistance is predicted by the heat sink vendor, modeled using a continuous flow dynamics (CFD) model, or measured. The following are the various important parameters in selecting a heatsink.

1. Thermal resistance
2. Airflow
3. Volumetric resistance
4. Fin density
5. Fin spacing
6. Width
7. Length

The thermal resistance is one parameter that changes dynamically depending on the airflow available.

Airflow is typically measured in LFM (linear feet per minute) or CFM (cubic feet per minute). LFM is a measure of velocity, whereas CFM is a measure of volume. Typically, fan manufacturers use CFM because fans are rated according to the quantity of air it can move. Velocity is more meaningful for heat removal at the board level, which is why the derating curves provided by most power converter manufacturers use this.

Typically, airflow is either classified as natural or forced convection.

- Natural convection is a condition with no external induced flow and heat transfer depends on the air surrounding the heatsink. The effect of radiation heat transfer is very important in natural convection, as it can be responsible for approximately 25% of the total heat dissipation. Unless the component is facing a hotter surface nearby, it is imperative to have the heatsink surfaces painted to enhance radiation.
- Forced convection occurs when the flow of air is induced by mechanical means, usually a fan or blower.

Limited thermal budget and space make the choice of a particular type of heatsink very important. This is where the volume of the heatsink becomes relevant. The volume of a heatsink for a given flow condition can be obtained by using the following equation:

$Volume_{(heatsink)}$ = volumetric resistance (Cm^3 °C/W)/thermal resistance θ_{SA} (°C/W)

An approximate range of volumetric resistance is given in the following table:

Available Airflow (LFM)	Volumetric Resistance (Cm^3 °C/W)
NC	500 – 800
200	150 - 250
500	80 - 150
1000	50 - 80

The next important criterion for the performance of a heatsink is the width. It is linearly proportional to the performance of the heatsink in the direction perpendicular to the airflow. An increase in the width of a heatsink by a factor of two, three, or four increase the heat dissipation capability by a factor of two, three, or four. Similarly, the square root of the fin length used is approximately proportional to the performance of the heatsink in the direction parallel to the airflow. In case of an increase in the length of the heatsink by a factor of two, three, or four only increases the heat dissipation capability by a factor of 1.4, 1.7, or 2.

If the board has sufficient space, it is always beneficial to increase the width of a heatsink rather than the length of the heatsink. This is only the beginning of an iterative process before the correct and the actual heatsink design is achieved.

The heat sink must be supported mechanically at each end of the IC. This mounting ensures the correct pressure to provide good mechanical, thermal and electrical contact. The heat sink should be connected to GND or left floating.

9.2 DDW Package

Thermal pad of the DDW package is attached at bottom of device to improve the thermal capability of the device. The thermal pad has to be soldered with a very good coverage on PCB in order to deliver the power specified in the datasheet. Refer to the Layout Guidelines section for more details.

9.3 PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. (70 µm) copper on both top and bottom layer is recommended for improved thermal performance and better EMI margin (due to lower PCB trace inductance).

10 Power Supply Recommendations

The DRV8462 device is designed to operate from an input voltage supply (VM) from 4.5 V to 65 V. A 0.01-µF ceramic capacitor rated for VM must be placed close to the VM pins of DRV8462. In addition, a bulk capacitor must be included on VM.

10.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

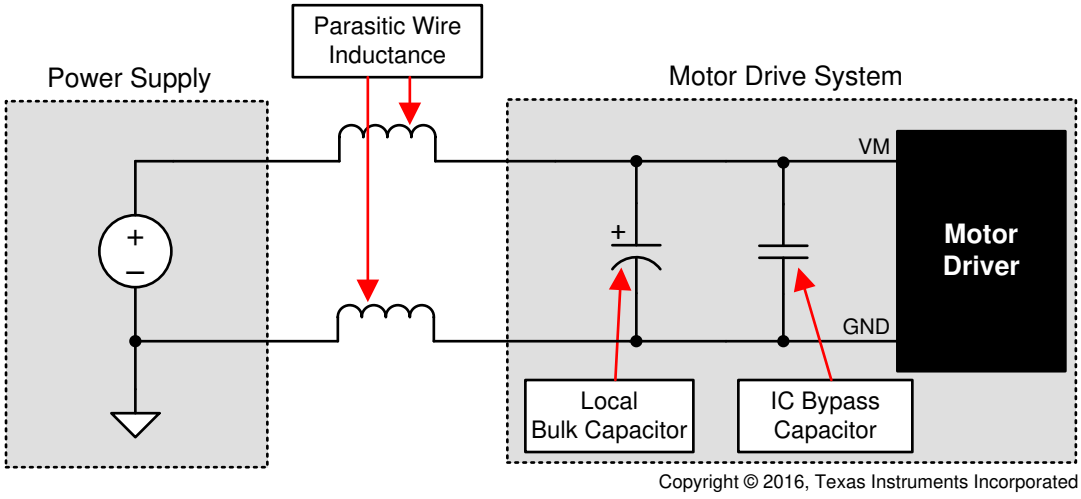

Figure 10-1. Example Setup of Motor Drive System With External Power Supply

10.2 Power Supplies

The DRV8462 needs only a single supply voltage connected to the VM pins.

- The VM pin provides the power supply to the H-Bridges.
- An internal voltage regulator provides a 5V supply (DVDD) for the digital and low-voltage analog circuitry. The DVDD pin is not recommended to be used as a voltage source for external circuitry.
- An external low-voltage supply can be connected to the VCC pin to power the internal circuitry. A 0.1-µF decoupling capacitor should be placed close to the VCC pin to provide a constant voltage during transient.
- Additionally, the high-side gate drive requires a higher voltage supply, which is generated by the built-in charge pump. The charg pump requires external capacitors.

11 Layout

11.1 Layout Guidelines

- The VM pins should be bypassed to PGND pins using low-ESR ceramic bypass capacitors with a recommended value of 0.01 µF rated for VM. The capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device PGND pins.
- The VM pins should be bypassed to PGND using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.
- A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.1 µF rated for VM is recommended. Place this component as close to the pins as possible.
- A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 1 µF rated for 16 V is recommended. Place this component as close to the pins as possible.
- Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 1 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.
- Bypass the VCC pin to ground with a low-ESR ceramic capacitor. A value of 0.1 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.
- In general, inductance between the power supply pins and decoupling capacitors must be avoided.
- The thermal PAD of the DDW package must be connected to system ground.
  - It is recommended to use a big unbroken single ground plane for the whole system / board. The ground plane can be made at bottom PCB layer.
  - In order to minimize the impedance and inductance, the traces from ground pins should be as short and wide as possible, before connecting to bottom layer ground plane through vias.
  - Multiple vias are suggested to reduce the impedance.
  - Try to clear the space around the device as much as possible especially at bottom PCB layer to improve the heat spreading.
  - Single or multiple internal ground planes connected to the thermal PAD will also help spreading the heat and reduce the thermal resistance.

11.2 Layout Example

Follow the layout example of the DRV8462 EVM. The design files can be downloaded from the DRV8462EVM product folder.

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12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Related Documentation

- Texas Instruments, *How to Reduce Audible Noise in Stepper Motors* application report
- Texas Instruments, *How to Improve Motion Smoothness and Accuracy* application report
- Texas Instruments, *How to Drive Unipolar Stepper Motors with DRV8xxx* application report
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *Motor Drives Layout Guide* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

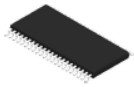
13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

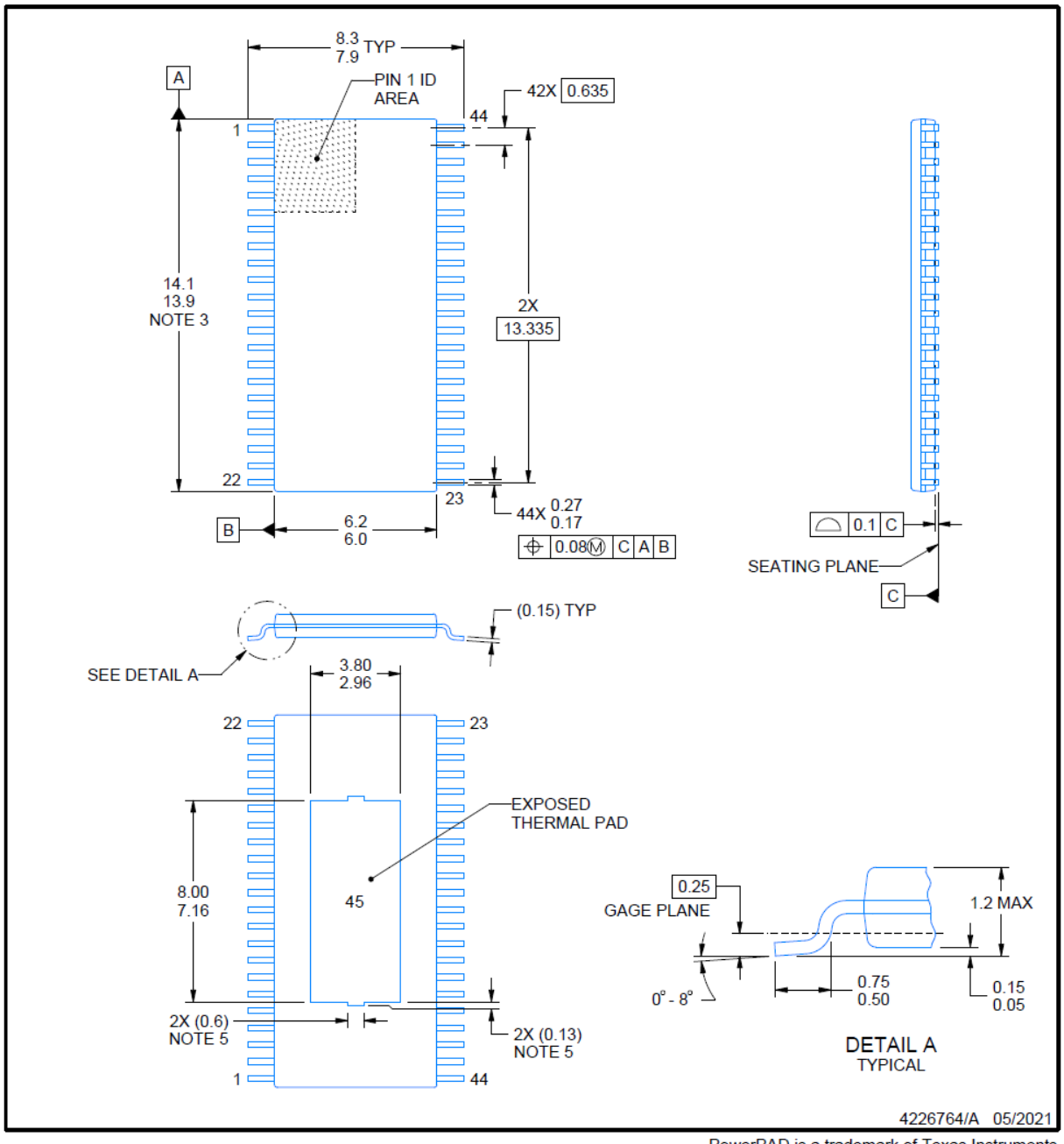
PACKAGE OUTLINE

DDW0044E



PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

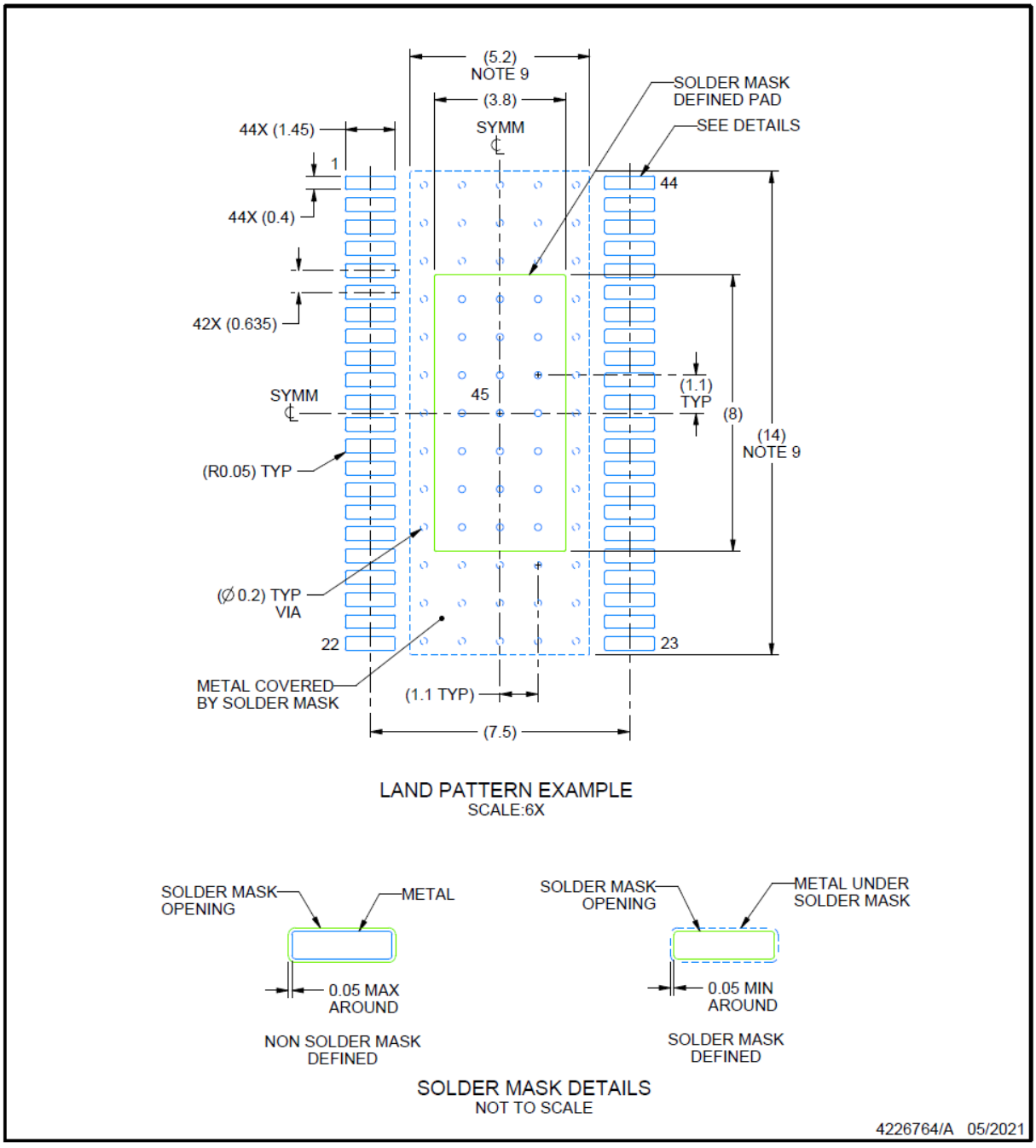
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

ADVANCE INFORMATION

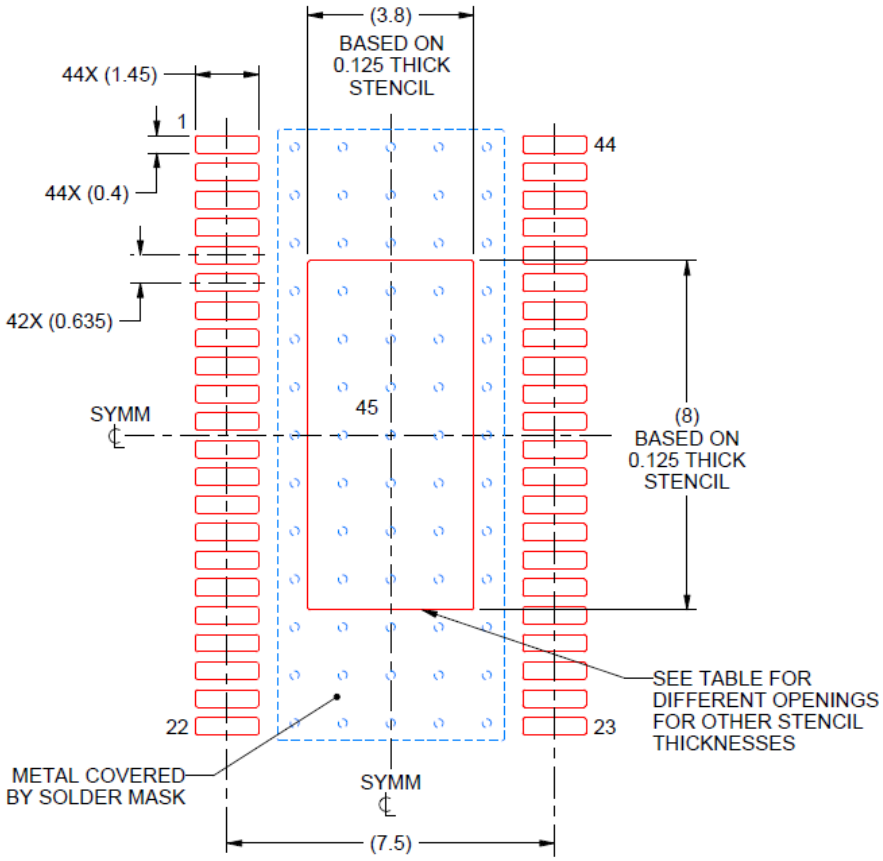
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
PAD 45:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.25 X 8.94
0.125	3.80 X 8.00 (SHOWN)
0.15	3.47 X 7.30
0.175	3.21 X 6.76

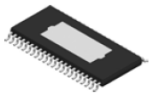
4226764/A 05/2021

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

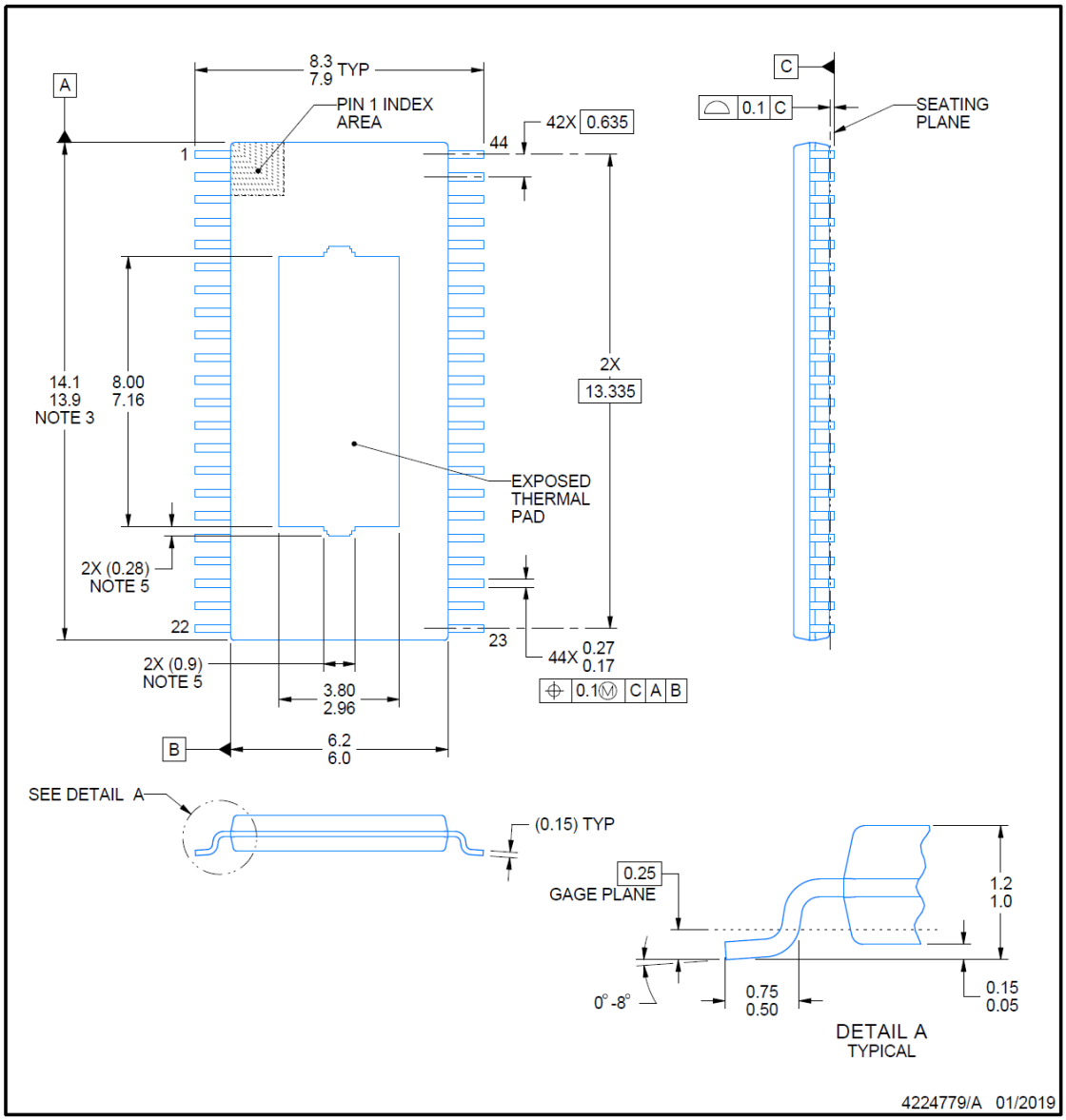
PACKAGE OUTLINE

DDV0044E



PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. The exposed thermal pad is designed to be attached to an external heatsink.
6. Features may differ or may not be present.

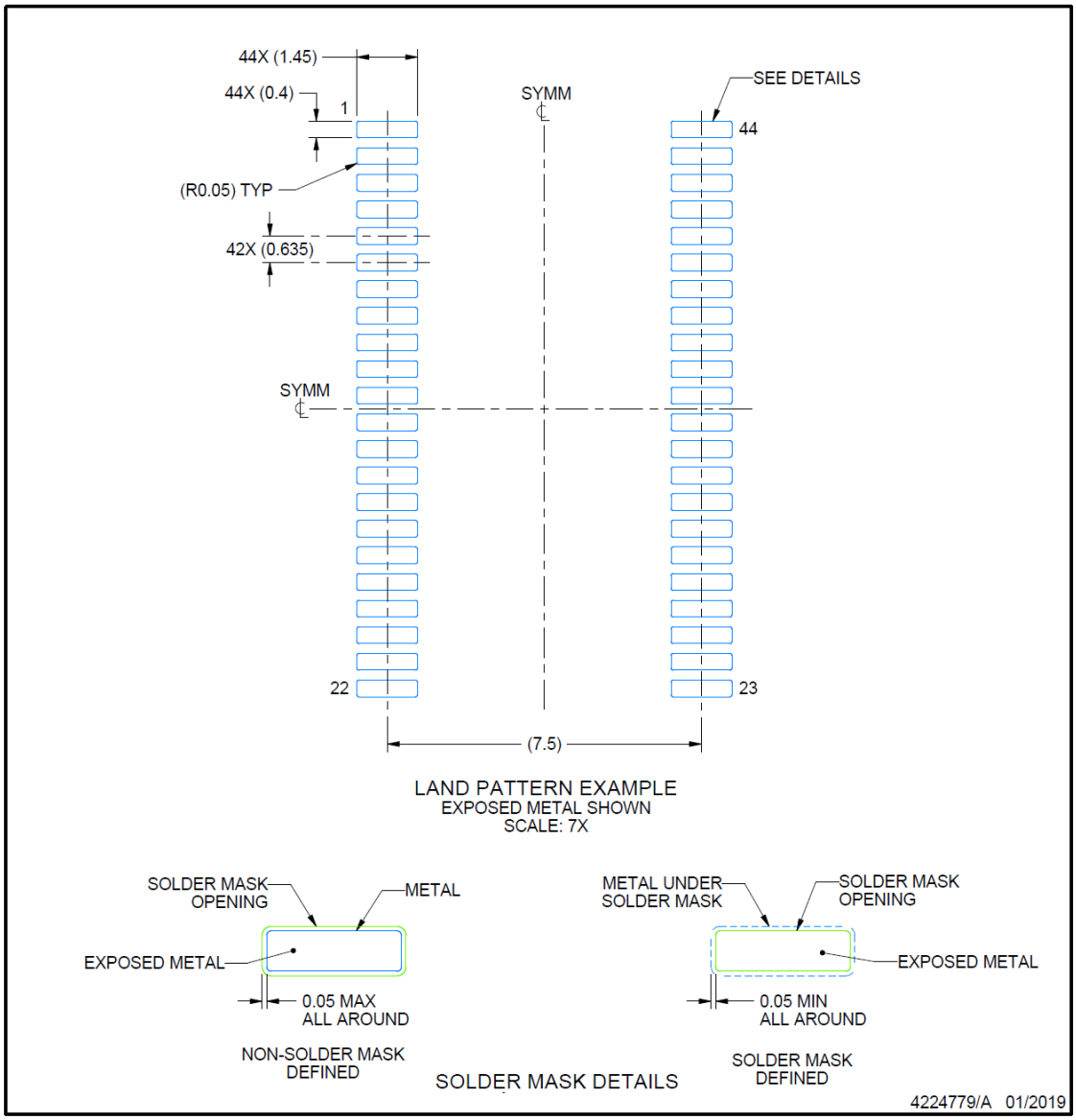
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DDV0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



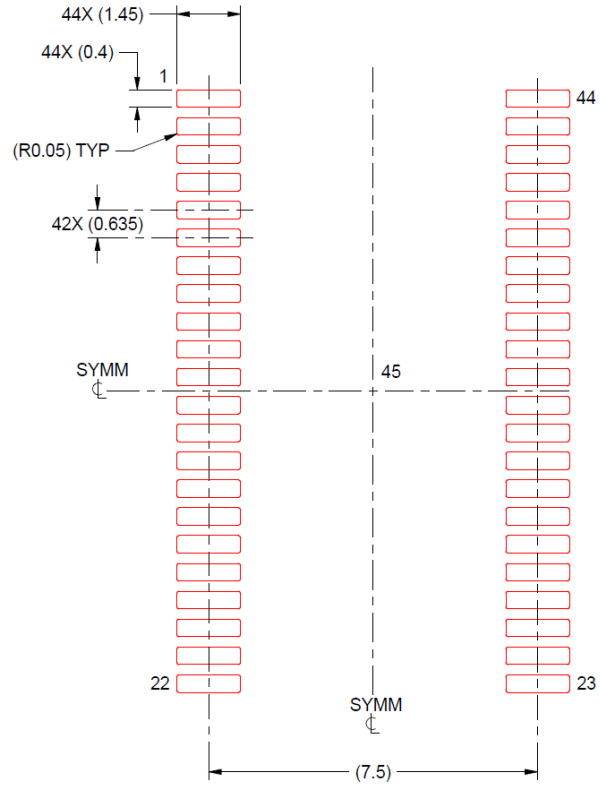
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDV0044E — **PowerPAD™ TSSOP - 1.2 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 7X

4224779/A 01/2019

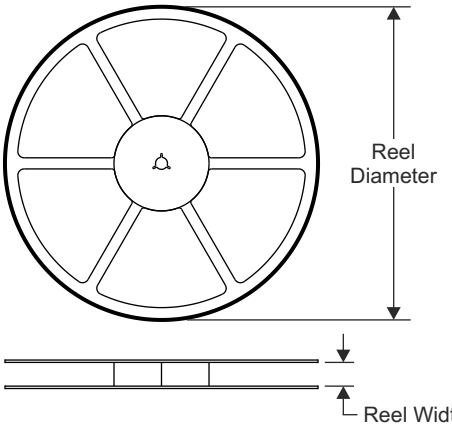
NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

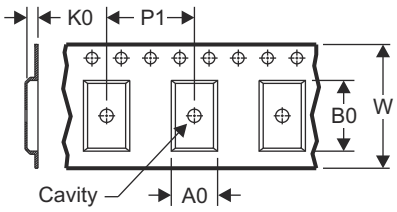
ADVANCE INFORMATION

13.1 Tape and Reel Information

REEL DIMENSIONS

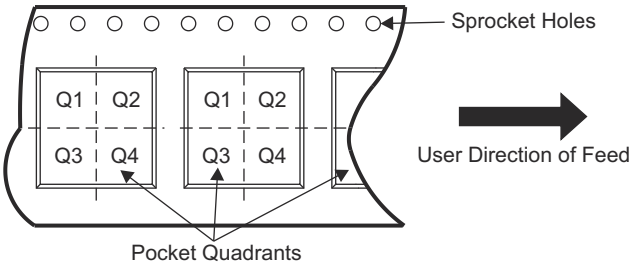


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

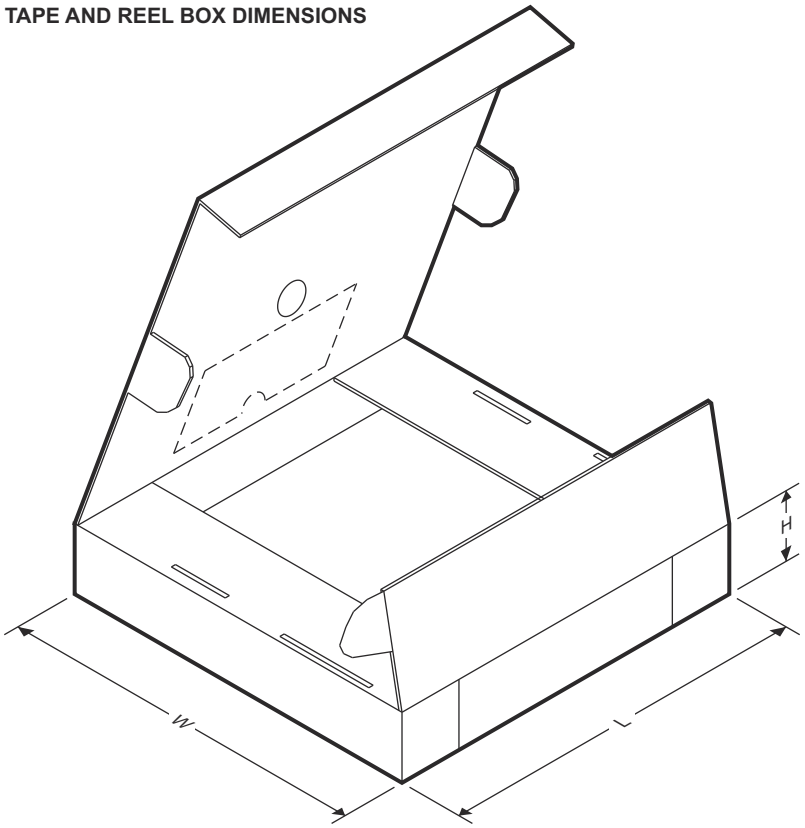
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8462DDWR	HTSSOP	DDW	44	2500	330	24.4	8.9	14.7	1.4	12	24	Q1
DRV8462DDVR	HTSSOP	DDV	44	2500	330	24.4	8.9	14.7	1.4	12	24	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8462DDWR	HTSSOP	DDW	44	2500	367.0	367.0	45.0
DRV8462DDVR	HTSSOP	DDV	44	2500	367.0	367.0	45.0

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PDRV8462DDWR	ACTIVE	HTSSOP	DDW	44	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

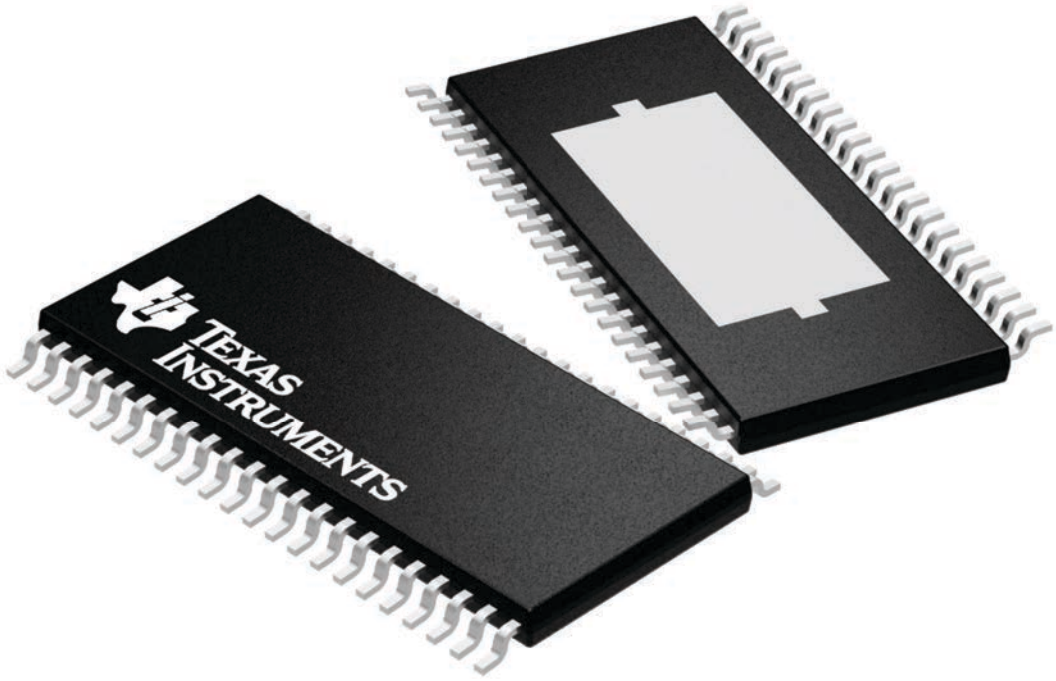
DDW 44

PowerPAD TSSOP - 1.2 mm max height

6.1 x 14, 0.635 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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