Application Report
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Using a Motor Driver DRV8848 for Low-Power Isolated Full-Bridge DC-DC Conversion

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ABSTRACT

The full-bridge DC-DC converter architecture can be used to generate isolated output voltages. This application report shows how a device originally designed for driving motors can be used to perform this function in a cost-effective and integrated way.

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1 Introduction

Electronic systems often have a requirement to provide an isolated voltage rail or multiple rails for powering wired interfaces such as RS485, wired mBus, 4-mA to 20-mA current loops, and various other types. An example application is a smart electricity meter (eMeter). Instead of producing these rails by using additional windings on the main flyback magnetics, producing these rails by taking a low voltage input and performing a low-voltage isolated conversion is sometimes desirable. This process prevents the magnetics of the main flyback converter from becoming too large, given the stringent safety isolation voltages and creepage and clearance rules that must be applied.

Various converter topologies are frequently used, such as the flyback, fly-buck (and fly-buckboost), and the push-pull converter. This application report describes another topology, the full-bridge (or H-bridge) converter. This topology offers number of advantages. One advantage is that the four FETs ensure the current always has a path to flow and therefore little or no overshoot voltage spike occurs. Using a center-tapped transformer is not required for this topology which means that low-cost toroid transformers can be used having one primary and one secondary winding. This topology has no energy storage and the transformer is fluxed in both positive and negative directions, which means the size of the magnetics is minimized. Integrated motor-control devices exist that integrate the FETs and current and thermal protection. Additionally, the dv/dt edges of these devices tend to be quite slow, benefitting systems trying to avoid RF emissions which can disrupt sensitive radio receivers that are also in the system. The final advantage of this topology is that some motor drive devices have more than one integrated H-bridge and these can be controlled separately, enabling multiple full-bridge converters to be controlled using one device. This feature is useful in applications where the outputs must be independent from each other and cannot be made simply by using one transformer having multiple isolated outputs.

2 Design of the Full Bridge DC-DC Converter

The DRV8848 device is a dual H-bridge motor control device. The device is rated up to 18-V input voltage which makes it useful for 12-V input voltage designs. Each H-bridge comprises high-side P-FETs and low-side N-FETs. An alternative architecture is a charge pump with high-side N-FETs. The charge pump can be a source of EMI and so for this EMI-sensitive application the DRV8848 device is a good choice. The DRV8848 device does have a digital core and a bead inductor (for example, Murata BLM18EG601SN1D) connected from the VINT pin to the 2.2-µF decoupling capacitor will attenuate the noise. Each H-bridge is controlled separately by the AINx and BINx logic inputs and each H-bridge has a programmable current limit (CL) using an external sense resistor (R_{ISENSE}) per H-bridge. When triggered, the current limit reacts by turning off the FETs that were ramping up the current and then by turning on the opposite pair of FETs, making the current ramp down for 20 µs (the PWM cycle) or until the next INx command occurs. The device also has a fast internal overcurrent limit, OCP (set to 2 A minimum), which, if triggered, is followed by a hiccup retry time of 1.6 ms. These protection circuits are useful for isolated converters that have to withstand a fault condition overload on their outputs. Often overlooked when making discrete FET H-bridges is the undervoltage lockout function (UVLO, approximately 3 V in the DRV8848 device). This UVLO helps prevent the FETs from switching when the supply voltage has fallen below a certain minimum level. Trying to switch on and off the FETs with a too-low supply voltage results in them entering their linear region which results in high power dissipation. The device also generates an internal supply voltage (VINT) of 3.3 V ± 5%. This voltage can be used externally, for example to power the VREF pin of the device, so as to program the current limit. Connecting the VINT pin to the VREF pin through an RC network ramps VREF during power-up, which then ramps the current limit, resulting in a soft-start behavior.

Use Equation 1 to calculate the programmable current limit (CL) on the DRV8848 device.

$$CL = \frac{VREF}{6.6 \times R_{ISENSE}} \quad (1)$$

When the VREF voltage is 3.3 V and the value of the R_{ISENSE} resistor is 1 Ω, then the current limit is 0.5 A.

Figure 1 shows an example schematic of the DRV8848 device performing a power conversion for two separately-isolated outputs. For demonstration purposes, one transformer has a center-tapped secondary with two rectifying diodes and the other has a single secondary winding followed by a full-bridge rectifier, as would usually be the case if the transformer is a toroid. A series 10-µF capacitor was added in the primary to ensure no dc offset reaches the transformer. The VREF pin is supplied from the VINT supply through an RC network that fully ramps the VREF pin in approximately 10ms to implement a soft-start.

The switching frequency is set to 200 kHz and must be supplied externally, which can be from a microprocessor I/O pin, or produced using a standalone LMC555 timer configured in 50% duty cycle mode as shown in the *LMC555 CMOS Timer* data sheet. The DRV8848 device also requires an inverted version of the clock, which is generated using an SN74LVC1G04 logic inverter gate in the schematic. To enable the device, the nSLEEP pin must be pulled high.

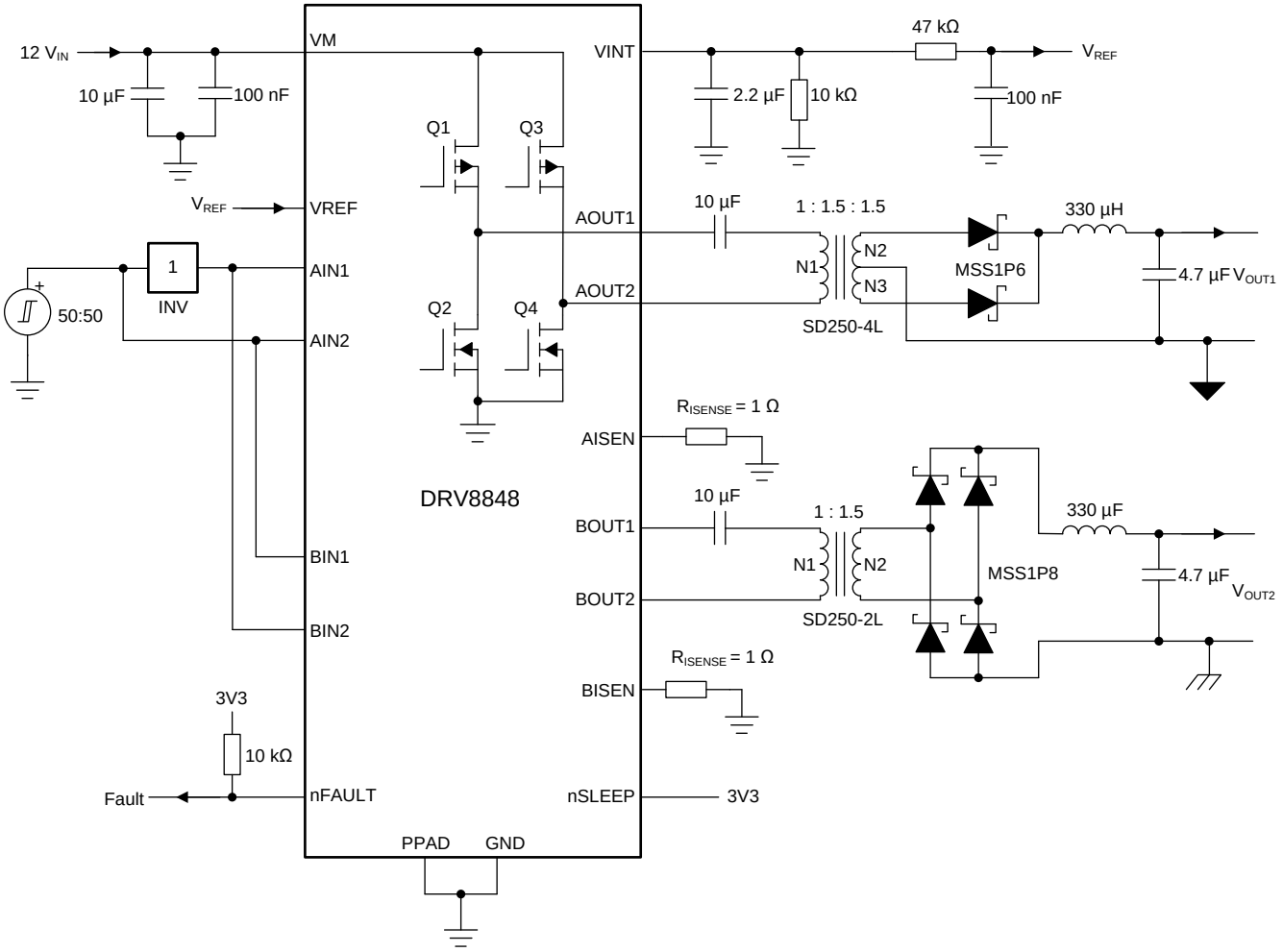


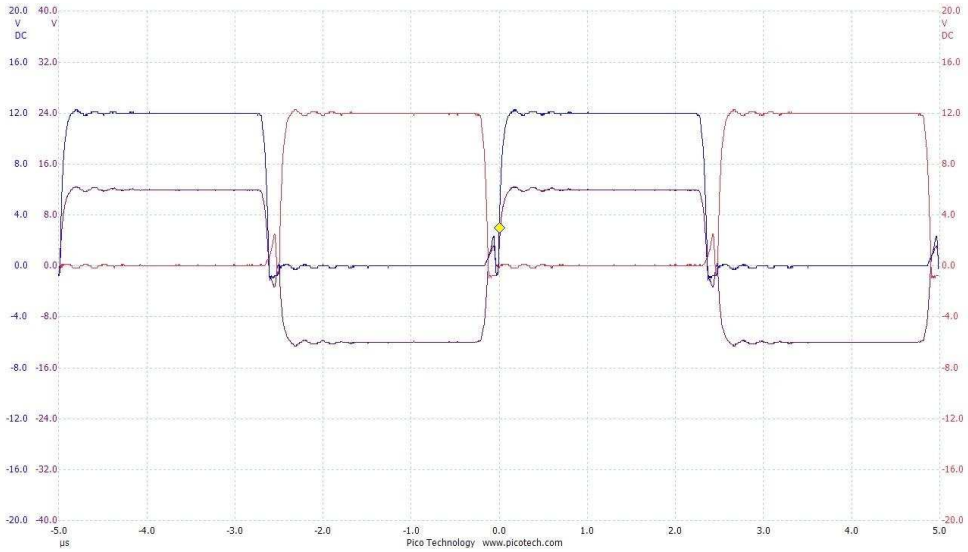
Figure 1. Circuit Schematic for Two H-Bridge Transformer-Isolated Converters Using DRV8848

A center-tapped Coilcraft transformer (SD250-4L) with a 1:1.5:1.5 turns ratio was used for the test circuit. The second channel of the DRV8848 drives another version of the magnetics (SD250-2L) with single windings 1:1.5. The DRV8848 implements a blanking period and this plus the rise/fall times subtracts from what would otherwise be a continuous 100% duty cycle converter. The blanking time is 200 ns (typical), between the switching of the high and low side FETs in each ½ bridge. Therefore the actual duty cycle seen in Figure 2 is approximately 92%. The 12-V input voltage is converted to 0.92 × 12 V × 1.5 = 16.5 V. The diode drop on the secondary reduces this to finally being a 16-V output voltage. The converter is nonregulated and this 16-V output voltage can be expected to fall as the load increases because of the winding resistances of the transformer, the FET on-resistances, and the output inductor winding resistance. In the case where the non-center-tapped transformer and full-bridge diode rectifier is used, then two diode drops must be subtracted. The Power Stage Designer™ Tool is a free downloadable TI software tool that allows users to quickly simulate the power stage waveforms for different power converter topologies. This tool was used to choose a suitable transformer primary inductance of 1.5 mH and a smoothing secondary-side inductor of 330 µH. Use Equation 2 to calculate the Volt-seconds product.

$$V_{IN} \times \frac{1}{2} \times T = 12\ V \times \frac{1}{2} \times \frac{1}{200}\ kHz = 30\ V\mu s \quad (2)$$

The selected transformer should have a Volt-seconds product that is larger than this value.

Figure 2 shows the primary phase-voltage waveforms. On the secondary side, 16 V_{DC} is measured. The load is 168 Ω. With reference to Figure 1, when the blue phase voltage falls, it is because the high-side and low-side diagonally-opposite FETs of that phase were turned off, essentially Q1 and Q4. Now a dead-time period of approximately 200 ns occurs, during which all the FETs are off, which are integral to the device. The leakage inductance of the transformer has stored energy and this pulls the blue phase negative and is clamped by the body diode of Q2. An oscillation starts, but very shortly afterwards the red-phase Q2 and Q4 FETs are turned on and the red phase voltage rises to 12 V.

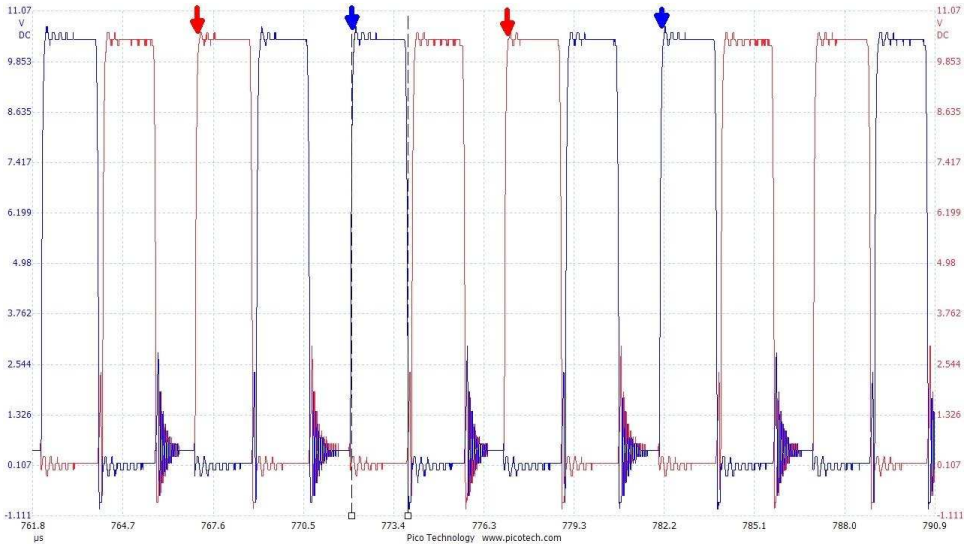


1 µs/div f_{SW} = 200 kHz

Figure 2. Primary-Side Phase Output Voltages (Red, Blue) of the Converter Phase-Phase Output is Computed (Purple) Showing the ±12-V Swing Across the Primary Side

Figure 3 shows the phase voltages during start-up, where the current limit is active. During start-up, the VREF pin is ramping and the full current limit of 0.5 A has not been reached. In Figure 3, the current limit is approximately 120 mA. The switching frequency has been reduced to 100 kHz for this test and the load has been increased to 112 Ω.

NOTE: These test conditions were not selected for any particular reason other than to show operation at a different switching frequency and load.



f_{SW} = 100 kHz

Figure 3. Primary-Side Phase Output Voltages (Red, Blue) of the Converter Showing CL Behavior of DRV8848 During Start-Up

The blue phase turns on (at the first blue arrow marker) and goes high for approximately 1.8 µs (the current-limit blanking time) at which point the current limit has been reached and it turns off (at the second dashed-line ruler marker shown in Figure 3). The DRV8848 control logic behavior is that the red phase now turns on to enable fast-decay mode, which it does so (after the second dashed-line ruler marker shown in Figure 3) and so the red phase goes high. After about 1.6 µs, the current has fallen almost to zero and the DRV8848 behavior is that the bridge is disabled to prevent reverse current flow. A period where neither phase is on now occurs. Sometime later, the red phase turns on (second red arrow shown in Figure 3) because the INx command has gone high to turn on that phase, which occurs before the 20-µs PWM period of the device has elapsed. The change (delta) between the two red arrows (or the two blue arrows) is 10 µs, which is the period of 100 kHz. The other instances where blue or red phase voltages appear are because of the current-limit behavior of the device.

Driving the H-bridge with a duty cycle other than 92% is also possible. Figure 4 shows the INx drive waveforms for a duty cycle of 60% and Figure 5 shows the phase voltages when driving the transformer. When the PWM signals driving the bridge are both low, the FETs are all off. On the falling edge of a phase voltage a resonance occurs followed by a dc-offset voltage of 0.6 V, set by the leakage currents of the H-bridge. Another way of driving a non-50% duty cycle is to overlap the INx drive signals as shown in Figure 6 and the resulting phase voltages in Figure 7. When both INx drive signals are high, the DRV8848 device responds by turning on the low-side FETs, Q2 and Q4 which clamps both sides of the transformer to 0 V and the result is a cleaner waveform.

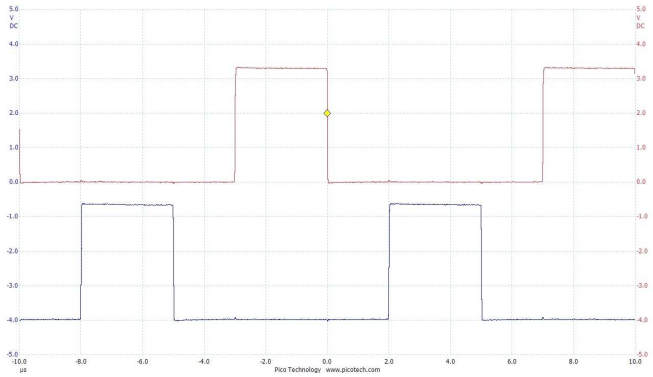
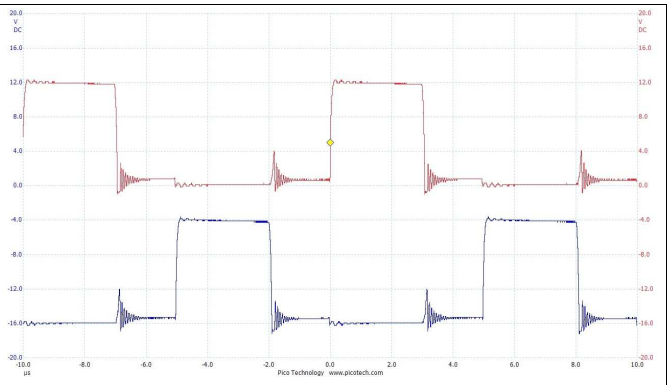


Figure 4. INx Drive Signals for a Duty Cycle of 60%



These phase voltages are a result from the drive signals of Figure 4.

Figure 5. Resulting Phase Voltages

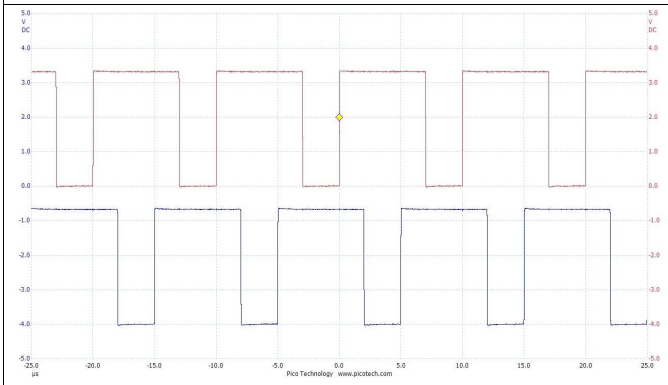
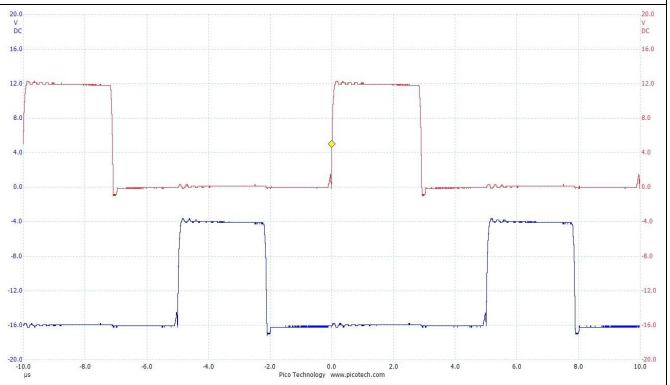


Figure 6. INx Drive Signals for a Duty Cycle of 60% When the INx are Overlapped



These phase voltages are a result from the drive signals of Figure 6.

Figure 7. Resulting Phase Voltages

3 Conclusion

The DRV8848 device can be used to make two independent full-bridge DC-DC converters. The device provides integrated protection features and is a useful addition to the techniques for generating isolated voltage rails. The DRV8848 device is a fully-integrated solution for implementing two cost-effective full-bridge converters. The DRV8848 device integrates protection features such as thermal limit and a programmable current limit. The device also has a fast peak overcurrent limit. A soft-start can be implemented by controlling the voltage on the VREF pin. Other motor driver devices can be used to implement a full bridge converter, ranging from low voltage devices, such as the DRV8835, DRV8837, and DRV8839, to higher voltages, such as the DRV8870, DRV8871, DRV8872, DRV8841, and DRV8842.

4 References

For additional reference, refer to:

- Texas Instruments, *LMC555 CMOS Timer* data sheet
- Texas Instruments, *DRV8848 Dual H-Bridge Motor Driver* data sheet
- Texas Instruments, *SN74LVC1G04 Single Inverter Gate* data sheet

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