Application Report
SNLA226–August 2014

DS125BR820 Linear Repeater Used in 40GbE nPPI / SFF-8431 Applications

SVA Data Path Solutions

ABSTRACT

This report summarizes the results of 40GbE nPPI and 4x10GbE SFF-8431 testing using TI's DS125BR820 low-power 12.5 Gbps 8-channel linear repeater. It specifically addresses applications where the DS125BR820 is used for front-port signal conditioning behind QSFP+ cages supporting 40GBASE-CR4/SR4/LR4 and SFF-8431 interfaces. The DS125BR820 is tested in an egress signal conditioning configuration against the eye mask and jitter requirements for 40GbE nPPI and 10G SFF-8431 using a 2x1 stacked QSFP+ connector and host compliance board (HCB). These tests demonstrate the excellent signal conditioning capabilities of the DS125BR820 linear repeater, showing that the DS125BR820 can extend the reach between the host ASIC and the front-port cage by up to 3× beyond the nPPI and SFF-8431 host PCB channel limits.

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1 Introduction

The testing carried out in this report involves the DS125BR820 low-power 12.5Gbps 8-channel linear repeater, which is designed to support 40GbE (40G-CR4/KR4/SR4/LR4), 12G SAS-3, and PCIe Gen 3.0 applications. The linear nature of the DS125BR820's equalization allows the DS125BR820 to preserve the transmit signal characteristics of the host switch, thereby allowing the host switch and the link partner ASIC to negotiate transmit equalizer coefficients during IEEE802.3ba Clause 72 Link Training. In addition, the low additive jitter allows the DS125BR820 to support the stringent front-port eye mask and jitter requirements of SFF-8431, which is necessary for 4x10G SFP+ applications.

The DS125BR820 is in a small 10-mm × 5.5-mm leadless WQFN package, which fits easily behind a standard 2x1 stacked QSFP+ connector, such as the Molex zQSFP+™ 171565 series connector used in these tests.

Figure 1 shows the typical front-port applications of the DS125BR820.

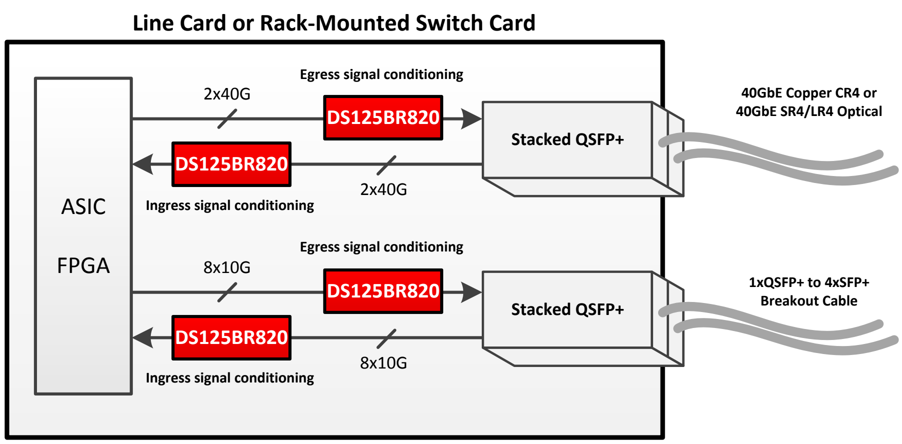


Figure 1. Typical Front-Port Applications of the DS125BR820

Numerous advantages exist for using the DS125BR820 linear repeater for 40GbE front-port applications versus a traditional PHY. Table 1 lists some of these advantages for a generic 36-port switch card application.

Table 1. System-Level Benefits Breakdown for a Generic 36-Port 40-GbE Switch Card

	TI DS125BR820 Implementation	Traditional CR4 PHY Implementation	Benefit of TI
Number of devices	18 (Egress signal conditioning only) 36 (Egress + Ingress signal conditioning)	18 (Egress + Ingress signal conditioning)	
Total device PCB area consumed	18 × 55 mm^2 = 990 mm^2 (Egress only) 36 × 55 mm^2 = 1980 mm^2 (Egress + Ingress)	Approximately 4050 mm^2	Less than half the PCB area
Number of power rails	One only (2.5 or 3.3 V)	Up to four	Simpler power supply design
Board power consumption	10 W (Egress only) 20 W (Egress + Ingress)	Approximately 36 W	Half the power
Input-to-output latency	<200 ps	Approximately tens of ns	Smaller latency
40GBASE-CR4/KR4	Yes	Yes	
40GBASE-LR4/SR4	Yes	Yes	
Reference clock required	No reference clock required	Low-jitter reference clock fan-out to all PHYs	No reference clock
PCB design flexibility	Unidirectional configuration allows for flexibility in device placement → more optimized for compact PCB design	Limited flexibility. Lane swapping is complicated and limited.	More flexibility in routing
User experience	Simple-to-use one-time configuration over I^2C or EEPROM. All devices can share one EEPROM.	Firmware load required	Faster initialization
Implementation cost	Minimal external passive components (that is decoupling capacitors), no need for supply filtering or reference clock distribution.	Numerous passive components typically used (power supply filters, low-jitter reference clock fan-out, and so forth)	Lower overall BOM cost

2 40GbE nPPI / SFF-8431 Egress Jitter and Eye Mask Testing

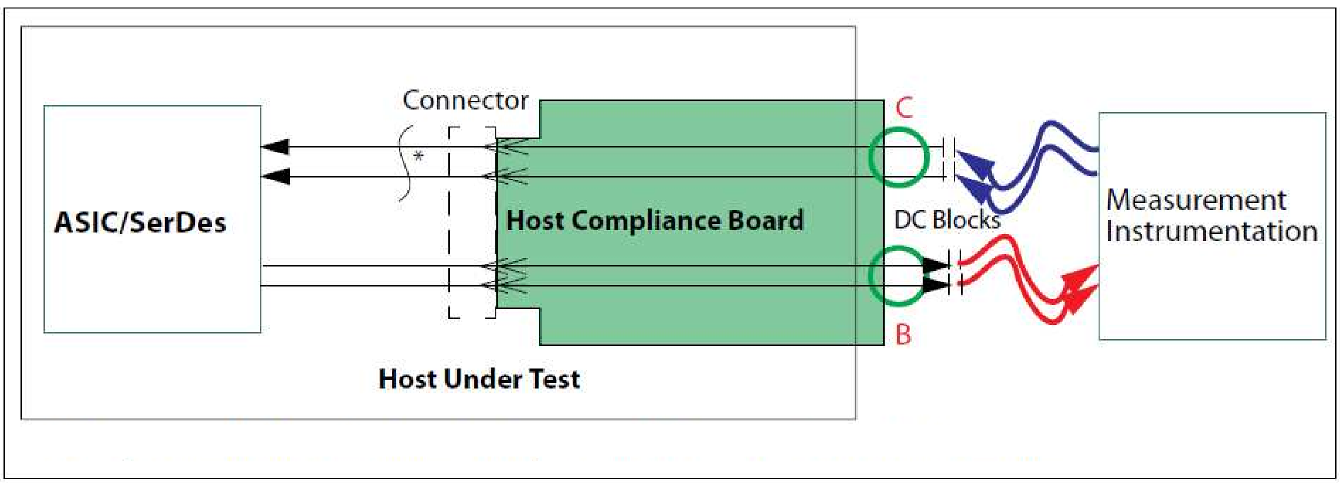
40GbE nPPI is a parallel physical interface that allows for the construction of compact optical transceiver modules for 40GBASE-SR4/LR4 with no clock and data recovery circuits inside. As a result, the IEEE802.3ba standard, which governs the nPPI interface, has defined several jitter and eye mask requirements for the eye opening at the host board output to ensure the proper functioning of the attached optical modules.

Some 40GbE front-port applications require backwards compatibility with 10GbE SFF-8431. For example, if 40G breakout cables are used (that is one QSFP+ to four SFP+ breakout cables), then the system must not only comply with 40GbE nPPI, but it must also pass the more stringent SFF-8431 transmit specifications. Due to the nature of the optical modules used in SFF-8431 applications, the jitter requirements for SFF-8431 are more stringent than those for 40GbE nPPI.

The experiments in this report demonstrate the DS125BR820's ability to provide excellent signal conditioning for the purposes of meeting the nPPI and SFF-8431 transmit electrical specifications.

2.1 *Industry Specifications*

Both nPPI and SFF-8431 specify jitter limits at a testpoint which is equivalent to the output of the HCB. This testpoint is shown in Figure 2 and is shown as compliance point B in SFF-841 and compliance point TP1a in nPPI.



A *C" equivalent is located about 1 inch past the SFP+ connector on the host board.

Figure 2. Host Transmitter Compliance Point

The jitter specifications for nPPI and SFF-8431 at the host transmitter compliance point are listed in Table 2.

Table 2. nPPI and SFF-8431 Host Transmitter Jitter Specifications

Interface Specification	Data Dependent Pulse Width Shrinkage (DDPWS) mUI (p-p)	Data Dependent Jitter (DDJ) mUI (p-p)	Total Jitter (TJ) mUI (p-p)	Comment
nPPI	≤70	N/A	≤290[(1)]	IEEE802.3ba, Table 86A-1
SFF-8431	≤55	≤100	≤280	SFF-8431, Table 12

(1) Based on nPPI J9 specification, which is total jitter at 1E-9 BER.

In addition to jitter requirements, both the nPPI and SFF-8431 specifications place requirements on the transmitter eye mask at the host compliance point, as shown in Figure 3 and Table 3.

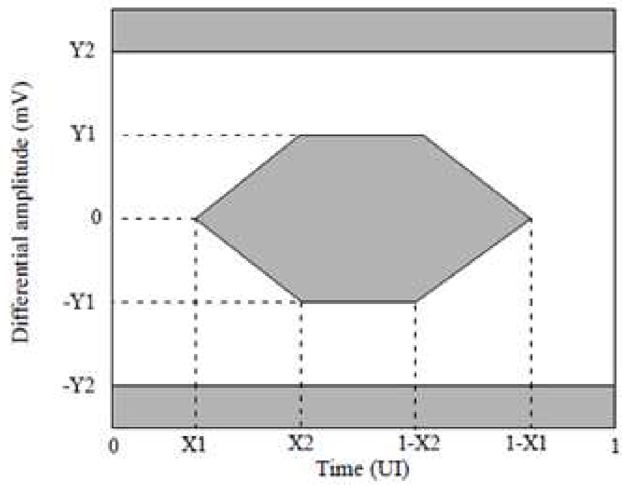


Figure 3. nPPI and SFF-8431 Host Transmitter Eye Mask

Table 3. nPPI and SFF-8431 Host Transmitter Eye Mask Specifications

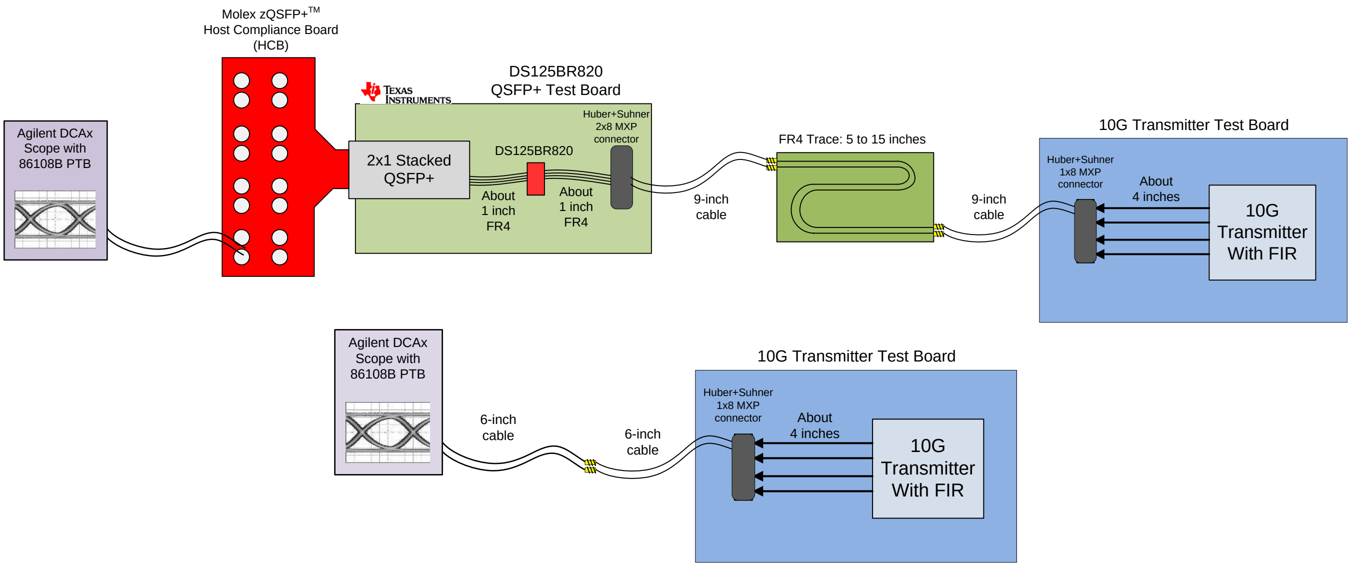
Interface Specification	X1 [UI]	X2 [UI]	Y1 [mV]	Y2 [mV]	Comment
nPPI	0.11	0.31	95	350	IEEE802.3ba, Table 86A-1
SFF-8431	0.12	0.33	95	350	SFF-8431, Table 12

2.2 Setup – Hardware

The hardware setup for these tests consists of:

1. Commercially-available 10GbE transmitter with 3-tap FIR filter and PRBS pattern generator
2. DS125BR820 QSFP+ test board, with 2x1 stacked QSFP+ cage
3. Various lengths of FR4 media (5in, 10in, 15in, etc.)
4. Huber+Suhner MXP cable assemblies, for connecting the 10G transmitter test board to the FR4 media, and the FR4 media to the DS125BR820 QSFP+ test board
5. Molex zQSFP+™ HCB
6. Agilent DCAx sampling scope, with 86108B precision time base (PTB) module

Figure 4 shows the test setup. In this scenario, the 10G transmitter test board transmits a PRBS9 data pattern, which is required by nPPI and SFF-8431 for transmitter testing. This data passes through various lengths of lossy media, then into the DS125BR820 QSFP+ test board. The DS125BR820 linear repeater equalizes the signal and redrives it toward the QSFP+ connector. The equalized eye is measured at the output of the HCB by the Agilent™ DCAx scope, which will check for jitter and eye mask compliance against the nPPI and SFF-8431 specifications.



A Top figure: With DS125BR820 QSFP+ board

B Bottom figure: 10GbE transmitter only

Figure 4. 40GBASE-SR4/LR4 Test Setups

This test fixture is intended to mimic a line card or rack-mounted switch card design, similar to Figure 5.

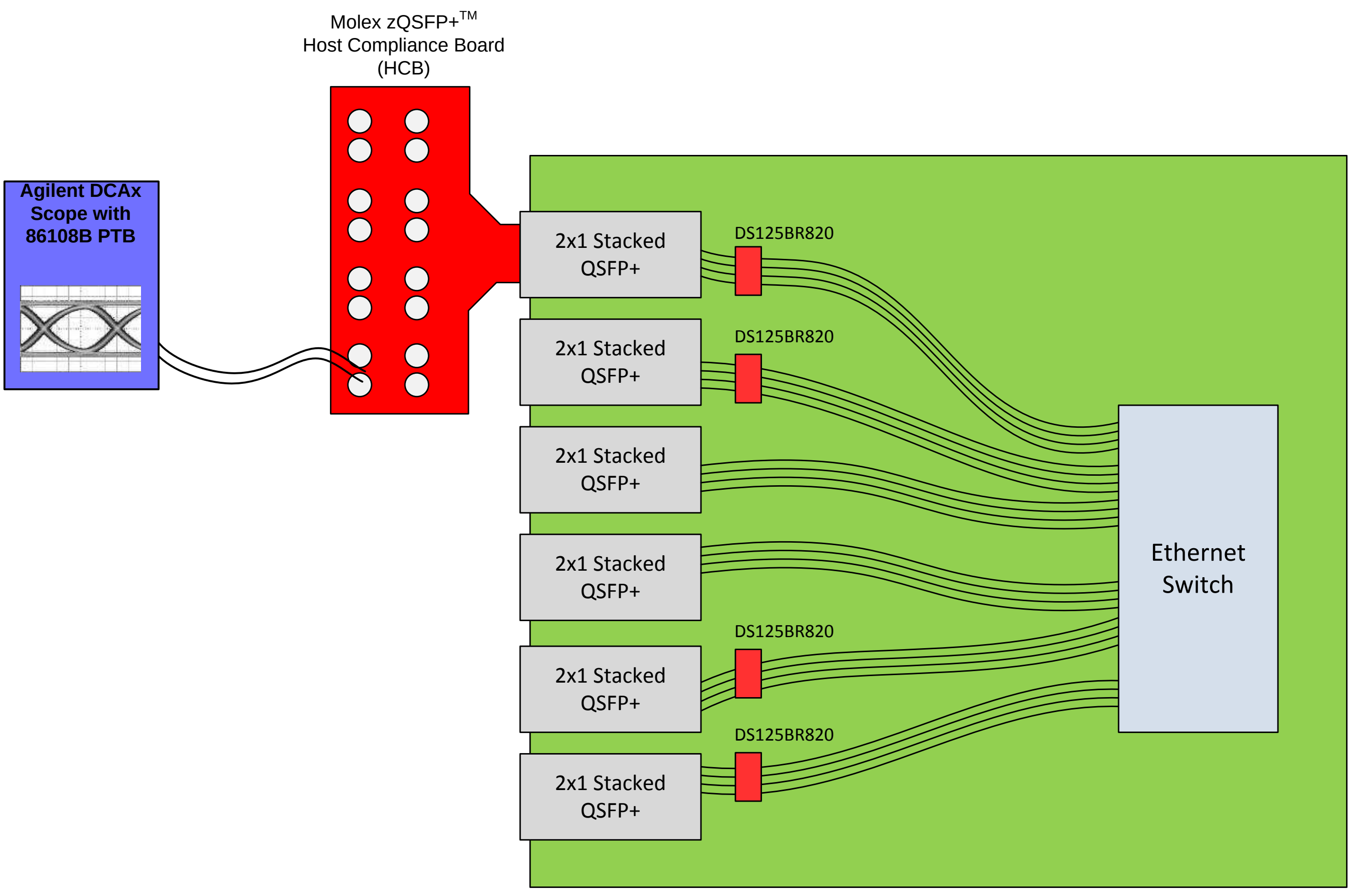
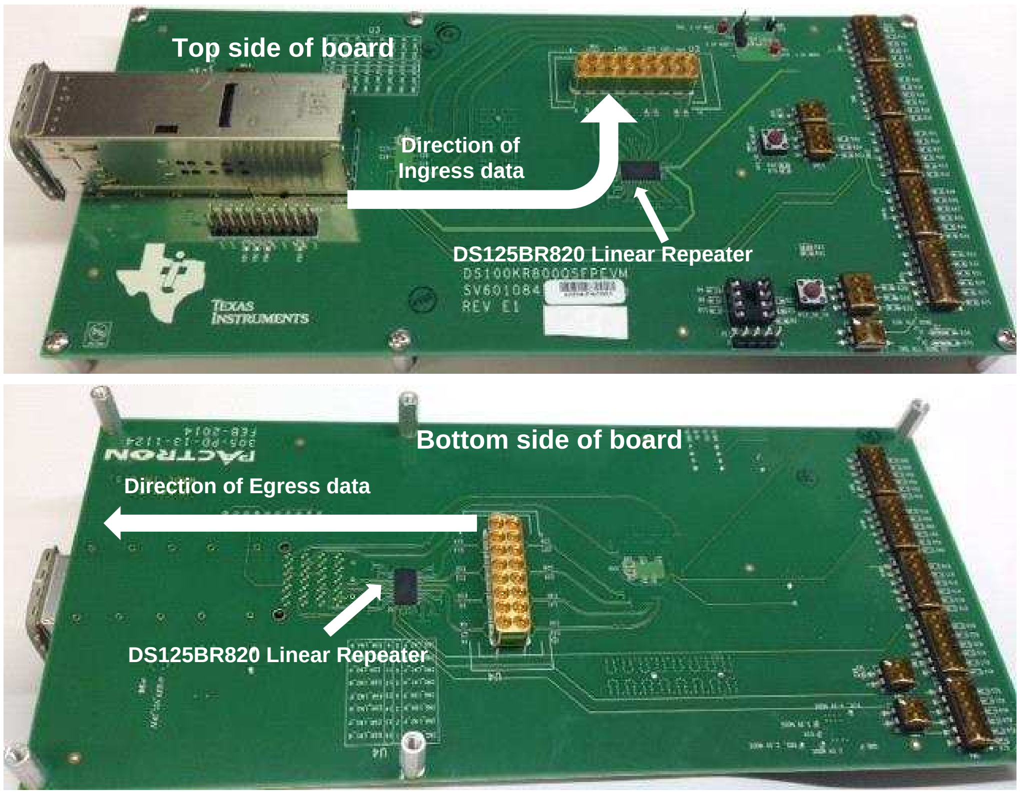


Figure 5. Front-Port Design Using DS125BR820 Linear Repeaters

Figure 6 shows the DS125BR820 QSFP+ test board. The test board has two 40G QSFP+ ports arranged in a stacked 2x1 configuration on the line-side interface. It has two high-density Huber+Suhner 2x8 MXP connectors on the host-side interface, for connecting to switch ASIC test cards.



A Top image: Top side of board, showing ingress chip

B Bottom image: Bottom side of board, showing egress chip

Figure 6. DS125BR820 QSFP+ EVM

2.3 Setup – Device Configuration

Table 4 lists the settings used for the DS125BR820 repeater in these tests.

Table 4. DS125BR820 Settings Used for Testing

EQ Setting			VOD Setting			Comments
Value	Pin Strap	Equivalent Register Setting (1)	Value	Pin Strap	Equivalent Register Setting (2)	
Level 1	0: 1 kΩ to GND	Reg_0xF = 0x00	Level 6	VODA1 = VODB1 = 1 (1 kΩ to VIH) VODA0= VODB0 = 0 (1 kΩ to GND)	Reg_0x10 = 0xAE	Different EQ settings used for different input channel length. VOD level 6 used for all channels.
Level 2	R: 20 kΩ to GND	Reg_0xF = 0x01				
Level 3	F: Floating	Reg_0xF = 0x02				
Level 4	1: 1 kΩ to VIH	Reg_0xF = 0x03				

(1) Each channel has its own EQ control register. Reg_0x0F controls channel 0, Reg_0x16 controls channel 1, and so on.

(2) Each channel has its own VOD control register. Reg_0x10 controls channel 0. Reg_0x17 controls channel 1, and so on.

2.4 Results

To demonstrate compliance to nPPI and SFF-8431, two tests were performed:

- Host transmitter output jitter
- Host transmitter output eye

2.4.1 Host Transmitter Output Jitter

The host transmitter output jitter was measured for various combinations of PCB trace, and Table 5 summarizes the results.

Table 5. Host Transmit Output Jitter Results

Test Case	Test Includes Repeater	Approximate DS125BR820 Input Loss [dB]	DDPWS [mUIpp]	TJ [mUIpp]	DDJ [mUIpp]	Overall Result	Comment
SFF-8431 specification			≤55	≤280	≤100		If 40G port is used as 4x10G port
nPPI specification			≤70	≤290[(1)]	N/A		For 40GBASE-SR4/LR4
Baseline Tests Without Repeater							
Baseline: Host TX → 4-inch Rogers → 6-inch H+S cable → 6-inch minibend cable → Agilent DCAx	No	N/A	64	144	64	Fail DDPWS	Host TX pre = 0, main = 30, pst = 0
Baseline: Host TX → 4-inch Rogers → 6-inch H+S cable → 6-inch minibend cable → Agilent DCAx	No	N/A	30	127	43	Pass	Host TX pre = –1, main = 34, pst = –2
Testing Different Lengths of Input Channel With a Repeater							
Host TX → 4-inch Rogers → 6-inch H+S cable → 9-inch H+S cable → BR820 EVM → top QSFP TX1 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–4	20	129	48	Pass	DS125BR820 EQ Level 1 Host TX pre = –2, main = 31, pst = –2
Host TX → 4-inch Rogers → 9-inch H+S cable → 5-inch 4mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX1→ HCB → 6-inch minibend cable → Agilent DCAx	Yes	–8	24	133	50	Pass	DS125BR820 EQ Level 2 host TX pre = –3, main = 34, pst = –1
Host TX → 4-inch Rogers → 9-inch H+S cable → 10-inch 4mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX1 → HCB → 6-inch minibend cable → Agilent DCAx→	Yes	–12	35	156	69	Pass	DS125BR820 EQ Level 2 Host TX pre = –3, main = 40, pst = –9
Host TX → 4-inch Rogers → 9-inch H+S cable → 15-inch 5mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX1 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–15	31	151	64	Pass	DS125BR820 EQ Level 3 Host TX pre = –5, main = 42, pst = –9
Host TX → 4-inch Rogers → 9-inch H+S cable → 15-inch 4mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX1 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–16	40	154	65	Pass	DS125BR820 EQ Level 3 Host TX pre = –5, main = 43, pst = –11
Testing All Channels in a Port With the Same Settings							
Host TX → 4-inch Rogers → 9-inch H+S cable → 15-inch 5mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX1 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–15	31	151	64	Pass	DS125BR820 EQ Level 3 Host TX pre = –5, main = 42, pst = –9
Host TX → 4-inch Rogers → 9-inch H+S cable → 15-inch 5mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX2 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–15	45	163	75	Pass	DS125BR820 EQ Level 3 Host TX pre = –5, main = 42, pst = –9
Host TX → 4-inch Rogers → 9-inch H+S cable → 15-inch 5mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX3 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–15	30	154	67	Pass	DS125BR820 EQ Level 3 Host TX pre = –5, main = 42, pst = –9

(1) nPPI specifies 'J9 Jitter', which can be thought of as total jitter at a 1E-9 BER level.

Table 5. Host Transmit Output Jitter Results (continued)

Test Case	Test Includes Repeater	Approximate DS125BR820 Input Loss [dB]	DDPWS [mUIpp]	TJ [mUIpp]	DDJ [mUIpp]	Overall Result	Comment
Host TX → 4-inch Rogers → 9-inch H+S cable → 15-inch 5mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX4 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–15	27	152	65	Pass	DS125BR820 EQ Level 3 Host TX pre = –5, main = 42, pst = –9

2.4.2 Host Transmitter Output Eye Mask

The host transmitter output jitter was measured for various combinations of PCB trace, and Table 6 summarizes the results.

Table 6. Host Transmit Output Eye Mask Results

Test Case	Test Includes Repeater	Approximate DS125BR820 Input Loss [dB]	Eye Mask Test Result		Comment
			nPPI	SFF-8431	
Baseline Tests Without Repeater					
Baseline: Host TX → 4-inch Rogers → 6-inch H+S cable → 6-inch minibend cable → Agilent DCAx	No	N/A	Pass	Pass	Host TX pre = 0, main = 30, pst = 0
Baseline: Host TX → 4-inch Rogers → 6-inch H+S cable → 6-inch minibend cable → Agilent DCAx	No	N/A	Pass	Pass	Host TX pre = –1, main = 34, pst = –2
Testing Different Lengths of Input Channel With a Repeater					
Host TX → 4-inch Rogers → 6-inch H+S cable → 9-inch H+S cable → BR820 EVM → top QSFP TX1 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–4	Pass	Pass	DS125BR820 EQ Level 1 Host TX pre = –2, main = 31, pst = –2
Host TX → 4-inch Rogers → 9-inch H+S cable → 5-inch 4mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX1→ HCB → 6-inch minibend cable → Agilent DCAx	Yes	–8	Pass	Pass	DS125BR820 EQ Level 2 host TX pre = –3, main = 34, pst = –1
Host TX → 4-inch Rogers → 9-inch H+S cable → 10-inch 4mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX1 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–12	Pass	Pass	DS125BR820 EQ Level 2 Host TX pre = –3, main = 40, pst = –9
Host TX → 4-inch Rogers → 9-inch H+S cable → 15-inch 5mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX1 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–15	Pass	Pass	DS125BR820 EQ Level 3 Host TX pre = –5, main = 42, pst = –9
Host TX → 4-inch Rogers → 9-inch H+S cable → 15-inch 4mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX1 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–16	1 hit in center region	Pass	DS125BR820 EQ Level 3 Host TX pre = –5, main = 43, pst = –11
Testing All Channels in a Port With the Same Settings					
Host TX → 4-inch Rogers → 9-inch H+S cable → 15-inch 5mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX1 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–15	Pass	Pass	DS125BR820 EQ Level 3 Host TX pre = –5, main = 42, pst = –9

Table 6. Host Transmit Output Eye Mask Results (continued)

Test Case	Test Includes Repeater	Approximate DS125BR820 Input Loss [dB]	Eye Mask Test Result		Comment
			nPPI	SFF-8431	
Host TX → 4-inch Rogers → 9-inch H+S cable → 15-inch 5mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX2 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–15	Pass	Pass	DS125BR820 EQ Level 3 Host TX pre = –5, main = 42, pst = –9
Host TX → 4-inch Rogers → 9-inch H+S cable → 15-inch 5mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX3 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–15	Pass	Pass	DS125BR820 EQ Level 3 Host TX pre = –5, main = 42, pst = –9
Host TX → 4-inch Rogers → 9-inch H+S cable → 15-inch 5mil FR4 → 9-inch H+S cable → BR820 EVM → top QSFP TX4 → HCB → 6-inch minibend cable → Agilent DCAx	Yes	–15	Pass	Pass	DS125BR820 EQ Level 3 Host TX pre = –5, main = 42, pst = –9

3 Conclusion

This report demonstrates that the DS125BR820 linear repeater can enable SFF-8431 and nPPI host TX compliance for channels up to 15 dB of insertion loss between the host TX and the DS125BR820 input. The SFF-8431 specification limits the loss between the host transmitter and the front-port cage to 5.2 dB of insertion loss (6.25 dB total including host compliance board), and the nPPI specification limits the host PCB loss to 4.4 dB. The tests in this report show that the DS125BR820 linear repeater enables host PCB loss up to 3× longer than the SFF-8431/nPPI specifications, extending the channel from 4.4 dB to approximately 15 dB. This provides ample margin for typical switch card designs, where the goal to minimize cost and power consumption drive the need for signal conditioning only on the outermost ports. Supporting 40GBASE-CR4/SR4/LR4 and SFF-8431 using the DS125BR820 is the optimal way to achieve the required performance while minimizing BOM cost and power consumption.

Appendix A Detailed Results

The following figures show the jitter and eye mask measurements for different lengths of PCB media between the host transmitter and the DS125BR820 input in a 40GbE front-port application. All eye masks shown are for nPPI, which is a more stringent eye mask compared to SFF-8431.

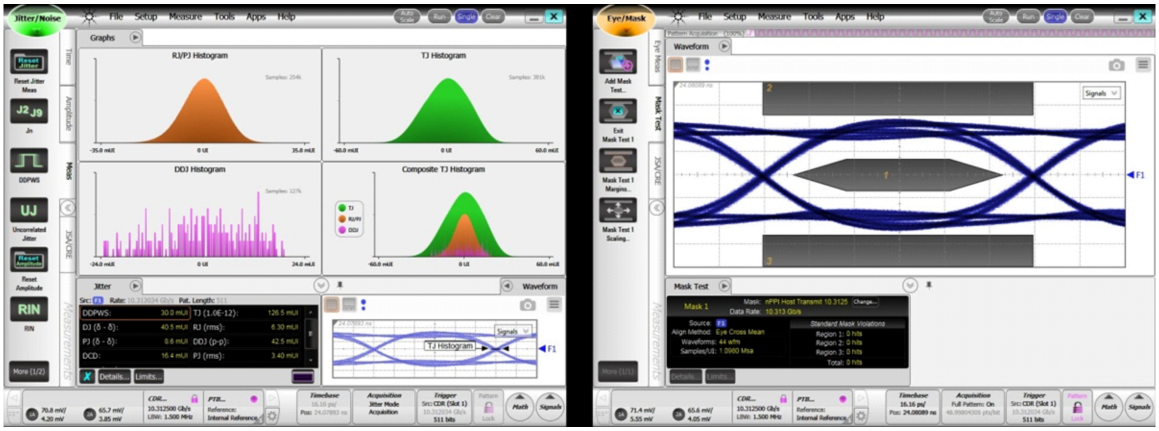


Figure 7. Baseline: Host TX → 4-inch Rogers → 6-inch H+S Cable → 6-inch Minibend Cable → Agilent DCAx

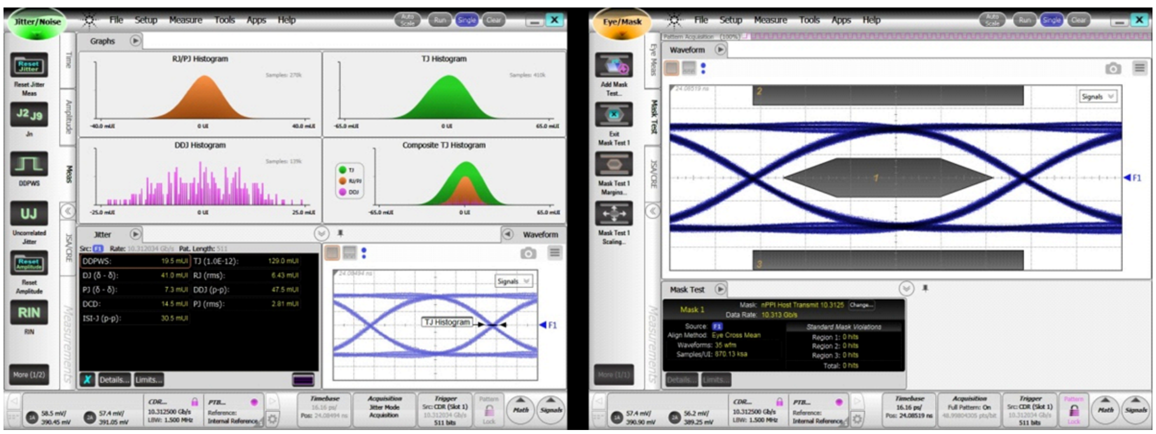


Figure 8. Host TX → 4-inch Rogers → 6-inch H+S Cable → BR820 EVM → Top QSFP TX1 → HCB → 6-inch Minibend Cable → Agilent DCAx

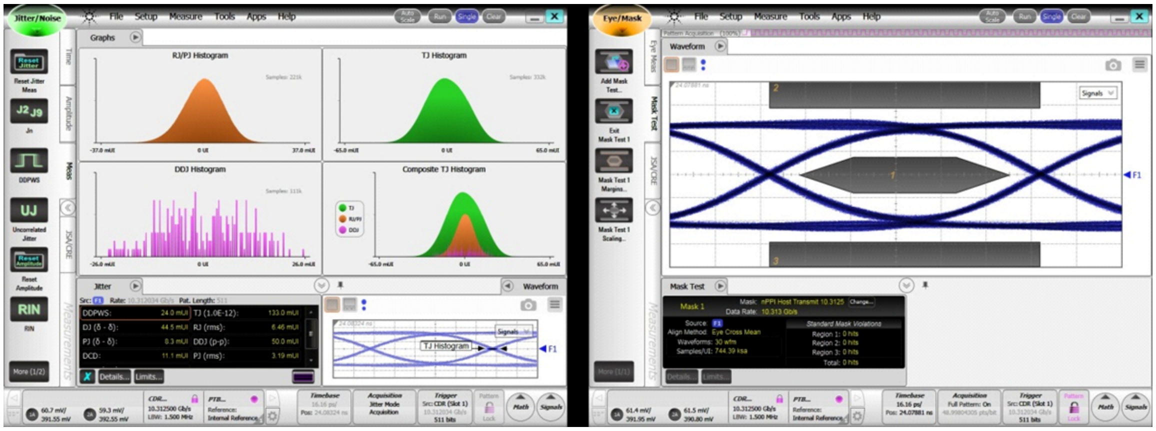


Figure 9. Host TX → 4-inch Rogers → 9-inch H+S Cable → 5-inch 4mil FR4 → 9-inch H+S Cable → BR820 EVM → Top QSFP TX1→ HCB → 6-inch Minibend Cable → Agilent DCAx

Figure 10. Host TX → 4-inch Rogers → 9-inch H+S Cable → 10-inch 4-mil FR4 → 9-inch H+S Cable → BR820 EVM → Top QSFP TX1 → HCB → 6-inch Minibend Cable → Agilent DCAx

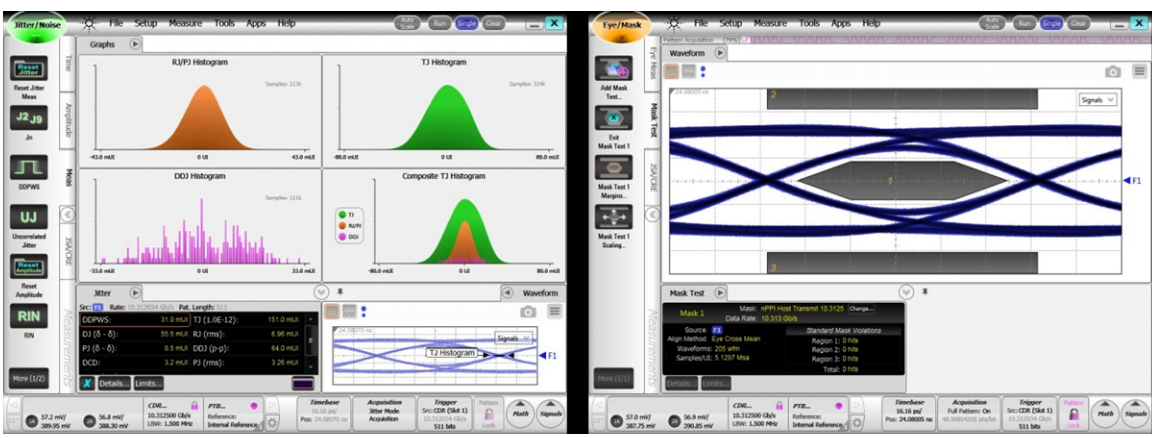


Figure 11. Host TX → 4-inch Rogers → 9-inch H+S Cable → 15-inch 5-mil FR4 → 9-inch H+S Cable → BR820 EVM → Top QSFP TX1 → HCB → 6-inch Minibend Cable → Agilent DCAx

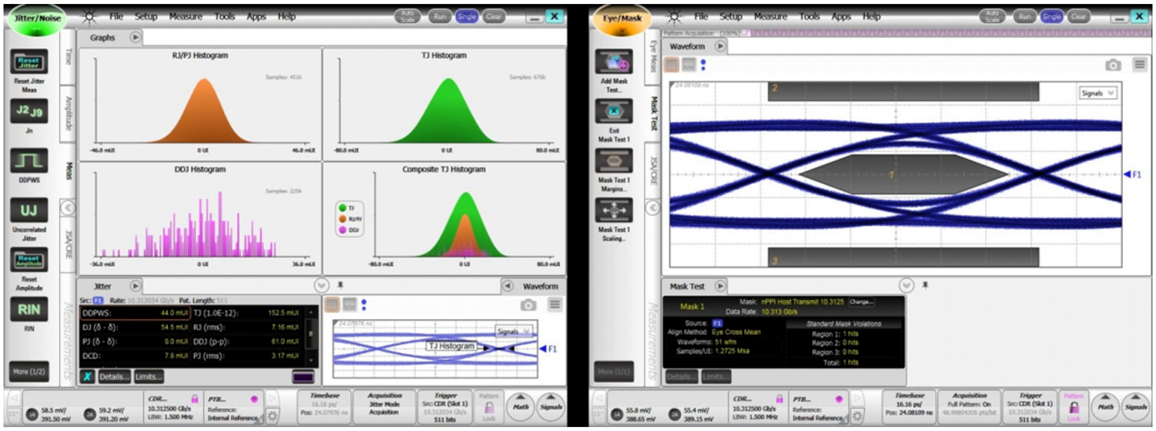
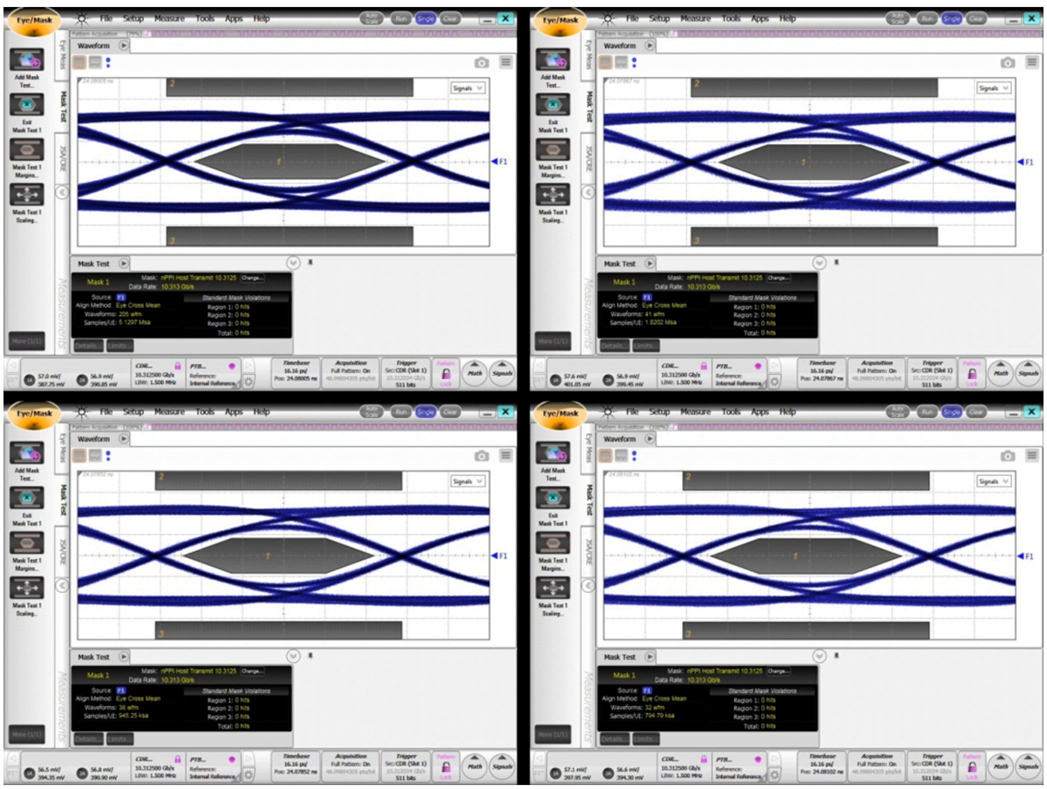


Figure 12. Host TX → 4-inch Rogers → 9-inch H+S Cable → 15-inch 4-mil FR4 → 9-inch H+S Cable → BR820 EVM → Top QSFP TX1 → HCB → 6-inch Minibend Cable → Agilent DCAx



A TX1 top left, TX2 top right, TX3 bottom left, TX4 bottom right

Figure 13. Comparison of All 4 Egress Channels for the 15-inch 5-mil Case

Appendix B Layout Considerations

Stacked QSFP+ cages are commonly used in 40GbE switch applications. The 8-channel DS125BR820 easily fits behind a standard 2x1 stacked QSFP+ cage to service all eight egress channels or all eight ingress channels. The unidirectional configuration of the DS125BR820 channels allow for optimum placement of the signal conditioner: close to the cage for egress applications and closer to the switch ASIC for ingress applications.

Figure 14 shows an example layout for the high-speed egress channels between a DS125BR820 device (placed on bottom of the PCB) and a stacked QSFP+ cage (placed on top of the PCB).

NOTE: Note that the DS125BR820 is placed close to the QSFP+ cage to equalize all the egress signals. This type of placement--close to the QSFP+ cage for egress data--is highly recommended.

The ingress signals can easily be routed to another DS125BR820 if the application requires, and the two DS125BR820 repeaters can be placed on opposite sides of the PCB (top and bottom) if that facilitates board routing. The DS125BR820 does not require a heat sink or airflow because the power consumption is only 70 mW/channel.

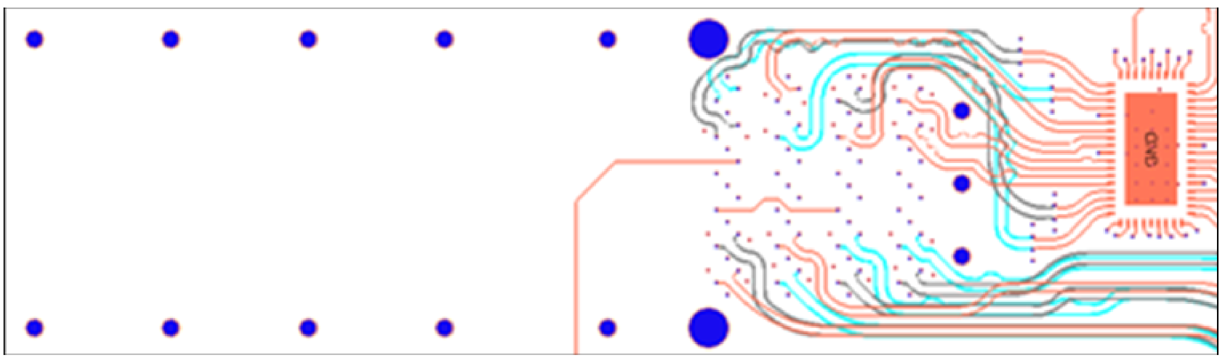


Figure 14. Example Layout for Egress Repeater to Stacked QSFP+ Cage

It is also possible for the egress signals to be routed all on one routing layer to avoid vias. This would require routing signals beyond the width of the QSFP+ cage; however, for typical applications where the QSFP+ cages are spaced 25 mm apart, there is still enough space to route all the high-speed signals. This concept is illustrated in Figure 15.

NOTE: Note that Figure 15 is not to scale and is not meant to represent an actual layout. It is for conceptual illustration only.

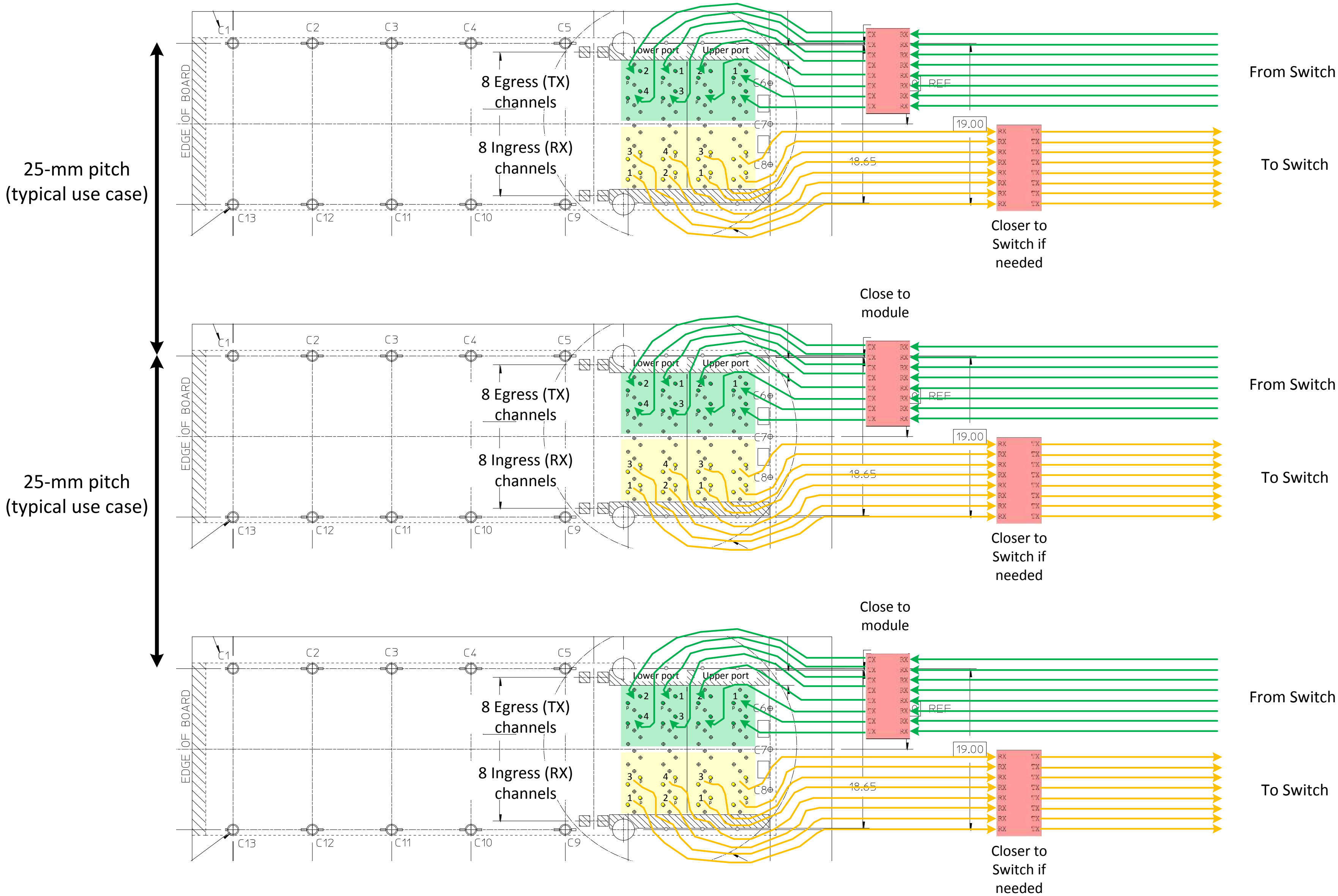


Figure 15. Conceptual Layout for Both Egress and Ingress Using DS125BR820

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

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