Application Report
SNLA227–October 2014

Advanced Linear Repeater Used in PCIe Gen 3.0 Add-in Card Compliance Environment

SVA Data Path Solutions

ABSTRACT

This report summarizes the results of PCIe Gen 3.0 add-in card compliance testing using TI's low-power 12.5 Gbps 8-channel advanced linear repeater. The advanced linear repeater is placed in a mid-channel configuration between a PCIe Gen 3.0 graphics card and a compliance base board (CBB) and tested for jitter, eye mask, and TX preset compliance. The results demonstrate the excellent signal conditioning performance of TI's advanced linear repeaters, including TX FIR transparency, low additive jitter, violation-free eye mask, and compliant preset ratios. This report shows TI's advanced linear repeaters are an ideal solution to leverage PCIe root complex and end point FIR settings while extending the total channel reach with high-performance equalization.

Topic **Page**

1 Introduction

The testing carried out in this report is performed on the DS125BR820 low-power 12.5 Gbps 8-channel repeater which is designed to support PCIe Gen 3.0, 40GbE (40G-CR4/KR4/SR4/LR4), and other applications up to 12.5 Gbps. The linear nature of the DS125BR820's equalization allows the root complex (RC) and end point (EP) to freely negotiate transmit equalizer coefficients during link training. In addition, low additive jitter and transparency of transmit FIR wave shape allows the DS125BR820 to support PCIe Gen 3.0 systems. The test results presented in this report are representative of all TI's advanced linear repeaters supporting PCIe Gen 3.0, including DS80PCI810, DS125BR111, and DS125BR401A (A channels only).The PCIe compliance test setup used in this report is shown in Figure 1.

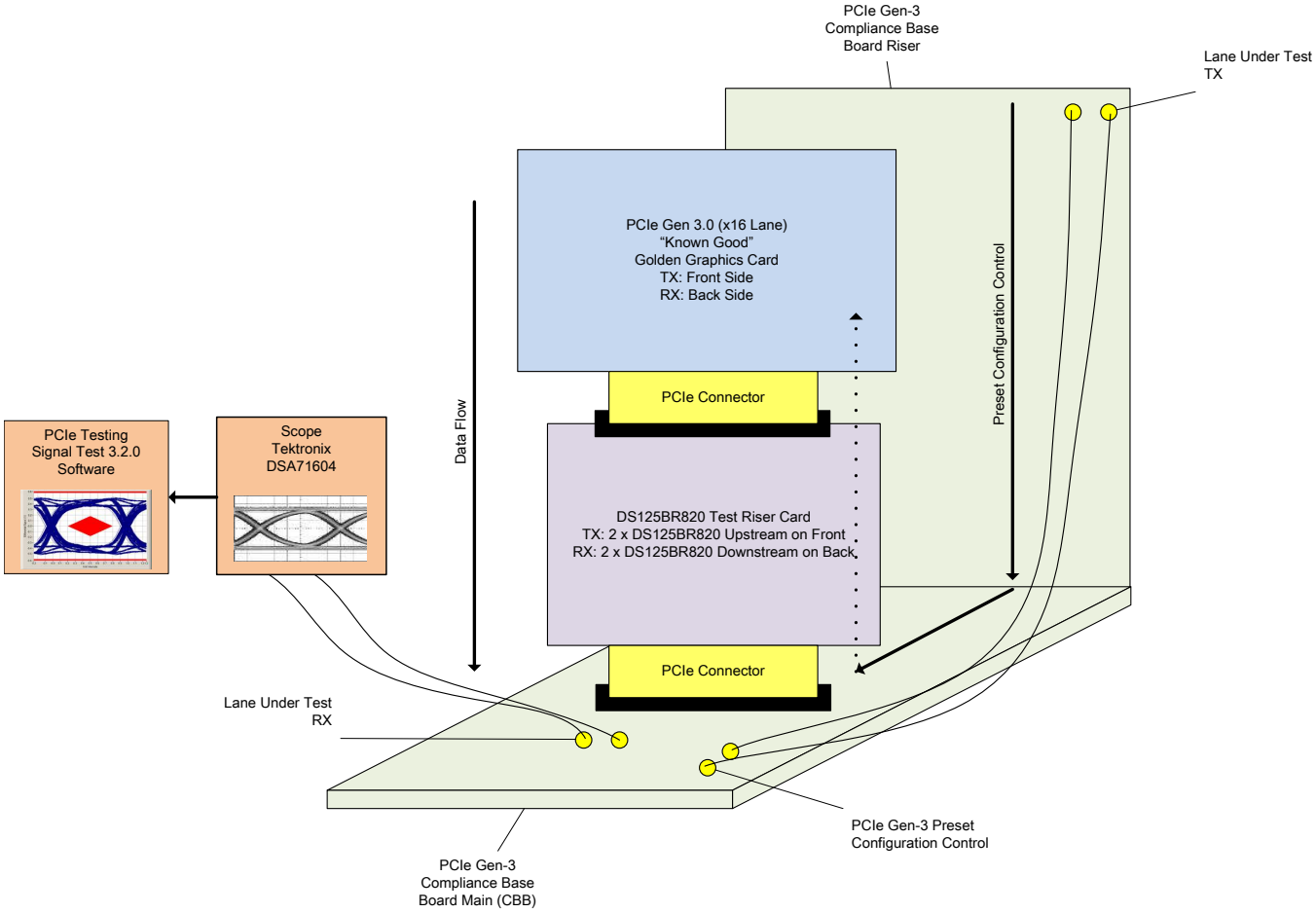


Figure 1. PCIe Compliance Test Setup With DS125BR820 Repeater

2 Advanced Linear Repeater Device Configuration

The DS125BR820 is configured to operate in pin mode with the voltage output differential (VOD) set to Level 6, which is the maximum VOD setting possible in pin mode. VOD Level 6 provides the highest degree of linearity between the input and output. The equalization is configured to the lowest level (EQ Level 1) since the DS125BR820 is located at a close proximity to the PCIe Gen 3.0 graphics card. The RXDET pin is set to the "Float" condition allowing auto-detection of the downstream/upstream receiver's termination.

Table 1. DS125BR820 Settings Used for Testing

EQ SETTING		VOD SETTING		RXDET	
VALUE	PIN STRAP	VALUE	PIN STRAP	VALUE	PIN STRAP
Level 1	0: 1 kΩ to GND	Level 6	VODA1 = VODB1 = 1 (1 kΩ to VIH) VODA0 = VODB0 = 0 (1 kΩ to GND)	Auto termination detection	F: Floating

3 Parametric Compliance With Advanced Linear Repeater

The data in Table 2 through Table 4 are extracted using the PCI-SIG SIGtest 3.2.0 software package. The signal integrity limits are described in the PCIe base specification section 4.3.3.13 and PCIe CEM specification sections 4.8.3, 4.8.2, and 4.8.1. The results show the system is passing PCIe Gen 3.0 signal integrity compliance tests at 2.5 Gbps, 5 Gbps, and 8 Gbps, respectively.

Table 2. DS125BR820 Parametric Results at 2.5 Gbps

Sigtest	2.5 Gbps Default
Overall sigtest result	Pass!
Mean unit interval (ps)	400.026007
Max unit interval (ps)	400.028876
Minimum unit interval (ps)	400.02287
Minimum time between crossovers (ps)	394.249166
Data rate (Gb/s)	2.499837
Per edge RMS jitter (ps)	9.250099
Mean median-to-peak jitter (ps)	30.442272
Max median-to-peak jitter (ps)	39.936779
Minimum median-to-peak jitter (ps)	25.782506
Mean peak-to-peak jitter (ps)	41.950994
Max peak-to-peak jitter (ps)	55.056088
Minimum eye width (ps)	344.973912
Minimum peak-to-peak jitter (ps)	36.186794
Minimum transition eye voltage (V)	–0.528
Maximum transition eye voltage (V)	0.5232
Composite eye height	0.514
Composite eye location	0.5
Minimum transition eye voltage margin above eye (V)	0
Minimum transition eye voltage margin below eye (V)	0
Minimum transition eye height (V)	0.514

Table 3. Parametric Results at 5 Gbps

Sigtest	5 Gbps/ 3.5 dB	5 Gbps/ 6 dB
Overall sigtest result	Pass!	Pass!
Mean unit interval (ps)	200.013	200.014
Minimum time between crossovers (ps)	194.598	194.318
Data rate (Gb/s)	5.000	5.000
Max peak-to-peak jitter (ps)	39.550	47.379
Total jitter at BER of 10E–12 (ps)	51.142	60.350
Minimum eye width (ps)	148.858	139.650
Deterministic jitter delta-delta jitter (ps)	11.224	20.226
Random jitter (RMS)	2.839	2.854
Minimum transition eye voltage (V)	–0.451	–0.446
Maximum transition eye voltage (V)	0.451	0.444
Minimum non-transition eye voltage (V)	–0.430	–0.389
Maximum non-transition eye voltage (V)	0.422	0.391
Composite eye height	0.622	0.474
Composite eye location	0.500	0.500
Minimum transition eye voltage margin above eye (V)	0.158	0.196
Minimum transition eye voltage margin below eye (V)	–0.165	–0.212
Minimum transition eye height (V)	0.703	0.714
Minimum non-transition eye voltage margin above eye (V)	0.120	0.106
Minimum non-transition eye voltage margin below eye (V)	–0.122	–0.108
Minimum non-transition eye height (V)	0.622	0.474

Table 4. Parametric Results at 8 Gbps

Sigtest	Preset 0	Preset 1	Preset 2	Preset 3	Preset 4	Preset 5	Preset 6	Preset 7	Preset 8	Preset 9	Preset 10
Overall sigtest result	Pass!	Pass!	Pass!	Pass!	Pass!	Pass!	Pass!	Pass!	Pass!	Pass!	Pass!
Mean unit interval (ps)	125.009	125.009	125.009	125.009	125.009	125.009	125.009	125.009	125.009	125.009	125.009
Minimum time between crossovers (ps)	103.747	102.102	101.657	99.746	96.609	104.313	103.616	106.528	107.018	107.702	106.483
Data rate (Gb/s)	7.999	7.999	7.999	7.999	7.999	7.999	7.999	7.999	7.999	7.999	7.999
Max peak-to-peak jitter (ps)	41.982	34.513	35.779	29.913	34.530	33.297	34.705	40.480	37.045	39.537	45.913
Total jitter at BER of 10E–12 (ps)	42.241	34.064	36.182	30.021	33.913	33.068	33.225	40.147	37.016	39.212	45.487
Minimum eye width (ps)	82.759	90.936	88.818	94.979	91.087	91.932	91.775	84.853	87.984	85.788	79.513
Deterministic jitter delta-delta jitter (ps)	34.722	27.095	28.850	23.201	27.383	26.387	26.622	32.727	29.967	32.198	37.752
Random jitter (RMS)	0.535	0.496	0.522	0.485	0.464	0.475	0.470	0.528	0.501	0.499	0.550
Minimum transition eye voltage (V)	–0.177	–0.189	–0.190	–0.190	–0.198	–0.185	–0.176	–0.163	–0.163	–0.150	–0.142
Maximum transition eye voltage (V)	0.170	0.183	0.184	0.184	0.198	0.185	0.176	0.158	0.159	0.147	0.139
Minimum non-transition eye voltage (V)	–0.175	–0.189	–0.193	–0.192	–0.201	–0.191	–0.178	–0.163	–0.163	–0.152	–0.142
Maximum non-transition eye voltage (V)	0.171	0.184	0.186	0.187	0.200	0.187	0.178	0.157	0.158	0.150	0.139
Composite eye height	0.116	0.134	0.133	0.139	0.137	0.147	0.135	0.124	0.131	0.119	0.091
Composite eye location	0.448	0.444	0.444	0.436	0.464	0.448	0.464	0.500	0.480	0.452	0.480
Minimum transition eye voltage margin above eye (V)	0.039	0.044	0.044	0.046	0.045	0.049	0.042	0.037	0.039	0.036	0.026
Minimum transition eye voltage margin below eye (V)	–0.043	–0.047	–0.046	–0.049	–0.044	–0.050	–0.045	–0.041	–0.043	–0.034	–0.027
Minimum transition eye height (V)	0.132	0.142	0.141	0.145	0.139	0.149	0.137	0.129	0.132	0.120	0.103
Minimum non-transition eye voltage margin above eye (V)	0.043	0.053	0.050	0.054	0.054	0.064	0.058	0.049	0.052	0.042	0.026
Minimum non-transition eye voltage margin below eye (V)	–0.042	–0.051	–0.050	–0.052	–0.056	–0.063	–0.056	–0.052	–0.053	–0.039	–0.031
Minimum non-transition eye height (V)	0.135	0.154	0.151	0.156	0.160	0.177	0.163	0.151	0.155	0.131	0.108
CTLE equalization index	7	6	7	5	3	4	3	7	5	3	7

4 Eye Diagrams With Advanced Linear Repeater

The data in the following sections show eye diagram test results for 2.5 Gbps, 5 Gbps, and 8 Gbps as analyzed by the PCI-SIG SIGtest 3.2.0 software package and the PCIe CEM specification requirements. For more details, see sections 4.8.1, 4.8.2, and 4.8.3 of the PCIe CEM 3.0 specification.

4.1 Eye Diagram at 2.5 Gbps

Table 5. Eye Requirements at 2.5 Gbps

Parameter	Min	Max	Unit
Differential Peak to Peak Voltage	514	1200	mVp-p
De-Emphasized Differential Peak to Peak Voltage	360	1200	mVp-p
Minimum Eye Width	287		ps
Median-to-Max Jitter Outlier		56.6	ps

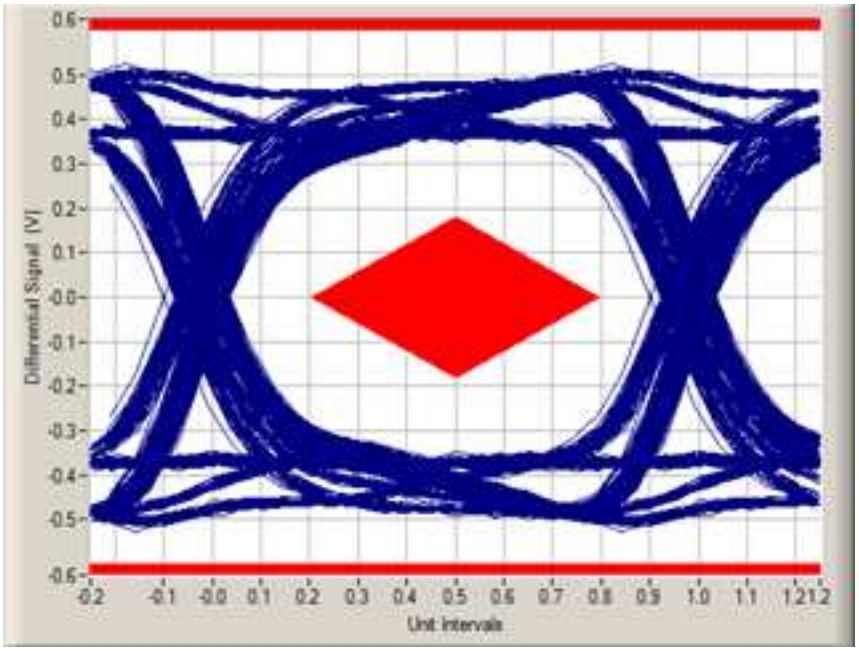


Figure 2. Default Eye Diagram at 2.5 Gbps

4.2 Eye Diagrams at 5 Gbps

Table 6. Eye Requirements at 5.0 Gbps at 3.5 dB De-emphasis

Parameter	Min	Max	Unit
Differential Peak to Peak Voltage	380	1200	mVp-p
De-Emphasized Differential Peak to Peak Voltage	380	1200	mVp-p
Minimum Eye Width with Crosstalk	123		ps
Minimum Eye Width without Crosstalk	126		ps

Table 7. Jitter Requirements at 5.0 Gbps at 3.5 dB De-emphasis

Condition	Max Rj (ps RMS)	Max Dj (ps)	Tj at BER 10E-12 (ps)
With Crosstalk	1.4	57	77
Without Crosstalk	1.4	54	74

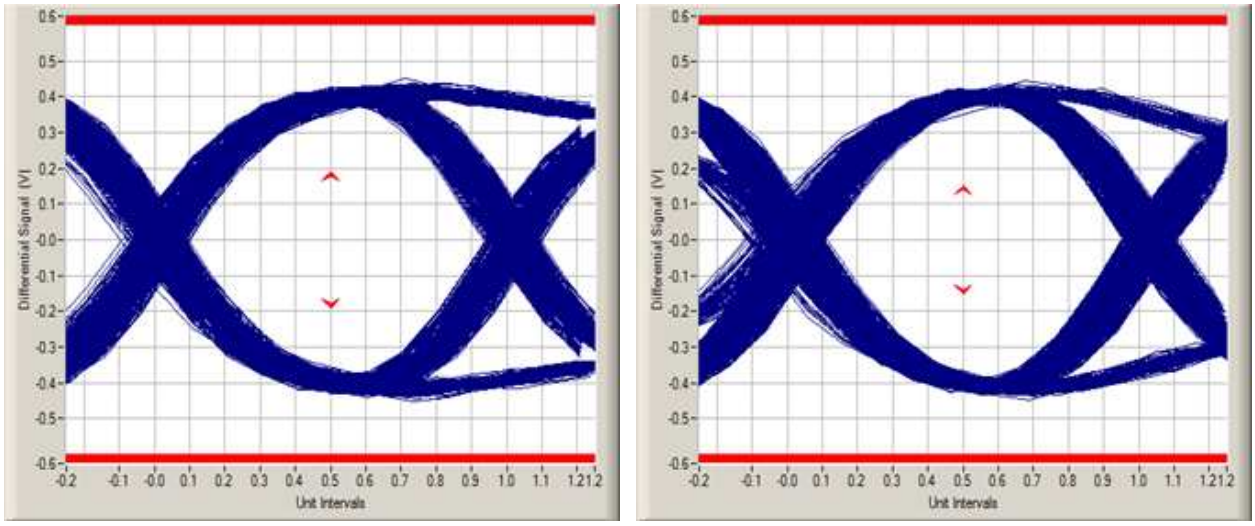
Table 8. Eye Requirements at 5.0 Gbps at 6.0 dB De-emphasis

Parameter	Min	Max	Unit
Differential Peak to Peak Voltage	306	1200	mVp-p
De-Emphasized Differential Peak to Peak Voltage	260	1200	mVp-p
Minimum Eye Width with Crosstalk	123		ps
Minimum Eye Width without Crosstalk	126		ps

Table 9. Jitter Requirements at 5.0 Gbps at 6.0 dB De-emphasis

Condition	Max Rj (ps RMS)	Max Dj (ps)	Tj at BER 10E-12 (ps)
With Crosstalk	1.4	57	77
Without Crosstalk	1.4	54	74

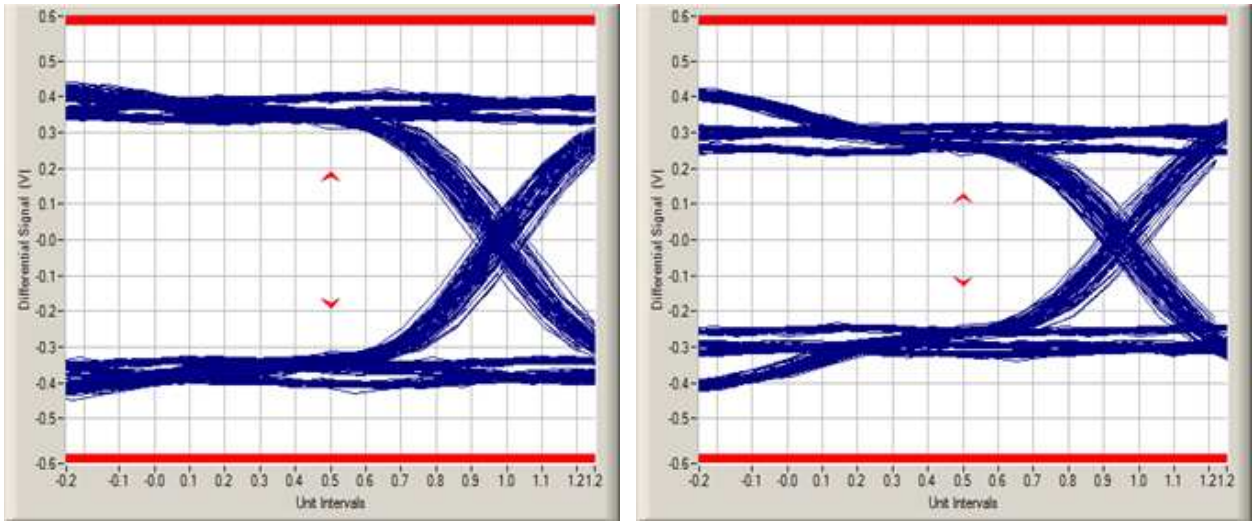
4.2.1 Transition Eye Diagrams at 5 Gbps



With 3.5-dB De-Emphasis With 6-dB De-Emphasis

Figure 3. Transition Eye Diagram at 5 Gbps

4.2.2 Non-Transition Eye Diagrams



With 3.5-dB De-Emphasis With 6-dB De-Emphasis

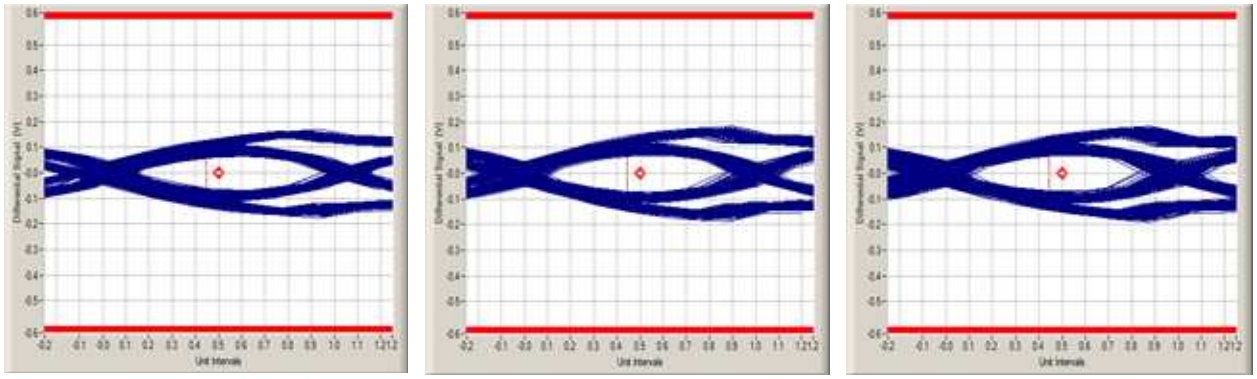
Figure 4. Non-Transition Eye Diagram at 5 Gbps

4.3 Eye Diagrams at 8 Gbps

Table 10. Eye Requirements at 8.0 Gbps

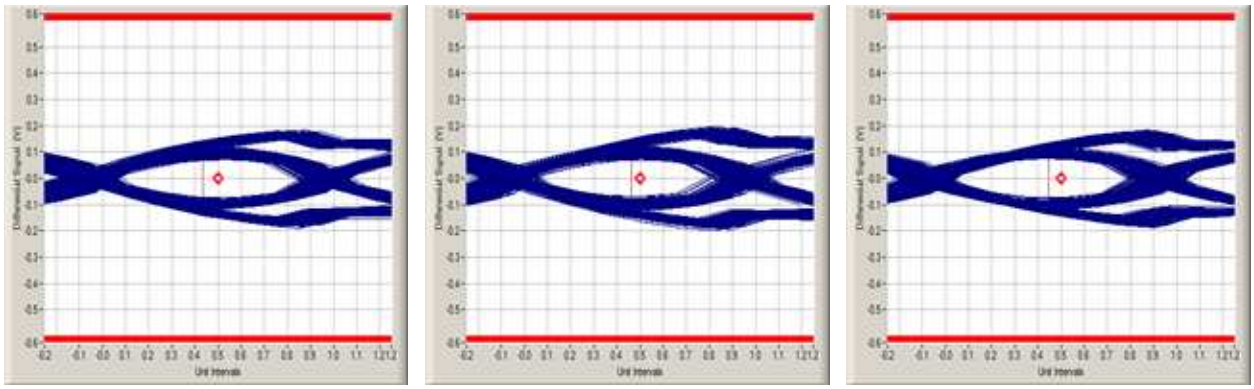
Parameter	Min	Max	Unit
Differential Peak to Peak Voltage	34	1200	mVp-p
De-Emphasized Differential Peak to Peak Voltage	34	1200	mVp-p
Minimum Eye Width	41.25		ps

4.3.1 Transition Eye Diagrams at 8 Gbps Using Preset 0 Through 10



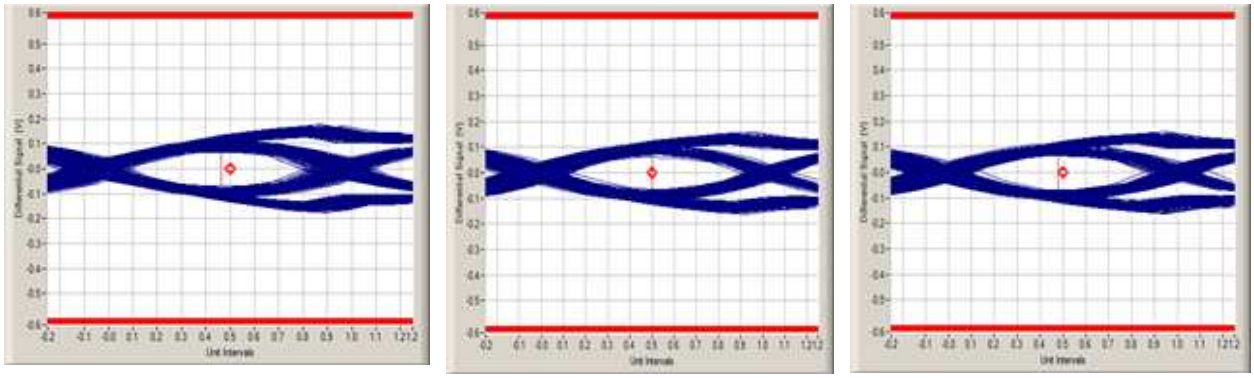
Preset 0 Preset 1 Preset 2

Figure 5. Transition Eye Diagrams



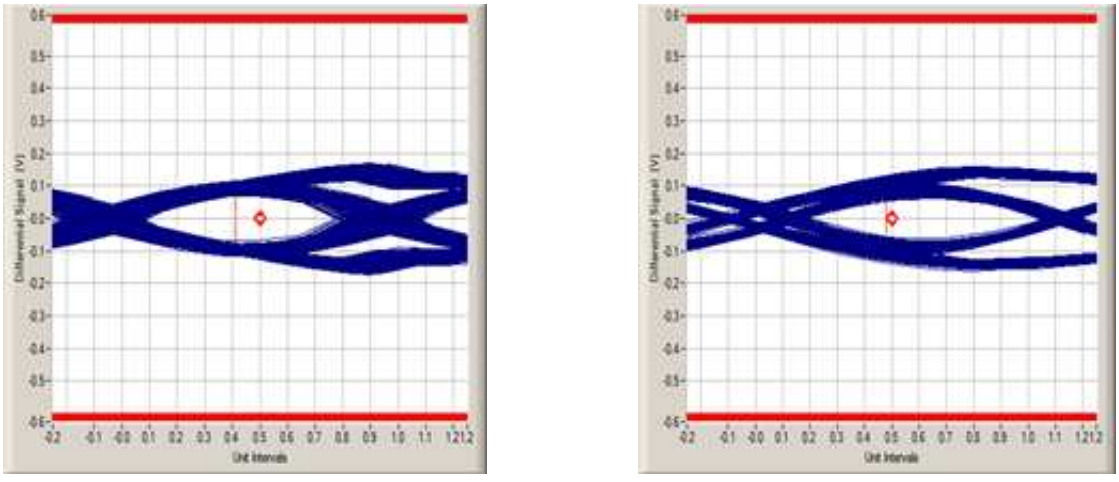
Preset 3 Preset 4 Preset 5

Figure 6. Transition Eye Diagrams



Preset 6 Preset 7 Preset 8

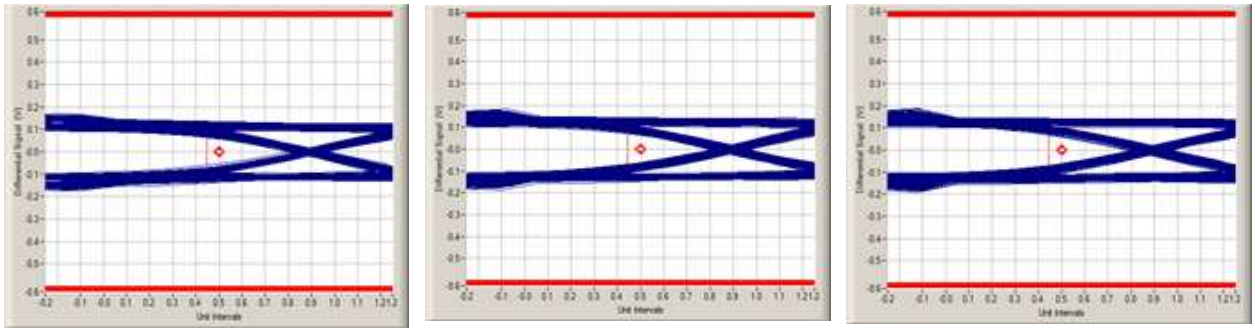
Figure 7. Transition Eye Diagrams



Preset 9 Preset 10

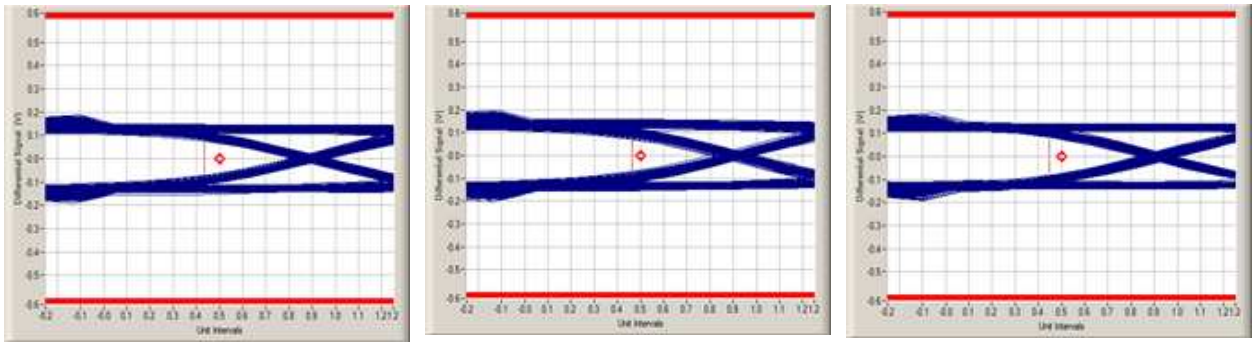
Figure 8. Transition Eye Diagrams

4.3.2 Non-Transition Eye Diagrams at 8 Gbps Using Preset 0 Through 10



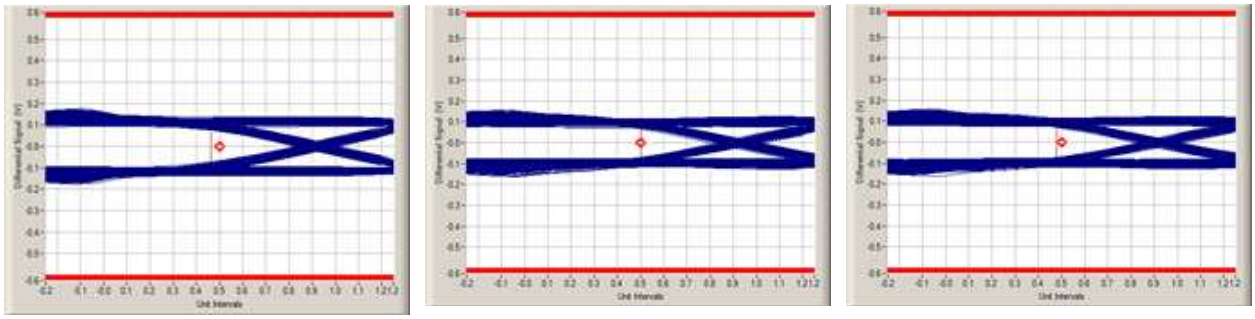
Preset 0 Preset 1 Preset 2

Figure 9. Non-Transition Eye Diagrams



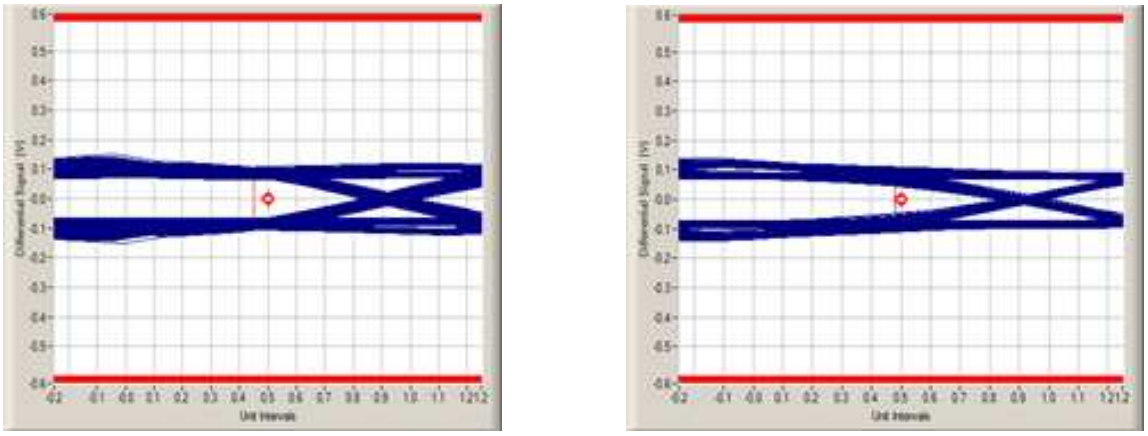
Preset 3 Preset 4 Preset 5

Figure 10. Non-Transition Eye Diagrams



Preset 6 Preset 7 Preset 8

Figure 11. Non-Transition Eye Diagrams



Preset 9 Preset 10

Figure 12. Non-Transition Eye Diagrams

5 Preset Testing With and Without the Advanced Linear Repeater

Table 11 defines the presets from section 4.3.3.5.2 of the PCI Express Base Specification 3.0. Figure 13 shows the preset results with the advanced linear repeater inserted in the data path. Figure 14 shows the preset results for the golden graphics card without the DS125BR820. The difference between Preset 1 for the golden graphics card versus Preset 1 with the DS125BR820 is approximately 0.7 dB. Table 12 summarizes the delta observed when using Preset 1 and Preset 9 with and without the DS125BR820 inserted.

It is normal to expect some change in the measured preset de-emphasis and preshoot values when comparing the source output directly versus the output of the DS125BR820 repeater plus some channel. The advanced linear repeaters devices do not create de-emphasis or preshoot on their own. Rather, TI's advanced linear repeaters are designed to be transparent to the de-emphasis and preshoot present at their input with minimum distortion through the repeater. This transparency evident in Figure 13 and Figure 14 makes TI's advanced linear repeaters an ideal candidate for systems that rely heavily on the root complex and endpoint de-emphasis and preshoot capabilities.

Table 11. Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1	0.0	-0.166	0.000	0.688	0.688	1.000
P8	3.5 ± 1	-3.5 ± 1	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1	-6.0 ± 1.5	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5	0.000	-0.200	1.000	0.600	0.600
P10	0.0	See Note(1)	0.000	See Note(1)	1.000	See Note(1)	See Note(1)

(1) P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. See the PCI Express Base Specification 3.0 for more details.

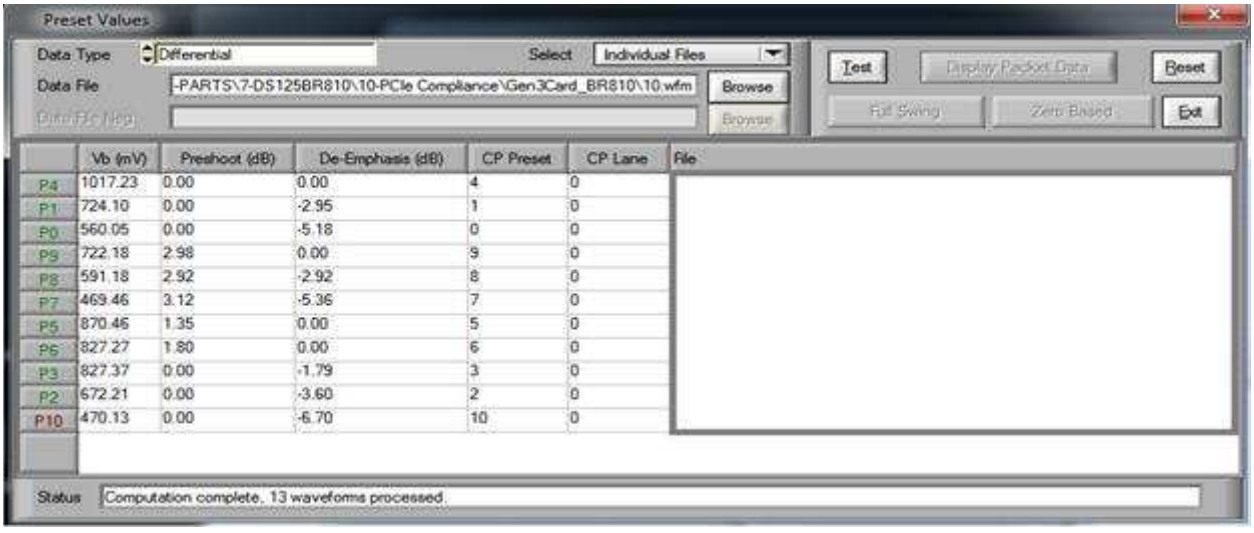


Figure 13. Preset Testing With DS125BR820 Inserted in Data Path

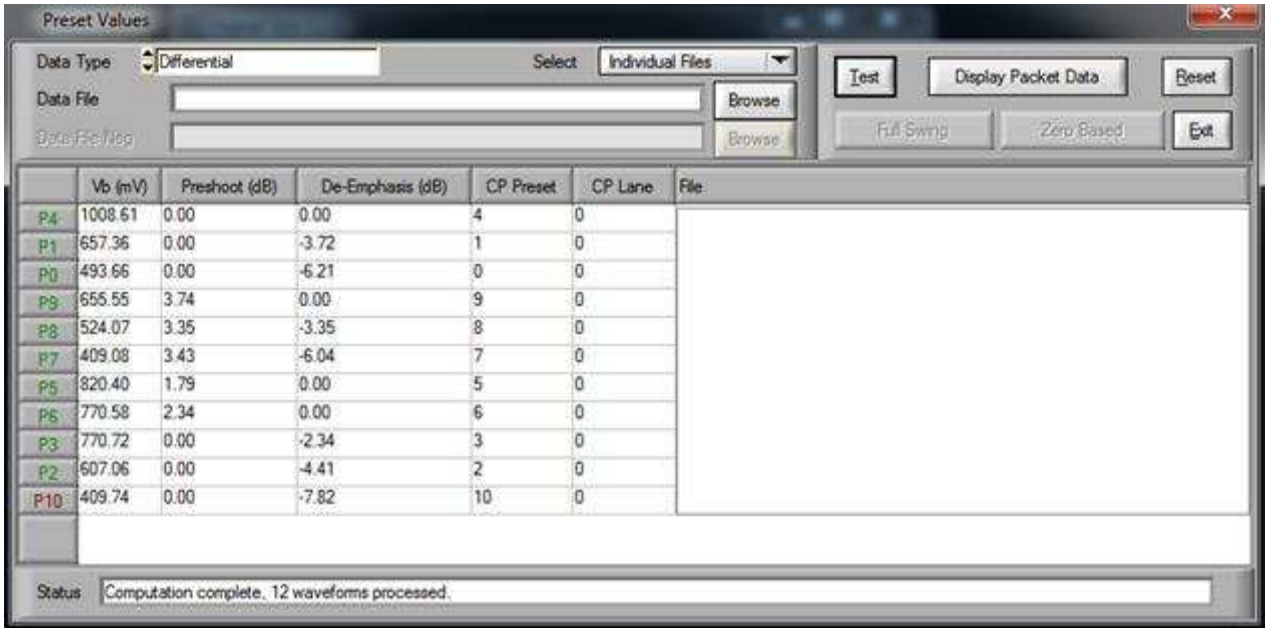


Figure 14. Preset Testing for Golden Graphics Card Only

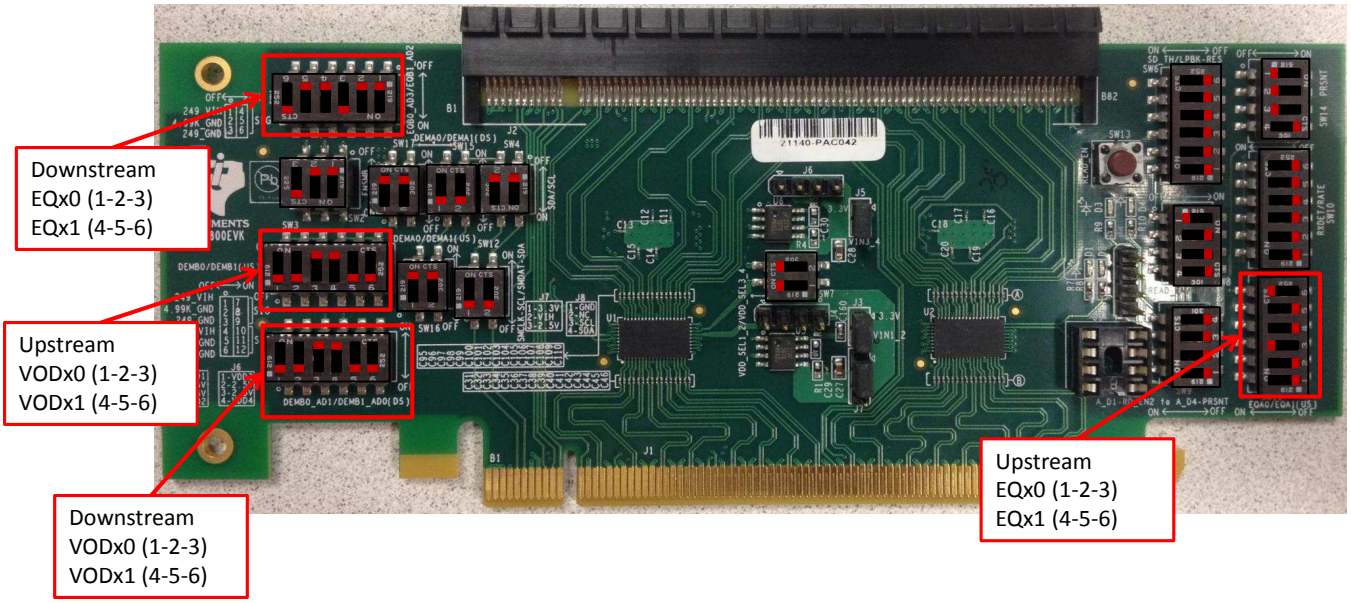
Table 12. Preset Analysis With and Without DS125BR820

	CONDITION	PRESET 1 (De-Emphasis)	PRESET 9 (Preshoot)
1	Graphic card + DS125BR820	–2.95 dB	2.98 dB
2	Graphics card only	–3.72 dB	3.74 dB
	Delta between condition 1 and condition 2	0.77 dB	0.76 dB

6 Conclusions

The tests in this report demonstrate compliance to PCIe Gen 3.0 add-in card CEM specifications with TI's advanced linear repeater used as a mid-channel repeater. The advanced linear repeater is ideal for PCIe Gen 3.0 applications that require low-additive jitter, preservation of transmit FIR wave shape, and violation-free eye mask. Using the available equalization settings, the advanced linear repeater offers superior link extension while maintaining signal quality and preset transparency.

Appendix A DS125BR820 Riser Board



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