Application Report
SNLA302–November 2018

# High-Speed Layout Guidelines for Reducing EMI for LVDS SerDes Designs

*Ikechukwu Anyiam*

**ABSTRACT**

The purpose of this application note is to provide guidelines on how to reduce EMI in designs that use TI serializers and deserializers.

**Contents**



**List of Figures**



**List of Tables**

## Trademarks



## 1 Introduction

Electromagnetic interference (EMI) is a prevalent issue in systems with parallel interfaces that have multiple high-speed outputs that traverse long distances. Although the use of low voltage differential signaling (LVDS) seriailizers/deserializers (SerDes) helps to reduce the amount of radiated emissions from the link, it does not completely eliminate them. System designers still need to consider EMI prevention early in the design process to avoid future issues.

EMI prevention starts with the printed-circuit board (PCB) layout. Signal integrity issues can lead to radiated emissions, therefore system designers must ensure that the PCB is compliant with the PCB guidelines for high-speed signals. This includes the board stack-up, traces and vias, decoupling capacitors, power and ground planes, and other PCB components.

A good way to ensure that a design is EMI-compliant is to reference the board design of TI evaluation modules (EVMs), but here are some additional considerations designers must take into account before beginning the layout:

- Create a diagram with the functional groups of the system (transmitter path, receiver path, analog

signals, digital signals, and so forth).

- Are there any interconnections between at least two independent functional groups? Take special care of them. Think about the return current and the crosstalk to other traces.
- How many different supply voltages are there? Do they need their own power plane, or is it possible to split them?
- What is the highest frequency and fastest rise time in the system?
- Are there sensitive signals to route? For example, clock signals and impedance controlled signals?
- Clarify the minimum width, separation, and height of a trace with the PCB manufacturer. What is the minimum distance between two layers? What about the minimum drill and the requirements of vias? Is it possible to use blind vias and buried vias?
- Is it possible to use a lower frequency than what is targeted? If so, do so.
- Is it possible to decrease the length of the traces and the cable? If so, do so.

This information will help a lot with the initial design.

The guidelines in the following sections should be closely followed to ensure that a design that uses TI's LVDS SerDes is EMI-compliant.

## 2 PCB Stack-Up and Board Layout

- At minimum, select a PCB with at least four layers. Two layers are for signals while the remaining two are for power and ground.
- Use dedicated ground and power planes.
  - Power and ground planes make an excellent high-frequency capacitor and act as an additional high-frequency bypassing capacitor in complement with discrete components.
- Avoid cutting up the power and ground planes, if possible.
  - Solid planes minimize inductance (a desirable trait for high-speed signals) and act as low impedance paths for return current.
  - If not possible, minimize using power and ground islands and use ground guards when separating two power planes.
- Keep the power and ground plane surface area equivalent in shape and size.
- Keep the power and ground shapes on top of each other for optimal board capacitance.
- Use ground pours on the top and bottom layers. Use evenly-spaced ground pores around differential traces.
- Keep traces as short as possible to reduce trace inductance.
- Place all connectors and external wires on one edge of the PCB.
- Place electrostatic discharge (ESD) susceptible circuitry at the center of the PCB away from the edges of the board, external wires, connectors, and power.
- Properly terminate unused pins of an IC (reference the datasheet).
- Keep single-ended signals away from differential traces – distances should be at least at least 2x the trace width. 5x would be best, but 2x is acceptable.

## 3 LVDS Traces

- As shown in Figure 1, traces should be 100-Ω (±5%) differential impedance of differential microstrip or differential stripline.
  - Microstrip lines are either on the top or bottom layer of a PCB. Microstrip construction consists of a differential pair and a single reference layer (typically ground).
  - Striplines are embedded between two reference layers, which results in a higher capacitance versus microstrip lines. There are generally longer propagation delays compared to microstrip lines.
  - Although striplines require an additional layer which may increase cost, they usually have better EMI and EMC performance.
- The distance between two adjacent LVDS pairs should be greater than or equal to twice the distance

between the two individual conductors of a single LVDS pair.

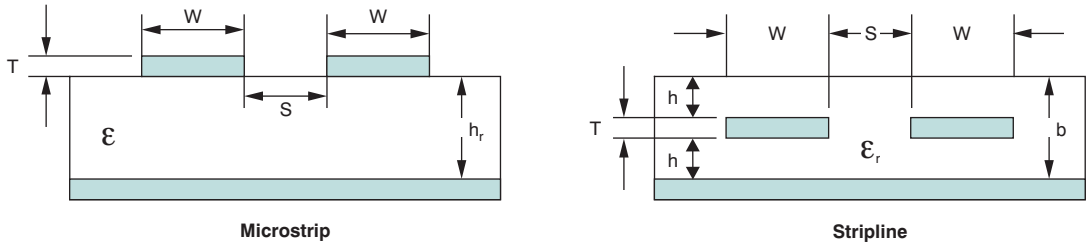


**Figure 1. Physical Geometries of Differential Traces**

- Keep signals within a LVDS pair closely coupled to minimize the noise injection and radiated electromagnetic field from other signals.
  - Maintain equal length on signal traces within a differential pair. As shown in Figure 2, the trace lengths should not deviate even if AC-coupling capacitors are used.
  - Maintain the same distance between signal traces within a LVDS pair across the entire length.

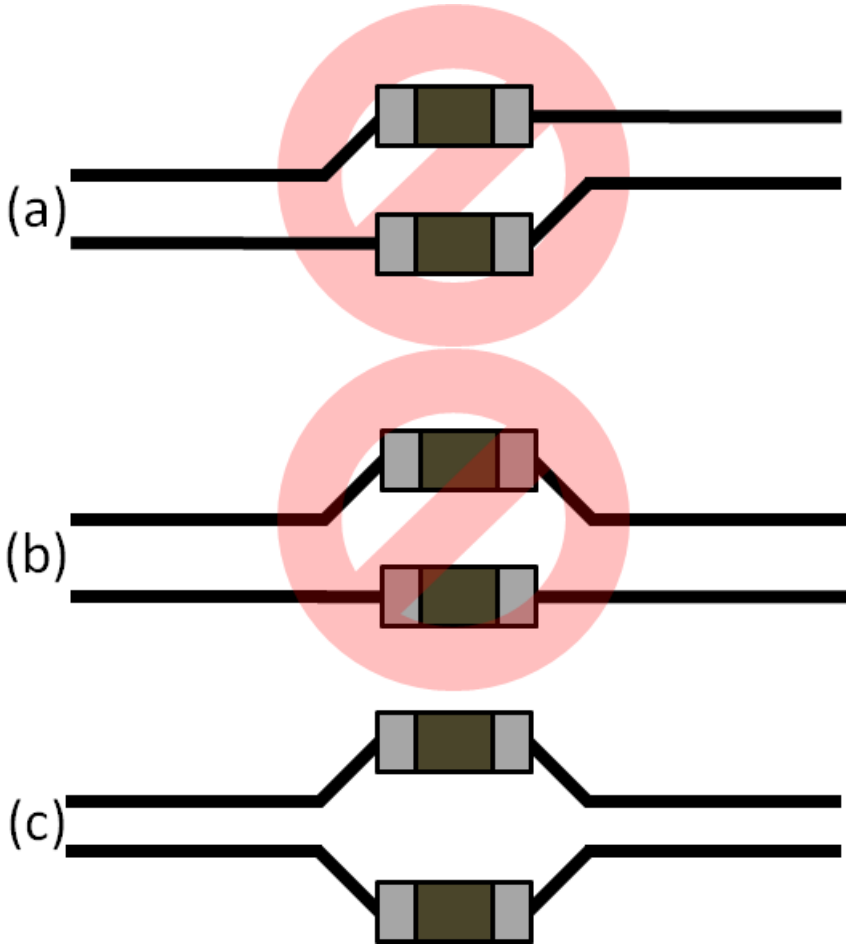


**Figure 2. Differential Pair Symmetry**

- Route the high-speed, LVDS signals with the most direct route and minimum trace length to the connector.
- Minimize stubs and junction taps in order to avoid reflections.
  - Place termination resistors as close as possible to the deserializer input pins to reduce stubs and effectively terminate the differential lines.

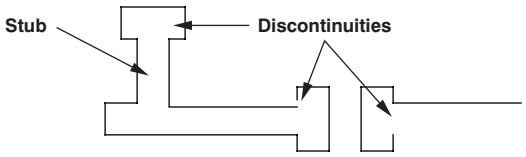


**Figure 3. PCB Trace Stubs and Discontinuities**

- If possible, avoid routing high-speed frequency traces through the vias.
  - The impedance mismatch between vias and signal traces can cause transmission-line reflections.
  - Any discontinuities that occur on one signal line of a differential pair should be mirrored on the other signal line of the LVDS pair.
- Bury longer high-speed traces in an inner signal layer
  - In a four-layer board, the high-speed trace can be on either the second or third layer.
  - Construct high-speed vias with controlled impedance.
- Minimize intra-pair and inter-pair skew.
  - Keep differential skew to ±30 ps by ensuring trace lengths are matched within 5mm of each other.
  - Avoid serpentining one side of the differential pair to match skew. Phase differences between the LVDS lines increase radiation and decrease the eye opening.
  - Trace layout, connectors, and cable wires can cause skew, while strong coupling within LVDS pairs reduces it.
  - If using a shielded twisted-pair (STP) cable, keep the intra-pair skew associated with STP cables in mind.

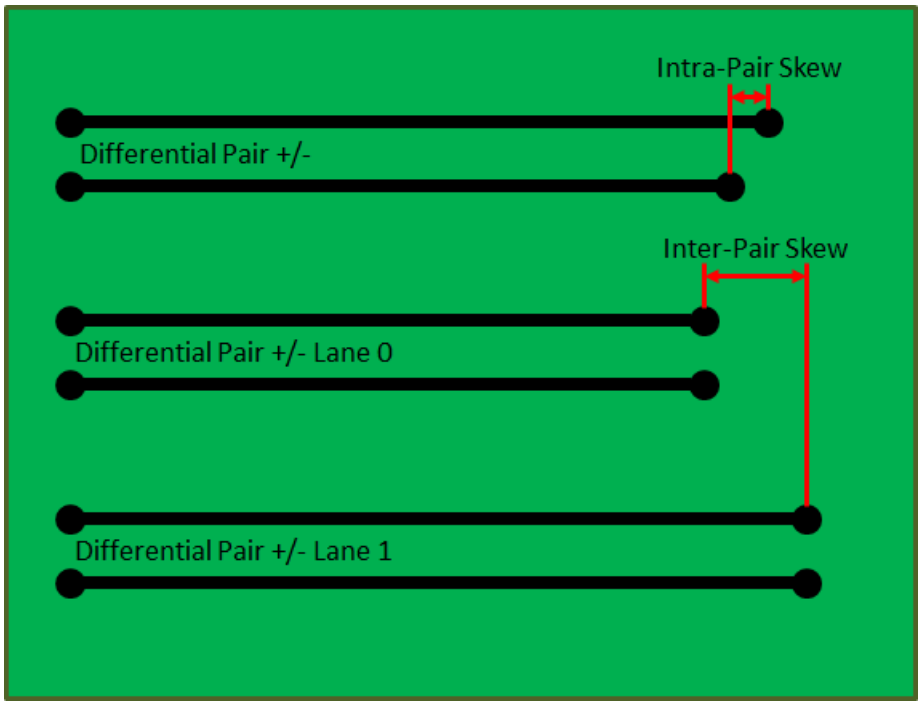


**Figure 4. Intra-Pair and Intra-Pair Skew**

- Use a continuous ground plane underneath the traces.
  - Routing across a plane split or a void in the reference plane forces high-frequency return current to flow around the split or void, which results in excess radiated emissions, degraded signal integrity, interference with adjacent signals, and signal propagation delays.
  - If routing over a plane-split is completely unavoidable, place stitching capacitors across the split to provide a return path for the high-frequency current. These capacitors should be 1 μF or lower and

placed as close to the plane crossing as possible.

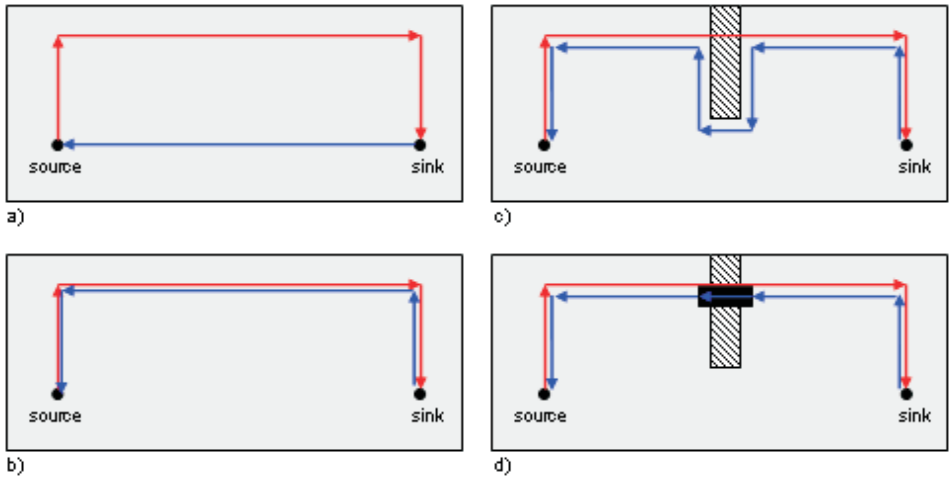


**Figure 5. Return Current and Resulting Loop Area**

- 45-degree corners are acceptable, but rounded corners are best.
  - Avoid asymmetric meanders and do not route traces at right angles to component pins or other traces.
  - Avoid right-angle traces, as they are known to cause more radiation.

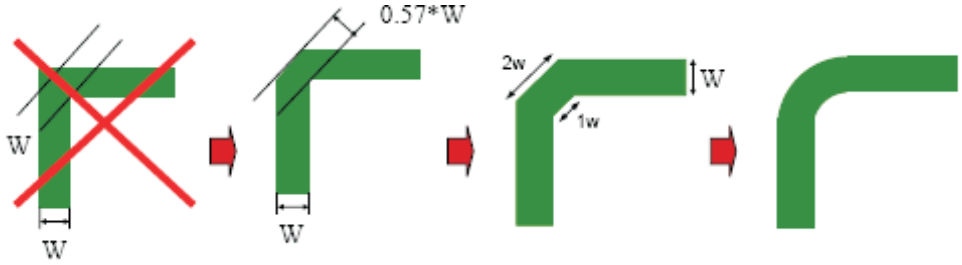


**Figure 6. Poor and Good Right Angle Bends**

- Use small-sized AC-coupling capacitors (0603 or smaller) to minimize pad discontinuity. 0201 decoupling filter capacitors can also be used.
  - Use common-mode chokes near AC-coupling capacitors.
- Do not route high-speed LVDS traces near the edge of the PCB.
- Take care to ensure the LVDS trace impedance matches the differential impedance of the selected physical media.
  - This impedance should also match the value of the termination resistor that is connected across the differential pair at the deserializer's input.
  - Keep the impedance matched across transitions such as connectors. Use a time-domain reflectometer (TDR) to verify.
- Do not place probe or test points on any high-speed differential signals.
- Do not route high-speed traces under or near crystals, oscillators, clock signal generators, switching power regulators, mounting holes, magnetic devices, or integrated circuits (IC) that use or duplicate clock signals.

## 4 Power and Grounding

- Use solid ground planes and avoid vias with transmission lines.
- Separate digital and analog power supplies with filtering and bypassing.
- Put the largest-value filter capacitors near power connector and supply inputs.

- Place high-quality X7R decoupling capacitors close to device pins.
  - Use multiple capacitors (0.1-μF, 0.01-μF, and 1-μF) in parallel to offer low impedance over higher frequency ranges.
  - Place the smallest-value capacitors closest to the power pin.
  - Connect the pad of the capacitor directly to a via to the ground plane. Use two or three vias to get a low-impedance connection to ground.

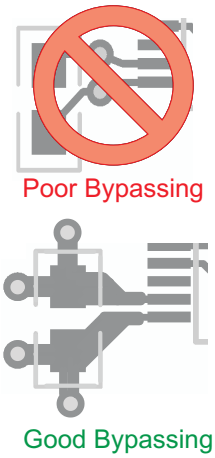


**Figure 7. Poor and Good Placement and Routing of Bypass Capacitors**

- Use a ferrite bead to decouple the IC power from the rest of the supply system.
- Keep the traces from decoupling caps to ground as short and wide as possible.
  - Connect power and ground as soon as possible to the power and ground planes, and use multiple vias to reduce inductance.
  - Ensure that bypass capacitors are on the same layer as the device for best results. Do not place capacitors on the opposite side of the board.
- Do not make ground or power connections with controlled impedance traces. Use wide, low-impedance traces for power and ground.
- Use an inductor or ferrite beads to split power and minimize noise coupling.
- More vias means lower inductance, so use multiple vias for both power and ground connections.
  - Do not place vias between bypass capacitors and the IC.
- Minimize current loops.
  - The return current takes the lowest impedance path.
  - At high frequencies, the return current tends to flow directly beneath the signal path.
  - Current loops in the layout generate noise. This noise can be minimized by keeping loops as small as possible to improve both EMI and ESD performance.
  - A solid ground plane provides a continuous, low-impedance path for return currents of high-speed signals.

## 5 Connectors and Cables

- Keep differential pairs close and monitor their electrical length.
- Use shielded high-speed connectors that have complete shielding around the connector interface.
- When using ribbon cable, place a ground line between each differential pair to act as a barrier to noise coupling between adjacent pairs.
- For twin-coax cable applications, use a shield on each cable pair.
  - All extended point-to-point applications should also employ an overall shield surrounding all cable pairs regardless of the cable type.
  - The overall shield results in improved transmission parameters such as faster attainable speeds,

longer distances between transmitter and receiver, and reduced problems associated with EMI.

– Twin-coax has been demonstrated to have very low cable skew and EMI due to its construction and double shielding.

## 6 Conclusion

Even with the use of LVDS SerDes, EMI issues can still plague poorly designed systems. The guidelines listed in this document should be closely followed to help reduce EMI in LVDS SerDes designs. Referencing TI's EVM schematic and layouts is also recommended to ensure of a good design.

## 7 References


- *An EMC/EMI System-Design and Testing Methodology for FPD-Link III SerDes* (SLYT719)
- *High-Speed Layout Guidelines for Signal Conditioners and USB Hubs* (SLLA414)
- *High-Speed Layout Guidelines* (SCAA082)
- *PCB Design Guidelines for Reduced EMI* (SZZA009)
- *Considerations for PCB Layout and Impedance Matching Design in Optical Modules* (SLLA311)
- *How to Design LVDS SerDes in Industrial Systems* (SLLA422)
- *Low-Voltage Differential Signaling (LVDS) Design Notes* (SLLA014)
- *LVDS Owner's Manual* (SNLA187)
- *LVDS SerDes Gen I PCB and Interconnect Design-In Guidelines* (SNLA008)

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265