Application Report
SNLA131A–July 2011–Revised April 2013

AN-2173 I2C Communication Over FPD-Link III with Bidirectional Control Channel

ABSTRACT

This application note describes communication between devices using the FPD-Link III SerDes with a bidirectional control channel using I²C. The low latency bidirectional control interface allows the master I²C device to remotely control peripherals across the serial link.

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1 I²C Overview

The Inter-Integrated Circuit (I²C) bus is a two-wire bidirectional bus that allows multiple devices to operate on the same bus (Figure 1). The bus consists of master and slave devices which transmit data back and forth over the I²C interface. Master devices control the bus and are typically microcontrollers, FPGAs, DSPs, or other digital controllers. The slave devices are controlled by a host controller. I²C uses a master-slave protocol when data is exchanged among devices. Each device on the bus (both master and slave) can be a receiver and/or transmitter. The bus consists of two wires, the SCL (clock) line, and the SDA (data) line. The two wires are open collector/drain outputs and must be pulled high using an external pull-up resistor. A logic state low is transmitted by driving the output low. A logic high state is transmitted by releasing the output and allowing it to be pulled-up externally. The appropriate pull-up resistor values will depend upon the total bus capacitance and operating bus speed.

The I²C bus is a two-wire serial interface. These wires convey information to and from devices connected to the bus, each of which is identified by a unique address. Each device can either transmit data or receive data. A device can operate as either a master or as a slave; depending on whether it generates or receives the serial clock (SCL). A master initiates a data transfer by addressing slave device and generates START and STOP signals. The I²C protocol allows for more than two devices to be connected to the bus and for multiple master/slave relationships to exist.

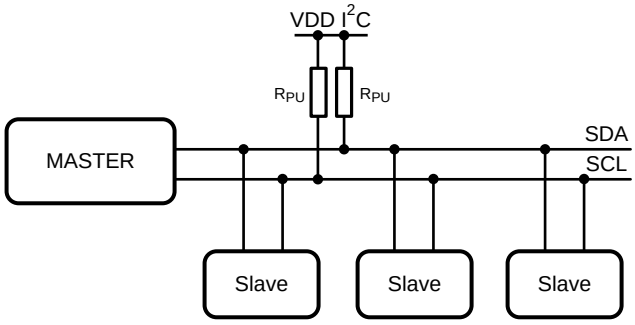

Figure 1. Example of I²C Bus

2 Acknowledge From Slave Device

To communicate with a particular device on the bus, the controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an “Acknowledge” (ACK = 1) or “No Acknowledge” (NACK = 0). The Acknowledge cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device. All bytes transmitted on the SDA line consists of eight bits of data followed by an Acknowledge bit. Each byte transferred effectively requires 9 bits. The ACK bit allows data to be sent in one direction to one device on the bus, and to indicate the data was received. A device acknowledges a transfer of each byte by pulling the SDA line low during the 9th clock pulse of SCL.

ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it is ready to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and terminates with a stop condition on the bus.

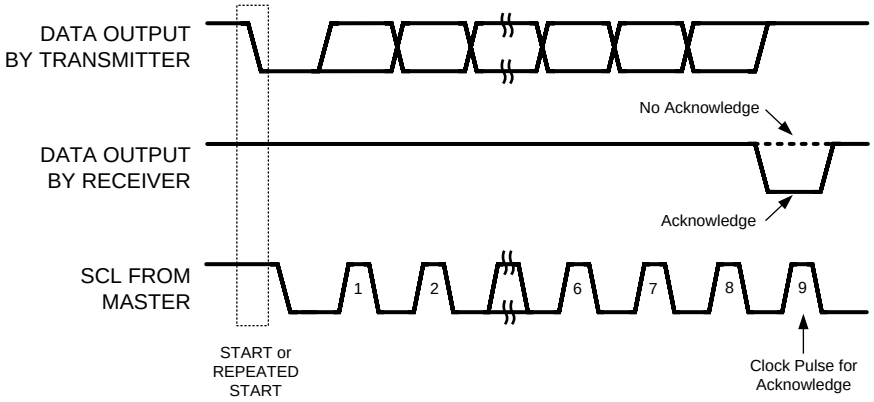

Figure 2. Acknowledge On The I²C Bus

3 Clock Stretching

In general, the I²C master controls the SCL clock line. This line provides timing of all transfers on the bus. When the master is reading from the slave, the slave sends data on the SDA line, but it is the master that controls the clock. However, there are situations where a slave device(s) is not ready to respond to the master or needs to slow down bus traffic. The I²C protocol defines a mode for the slave to hold the SCL line Low. This mechanism is known as “Clock Stretching”. When the slave receives the write/read command from the master it holds the clock line Low. During any SCL low period, the slave holds down SCL to prevent it from rising high again to delay the SCL clock rate and pause communication.

When the master attempts to make SCL high to complete the current clock pulse, it should verify that SCL has really gone high. If it is still low, this indicates a slave is holding SCL low and the master must wait until SCL goes high before continuing

4 Bidirectional Control Channel Using I²C

The FPD-Link III Serializer/Deserializer (SerDes) chipsets support full-duplex transmission of high-speed video data and an embedded a bidirectional control channel (referred as BCC) concurrently over a single differential link. The BCC interface is I²C compliant according to the I²C standard. The BCC interface provides access to programmable functions and registers on the local and remote device(s). Three types of operations are supported for I²C transactions with the bidirectional control channel SerDes chipsets: local, remote, and remote slave as shown in Figure 3. Each device can function as an I²C slave proxy or master proxy depending on the I²C mode of operation. The SerDes interface acts as a virtual bridge between host controller and the remote device. Local operations use standard master to slave operations to the local Serializer or Deserializer. Local I²C operations do not require any clock stretching by the slave and do not result in transactions across the bidirectional control link. When addressing a remote peripheral or SerDes, the slave proxy will forward any byte transactions sent by the Master controller to the target device. The device will function as a master proxy device; acts as a master on behalf of the I²C host controller.

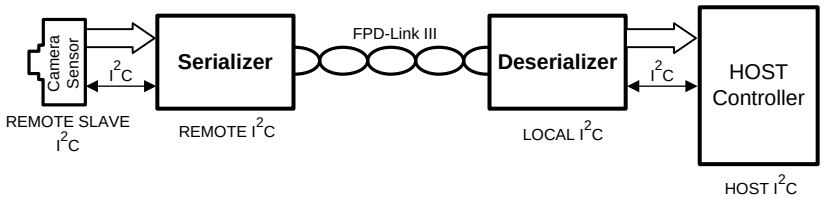

Figure 3. Typical FPD-Link III Connection with I²C Bus

In order to communicate with remote devices on the I²C bus through the bidirectional control channel, slave clock stretching must be supported by the I²C host controller. The chipsets with a bidirectional control channel employ I²C clock stretching during remote data transmission; as described in the CLOCK STRETCHING section. During this phase, the control channel is embedded on the link and then data is reconstructed on the remote bus. Note the slave device will not control the clock and only stretches it until the remote peripheral has responded.

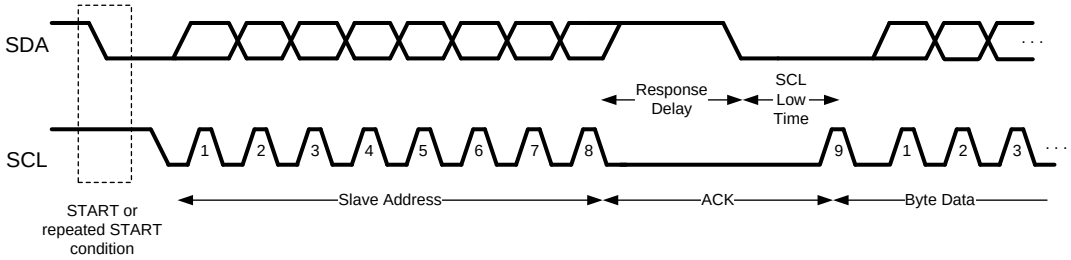

Figure 4. Clock Stretch For Sent Byte

Figure 4 shows an example of a remote access including the clock stretching period following the transmitted byte, prior to completion of the acknowledge bit. Since each byte transferred to the I²C slave must be acknowledged separately, the clock stretching will be done for each byte sent by the host controller. For remote accesses, the “Response Delay” shown is on the order of 5 – 10 us and 10 – 15 us for DS90UH925Q/UH926Q/UB925Q/UB926Q and DS90UB901Q/902Q/903Q/904Q respectively. The “Response Delay” includes the latency time of the control channel packing and serialization protocol across the differential link to the remote peripheral. The following diagrams (*Figure 5 Figure 6*) show the timing relationships of the SCL clock and SDA data signals.

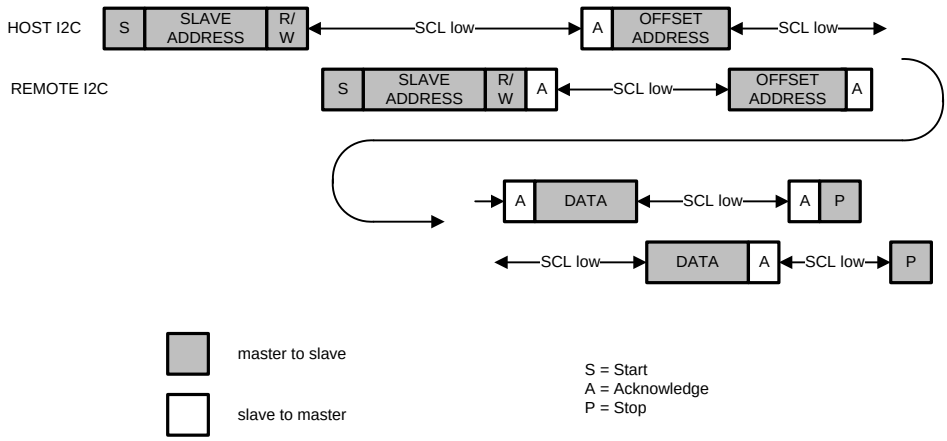

Figure 5. Write Format To Remote I²C Slave

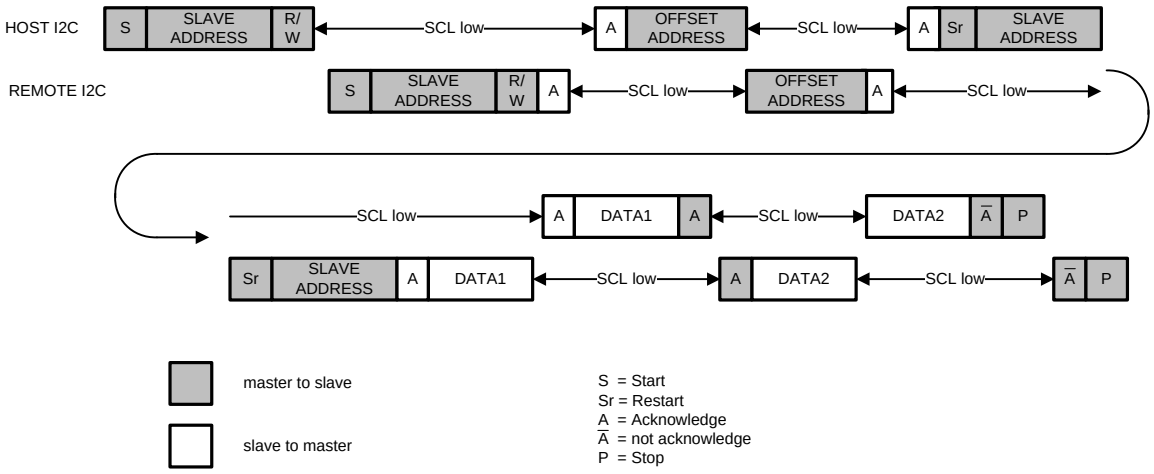

Figure 6. Combined Format Read From Remote I²C Slave

5 Data Throughput To Remote I²C Slaves

Since the BCC buffers each I²C data byte and regenerates the I²C protocol on the remote side of the link, the overall I²C throughput will be reduced. The reduction is dependent on the operating frequencies of the local and remote interfaces. The local I²C rate is based on the host controller clock rate, while the remote rate depends on the settings for the proxy I²C master (SCL frequency).

For purposes of understanding the effects of the BCC on data throughput from a host controller to a remote I²C master, the approximate bit rate including latency timings across the control channel can be calculated by the following:

$$9 \text{ bits} / ((\text{Host\_bit} * 9) + (\text{Remote\_bit} * 9) + \text{FCdelay} + \text{BCCdelay}) \quad (1)$$

Example of DS90UH925Q/926Q/UB925Q/UB926Q chipset:

For the 100 kbit/s (100 kHz) :

Host_bit = 10us (100 kHz)

Remote_bit = 13.5us (default 74 kHz)

FCdelay = 1us (max)

BCCdelay = 9us (typical value)

Effective rate = 9bits / (90us + 121us + 1us + 9us) = 40.6 kbit/s

Table 1. Typical Achievable Bit Rates

FPD-Link III SerDes	Host I²C rate	Remote I²C Rate	Net bit rate
DS90UH925Q/926Q DS90UB925Q/926Q	100 kbit/s	74 kbit/s (default settings)	40.6 kbit/s
	100 kbit/s	100 kbit/s	47.4 kbit/s
	400 kbit/s	100 kbit/s	73.5 kbit/s
	400 kbit/s	400 kbit/s	163.6 kbit/s
DS90UB901Q/902Q DS90UB903Q/904Q	100 kbit/s	100 kbit/s (default settings)	46.6 kbit/s
	100 kbit/s	75 kbit/s	40.4 kbit/s
	50 kbit/s	100 kbit/s	31.8 kbit/s
	25 kit/s	100 kbit/s	19.4 kbit/s

Since the I²C protocol includes overhead for sending address information as well as START and STOP bits, the actual data throughput depends on the size and type of transactions used. Use of large bursts to read and write data will result in higher data transfer rates.

6 Conclusion

This application note provides an overview of the I²C bus along with details describing the interface between FPD-Link III chipsets with a bidirectional control channel and I²C peripherals.

7 References

1. NXP UM102104, I²C-bus specification and user manual, Rev. 03 - 19 June 2007
2. DS90UB901Q/DS90UB902Q 10 - 43MHz 14 Bit Color FPD-Link III Serializer and Deseri (SNLS322)
3. DS90UB903Q/DS90UB904Q 10 - 43MHz 18 Bit Color FPD-Link III Serializer and Deseri (SNLS332)
4. DS90UH925Q 720p 24-bit Color FPD-Link III Serializer with HDCP (SNLS336)
5. DS90UH926Q 720p 24-bit Color FPD-Link III Deserializer with HDCP (SNLS337)
6. DS90UB925Q DS90UB925Q 5-85 MHz 24-bit Color FPD-Link III Serializer w/BCC(SNLS407)
7. DS90UB926Q DS90UB926Q 5-85 MHz 24-bit Colr FPD-Link III Desrializr w/ Bidirectionl Ctrl Chl (SNLS422)

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