Application Report
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Migrating DS90UB914A-Q1 Designs to DS90UB934-Q1 for Automotive ADAS Systems

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ABSTRACT

This application report details areas to be considered when upgrading an existing design using TI's DS90UB914A-Q1 FPD-Link III deserializer to TI's DS90UB934-Q1 deserializer for Automotive ADAS systems.

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Trademarks

1 Feature Summary

There are a number of benefits to migrate from DS90UB914A to DS90UB934. A feature comparison is shown in Table 1

Table 1. Feature comparison between DS90UB934 and DS90UB914A

PARAMETER	DS90UB934	DS90UB914A	NOTES
Maximum PCLK frequency (MHz)	12-bit: 100 MHz	12-bit: 75 MHz	Increased maximum frequency
Equalization	Adaptive EQ	Adaptive EQ	Increased channel loss margin by 3 dB
Maximum I2C data rate	1 MHz	400 KHz	Faster control channel/back channel speeds
Programmable interrupt functionality (INTB)	Yes	No	Additional control pin for serializer and deserializer monitoring
Power over coax (PoC)	Yes	Yes	—
Diagnostic capability	Yes	Yes	Increased diagnostic capability
Interrupt on loss of lock	Yes	No	—
Internal FrameSync capability	Yes	No	—
Passes CISPR 25 level 5 EMI; Passes BCI 100 mA	Yes; Yes	Yes; Yes	—
Package	48-pin VQFN; 7 mm × 7 mm	48-pin WQFN; 7 mm × 7 mm	Note pin and DAP differences below

DS90UB934 and DS90UB914A also share common features that are not listed in Table 1. These common features include:

- Built-in self-test (BIST)
- 2:1 multiplexer for deserializer inputs
- Cable interconnect: coaxial and STP
- Deserializer programmable spread—spectrum clock generation for LVCMOS outputs (SSCG)

2 Additional Functionality

The following section details added functionality available on DS90UB934 device and how the DS90UB934 compares to current feature set on DS90UB914A.

2.1 LVCMOS Interface—PCLK Frequency Range

The DS90UB934 supports a wider frequency range than the DS90UB914A with PCLK rates supported for 10-bit, 12-bit high-frequency (HF) and 12-bit low-frequency (LF) mode. Table 2 shows a matrix of the supported PCLK speeds.

Table 2. DS90UB914A and DS90UB934 PCLK Frequency Range

MODE	DS90UB934	DS90UB914A
10-bit	50 MHz to 100 MHz	50 MHz to 100 MHz
12-bit high frequency	37.5 MHz to 100 MHz	37.5 MHz to 75 MHz
12-bit low frequency	25 MHz to 50 MHz	25 MHz to 50 MHz

2.2 Maximum I2C Data Rate

The DS90UB934 device can support a maximum of 1-MHz data rate for I2C compared to the DS90UB914A maximum, which is 400 KHz. This greatly enhances control channel speed during device initialization.

2.3 Programmable Interrupt Functionality

The DS90UB934 device has a dedicated interrupt pin (INTB), which can be used for device monitoring. Table 3 shows a description of this pin. Interrupts can be brought out on the INTB pin by registers as explained in Section 3.2.2.

Table 3. DS90UB934 Interrupt Behavior

SIGNAL	PIN NUMBER	TYPE	DESCRIPTION
GPIO[3]/INTB	25	IO, Open Drain	General purpose input/output: Pin GPIO3 can be configured to be an input signal for GPOs on the serializer. Pin 25 is shared with INTB. Pull up with 4.7 kΩ to VDDIO. Programmable input/output pin is an active-low open drain and controlled by the status registers.

2.4 Internal FrameSync

A FrameSync signal can be sent via the back channel using any of the back channel GPIOs. In addition to sending external FrameSync signals, the DS90UB934 is capable of generating a FrameSync signal internally. In internal FrameSync mode, an internally generated FrameSync signal can be sent to one or more attached FPD-Link III serializers. FrameSync operation can be controlled through register as explained in Section 3.2.2.

2.5 Power Consumption

The DS90UB934 device has an internal 1.8-V to 1.1-V regulator for all power supplies except VDDIO. The device must be sourced with a power supply rail of 1.8 V ± 5% for these regulated supplies. Decoupling capacitors for this regulator should be placed on pins 3, 20, and 34. The DS90UB914A does not have an internal regulator and is sourced directly with 1.8 V ± 5%.

The DS90UB934 and DS90UB914A both include the option to source the VDDIO supply with either 1.8 V ± 5% or 3.3 V ± 10%. The VDDIO supply is not regulated internally in either chip.

Due to the presence of the internal 1.8-V to 1.1-V regulator on the DS90UB934 device, the power consumption numbers will differ from the DS90UB914A. Table 4 shows the typical estimated power consumption quantities.

Table 4. DS90UB914A and DS90UB934 Power Consumption

DS90UB934 total power, typical	Total power consumption normal operation	Worst case pattern default registers	VDD18 = VDDIO = 1.89 V	500 mW
			VDD18 = 1.89 V, VDDIO = 3.6 V	900 mW
DS90UB914A total power, typical	Total power consumption normal operation	Worst case pattern default registers	VDD18 = VDDIO = 1.89 V	163 mW
			VDD18 = 1.89 V, VDDIO = 3.6 V	272 mW

3 Required Modifications

3.1 PCB Design Modifications

3.1.1 Footprint

The DS90UB914A and DS90UB34 chipsets are both 48-pin, 7-mm × 7-mm QFN packages; however, the footprint of the DS90UB934 differs slightly from the footprint of the DS90UB914A. The DS90UB934 uses TI package RGZ0048B while the DS90UB914A uses TI package RHS0048A. The main difference between the two is that the RGZ and RHS packages use different lead frames, which leads to a slight difference in dimensions of the GND PAD (also referred to as DAP) located on the bottom of the chip. The differing GND PAD dimension is highlighted Figure 1 and Figure 2 which shows recommended landing patterns—the RGZ package has a 4.1-mm × 4.1-mm DAP area while the RHZ package has a 5.1-mm × 5.1-mm DAP area. It is possible to accommodate both design using the RGZ footprint.

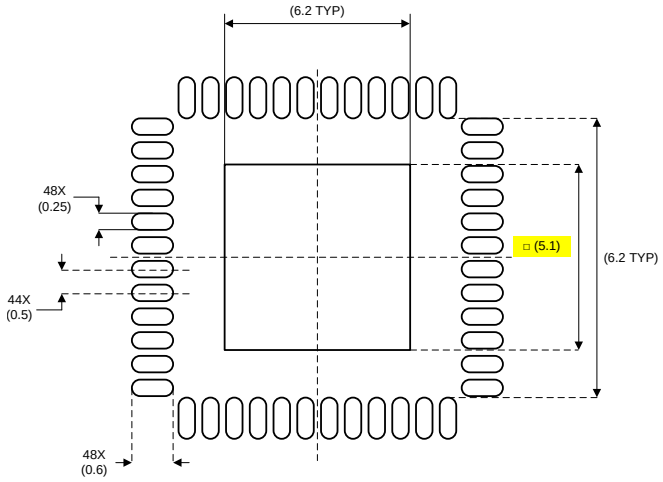

Figure 1. DS90UB934 Landing Pattern

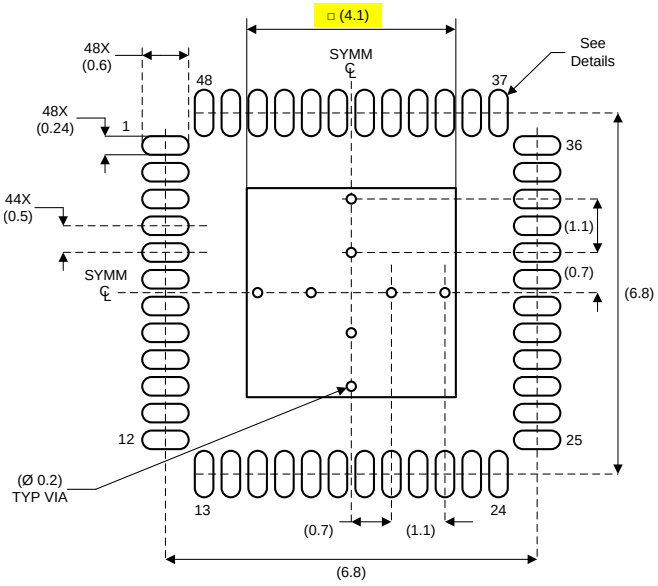

Figure 2. DS90UB914A Landing Pattern

3.1.2 Pinout

When converting a DS90UB914A design to a DS90UB934 design, the pinout of the DS90UB934 is almost identical to the DS90UB914A with the following exception: there are three pins (3, 20, and 34) on the 934 design that should have decoupling capacitors attached but NO voltage applied. Decoupling capacitors should be attached to each power supply pins. Refer to the DS90UB934 datasheet[1] for recommended values. A schematic that is compatible with both DS90UB914A and DS90UB934 is provided and detailed in Section 3.1.5. Table 5 shows a matrix of pinout comparisons between DS90UB914A and DS90UB934.

Table 5. DS90UB914A and DS90UB934 Pin Comparison

DS90UB934 PIN NAME	DS90UB914A PIN NAME	PIN NUMBER	DS90UB934 DESCRIPTION	DS90UB914A DESCRIPTION	IO TYPE DS90UB934	IO TYPE DS90UB914A
VDD11_D	VDDSSCG	3	Decoupling capacitor connection for internal analog regulator	SSCG PLL power, 1.8V ± 5%	D	Power, Analog
VDD11_DVP	VDDIO2	20	Decoupling capacitor connection for internal analog regulator	LVCMOS IO buffer power, 1.8 V ± 5% or 3.3 V ± 10%	D	Power, Digital
VDD11_FPD	IDx[1]	34	Decoupling capacitor connection for internal analog regulator	Used to assign I2C device address, resistor to GND and 10-kΩ pullup to 1.8-V rail	D	Input
VDD18	VDDD	17	1.8-V (± 5%) power supply	Digital core power, 1.8 V ± 5%	P	Power, Digital
VDDIO	VDDIO3	7	VDDIO voltage supply input, 1.8 V ± 5% or 3.3 V ± 10%	LVCMOS IO buffer power, 1.8 V ± 5% or 3.3 V ± 10%	P	Power, Digital
VDDIO	VDDIO1	29	VDDIO voltage supply input, 1.8 V ± 5% or 3.3 V ± 10%	LVCMOS IO buffer power, 1.8 V ± 5% or 3.3 V ± 10%	P	Power, Digital
VDD18_P0	VDDPLL	45	1.8-V (± 5%) PLL power supplies	PLL power, 1.8 V ± 5%	P	Power, Analog
VDD18_P1	VDDR	36	1.8-V (± 5%) PLL power supplies	Rx analog power, 1.8 V ± 5%	P	Power, Analog
VDD18_FPD0	VDDCML0	40	1.8-V (± 5%) high-speed transceiver (HSTRX) analog power supplies	CML and bidirectional control channel drive power, 1.8 V ± 5%	P	Power, Analog
VDD18_FPD1	VDDCML1	31	1.8-V (± 5%) high-speed transceiver (HSTRX) analog power supplies	CML and bidirectional control channel drive power, 1.8 V ± 5%	P	Power, Analog

3.1.3 I2C Addressing

The number of pins and recommended configurations for IDx addresses differ between the 914A and 934 devices. For the 914A, there are two IDx pins (pin 35 is IDx [0], pin 34 is IDx [1]) where the user may only choose the pulldown resistor values for each pin (RID0, RID1). Pullup value is chosen as a 10-kΩ resistance for each pin. For the 934, there is no recommended value for the pullup resistor and the user may select both R1 and R2 for the single IDx pin (pin 35). For both these devices, the resistors should be selected to ensure the desired ratio and corresponding IDx address as seen in Table 6 and Table 7

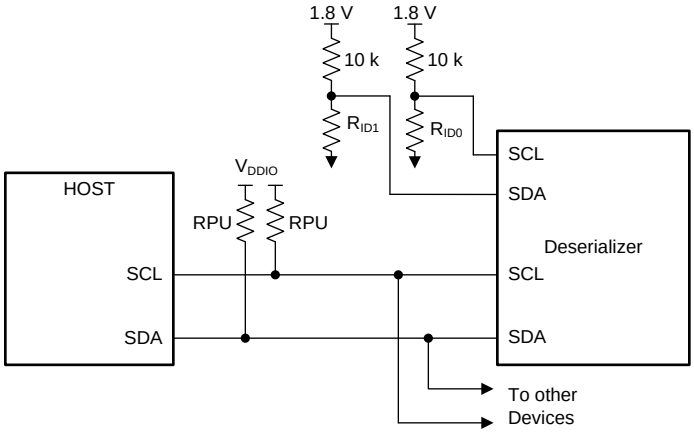

Figure 3. DS90UB914A IDx Strapping

Table 6. Resistor Values for IDx [0] and IDx [1] on DS90UB914A-Q1 Deserializer

ID[X] RESISTOR VALUE—DS90UB914A-Q1 DESERIALIZER			
Resistor R_{ID1} (kΩ) (1% Tolerance)	Resistor R_{ID0} (kΩ) (1% Tolerance)	Address 7'b	Address 8'b 0 appended (WRITE)
0	0	0x60	0xC0
0	3	0x61	0xC2
0	11	0x62	0xC4
0	100	0x63	0xC6
3	0	0x64	0xC8
3	3	0x65	0xCA
3	11	0x66	0xCC
3	100	0x67	0xCE
11	0	0x68	0xD0
11	3	0x69	0xD2
11	11	0x6A	0xD4
11	100	0x6B	0xD6
100	0	0x6C	0xD8
100	3	0x6D	0xDA
100	11	0x6E	0xDC
100	100	0x6F	0xDE

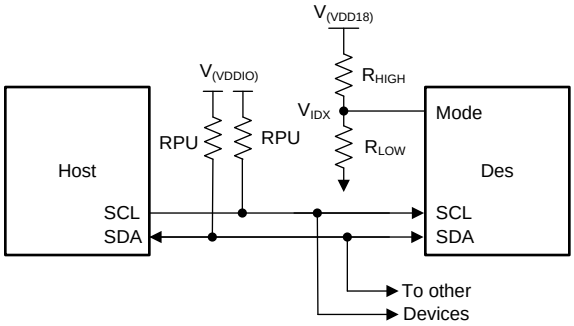

Figure 4. DS90UB934 IDx Strapping

Table 7. Resistor Values IDx on DS90UB934-Q1 Deserializer

SUGGESTED STRAP RESISTORS (1% TOLERANCE)		ASSIGNED I2C ADDRESS	
R_{HIGH} (kΩ)	R_{LOW} (kΩ)	7 BIT	8 BIT
OPEN	10.0	0x30	0x60
88.7	23.2	0x32	0x64
75.0	35.7	0x34	0x68
71.5	56.2	0x36	0x6C
78.7	97.6	0x38	0x70
39.2	78.7	0x3A	0x74
25.5	95.3	0x3C	0x78
10.0	OPEN	0x3D	0x7A

3.1.4 Mode Selection

Both DS90UB934 and DS90UB914A offer 10-bit mode, 12-bit high-frequency mode and 12-bit low-frequency mode; however, the mode strapping setting differs between the two devices. For DS90UB914A, the mode select pin is pulled to V_{DD} with a 10-kΩ resistor and pulled down with resistor R_{MODE} as shown in Figure 5. The recommended value of R_{MODE} to select a desired mode of operation is listed in Table 8. For DS90UB934, the mode select pin is pulled to V_{VDD18} with R_{HIGH} and R_{LOW} as shown in Figure 6. In addition to selecting the DVP mode, the DS90UB934 allows FPD-LINK III coax or STP selection through MODE strap pin. Recommended values of R_{HIGH} and R_{LOW} to select different modes of operation are listed in Table 9.

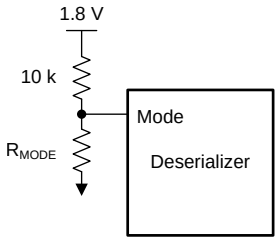

Figure 5. DS90UB914A MODE Strap

Table 8. DS90UB914A MODE Strap Resistor Value

DS90UB914A-Q1 DESERIALIZER MODE RESISTOR VALUE	
MODE SELECT	R_{MODE} RESISTOR VALUE (kΩ)
12-bit low-frequency mode: 25 MHz to 50 MHz PCLK, 10-bits or 12-bits DATA+ 2 SYNC. Note: No HS/VS restrictions (raw).	0
12-bit high-frequency mode: 37.5 MHz to 75 MHz PCLK, 10-bits or 12-bits DATA+ 2 SYNC. Note: No HS/VS restrictions (raw).	3
10-bit mode: 50 MHz to 100 MHz PCLK, 10-bits DATA+ 2 SYNC. Note: HS/VS restricted to no more than one transition per ten PCLK cycles.	11

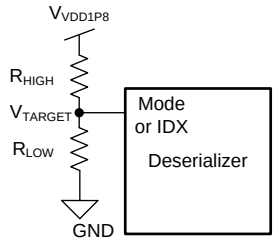

Figure 6. DS90UB934 MODE Strap

Table 9. DS90UB934 MODE Strap Resistor Value

SUGGESTED STRAP RESISTORS (1% TOLERANCE)		COAX OR STP	RX MODE
R_{HIGH} (kΩ)	R_{LOW} (kΩ)		
88.7	23.2	STP	RAW12 LF
75.0	35.7	STP	RAW12 HF
71.5	56.2	STP	RAW10
39.2	78.7	COAX	RAW12 LF
25.5	95.3	COAX	RAW12 HF
10.0	OPEN	COAX	RAW10

3.1.5 Schematic

There are a few changes that must be made to the DS90UB914A schematic and layout in order to accommodate the DS90UB934 device. Figure 7 and Figure 8 show two schematics—one version for VDDIO = 1.8 V and the other for VDDIO = 3.3 V, which has the option to accommodate either the DS90UB914A or DS90UB934 device depending upon which components are populated. Both versions list the minimum required components for either DS90UB914A or DS90UB934 device option.

The text boxes illustrate whether the specified component should be populated, not populated (DNP), or replaced with another component for both device options—914A and 934. The schematic as shown lists the default components for a DS90UB934 device configuration. Therefore, the default device symbol and pinout illustrated in the schematic is for the DS90UB934. The DS90UB914A pinout is listed in parentheses next to each pin on the schematic symbol.

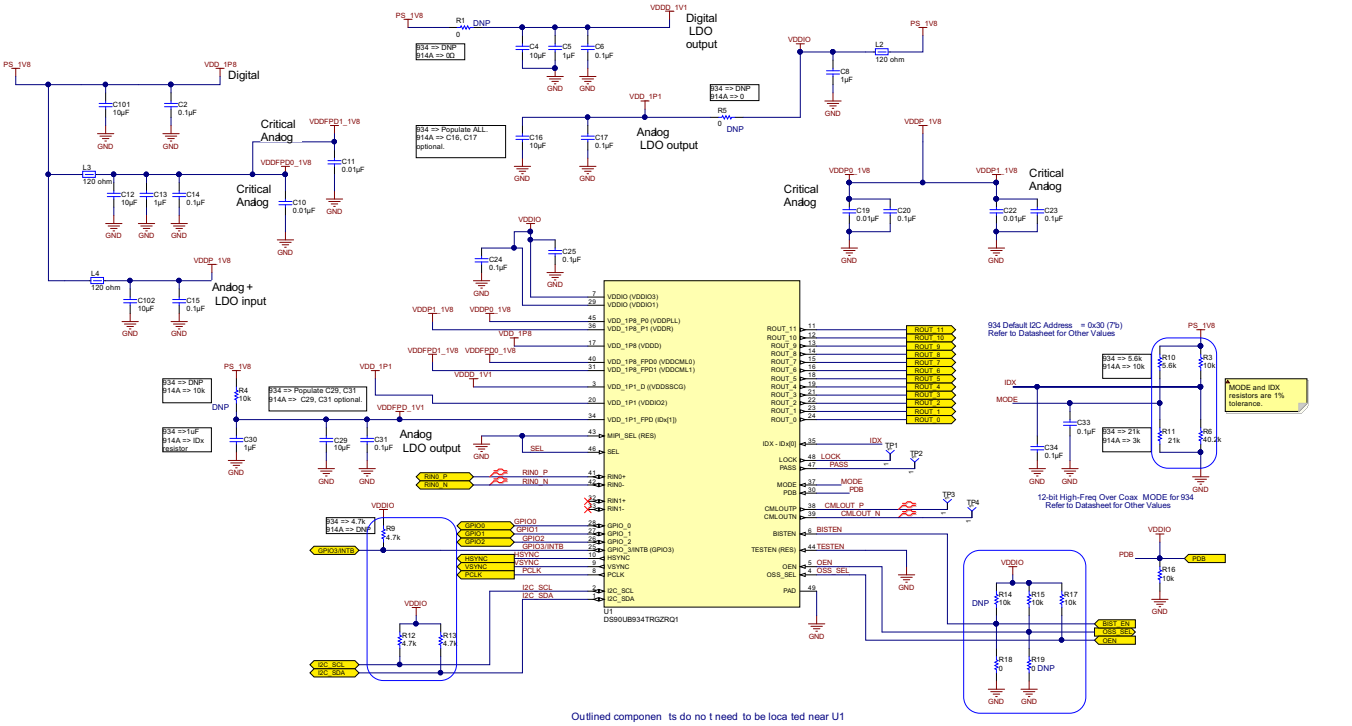

Figure 7. VDDIO=1.8V Schematic

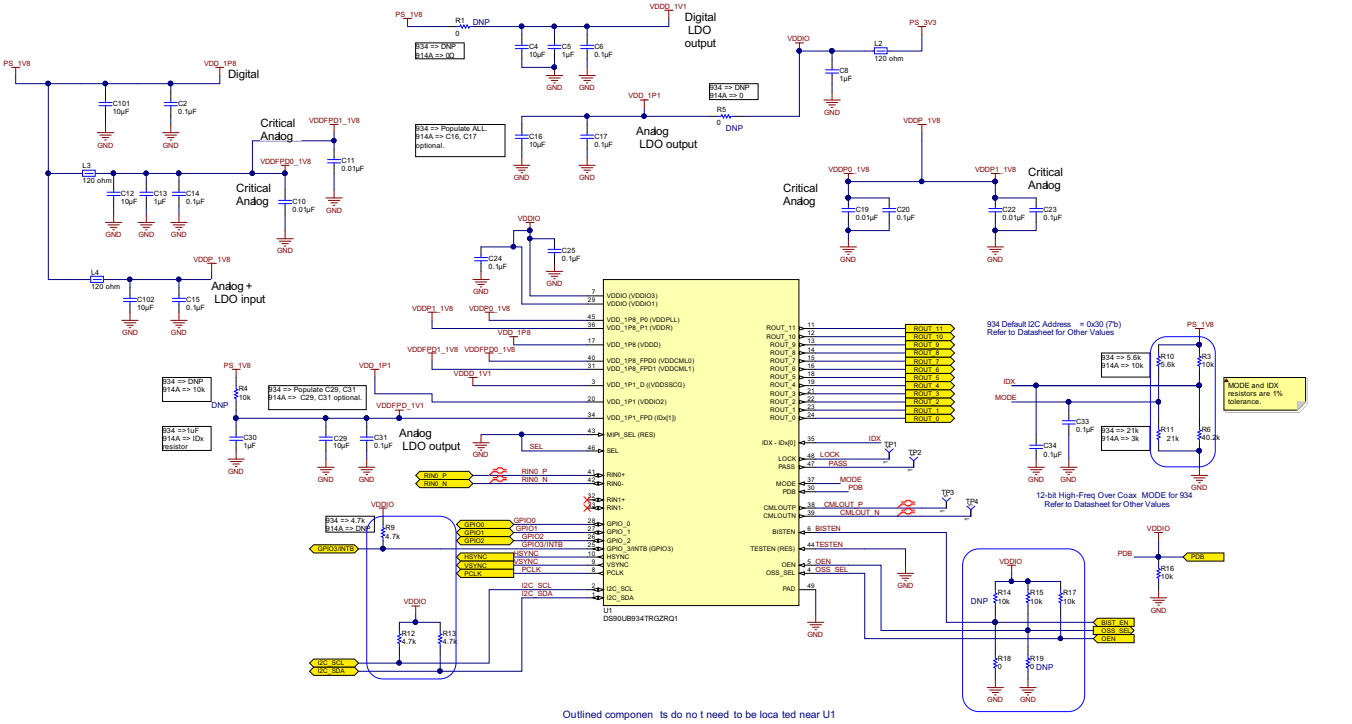

Figure 8. VDDIO=3.3V Schematic

3.2 Software Design Modifications

3.2.1 Register Map comparison

The DS90UB934 has a more extensive register map than the DS90UB914A device. Table 10 shows the differences between the register maps of the DS90UB914A and the DS90UB934. The shaded columns of Table 10 identify which register addresses in the DS90UB934 corresponding to the existing registers in the DS90UB914A. Not applicable denotes where there is no corresponding register. Additional functionality in the DS90UB934 programming is detailed in section 3.2.2. Reference the DS90UB934 datasheet [1] and DS90UB914A datasheet [2] for complete register maps.

Table 10. DS90UB914A and DS90UB934 Register Comparison

DS90UB914A				DS90UB934			
REGISTER ADDRESS	**REGISTER NAME**	**BITS**	**FIELD NAME**	**REGISTER ADDRESS**	**REGISTER NAME**	**BITS**	**FIELD NAME**
0x01	Reset	5	ANAPWDN	Not applicable			
		2	BC Enable	0X58	BCC_CONFIG	4	BACK CHANNELENABLE FOR CAMERA MODE
0x02	General Configuration 0	5	Auto-Clock	Not applicable			
		4	SSCG LFMODE	Not applicable			
		3:0	SSCG	Not applicable			
0x03	General Configuration 1	7	RX Parity Checker Enable	0x02	General Configuration	1	RX_PARITY_CHECK ER_EN
		6	TX CRC Checker Enable	Not applicable			
		5	VDDIO Control	0x0D	IO_CTL	6	IO_SUPPLY_MODE_OV
		4	VDDIO Mode			5:4	IO_SUPPLY_MODE
		3	I2C Pass-Through	0X58	BCC_CONGIF	6	I2C PASS THROUGH
		2	AUTO ACK	0x58	BCC_CONGIF	5	AUTO ACK ALL
		1	Parity Error Reset	Not applicable (1)			
		0	RRFB	0X3B	DVP_CLK_CTL	0	RRFB
0x04	EQ Feature Control	7:4	EQ Level	Not applicable			
0x05	Forward Channel Low Frequency Gain	7:0	LF GAIN	Not applicable			
0x06	SER ID	7:1	Remote ID	0x5B	SER_ID	7:1	SER ID
		0	Freeze Device ID			0	Freeze Device ID
0x07	SER Alias	7:1	Serializer Alias ID	0x5C	SER Alias	7:1	SER Alias ID
0x08	Slave ID[0]	7:1	Slave ID0	0x5D	Slave ID[0]	7:1	Slave ID0
0x09	Slave ID[1]	7:1	Slave ID1	0x5E	Slave ID[1]	7:1	Slave ID1
0x0A	Slave ID[2]	7:1	Slave ID2	0x5F	Slave ID[2]	7:1	Slave ID2
0x0B	Slave ID[3]	7:1	Slave ID3	0x60	Slave ID[3]	7:1	Slave ID3
0x0C	Slave ID[4]	7:1	Slave ID4	0x61	Slave ID[4]	7:1	Slave ID4
0x0D	Slave ID[5]	7:1	Slave ID5	0x62	Slave ID[5]	7:1	Slave ID5
0x0E	Slave ID[6]	7:1	Slave ID6	0x63	Slave ID[6]	7:1	Slave ID6
0x0F	Slave ID[7]	7:1	Slave ID7	0x64	Slave ID[7]	7:1	Slave ID7
0x10	Slave Alias[0]	7:1	Slave Alias ID0	0x65	Slave Alias[0]	7:1	Slave Alias ID0

(1) Parity register 0x55 and 0x56 will be cleared on read

Table 10. DS90UB914A and DS90UB934 Register Comparison (continued)

0x11	Slave Alias[1]	7:1	Slave Alias ID1	0x66	Slave Alias[1]	7:1	Slave Alias ID1
0x12	Slave Alias[2]	7:1	Slave Alias ID2	0x67	Slave Alias[2]	7:1	Slave Alias ID2
0x13	Slave Alias[3]	7:1	Slave Alias ID3	0x68	Slave Alias[3]	7:1	Slave Alias ID3
0x14	Slave Alias[4]	7:1	Slave Alias ID4	0x69	Slave Alias[4]	7:1	Slave Alias ID4
0x15	Slave Alias[5]	7:1	Slave Alias ID5	0x6A	Slave Alias[5]	7:1	Slave Alias ID5
0x16	Slave Alias[6]	7:1	Slave Alias ID6	0x6B	Slave Alias[6]	7:1	Slave Alias ID6
0x17	Slave Alias[7]	7:1	Slave Alias ID7	0x6C	Slave Alias[7]	7:1	Slave Alias ID7
0x18	Parity Errors Threshold	7:0	Parity Error Threshold Byte 0	0x05	PAR_ERR_THOLD_HI	7:0	PAR_ERR_THOLD_HI
0x19	Parity Errors Threshold	7:0	Parity Error Threshold Byte 1	0x06	PAR_ERR_THOLD_LO	7:0	PAR_ERR_THOLD_LO
0x1A	Parity Errors	7:0	Parity Error Byte 0	0x55	PAR_PAR_ERR_HI	7:0	PAR ERROR BYTE 1
0x1B	Parity Errors	7:0	Parity Error Byte 1	0x56	PAR_PAR_ERR_LO	7:0	PAR ERROR BYTE 0
0x1C	General Status	7:4	Rev-Id	0x03	Revision/Mask ID	7:4	REVISION_ID
		2	Parity Error	0x4D	RX_PORT_STS1	2	PARITY_ERROR
		1	Signal Detect	0x4E	RX_PORT_STS2	1	NO_FPD3_CLK
		0	Lock	0x4D	RX_PORT_STS1	0	LOCK_STS
0x1D	GPIO[1] and GPIO[0] Config	7	GPIO1 Output Value	0x11	GPIO1_PIN_CTL	1	GPIO1_OUT_VAL
		5	GPIO1 Direction	0x0F	GPIO_INPUT_CTL	1	GPIO1_INPUT_EN
		4	GPIO1 Enable	0x11	GPIO1_PIN_CTL	0	GPIO1_OUT_EN
		3	GPIO0 Output Value	0x10	GPIO0_PIN_CTL	1	GPIO0_OUT_VAL
		1	GPIO0 Direction	0x0F	GPIO_INPUT_CTL	0	GPIO0_INPUT_EN
		0	GPIO0 Enable	0x10	GPIO0_PIN_CTL	0	GPIO0_OUT_EN
0x1E	GPIO[3] and GPIO[2] Config	7	GPIO3 Output Value	0x13	GPIO3_PIN_CTL	1	GPIO3_OUT_VAL
		5	GPIO3 Direction	0x0F	GPIO_INPUT_CTL	3	GPIO3_INPUT_EN
		4	GPIO3 Enable	0x13	GPIO3_PIN_CTL	0	GPIO3_OUT_EN
		3	GPIO2 Output Value	0x12	GPIO2_PIN_CTL	1	GPIO2_OUT_VAL
		1	GPIO2 Direction	0x0F	GPIO_INPUT_CTL	2	GPIO2_INPUT_EN
		0	GPIO2 Enable	0x12	GPIO2_PIN_CTL	0	GPIO2_OUT_EN
0x1F	Mode and OSS Select	7	OEN_OSS Override	0x02	General Configuration	5	OUTPUT_OVERRIDE
		6	OEN Select	0x02	General Configuration	3	OUTPUT_ENABLE
		5	OSS Select	0x02	General Configuration	2	OUTPUT_SLEEP_STATE_SEL
		4	MODE_OVERRIDE	Not applicable (2)			
		3	PIN_MODE_12-bit HF mode	0xB8	MODE_IDX_STS	2:0	MODE
		2	PIN_MODE_10-bit HF mode				
		1	MODE_12-bit High Frequency	0x6D	PORT_CONFIG	1:0	FPD3_MODE
		0	MODE_10-bit mode	0x6D	PORT_CONFIG	1:0	FPD3_MODE
0x20	BCC Watchdog Control	7:1	BCC Watchdog Timer	0x07	BCC Watchdog Control	7:1	BCC WATCHDOG TIMER
		0	BCC Watchdog Timer Disable			0	BCC WATCHDOG TIMER DISABLE

(2) Set 0x6D [2] and [1:0] override modes

Table 10. DS90UB914A and DS90UB934 Register Comparison (continued)

0x21	I2C Control 1	7	I2C Pass Through All	0x58	BCC_CONFIG	7	I2C PASS THROUGH ALL
		6:4	I2C SDA Hold	0X08	I2C Control 1	6:4	I2C SDA HOLD
		3:0	I2C Filter Depth			3:0	I2C FILTER DEPTH
0x22	I2C Control 2	7	Forward Channel Sequence Error	Not applicable			
		6	Clear Sequence Error	Not applicable			
		4:3	SDA Output Delay	0X09	I2C Control 2	3:2	SDA Output Delay
		2	Local Write Disable	0x08	I2C Control 1	7	LOCAL WRITE DISABLE
		1	I2C Bus Timer Speedup	0X09	I2C Control 2	1	I2C BUS TIMER SPEEDUP
		0	I2C Bus Timer Disable			0	I2C BUS TIMER DISABLE
0x23	General Purpose Control	7:0	GPCR	Not applicable			
0x24	BIST Control	3	BIST Pin Configuration	0xB3	BIST Control	3	BIST PIN CONFIG
		2:1	BIST Clock Source			2:1	BIST CLOCK SOURCE
		0	BIST Enable			0	BIST_EN
0x25	BIST ERROR COUNT	7:0	BIST Error Count	0x57	BIST_ERR_COUNT	7:0	BIST ERROR COUNT
0x26	Bidirectional Control Channel (BCC) Tuning for Channel 0 (RIN0±)	3:2	Termination Resistance Control	Not applicable			
0x27	Forward Channel Tuning for Channel 0 (RIN0±)	7:0	Impedance Control	Not applicable			
0x3C	Oscillator output divider select	1:0	Osc Out Divider Sel	Not applicable			
0x3F	CML Output Enable	4	CML OUT Enable	See datasheet for enable sequency			
0x40	SCL High Time	7:0	SCL High Time	0x0A	SCL High Time	7:0	SCL High Time
0x41	SCL Low Time	7:0	SCL Low Time	0x0B	SCL Low Time	7:0	SCL Low Time
0x42	CRC Force Error	1	Force Back Channel Error	0xD0	PORT DEBUG	1	FORCE BC ERRORS
		0	Force One Back Channel Error			0	FORCE 1 BC ERROR
0x46	Bidirectional Control Channel (BCC) Tuning for Channel 1 (RIN1±)	3:2	Termination Resistance Control	Not applicable			
0x47	Forward Channel Tuning for Channel 1 (RIN1±)	7:0	Impedance Control	Not applicable			
0x4C	SEL REGISTER	7	Pin Channel SEL Override	0x2	General Configuration	7	INPUT_PORT_OVERRIDE
		6	Channel SEL	0x2	General Configuration	6	INPUT_PORT_SEL
0x4D	AEQ test Mode Select	6	AEQ Bypass	Not applicable			
0x4E	EQ Value	7:4	AEQ/Manual Eq Readback	Not applicable			

3.2.2 Additional Programming and Diagnostic Capabilities for DS90UB934

Aside from common registers shared by the DS90UB934 and the DS90UB914A, the DS90UB934 provides additional functionality through registers.

Both the DS90UB934 and the DS90UB914A- device has a 2:1 multiplexer, which allows customers to select between two serializer inputs. On the DS90UB914A, this selection can only be made through pin 46 SEL. However, on DS90UB934 the selection can be either pin controlled through pin 46 SEL or register controlled through register General Configuration 0x02 bit 7 and bit 6. Read and write between port 0 register and port 1 register is controlled through register FPD3_PORT_SEL 0x4C.

Table 11. Digital RX Port Registers

PAGE	ADDR(HEX)	REGISTER NAME	BITS	FIELD	TYPE	DEFAULT	DESCRIPTION
Share	0x02	GENERAL_CFG	7	INPUT_PORT_OVERRIDE	RW	0	Input port override bits allow control of the input port selection through the INPUT_PORT_SEL bit in this register.
			6	INPUT_PORT_SEL	RW	0	Input port select. This bit either controls the input mode (if INPUT_PORT_OVERRIDE is set) or indicates the status of the SEL pin.
Share	0x4C	FPD3_PORT_SEL	7:6	PHYS_PORT_NUM	R	0	Physical port number This field provides the physical port connection when reading from a remote device through the bidirectional control channel. When accessed through local I2C interfaces, the value returned is always 0. When accessed through bidirectional control channel, the value returned is the port number of the receive port connection.
			5	RESERVED	R	0	Reserved
			4	RX_READ_PORT	RW	0	Select RX port for register read This field selects one of the two RX port register blocks for read back. This applies to all paged FPD3 receiver port registers. 0: Port 0 registers 1: Port 1 registers When accessed through local I2C interfaces, the default setting is 0. When accessed through bidirectional control channel, the default value is the port number of the receive port connection.
			3:2	RESERVED	R	0	Reserved
			1	RX_WRITE_PORT_1	RW	0	Write Enable for RX port 1 registers This bit enables writes to RX port 1 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 receiver port registers. 0: Writes disabled 1: Writes enabled When accessed through bidirectional control channel, the default value is 1 if accessed over RX port 1.
			0	RX_WRITE_PORT_0	RW	0	Write Enable for RX port 0 registers This bit enables writes to RX port 0 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD3 Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed through bidirectional control channel, the default value is 1 if accessed over RX port 0.

DS90UB934 supports both external FrameSync control and internally generated FrameSync. FrameSync control mode can be selected in FS_CTL(x018) register. If using internally generated FrameSync, the FrameSync timing can be controlled by setting FS_HIGH_TIME and FS_LOW_TIME in register 0x19 to 0x1C. Sample scripts are provided in Section 3.2.3.1.

Table 12. FrameSync Registers

PAGE	ADDR(HEX)	REGISTER NAME	BITS	FIELD	TYPE	DEFAULT	DESCRIPTION
Share	0x18	FS_CTL	7:4	FS_MODE	RW	0	FrameSync Mode 0000: Internal Generated FrameSync, use back channel frame clock from port 0 0001: Internal Generated FrameSync, use back channel frame clock from port 1 001x: Reserved 01xx: Internal Generated FrameSync, use 25-MHz clock 1000: External FrameSync from GPIO0 1001: External FrameSync from GPIO1 1010: External FrameSync from GPIO2 1011: External FrameSync from GPIO3 1100: External FrameSync from GPIO4 1101: External FrameSync from GPIO5 1110: External FrameSync from GPIO6 1111: Reserved
			3	FS_SINGLE	RW/SC	0	Generate Single FrameSync pulse When this bit is set, a single FrameSync pulse will be generated. The system should wait for the full duration of the desired pulse before generating another pulse. When using this feature, the FS_GEN_ENABLE bit should remain set to 0. This bit is self-clearing and will always return 0.
			2	FS_INIT_STATE	RW	0	FrameSync Initial State This register controls the initial state of the FrameSync signal. 0: FrameSync initial state is 0 1: FrameSync initial state is 1
			1	FS_GEN_MODE	RW	0	FrameSync Generation Mode This control selects between Hi/Lo and 50/50 modes. In Hi/Lo mode, the FrameSync generator will use the FS_HIGH_TIME and FS_LOW_TIME register values to separately control the High and Low periods for the generated FrameSync signal. FrameSync times are based on the settings of the FS_MODE field. In 50/50 mode, the FrameSync generator will use the values in the FS_HIGH_TIME_0, FS_LOW_TIME_1 and FS_LOW_TIME_0 registers as a 24-bit value for both the high and low periods of the generated FrameSync signal. 0: Hi/Lo 1: 50/50
			0	FS_GEN_ENABLE	RW	0	FrameSync Generation Enable 0: Disabled 1: Enabled
Share	0x19	FS_HIGH_TIME_1	7:0	FRAMESYNC_HIGH_TIME_1	RW	0	FrameSync High Time bits 15:8 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.
Share	0x1A	FS_HIGH_TIME_0	7:0	FRAMESYNC_HIGH_TIME_0	RW	0	FrameSync High Time bits 7:0 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

Table 12. FrameSync Registers (continued)

PAGE	ADDR(HEX)	REGISTER NAME	BITS	FIELD	TYPE	DEFAULT	DESCRIPTION
Share	0x1B	FS_LOW_TIME_1	7:0	FRAMESYNC_LOW_TIME_1	RW	0	FrameSync Low Time bits 15:8 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.
Share	0x1C	FS_LOW_TIME_0	7:0	FRAMESYNC_LOW_TIME_0	RW	0	FrameSync Low Time bits 7:0 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

Interrupts can be brought out on the INTB pin by setting the INTERRUPT_CTL 0x23 and INTERRUPT_STS 0x24 registers. Interrupt generation is controlled via the PORT_ICR_HI 0xD8 and PORT_ICR_LO 0xD9 registers. In addition, the PORT_ISR_HI 0xDA and PORT_ISR_LO 0xDB registers provide read-only statuses for the interrupts. The status bits in the PORT_ISR_HI/LO registers are copies of the associated bits in the main status registers. Sample scripts on demonstrating the use of the interrupt pins in Section 3.2.3.2.

Table 13. Interrupt Registers

PAGE	ADDR(HEX)	REGISTER NAME	BITS	FIELD	TYPE	DEFAULT	DESCRIPTION
Share	0x23	INTERRUPT_CTL	7	INT_EN	RW	0	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.
			6:2	reserved	R	0	Reserved
			1	IE_RX1	RW	0	RX Port 1 Interrupt: Enable interrupt from Receiver Port 1.
			0	IE_RX0	RW	0	RX Port 0 Interrupt: Enable interrupt from Receiver Port 0.
Share	0x24	INTERRUPT_STS	7	INT	R	0	Global Interrupt: Set if any enabled interrupt is indicated in the individual status bits in this register. The setting of this bit is not dependent on the INT_EN bit in the INTERRUPT_CTL register but does depend on the IE_xxx bits. For example, if IE_RX0 and IS_RX0 are both asserted, the INT bit will be set to 1.
			6:2	reserved	R	0	Reserved
			1	IS_RX1	R	0	RX Port 1 Interrupt: An interrupt has occurred for Receive Port 1. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, andRX_PORT_STS2.
			0	IS_RX0	R	0	RX Port 0 Interrupt: An interrupt has occurred for Receive Port 0. This interrupt will be cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, and RX_PORT_STS2

Table 13. Interrupt Registers (continued)

PAGE	ADDR(HEX)	REGISTER NAME	BITS	FIELD	TYPE	DEFAULT	DESCRIPTION
RX	0xD8	PORT_ICR_HI	7:3	Reserved	R	0	Reserved
			2	IE_FPD3_ENC_ERR	RW	0	Interrupt on FPD-Link III Receiver Encoding Error When enabled, an interrupt will be generated on detection of an encoding error on the FPD-Link III interface for the receive port as reported in the FPD3_ENC_ERROR bit in the RX_PORT_STS2 register
			1	IE_BCC_SEQ_ERR	RW	0	Interrupt on BCC SEQ Sequence Error When enabled, an interrupt will be generated if a Sequence Error is detected for the Bidirectional Control Channel forward channel receiver as reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register.
			0	IE_BCC_CRC_ERR	RW	0	Interrupt on BCC CRC error detect When enabled, an interrupt will be generated if a CRC error is detected on a Bidirectional Control Channel frame received over the FPD-Link III forward channel as reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register.
RX	0xD9	PORT_ICR_LO	7:3	Reserved	RW	0	Reserved
			2	IE_FPD3_PAR_ERR	RW	0	Interrupt on FPD-Link III Receiver Parity Error When enabled, an interrupt will be generated on detection of parity errors on the FPD-Link III interface for the receive port. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register.
			1	IE_PORT_PASS	RW	0	Interrupt on change in Port PASS status When enabled, an interrupt will be generated on a change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register.
			0	IE_LOCK_STS	RW	0	Interrupt on change in Lock Status When enabled, an interrupt will be generated on a change in lock status. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register.

3.2.3 Sample Scripts

3.2.3.1 Internally Generated FrameSync Script Sample

The following example shows generation of a FrameSync signal at 60 pulse per second with 10% duty cycle

```
WriteI2C(0x4C,0x01) # Enable write to port RX0
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: Send FrameSync signal to GPIO0/1
WriteI2C(0x10,0x91) # Enable GPIO0 Output
WriteI2C(0x58,0x58) # BC FREQ SELECT: 2.5 Mbps
WriteI2C(0x19,0x00) # FS_HIGH_TIME_1
WriteI2C(0x1A,0x8A) # FS_HIGH_TIME_0
WriteI2C(0x1B,0x04) # FS_LOW_TIME_1
WriteI2C(0x1C,0xE1) # FS_LOW_TIME_0
WriteI2C(0x18,0x01) # Enable FrameSync
```

3.2.3.2 Interrupt Support Script Sample

The following example enables interrupt on either RX0 or RX1

```
# RX0/1 INTERRUPT_CTL enable
# "RX0 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x23,0x81) # RX0 & INTB PIN EN
# "RX1 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x23,0x82) # RX1 & INTB PIN EN
```

The following example shows how to read back interrupt status

```
INTERRUPT_STS = ReadI2C(0x24) # 0x24 INTERRUPT_STS
if ((INTERRUPT_STS & 0x80) >> 7):
print "# GLOBAL INTERRUPT DETECTED "
if ((INTERRUPT_STS & 0x02) >> 1):
print "# IS_RX1 DETECTED "
if ((INTERRUPT_STS & 0x01) ):
print "# IS_RX0 DETECTED "
# "################################################"
# "RX0 status"
# "################################################"
WriteReg(0x4C,0x01) # RX0
PORT_ISR_LO = ReadI2C(0xDB)
print "0xDB PORT_ISR_LO : ", hex(PORT_ISR_LO) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_LO & 0x04) >> 2):
print "# IS_FPD3_PAR_ERR DETECTED "
if ((PORT_ISR_LO & 0x02) >> 1):
print "# IS_PORT_PASS DETECTED "
if ((PORT_ISR_LO & 0x01) ) :
print "# IS_LOCK_STS DETECTED "
################################################
PORT_ISR_HI = ReadI2C(0xDA)
print "0xDA PORT_ISR_HI : ", hex(PORT_ISR_HI) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_HI & 0x04) >> 2):
print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
print "# IS_BCC_CRC_ERR DETECTED "
################################################
RX_PORT_STS1 = ReadI2C(0x4D) # R/COR
if ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
print "# RX_PORT_NUM = RX0"
```

```
if ((RX_PORT_STS1 & 0x20) >> 5):
print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
print "# PARITY_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x02) >> 1):
print "# PORT_PASS=1 "
if ((RX_PORT_STS1 & 0x01) ):
print "# LOCK_STS=1 "
##################################################RX_PORT_STS2 = ReadI2C(0x4E)
if ((RX_PORT_STS2 & 0x20) >> 5):
print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x04) >> 2):
print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
print "# NO_FPD3_CLK DETECTED "
################################################
# "################################################"
# "RX1 status"
# "################################################"
WriteReg(0x4C,0x12) # RX1
PORT_ISR_LO = ReadI2C(0xDB) # PORT_ISR_LO readout; cleared by RX_PORT_STS2
if ((PORT_ISR_LO & 0x04) >> 2):
print "# IS_FPD3_PAR_ERR DETECTED "
if ((PORT_ISR_LO & 0x02) >> 1):
print "# IS_PORT_PASS DETECTED "
if ((PORT_ISR_LO & 0x01) ) :
print "# IS_LOCK_STS DETECTED "
################################################
PORT_ISR_HI = ReadI2C(0xDA) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_HI & 0x04) >> 2):
print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
print "# IS_BCC_CRC_ERR DETECTED "
################################################
RX_PORT_STS1 = ReadI2C(0x4D) # R/COR
if ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
print "# RX_PORT_NUM = RX0"
if ((RX_PORT_STS1 & 0x20) >> 5):
print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
print "# PARITY_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x02) >> 1):
print "# PORT_PASS=1 "
if ((RX_PORT_STS1 & 0x01) ):
print "# LOCK_STS=1 "
################################################
RX_PORT_STS2 = ReadI2C(0x4E)
if ((RX_PORT_STS2 & 0x20) >> 5):
print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x04) >> 2):
print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
print "# NO_FPD3_CLK DETECTED "
################################################
```

4 References

1. Texas Instruments, *DS90UB934-Q1 12-Bit 100-MHz FPD-Link III Deserializer for 1MP/60fps and 2MP/30fps Cameras* (SNLS507)
2. Texas Instruments, *DS90UB914A-Q1 25-MHz to 100-MHz 10/12-Bit FPD-Link III Deserializer* (SNLS499)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2017) to A Revision	Page
• Changed text from: there are three pins (3, 20, and 34) on the 941A design that should have decoupling capacitors attached but NO voltage applied to: there are three pins (3, 20, and 34) on the 934 design that should have decoupling capacitors attached but NO voltage applied	5

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