Application Report
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How to Configure DS90UH940N-Q1 MIPI® D-PHY Timing Parameters

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ABSTRACT

The DS90UH940N-Q1 has built-in support for detecting the incoming video format extracted from the FPD-Link III datastream(s) and automatically generates D-PHY output timing parameters. The input video format detection is derived from progressive display resolutions based on the CEA−861D specification. For system implementations with custom video resolutions, system designers should either program the TI-validated D-PHY timing parameters provided in this report or validate the auto-generated parameters. The DS90UH940N-Q1 provides internal register control, which enables end users to configure their desired D-PHY timing.

Contents

Trademarks

1 Introduction

The DS90UH940N-Q1 is a FPD-Link III deserializer that recovers data from one or two FPD-Link III serial streams, and translates that data into a MIPI® CSI-2 format that can support video resolutions up to WUXGA and 1080p60 with 24-bit color depth. For the conformance to MIPI® D-PHY Version 1.2 specification, the DS90UH940N-Q1 automatically determines necessary D-PHY timing parameters for a list of standard video resolutions. While the parameters are automatically determined for the non-standard video resolutions as well, the timing parameters in some instances may be sub-optimal or without sufficient timing margin. Therefore, TI recommends to either program the TI-validated parameters or validate the auto-generated parameters for custom video resolutions. This application report reviews the D-PHY timing parameters, lists supported video resolutions, and suggests necessary DS90UH940N-Q1 register settings for non-standard video resolutions.

Information in this report is also applicable to DS90UB940N-Q1, DS90UH940-Q1, and DS90UB940-Q1.

2 D-PHY Timing Parameters

There are timing limits for all the phases of Start-of-Transmission (SoT), End-of-Transmission (EoT), High-Speed (HS), and Low-Power (LP) data transmission, as defined in the MIPI D-PHY specification (see Section 6). The DS90UH940N-Q1 provides internal register control for adjusting the D-PHY timing parameters listed in Table 1.

Table 1. D-PHY Timing Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CLK-POST}$	HS exit		60 + 52×UI			ns
$t_{CLK-PREPARE}$	Clock Lane HS Entry		38		95	ns
$t_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst		60			ns
$t_{CLK-ZERO}$	Time that the transmitter drives the HS-0 state prior to starting the Clock		262			ns
$t_{HS-EXIT}$	Time that the transmitter drives LP=11 following a HS burst		100			ns
$t_{HS-PREPARE}$	Data Lane HS Entry		40 + 4×UI		85 + 6×UI	ns
$t_{HS-ZERO}$	Time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence		105 + 6×UI			ns
$t_{HS-TRAIL}$	Data Lane HS Exit		60 + 4×UI			ns
t_{LPX}	Transmitted length of LP state		50			ns

The D-PHY timing parameters are shown in Figure 1 and Figure 2.

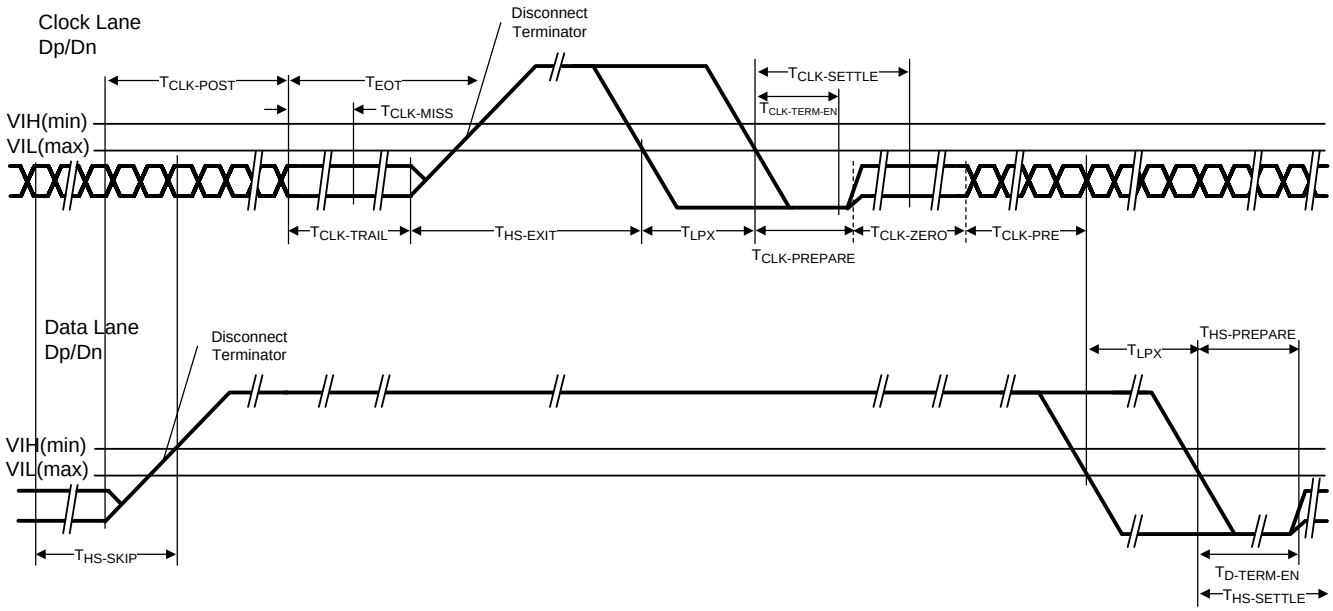

Figure 1. Switching the Clock Lane Between Clock Transmission and Low-Power Mode

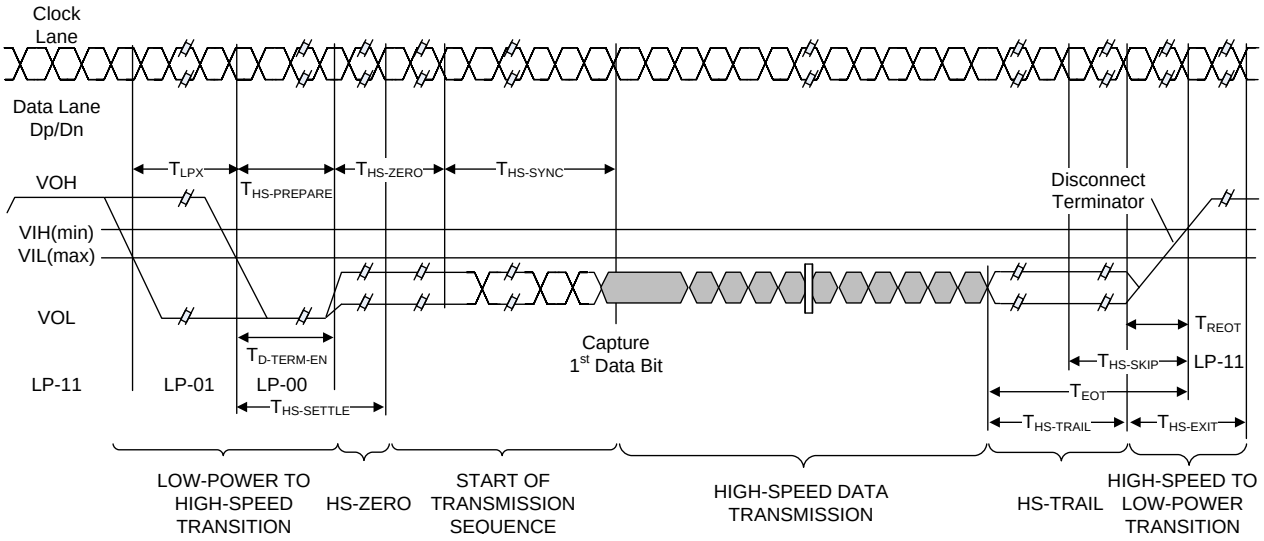

Figure 2. High-Speed Data Transmission Burst

3 Supported Video Resolutions

The D-PHY timing parameters are correctly auto-determined when video resolution is one of the listed resolutions in Table 2. The supported video resolutions are described in terms of the pixel allocations for horizontal and vertical resolutions, along with the frame rate in terms of frames per second (FPS) and pixel clock frequency (PCLK).

Table 2. Supported Video Resolutions

H-Active (pixels)	V-Active (pixels)	H-Total (pixels)	H-Blanking (pixels)	V-Total (pixels)	V-Blanking (pixels)	FPS (Hz)	PCLK (MHz)	CEA-861D Video ID(1)
640	480	800	160	525	45	59.94	25.18	1
800	600	1056	256	628	28	60	39.79	* (SVGA)
1024	768	1344	320	806	38	60	65	* (XGA)
1280	1024	1688	408	1066	42	60	107.96	SXGA
1400	1050	1560	160	1080	30	60	101	1400x1050RB
1400	1050	1904	504	1092	42	60	124.75	SXGA+
1920	1200	2080	160	1235	35	60	154	UXGAW
1600	1200	2160	560	1250	50	60	162	UXGA
1680	1050	-	-	-	-	59.95	146.29	*
1440	240	1716	276	263	23	59.89	27.03	8, 9
1440	240	1716	276	262	22	60.12	27.03	8, 9
720	480	858	138	525	45	59.94	27	2,3
720	480	858	138	525	45	60	27.03	2,3
1280	720	1980	700	750	30	50	74.25	19
1280	720	1650	370	750	30	59.94	74.18	4
1280	720	1650	370	750	30	60	74.25	4
1920	540	-	-	-	-	50	74.29	*
1920	540	-	-	-	-	59	74.14	*
1920	540	-	-	-	-	60	74.29	*
1080	1920	-	-	-	-	23	74.14	*

(1) Video formats with asterisk (*) are not specified by the CEA861-D specification. They are the display resolutions supported by DS90UH940N-Q1.

Table 2. Supported Video Resolutions (continued)

H-Active (pixels)	V-Active (pixels)	H-Total (pixels)	H-Blanking (pixels)	V-Total (pixels)	V-Blanking (pixels)	FPS (Hz)	PCLK (MHz)	CEA-861D Video ID[1]
1080	1920	-	-	-	-	24	74.29	*
1080	1920	-	-	-	-	25	74.29	*
1080	1920	-	-	-	-	29	74.14	*
1080	1920	-	-	-	-	30	74.14	*
1080	1920	-	-	-	-	50	148.57	*
1080	1920	-	-	-	-	59	148.43	*
1080	1920	-	-	-	-	60	148.57	*
2048	1080	-	-	-	-	23	74.14	*
2048	1080	-	-	-	-	24	74.29	*
2048	1080	-	-	-	-	25	74.29	*
2048	1080	-	-	-	-	29	74.14	*
2048	1080	-	-	-	-	30	74.29	*
2048	1080	-	-	-	-	50	148.57	*
2048	1080	-	-	-	-	59	148.43	*
2048	1080	-	-	-	-	60	148.57	*

4 Handling Custom Video Resolutions

While the DS90UH940N-Q1 correctly auto-determines the D-PHY timing parameters for a number of standard video resolutions, the device can be used in systems with custom video resolutions not included in Table 2. For custom video resolutions, one option is to program the TI-validated timing parameter settings in the DS90UH940N-Q1 CSI-2 indirect registers. The register settings control the timers for each phase of the CSI-2 transmission. Another option it to validate the auto-generated timing parameters and ensure they are within limits provided in Table 1.

4.1 Recommended D-PHY Timing Parameter Settings

The D-PHY timing parameter settings provided in Table 3 or Table 4 are TI-validated values for the supported range of the PCLK frequencies.

If the pixel clock (PCLK) frequency is a decimal number, the parameter settings corresponding to the PCLK frequency of the nearest integer should be used. For example, if the PCLK frequency is 36.5 MHz, the parameter setting corresponding to the PCLK frequency of 37 MHz should be used.

Table 3. Recommended Parameter Settings When Using Four CSI-2 Lanes

PCLK (MHz)	$t_{CLK-PREPARE}$	$t_{CLK-ZERO}$	$t_{CLK-TRAIL}$	$t_{CLK-POST}$	$t_{HS-PREPARE}$	$t_{HS-ZERO}$	$t_{HS-TRAIL}$	$t_{HS-EXIT}$	t_{LPX}
25 - 33	2	2	1	1	3	1	2	1	3
34 - 36	2	2	1	2	3	1	2	1	3
37	2	2	1	2	3	1	3	1	3
38	2	2	1	2	3	1	3	1	4
39 - 41	2	3	2	2	4	1	3	1	4
42	2	4	2	2	4	1	3	1	4
43	3	4	2	2	4	1	3	1	4
44	3	4	2	3	4	1	3	1	4
45	3	5	2	3	4	1	3	1	4
46 - 47	3	5	2	3	4	2	3	1	4
48	3	6	2	3	4	2	3	1	4
49 - 50	3	6	2	3	4	2	4	1	4
51 - 52	3	7	2	3	4	2	4	1	5

Table 3. Recommended Parameter Settings When Using Four CSI-2 Lanes (continued)

PCLK (MHz)	$t_{CLK-PREPARE}$	$t_{CLK-ZERO}$	$t_{CLK-TRAIL}$	$t_{CLK-POST}$	$t_{HS-PREPARE}$	$t_{HS-ZERO}$	$t_{HS-TRAIL}$	$t_{HS-EXIT}$	t_{LPX}
53	3	7	3	3	5	2	4	1	5
54 - 56	3	8	3	4	5	2	4	1	5
57 - 59	3	9	3	4	5	2	4	1	5
60	3	10	3	4	5	2	4	1	5
61 - 62	4	10	3	4	5	2	5	1	5
63	4	11	3	4	5	2	5	1	5
64 - 65	4	11	3	5	5	2	5	1	6
66	4	12	3	5	5	2	5	1	6
67 - 68	4	12	4	5	6	3	5	1	6
69 - 71	4	13	4	5	6	3	5	1	6
72	4	14	4	5	6	3	5	1	6
73	4	14	4	5	6	3	6	1	6
74	4	14	4	6	6	3	6	1	6
75 - 76	4	15	4	6	6	3	6	1	6
77	4	15	4	6	6	3	6	1	7
78	4	16	4	6	6	3	6	1	7
79 - 80	5	16	4	6	6	3	6	1	7
81 - 83	5	17	5	6	7	3	6	1	7
84	5	18	5	7	7	3	6	1	7
85 - 86	5	18	5	7	7	3	7	1	7
87	5	19	5	7	7	3	7	1	7
88	5	19	5	7	7	4	7	1	7
89	5	19	5	7	7	4	7	1	8
90 - 92	5	20	5	7	7	4	7	1	8
93	5	21	5	7	7	4	7	1	8
94	5	21	5	8	7	4	7	1	8
95	5	21	6	8	8	4	7	1	8
96	5	22	6	8	8	4	7	1	8
97 - 98	6	22	6	8	8	4	8	1	8
99 - 100	6	23	6	8	8	4	8	1	8
101	6	23	6	8	8	4	8	1	9
102 - 103	6	24	6	8	8	4	8	1	9
104	6	24	6	9	8	4	8	1	9
105 - 107	6	25	6	9	8	4	8	1	9
108	6	26	6	9	8	4	8	1	9
109 - 110	6	26	7	9	9	5	9	1	9
111 - 112	6	27	7	9	9	5	9	1	9
113	6	27	7	9	9	5	9	1	10
114	6	28	7	10	9	5	9	1	10
115 - 116	7	28	7	10	9	5	9	1	10
117 - 119	7	29	7	10	9	5	9	1	10
120	7	30	7	10	9	5	9	1	10
121 - 122	7	30	7	10	9	5	10	1	10
123	7	31	8	10	10	5	10	1	10
124	7	31	8	11	10	5	10	1	10
125	7	31	8	11	10	5	10	1	11
126 - 128	7	32	8	11	10	5	10	1	11

Table 3. Recommended Parameter Settings When Using Four CSI-2 Lanes (continued)

PCLK (MHz)	$t_{CLK-PREPARE}$	$t_{CLK-ZERO}$	$t_{CLK-TRAIL}$	$t_{CLK-POST}$	$t_{HS-PREPARE}$	$t_{HS-ZERO}$	$t_{HS-TRAIL}$	$t_{HS-EXIT}$	t_{LPX}
129 - 131	7	33	8	11	10	5	10	1	11
132	7	34	8	11	10	6	10	1	11
133	8	34	8	11	10	6	11	1	11
134	8	34	8	12	10	6	11	1	11
135	8	35	8	12	10	6	11	1	11
136	8	35	9	12	10	6	11	1	11
137	8	35	9	12	11	6	11	1	12
138 - 140	8	36	9	12	11	6	11	1	12
141 - 143	8	37	9	12	11	6	11	1	12
144	8	38	9	13	11	6	11	1	12
145 - 146	8	38	9	13	11	6	12	1	12
147 - 149	8	39	9	13	11	6	12	1	12
150	9	40	10	13	11	7	13	1	13
151 - 152	9	40	10	13	12	7	13	1	13
153	9	41	10	13	12	7	13	1	13
154 - 155	9	41	10	14	12	7	13	1	13
156 - 158	9	42	10	14	12	7	13	1	13
159	9	43	10	14	12	7	14	1	14
160 - 161	9	43	11	14	12	8	14	1	14
162 - 163	9	44	11	14	12	8	14	1	14
164	9	44	11	15	12	8	14	1	14
165 - 166	9	45	11	15	12	8	14	1	14
167	10	45	11	15	12	9	15	1	15
168 - 170	10	46	12	15	12	9	15	1	15

Table 4. Recommended Parameter Settings When Using Two CSI-2 Lanes

PCLK[(1)]	$t_{CLK-PREPARE}$	$t_{CLK-ZERO}$	$t_{CLK-TRAIL}$	$t_{CLK-POST}$	$t_{HS-PREPARE}$	$t_{HS-ZERO}$	$t_{HS-TRAIL}$	$t_{HS-EXIT}$	t_{LPX}
25	2	8	4	11	2	4	4	6	2
26 - 27	2	8	4	12	2	4	4	6	2
28	2	8	4	12	2	4	4	7	2
29	2	9	4	12	3	4	4	7	2
30	2	9	5	12	3	5	4	7	3
31 - 32	2	9	5	12	3	5	5	7	3
33	2	10	5	12	3	5	5	8	3
34 - 36	2	10	5	13	3	5	5	8	3
37	2	11	5	13	3	5	5	8	3
38	2	11	6	13	3	5	6	9	3
39 - 40	2	11	6	13	4	6	6	9	3
41 - 42	2	12	6	13	4	6	6	9	3
43	3	12	6	14	4	6	6	10	3
44	3	13	6	14	4	6	6	10	3
45	3	13	6	14	4	6	7	10	3
46 - 47	3	13	7	14	4	6	7	10	3
48	3	14	7	14	4	6	7	11	3
49	3	14	7	14	4	7	7	11	3

(1) When operating DS90UH940N-Q1 with two CSI-2 lanes, the maximum allowed pixel clock frequency is 107 MHz.

Table 4. Recommended Parameter Settings When Using Two CSI-2 Lanes (continued)

PCLK[1]	$t_{CLK-PREPARE}$	$t_{CLK-ZERO}$	$t_{CLK-TRAIL}$	$t_{CLK-POST}$	$t_{HS-PREPARE}$	$t_{HS-ZERO}$	$t_{HS-TRAIL}$	$t_{HS-EXIT}$	t_{LPX}
50	3	14	7	14	4	7	7	11	4
51	3	14	7	15	4	7	7	11	4
52	3	15	7	15	4	7	7	11	4
53 - 54	3	15	7	15	5	7	8	12	4
55	3	15	8	15	5	7	8	12	4
56 - 57	3	16	8	15	5	7	8	12	4
58	3	16	8	15	5	8	8	13	4
59	3	16	8	16	5	8	8	13	4
60	3	17	8	16	5	8	9	13	4
61 - 62	4	17	8	16	5	8	9	13	4
63 - 66	4	18	9	16	5	8	9	14	4
67	4	19	9	16	6	8	10	14	4
68 - 69	4	19	9	17	6	9	10	15	4
70	4	19	9	17	6	9	10	15	5
71 - 72	4	20	10	17	6	9	10	15	5
73 - 74	4	20	10	17	6	9	10	16	5
75	4	21	10	17	6	9	11	16	5
76	4	21	10	18	6	9	11	16	5
77	4	21	10	18	6	10	11	16	5
78	4	21	10	18	6	10	11	17	5
79	5	22	10	18	6	10	11	17	5
80	5	22	11	18	6	10	11	17	5
81 - 82	5	22	11	18	7	10	12	17	5
83	5	23	11	18	7	10	12	18	5
84 - 85	5	23	11	19	7	10	12	18	5
86	5	24	11	19	7	10	12	18	5
87	5	24	11	19	7	11	12	18	5
88 - 89	5	24	12	19	7	11	13	19	5
90 - 92	5	25	12	19	7	11	13	19	6
93	5	25	12	20	7	11	13	20	6
94	5	26	12	20	7	11	13	20	6
95	5	26	12	20	8	11	14	20	6
96	5	26	13	20	8	12	14	20	6
97	6	26	13	20	8	12	14	20	6
98 - 100	6	27	13	20	8	12	14	21	6
101	6	27	13	21	8	12	14	21	6
102	6	28	13	21	8	12	15	21	6
103 - 104	6	28	13	21	8	12	15	22	6
105	6	29	14	21	8	12	15	22	6
106	6	29	14	21	8	15	15	22	6
107	6	29	14	21	8	17	15	22	6

4.2 Accessing CSI-2 Indirect Registers

DS90UH940N-Q1 CSI-2 indirect register access is provided through an indirect access mechanism through the Indirect Access registers (CSIIA and CSIID). These registers are located at offsets 0x6C-0x6D in the main register space.

The indirect address mechanism involves setting the register offset address and reading or writing the data register.

For writes, the process is as follows:

1. Write to the CSIIA register to set the register offset
2. Write the data value to the CSIID register

For reads, the process is as follows:

1. Write to the CSIIA register to set the register offset
2. Read from the CSIID register

4.2.1 CSIIA Indirect Access Register (Address = 6Ch) [reset = 0h]

CSIIA is described in Table 5.

Table 5. CSIIA Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CSI_IA	R/W	0h	Indirect address port for accessing CSI registers

4.2.2 CSIID Indirect Access Register (Address = 6Dh) [reset = 0h]

CSIID is described in Table 6.

Table 6. CSIID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CSI_ID	R/W	0h	Indirect data port for accessing CSI registers

4.2.3 CSI-2 Indirect Registers

Table 7 summarizes the DS90UB940N-Q1 CSI-2 indirect registers. All register offset addresses not listed in Table 7 should be considered as reserved locations and the register contents should not be modified.

Table 7. CSI-2 Indirect Registers Summary

Address	Register Name	D-PHY Timing Parameter	Section
0h	CSI_TCK_PREP	$t_{CLK-PREPARE}$	Go
1h	CSI_TCK_ZERO	$t_{CLK-ZERO}$	Go
2h	CSI_TCK_TRAIL	$t_{CLK-TRAIL}$	Go
3h	CSI_TCK_POST	$t_{CLK-POST}$	Go
4h	CSI_THS_PREP	$t_{HS-PREPARE}$	Go
5h	CSI_THS_ZERO	$t_{HS-ZERO}$	Go
6h	CSI_THS_TRAIL	$t_{HS-TRAIL}$	Go
7h	CSI_THS_EXIT	$t_{HS-EXIT}$	Go
8h	CSI_TLPX	t_{LPX}	Go

4.2.3.1 CSI_TCK_PREP Register (Address = 0h) [reset = 0h]

CSI_TCK_PREP is described in Table 8.

Return to Summary Table.

Table 8. CSI_TCK_PREP Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CSI_TCK_PREP_OV	R/W	0h	Override CSI Tck Prep Parameter 0: Tck Prep is automatically determined. 1: Override Tck Prep parameter with a value in bits [4:0] in this register.
6-5	RESERVED	R/W	0h	Reserved
4-0	CSI_TCK_PREP	R/W	0h	Tck Prep Value.

4.2.3.2 CSI_TCK_ZERO Register (Address = 1h) [reset = 0h]

CSI_TCK_ZERO is described in Table 9.

Return to Summary Table.

Table 9. CSI_TCK_ZERO Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CSI_TCK_ZERO_OV	R/W	0h	Override CSI Tck Zero Parameter 0: Tck Zero is automatically determined. 1: Override Tck Zero parameter with a value in bits [5:0] in this register.
6	RESERVED	R/W	0h	Reserved
5-0	CSI_TCK_ZERO	R/W	0h	Tck Zero Value.

4.2.3.3 CSI_TCK_TRAIL Register (Address = 2h) [reset = 0h]

CSI_TCK_TRAIL is described in Table 10.

Return to Summary Table.

Table 10. CSI_TCK_TRAIL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CSI_TCK_TRAIL_OV	R/W	0h	Override CSI Tck Trail Parameter 0: Tck Trail is automatically determined. 1: Override Tck Trail parameter with a value in bits [3:0] in this register.
6-4	RESERVED	R/W	0h	Reserved
3-0	CSI_TCK_TRAIL	R/W	0h	Tck Trail Value.

4.2.3.4 CSI_TCK_POST Register (Address = 3h) [reset = 0h]

CSI_TCK_POST is described in Table 11.

Return to Summary Table.

Table 11. CSI_TCK_POST Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CSI_TCK_POST_OV	R/W	0h	Override CSI Tck Post Parameter 0: Tck Post is automatically determined. 1: Override Tck Post parameter with a value in bits [5:0] in this register.
6	RESERVED	R/W	0h	Reserved
5-0	CSI_TCK_POST	R/W	0h	Tck Post Value.

4.2.3.5 CSI_THS_PREP Register (Address = 4h) [reset = 0h]

CSI_THS_PREP is described in Table 12.

Return to Summary Table.

Table 12. CSI_THS_PREP Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CSI_THS_PREP_OV	R/W	0h	Override CSI Ths Prep Parameter 0: Ths Prep is automatically determined. 1: Override Ths Prep parameter with a value in bits [4:0] in this register.
6-5	RESERVED	R/W	0h	Reserved
4-0	CSI_THS_PREP	R/W	0h	Ths Prep Value.

4.2.3.6 CSI_THS_ZERO Register (Address = 5h) [reset = 0h]

CSI_THS_ZERO is described in Table 13.

Return to Summary Table.

Table 13. CSI_THS_ZERO Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CSI_THS_ZERO_OV	R/W	0h	Override CSI Ths Zero Parameter 0: Ths Zero is automatically determined. 1: Override Ths Zero parameter with a value in bits [4:0] in this register.
6-5	RESERVED	R/W	0h	Reserved
4-0	CSI_THS_ZERO	R/W	0h	Ths Zero Value.

4.2.3.7 CSI_THS_TRAIL Register (Address = 6h) [reset = 0h]

CSI_THS_TRAIL is described in Table 14.

Return to Summary Table.

Table 14. CSI_THS_TRAIL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CSI_THS_TRAIL_OV	R/W	0h	Override CSI Ths Trail Parameter 0: Ths Trail is automatically determined. 1: Override Ths Trail parameter with a value in bits [3:0] in this register.
6-4	RESERVED	R/W	0h	Reserved
3-0	CSI_THS_TRAIL	R/W	0h	Ths Trail.

4.2.3.8 CSI_THS_EXIT Register (Address = 7h) [reset = 0h]

CSI_THS_EXIT is described in Table 15.

Return to Summary Table.

Table 15. CSI_THS_EXIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CSI_THS_EXIT_OV	R/W	0h	Override CSI Ths Exit Parameter 0: Ths Exit is automatically determined. 1: Override Ths Exit parameter with a value in bits [4:0] in this register.
6-5	RESERVED	R/W	0h	Reserved
4-0	CSI_THS_EXIT	R/W	0h	Ths Exit.

4.2.3.9 CSI_TLPX Register (Address = 8h) [reset = 0h]

CSI_TLPX is described in Table 16.

Return to Summary Table.

Table 16. CSI_TLPX Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CSI_TLPX_OV	R/W	0h	Override CSI Tlpx Parameter 0: Tlpx is automatically determined. 1: Override Tlpx parameter with a value in bits [3:0] in this register.
6-4	RESERVED	R/W	0h	Reserved
3-0	CSI_TLPX	R/W	0h	Tlpx.

4.3 Programming Example

Assuming a custom video resolution and frame rate that results in a pixel clock frequency of 125 MHz and the need to use the DS90UH940N-Q1 with four CSI-2 lanes, it is easy to look up the recommended D-PHY timing parameter settings in Table 3. For this example, the recommended settings are summarized in Table 17.

Table 17. Recommended Parameter Settings Example

PCLK	CSI_TCK_PREP	CSI_TCK_ZERO	CSI_TCK_TRAIL	CSI_TCK_POST	CSI_THS_PREP	CSI_THS_ZERO	CSI_THS_TRAIL	CSI_THS_EXIT	CSI_TLPX
125 MHz	7	31	8	11	10	5	10	1	11

The following example code configures the DS90UH940N-Q1 D-PHY timing parameters per recommended settings given in Table 17.

```
WriteI2C (0x6C, 0x00)    // Set register offset for CSI_TCK_PREP
WriteI2C (0x6D, 0x87)    // Set register value for CSI_TCK_PREP
WriteI2C (0x6C, 0x01)    // Set register offset for CSI_TCK_ZERO
WriteI2C (0x6D, 0xB1)    // Set register value for CSI_TCK_ZERO
WriteI2C (0x6C, 0x02)    // Set register offset for CSI_TCK_TRAIL
WriteI2C (0x6D, 0x88)    // Set register value for CSI_TCK_TRAIL
WriteI2C (0x6C, 0x03)    // Set register offset for CSI_TCK_POST
WriteI2C (0x6D, 0x91)    // Set register value for CSI_TCK_POST
WriteI2C (0x6C, 0x04)    // Set register offset for CSI_THS_PREP
WriteI2C (0x6D, 0x90)    // Set register value for CSI_THS_PREP
WriteI2C (0x6C, 0x05)    // Set register offset for CSI_THS_ZERO
WriteI2C (0x6D, 0x85)    // Set register value for CSI_THS_ZERO
WriteI2C (0x6C, 0x06)    // Set register offset for CSI_THS_TRAIL
WriteI2C (0x6D, 0x90)    // Set register value for CSI_THS_TRAIL
WriteI2C (0x6C, 0x07)    // Set register offset for CSI_THS_EXIT
WriteI2C (0x6D, 0x81)    // Set register value for CSI_THS_EXIT
WriteI2C (0x6C, 0x08)    // Set register offset for CSI_TLPX
WriteI2C (0x6D, 0x91)    // Set register value for CSI_TLPX
```

5 Conclusion

While the DS90UH940N-Q1 correctly auto-determines necessary D-PHY timing parameters for a list of standard video resolutions, for systems with custom video resolutions, TI recommends that the designer programs the TI-validated parameter settings for optimal D-PHY timing margins or validates the auto-generated parameters to ensure compliance to the D-PHY specification. Programming of the parameters can easily be done by setting the corresponding indirect registers with the values provided in this report.

6 References

1. *DS90UH940N-Q1 1080p FPD-Link III to CSI-2 Deserializer With HDCP* (SNLS613)
2. *MIPI® Alliance, Specification for D-PHY Version 1.2, August 2014*

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