

AN-1503 Designing an ATCA Compliant M-LVDS Clock Distribution Network

ABSTRACT

This application report provides a guide to designing ATCA compliant clock distribution networks using M-LVDS devices. The application report consists of a quick description of an ATCA synchronization clock interface, an overview of M-LVDS standard, an extensive discussion on performance of M-LVDS devices in an ATCA backplane and a set of design recommendations and rules that will assist you in building a bullet proof clock distribution network.

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1 Introduction

Many telecommunication systems including those designed based on the Advanced Telecommunications Computing Architecture (ATCA) specifications require synchronization of their internal interfaces and the external networks. To enable implementation of such systems the ATCA or PICMG 3.0 specification defines a synchronization clock interface in the architecture. Per this specification, the task of sourcing clock signals has been assigned to integrated circuits (ICs) conforming to TIA/EIA-899 (Multipoint Low Voltage Differential Signaling or M-LVDS) standard.

2 Synchronization Clock Interface in an ATCA Backplane

In an AdvancedTCA backplane ([Figure 1](#)), there are three connector zones:

- Zone 1 for Power Connection and Shelf management
- Zone 2 for Data Transport Interfaces
- Zone 3 for User-defined I/O Interconnect

The Data Transport Interfaces are Base Interface, Fabric Interface, Update Channel Interface, and Synchronization Clock Interface. These interfaces provide connectivity between up to 16 slots. As [Figure 1](#) illustrates, each slot can have up to 5 Advanced Differential Fabric (ADF) or zone 2 connectors. Examples of the ADF connectors are Tyco HM-Zd and ERNI ERmetZD.

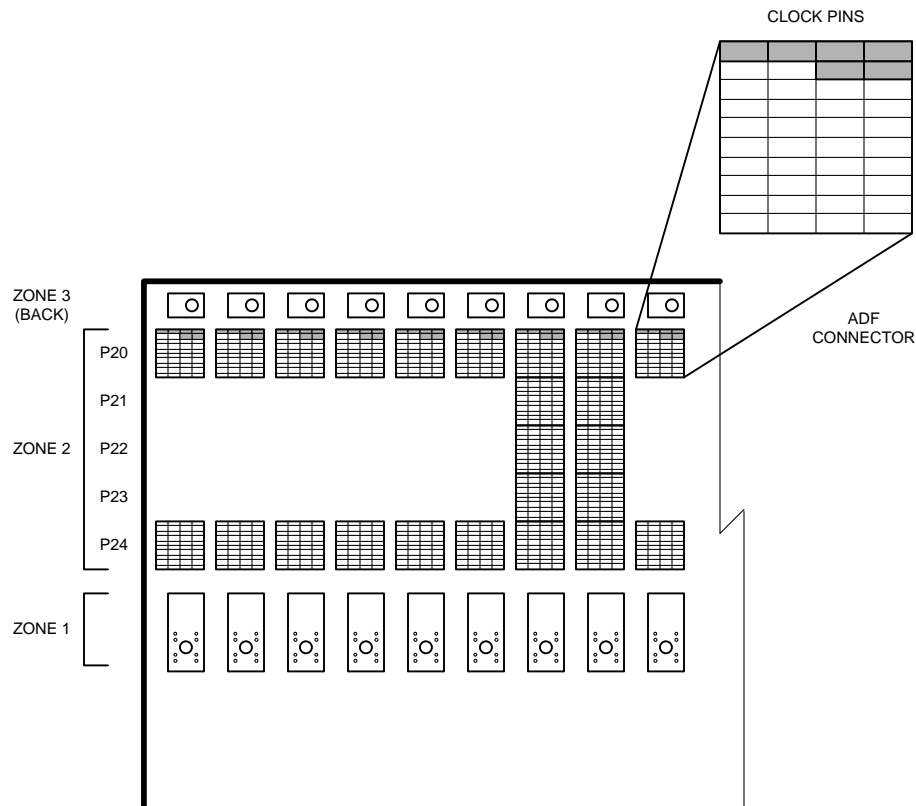


Figure 1. Location of Clock Pins in an ATCA Backplane

The clock synchronization interface enables exchange of timing information between all slots in the backplane. It consists of 3 pairs of redundant clock busses: CLK1A, CLK1B, CLK2A, CLK2B, CLK3A and CLK3B. The PICMG 3.0 specification defines usage, frequency, and quality of each clock group:

- CLK1A and CLK1B are for redundant 8 kHz standard digital telephony transmission system clocks.
- CLK2A and CLK2B are for 19.44 MHz clocks for synchronization of the SONET/SDH networks.
- CLK3A and CLK3B are for user-defined signals (clock or data).

The first two rows of pins of each P20 ADF connector connect to the 6 clock busses. The busses are essentially 130-ohm differential PCB traces terminated with 80-ohm resistors on both sides. Figure 2 shows how M-LVDS drivers and receivers create a multipoint clock distribution network when three or more line cards are installed in the backplane.

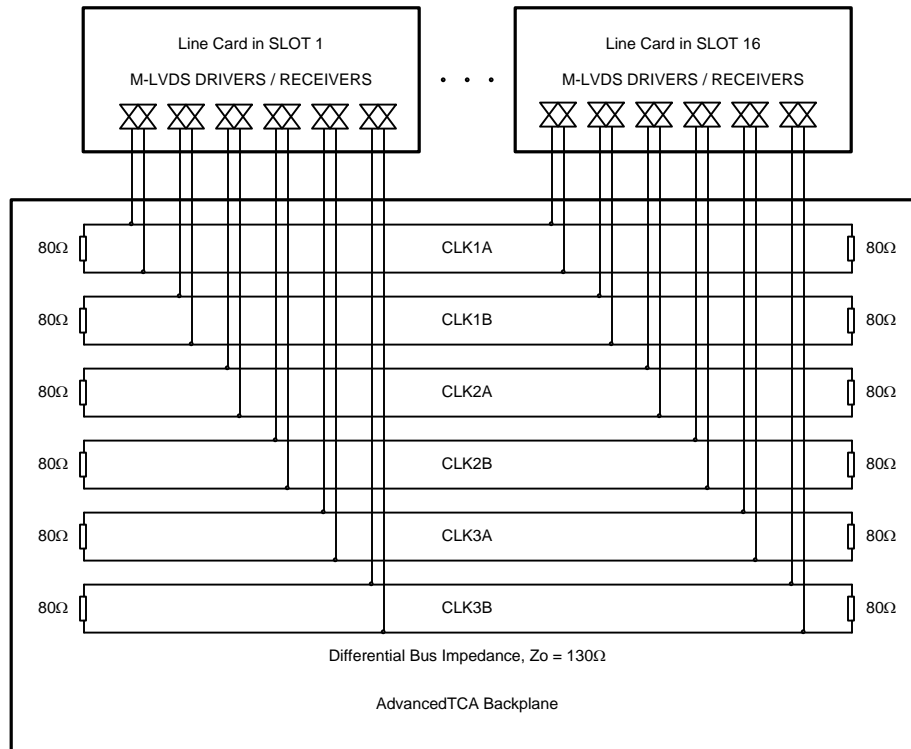


Figure 2. M-LVDS Drivers / Receivers Connect to Clock Buses

3 M-LVDS Overview

The multipoint low voltage differential signaling, or M-LVDS (TIA/EIA-899) standard specifies the electrical characteristics of line drivers and receivers intended for general data transport within a multipoint bus where up to 32 nodes may be connected. More specifically, it defines driver output characteristics, and input characteristics of two receiver types.

Per TIA/EIA-899 standard, a M-LVDS driver generates a differential signal with a 480 – 650 mV amplitude and an offset within the 0.3 – 2.1 V range. The signal must have 10% - 90% transition times (rise and fall) of 1 ns or greater and up to one half of a unit interval (t_{UI}) to alleviate the effects of stubs that are the “artifacts” of multipoint architectures. Table 1 summarizes key characteristics of LVDS (popular interface for point to point topologies) and M-LVDS drivers.

The key M-LVDS receiver specifications are input voltage threshold and input common mode range. The input threshold levels differentiate the two types of M-LVDS receivers as illustrated in Figure 3. Type 1 receivers have threshold levels centered at 0 V and provide higher noise margin than type 2 receivers. Type 2 receivers have lower positive noise margin but provide fail-safe provisions for control signals (See Figure 5 and Figure 6).

The receiver input common mode range of –1.4 to 3.8 V makes M-LVDS a robust interface for connecting sub-systems that may have potential difference between their ground references of up to ±1 volts.

Table 1. Comparison of Key Driver Parameters

Parameter	LVDS	M-LVDS
V_{OD} [mV]	250 - 450	480 - 650
V_{OS} [V]	1.125	0.3 - 2.1
I_{OD} [mA]	2.5 - 4.5	9 - 13
I_{OS} [mA]	< 24	< 43
t_{RISE} / t_{FALL} Min [ns]	N / A	1
t_{RISE} / t_{FALL} Max [s]	$0.3 t_{UI}$	$0.5 t_{UI}$

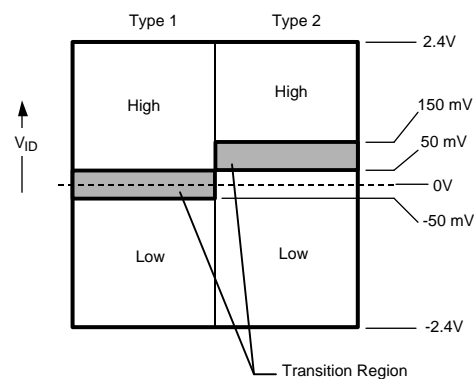


Figure 3. M-LVDS Standard Defines Two Receiver Types

4 M-LVDS Performance in an ATCA Backplane

Currently, Texas Instruments family of M-LVDS devices consists of four single channel devices:

- DS91D176 – A Half Duplex with Type 1 M-LVDS Inputs
- DS91C176 – A Half Duplex with Type 2 M-LVDS Inputs
- DS91D180 – A Full Duplex with Type 1 M-LVDS Inputs
- DS91C180 – A Full Duplex with Type 2 M-LVDS Inputs

This section reports on the performance of the DS91D176, a representative of the family, in an AdvancedTCA backplane. The following subsections describe setup, experiment method and findings in detail.

4.1 Setup Description

A 14-slot dual-star AdvancedTCA compliant backplane developed by ELMA Bustronic (www.bustronic.com) and fourteen line cards (P/N: DS91D176EVK) developed by Texas Instruments enabled testing of various multi-point clock distribution networks. Each line card features six DS91D176 devices whose M-LVDS I/O pins connect to an ADF connector. By installing the line card in the backplane, each of the six devices on the card connects to each of the six clock busses on the backplane. Installation of all fourteen line cards creates six multi-drop networks. Each line card can be setup as a driver card (all six devices configured as M-LVDS drivers) or a receiver card (all six devices on the card configured as M-LVDS receivers). [Figure 4](#) shows a picture of the backplane fully loaded with the M-LVDS line cards.

On the M-LVDS line card, the un-terminated short PCB tracks (stubs) that connect M-LVDS I/O pins to the bus have different geometries for each device. The stub lengths range from 0.25 to 2 inches (1 inch \approx 2.54 cm) and differential stub impedances range from 80 to 130 ohms. [Table 2](#) shows characteristics of the stubs found on the line card

For the M-LVDS line card schematic files, gerbers, board stack up and other information about the line card, see the latest user manual on the TI web site at [LVDS & CML Solutions](#).

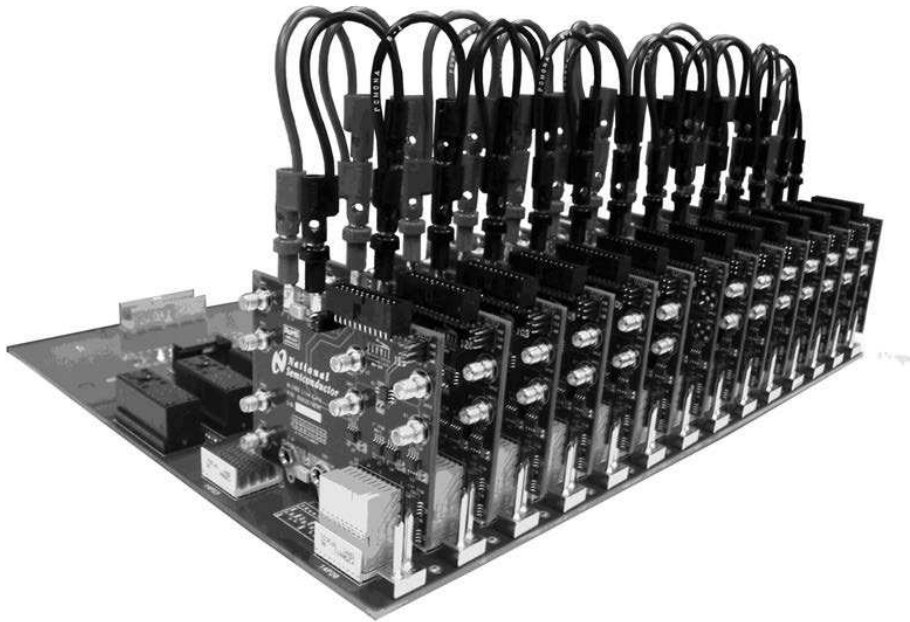


Figure 4. 14-Slot ATCA Backplane Fully Loaded with M-LVDS Line Cards

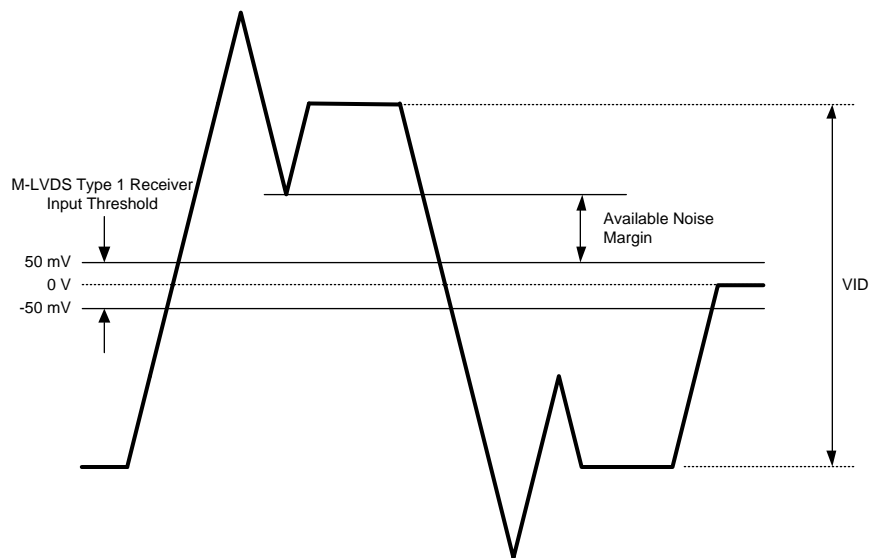
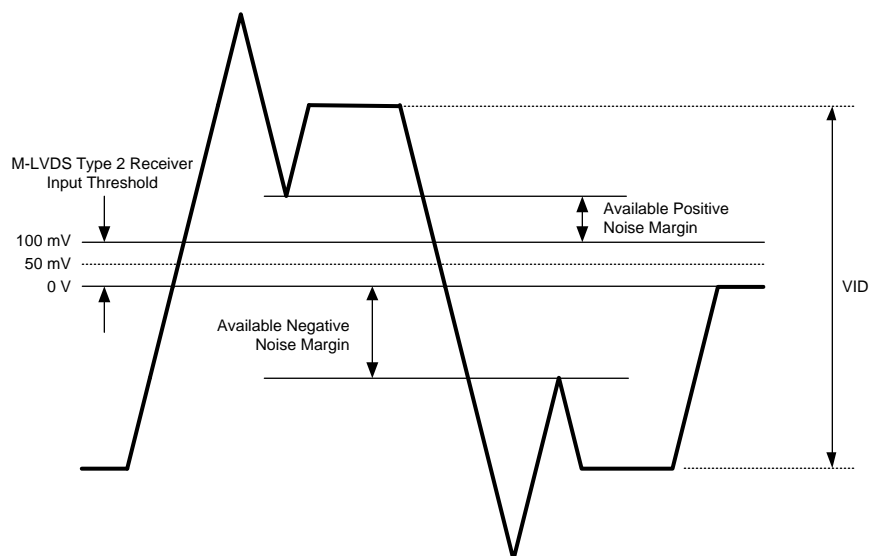
Table 2. M-LVDS Line Card Stub Characteristics and Pin Mapping

Device	M-LVDS Pins	ADF Connector Pins	Stub Length	Stub Diff. Impedance
U1	A1, B1	B1, A1	0.25"	100 ohms
U2	A2, B2	D1, C1	0.50"	100 ohms
U3	A3, B3	F1, E1	1.00"	130 ohms
U4	A4, B4	H1, G1	1.00"	100 ohms
U5	A5, B5	D2, C2	1.00"	80 ohms
U6	A6, B6	B2, B1	2.00"	100 ohms

4.2 Experiment Method

When it comes to performance of M-LVDS clock distribution networks, it is mainly the noise margin that differentiates a good design from one that is marginal. Stubs are the major detriment to noise margin in a multi-drop environment. They reduce noise margin in two ways: first, stubs load the bus and as a result reduce the amplitude of the driver output signal. Second, stubs create impedance discontinuities that cause reflections and, as a result, further reduce available noise margin.

In this experiment, evaluation method consists of looking at the available noise margin ([Figure 5](#) and [Figure 6](#)) at the input of each receiver and examining effects of clock driver position and stub characteristics on the noise margin.


Figure 5. Available Noise Margin to a Type 1 Receiver

Figure 6. Available Noise Margin to a Type 2 Receiver

4.3 Experiment Findings

Extensive experimentation with various multi-drop configurations, stub lengths, stub impedances and frequencies has led to the following set of conclusions:

- Noise margin on the receivers' inputs is higher if the location of the driver card is closer to one of the termination resistors. In other words, the first and the last slot in a backplane are the best driver card locations; slots in the middle are the worst.
- Noise margin is the lowest for the receivers in the slot adjacent to the slot with the driver card; it is the highest for the receivers on the furthest card. [Table 3](#) shows available noise margin for the receivers in the slot adjacent to and furthest from the slot with the driver card. The backplane is fully loaded and the clock frequency is 19.44 MHz.

- Noise margin is higher with shorter and narrower stubs. Once a stub starts to behave as an un-terminated transmission line, at the point where it connects to the bus, it lowers the impedance of that section of the bus. These impedance variations or discontinuities along the bus cause reflections that lower noise margin. [Figure 7](#) shows effects of the stub length on the available noise margin for the receivers in slot #8 while the driver card is in slot #7 and driving a 19.44 MHz clock to all thirteen receiver cards.
 - In [Figure 7](#), the four waveforms are measured at the input of the adjacent receivers from the four networks with 0.25-, 0.5-, 1- and 2-inch stubs. It is clear that the receiver from the network with 2-inch stubs has the lowest noise margin. [Table 4](#) presents measured noise margin for the receivers in the slot #8 while the driver card is in the slot #7 and driving clock signals to all thirteen receiver cards at some common frequencies. As data in [Table 4](#) indicates, the worst noise margin for the given configuration is when the clock signals have a frequency around 60 MHz. At 100 MHz, the maximum frequency allowed for AdvancedTCA systems, signals have the most attenuation and become sine-wave shaped waveforms without any major reflections at the receiver. As a result, noise margin is the highest at that frequency.
 - [Figure 8](#) shows effects of the stub impedance on the available noise margin for the receivers in slot #8 when the driver card is in slot #7 and drives a 19.44 MHz clock to all thirteen receiver cards.
 - In [Figure 8](#), the three waveforms are measured at the input of the adjacent receivers from the three networks with 80-, 100- and 130-ohm stubs. The receiver from the network with 130-ohm stubs has the highest noise margin. [Table 5](#) presents measured noise margin for the receivers in slot #8 when the driver card is in slot #7 and drives clock signals to all thirteen receiver cards at some common frequencies.

Table 3. Noise Margin Depends on Driver and Receiver Cards Locations and Stub Length

Driver Location	Receiver Location	Available Noise Margin [mV]			
		0.25" Stubs	0.50" Stubs	1.00" Stubs	2.00" Stubs
Slot #1	Slot #2	350	310	230	230
Slot #1	Slot #14	>350	>350	>350	>350
Slot #7	Slot #8	230	230	150	70
Slot #7	Slot #14	310	310	230	230

Table 4. Noise Margin is Higher with Shorter Stubs

Frequency [MHz]	Driver Location	Receiver Location	Available Noise Margin [mV]			
			0.25" Stubs	0.50" Stubs	1.00" Stubs	2.00" Stubs
19.44	Slot #7	Slot #8	230	230	150	70
30.72	Slot #7	Slot #8	230	230	115	105
61.44	Slot #7	Slot #8	180	160	140	0
100.0	Slot #7	Slot #8	>350	>350	>350	>350

Table 5. Higher Impedance Stubs Have a Lesser Impact on Noise Margin

Frequency [MHz]	Driver Location	Receiver Location	Available Noise Margin [mV]		
			80 ohm Stubs	100 ohm Stubs	130 ohm Stubs
19.44	Slot #7	Slot #8	130	150	170
30.72	Slot #7	Slot #8	105	115	130
61.44	Slot #7	Slot #8	130	140	160
100.0	Slot #7	Slot #8	>350	>350	>350

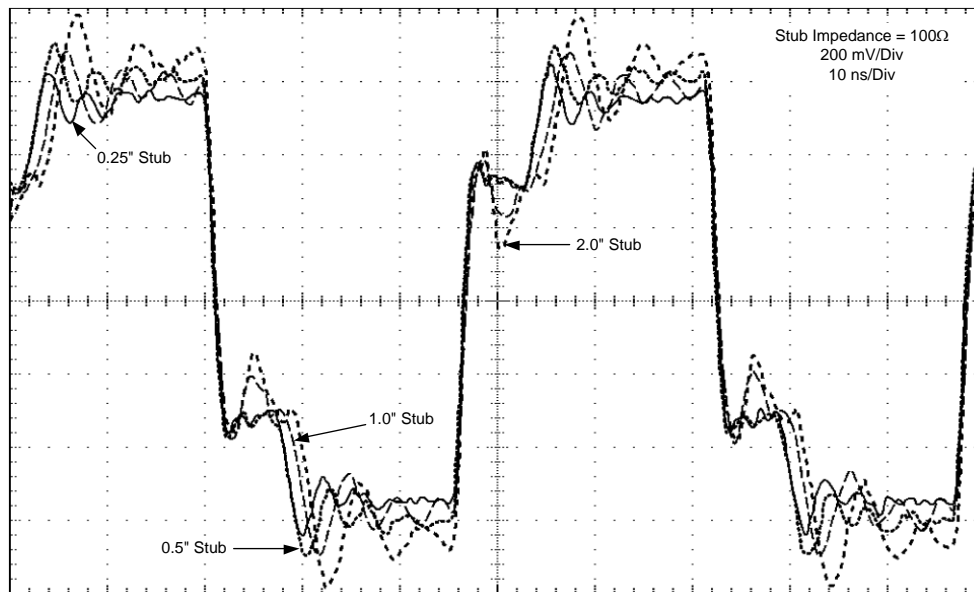


Figure 7. Noise Margin is Higher with Shorter Stubs

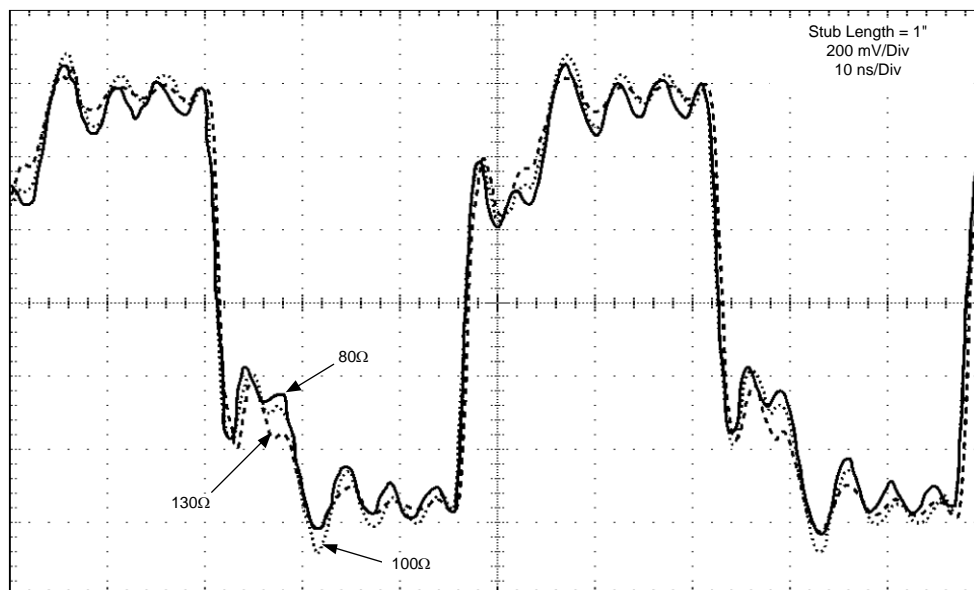


Figure 8. Higher Impedance Stubs Have a Lesser Impact on Noise Margin

5 Designing an M-LVDS Clock Distribution Network - Tips and Tricks

Designing an ATCA compliant M-LVDS clock distribution network is a not as straightforward a task as it may appear if one only relies on the recommendations given in the PCIMG 3.0 standard. The following set of design recommendations and tips derived from experimentation with an ATCA compliant backplane and M-LVDS products from Texas Instruments will help you to build a reliable clock distribution network with the highest noise margin possible.

- Select M-LVDS drivers with the slowest transition time that will satisfy the bandwidth requirements of your clock system. TIA/EIA-899 standard specifies 1 ns as the minimum transition time for output of an M-LVDS driver. In an ATCA backplane with 1-inch stubs, 1 ns transition time is too fast for certain configurations. M-LVDS drivers from Texas Instruments have typical 10%-90% transition times of 1.7 ns and can operate at frequencies of up to 100 MHz.
- Place your clock drivers on line cards located in slots closer to the ends of the backplane provided other system requirements allow it. This arrangement creates longer signal paths. The longer signal paths are lossier and lay down the signal edges. Again, slower transition times are more “forgiving” when they encounter impedance discontinuities.
- Minimize the stub length as much as possible. The PCIMG 3.0 specifies 1 inch (excluding the ADF connector) as the maximum stub length for M-LVDS devices. Anything longer than that may cause your system to fail. Shortening the stubs from 1 inch to ½ inch may increase your noise margin by 50%.
- When noise margin is at a premium, one should consider maximizing the stub impedance. This can be accomplished by either increasing the dielectric thickness between the stub and the copper plane(s) or by making the stubs as narrow as PCB manufacturers can make it (in addition to minimizing the stub length) or both.
- Any power supply noise can reduce available noise margin. Ensure that M-LVDS devices are properly decoupled. Use two vias for VDD and GND pins and place decoupling capacitors close to the device VDD pin. [Figure 9](#) shows how to place decoupling capacitors and connect DS91D176 to the power and ground planes.

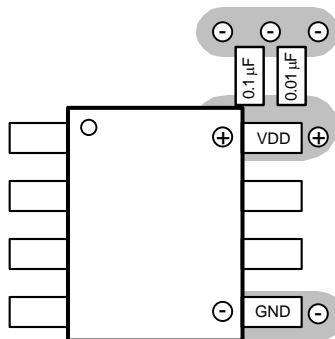


Figure 9. Decoupling DS91D176

6 Conclusion

Short, narrow stubs coupled with signal drivers (that is, M-LVDS line drivers) that have controlled output edge-rates are the key to increased noise margin and improved overall performance of any multipoint network including M-LVDS clock distribution networks in ATCA backplanes. By keeping this in mind and following PCB design recommendations given in this note, reliable clock distribution networks can be designed with ease.

7 References

1. *DS91D176/DS91C176 100 MHz Single Channel M-LVDS Transceivers* ([SNLS146](#))
2. PICMG 3.0 Revision 2.0, ATCA Base Specification. March 18, 2000
3. TIA/EIA-899-A, Electrical Characteristics of Multipoint Low Voltage Differential Signaling (M-LVDS) Interface Circuits, Telecommunications Industry Association. March 2002
4. TIA/EIA-644-A, Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, Telecommunications Industry Association. February 2001

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