

AN-1926 An Introduction to M-LVDS and Clock and Data Distribution Applications

ABSTRACT

This application note provides an overview of the M-LVDS standard, introduces Texas Instrument’s current M-LVDS product portfolio, describes common M-LVDS applications, and details important design guidelines.

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Since it's been ratified in early 2002, the TIA/EIA-899 (Multipoint Low Voltage Differential Signaling or M-LVDS) has become a popular electrical standard for binary data interchange over multipoint clock distribution and data buses. While keeping many benefits of LVDS circuits (high speed, low power consumption, and excellent noise immunity), M-LVDS circuits include additional provisions – a stronger drive, controlled transition times, extended input common mode voltage range, and failsafe – all necessary for reliable multipoint networks.

1 M-LVDS Standard Overview

The M-LVDS standard specifies electrical characteristic of line drivers and receivers intended for general data transport over a multipoint bus (Figure 1) where up to 32 nodes may be connected. More specifically, it defines driver output characteristics, and input characteristics of two receiver types. The following two sections summarize the key M-LVDS driver and receiver characteristics and compare them to the characteristics of drivers and receivers conforming to the two other popular differential standards: RS-485 (TIA/EIA-485-A) and LVDS (TIA/EIA-644-A).

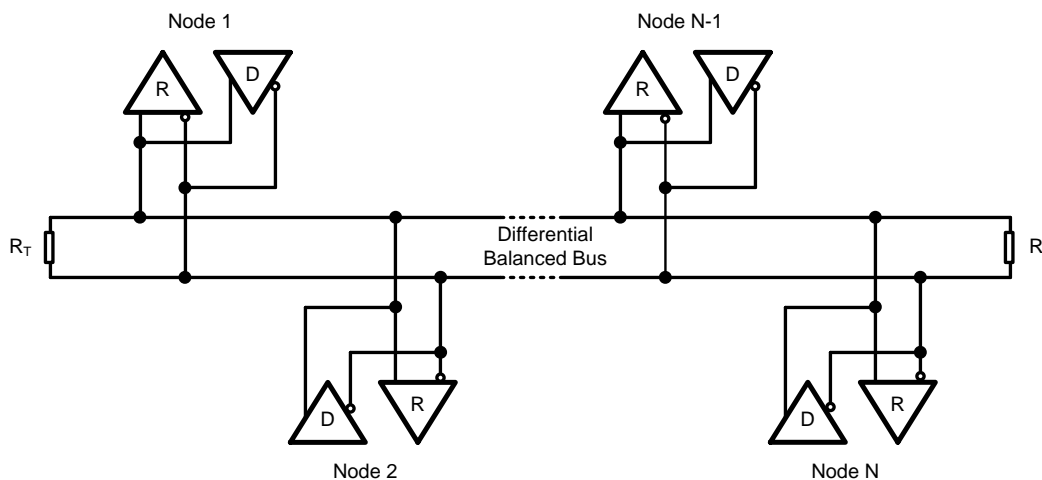


Figure 1. Multipoint Network

2 Driver Characteristics

Per TIA/EIA-899 standard, an M-LVDS driver generates a differential signal with 480 – 650 mV amplitude and an offset within the 0.3V to 2.1V range. The signal must have 10% – 90% transition times (rise and fall) of 1 ns or greater and up to one half of a unit interval (t_{UI}).

When compared to RS-485 drivers, M-LVDS drivers provide significantly reduced signal amplitudes (See Figure 2) that result in lower power consumption and reduced electromagnetic interference (EMI). The lower signal amplitudes enable higher signaling rates or signal frequencies. While the M-LVDS standard specifies maximum signaling rate of 500 Mbps based on the 1 ns minimum transition time, current commercially available M-LVDS drivers peak at 250 Mbps. On the other side, the fastest RS-485 drivers typically peak at 10 Mbps with a few unique devices reaching 30 Mbps to 50 Mbps rates. The benefits of faster speeds, lower power, and reduced EMI come at the expense of reduced noise margins, however, by following necessary design guidelines given later in this application note, successful M-LVDS networks can be designed without significant efforts.

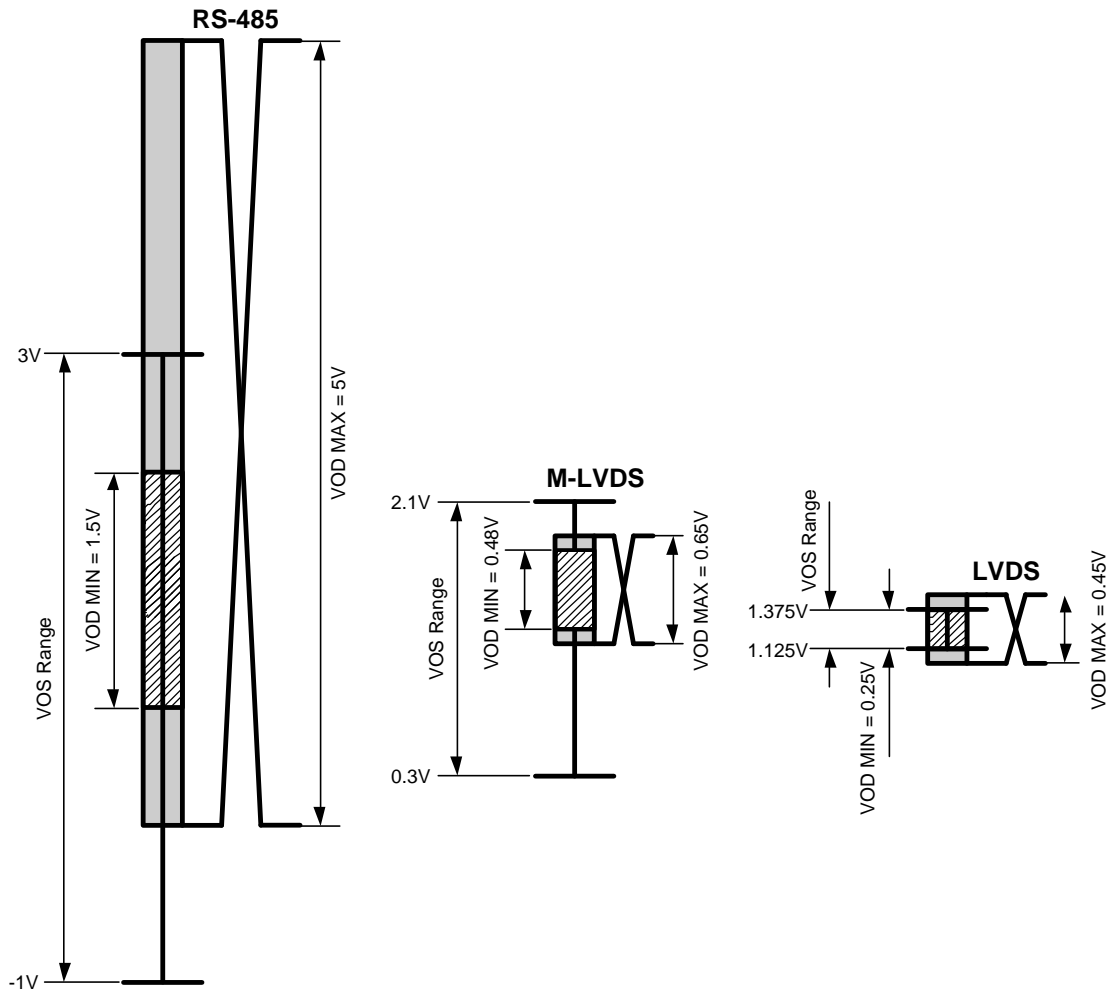


Figure 2. Driver VOD and VOS Comparison

When compared to LVDS drivers, M-LVDS drivers pose as drivers with a stronger drive (larger IOD). The stronger drive enables the M-LVDS drivers to drive signals across multipoint networks that are typically doubly terminated. Doubly terminated networks present a heavier load to the driver, so the stronger drive is necessary for retaining required signal amplitudes. Both M-LVDS and RS-485 driver output amplitudes are typically specified with a 50Ω differential load. This is a load that a driver typically sees in a multipoint network with a double termination as illustrated in Figure 1. LVDS driver output amplitudes are specified with a 100Ω differential load. This is a load that a driver typically sees in a point-to-point link with a single termination as shown in Figure 3. M-LVDS drivers also pose as drivers with controlled transition times, a characteristic that is highly desirable for multipoint networks. On the other side, LVDS drivers with transition times typically ranging from as low as 100 ps to only several 100 ps are rarely a good fit for any topology except a point-to-point topology.

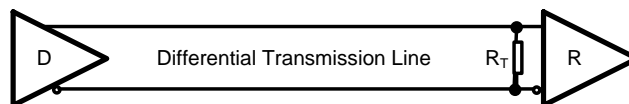


Figure 3. Point-to-Point Link

Table 1 shows a comparison of key RS-485, M-LVDS, and LVDS driver characteristics:

Table 1. Comparison of Key Driver Parameters

Parameter	RS-485	M-LVDS	LVDS
VOD (V)	1.5 to 5.0	0.48 to 0.65	0.25 to 0.45
VOS (V)	-1.0 to 3.0	0.3 to 2.1	1.125 to 1.375
IOD (mA)	28 to 93	9 to 13	2.5 to 4.5
IOS (mA)	<250	<43	<24
t_{RISE} / t_{FALL} Min (ns)	N/A	1	N/A
t_{RISE} / t_{FALL} Typ (ns)	5 to 50	1 to 5	<1
t_{RISE} / t_{FALL} Max (ns)	$0.3 t_{UI}$	$0.5 t_{UI}$	$0.3 t_{UI}$
Typ Data Rate (Mbps)	DC to 10	DC to 500	DC to 3125

3 Receiver Characteristics

The key receiver specifications are input voltage threshold, input common mode range, and input leakage current. The input threshold levels differentiate the two types of M-LVDS receivers. Type 1 receivers have threshold levels centered at 0V differential and provide higher noise margin than Type 2 receivers. Type 1 receivers are used in clock or data transmission applications that either require application specific external failsafe networks or don't require failsafe provisions at all. Type 2 receivers have threshold levels shifted by +100 mV differential. The shift lowers noise margin but provides a known, low output state when a bus or a transmission line is undriven and having 0V differential bias. In addition to the failsafe, Wired-OR function is another possible application of Type 2 receivers. More information about the Wired-OR implementation using M-LVDS devices is given later in the note.

When compared to RS-485 and LVDS receivers, M-LVDS receivers have the tightest threshold levels. [Figure 4](#) illustrates threshold levels and maximum recommended differential input amplitude levels of RS-485, LVDS, and both M-LVDS receivers.

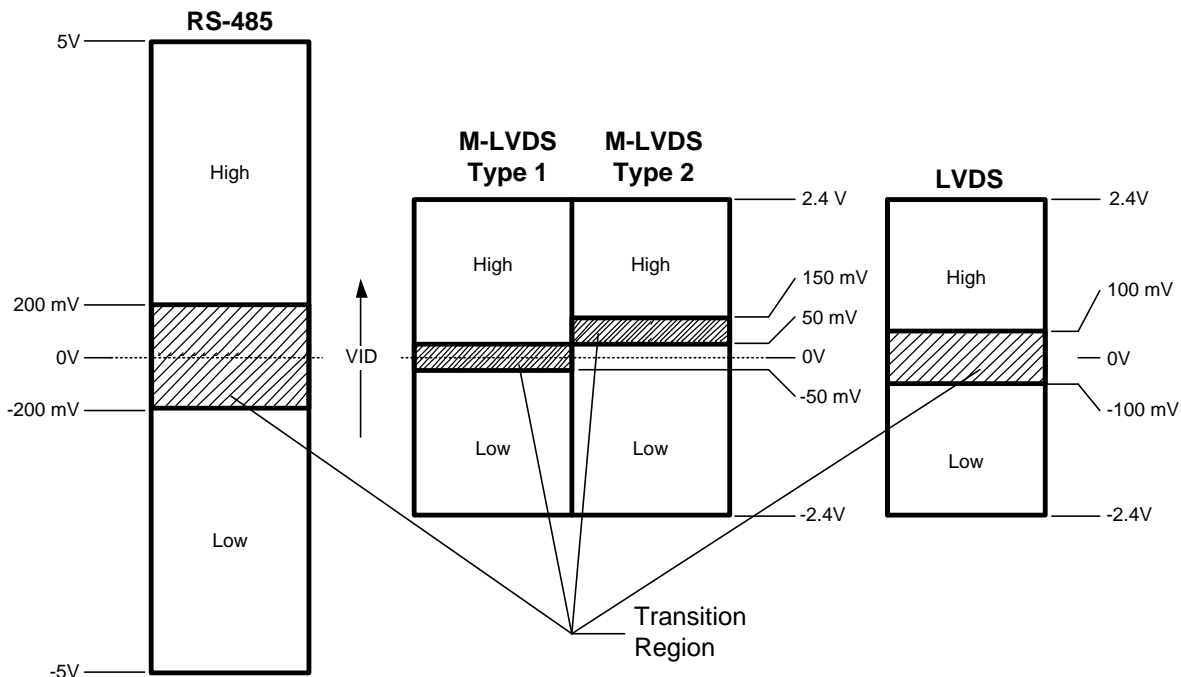


Figure 4. M-LVDS Standard Defines Two Receiver Types

The M-LVDS receiver input common mode range of -1.4V to 3.8V makes M-LVDS a robust interface for connecting sub-systems that may have a potential difference between their ground references of $\pm 1\text{V}$. Given the fact that many M-LVDS drivers have a much tighter VOS specification than what the standard specifies, the unwanted potential difference between network nodes may be greater than $\pm 1\text{V}$. RS-485 receivers are suitable for even harsher environments. Their common mode range of -7V to 12V allows for $\pm 7\text{V}$ of unwanted potential difference between the nodes. The LVDS receivers pose as the least robust receivers given their input common mode range of 0V to 2.4V (0 to V_{DD} is also very common), however, tight VOS specification of LVDS drivers allows a potential difference between driver and receiver circuit commons of $\pm 1\text{V}$.

As all M-LVDS, LVDS and RS-485 devices may be used in multipoint networks, the receivers have to pose as light loads to the active drivers so that many of them can be connected on a single bus. Based on this requirement, all three standards specify maximum input leakage current which allows up to 32 loads (receivers or inactive drivers) on a bus. A load of a single device or one unit load for M-LVDS and LVDS receivers is equivalent to a $120\text{ k}\Omega$ resistor into a 0V to 2.4V voltage source. One unit load for an RS-485 receiver is equivalent to a $12\text{ k}\Omega$ resistor into a 0V to 5V source. In addition, the RS-485 devices are available in $1/2$, $1/4$ and $1/8$ unit loads allowing up to 256 devices on a bus. [Table 2](#) shows key RS-485, M-LVDS and LVDS receiver characteristics.

Table 2. Comparison of Key Receiver Parameters

Parameter	RS-485	M-LVDS	LVDS
VID (V)	0.4 to 5.0	0.1 to 2.4	0.2 to 2.4
VCM (V)	-5.0 to 12.0	-1.4 to 3.8	0 to 2.4
IIN (μA)	<1000	<32	<20

4 M-LVDS Portfolio

TI's current M-LVDS product family consists of a wide array of devices ranging from single channel transceivers and driver/receiver pairs to quad channel transceivers, drivers and 1:4 repeaters/fan-out buffers.

The first generation of TI's M-LVDS devices introduced in 2006 includes four single channel devices providing 100 MHz / 200 Mbps transceivers and driver/receiver pairs with Type 1 and Type 2 receiver options. [Table 3](#) summarizes the available options. Detailed information on each device can be found at www.ti.com.

Table 3. Summary of the First Generation of TI's M-LVDS Devices

Part Number	Description	Package	Features
DS91D176	100 MHz Single Channel M-LVDS Transceiver	SOIC-8	`176 Pinout, Type 1 Receiver
DS91C176	100 MHz Single Channel M-LVDS Transceiver	SOIC-8	`176 Pinout, Type 2 Receiver
DS91D180	100 MHz Single Channel M-LVDS Line Driver / Receiver Pair	SOIC-8	`180 Pinout, Type 1 Receiver
DS91C180	100 MHz Single Channel M-LVDS Line Driver / Receiver Pair	SOIC-8	`180 Pinout, Type 2 Receiver

The first generation of M-LVDS devices features drivers with transition times (1.8 ns typ) optimized for multipoint networks, more specifically for ATCA clock distribution networks. In addition, the drivers feature output amplitude control circuitry that maintains constant VOD over a wide range of loads as illustrated in Figure 5. This feature helps with the noise margin in heavily loaded backplanes.

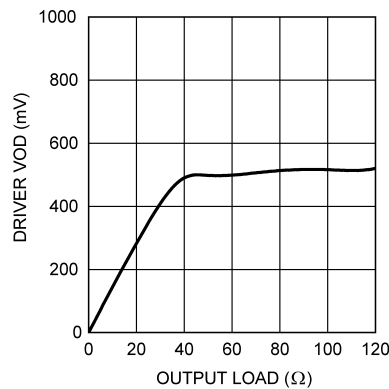


Figure 5. DS91D176 Driver Output Amplitude as a Function of Output DC Load

The second generation of M-LVDS devices introduced in 2008 includes four quad channel 125 MHz / 250 Mbps devices. Table 4 summarizes the available options. Similar to the first generation, these devices also feature controlled transition times (2.0 ns typ) and output amplitude control circuitry for maintaining constant VOD over a wide range of loads.

Table 4. Summary of the Second Generation of TI's M-LVDS Devices

Part Number	Description	Package	Features
DS91M040	125 MHz Quad M-LVDS Transceiver	LLP-32	Space saving package, pin settable receiver type, per channel output enable
DS91M047	125 MHz Quad M-LVDS Line Driver	SOIC-16	'047 pinout, per channel output enable
DS91M124	125 MHz 1:4 M-LVDS Repeater with LVCMOS Input	SOIC-16	Low skew, per channel output enable
DS91M125	125 MHz 1:4 M-LVDS Repeater with LVDS Input	SOIC-16	LVDS input, per channel output enable

5 M-LVDS Applications

M-LVDS devices are primarily used in clock distribution networks such as clock distribution interfaces of AdvancedTCA (ATCA) and MicroTCA (μTCA) based systems. However, the long list of features that M-LVDS devices bring, make them ideal for many other applications that can benefit from high-speed, low power, reduced EMI, controlled transition times and failsafe provisions. This section of the application note provides a brief overview of common M-LVDS applications.

6 Clock Distribution in AdvancedTCA Systems

AdvancedTCA is PCI Industrial Computer Manufacturers Group's (PICMG) open standard for modular communications systems with capacity of up to 2.5 Tbps. The standard specifies a range of system level design aspects and parameters including mechanical dimensions, power distribution, thermal considerations and data transport.

As in many communication systems, AdvancedTCA (ATCA) based systems require synchronization of its internal and external networks. Synchronization Clock Interface is a section of the ATCA Base Specification (PICMG 3.0) that specifies M-LVDS as the signalling technology of choice. In an ATCA system, there are three redundant clocks (totaling 6) distributed to up to 16 backplane slots in a multipoint fashion:

- CLK1A and CLK1B are for redundant 8 kHz standard digital telephony transmission system clocks.

- CLK2A and CLK2B are for 19.44 MHz clocks for synchronization of the SONET/SDH networks.
- CLK3A and CLK3B are for user-defined signals (clock or data).

Each ATCA clock network consists of up to 16 M-LVDS ports connected to a common clock bus as illustrated in Figure 6. The clock bus, physically located on the standard backplane, is a 130Ω differential microstrip terminated on both sides with 80Ω resistors. An M-LVDS port is an I/O of a M-LVDS device located on a line card. An interconnect that connects an M-LVDS port to a clock bus is referred to as unterminated stub. A stub in a standard ATCA clock distribution multipoint network consists of a differential trace connecting the M-LVDS device's I/O pins to the line card's standard Zone 2 connector pins and the connector's conductors. The standard ATCA Zone 2 connectors are Advanced Differential Fabric (ADF) connectors such as Tyco's HM-Zd connectors. Minimizing electrical length of stubs in ATCA clock distribution networks is critical and is discussed later in the design guidelines. The ATCA standard specifies 1 inch (25.4 mm) as the maximum stub length.

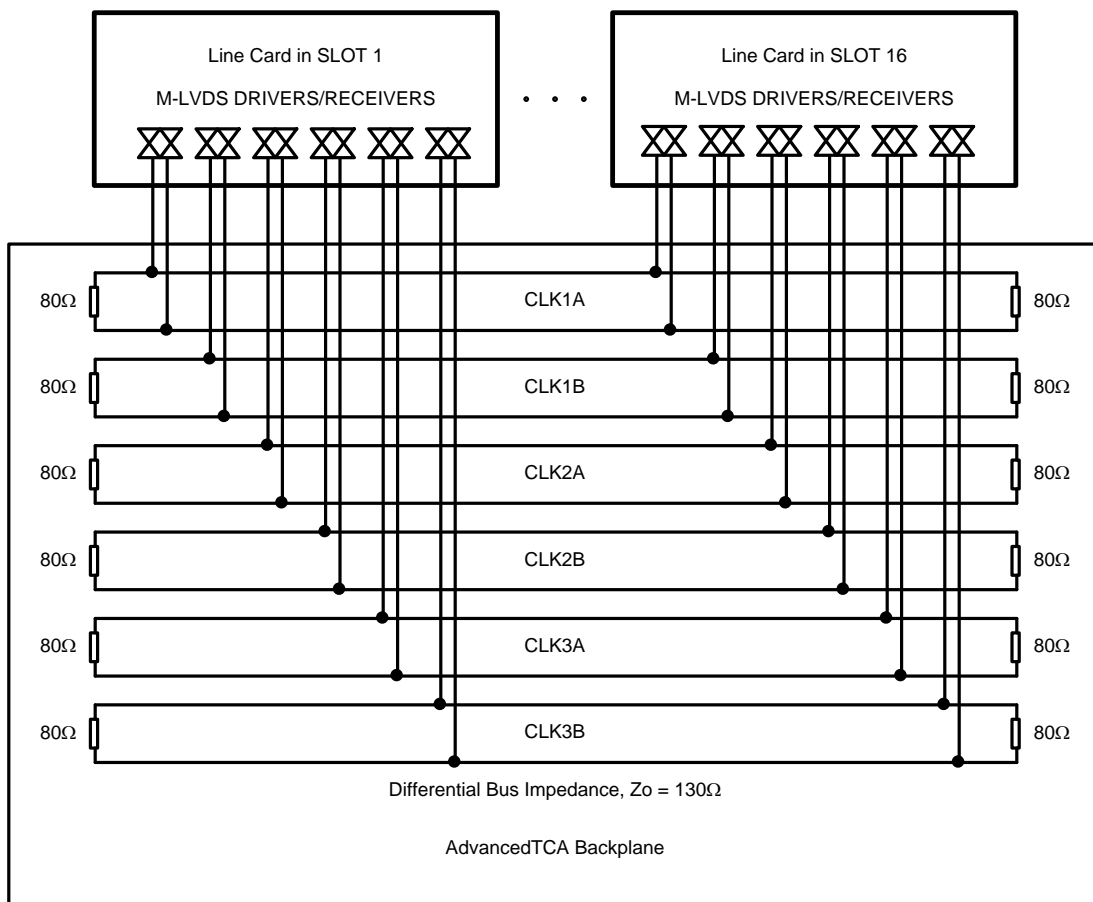


Figure 6. AdvancedTCA Clock Distribution Interface Example

7 Clock Distribution in MicroTCA Systems

MicroTCA standard provides a modular, open platform for Low to Mid-range telecom and datacom equipment with capacity of up to 144 Gbps. MicroTCA systems are optimized for smaller physical sizes and more cost sensitive applications.

Similar to the ATCA standard, the MicroTCA (uTCA) standard also specifies the use of M-LVDS technology for clock distribution networks. The MicroTCA specification (PICMG MTCA.0) defines non-redundant and redundant clocking architectures. The non-redundant clocking architecture is for systems with a single MicroTCA Carrier Hub (MCH). This architecture allows up to three point-to-point links per Advanced Mezzanine Card (AMC) and up to 36 links per MCH. Figure 7 shows a single point-to-point clock link between a MCH and AMC in a non-redundant backplane. Note that the clock bus is terminated on the backplane at the MCH card and on the AMC card. In point-to-point links, M-LVDS device transmit clock signals with maximum noise margin.

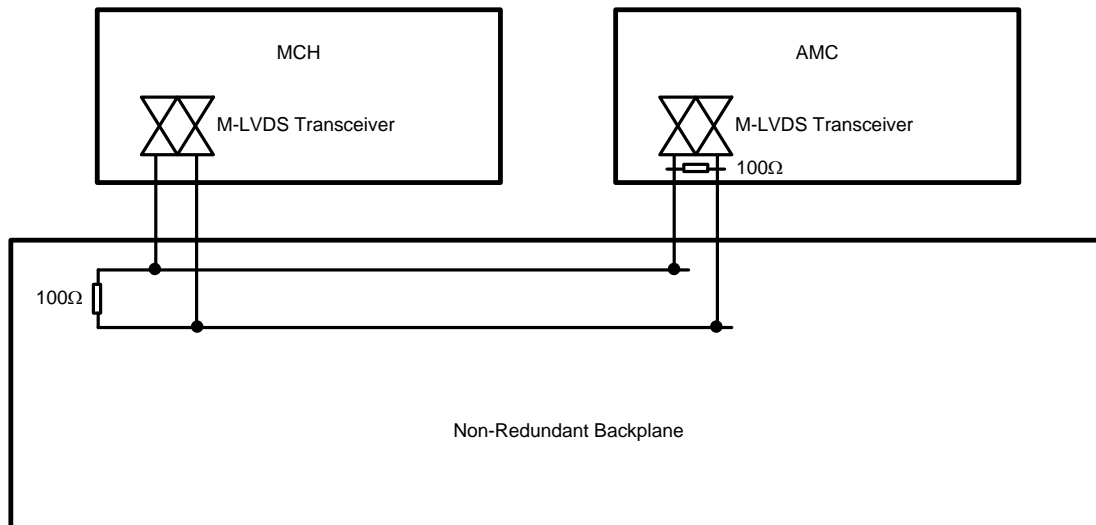


Figure 7. MicroTCA Non-redundant Clock Distribution Interface Example

The redundant clock architecture is for dual MCH systems that operate in a redundant manner. In this clock architecture, each MCH connects to each AMC cards with a point-to-point link as in Figure 7. However, the connection between an AMC to each of the MCH cards is implemented with a multipoint network as illustrated in Figure 8. The effects of unterminated stubs in this multipoint topology variant are minimized with the use of series resistors. The controlled signal edges of M-LVDS devices further aid in distributing clocks to all cards within a system.

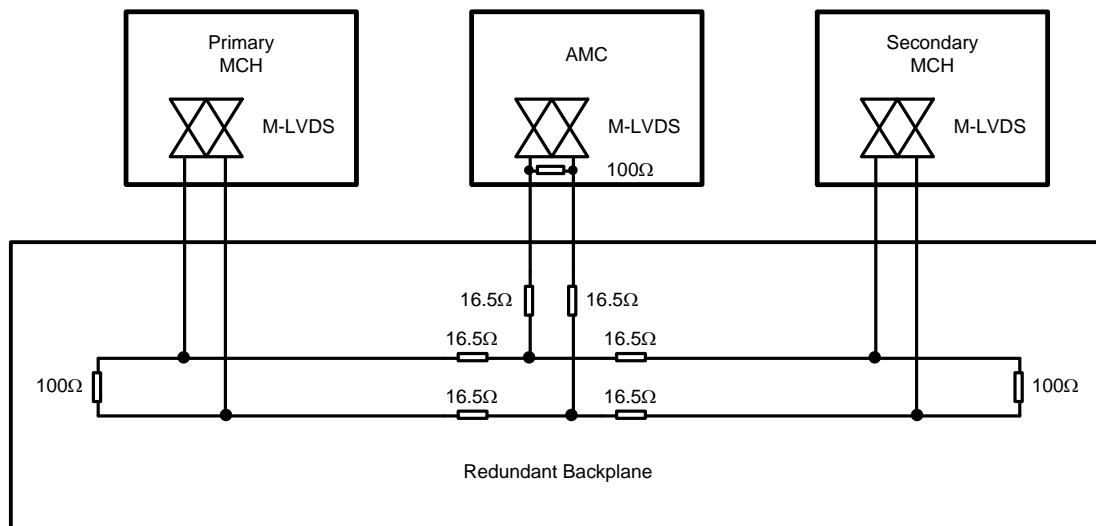


Figure 8. MicroTCA Redundant Clock Distribution Interface Example

8 M-LVDS as a Short Reach RS-485 Alternative

While RS-485 multipoint differential busses are long reach and typically implemented with cables as transmission media, M-LVDS devices have found applications in backplane environments. Multipoint links that utilize cables as interconnects are possible with M-LVDS as well. However, system designers need to pay extra attention to stub lengths, bus impedance, and potential differences between nodes. Making stubs as short as possible, spacing the loads evenly, and ensuring less than $\pm 1V$ of potential difference between the nodes enables robust designs of M-LVDS multipoint networks outside the backplane arena.

Another common application space that RS-485 and M-LVDS interfaces share is a point-to-point signal transmission over cables. When it comes to driving signals over long cables, a larger swing of RS-485 and especially wider input common mode range do help to achieve longer transmission distances; however, M-LVDS devices have the advantages of higher speed, lower power consumption and lower EMI. These key M-LVDS characteristics are beneficial in many applications.

Figure 9 shows a typical CAT5e cable length as a function of bit rate for the RS-485 and M-LVDS point-to-point links. The sloped portion of the RS-485 curves is determined based on the maximum attenuation of 9 dB at the frequency of $1/t_{UI}$ in hertz, where t_{UI} is a unit interval at a given signaling rate. This is an accepted industry guideline for determining maximum signaling rate for the RS-485 point-to-point links. The flat portion of the RS-485 curve is based on the ohmic loss of a typical CAT5e cable ($9\Omega / 100m$).

For networks that use low voltage differential drivers (M-LVDS, LVDS), the maximum attenuation of 6 dB at $1/t_{UI}$ hertz may be used as a general guideline when determining maximum signaling rate for a given cable length. The guideline assumes dc-balanced data, point-to-point links, zero crosstalk and pair-to-pair skew, and no external interference. Note the dashed portion of the M-LVDS curve. In theory, M-LVDS interfaces can transmit sub-Mbps signals over hundreds of meters of CAT5e cable, however, M-LVDS receivers can only handle $\pm 1V$ of ground noise. System designers building M-LVDS interfaces over long cables need to ensure that the ground noise does not exceed the $\pm 1V$ limit or they need to fully eliminate the DC component of signals by implementing either AC-coupled or transformer-coupled interfaces.

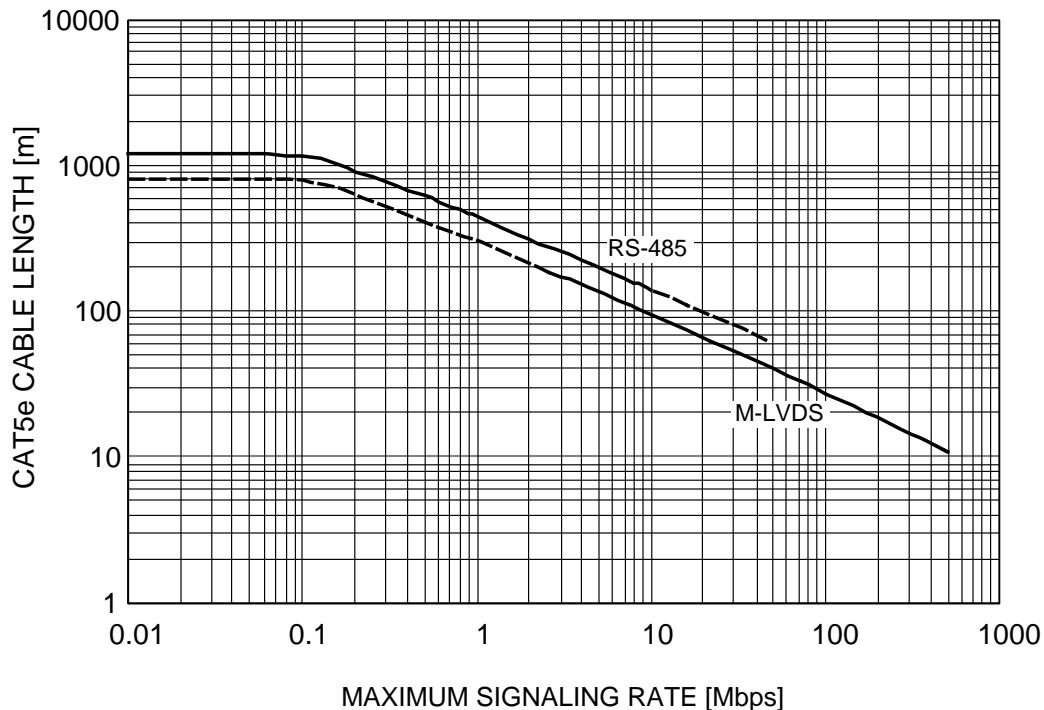


Figure 9. CAT5e Length as a Function of Bit Rate for M-LVDS and RS-485 Point-to-Point Links

9 Signal Distribution with Point-to-Point Links

Among many other benefits, signal distribution with multipoint networks reduces connector size and cable diameter, lowers conductor count and PCB thickness, and ultimately decreases system cost. These benefits come at the cost of signal integrity, maximum transmission reach and speed. When satisfactory signal integrity, transmission reach or speed using multipoint networks cannot be achieved, signal distribution with point-to-point links may be the only option. Signal distribution with point-to-point links is accomplished using fan-out buffers as illustrated in Figure 10.

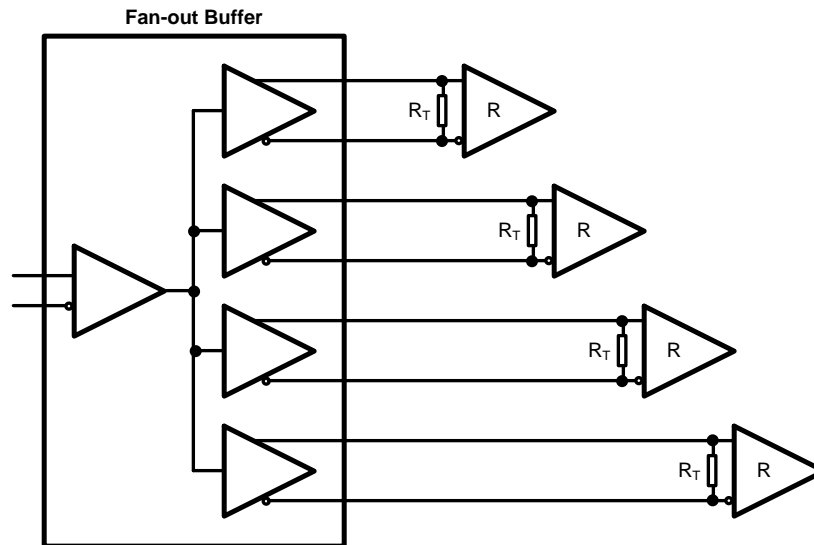


Figure 10. Signal Distribution with Point-to-Point Links

The current M-LVDS portfolio offers two 1:4 fan-out buffers/signal repeaters: DS91M124 and DS91M125.

The DS91M124 is the fan-out buffer with an LVCMOS input and four M-LVDS outputs. It provides LVCMOS-to-M-LVDS level translation and 1:4 signal distribution. It is best suited for taking an LVCMOS signal from a local signal source and distributing it to local or remote M-LVDS receivers.

The DS91M125 is the fan-out buffer with an LVDS input and four M-LVDS outputs. It can take an LVDS compatible signal from a local or remote source via a point-to-point or multidrop link and distribute it to four local or remote M-LVDS receivers or M-LVDS multipoint networks.

In addition to M-LVDS fan-out buffer, there are also several LVDS and Bus LVDS fan-out buffers. Table 5 provides the summary.

Table 5. Summary of the TI's Fan-out Buffers

Part Number	Description	Package	Features
DS91M124	125 MHz 1:4 M-LVDS Repeater with LVCMOS Input	SOIC-16	Low skew, per channel output enable
DS91M125	125 MHz 1:4 M-LVDS Repeater with LVDS Input	SOIC-16	LVDS input, per channel output enable
DS92CK16	125 MHz Bus LVDS 1:6 Clock Buffer/Bus Transceiver	TSSOP-24	1:6 LVCMOS Outputs, Bus LVDS I/O
DS90LV110T	1:10 LVDS Clock / Data Distributor	TSSOP-28	200 MHz / 400 Mbps Operation, Low Skew
DS90LV110AT	1:10 LVDS Clock / Data Distributor with Failsafe	TSSOP-28	Failsafe Operation
DS10BR254	1.5 Gbps 2:4 LVDS Repeater	LLP-40	LOS, 8 kV ESD
DS25BR204	3.125 Gbps 2:4 LVDS Repeater, with Transmit Pre-emphasis and Receive Equalization	LLP-40	Input Equalization, Output Pre-emphasis, LOS

10 Wired-OR Implementation

M-LVDS drivers and Type 2 receivers can be used to implement Wired-OR logic function. [Figure 11](#) illustrates an example of the implementation using three M-LVDS drivers and a single Type 2 receiver interconnected with a doubly terminated multipoint bus. All driver inputs are set to H while driver output enable (DE) pins serve as inputs. The receiver output serves as an output of the function. When disabled, the drivers outputs provide a 0V differential bias to the bus and the Type 2 receiver detects a logic L. When any of the drivers is enabled, the bus is biased to a H and the receiver detect a logic H.

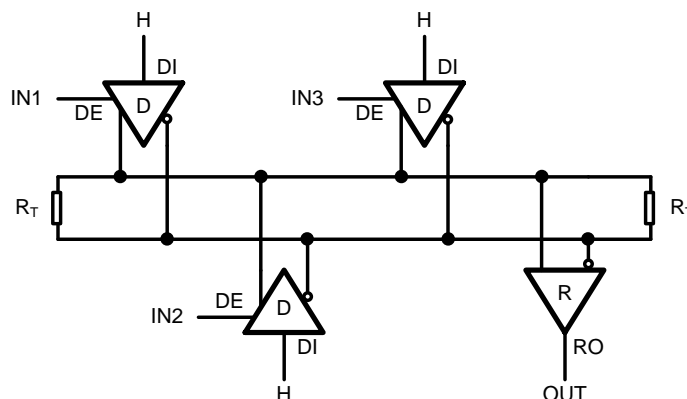


Figure 11. Wired-OR Circuit with Three M-LVDS Drivers and One Type 2 Receiver

11 Design Guidelines

Multipoint networks provide designers with an economical and simple method to interface multiple devices using a single interconnect or a bus. While simplicity and low cost make multipoint networks appealing for many, designing these networks is never a straightforward task. The following list provides design guidelines for implementing reliable M-LVDS multipoint networks.

- Design or select interconnects that are optimal for multipoint networks. In a multipoint network, each port presents a load to the bus. The loads are typically capacitive consisting of M-LVDS I/O capacitance and intrinsic capacitance of the stubs. A capacitive load on a bus with uniform impedance lowers the impedance of the bus at the port location and creates impedance mismatches. When multiple loads are connected on a bus with relatively uniform spacing between the loads, the overall characteristic impedance of the bus becomes lower. Lower characteristic impedance of the bus requires lower value termination resistors. Lower value termination resistors mean lower DC load for a signal driver and ultimately lower signal amplitude. Even though the M-LVDS drivers feature control circuitry that keeps output amplitude constant, the output amplitude is only constant for a load of 40Ω or higher. This means that the differential characteristic impedance of the loaded bus needs to be 80Ω or higher. To achieve this, select or design a bus with higher than nominal (100Ω differential) characteristic impedance so that its impedance does not go below 80Ω when fully loaded.
- Select M-LVDS drivers with the slowest transition time that will satisfy the bandwidth requirements of the system. Drivers that have transition times of one half of the unit interval (UI) at the bit rate of interest provide the highest noise margin. For example, the M-LVDS drivers have typical transition times of 2 ns. This makes them ideal for operation at 250 Mbps/125 MHz (4 ns UI). At 250 Mbps, any reflections that may occur in the bus have energy that is only at the frequencies that are multiples of the Nyquist frequency (125 MHz). With this distribution of the signal energy, reflections that have energy at the frequencies that are higher than the Nyquist frequency are absent. The reflections that have energy at frequencies higher than the Nyquist frequency are a serious threat to signal distribution in multipoint networks.
- Minimize the length of stubs as much as possible. M-LVDS devices are typically fine with stubs that are 1 inch (2.5 cm) or shorter (Connector electrical length should be considered when determining the total stub length). Anything longer than that may cause a system to fail. Experimental data presented in the application note AN-1503 has shown that shortening the stubs from 1 to 1/2 inches may increase noise margin by as much as 50%. In addition, when noise margin is at premium, one should consider maximizing the stub impedance. This can be accomplished by increasing the dielectric thickness of the

material, reducing the stub width, and uncoupling or loosely coupling the individual traces of the stub.

- Place M-LVDS drivers next to termination resistors provided other system constraints allow it. The worst driver location is in the middle of a multipoint network; the receivers adjacent to the driver always have the worst noise margin. By placing the drivers at one end of the network close to one of the two termination resistors, network topologies with longer signal paths are created. The longer signal paths have more loss and as result increase transition times of the signal as it propagates from the driver toward the furthest receiver. Slower transition times are more “forgiving” when encountering impedance discontinuities.
- Any power supply noise reduces available noise margin. Ensure that M-LVDS devices are properly decoupled. Each V_{DD} or GND pin of an M-LVDS device should be connected to a printed circuit board (PCB) through a low inductance path. For best results, one or more vias should be used to connect a V_{DD} or GND pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding intrinsic trace inductance. Bypass capacitors should be placed close to V_{DD} pins. Small physical size capacitors, such as 0402, X7R, surface mount capacitors should be used to minimize package inductance of capacitors. Each bypass capacitor should be connected to the power and ground planes through vias tangent to the pads of the capacitor. An X7R surface mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values such as 100 pF, 1 nF, 0.03 μ F, and 0.1 μ F are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2–3 mils. With a 2 mil FR-4 dielectric, there is approximately 500 pF per square inch of a PCB. For devices packaged in LLP packages (e.g. DS91M040), the die attach pad (DAP) should be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the LLP package.

12 Conclusion

M-LVDS is a versatile interface technology optimal for a range of applications including clock distribution systems in popular AdvancedTCA and MicroTCA backplanes. TI's current M-LVDS portfolio offers devices that bring all standard and some unique M-LVDS features to engineers looking to solve point-to-point and multipoint network challenges.

13 References

DS91M040 125 MHz Quad M-LVDS Transceiver ([SNLS283](#))

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